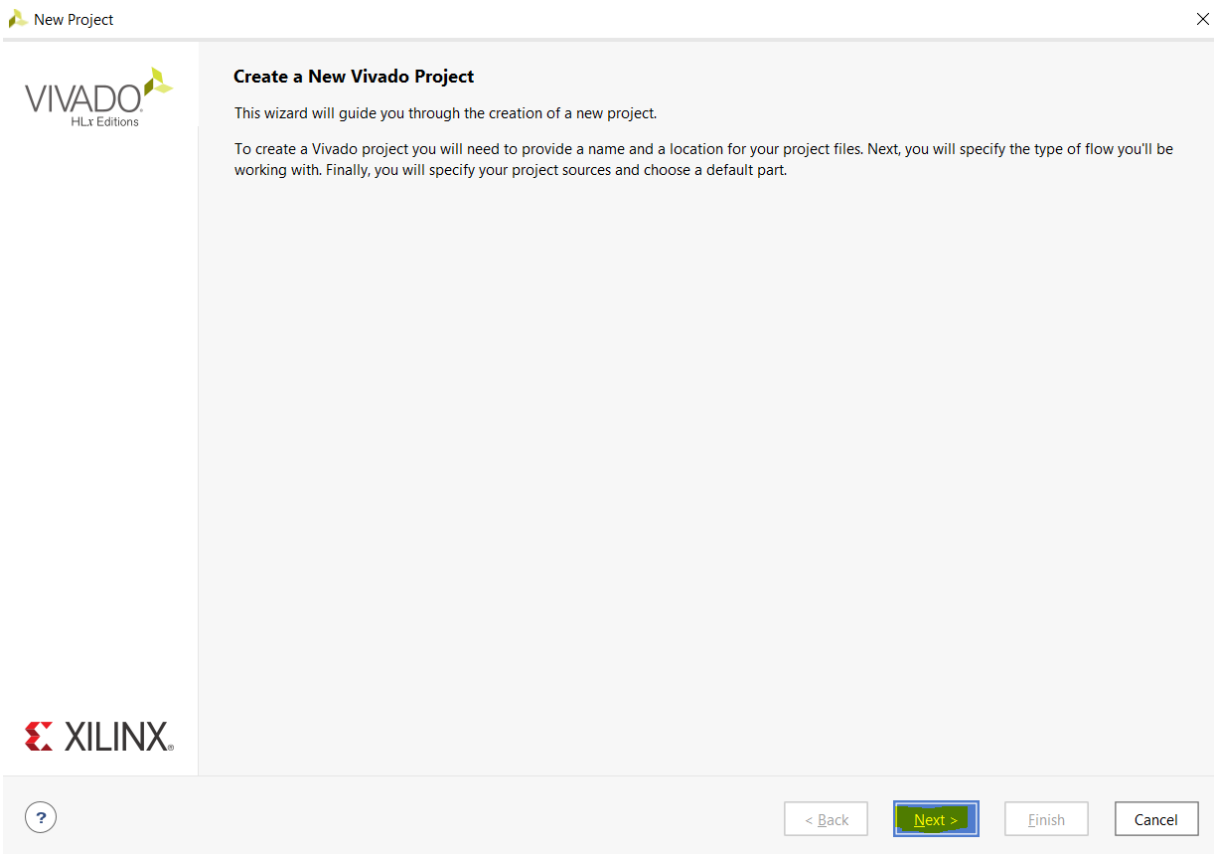
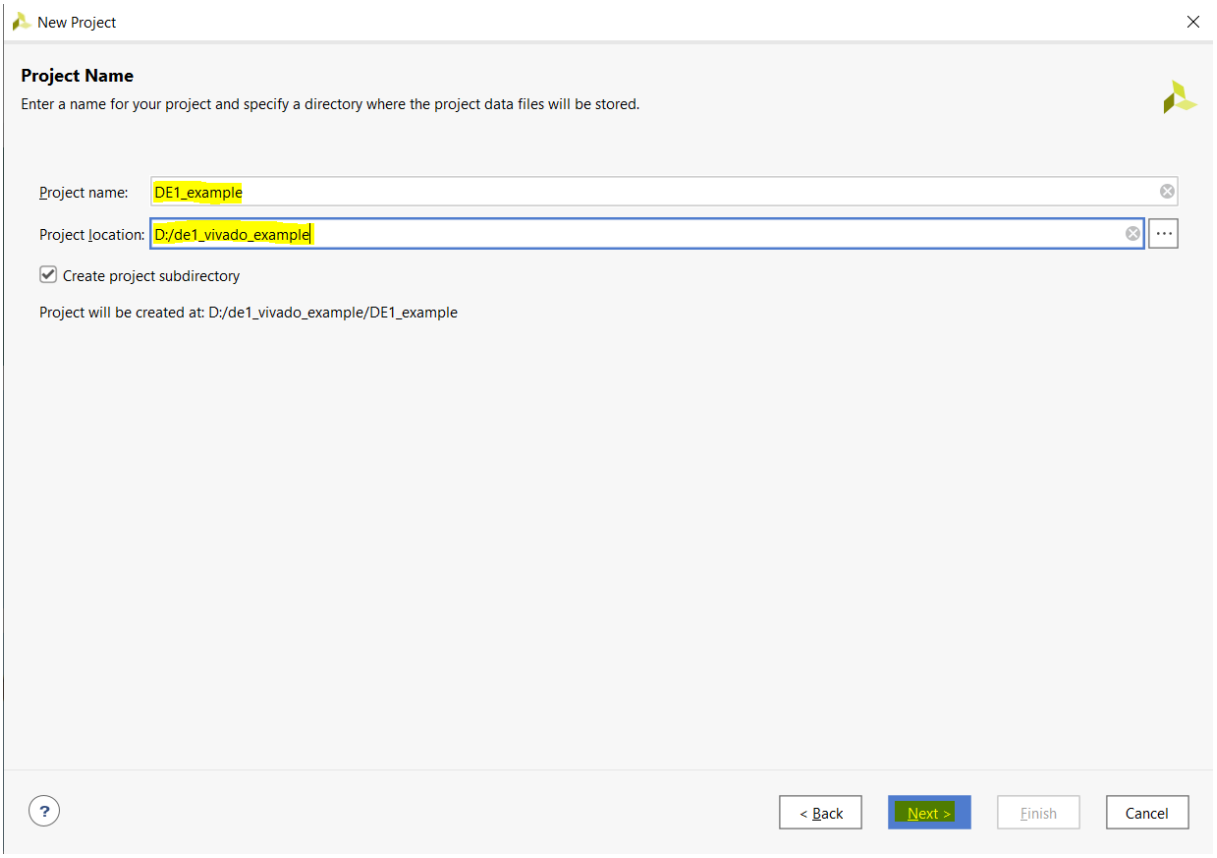
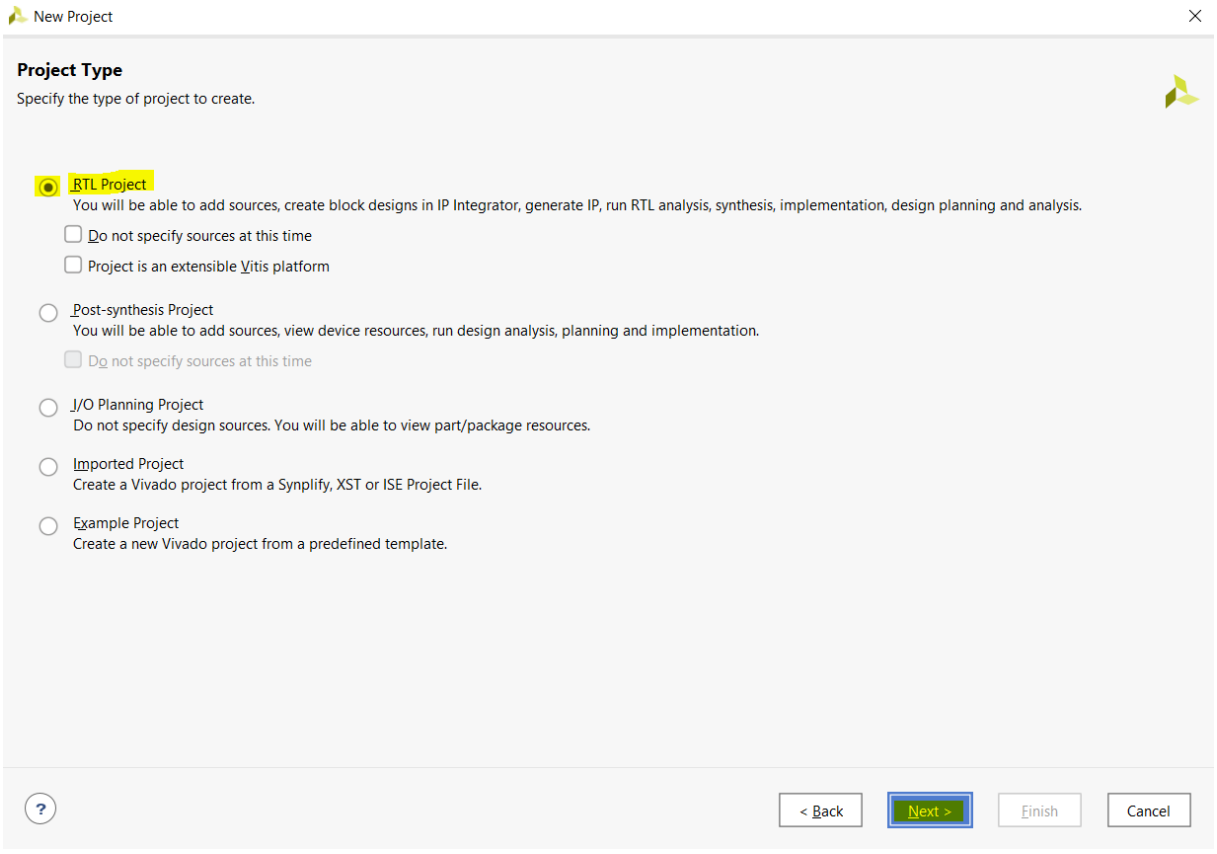
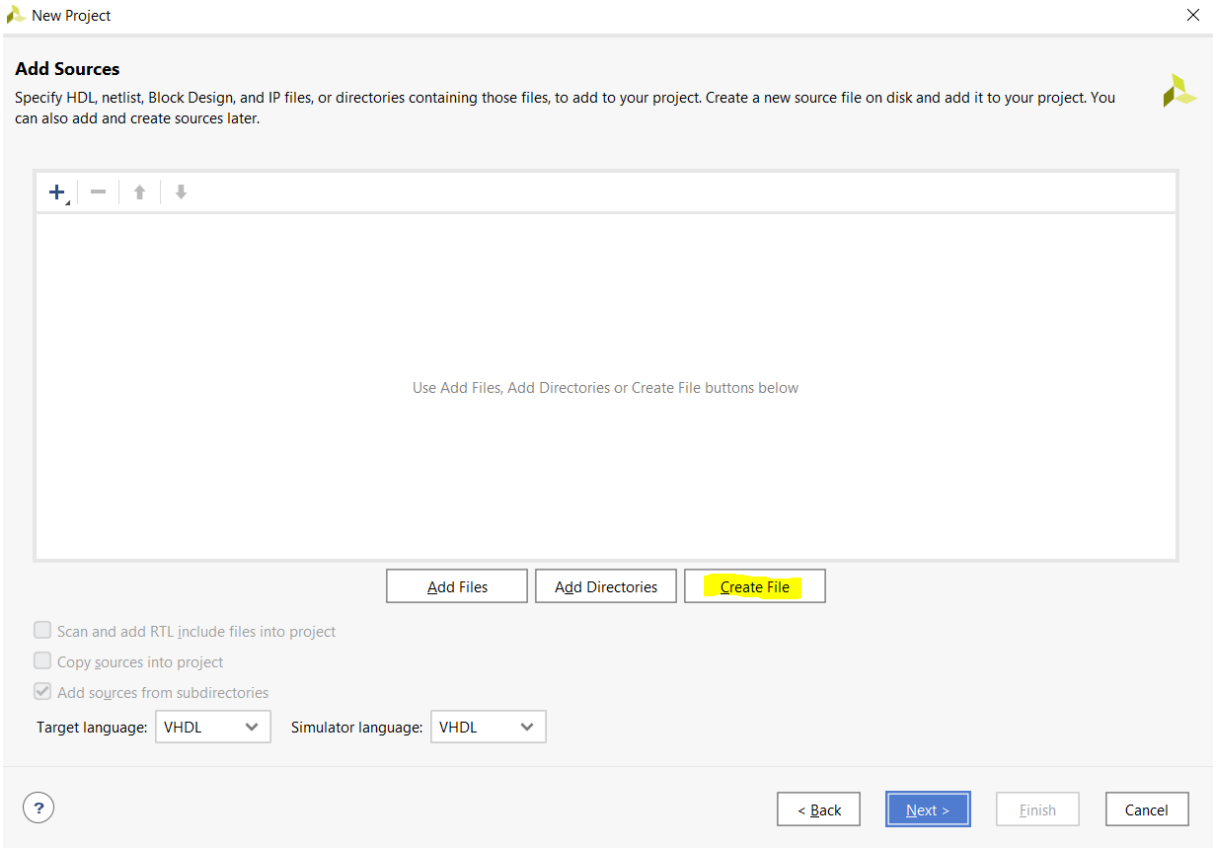
# Vivado Tutorial

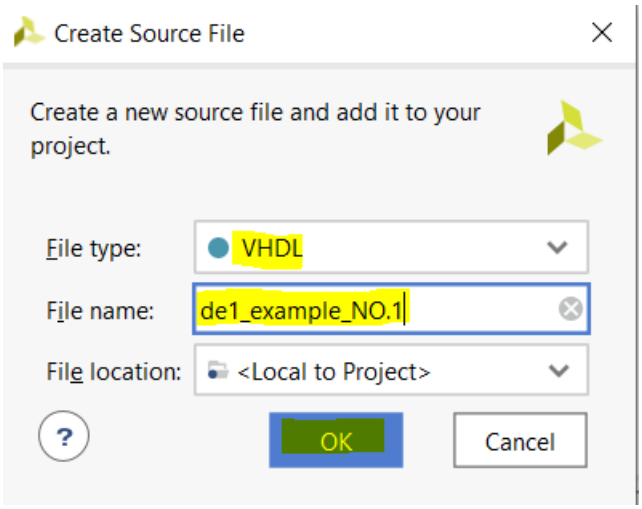
## Step1.: create a new project

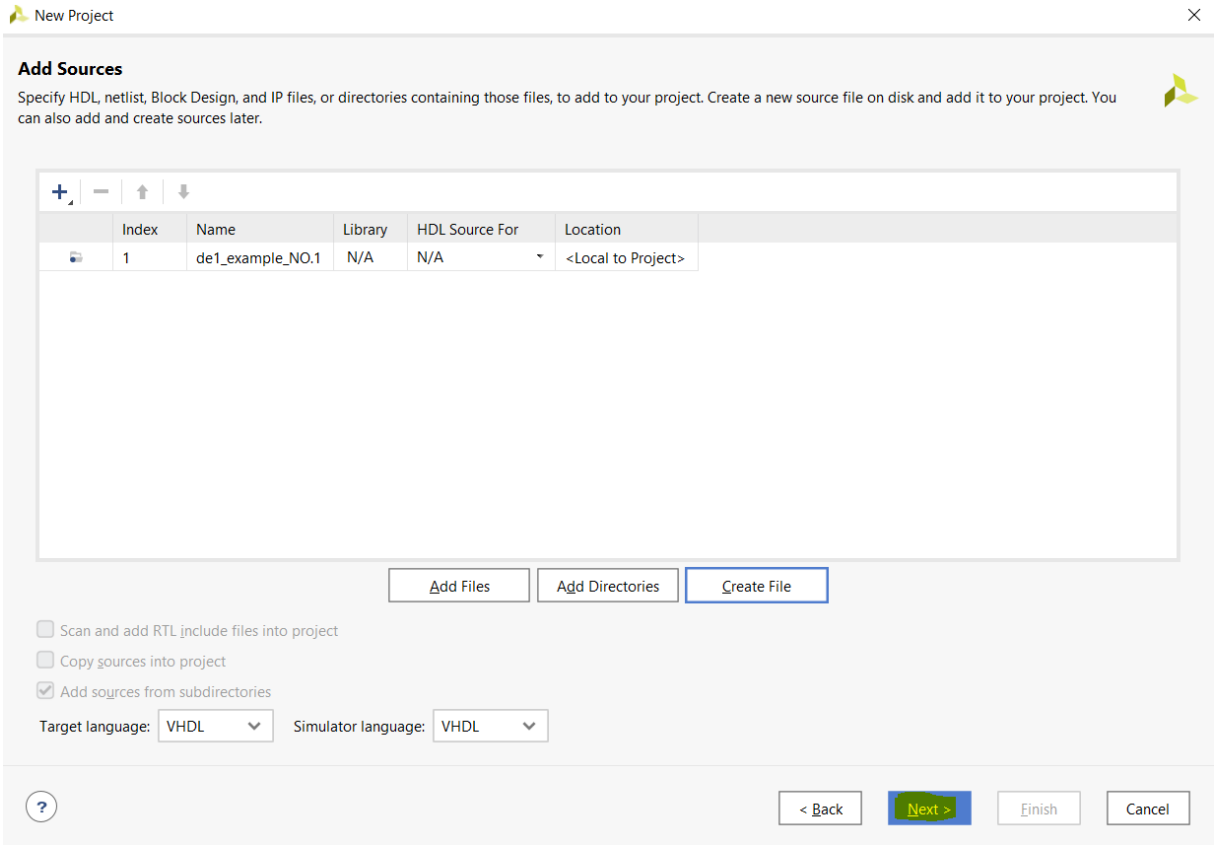



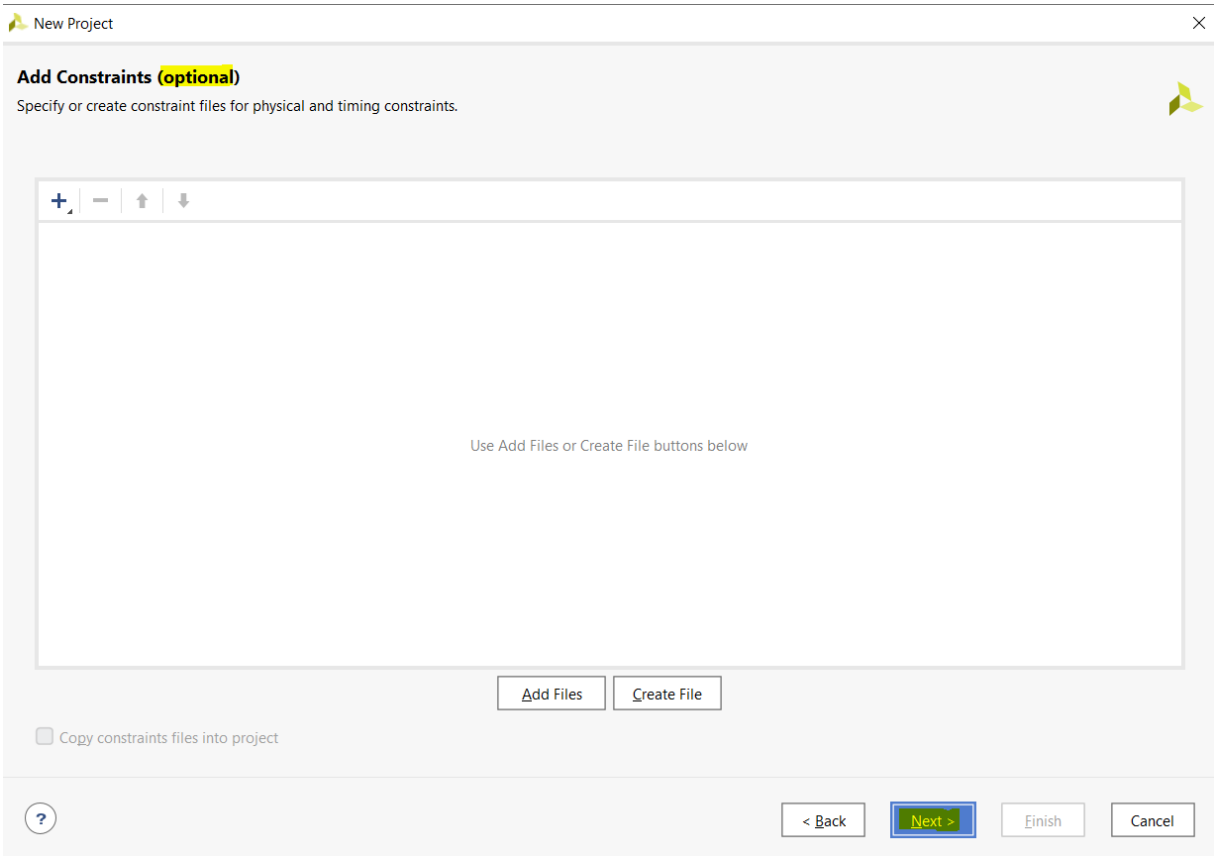

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name:
DE1_example
Project location:
D:/de1_vivado_example
Create project subdirectory
Project will be created at: D:/de1_vivado_example/DE1_example
< Back
Next >
Finish
Cancel


New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Project is an extensible Vitis platform
Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel


New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel


Create Source File
Create a new source file and add it to your project.
File type: VHDL
File name: de1_example_NO.1
File location: <Local to Project>
OK
Cancel


New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Index
Name
Library
HDL Source For
Location
1
de1_example_NO.1
N/A
N/A
<Local to Project>
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language:
VHDL
Simulator language:
VHDL
< Back
Next >
Finish
Cancel


New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel

New Project

## Default Part

Choose a default Xilinx part or board for your project.

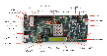
Parts | **Boards**

Reset All Filters

Install/Update Boards

Vendor: All  Name: All  Board Rev: Latest

Search:

| Display Name | Preview | Vendor | File Version | Part | I/O Pin Count | Board Rev | Available IOBs | LUT Elem |
|---|---|---|---|---|---|---|---|---|
| Nexys4 | | digilentinc.com | 1.1 | xc7a100tcsg324-1 | 324 | B.1 | 210 | 63400 |
| Nexys4 DDR | | digilentinc.com | 1.1 | xc7a100tcsg324-1 | 324 | C.1 | 210 | 63400 |
| Artix-7 AC701 Evaluation Platform<br>Add Companion Card Connections |  | xilinx.com | 1.4 | xc7a200tfbg676-2 | 676 | 1.1 | 400 | 134600 |
| Spartan-7 SP701 Evaluation Platform |  | xilinx.com | 1.0 | xc7s100fgga676-2 | 676 | 1.0 | 400 | 64000 |

< Back  Next >  Finish  Cancel

New Project

VIVADO HLx Editions

## New Project Summary

A new RTL project named 'DE1_example' will be created.

1 source file will be added.

No constraints files will be added. Use Add Sources to add them later.

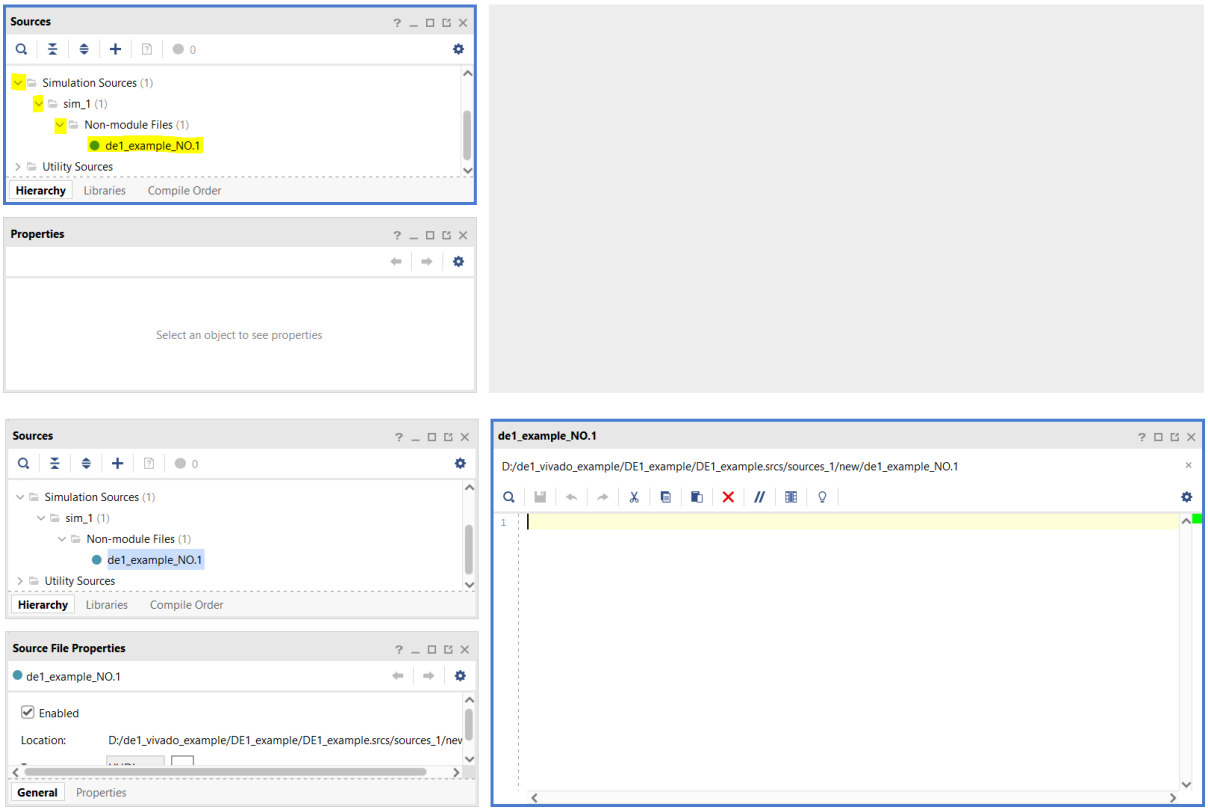
The default part and product family for the new project:
Default Part: xc7k70tfbv676-1
Product: Kintex-7
Family: Kintex-7
Package: fbv676
Speed Grade: -1

XILINX

To create the project, click Finish

< Back  Next >  Finish  Cancel

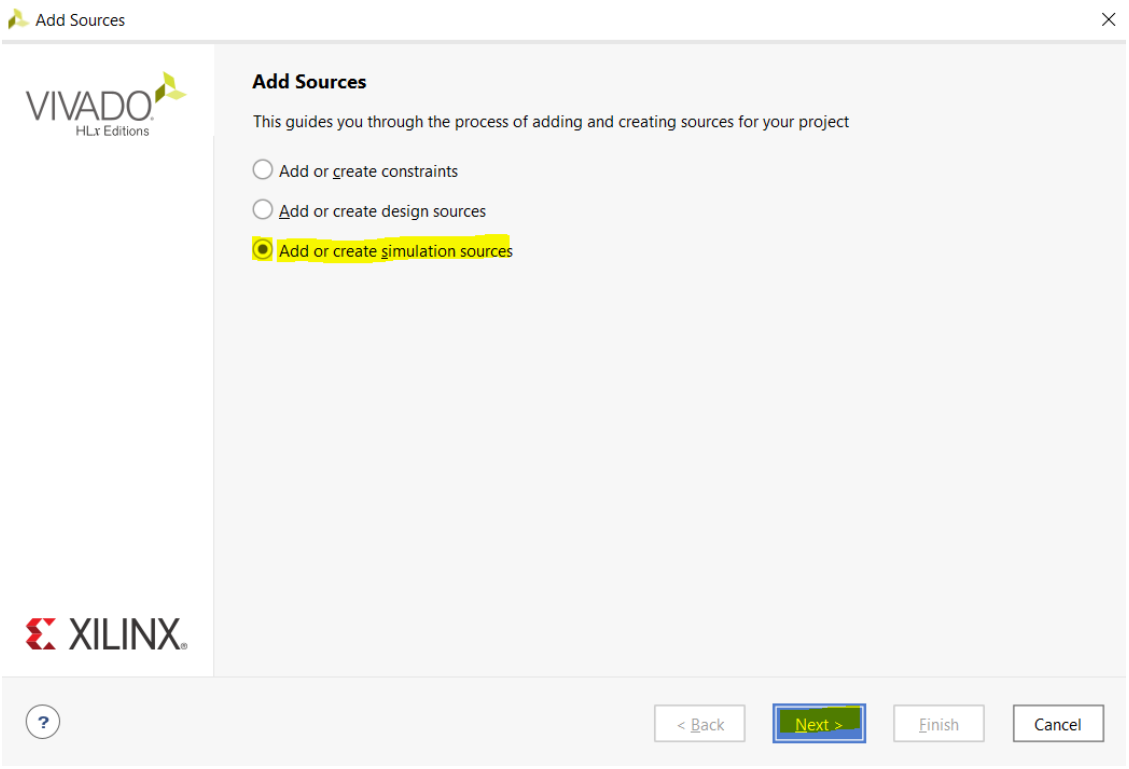
## Step2.: Writing Design/Testbench VHDL code

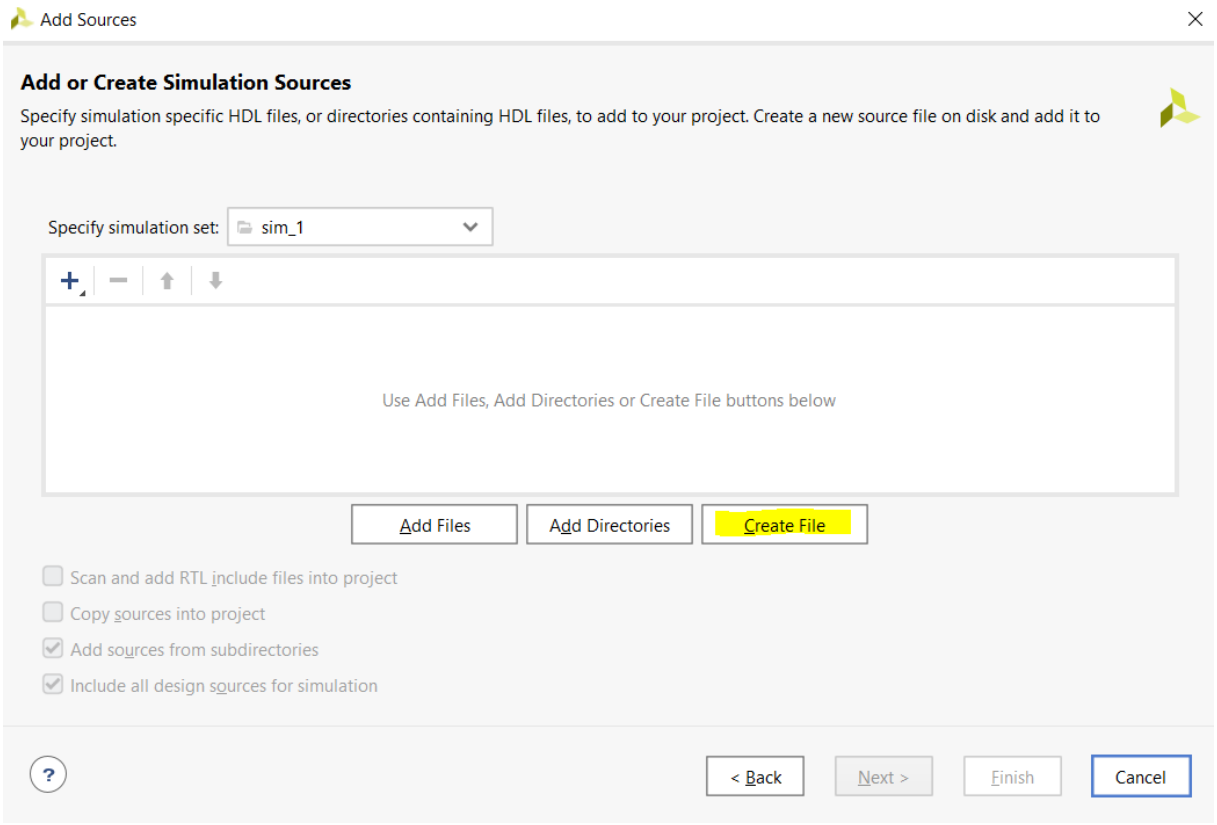


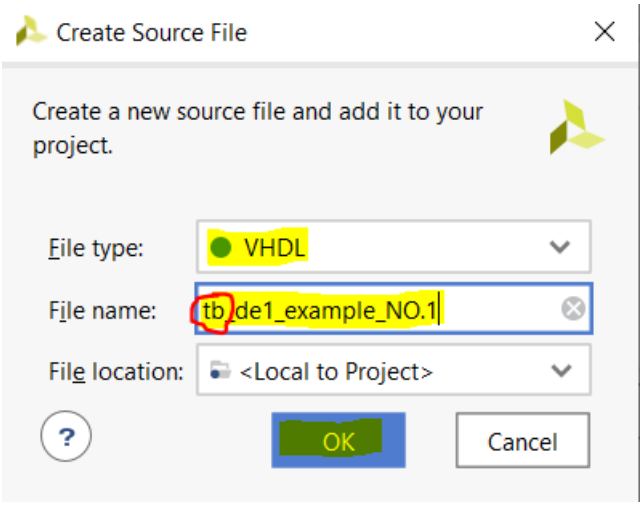

- now we can write VHDL code in the de1_example_NO.1

- when we are done with de1_example_NO.1 (design part), we can create our testbench

- press **ALT+A**




Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel


Create Source File
Create a new source file and add it to your project.
File type:
VHDL
File name:
tb_de1_example_NO.1
File location:
<Local to Project>
OK
Cancel

Add Sources

## Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

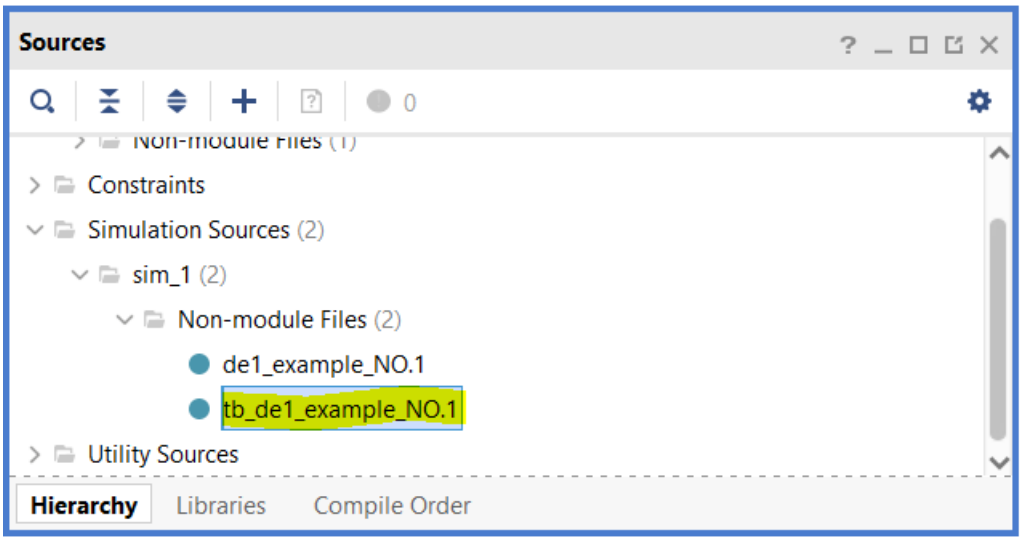
Specify simulation set: sim_1

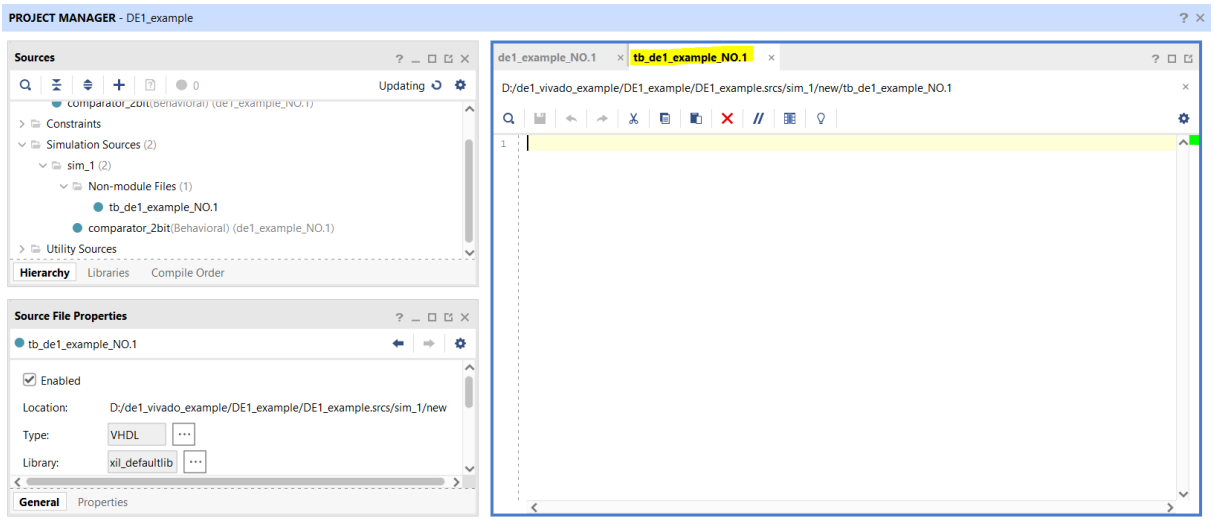
| | Index | Name | Library | Location |
|---|---|---|---|---|
| | 1 | tb_de1_example_NO.1 | N/A | <Local to Project> |

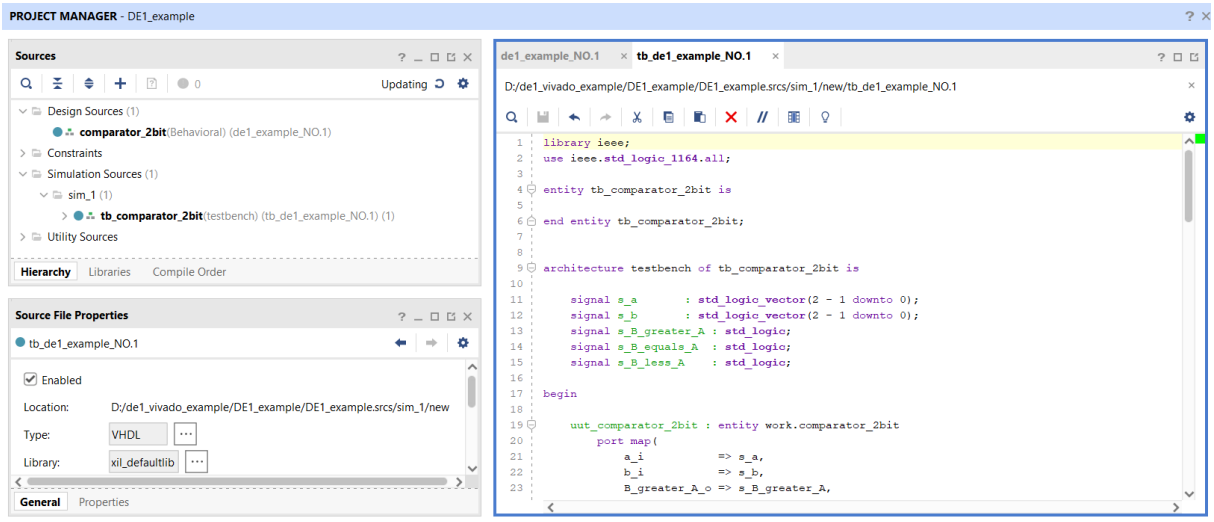
Add Files | Add Directories | Create File

- [ ] Scan and add RTL include files into project
- [ ] Copy sources into project
- [x] Add sources from subdirectories
- [x] Include all design sources for simulation

< Back | Next > | Finish | Cancel



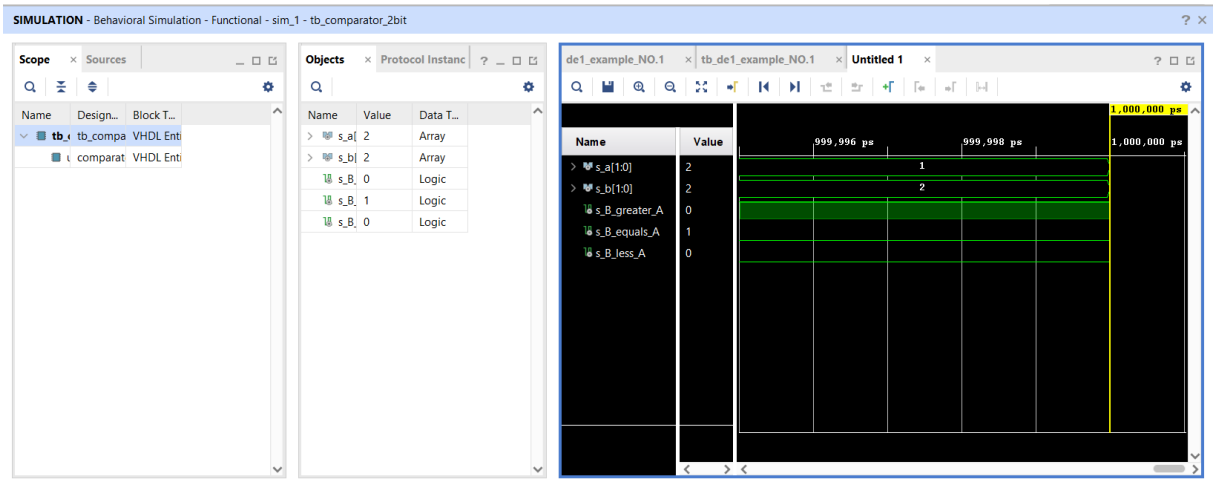


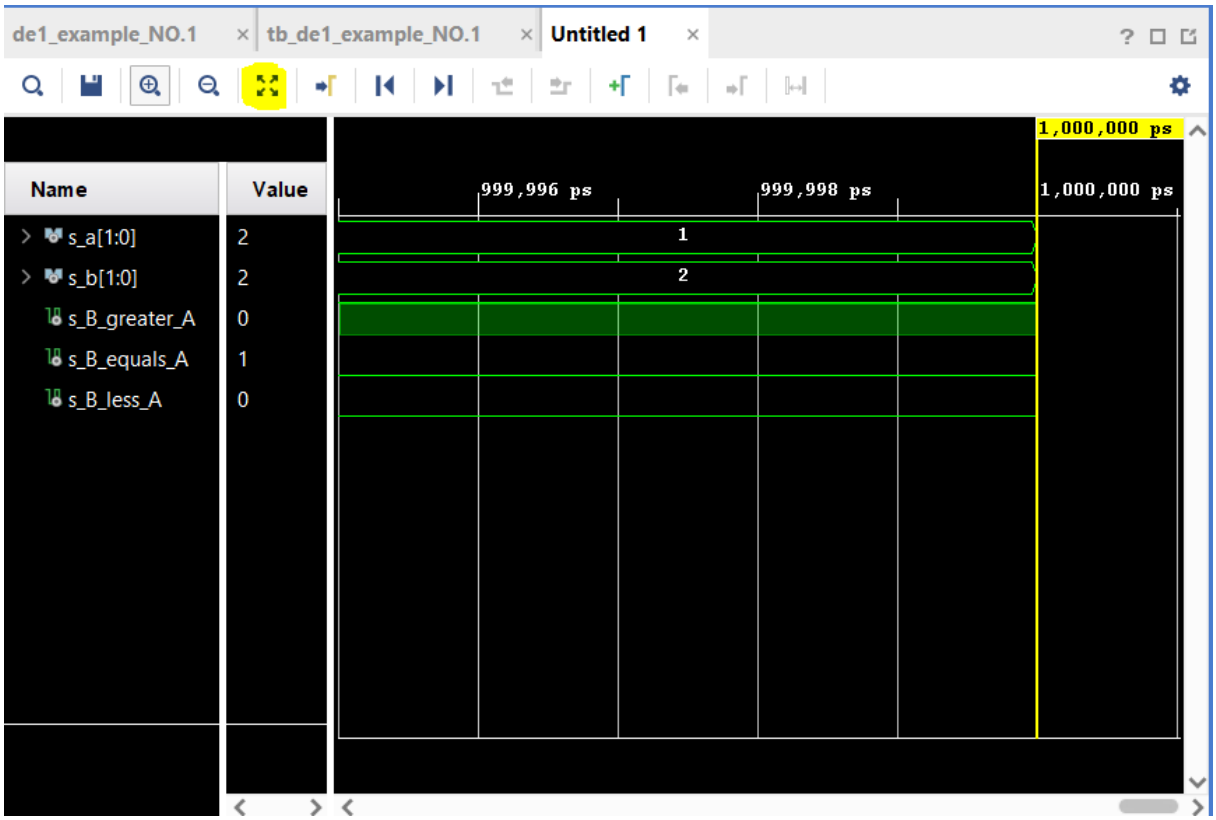



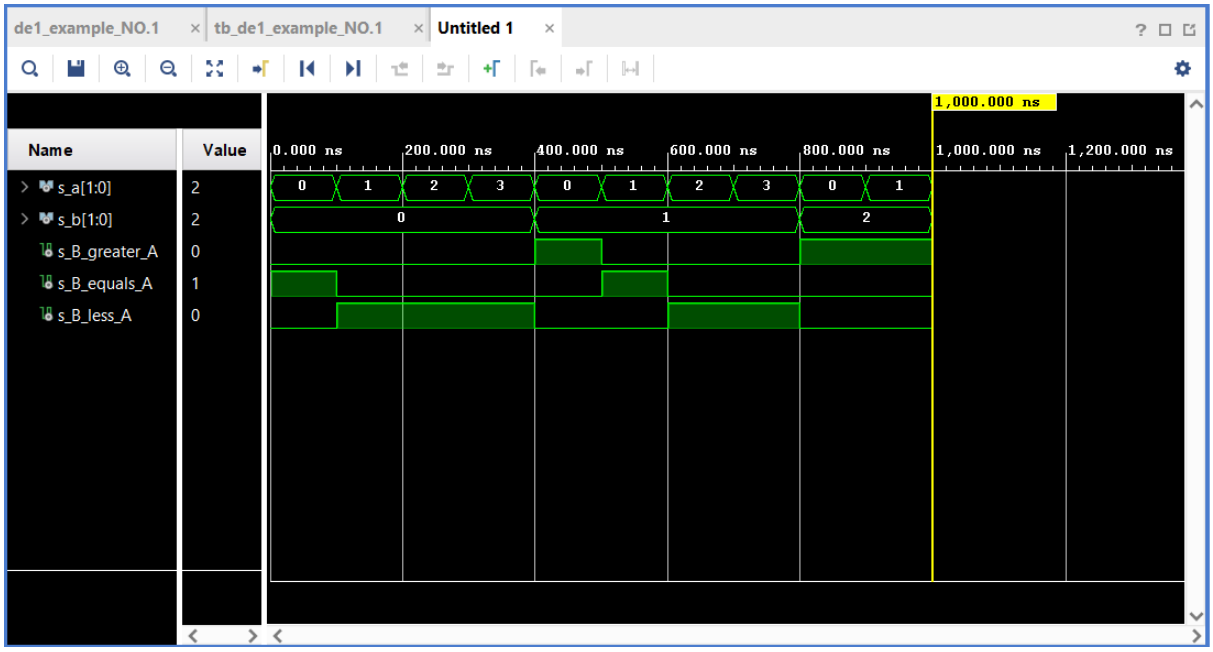

- after we are done with testbench, we can run simulation

Step 3.: Running the simulation

- go to Flow -> Run simulation -> Run Behavioral simulation




de1_example_NO.1
tb_de1_example_NO.1
Untitled 1
Name
Value
s_a[1:0]
2
s_b[1:0]
2
s_B_greater_A
0
s_B_equals_A
1
s_B_less_A
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,000.000 ns
0 1 2 3 0 1 2 3 0 1
0 1 2