	Signal Name	R-format	I-format (not lw)	lw	sw	beq
Inputs	I6	0	0	0	0	1
	I5	1	0	0	1	1
	I4	1	1	0	0	0
	I3	0	0	0	0	0
	I2	0	0	0	0	0
	I1	1	1	1	1	1
	I0	1	1	1	1	1
Outputs	MemtoReg	0	0	1	X	X
	RegWrite	1	1	1	0	0
	MemRead	0	0	1	0	0
	MemWrite	0	0	0	1	0
	Branch	0	0	0	0	1