

Jefferies

July 10, 2017

Semiconductors The 4th Tectonic Shift in Computing: To a Parallel Processing / IoT Model

Key Takeaway

Every 15 years the computing industry experiences a tectonic shift, which dramatically changes the computing model and competitive landscape. We believe we are at the start of a tectonic shift now, driven by low memory prices, improved parallel processors/software, and improved AI technologies like Neural Networks. We view NVDA, AMD, XLNX, CAVM, MXIM, TXN, ADI, MCHP as beneficiaries. We think INTC has the most to lose as the data center incumbent.

There Have Been 3 Tectonic Shifts in Computing. Every 15 years, an accumulation of technical innovations translates to tectonic shifts in the computing model. In the 60s the industry shifted from Mainframes to Mini-Computers, in the early 80s it shifted to PCs, and in the late 90s it shifted to a cell phone / datacenter model. Each computing model shift brought a shift in the beneficiaries: IBM in Mainframes to DEC in MiniComputers, to INTC/MSFT in PCs, to AAPL/Samsung/INTC/MSFT in the cell phone / datacenter model.

We Believe We are at the Start of the 4th Tectonic Shift Now, to a parallel processing / IoT model, driven by lower memory costs, free data storage, improvements in parallel processing hardware and software, and improvements in AI technologies like neural networking, that make it easy to monetize all the data that is being stored.

Those Architected for Parallel Best Positioned. Computing platforms historically relied on higher clock speeds in successive generations for improved platform performance. However Moore Stress is now at play, preventing higher clock speeds translating to higherand-higher processor core devices. We think those companies that have architected their hardware and software platforms from the ground up for parallel processing are best positioned to benefit - NVDA, XLNX, CAVM and AMD make that list.

NVDA Appears Best Positioned as the Leading Parallel Processing Platform. NVDA was the first to recognize and successfully invest in a HW/SW platform (GPU/CUDA) targeted specifically at parallel processing applications, and our field checks suggest it is years ahead of its competition.

We Also Like AMD, XLNX and CAVM as Parallel Processing Beneficiaries. With their own parallel processing platforms, we think AMD, XLNX and CAVM also benefit as the industry shifts to a parallel processing paradigm. We think the market is underestimating the longer term opportunity for these companies, and upgrade XLNX and CAVM to Buy in conjunction with this note.

We Favor MXIM, TXN, ADI, and MCHP as IoT Beneficiaries. As more companies figure out how to monetize data generated by IoT, we expect higher demand for these devices, which we expect benefits MXIM, TXN, ADI and MCHP.

INTC has the most to Lose as the Dominant Datacenter Processor Incumbent. With dominant market share in the datacenter, we think INTC has the most to lose as the industry shifts to a parallel processing / IoT model. While we don't expect INTC's DCG revenues to disappear or dramatically decline, we do believe that they continue their deceleration to the mid-single digit range for the next 12-24 months. We lower our rating on INTC to Underperform.

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^Prior trading day's closing price unless otherwise noted.

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There has been a tectonic shift in the computing industry about every 15 years

Today's cell phone is a descendant of the 1946 ENIAC, three tectonic shifts removed

Innovations in TTL-transistors led to a tectonic shift to Mini-Computers from Mainframes in the mid-'60s

Mainframes cost \$100,000s Mini-Computers cost \$10,000s

The tectonic shift to PCs from Mini-Computers was driven by both technical and business innovations

With the PC, computing ASPs declined another 10x into the \$1,000s, while units increased 100x into the 100s of millions

Faster air-interface standards and efficient centralized computing set up a tectonic shift to the Cell-Phone / Datacenter computing model

With the Cell-Phone, computing ASPs declined by 10x and units increased 10x vs the PC

Each tectonic shift in computing model brought a shift in beneficiaries:

- Mainframes -> IBM
- Mini-Computers -> DEC
- PCS -> MSFT + INTC
- Cellphone/Datacenter -> AAPL, MSFT+INTC

Tectonic Shifts in Computing

Previous Tectonic Shifts in Computing

Just about every 15 years over the past 60, the accumulation of innovations has caused tectonic shifts in the computing industry. Describing these shifts as tectonic makes sense to us because tectonic shifts can change the landscape to the point where it is not recognizable. Consider that today's computing device of choice, the cellphone, is actually a descendant of ENIAC, the first mainframe computer. The ENIAC was built in 1946 and comprised of 6,000 mechanical switches and 18,000 vacuum tubes. Its footprint was 2,000 square feet; it weighed 30 tons and cost \$500,000. Three tectonic shifts later, you carry your \$600 cellphone in your pocket – it has a \$30 processor, and with wireless access to the cloud, has infinitely more processing power than the ENIAC.

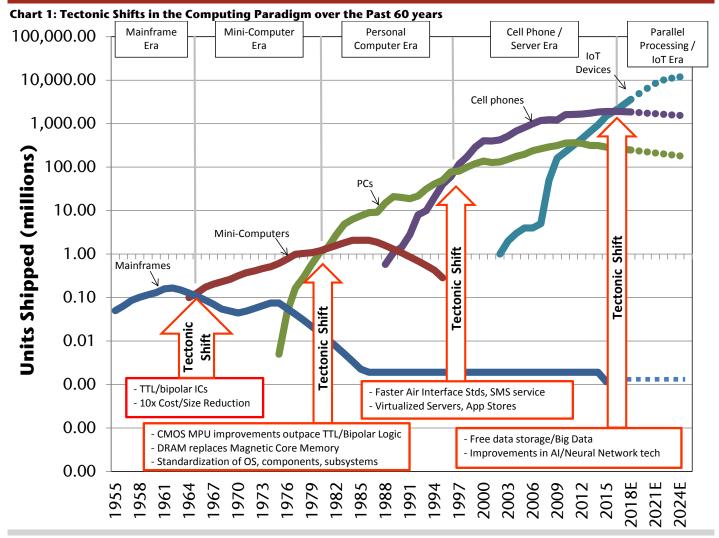
Mainframes in the 1950s saw improvements from the ENIAC, but were still measured in terms of \$100,000s in cost and 1,000s of square feet. By the mid-'60s, improvements in TTL-bipolar transistor technology led to a tectonic shift to mini-computers, the poster-child of which was Boston-based Digital Equipment Corporation (DEC). DEC's mini-computer price-tags were quoted in \$10,000s, and the space required to host them was measured in 10s of square feet. While mainframe sales peaked in the 100,000 unit range annually, annual mini-computer units reached to the 1,000,000 unit range.

The tectonic shift toward Personal Computers was driven by both technological and business innovations. CMOS microprocessor design improvements outpaced TTL-bipolar transistors, which allowed for much higher levels of integration, while DRAM replaced magnetic core memory. So both logic and memory were put on the Moore's Law size and cost model. On the business innovation front, IBM anointed Microsoft and Intel as their PC standard, and IBM shared its PC architecture with the world. The computing industry quickly shifted to a horizontal model from a vertical one, allowing component and subsystem vendors to benefit from global economies of scale, and PC-OEMs to benefit from a low-cost, assembly line manufacturing model. The PC model shifted by two orders of magnitude in units to 100s of millions, and one order of magnitude in costs to 1,000s of dollars.

By the late '90s, faster air-interface standards and efficient, centralized computing in the form of data centers set the computing industry up for a tectonic shift to a cell phone / datacenter paradigm, where a \$30 processor in your hand could potentially get you access to the computing power in all the datacenters of the world. VMWare was founded in 1998 and server virtualization dramatically lowered the cost of server compute cycles. A killer app called SMS was introduced, and Apple and Google created App Stores, harnessing the power of a huge ecosystem of software developers that drove utility into the cell phone today that few could have imagined in the '90s.

Importantly, each tectonic shift in the computing model brought with it a tectonic shift in its beneficiaries. IBM dominated the Mainframe Era, but DEC replaced IBM as the face of the Mini-Computer Era. IBM resurfaced in the PC Era to set PC standards, but Microsoft and Intel ended up controlling the standards and dominating the PC industry profits. The Cell Phone / Datacenter Era was dynamic — Nokia, with its Symbian OS and candybar form factor captured the lion's share of industry profits earlier, but is a shadow of its former self as Apple and distant second (as measured by operating profits) Samsung, dominate today. Intel and Microsoft have been the biggest beneficiaries on the backend of the Cell Phone / Datacenter Era.

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Source: Jefferies Equity Research, Mainframe computer data sourced from IBM Company Filings, "The Early Computer Industry: Limitations of Scale and Scope", A. Gandy; Minicomputer "History of Computer Communications" J. Pelkey; Personal Computer data sourced from "Total Share: Personal Computer Market Share 1975-2010", J. Reimer, Gartner; Mobile devices sourced from Counterpoint Research, Canalys Research, "Smartphones" Research Report, M. Ilyas, S. Ahson; IoT devices sourced from Gartner.

The Computing Industry has seen Tectonic Shifts about every 15 years

Each shift in computing model is 10x larger in units, and 10x smaller in ASP

We believe we are at the beginning of the next Tectonic Shift in Computing, toward a Parallel Processing / IoT Paradigm

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We believe the computing industry is at the beginning of the next tectonic shift, to a Parallel Processing / IoT model

Price declines in memory have led to "free storage" for many, and are an important driver of this shift

Improvements in AI, Neural Networking, Parallel Processors and Parallel software are also driving this tectonic shift

Parallel processing software is difficult to get right

NVidia recognized the market potential early and invested in its parallel processing platform 10 years ago, well ahead of its peers

Like the PC market in the '80s and the cell phone market in the '90s, Neural Networking technology is creating markets that don't exist – consequently they are difficult to forecast

Consistent with the 10x increase in units every tectonic shift, the IoT market is approaching 10 billion

Three tectonic shifts from today, your cellphone will be your grandkids' ENIAC

The Next Tectonic Shift is Happening—to a Parallel Processing / IoT Paradigm

It has been about 15 years since the shift to the Cell Phone / Datacenter model, and the accumulation of innovations since then leads us to believe that the computing industry is at the beginning of its next tectonic shift.

We view price declines in memory as one marker of this shift. Fifteen years ago, \$10 bought you enough memory to store 500, 2MB photos. Today, that same \$10 gets you enough memory to store over 100,000 photos. That price decline has translated to massive elasticities in demand – to the point where 10s of petabytes of data are now being stored (think of a group of 100 million bits, stored in 1 billion different places). Data storage for many today is practically free.

But if someone is allowing you to store all that data for free, then they likely want to monetize it – right? This is where improvements in Artificial Intelligence, more specifically, Neural Networking, as well as in parallelized software and parallel processing architectures play a role in our tectonic shift thesis.

Computer Science theory has always held that parallel computing architectures could be more efficient than serial ones for many applications. The challenge to that theory, however, had been that there never was good software to distribute your processing stream across parallel processors and then pull the outputs from those processors back together in the right order. This is a very difficult problem to solve. Consequently, computing architectures and software, have been largely serial in nature, up until recently.

However, 10 years ago last month, NVidia launched a software platform, called CUDA, that effectively did just that. The idea was that the CUDA software would enable programmers to leverage the parallel architecture in GPUs for general purpose computing, using widely deployed high-level languages like C++. Initial versions of CUDA weren't perfect, but five generations later, in 2012, the CUDA efforts bore fruit. A team from the University of Toronto used Deep Neural Networks and NVidia GPUs to smash its competition at the annual ImageNet competition, where teams compete to identify objects from a database of over 10 million images. The event caused a tectonic shift in the AI industry itself, shifting it from a "Knowledge-based" to "Data-based" discipline – and creating demand for GPU compute cycles.

Much like the PC market in the '80s and the cell phone market in the '90s, the size of the market for Neural Networking and parallel processing is difficult to quantify, because the markets they are creating simply don't exist. At four different Al conferences Jefferies hosted over the last 8 months (Boston, London, Hong Kong, Zurich) we heard how 30 different startups were using Al and Neural Networking for new business models, for example: 1) identify and sort recyclables from garbage; 2) write large portions of 10Qs and 10Ks from 3 years of financial statements, 3) do facial recognition on video from the far-flung CCTV network in China to catch criminals; and 4) using a wrist-worn heart rate monitor to predict with a 90% accuracy rate whether you will have a heart attack within the next two hours.

The data shows that each new computing model is 10x the size of the previous one in units. If cell phone units are measured in the billions, then the next one has to be in the 10s of billions. Gartner estimates that IoT unit shipments are currently approaching 10 billion units. With data storage effectively free, we expect that the data generated from all these IoT devices will be stored, and processed, using parallel processing platforms and AI technologies. The data tells us that we are at the beginning of the next tectonic shift in computing to a parallel processing and IoT platform paradigm. It is hard to imagine when you are so close to it, but three tectonic shifts from today, the cellphone in your pocket will likely become your grandkids' ENIAC.

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We believe that there have been three tectonic shifts in computing, each of which happened roughly every 15 years:

- 1) From Mainframes to Mini-Computers in the mid-'60s
- 2) From Mini-Computers to PCs in the early 1980s
- 3) From PCs to Mobile Phones / Datacenters in the late '90s

It has been about 15 years since the last tectonic shift, and we think we are at the beginning of the next shift now, to a Parallel Processing / IoT paradigm, driven by improvements in memory costs, as well as by improvements in parallel processing hardware and software, and Al and neural network technologies

Each tectonic shift can be characterized by a 10x magnitude change in price, size and weight. We think that the Parallel Processing / IoT model fits this rule of thumb

Chart 2: Drivers of Tectonic Shift in Computing Platform

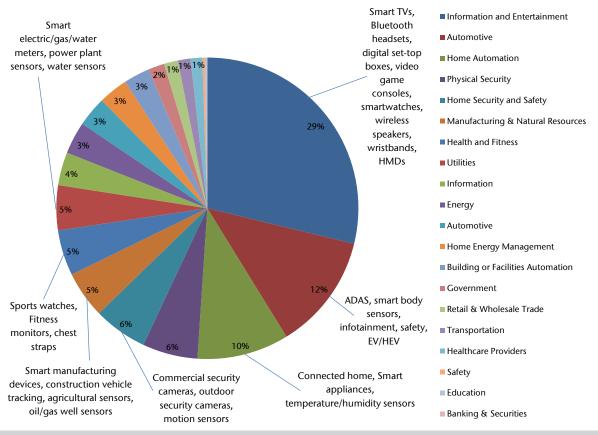
Tectonic Shift	<u>Years</u>	<u>Drivers</u>
Mainframe Computers to Minicomputers	Mid 1960s	TTL (transistor-transistor logic) bipolar logic circuits replaced slower DTL (Diode Transistor Logic) circuits Space requirement lowered to 10s of sq ft from 100s/1000s of sq ft ASP declines to 10s of thousands of dollars from 100s of thousands of dollars
Mini-Computers to Personal Computers	Early 1980s	CMOS MPU integration outpaces TTL/bipolar logic ICs DRAM replaces Magnetic Core Logic Standardization of the OS motivated a software ecosystem Standardization of components and subsystem enabled lower costs associated with production-line assembly and global economies of scale ASP lowers to the thousands of dollars from 10s of thousands of dollars Space requirement lowered to 1 sq ft from 10s of sq ft
PCs to Cell Phones / Servers	Late 1990s	Centralizing Processing Power - Faster Air Interface standards enable a \$30 CPU to potentially access all the processing power located in the data centers in the world SMS/texting services launched Virtualized server software lowers the cost/data center compute cycle Apple and Android App Stores drive utility into smartphones
Cell phones / Servers to Parallel Processing / IoT	Mid-2010s	Low cost of storage and "free" data storage translate to petabytes of data stored Improvements in AI and Neural Networking technology enable cloud players to process and monetize all the new data stored Moore Stress changes historical compute cost curve and results in more cores being added to processors

Source: Jefferies; "Rise and Fall of Minicomputers", Engineering and Technology History Wiki

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Chart 3: IoT: Internet of Things — Endpoints and Associated Services 2017



Source: Gartner (December 2016)

Applications run on a serial processor (such as the single core CPU depicted below) use one core at a time and process tasks in sequential order

Compare that to a parallel processor that breaks up tasks amongst several cores and re-assembles the completed tasks

Parallel processors can multiply the processing power of a similarly clocked serial processor *if* the application code is written to optimize the architecture

While CPUs tend to have an easily countable number of cores, GPUs can have thousands of low-powered cores being better suited for running simpler simultaneous calculations (e.g. graphics, matrix algebra)

Chart 4: Parallel Processing versus Serial Processing GPU w/ 10 GPU Cores GPU Core 10x10 pixel image GPU Core **GPU Core** - Assuming it takes 1 GPU core 1 **GPU** Core clock cycle to process 1 pixel, it 10x10 pixel image GPU Core GPU Core vould take 1 GPU with 10 cores 10 pre processing GPU Core clock cycles to process a 10x10 GPU Core pixel image GPU Core GPU Core CPU w/1 CPU Cores 10x10 pixel image - Assuming it takes 1 CPU core 1 clock cycle to process 1 pixel, it 10x10 pixel image CPU Core would take 1 CPU with 1 core 100 pre processing clock cycles to process a 10x10 pixel image Source: Jefferies

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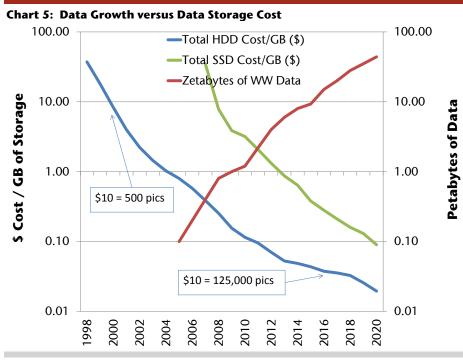
In 2000, \$10 purchased enough memory to store 500, 2MB photos. Today, that same \$10 buys you enough memory to store over 100,000 photos

Fifteen years of memory price declines have driven massive price elasticities in memory demand. Petabytes of memory (imagine 100 million bits stored in 1 billion different places) are now being stored at very low cost

Today, for many, data storage is effectively free

Improvements in parallel software and parallel processing architectures, like Nvidia's CUDA and graphics processors, have enabled powerful parallel processing Al frameworks like deep neural networks, to mine and monetize all the data that is being stored

As successful as some companies have been at harnessing the power of deep neural networks (Facebook, Google, Amazon, Baidu), these technologies have only recently been deployed in scale, we still consider the industry to be in its early stages



Source: Jefferies, Gartner

Chart 6: Depiction of a Neural Network

Input Layer Hidden Layers Output Layer

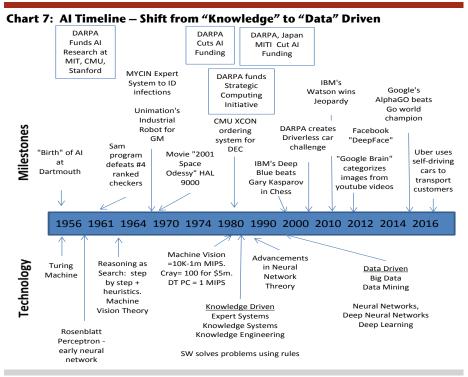
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Back Propagation

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Deep Neural Networks and easily programed parallel processing platforms have shifted the AI industry from a "Knowledge" driven model to a "Data" driven one



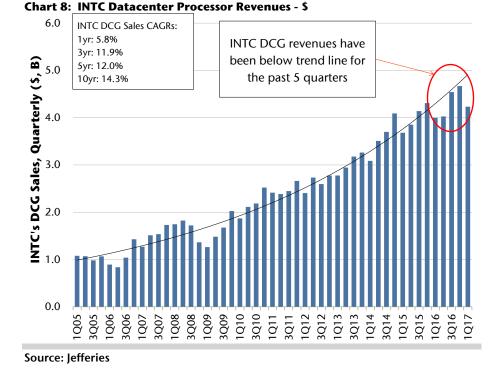
Source: Jefferies, Public Domain

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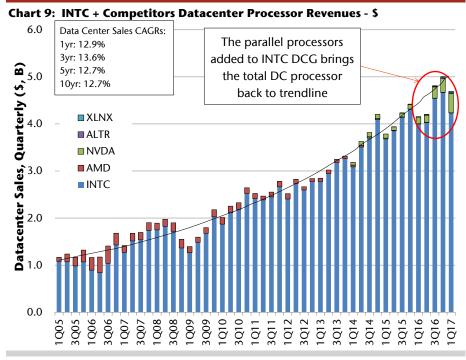
Intel's Datacenter business has grown at a low-to-mid double-digit CAGR over the past 3, 5 and 10 years

However, its 1-yr growth rate decelerated to 6% in the most recent quarter, and the past 5 quarters have been below trendline



When we add revenues from companies that sell parallel processors to revenues from Intel's Datacenter business, the aggregate datacenter processor revenue bars come back up to trendline

This suggests that processor growth in the datacenter has shifted to parallel processors from Intel x86 processors

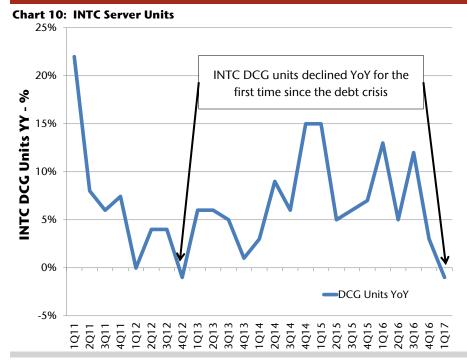


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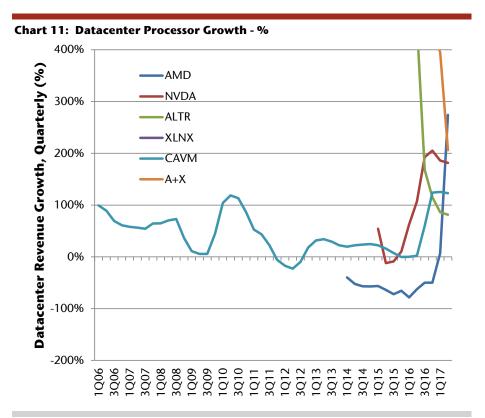
Intel Datacenter MPU unit shipments declined in 1Q17 for the first time since the debt crisis

Intel's 1Q17 suffered from a difficult YoY comparison due to an extra week in the 1Q16 quarter. Intel also may have suffered from an "airpocket" in demand in front of its next gen server MPU, Purley. That said, we still believe something secular is going on and expect Intel DCG growth rates to remain subdued



Source: Jefferies

Other companies that sell processors into the datacenter are posting impressive growth rates, albeit largely off of small bases



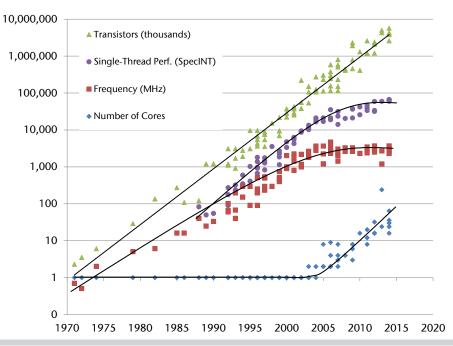
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Multiple sources highlight that while microprocessors appear to be staying on Moore's Law transistor density curve, that single threaded performance and clock frequency have not kept up, suggesting that the MPU industry could be at an inflection

The bottom line on this chart suggests that MPU makers are trying to make up for the stagnating single threaded performance with more processor cores per MPU consistent with our thesis that the industry is moving to a parallel processing paradigm

Chart 12: 40 Years of Microprocessor Trend Data

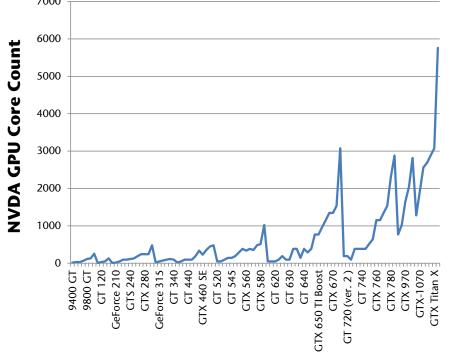


Source: Jefferies. Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten. New plot and data collected for 2010-2015 by K. Rupp.

NVidia has also been increasing its own core count in its GPUs

NVidia's Titan X can have up to 6,000 GPU cores - two full orders of magnitude higher than the highest core count MPUs

Chart 13: NVDA Discrete GPU Core Count (2008-2016) 7000



Source: Jefferies, NVDA

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The chart below highlights examples of non-x86 processors being deployed by the Super 7 cloud players, suggesting that the center of gravity of cloud processing is drifting away from x86

Chart 14: "Super 7" Non-x86 Data Center Announcements

Date	"Super 7"	Product	Processor	Comments
9-Mar-17	Facebook	Big Basin	NVDA GPU	FB Big Basin AI compute adopts NVDA Tesla P100 for data centers
13-Jul-16		Big Sur	NVDA GPU	FB Big Sur uses NVDA M40s for neural network training
15-Nov-16	Google	GCP	AMD GPU	GCP announces AMD FirePro S9300 for remote workstations
15-Nov-16		1	NVDA GPU	GCP announces NVDA Tesla P100 and K80s for deep learning
8-Mar-17	Microsoft	Azure	CAVM ARM	MSFT announces collaboration with CAVM using its 64-bit ARM processors
4-Aug-16		1	NVDA GPU	MSFT Azure announces NVDA K80 accelerators for GA on 1-Dec-16
19-Apr-17	Amazon	AWS	XLNX FPGA	AWS announces EC2 F1 instances for GA
29-Sep-16		1	NVDA GPU	AWS adopts NVDA K80 accelerators in its EC2 PC instances
17-Apr-17	Baidu	Baidu Cloud	NVDA GPU	Baidu integrates NVDA's Pascal-based Tesla GPU accelerators
17-Oct-16		1	XLNX FPGA	Baidu adopts XLNX in its data centers
3-Dec-16	Alibaba	AliCloud	ARM CPU	BABA to use SoftBank's ARM CPUs in data center
14-Oct-16			AMD GPU	BABA reaches deal with AMD to use Radeon Pro GPUs in data center
20-Jan-16		1	NVDA GPU	BABA teams with NVDA in \$1b bet on cloud computing
29-Mar-17	Tencent	Tencent Cloud	NVDA GPU	Tencent integrates NVDA's Pascal-based Tesla GPU accelerators

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Jefferies Artificial Intelligence Summit Series

The four charts below highlight AI startup companies Jefferies hosted over the past 8 months in Boston, London, Hong Kong and Zurich.

The examples highlight that it is difficult to quantify the market for Al/Neural Networking and Parallel Processing, because with the new technologies, these companies are creating new markets.

Location	Company	Description
Boston	Finn Advisors	Finn.ai is a white label virtual banking assistant, powered by Al (Siri for your bank). Finn helps digitally
		savvy financial institutions put a 'personal banker' in every customer's pocket, helping them to manage
		their money wherever they are, whatever they need via a simple, natural conversation.
Boston	Google Research	Research at Google (Google Brain team) is at the forefront of innovation in Machine Intelligence, with
		active research exploring virtually all aspects of machine learning, including deep learning and more classical algorithms.
Boston	IronNet Cybersecurity	IronNet Cybersecurity (founded in 2014 has raised \$33m in venture funding) is focusing on solutions for
		the commercial sector to make our networks safe through the implementation of behavioral modeling,
		statistical analysis, and machine learning techniques.
Boston	MIT Computer Science and Al Laboratory	Tommi Jaakkola, Ph.D., Professor of Electrical Engineering and Computer Science, focuses on machine
		learning and natural language processing. His academic work on statistical inference and estimation is wel known in the field of machine learning.
Boston	Nvidia	Nvidia Corporation is an American technology company based in California. It designs graphics processing units for the gaming and professional markets, and its progress advancing the deep learning industry has resulted in a lead versus its competitors.
Boston	Sentient Technologies	Sentient, founded in 2008, is well known in the tech circles for being the highest funded Artificial
Doston	sendent reamonogies	Intelligence company in the world. Co-founder Antoine Blondeau, helped invent the technology behind
		Apple's Siri and has been developing a distributed Al platform across multiple disciplines including
		marketing, e-commerce and finance markets.

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Chart 16:	Jefferies Artificial Intellic	gence Summit	. London 23-lan-17

London Babylon Health Babylon Health is the UK's leading digital healthcare service. Its pur	rpose is to democratise healthcare by
putting an accessible and affordable health service into the hands of	of every person on earth by building an
Al doctor to diagnose illness via its app. Babylon Health has raised o	over \$60m in venture funding.
London Cortexica Vision Systems Cortexica Vision Systems is the leading provider of image and object	ct recognition systems. Through
utilising the latest Al techniques, Cortexica provides unique and per business problems and needs.	rsonalised solutions to solve various
London Deepomatic Deepomatic helps companies and scientists build massive, high qua	,
the new generation of Al. Deepomatic's technology is based on dea	
visual inputs into meaningful concepts. The company has designed handling millions of search requests among millions of products.	a visual search engine, capable of
London Featurespace Featurespace is the world-leader in Adaptive Behavioural Analytics	and creator of the ARIC platform, a
machine learning software system developed out of the University of	• •
London Intelligent Voice Intelligent Voice Limited is a global leader in the development of pi	3
technology solutions for voice, video and other media. Intelligent V	oice turns your company and your
client's calls, email and IM into smart data, using a powerful Machir	ne Learning Engine and the "World's
Fastest" Speech to Text Engine.	
London re:infer re:infer is an artificial intelligence solution that provides structured,	human-like understanding of B2C
conversations. B2C businesses are talking more and more with their	r customers be that on in-app or on-
website chat, third party messaging platforms, social, calls or emails	5.
London Sadako Technologies Sadako Technologies is a Spanish innovative company incorporated	d in 2012 as a result of the concern of
its founders to use technology and engineering to build a better wo	orld. Specialists in the development of
latest generation technologies in the areas of computer vision and	robotics.
London Stepsize Stepsize's first product solves a problem developers working in tear	, ,
code, who wrote it, and why? Since these questions emerge from the	. , , , ,
metadata from the tools they use daily and provide a context layer	available directly from their editor.
London V.U. Amsterdam Dr. Eiben is a professor of Computational Intelligence at VU Univers	ity Amsterdam and Visiting Professor on
the University of York, UK. His research lies in the field of Artificial In	telligence, Evolutionary Computing,
Evolutionary Robotics, Artificial Life, and Adaptive Collective System	ns.

Source: Jefferies

Chart 17: Jefferies Artificial	Intelligence Summ	it, Hong I	Kong 6-Apr-17
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Location	Company	Description
HK	Baidu Big Data Lab	Baidu's Big Data Lab focuses on large-scale machine learning algorithms and applications in areas such as predictive analysis, large data structure algos and intelligent systems research. Haishan Wu is a senior data
HK	Claudh Garda Tacharala an	scientist and leads a team focusing on mining spatial-temporal big data of Baidu.
ПК	CloudMinds Technology	CloudMinds is researching avenues for many rapidly advancing Al engines in the cloud to make robots smarter. Bill Huang is the CEO of CloudMinds, where he is implementing a vision to provide households around the world with cloud base intelligent robots.
HK	Hangzhou Hikvision Digital Technology	The image recognition technology developed by Hikvision Robust Reading platform is currently the world's most influential contest in OCR technology field.
HK	HKUST and WeChat Joint Lab on Al	Research areas of WHAT LAB include intelligent robotic systems, natural language processing, data mining, speech recognition and understanding. The lab will bring together top researchers in the development of innovative artificial intelligence application with the database of WeChat.
HK	LeEco	Kai Ni is a Vice President in the Autonomous Driving Division at LeEco. Mr. Ni is responsible for leading the advanced engineering activity of autonomous driving and is in charge of product development of ADAS and automated driving systems.
HK	Megvii Technology / Face++	Megvii is producing China's top cutting-edge vision technology Al platform, Megvii products are now being used by Financial Institutions, real estates, security industries all around China.
HK	SenseTime	Founded in 2014, SenseTime's face recognition technology has an error rate below one in 100,000. It also provides text, vehicle and image recognition to mobile Internet companies, financial services and security companies. SenseTime has raised over \$120 million in venture funding.
HK	UB Tech	Ubtech is China's biggest robot maker, a \$5b technology company based in Shenzen. The University of Sydney partnered with Ubtech to create the Ubtech Al Research Center which aims to bring researchers from different academic fields together to collaborate on artificial intelligence.

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Chart 18: Jefferies Artificial Intelligence Summit, Zurich 13-Apr-17

Location	Company	Description
Zurich	Demiurge Technologies AG	Demiurge Technologies AG is a Switzerland-based artificial intelligence company developing the next
		generation of deep neural networks and brain chips for mobile robots.
Zurich	Ditto Al	Ditto Labs is a leading provider of vision-as-a-service for enterprises. The award winning company offers
		enterprise-class machine-learning and computer vision to businesses demanding a cloud-based API to
		label, filter and search visual media using artificial intelligence.
Zurich	Gamaya	Gamaya fits drones with a hyperspectral imaging system. This type of imaging can give scientists
		information about the type of ground, vegetation, and even building materials used. Drones are then
		flown over fields and industrial farmers can accurately measure the health of crops and their environment.
Zurich	Sentifi	Sentifi is building the largest online ecosystem of crowd-experts and influencers in global financial markets
		(Sentifi Crowd) to generate Sentifi Signals, market intelligence that is not available via traditional news
		media using our proprietary technology Sentifi Engine.
Zurich	Starmind International AG	Starmind Brain's vision is people to be able to think with the power of 1,000 brains by interlinking millions
		of people with billions of experiences and making this collective knowledge available in real time
		anywhere, anytime.
Zurich	Swiss AI Lab IDSIA	Prof. Marco Zaffalon, Swiss Al Lab IDSIA (Dalle Molle Institute for Artificial Intelligence), Founder & Head of
		the Imprecise Probability Group.
Zurich	University of Zurich	Professor Davide Scaramuzza, is the Director of Robotics & Perception Group at the University of Zurich.
		Professor Scaramuzza's main research interest is computer vision applied to the autonomous navigation of
		visually-guided ground and micro flying robots.

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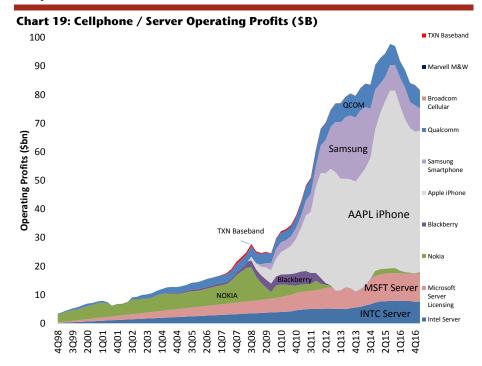
The smartphone and PC markets illustrate the importance of delivering a platform in order to capture industry profits.
Interestingly, while Nokia and its Symbian/Cellphone platform dominated up until 2008, Apple and its iPhone platform dominated since

Since an important part of the smartphone value proposition is its ability to harness the computing power of datacenters around the world, we include Intel and Microsoft as proxies for the other half of the Cell Phone / Datacenter computing paradigm

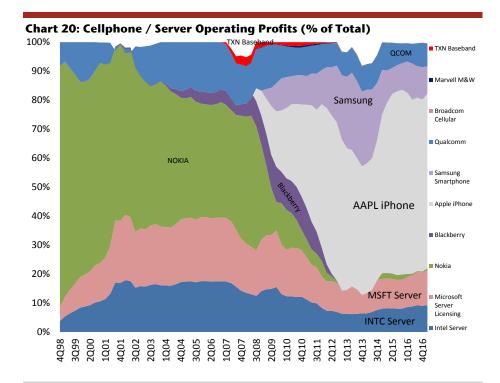
Apple's iPhone emerges as the dominate platform of this computing model today, capturing the majority of profits as it owns all the critical components of the platform: the SoC (Apple's AX SoCs), operating system (iOS), system-level hardware (iPhone) and App Store

On the backend of the Datacenter, Intel and Microsoft account for about 20% of this computing models' industry profits

Importance of the Platform – Case Studies



Source: Jefferies, company data

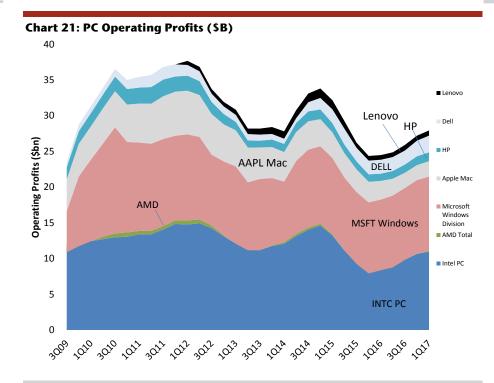


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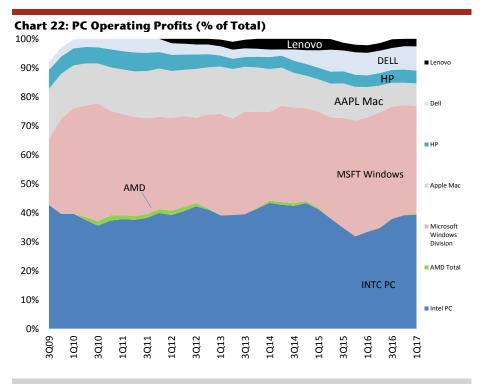
In the PC computing era, IBM anointed Intel and Microsoft as the standards of their PC, and shared its architecture, which enabled the IBM PC clone industry, and exposed component and subsystem makers to global economies of scale

Intel and Microsoft largely define the PC platform (Wintel) and have captured the lion's share of the PC industry profits



Source: Jefferies, company data

PC OEMs capture the remaining 20% of the industry profits—only Apple, by virtue of developing its own OS (MacOS), capable of capturing an outsized portion relative to its size



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Parallel Processing Platform Map

In this section we provide a framework for understanding how the different parallel processing platforms (hardware and software) relate to one another and to the high level deep learning frameworks that exist in the market today. For each platform, we highlight the Processor, Native Languages, the higher level Libraries and Primitives, as well as the high level Deep Learning Programing Languages and Frameworks that support that platform

Based on this framework, and our own field checks, we come to the following conclusions:

- 1) NVidia is the best Positioned Platform Provider at the Processor and Software Level. NVidia was early in recognizing the potential for the parallel processing market and 10 years ago started investing in a Software and Hardware Platform to prosecute this market. NVDA's proprietary CUDA software is on its 9th generation, where most other parallel software programs are on their 1st or 2nd. Not only did NVidia invest in CUDA, but it also invested in placing CUDA and its GPUs at engineering and science programs at top universities around the world. At the four Jefferies hosted AI conferences, we heard contacts from MIT, Princeton and VU in the Netherlands say things like "we all use NVDA and CUDA at our university." At the processor level, NVidia launched its Pascal GPU with mixed precision support, and is expected to launch its next gen GPU, Volta, with tensor cores, which we believe means that it has at least a 2-year lead on its processor and at least a 2-to-5 year lead on its CUDA software. We think that being a first mover is key, due to the transaction costs associated with porting software to a new platform.
- 2) Google's TensorFlow and TPU (Tensor Processor Unit) appear to be Second. Google introduced its TPU1 for inferencing last year, and recently announced its TPU2 for training last month. Google has its own deep learning framework, called TensorFlow, which is a high level language for writing code to train Neural Networks, that makes the platform underneath it invisible to developers. In the limit, Google's TPU2 could disrupt NVDA's training, but we think it would be limited to disruption at Google. We believe Google is still purchasing NVDA GPUs, and as of yet, Google has not opened its TPU2 up for public use.
- 3) Intel Has Made Good Efforts in its Software and Processors, but is still lagging NVidia and Google. Intel has three platforms... arguably four: based on Xeon, Xeon PHI, Altera FPGA (Programmable Solutions Group), and Lake Crest (Nervana). On the positive side, Intel has expanded its Math Kernel Library (MKL) to support deep neural network libraries (MKL-DNN), and its Neon Deep Learning Framework has promise. However, its parallel processing solution Xeon PHI does not support mixed precision processing, nor does it have tensor cores for matrix multiplication key for Deep Learning Training.
- 4) AMD and XLNX have new deep learning products but yet to see broad adoption. AMD's MiOpen and XLNX SDAccel have been recently introduced to the market. These solutions bear watching, but we have not seen broad support for these solutions in production environments.

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A Guide to Understanding Parallel Processing Platforms (Hardware and Software)

Chart 23: Parallel Processing Platform Map

	t 23: Parallel Processing Pl	•	Optimized Deep	Learning Framewor	ks / Design Language	es		
Apac	he Singa	Υ					Y	
Caffe	1	Υ		Y	Y	Υ	Y	
Caffe	2	Υ		Under Development				
Deep	learning4j	Υ					On Roadmap	
Dlib		Υ					No	
Kera	s	Υ					Under Development	
Micro	osoft Cognitive Toolkit CNTK	Υ		Y			Y	
MXN	et	Υ		Y	Under Development		Y	
Neon	1			Y		Υ		Υ
Open	INN	Υ					No	
Goog	le TensorFlow	Υ	Y	Y	Under Development		Y	
Thea	no	Y		Y			Y	
Torcl	h	Y		Y			Y	
	Libraries / Primitives	Nvidia Deep Learning SDK (cuDNN)	Google TPU Software Stack (API, Drivers)	Intel MKL (MKL-DNN, DAAL)	Xilinx reVISION, RAS (xfDNN, xfBLAS)		AMD MIOpen (OpenCL, HIP)	Intel MKL (MKL-DNN, DAAL)
PLATFORM	Native Languages / Drivers	CUDA	C++, CUDA	C++	OpenCL, C++ Vivado, SDAccel	OpenCL Quartas	ROCm (HCC, HIP, OpenCL, Python)	C++, Python
	Processor	Nvidia GPU	Google TPU	Intel Xeon Phi, Xeon	Xilinx "UltraScale" FPGA	Intel (Altera) "Arria 10" FPGA	AMD GPU	Intel Nervana "Lake Crest"

Source: Jefferies Equity Research

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Based on the findings in Chart 23 (above), NVDA is the best positioned platform provider at the processor and software level

At the chip level, NVDA's Volta launch extends its lead versus competitors which we estimate to be ~2 years

At the software enablement level, we see an even wider lead as NVDA has so deeply seeded its CUDA software and libraries amongst researchers at top universities around the world

NVDA's GPU are available at every major cloud service provider (Amazon, Microsoft, Google, IBM) and its hardware is optimized on all of the most popular deep learning frameworks today (including Baidu's PaddlePaddle which is not presented above).

We view this as a major competitive advantage that is not fully appreciated by investors

Deep Learning Platform Summaries

Chart 24: NVDA Deep Learning Platform Summary

Parallel Processing Platform Element	Comments
Deep Learning Frameworks / Design Languages	Compared to other parallel processing platforms, Nvidia has the broadest support amongst the design languages, which is consistent with its first mover advantage and with its parallel processing native language and extensive libraries.
	Nvidia arguably has the most comprehensive and libraries for deep neural network training and parallel processing. The "Nvidia Deep Learning SDK" includes libraries like cuDNN (Neural Net building blocks), TensorRT (inferencing production deployment), DeepStream (inference, transcoding), cuBLAS and cuSPARSE (Linear Algebra), NCCL (collective communication modules).
Libraries / Primitives	The table above is largely focused on parallel processing as it relates to deep learning, however one could consider a broader view of NVidia's parallel processing capabilities. In Automotive, Nvidia's SDK is called "DriveWorks," which includes libraries for sensor fusion, map localization, vehicle control and ADAS rendering. In gaming, NVidia's SDK is called "GameWorks," which includes libraries like VisualFX (face, hair, wave, shadow movements), PhysX (clothing, explosions) and OptiX (ambient light, acoustics, line of sight). Importantly, all of NVidia SDKs are based on CUDA and can be integrated with cuDNN.
Native Languages	Nvidia's GPU native language is its proprietary CUDA. CUDA is like a proprietary C++ for Nvidia GPUs that was constructed to support parallel processing. Nvidia originally started investing in CUDA over 10 years ago, and the company has been seeding CUDA in engineering and science programs at Universities for the past 10 years - and consequently the company can boast it has 500,000 developers that know CUDA.
Processor	All of Nvidia's GPUs support CUDA, which means that software developed on one class of GPU can be run on a different class. Its GPUs for the datacenter include its Tesla-class, including its most recently launched DGX-1 (aka supercomputer in a box), which are designed for Neural Network Training, and P1 (or P40?) for inferencing. NVidia's gaming family of GPUs include its Titan family, as well as it GeForce. NVDA's Automotive solutions are called Drive-CX (infotainment, digital dash) and Drive-PX (ADAS, autonomous driving). And its mobile solution is called Tegra.
	Importantly, NVidia's most recently announced GPU architecture, Volta, has "tensor cores" which allow for rapid matrix multiplication calculations critical for neural network training and inferencing.

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In our view, Google's Tensor Processing Unit optimized for Tensor Flow appears to be second

In our estimation, it would take months to optimize the TensorFlow code for alternate deep learning frameworks. This limits the use cases for researchers and developers who have already committed to another type of framework (e.g. Caffe or Theano)

Google introduced its TPU1 for inferencing last year, and recently announced its TPU2 for training last month. Google has stated that it will offer Volta-based NVDA GPUs in its Cloud Platform, but we view the TPU as a disruptor in the industry

The TPU puts pressure on the other hyperscale cloud providers to develop a similar offering to remain competitive

Parallel Processing Platform Element	Comments		
Platform Element	Google's Tensor Processing Unit (TPU) is only compatible with TensorFlow, Google		
	designed open sourced deep learning framework. Google's TPU 2.0 (announced		
Deep Learning	2Q17) was optimized for TensorFlow so researchers who develop in TensorFlow		
Frameworks / Design	abstraction can expect better performance, while developers using competing		
Languages	software engines (such as Caffe and Torch) will have to conform to adopt the		
	hardware. Bear in mind TensorFlow is the most widely used deep learning		
	framework.		
	Google's engineering team developed a compiler and a proprietary software stack		
Libaariaa / Drimaitiwa	that translates API calls from TensorFlow to TPU instructions. Compared to a CPU		
Libraries / Primitives	that can compute 10's of operation per cycle, a TPU can compute hundreds of		
	thousands a cycle.		
Native Languages	C++, Python, CUDA are the native languages. Like a GPU the TPU stack is split into a		
	User Space Driver and a Kernel Driver. The Kernel Driver is lightweight and handles		
	only memory management and interrupts - designed for long-term stability. The		
	User Space driver changes frequently. It sets up and controls TPU execution,		
	reformats data into TPU order, translates API calls into TPU instructions, and turns		
	them into application binary.		
	The User Space driver compiles a model the first time it is evaluated, caching the		
	program image and writing the weight image into the TPU's weight memory; the		
	second and following evaluations run at full speed.		
	Google's Tensor Processing Unit (TPU) is a custom-ASIC that was conceived in 2013		
	as a need for larger computational demands for neural networks were identified		
	within the company leading to a requirement to double the datacenter footprint. In		
Processor	just over a year the chip was 28nm silicon was designed, built and shipped		
	unprecedented for the industry. Matrix multiplication operations were targeted		

within the organization to limit reliance on 16- and 32-bit CPUs and GPUs.

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In our view, INTC has made good efforts in its software enablement platforms as well as at the processor level, but it still lags NVDA and Google in the deep learning field

INTC has a myriad of product offerings (Xeon, Xeon Phi, Arria 10 FPGAs, and Nervana silicon)

We view the software development with its Math Kernel Libraries (DAAL, MKL-DNN, etc.) as a differentiator – but it still lags NVDA's robust software suite and libraries

Parallel Processing Platform Element	Comments		
Deep Learning Frameworks / Design Languages	Compared to other parallel processing platforms, Intel has been investing more nominal dollars in the development of its ecosystem simply because of its size. In our view, Intel's efforts in the field lack the expertise of Nvidia and the impact of Google.		
Intel Math Kernel Library (MKL) attempt to abstract the reliance on any hardware (whether that be a CPU, GPU, ASIC, DSP or FPGA). Intel origi its MKL over a decade ago, but a more stable release (v 11.3) was upd February 2016. MKL software supports code to optimize mathematical specifically for Intel processors (Xeon, Xeon Phi, and Nervana silicon) tapplication performance. Highly vectorize and threaded functions such algebra (BLAS), fast fourier transforms, deep neural networks, vector mand data fitting optimizations are released for free to customers through community licensing program.			
Libraries / Primitives	Intel Math Kernel Library - Deep Neural Networks (MKL-DNN) is an open source primitive that is included in Intel's Math Kernel Library to optimize performance of a deep neural net. MKL-DNN is meant to accelerate technologies like image recognition and allows use with Python and Java.		
	Within Intel MKL is the Intel Data Analytics Acceleration Library (DAAL) which helps speed big data analytics by providing optimized algorithmic building blocks for all data analysis stages (pre-processing, transformation, analysis, modeling, validation and decision making). Intel DAAL is optimized to support Intel's Xeon, Xeon Phi, Core and Atom processors.		
Native Languages	Initial release of Intel Math Kernel Libraries was August 2015 and supports both C+		
Processor	Intel processors targeting the deep learning industry include Xeon, Core and Atom; while accelerators include Xeon Phi, Altera FPGAs, and Nervana. While Intel's approach to tackle the deep learning market does not appear to be as unified as Nvidia's, we not that the widespread adoption of Intel silicon does work to its		

Source: Jefferies, company data

advantage in the space.

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XLNX SDAccel has been recently introduced to the market

This solution bears watching, but we have not seen broad support for this solution in production environments

Chart 27: XLNX Deep Learning Platform Summary

Parallel Processing	Comments			
Platform Element	Comments			
	While Xilinx's main FPGA competitor at the leading edge (Altera) was acquired by			
Deep Learning	Intel in 2015, the competition in the FPGA accelerator market is intense. This market			
Frameworks / Design	represents less than 5% of total sales today, but is growing quickly as hyperscale			
Languages	cloud providers like AWS, Azure and Baidu Cloud adopt FPGAs-AAS in the			
	datacenter.			
	Xilinx's reVISION software stack for machine learning and computer vision			
	applications at the edge sit on top of Xilinx's Zynq MPSoCs. In the datacenter			
	Xilinx's Reconfigurable Acceleration Stack sit on top of UltraScale+ FPGAs to			
	optimize performance. Xilinx proprietary libraries (xfDNN, xfBLAS, etc.) are highly			
Libraries / Primitives	optimized for Xilinx FPGAs at 16-bit and 8-bit integer data types.			
	Given that Xillinx's SDAccel environment sits on top of OpenCL, we think the pole			
	position in the accelerator market rests with Nvidia largely due to its robust libraries			
	for deep neural network training and parallel processing.			
	Xilinx SDAccel development environment for OpenCL and C/C++ enables optimized			
	performance of Xilinx's FPGAs in data center acceleration applications. SDAccel			
	combines the optimized compiler supporting OpenCL, C and C++ kernels, along			
	with proprietary libraries, and development boards to streamline run-time			
	performance on an FPGA.			
Native Languages				
	Xilinx SDAccel was first released in 2015 and while the initiative is being invested in			
	currently, the company notes that development is significantly behind Nvidia with			
	its proprietary CUDA software.			
	Xilinx's Vivado design suite allows users to leverage C-based design calls.			
	Xilinx FPGAs for training and inference (machine learning, computer vision, etc.) are			
	based on the reconfigurable nature, lending itself to a wide range of workloads and			
	new evolving algorithms. Microsoft Azure (using Altera FPGAs) and Amazon AWS			
	(using Xilinx FPGAs) are the two most notable hyperscale cloud vendors to deploy			
	FPGAs for commercial availability. Baidu has also adopted Xilinx FPGAs in its			
	datacenter. FPGA instances in the datacenter are useful in many HPC applications			
Processor	such as genomics research, financial analytics, real-time video processing, big data			
	search, and security.			
	One of the major drawbacks to deploying FPGAs at massive scale is the difficulty to			
	program, but increased levels of software abstraction (such as SDAccel) intend to			
	alleviate this problem.			

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AMD's miOpen has been recently introduced to the market

This solution bears watching, but we have not seen broad support for this solution in production environments

Chart 28: AMD Deep Learning Platform Summary
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Parallel Processing Platform Element	Comments		
Deep Learning Frameworks / Design Languages	While AMD's main competitor in the Deep Learning market has the broadest support amongst design languages, AMD has recognized the importance of a GPU as a parallel processor and believes its competitive advantage is its open source strategy.		
Libraries / Primitives	MiOpen is AMD's open source library to enable Radeon-GPU acceleration for deep learning and was made available to developers in early July 2017. Analogous to NVDA's cuDNN, miOpen provides GPU-tuned implementations for standard calls into programming languages OpenCL and Python. In our view, AMD's miOpen deep learning library is an important step to optimize performance on Radeon GPU-specific hardware.		
Elbianes / Timilaves	MiOpen supports 2 programming models - OpenCL and HIP (Heterogeneous-Compute Interface for Portability). HIP is a CUDA porting tool that scans CUDA source code and converts it to source code that can run on AMD GPUs.		
	AMD is targeting a broad range of applications with its parallel processing capabilities including autonomous vehicles, smart homes, drones, etc.		
Native Languages	AMD announced its Radeon Open Compute Platform (ROCm) v 1.0 in April 2016 in attempt to provide an alternative to CUDA, NVDA's proprietary GPU language. Various compilers and porting tools within ROCm allow for the possibility to use of alternative languages on the platform (CUDA, C/C++, Lua, Python, R, Ruby, etc.).		
	Theoretically this porting of code from a higher level abstraction layer to the AMD silicon provides a migration path for developers, but we believe performance will inevitably be sacrificed.		
AMD has a unique position in the deep learning stack, as it is the only com with x86 and discrete GPU silicon expertise and has been promoting the coan Heterogeneous System Architecture (HSA). The HSA allows the CPU and Coan to be written in the same source file and support capabilities such as a uniform GPU memory space. AMD's Vega GPU Architecture (expected to be released 3Q17) is targeting the high end of the discrete GPU market, a market that it dominated. While we view the product rollout as a positive for AMD, we we see what features are unveiled with deep learning in mind, to remain comparison.			

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Parallel Processing / IoT Winners and Losers

Chart 29: Tectonic Shift Winners & Losers

Company	Winner/Loser	Comments
AMD	Winner	We see AMD as a beneficiary of the shift in computing as it is the only other company besides NVDA with GPU technology, and this will be increasingly valued as workloads migrate to parallel, multi-core architectures
CAVM	Winner	We see CAVM as a beneficiary of the shift toward a parallel computing model due to its heritage in networking and multi-core processing CAVM is the only commercially viable 64-bit ARM server vendor, and we think it gains share in emerging workloads due to its lower price/performance/watt We think MSFT's adoption of ARM in datacenter catalyzes broader adoption
INTC	Loser	 We see INTC as structurally disadvantaged in the shift in computing due to its reliance on x86 architecture, and dominant market position x86 single-core performance per dollar has plateaued, while multi-core perfomance per dollar has increased We see emerging workloads migrating to parallel, multi-core architectures based on NVDA's GPUs and CAVM's ThunderX
NVDA	Winner	 As the de facto standard in Al, we see NVDA as a primary beneficiary of the shift in computing to parallel, multi-core workloads NVDA dominates the GPU market and has invested heavily in the ecosystem needed to enable developers to use them We see NVDA capitalizing on its dominate position as machine learning workloads grow
XLNX	Winner	 We see XLNX as a beneficiary of the shift to a parallel computing model as its programmable devices are capable of being parallelized Like NVDA, XLNX has invested heavily in the software ecosystem and expanded its user base 5x by creating development environments (SDAccel, SDSoC, SDNet), and supporting machine learning in embedded vision (reVISION) As the last independent FPGA vendor we see it capitalizing on the tailwind from share gains on the latest leading-edge nodes-65% on 28nm; 80% on 20nm; and 100% on 16nm

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(Article 3(1)e and Article 7 of MAR)

Recommendation Published , 00:31 ET. July 10, 2017 Recommendation Distributed , 01:00 ET. July 10, 2017

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- Broadcom (AVGO: \$253.11, BUY)
- Cavium Inc. (CAVM: \$66.57, BUY)
- Cisco Systems, Inc. (CSCO: \$31.84, BUY)
- Inphi Corporation (IPHI: \$38.99, BUY)
- Intel Corporation (INTC: \$34.73, UNDERPERFORM)
- Lattice Semiconductor Corporation (LSCC: \$6.72, HOLD)
- M/A-COM Technology Solutions Holdings, Inc. (MTSI: \$63.02, BUY)
- Marvell Technology Group Ltd. (MRVL: \$16.25, HOLD)
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Rating	Count	Percent	Count	Percent
BUY	1086	50.87%	335	30.85%
HOLD	897	42.01%	180	20.07%
UNDERPERFORM	152	7.12%	15	9.87%

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