Global Semiconductors

Semiconductor Primer 2020: at cross roads of secular, geo-political, competitive forces

Primer

Investor handbook on the global semiconductor industry

We examine the key building blocks, growth drivers, and barriers to entry shaping the $437bn global semiconductor industry that has become a flashpoint in the trade war between the US and China. If data is the new oil, self-sufficiency in semi technology and manufacturing is as critical to every global power as energy independence has been for the past century. Our collaborative primer outlines critical semi products, manufacturing processes, and competitive landscape between US/western and Chinese suppliers.

At cross roads of secular, geopolitics, competitive forces

Over the past five years, semi sales have grown at a 5% annualized pace or 2x the growth of global GDP, enabling secular megatrends such as cloud computing, AI, ubiquitous mobile broadband (5G, Wi-Fi), Internet-of-Things, smart factories/robotics, and advanced industrial/electric vehicles. A decade of consolidation has created an enormously profitable industry with ~30%+ EBITDA margins, up 800bps since 2013. However, the industry now faces two opposing forces: 1) geopolitics as US/China race to control/secure capacity, intellectual property and technical standards, with no hesitation in using disruptive tariffs/blacklisting of customers (Huawei, SMIC, etc.); 2) competition from new entrants such as Apple, Amazon and others who are leveraging their R&D forces to insource products they used to buy from mainstream semiconductor vendors.

US/China trade tensions could define next decade of semis

In 2019, China consumed 49% of US and 35% of global semi output but produced just 5% of global semi output. It is therefore no surprise that China is taking great strides to build out a domestic semi industry, notably through its “Made in China 2025” policy that targets 70% domestic semi production by 2025. Our primer discusses this imbalance and argues that despite China’s $30bn in funding, without access to critical US/allies design tools (Cadence, Synopsys), manufacturing equipment (ASML, Applied Materials, Lam Research, others), packaging/test (Teradyne, Advantest, TSMC), analog chips (Texas Instruments, Analog Devices), and high-end cloud processors (Nvidia, AMD), it will be difficult for China to catch-up. Separately, while US dominates in semi IP and design, only 12% of global manufacturing is based in the US, with >80% in Asia. Sovereign manufacturing will be a key trend for semis over the next decade, though will not be easy as leading-edge fabs require $15-$20bn of capex and 1-2 years of construction.

TSMC, ARM, Cloud scale changing competitive chessboard

While small today, we note growing risk of large tech customers like Apple and Amazon insourcing key semi products; leveraging their scale, ability to hire top semis talent, and availability of off the shelf design tools, IP (Arm) and outsourced manufacturing/foundry ecosystem (TSMC/Samsung.) This, plus the exponential increase in chip design costs and complexity could promote faster consolidation between semis looking to pool design, software and developer talent, such as announced M&A from Nvidia, AMD, and Marvell.

Refer to important disclosures on page 39 to 41. **12211540**

Timestamp: 07 December 2020 05:00AM EST

07 December 2020

Equity
Global
Semiconductors

Vivek Arya
Research Analyst
BofAS
+1 646 855 1755
vivek.arya@bofa.com

Jamie Zakalik
Research Analyst
BofAS
+1 646 556 4825
jamie.zakalik@bofa.com

Robin Cheng >>
Research Analyst
Merrill Lynch (Taiwan)
+886 2 2376 3733
robin.r.cheng@bofa.com

Adithya Metuku, CFA >>
Research Analyst
MLI (UK)
+44 20 7995 8323
adithya.metuku@bofa.com

Simon Woo, CFA >>
Research Analyst
Merrill Lynch (Seoul)
+82 2 3707 0554
simon.woo@bofa.com

Mikio Hirakawa >>
Research Analyst
BofAS Japan
+81 3 6225 7989
mikio.hirakawa@bofa.com

Blake Friedman
Research Analyst
BofAS
+1 646 556 1850
blake.friedman@bofa.com

Karan Pasricha
Research Analyst
BofAS
+1 646 743 0581
karan.pasricha@bofa.com

Mike Yang >>
Research Analyst
Merrill Lynch (Taiwan)
+886 2 2376 3729
mike.c.yang@bofa.com

Dah-Yeon Rhee >>
Research Analyst
Merrill Lynch (Seoul)
+82 2 3707 0460
dahyeon.rhee@bofa.com

Contents

PM Summary

Semiconductors are integral components for virtually every electronic device used today from smartphones, to PCs, to servers, to automobiles, to industrial robotics, making self-sufficiency in semi technology and manufacturing critical for global superpowers.

Today, the US is the world leader in semiconductor production with roughly 47% share. In 2019, China consumed 49% of the US's chip output, and 35% of global semi output, but produced just 5% of global semi output. To put that in context, this means that China has to import roughly $125bn worth of semiconductors, or 86% of the total chips they consume. It is therefore no surprise that China is taking great strides to build out a domestic semi industry. However, despite $30bn in government funding set aside for investment in a domestic chip industry, without access to critical US/allies design tools, equipment, manufacturing technology, and packaging/test, it will be difficult for China to catch-up to current incumbents (the US, Taiwan, Korea, Europe and Japan).

Exhibit 1: China consumed 35% of the $412bn semiconductor market in 2019 but produced just 5% requiring them to import ~86% of total chips consumed

	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
Semiconductor Sales ($bn)	$226	$298	$300	$292	$306	$336	$335	$339	$412	$469	$412
YoY (%)	*-9%*	*32%*	*0%*	*-3%*	*5%*	*10%*	*0%*	*1%*	*22%*	*14%*	*-12%*
China Semiconductor Production ($bn)	$4	$6	$8	$9	$10	$12	$13	$13	$19	$24	$21
% of Total Semis	*2%*	*2%*	*3%*	*3%*	*3%*	*3%*	*4%*	*4%*	*5%*	*5%*	*5%*
China Semiconductor Consumption ($br	$46	$63	$66	$62	$81	$92	$99	$108	$132	$158	$144
% of Total Semis	*20%*	*21%*	*22%*	*21%*	*26%*	*27%*	*29%*	*32%*	*32%*	*34%*	*35%*
China Import %	*91%*	*91%*	*88%*	*86%*	*87%*	*87%*	*86%*	*88%*	*85%*	*85%*	*86%*

Source: BofA Global Research, SIA, IC Insights

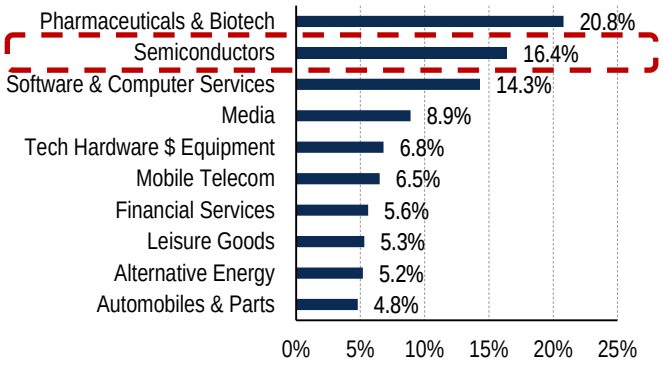
China semiconductor initiatives

In March 2020, China updated its "IC Fund" with Phase-2, which targets to invest $30bn in semiconductor equipment and materials. This is part of the Chinese government's wider initiative called **Made in China (MIC) 2025** – pushing for leadership in robotics, information technology, and clean energy. Among its various goals, MIC 2025 sought to produce 40% of its China's semiconductors domestically by 2020 and 70% by 2025.

Design: EDA tools, IP, and fabless companies

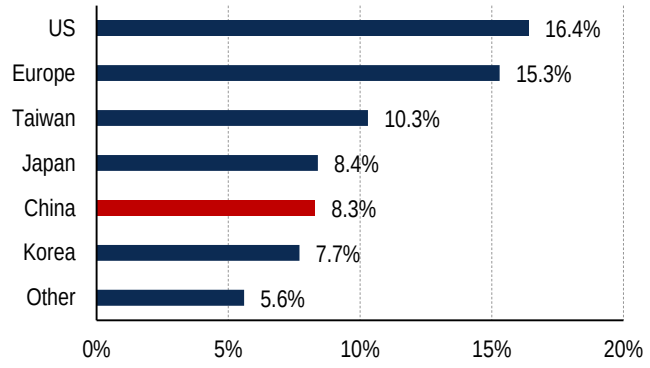
To remain competitive in the semiconductor industry, firms must continually invest a significant amount in designing chips. Indeed, in the US, semi industry R&D intensity (16.4%) is among the highest in major sectors, 2nd only to US pharma & biotechnology. By comparison China semi companies invests just 8.3% of its sales in to R&D. To put this in context, at an R&D intensity of 8.3% China semi companies spent ~$2bn in R&D in 2019. This compares to the $13bn that Intel alone spent on R&D last year.

Chart 1: US Semi R&D % of sales is 16.4%, 2nd to Pharma & Biotech



Source: 2019 EU Industrial R&D Investment Scorecard, SIA

Chart 2: US R&D intensity nearly 2x larger than China



Source: 2019 EU Industrial R&D Investment Scorecard

The design of modern day chips is not possible without assistance of computer design software (EDA tools) at every step in the design process. This market is dominated by 3 US firms: Synopsys, Cadence, and Mentor Graphics. China currently does not have any EDA vendors that have a full end-to-end design and verification solutions.

In lieu of developing unique internal designs, companies can also buy semi intellectual property (IP) or pre-designed blocks of circuits. The largest semiconductor IP vendor is Arm (British company currently owned by Japanese conglomerate Softbank but in the process of being acquired by US semi vendor, Nvidia) with roughly 40% of the market share. Synopsys is the 2nd largest with 18% share followed by Cadence with 6% share.

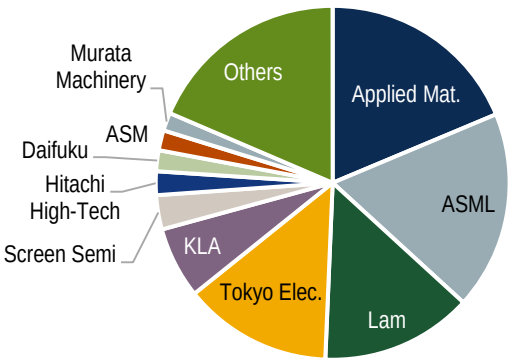
Manufacturing: foundries, IDMs, semicap equipment

Semiconductor manufacturing involves one of the most sophisticated processes in modern mass production of any product. A single chip, about 1 square inch in size, can contain billions of interconnected transistors. A state-of-the-art chip factory (known in the industry as a fab) cost $18-$27bn to build and operate (per SIA) and relies on tens of thousands of global suppliers for key inputs, including equipment and materials.

In 2001, 30 companies manufactured at the leading edge however as semi manufacturing grew in cost and difficulty, this number has fallen to just 3 firms (called foundries or IDM if they both design and manufacture): TSMC (Taiwan), Samsung (Korea), Intel (the US). China's largest foundry (SMIC) is still on legacy (14nm) process technology, which is 5+ years and 2-3 generations behind TSMC, Samsung, and Intel.

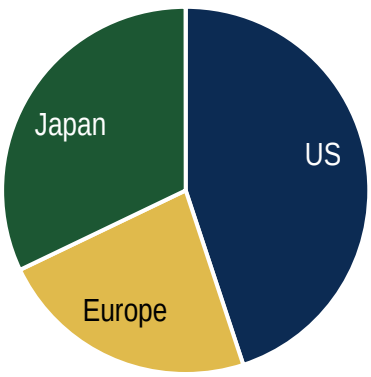
In order to manufacture semis (esp. at leading edge) foundries must purchase semicap equipment from the top 5 vendors which make up 70% of the market. 3 out of the 5 are US based (Applied Materials, Lam Research, KLA), while 1 is European (ASML) and 1 is Japanese (Tokyo Electron). The US, Japan, and Europe dominate the semicap market with 87% share. While Chinese semicap equipment vendors do exist (2% of total in 2019), they tend to provide equipment for legacy nodes, with little to no position in leading edge. Thus, if China wants to manufacture leading edge chips, it is virtually impossible without equipment from the US or allies. Indeed, roughly 80% or more of SMIC equipment comes from US vendors, a concern for SMIC as it faces mounting US restrictions. Moreover, as process nodes shrink (to <5nm), Extreme Ultraviolet (EUV) lithography becomes critical, a technology in which ASML has a monopoly.

Chart 3: The top 5 semicap vendors make up nearly 70% of the market



Source: Gartner

Chart 4: % of top 15 WFE from different regions



Source: Gartner

Internal silicon efforts

We also outline the changing semi competitive environment as hyperscale customers (like Apple, Amazon) accelerate internal chip efforts given the wider availability of pre-defined chip IP (from Arm) and leading-edge foundry capacity (from TSMC, Samsung).

Semiconductors 101

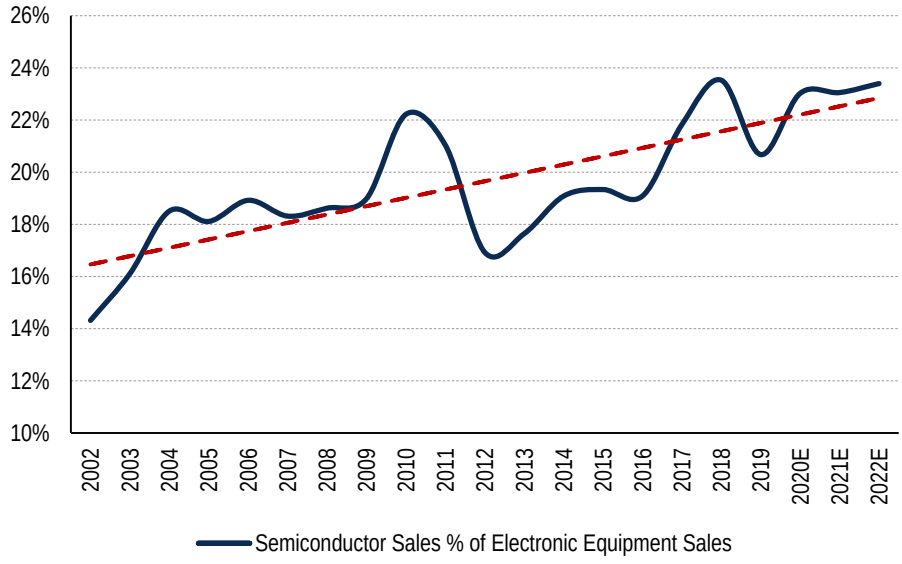
What is a Semiconductor?

Semiconductor devices, commonly known as chips (short for microchips), are integral components for virtually every electronic device. Different chips range in 'intelligence' and function, but the purpose for most is to process, store, and/or transmit data. Chips are made using semi-conductive materials (hence the name) like Silicon (Si), Gallium Arsenide (GaAs), Silicon Carbide (SiC), and Silicon Germanium (SiGe). These materials can be manipulated to be either a conductor of electricity (can carry a current, like copper) or an insulator (cannot carry a current, like glass). So, at a microscopic level, chips function by regulating electrical flow along a circuit. The subsequent electrical pattern is translated in to a specific digital binary code (combination of 1s and 0s) and serves as the instructions for the electrical device.

On a microscopic level, chips function by regulating electrical flow between silicon regions. **Transistors** serve as the gates regulating that flow of electrons. An **integrated circuit (IC)** refers to a singular semiconductor chip that is designed with many other discrete semiconductor components (resistors, capacitors, inductors, diodes) that are integrated into its geometry. Integrated circuits have millions or billions of transistors on a single chip. Microprocessors, microcontrollers, analog, and FPGAs are all examples of common semiconductor devices that are designed from integrated circuits.

Semiconductors are becoming increasingly important components of electronic equipment, especially as the number of "smart" and connected devices grow exponentially. As you can see in Chart 1, semiconductors have grown over the last 20 years from ~14% of electronic equipment bill of materials (BOM) to nearly 25% today. But it's not just smartphones and PCs that use chips anymore, modern semiconductors are now embedded into almost everything, from cars and washing machines to fighter jets. This means, having access to the most advanced semiconductor components is more and more critical to a successfully technology industry as well as military and national security.

Chart 5: Semiconductors now represent nearly 25% of electronic equipment bill of materials



Source: BofA Global Research estimates, Gartner

Semiconductor TAM was $412bn in 2019

Per SIA, worldwide semiconductor sales were $412bn in 2019, down from 2018 high of $469bn given a significant memory correction (memory sales down 33% in 2019). Over the last 5 years, semiconductor sales have grown at a compounded rate of 5%, or roughly 2-3x GDP. Integrated Circuits (ICs) excluding memory sales were $227bn in

2019, or 55% of all semiconductor sales. Memory sales were $106bn, or 26% of all semiconductors with the remaining 19% were discrete chips.

However, these raw numbers somewhat underestimate the importance of semiconductors. The global e-commerce industry is estimated to have revenues of over $2tn a year. So if data is the new oil, chips are the internal-combustion engines that turn them into something useful.

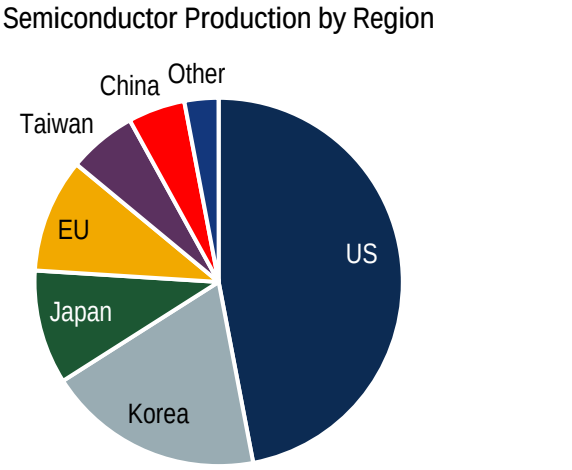
Table 1: Semiconductor sales have grown at compounded pace of 5% over the last five years, or 2-3x GDP

	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	CAGR 2015-2020
Semiconductor Sales ($bn)	$226	$298	$300	$292	$306	$336	$335	$339	$412	$469	$412	$437	5%
YoY (%)	*-9%*	*32%*	*0%*	*-3%*	*5%*	*10%*	*0%*	*1%*	*22%*	*14%*	*-12%*	*6%*	
IC Ex-Memory Sales ($bn)	$146	$180	$186	$181	$185	$198	$197	$200	$219	$235	$227	$238	4%
YoY (%)	*-10%*	*24%*	*3%*	*-3%*	*2%*	*7%*	*0%*	*1%*	*10%*	*7%*	*-4%*	*5%*	
Memory Sales ($bn)	$45	$70	$61	$57	$67	$79	$77	$77	$124	$158	$106	$119	9%
YoY (%)	*-3%*	*55%*	*-13%*	*-6%*	*18%*	*18%*	*-3%*	*-1%*	*61%*	*27%*	*-33%*	*12%*	
Discretes Sales ($bn)	$36	$48	$52	$53	$54	$59	$61	$62	$69	$75	$79	$80	6%
YoY (%)	*-10%*	*35%*	*8%*	*2%*	*1%*	*9%*	*4%*	*3%*	*11%*	*9%*	*5%*	*1%*	
Global GDP ($tn)	$60,340	$66,037	$73,358	$75,046	$77,190	$79,297	$75,002	$76,104	$80,886	$85,791	$88,450	$85,089	3%
YoY (%)	*-5%*	*9%*	*11%*	*2%*	*3%*	*3%*	*-5%*	*1%*	*6%*	*6%*	*3%*	*-4%*	

Source: BofA Global Research, SIA

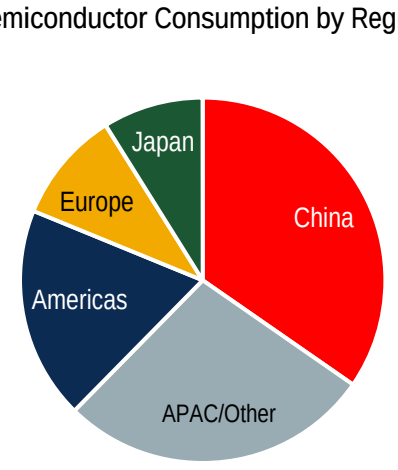
US-based semiconductor firms have the largest market share at 47% in 2019, per SIA. Korea is the second largest semiconductor market with 19% share, followed by Japan/EU at 10%, Taiwan at 6%, and lastly China at 5%. This is in stark contrast to the amount of semiconductors consumed by each region with China consuming nearly 35% of all semis in 2019, per SIA.

Chart 6: The US is the largest producer of semis at 47% of total...



Source: SIA

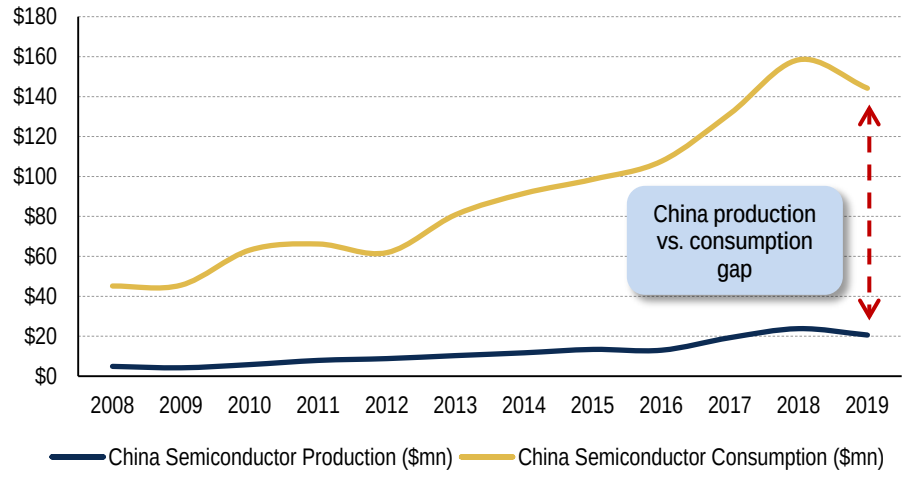
Chart 7: ...while China consumes nearly 35% of all semis



Source: SIA

To put that in context, this means that China has to import roughly $125bn worth of semiconductors (or 86% of all the semiconductors they consume), with the majority coming from the US (China purchases 1/3 of all US chip sales). That's because China is the leading hub for assembling finished chips into circuit boards, which are then embedded into finished electronics like TVs, smartphones, and laptops.

Chart 8: China semiconductor production vs. consumption

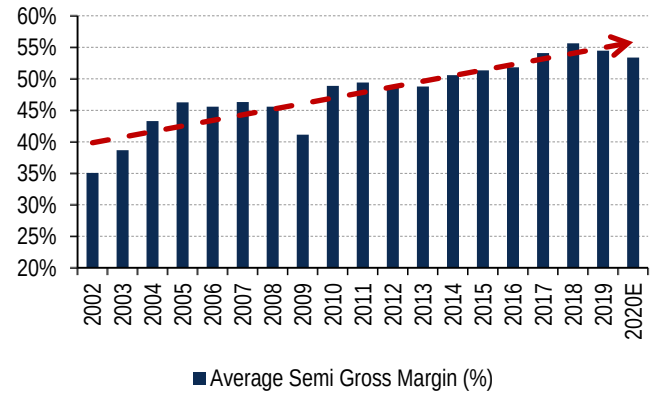


Source: BofA Global Research, SIA, IC Insights

The US has long seen its lead in chip making as a vital strategic asset. One of the earliest uses for semiconductors was in guidance systems for nuclear missiles. On the other hand, China has been eager to reduce its reliance on semiconductor imports due to fears that such dependence undermines China's own national security and hampers the development of a thriving home-grown technology sector. Below we outline some of the steps the Chinese government has taken to reduce its reliance on semi imports.

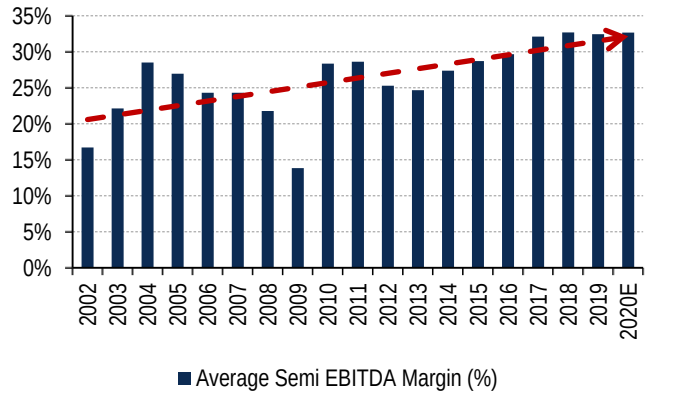
In additional to almost doubling in size over the last 10 years, the semiconductor industry is also much more profitable than it was 10 years ago, which we attribute to rapid consolidation and a more disciplined industry. As illustrated in the charts below, average semiconductor industry gross margins have expanded from low- to mid-40% in the early 2000s to roughly 55% today, while average EBITDA margins have expanded from 15-25% to over 30% today.

Chart 9: Avg semi GMs have grown from low- to mid-40% to 55% today



Source: BofA Global Research, company reports

Chart 10: Avg semi EBITDA margins are 1000-1500bp higher at >30%



Source: BofA Global Research, company reports

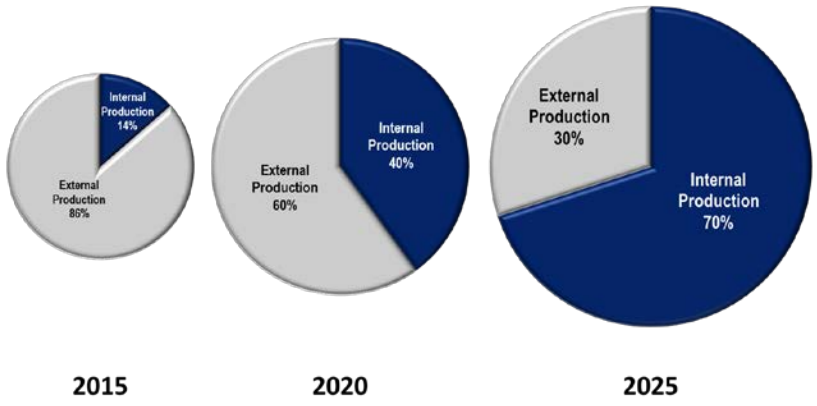
Made in China ambitions

For many years in China there has been a national imperative to increase self-sufficiency in semiconductor production. This desire has only been accelerated as the US increases pressure and limits access to key components on the country's top technology companies (like Huawei and SMIC). In 2014, the Chinese government established Phase-1 of the National Integrated Circuit Industry Investment Fund, or "IC Fund", which raised $20bn in funds and targeted opportunities focused mostly on IC design and manufacturing, with a small amount invested in equipment (1.2%) and materials (1.4%).

More recently, China has updated its "IC Fund" with Phase-2 announced in March 2020, which targets $30bn in funds with a significant portion focused in equipment and materials.

In 2015, the Chinese government's Ministry of Industry and Information Technology launched an aggressive initiative called **Made in China (MIC) 2025** – pushing for leadership in robotics, information technology, and clean energy. Among its various goals, MIC 2025 sought to produce 40% of its own semiconductors by 2020 and 70% by 2025, while accelerating its efforts in 14nm FinFETs, advanced packaging, MEMS, and memory. While the end goal of the MIC 2025 was self-sufficiency for domestic companies, China could then enable Chinese companies to compete for greater foothold in global markets.

Exhibit 2: Made in China 2025 Internal production goals



Source: BofA Global Research

US response to Made in China 2025

To the US government, the MIC 2025 policy was a prime example of how China's development model promotes unfair competition and disadvantages US businesses by subsidizing Chinese companies and limiting market access to foreign ones. Some of its biggest critics have argued the China's ambitious targets to transition the country from one known for making toys and cheap plastic tchotchkes, to one that leads in advanced technologies (like AI, autonomous vehicles, robotics, and 5G) motivate the more questionable behaviors US officials have accused China of, including forced technology transfer and cyber theft.

In response to these alleged unfair trade practices, in July 2018 President Trump implemented the first China-specific tariffs (25% tariff on 818 imported Chinese products valued at $34bn) imposed sweeping tariffs on China which kick-started what has evolved in to an all-out trade war between the US and China. So far the US has applied tariffs on $550bn worth of Chinese products. China in turn has set tariffs on $185bn worth of US goods.

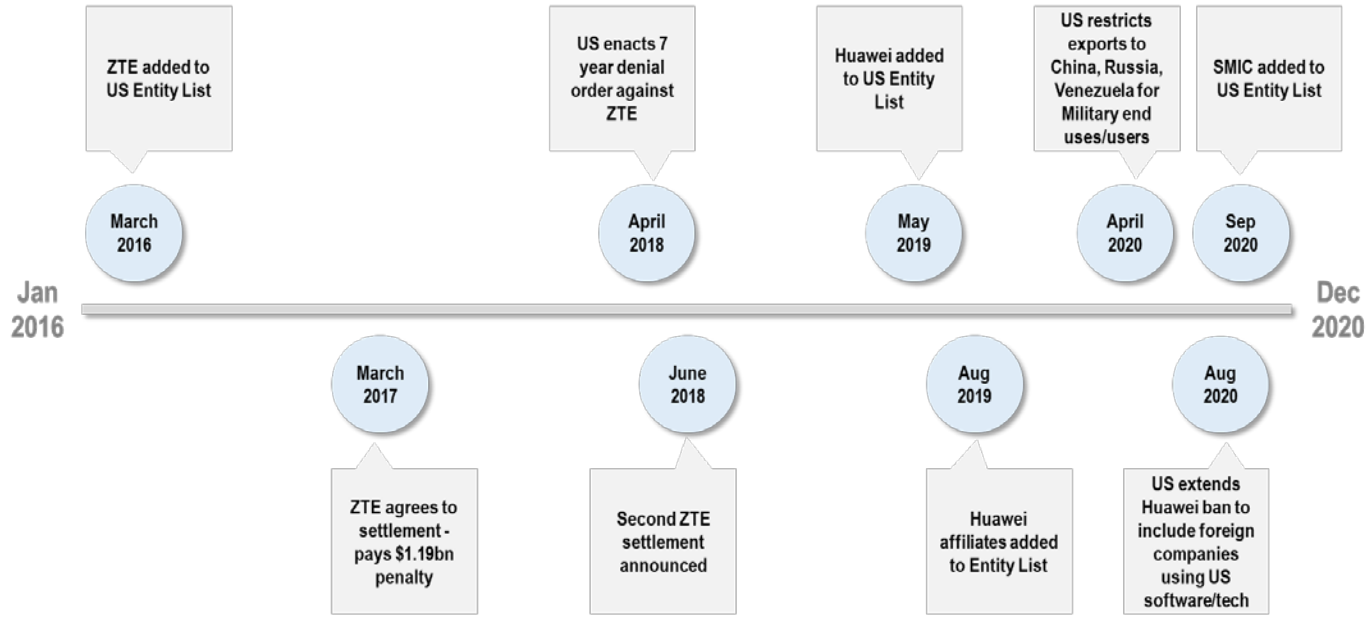
Other restrictions by the US government have been company specific. The first of which was when the US Department of Commerce (DoC) added ZTE to the "Entity List" in March 2016, meaning US companies could not sell goods or services to ZTE without a license. In March 2017, ZTE reached a settlement with the US government and paid a $1.19bn penalty. Then in April 2018, the US again enacted a denial order against ZTE for violating the terms of the March 2017 settlement, which prevented ZTE from buying US components again. This ban was short lived and in June of 2018 the US and ZTE agreed to a deal where ZTE had to: (1) pay $1bn in penalties (and place an additional $400mn in suspended penalty money); (2) retain a team of special compliance coordinators selected by and answerable to the US Department of Commerce's (DoC)

Bureau of Industry and Security (BIS) for a period of 10 years; and (3) replace the entire board of directors and senior leadership.

A little over a year later, in May 2019 the US DoC added Huawei to its "entity list" which effectively bans US companies from selling to the Chinese telecommunications company without US approval. Later on, in May and August 2020, the US extended the Huawei export ban to include semiconductors developed outside the US but use American software or technology. The idea was to present foreign manufacturers like TSMC and Samsung with a choice: in order to access American-made tools used to fabricate semiconductors, those companies would need to agree not to sell to Huawei.

More recently, in September 2020, the Trump administration issued new restrictions on US technology exports to China's largest semiconductor manufacturer, SMIC. US companies now need licenses to export certain technology to SMIC since these exports to SMIC may pose an unacceptable risk of diversion to a military end use in China.

Exhibit 3: Timeline of US export restrictions on Chinese entities



Source: BofA Global Research

How does 5G fit in to US/China trade tensions?

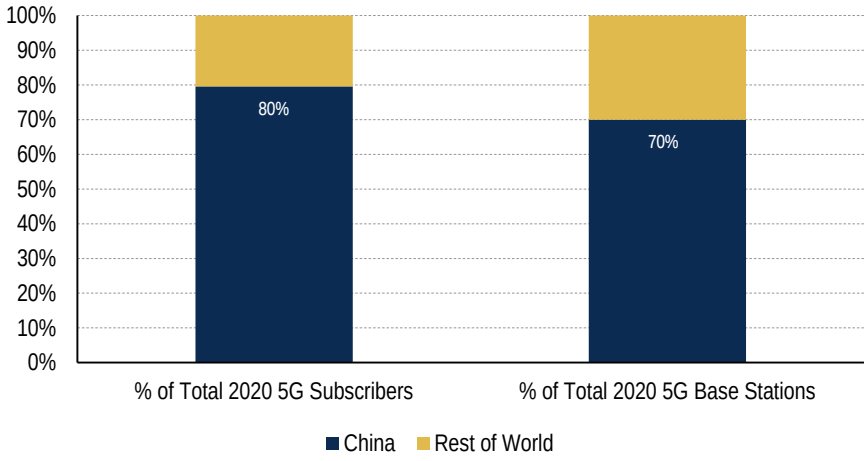
To put it simply, 5G has everything to do with the escalating trade tensions between the US and China. 5G, the next generation wireless network will not just allow you to download an entire Netflix series in seconds, but it will also serve as the foundation to support the next generation of data infrastructure, including billions of connected devices powering smart cities, VR and AR applications, AI, and driverless cars.

Being first to the next generation wireless network is crucially important for any nation looking to leading in the technology of tomorrow. Using 4G as a guide, if the US hadn't led the way the country may not dominate mobile technology and its platforms (Instagram, Snapchat, Facebook, Netflix). A study commissioned by U.S. wireless trade association CTIA concluded that America's 4G leadership led to roughly $125bn in revenue for U.S. companies that could have gone elsewhere had the country not been at the technology forefront. While it's impossible to know what new innovations will come from 5G, being first could give a country an important competitive advantage. So what is at stake in the global 5G race is much more than just bragging rights; in our view, the outcome could determine whether or not the US will continue to maintain its technological edge or if it will cede that position to China. On China's part, leading in 5G is an opportunity to surpass the US and the West to become the economic and geopolitical superpower it has long wanted to become.

China's government has poured massive amounts of money in to companies such as Huawei to develop 5G technologies, and to great success. As of 2020, no other country comes close to China in terms of broad 5G investment and infrastructure deployment. By the end of 2020, China is expected to have ~700K base stations deployed to support advanced 5G capabilities – this is more than 2x the number of 5G base stations outside China, according to China's Ministry of Industry and Information Technology (MIIT) vice-minister Liu Liehong. This has been necessary to support the roughly 175mn 5G subscribers in China, which is a large majority (80%) of the total 5G subscriber base in 2020 of 220mn, per Ericsson Mobility Report. Meanwhile, there are no major US companies building 5G telecom equipment due to decades of market consolidation.

In addition, the Chinese government control's China's wireless service market and is pushing its three major providers (China Mobile, China Unicom, China Telecom) to combine efforts to develop a nationwide standalone 5G network. The US's free market approach makes getting a nationwide 5G network built quickly more of a challenge as the major US wireless companies struggle to balance intense competition with network investment and innovation for 5G.

Chart 11: China has 5G lead with roughly 80% of 5G subscribers and 70% of 5G base stations in 2020



Source: BofA Global Research, Ericsson Mobility Report, China MIIT

But the largest issue for the US, according to a Defense Innovation Board report, is that the country hasn't been quick enough to making available the wireless spectrum essential to deploying the service. While China has quickly reallocated its spectrum, the US airwaves have been tied up in disputes between military and other federal agencies fighting for allocation.

US efforts to catch up with China on 5G could force the rest of the world to choose sides in a tech cold war. US officials have already cautioned companies that Huawei gear could be used by the Chinese for intelligence efforts. This concern was one of the major factor in the US adding Huawei to its Entity List. In February 2020, Defense Secretary Mark Esper warned European countries that they could jeopardize their alliances with the U.S. if they used Huawei gear in their 5G networks. While some countries, like Australia and Japan, have heeded the U.S. warnings, others including Germany and Saudi Arabia continue to work with Huawei.

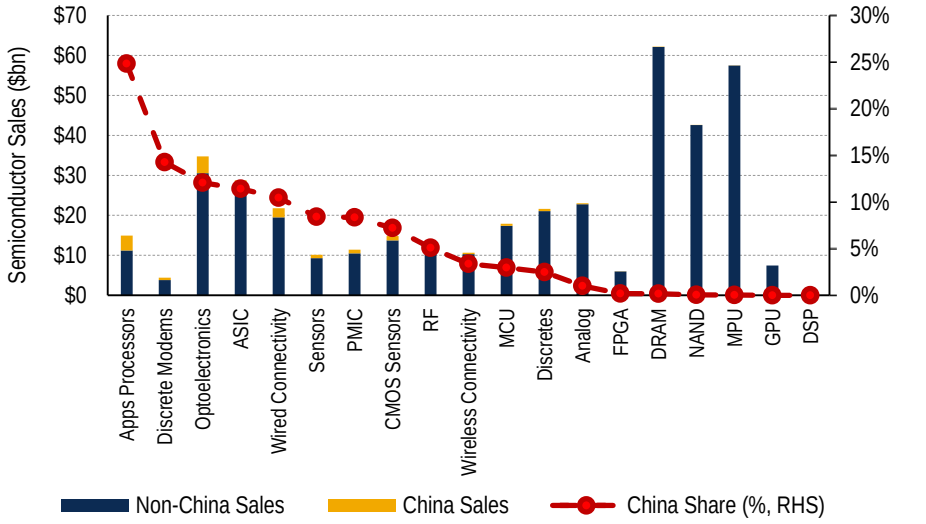
Summary of domestic China semiconductor strengths and weaknesses

While domestic China semiconductor companies represent just ~5% of total semiconductor sales, per SIA, there are some product categories where China has been much more successful. Chart 4 outlines China domestic semi share by product category.

China has had the most successes in integrated application processors and secrete modems (used in smartphones) due to HiSilicon's success in these areas. Importantly,

there are key semiconductor categories where China still has little to no position, including analog semis, FPGAs, DRAM/NAND memory, MPUs, and GPUs. These are categories that can continue to be very difficult for China to break in to without access to US design and manufacturing equipment and years of experience.

Chart 12: China share highest in Apps processors/modems, lowest in analog, FPGA, memory, MPU, GPU



Source: Gartner

Manufacturing basics: foundry vs. IDM

Semiconductor manufacturing involves one of the most sophisticated processes in modern mass production of any product. Today a single chip, about 1 square inch in size, can contain billions of interconnected transistors. In fact, because of the complexity associated with atomic-level fabrication and design, it actually costs more to make a chip than it does to make a plane. A state-of-the-art chip factory (known in the industry as a **fab**) cost $18-$27bn to build and operate (per SIA) and relies on tens of thousands of global suppliers for key inputs, including equipment and materials.

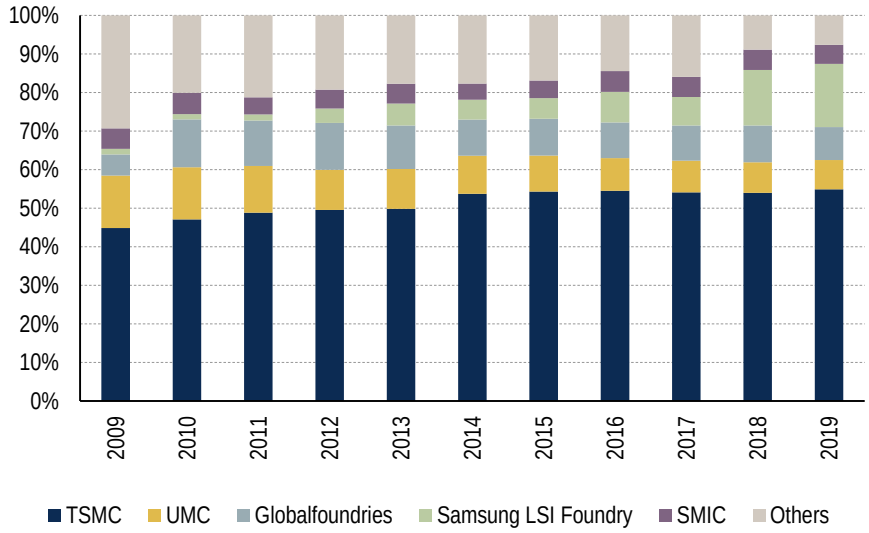
Unlike most traditional manufacturing processes in other industries, where products are individually made one after the other, chip manufacturing is done simultaneously in "batches" on a single round silicon disk, known as a **wafer**. Multiple chips are made on a single wafer (each chip on the wafer is commonly referred to as a **die**). The actual chip fabrication process requires hundreds to thousands of different steps that are executed at an atomic scale. From start to finish, including fabrication, testing and packaging, it takes about 3 months to make a chip. The three main phases of the chip production process include: (1) wafer manufacturing, (2) the actual chip fabrication or the "front-end process", and (3) assembly & packaging or the "back-end process".

There are two main types of business models today in the industry – companies either design and manufacture their chips, or just design and outsource manufacturing. Companies that employ the former strategy are known as **integrated device manufacturers (IDMs)**. On the other hand, companies that just design their chips and outsource manufacturing to **foundries** (which only manufacture pre-designed chips for their customers) are known as **fabless** semiconductor companies.

In the early to mid-2000s the industry shifted to the foundry model, because it allowed companies to focus on design and reduce capex burdens associated with manufacturing. Today most memory companies (Samsung, SK Hynix, Micron) still employ the IDM business model, and the largest remaining logic IDMs are Intel, Texas Instruments, Infineon, and STM. However, the vast majority of companies today rely either entirely on foundries or a mix of internal and outsourced manufacturing. The main foundries are

Taiwan Semiconductor Manufacturing Company (TSMC, 55% share), Samsung (16% share), GlobalFoundries (9% share), Semiconductor Manufacturing International Corp (SMIC, 5% share), and United Microelectronics Corp (UMC, 8% share).

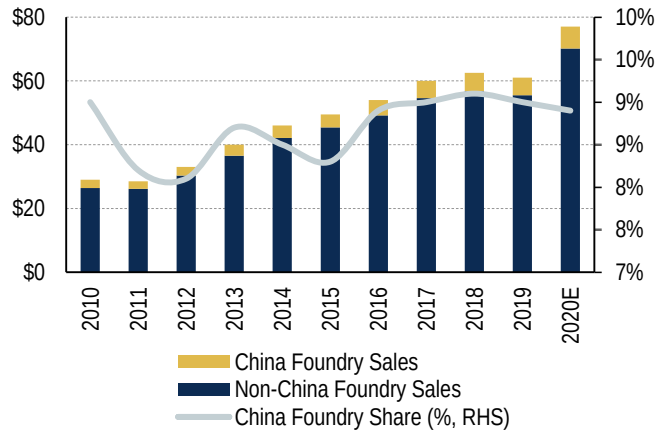
Chart 13: TSMC is foundry market share leader with 55% share but Samsung share is growing



Source: BofA Global Research estimates, company data, Gartner

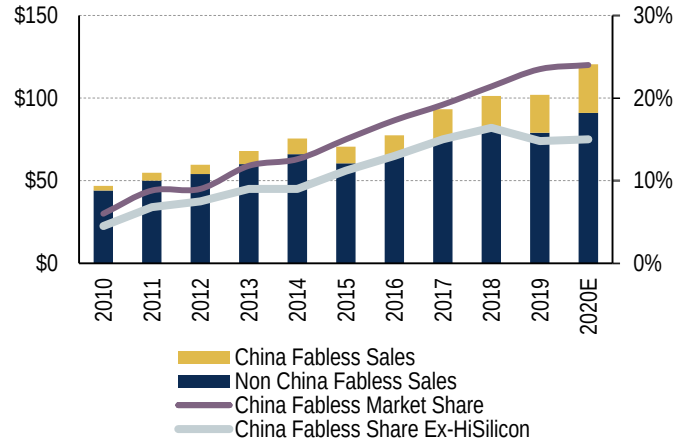
While China has had some success with its fabless semiconductor companies (fabless share has grown to nearly 25% from just 5% ten years ago), it has not had as much success growing its own domestic semiconductor manufacturing industry. China's largest foundry, SMIC, which was founded in 2000, has roughly 5% of foundry share today, unchanged from ten years ago. China's overall foundry share has remained within an 8-9% range over this time period as well.

Chart 14: China foundry share has remained in 8-9% range since 2010...



Source: BofA Global Research estimates, company reports

Chart 15: ...while fabless share has grown from 5% to nearly 25%

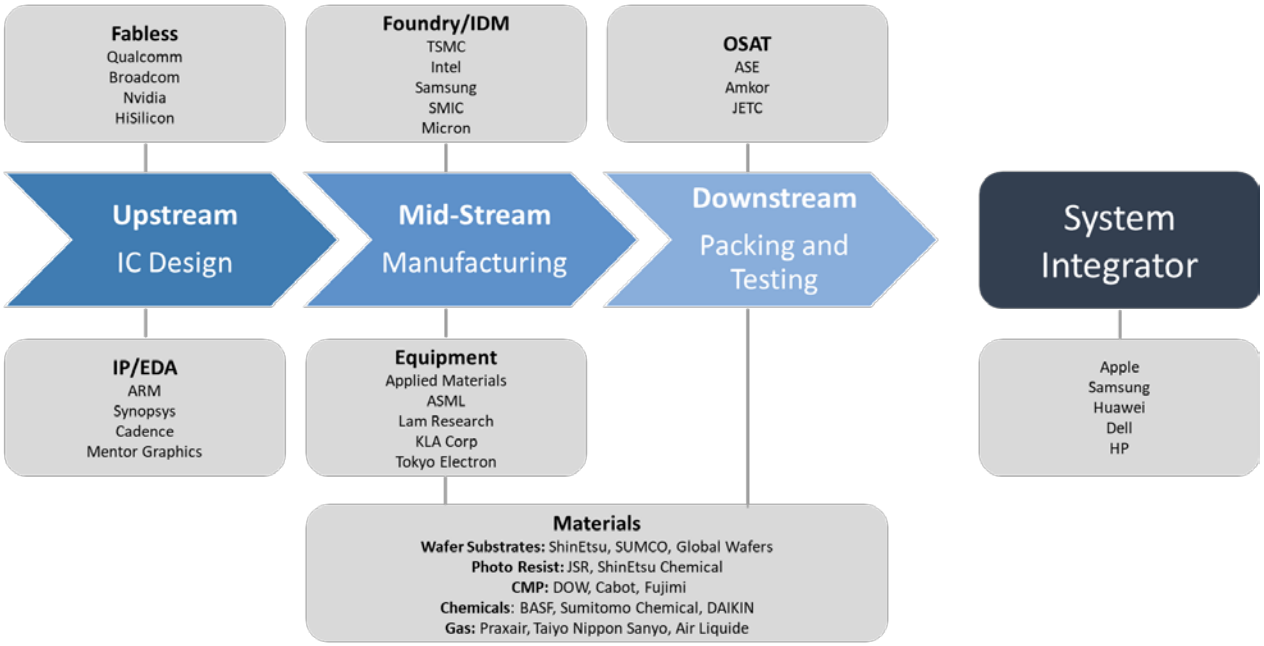


Source: BofA Global Research estimates, company reports

Semiconductor value chain intricate and global in nature

The semiconductor industry has an extraordinarily complicated supply chain that stretches from fabs to back-end factories all the way to the world's leading electronics companies. Carrying out each step in the supply chain requires great specialization and offers a chance to add significant value; thus the supply chain becomes a value chain, with each activity contributing to the overall competitive edge of the final product. Few industrials have a value chain and ecosystem so complex, geographically widespread, and intertwined. In exhibit 2, we outline the major steps in the semi supply chain.

Exhibit 4: Semiconductor supply chain spans from design to manufacturing to packaging/testing all the way to the world's leading electronics companies



Source: BofA Global Research estimates

Furthest upstream is IC design. This is the process of transforming the structural description of the logic circuitry into a detailed physical layout. Here fabless semiconductor companies (like Qualcomm, Broadcom, Nvidia, HiSilicon) or IDMs (Intel) use Electronic Design Automation (EDA) software tools to design and verify their chip designs. Alternatively, companies can license pre-designed blocks (or IP) of circuits for commonly used functions that can be used in the designs of complete semiconductor devices.

Next is IC manufacturing where foundries (TSMC, SMIC) or IDMs create electronic circuits on wafers using photolithographic and chemical procedures with equipment from semicap equipment vendors (Applied Materials, Lam Research, ASML).

Lastly, the semiconductor is packaged to provide protection as well as an interface that connects internal electrical signals to the system through pins and tested to ensure the dies meet their electrical specifications. It is then integrated into a circuit board and combined with the rest of the system.

The semi supply chain is not just complex, it is also extremely global in nature. A typical journey along the semiconductor supply chain may start with sand shipped to Japan to be turned into pure ingots of silicon. These are then sliced into standard-sized wafers (300mm across) and sent to a fab, perhaps in Taiwan or South Korea. Here the slices will be imprinted with a particular pattern using photolithography equipment made in the Netherlands while being measured and tested by equipment made in the US. The particular pattern on the chip will be determined by the design of the chip, which might come from Arm (based in Britain) or might be made using design tools from US based Synopsys or Cadence. Once finished, it must be assembled into a package and finally tested, which might take place in China, Vietnam or the Philippines. This is then integrated into a circuit board, which could happen somewhere else altogether.

In Table 8 we summarize China's positioning throughout the semi supply chain. China has had the most success in assembly & test where they boast 28% share. China has moderate share in semiconductors such as application processors, MEMS, and discrete chips, as well as in legacy (28nm and above) manufacturing. China has had little success

in memory/CPU/analog chips, advanced manufacturing (14nm and below), IP, EDA, and materials. Notably, China has no position in advanced front-end equipment.

Table 2: Global market share of Chinese companies throughout the semiconductor supply chain

Field	Sub-Category	Global Market Share of Chinese Companies	Representative Chinese companies
Fabless & IDM	Memory	2%	YMTC, Changxin
	CPU/MPU	1%	Longxin, Zhaoxin, Feiteng, Zhongwei
	AP/BP	20%	HiSilicon, Spectrum, JLQ
	MEMS/Actuator	10%	Manufacturer: Silan, Silex Product : Goertek, ACC
	Other Logic	13%	Gigadevice, Sino Wealth, Actions Technology, China Resources Microelectonics, HDSC
	Analog	2%	SG Micro, Will Semi
	FPGA/CPLD	1%	Capital Micro, Gowin, Unisemicon, Analogic, Intelligence Silicon
	Discrete	25%	WeEn, Yangzhou Yangjie Electronic, Jiejie Microelectronics
Manufacturing	14nm and below (advanced)	1%	SMIC
	28nm and up (mainstream)	20%	SMIC, HHGrace
	8-inch matured tech	18%	SMIC, HHGrace
	Compound Semiconductor	2%	Sanan
	Special Analog	1%	
Assembly & Test		28%	JETC, TFME, Hua Tian
Equipment	Front-end advanced	0%	
	Front-end Mainstream	4%	AMEC, NAURA, SMEE, ACM
	Back-end	6%	Changchuan Tech
Materials		2%	Konfoong Materials, NSIG, Sinyang Semiconductor Materials
IP		1%	ARM (China)
EDA		1%	Emprean

Source: IC Wise, company press and announcement
Note: 1% is the estimated number if the market share is negligible

Internal silicon efforts

One trend that has been evolving over the last several years but has picked up steam more recently is the trend of large hyperscale/cloud/tech customers building their own custom silicon. Creating internal silicon has become more feasible now that foundries (like TSMC) are manufacturing at the leading edge and have surpassed Intel on its technology roadmap. Outsourced manufacturing combined with pre-defined silicon processor IP from Arm has enabled a number of new competitors in the PC and server market. Below we outline some significant internal silicon efforts:

Apple

Apple has long set a precedent of manufacturing some of its chips (e.g. apps processor) internally, and has added to this effort with its recently announced M1 processor, its first chip designed specifically for Macs. The M1 is a 5nm, 16 billion transistor, Arm-based CPU, which replaced Intel's x86-based CPUs previously used in Macs.

Google (Tensor Processing Unit)

In early 2016, Google revealed that it had created a custom AI chip dubbed the tensor processing unit (TPU). The application specific integrated circuit (ASIC) was designed to provide more energy efficient performance for the company's deep learning AI applications. The chip formed the foundation for TensorFlow, the framework used to train the company's AI systems. Google is expected to release its fourth generation TPU in the coming months, which they say demonstrates 2.7x higher performance vs. the third-generation (released in 2018)

Amazon

Amazon bolstered its processor expertise with the $350mn acquisition of Annapurna Labs in early 2015. Then, in 2018, Amazon put this knowledge to use by debuting a new processor chip designed for cloud computing and machine learning called Graviton. This

Arm-based processor is publicly available in Amazon's AWS EC2 'A1' instances. In late 2019, Amazon doubled down on this efforts by announcing Graviton2, the next gen of this Arm-based SoC with 7x higher performance vs. the first gen and 5x higher memory access speed. Even more recently, in December 2020, Amazon debuted AWS Trainium, a custom chip designed to deliver cost-effective machine learning training in the cloud. AWS promises 30% higher throughput and 45% lower cost-per-inference compared to standard AWS GPU instances. These new chips will debut in AWS cloud in early 2021.

Facebook

In early 2019, Facebook's Chief AI researcher told Bloomberg the company is working on a new semi design made specifically to handle the massive amounts of data used in AI. The company wants to develop semis that can better train deep learning algorithms by manipulating data all at once instead of having to break it down into manageable tasks. Still, to date nothing has officially been announced.

Tesla

In late 2017, we learned that Tesla was attempting to build its very first computer chip for its self-driving vehicles. Then, in 2019, Tesla announced the new chip manufacturing by Samsung as part of its Hardware 3.0 (HW 3.0) self-driving computer. Tesla claimed a 21x improvement in frames per second processing vs. the previous generation Tesla Autopilot hardware which was powered by Nvidia. More recently, media reports have suggested that Tesla is working on its next gen HW4.0 self-driving chip with TSMC expected for mass production in Q4 2021.

Megatrends driving semiconductor growth

In this section we briefly outline the key secular themes that are driving semis growth over the next few years. These themes include AI, cloud computing, memory, 5G, IoT, autonomous and electric vehicles, and gaming.

Exhibit 5: Key megatrends driving semiconductor demand over the next several years

MEGATREND:	WHAT?	WHY IMPORTANT?
The rise of Artificial Intelligence / Machine Learning	Artificial Intelligence is the concept that machines attain human-like intelligence. Machine learning is a subset of AI and consists of taking some data, training a model on that data, and using the trained model to make predictions on new data	Implications can range from speeding up drug discovery, automating transportation, smart online assistants, detecting anomalous behavior, etc. This, in turn, will drive greater demand for high speed compute and storage. $25bn TAM by 2022E, up 58% annually
The shift from enterprise to cloud data centers	Data center infrastructure is shifting from a rigid hardware-centric on-premise ecosystem commonly employed by enterprises, to a more dynamic ecosystem known as the "cloud"	Cloud adoption is expected to drive overall growth in data center infrastructure spending. $90bn TAM by 2022E, up 13% annually
Memory is critical to enabling data growth and analytics	Memory chips, which store data temporarily (DRAM) or permanently (NAND), are used in virtually all electronic goods including smartphones and cellular phones, PCs, TVs, servers, communications infrastructure, etc.	We are approaching an inflection point in data traffic, which will be propelled by the proliferation of connected devices. Memory is essential to the data growth paradigm and becomes even more critical in a data driven economy
5G as the next wireless network to enable new applications	5G is the fifth generation of wireless technology for mobile networks – each generation is typically characterized by data transmission speeds and capacity	Faster speeds, increased capacity, and reduced latency will support the growing insatiable demand for mobile data, and will enable new applications such as connected cars, IoT (including smart cities, healthcare, industrial, agriculture, etc), and AV/VR
The proliferation of the Internet of Things (IoT)	IoT can be defined by the wave of devices that will be connected to the internet. This includes washing machines, wearables, smart home assistants (Amazon Echo), and machinery such as autonomous vehicles, and factory equipment.	We expect IoT device chip sales could more than double to over the next 2 years. $43bn TAM by 2021, up 25% annually
Autonomous and electric vehicles "drive" new era of transportation	Autonomous vehicles are cars that can drive completely independent of human interaction. Electric vehicles are cars that run on electricity instead of fuel	Semiconductor content in autonomous and electric vehicles is significantly higher than that in traditional automobiles. $60bn TAM by 2022E, up 30% annually
Robust PC gaming secular tailwinds to continue	2bn people – or 1/3 of the global population – game today. Of that 2bn, approximately 400mn "core gamers" – or people who game at least once per week. The key enabler of the cinematic realism many have come to expect from the AAA game titles available today is a semi component known as a graphics processor or GPU.	As the production value of games continues to increase, gamers need to either replace their PC (with one that has a higher performance GPU) or upgrade the graphics capability of their existing rig by buying a standalone, higher performance graphics card. This virtuous cycle has driven strong secular growth for discrete GPU's.

Source: BofA Global Research, Gartner, IDC

The rise of Artificial Intelligence (AI) and Machine Learning

Artificial Intelligence, or AI, is the overarching concept which refers to a machine exhibiting human intelligence. Machine learning is a subset of AI and consists of taking some data, training a model on that data, and using the trained model to make predictions on new data. The two main steps in machine learning are training and inference. Training involves teaching a neural network to recognize objects, voices etc., just like the neurons in a child's brain are taught to do so by school teachers. In the inference phase, the model gets put to actual use – small amounts of data are sent through the model to get an inferred output.

Digital processing chips are enabling computing devices to achieve human sight/sound/perception and to continuously learn and make predictions from the explosive amount of unstructured text, images, sound and video. The ability of machines to see, hear, learn, predict, and correct with superhuman abilities requires cognitive abilities matching the brain with its 100 billion neurons and 1 trillion bits per second of processing. It requires massive amounts of parallel computation, which is only feasible with graphics processors from Nvidia, programmable chips from Intel and Xilinx, and other ASIC/accelerators from Google, IBM, and others

Shift from enterprise to cloud data centers

The recent shift from traditional enterprise data centers to the cloud has disrupted the data center infrastructure landscape. Essentially, data center infrastructure is moving from a hardware-centric, rigid ecosystem dominated by a few hardware vendors, to a more dynamic system of generic or white-box hardware running open-source software that provides customers with greater agility, flexibility, improved economics, and enhanced security for new complex workloads. Large cloud customers such as Amazon, Facebook, Baidu and Google are leading this charge and driving greater economies of scale in generic hardware.

Despite the continued adoption of the cloud, traditional enterprise still accounted for the majority of data center hardware spend ($140bn in 2018), representing roughly 53% wallet share with the balance coming from cloud.

Memory critical to enabling data growth and analytics

Memory refers to semiconductor chips that store data either temporarily (DRAM - dynamic random access memory) or permanently (NAND). DRAM assists processors (non-memory/logic) only when PC, smartphones, servers, etc are running (power-on), while NAND retains the data generated by the processors even when switched off. Memory plays a critical role in the tech ecosystem, which is dealing with more data than ever. Processors can still work without DRAM, but performance (data speed, etc) will be inefficient immediately. Further, the data that processors generate are stored in NAND given quite limited space of both DRAM and logic.

Memory chip demand is more diversified with mobile (about 35% of 2018-19 DRAM demand) and cloud/enterprise (30%). PC (sub-20%) is no longer mainstream (for DRAM demand), but it represents a spot market as a commodity application. Auto and 5G networks consume low-single-digit percentages of global memory supply.

5G as the next wireless network to enable new applications

Fifth-generation or 5G will be the next major iteration of the mobile industry's technology evolution that started in the 1980s with 1G (voice-only). Every generation (2G, 3G, 4G/LTE) has boosted the download speeds on mobile devices enabling new data services. The last major transition from 3G to 4G kicked-off in 2008, supporting download speeds of 1 Gigabit/second (Gb/s) in stationary and 100 Megabits/second (Mb/s) when the subscriber is mobile. 5G promises to provide a 10x+ jump, with peak download speeds over 10 Gb/s and mobile speeds exceeding 1 Gb/s.

Mobile data traffic is expected to grow five-fold by 2024 to nearly 24 Gigabytes per user per month from around 5 GB last year, per GSMA. So there is an ever-expending need for more mobile data. However, 5G also enables much lower levels of latency (connection speed) and the ability to create and provision much more secure levels of service. Hence the really big deal about 5G will be the support for smarter, more secure enterprise services in the industrial/manufacturing, healthcare, utilities, public services and other professional services areas. 5G could also provide enough capacity to serve as a last mile alternative to deploying expensive fiber to the home. Overall, 5G could drive nearly $2.2 Trillion in global economic activity over the next 15 years, per GSMA, the telecom industry's trade association.

The proliferation of the Internet of Things (IoT)

The Internet of Things (IoT) can be defined by the wave of devices that will be connected to the internet. This includes appliances such as washing machines, consumer devices such as wearables, artificial intelligence (AI) equipped home assistants (Amazon Echo), and machinery such as autonomous vehicles, and factory equipment. The processing, sensing and connectivity required to cost-effectively connect the explosion of connected things could be one of the next big growth drivers for the semi industry.

In order to take a "dumb" device and make it into a "smart" IoT endpoint, three fundamental semiconductor building blocks are required: (1) processors via microcontrollers (MCU), microprocessors (MPU), or application specific standard products (ASSP); (2) sensors/analog products (such as pressure, temperature, light, sound, etc.) which can recognize real world analog signals and translate them into the digital domain; and (3) connectivity semis such as Wi-Fi, Bluetooth, Zigbee, Cellular, and Radio Frequency products which transmit and receive data to/from the internet.

Autonomous and electric vehicles "drive" new era of transportation

Government mandates for better fuel efficiency standards and safety are key drivers of growth in the autonomous vehicle (AV) and electric vehicle (EV) markets. Chips, particularly those with higher compute capabilities, are driving newer generations of ADAS and battery and engine management systems.

Autonomous vehicles are a vision of the not too distant future in which a vehicle can drive itself from point A to B without human input. Autonomous cars/trucks have the potential to improve safety and convenience while reducing transportation costs. Nearly every major car manufacturer today is developing autonomous driving tech that will be made possible through the use of various sensors, lasers, radars, cameras, advanced driver assistance systems, software, GPS, and wireless data communication systems. At the heart of an AV is a control system which consists of two primary functions: (1) the "eyes" which are responsible for preprocessing images collected from the cameras placed around the car in order to isolate objects of interest; and (2) the "brain" which identifies the objects, controls the vehicle, and calculates an optimal path.

Increasingly stringent greenhouse gas (GHG) emissions standards and fuel economy regulations have prompted automotive OEMs to invest heavily to improve vehicle efficiency, specifically through the development of electric (EV) and hybrid electric vehicles (HEV). With regards to semiconductors, emission targets drive a few significant trends all of which necessitate higher semis content including: (1) higher fuel efficiency of the classic internal combustion engine (ICE) vehicle through adoption of features such as electric power steering, start-stop, dual-clutch, alternators; (2) improved energy efficiency of body applications (power distribution, electric motors for pumps and fans); and (3) the electrification of the drivetrain (the group of auto components that deliver power to the driving wheels).

Robust secular PC gaming tailwinds to continue

The current global health crisis has created significant near-term gaming demand (particularly for high-end gaming GPUs and next generation gaming consoles) as

consumers continue to live, work, and play from home. Longer-term gaming, and game related artistic creation across multiple media formats (YouTube, Twitch, etc.) is a structural growth industry that requires significant computing power from key GPU vendors, Nvidia and AMD.

Performance requirements for core PC gamers are typically much higher than the average PC user. Fueled by the increased graphics requirements of games with perpetually increasing production quality, gamers have increasingly gravitated toward mid-to-higher end graphics cards in order to squeeze the most performance out of their systems and render the most visually enriched version of a game possible.

Difficulty of leading edge manufacturing

The guidepost for innovation in the semiconductor industry over the last 50+ years has been **Moore's Law**, which is the observation that the number of transistors (building blocks of chips) per square millimeter should double approx. every 2 years. The observation was coined by Gordon Moore (co-founder of INTC) in 1965. By shrinking transistors, companies can increase a chip's density (the # of transistors per chip) and thus drive improved performance (more transistors per chip, better the performance).

A **technology node**, or process technology, refers to a specific generation of semiconductor manufacturing process and its design rules. Different nodes often imply different circuit geometries and architectures. The smaller the technology nodes, the smaller the feature size, which in turn means smaller transistors which are faster and more power-efficient. Historically, the process node name referred to a number of features of a transistor including the gate length and half-pitch. More recently, due to discrepancies among foundries/IDMs, the number has lost the exact meaning it once held. Back in the early 1960s, the original chips were built on 50 µm (or 50K nm) while today's most advanced chips are built on 10nm/7nm/5nm process technologies.

However, Moore's Law is not a law of physics – instead, it is more of an economic observation; the growth in the number of transistors per squared millimeter of a chip (due to smaller transistor sizes) more than offsets the higher cost per squared millimeter of a chip, causing the actual cost per transistor to decline. This has led to smaller, faster, and less expensive chips, which in turn has accelerated adoption of semiconductor devices across various applications. For example, today notebook PCs are more powerful than mainframe servers that could fill a room decades ago.

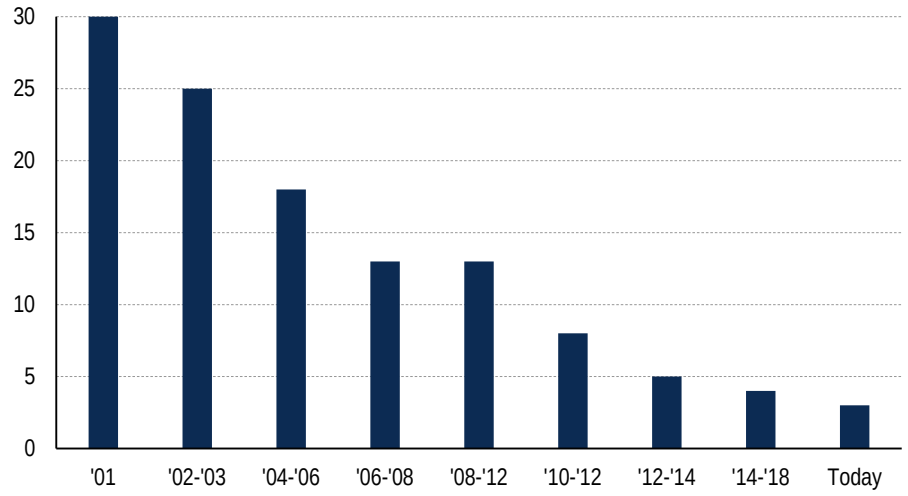
To put this into context, Intel's 14nm processors deliver 3,500x higher performance, are 90,000x more power efficient, and the price/cost per transistor is 60,000x lower compared to the first processor ever made. To draw a more tangible analogy, if cars had progressed at the same rate, they would be able to achieve 300,000 miles per hour speeds, get 2,000,000 miles per gallon, and only cost 4 cents.

Only 3 remaining logic manufacturers at the leading edge

As recently as 2001, 30 companies manufactured leading edge chips. As time has progressed and leading-edge semiconductors have become more difficult and costly to manufacture, that number has dwindled to 3 remaining firms: TSMC, Samsung, and Intel.

TSMC and Samsung are really the only two options for fabless semiconductor companies looking to produce chips on leading edge nodes. Intel on the other hand just produces these chips internally. While more recently Intel has delayed its manufacturing roadmap (7nm process technology pushed out to late 2022/early 2023) we still consider it as one of the vendors manufacturing at the leading edge.

Chart 16: The number of leading edge logic manufacturers has fallen from 30 in 2001 to just 3 today



Source: SIA, Intel

Moore's Law not dead yet, but slowing

More recently, the state of Moore's law is somewhat unclear. Already, the billions of transistors on the latest chips are invisible to the human eye. If Moore's Law was to continue through 2050, engineers would have to build transistors from components that are smaller than a single atom of hydrogen. As the scale of chip components gets closer and closer to that of individual atoms, it will be significantly harder to keep up the pace of Moore's Law. Indeed, in 2016, Intel announced that it is slowing the pace with which it will launch new chip technology nodes from its historical 2 year cadence to 3 years.

Still, leading edge manufacturers have found ways to continue to scale. As of 2020, TSMC and Samsung are ramping their 5nm process technology while Intel is still on its 10nm+ (known as 10SF or 10 SuperFin) node which is similar to TSMC/Samsung 7nm. China's largest foundry (SMIC) is still on more legacy 14nm process technology, which is 5+ years and 2-3 generations behind TSMC, Samsung, Intel.

Table 3: Process node roadmap comparisons of key semiconductor manufacturers

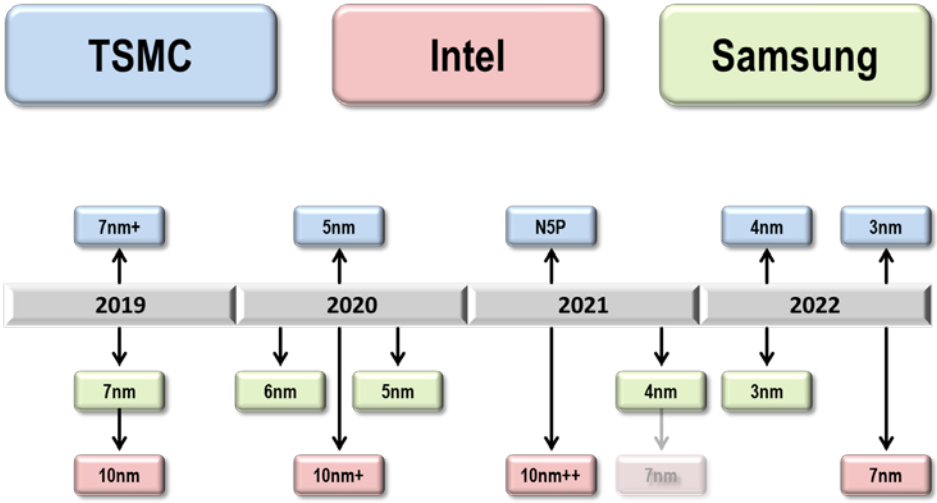
	1H17	2H17	1H18	2H18	1H19	2H19	1H20	2H20
TSMC	10nm		7nm				5nm	
Intel	14nm					10nm		
SMIC	28nm					14nm		
Samsung	10nm			7nm				5nm
UMC	14nm							
GF	14nm							

Source: BofA Global Research estimates, company data

Intel recently delayed its next generation 7nm process technology (TSMC/Samsung 5nm equivalent) until late 2022 or early 2023, causing them to fall further behind TSMC and Samsung which are already ramping their 5nm technologies and are already looking ahead to 4nm/3nm and beyond.

While SMIC is currently on a lagging 14nm process technology, recent media reports (from China.org.cn) have suggested that SMIC is ready to introduce its N+1 node, which some reports say is comparable to an 8nm process note, or an early, low-performance variant of the 7nm node, and marks a significant improvement over its current 14nm node (20% increase in performance, 57% power consumption reduction, 63% reduced logic area, per SMIC). Still continued scaling will get more and more difficult for SMIC without access to key EUV lithography equipment, which we discuss in more detail later.

Exhibit 6: Roadmaps for remaining 3 leading edge logic manufacturers



Source: BofA Global Research

Advanced packaging could augment the future of scaling

As scaling becomes more difficult and expensive at each node, the price/performance benefits are diminishing. Even for customers that can afford the high cost, some of the die sizes are running up against the maximum reticle size, resulting in yield challenges that further exacerbate the cost problem. So, while scaling will continue, not all components in a system may scale equally. Many semiconductor customers want a more optimized technical option, which will deliver a more cost-effective business solution. In the advanced semiconductor world the result is both disaggregation (offloading functions that do not require or benefit from the most advanced logic) as well as heterogeneous integration (using high-speed die-to-die interconnects). There are many options available but the most popular option at the moment is **chiplets**.

Chiplets

The term chiplet is a colloquial term which refers to a new type of semiconductor design in which a complete chip system is constructed from a "menu" of modular chips, aka chiplets. Chiplet technology is not necessarily new as it can be traced back to the 1980s, when the industry first developed multi-chip modules (MCMs). At that time however, MCMs – as well as several other advanced packaging techniques – were consigned to extremely high-end systems like mainframe computers. For other systems, the semiconductor industry still relied on commodity packaging for ICs.

Exhibit 7: Monolithic vs Modular (Chiplet) design

Source: Intel

In theory, the chiplet design approach is a faster and cheaper way to assemble various types of third party chips (I/O's, memory, and processor cores, etc.) into a single package. The closest comparison would be a System-on-Chip (SoC) in which a main microprocessor (CPU) plus complementary IP blocks are built on the same die. However,

in order to scale the performance of an SoC, the entire design (CPU + IP building blocks) must be ported to the next manufacturing node (i.e. from 14nm →10nm → 7nm, etc.)

On the contrary, the LEGO-like nature of chiplet design means that the most expensive/leading edge manufacturing technology can be reserved for the chiplets within the design where the incremental investment will most likely pay off. Peripheral chiplets can be made using more established techniques, where manufacturing yields are higher, and costs are consequentially lower. This should enable semiconductor companies to design & ship more powerful processors at a faster cadence when compared to the more traditional SoC-design model where every IP block must be redesigned/redeployed into a fully integrated die at the latest leading edge node.

There have been several early examples of chiplet based semiconductor designs emerging from some of the more prominent semiconductor companies, most notably with AMD and their EPYC line of server processors.

Chiplet technology sounds great on paper, but there are some puts and takes. For example, chiplets do have some costs associated with them both in packaging costs as well as increase in die area cost. You cannot just take a 2X area monolithic component and divide it into two smaller die that are 1X area each. There is an overhead when communicating between the two, as well as additional power logic, additional coherency logic, additional clocking controls, as well as a efficient test controls.

US share of global semi manufacturing is dwindling

While the US remains the global leader in semiconductor production and design, from a manufacturing standpoint, the US is losing ground due to rising manufacturing and technology costs and mounting overseas competition. US share of global manufacturing capacity has declined from 37% in 1990 to just 12% today. Indeed, only 44% of US firms manufacturing capacity is located in the US, with almost 50% located in Asia (Singapore, Taiwan, Japan, China). This is because significant semiconductor manufacturing incentives have been put in place by other counties, while the US has lacked federal incentives. For example, China's share of global 300 mm chip products is also 12% today, although contrary to the US, has grown at a 16% pace over the last 7 years. Per SIA, China share of global chip products could grow to be largest (28%) by 2030.

The dwindling position of the US in global semiconductor manufacturing has become a key area of focus for republicans and democrats alike. Indeed, in June 2020, a new bipartisan legislation was introduced in the Senate called the CHIPS for America Act. This legislation would invest an estimated $25bn over 5-years in incentives (equipment purchase credits, R&D tax credits) with the goal of enhancing US leadership in semiconductor production and to counter China's rise.

Some large manufacturers have already started making moves to add more capacity in the US. This summer, TSMC announced their intention to build a 5nm fab in Arizona which is set to come online in 2024. With the final price tag expected to be $12bn, this would make this one of the most expensive fabs ever built in the US. More recently, Intel CEO Bob Swan penned an open letter to US President elect Joe Biden about the importance of US manufacturing and the need for more government incentives to level the playing field.

Still, translating funding intentions into practical legislation and then to cutting-edge US manufacturing will take a matter of years given the complexity (only 3 leading-edge chipmakers left), expense ($10-$15bn for a new fab) and time (2+ years).

Semicap: oligopolistic and nationalistic

As we mentioned earlier, there are three main phases of the chip production process: (1) wafer manufacturing; (2) chip fabrication or the "front-end process"; and (3) assembly & packaging or the "back-end process". In this section, we focus on the front-end part of the manufacturing process.

Front-end manufacturing typically takes place in a large, state-of-the-art "cleanroom" within a fab, since the process is so precise that even small particles of dust can ruin the circuitry on a chip. The air in standard fab cleanroom must qualify as class 10 purity, which means that there can't be more than 10 particles larger than half a micron (about the size of a bacteria) per cubic foot. To put that in perspective, there are approx. 3mn particles per cubic foot in the air we breathe every day.

Modern fabs are outfitted with advanced automated systems that allow companies to operate 24 hours a day, 7 days a week, and 365 days a year. Batches of 25 wafers are transported throughout a fab from station to station in pods, called front-opening unified pods (FOUPs) via an overhead monorail system. Each "station" is outfitted with different types of machines, commonly referred to as "tools", responsible for different process steps. Each machine can cost up to tens to hundreds of millions of dollars.

The companies that make these tools are known as semiconductor capital equipment vendors, or semicap equipment for short. These companies provide **wafer fab equipment** (or WFE) to IDMs, foundries, and memory customers, which is critical for the manufacturing process. The collective amount of capex that is spent on this equipment is often referred to as WFE, and this portion typically makes up 55% of capex, while the rest ('other' capex) refers to non-equipment like the actual building.

The overall semiconductor industry is expected to account for a roughly $430bn addressable market in 2020 (according to Gartner) and the actual manufacturing of chips is extremely capital intensive. The total capex required to support global semi sales is expected to be over $100bn in 2020 (per Gartner), or about 20%-25% of expect sales. Further, the portion of overall capex attributed to WFE is expected to be $58bn (per Gartner), or 58% of total capex, slightly above the long term average of 55%.

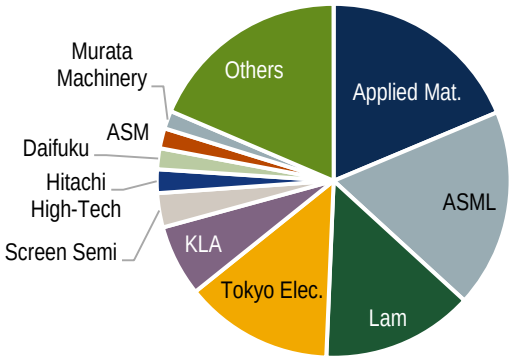
The increasing complexity (and cost) associated with migrating to future manufacturing process technologies has made semicap equipment extremely critical, not just to the continued scaling of semiconductor nodes, but also to the advancement of key technologies like artificial intelligence, 5G networks, cloud computing and autonomous driving. However, given industry consolidation and high barriers to entry, the semicap equipment industry is an oligopoly with 5 companies controlling roughly 70% of the market.

US, Europe, Japan lead in semicap equipment market

The top 5 semicap equipment vendors make up nearly 70% of the market. 3 out of these 5 are US companies (Applied Materials, Lam Research, KLA Corp), while 1 is European (ASML) and 1 is Japanese (Tokyo Electron).

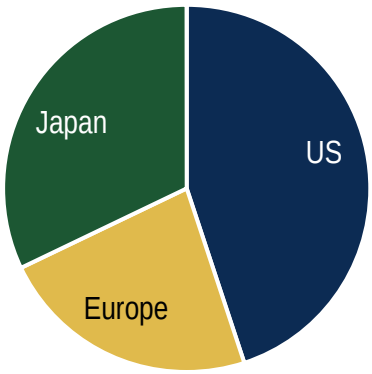
Indeed, the US, Japan and Europe dominate the semicap equipment market. Of the top 15 WFE vendors (87% of total WFE), all of them are from these three regions, with 45% of the revenue share from the US, 32% of Japan, and 23% from Europe. In other words, these three countries basically control the manufacturing of semiconductor chips, and supply all other regions with their semicap equipment.

Chart 17: The top 5 semicap vendors make up nearly 70% of the market



Source: Gartner

Chart 18: % of top 15 WFE from different regions



Source: Gartner

Importantly, there are no Chinese semicap equipment vendors within the top 15. While Chinese semicap equipment vendors do exist (were cumulatively ~2% of WFE in 2019), they tend to provide front-end equipment for legacy nodes, with little to no position in advanced, or leading edge equipment. This means that if a Chinese company wants to manufacture leading edge semiconductors, it is virtually impossible for them to do that without equipment from US companies, or US allies. Additionally, as process nodes continue to shrink (to 5nm and below), Extreme Ultraviolet (EUV) lithography becomes increasingly critical, a technology in which ASML has a monopoly.

Below we outline the areas where China semicap suppliers are gaining ground. Chinese semicap vendors have gained ~2% share in deposition, etch, material removal/clean, and RTP, per Gartner. However this is still well below the 40-60% share of US semicap firms.

Table 4: China semicaps gaining ground in deposition, etch, material clean, and RTP but still well below 40-60% share of US semicap firms

		Incumbent Equpment Supplier						Emerging China Suppliers		
Semicap Category	2019 Size ($bn)	ASML	Applied Materials	Lam Research	KLA Tencor	Tokyo Electron	Screen	AMEC	NAURA	ACM
Deposition	$12.0		44%	19%		10%		1.1%	0.9%	0.1%
Lithography	$11.7	83%	0%							
Etch	$10.8		18%	45%		28%		1.1%	0.8%	
Process Control	$6.2	5%	11%		54%					
Material Removal/Clean	$3.7		18%	34%		24%	10%	0.7%	0.8%	0.6%
Fab Automation	$2.9		5%							
Photoresist Processing (Track)	$2.1					91%	6%			
CMP	$0.0		66%							
RTP	$1.4		40%			20%	4%		1.7%	
Ion Implant	$1.2		60%							
Wafer Level Packing	$2.1					14%				
Total Market	$54.1	18%	19%	14%		14%	3%	0.5%	0.5%	0.2%

Source: Gartner

EUV critical for advancing leading edge manufacturing

Extreme ultraviolet (EUV) is a next-generation lithography technology that should enable the industry to continue transistor shrinks to 2nm through 2025 and potentially beyond. EUV uses extreme ultraviolet light wavelength of 13.5nm, a wavelength that is less than a tenth of what is used in today's most state-of-the-art machines, to imprint designs on to wafers. EUV technology is significantly different to current immersion lithography (193nm wavelength light source) techniques, which have become increasingly complicated over the last few years. In EUV, a power source produces plasma which in turn gives out EUV radiation. Then, the light bounces off a complex

scheme of multi-layer mirrors before hitting a mask and eventually the wafer on which designs need to be imprinted.

In theory, any design dimension can be obtained using older generation lithography (DUV) and multi-patterning techniques. Multiple patterning techniques have been extended as far as octuple patterning in R&D. However, extending multiple patterning to get to smaller dimensions increases the number of steps in the manufacturing process and makes it more complex. This in turn generally reduces yields and increases manufacturing costs. This trade off will however also be a function of the throughput of the EUV tool.

Using traditional multi-patterning techniques, chipmakers are struggling to shrink the sizes of devices, while keeping costs low. Use of EUV simplifies and reduces critical lithography costs by 15-50% compared to multi-patterning schemes, thus making the economic arguments for EUV adoption compelling. ASML, the only supplier of EUV lithography machines, anticipates a 3-6x reduction in cycle time compared to using multi-patterning for critical layers.

High NA developments

As the industry looks to 3nm and beyond, the most critical layers are expected to require multiple patterning with current EUV tools (with a numerical aperture of 0.33). To avoid multiple patterning (and keep manufacturing yields high/costs low), ASML is focusing on developing tools with a higher numerical aperture (0.55). Resolution of designs printed with EUV tools is inversely proportional to the numerical aperture. A larger numerical aperture results in higher resolution, a reduced number of litho/etch steps and hence lower cost.

ASML, in collaboration with Carl Zeiss, has developed these next generation EUV tools with commitment from 3 customers for a total of 12 orders. Initial development systems are expected to ship in 2022.

Exhibit 8: EUV roadmap to 2025

Source: ASML

Note, in the chart above, overlay refers to the placement of successive layers on a chip, and is expressed in nanometres (nm). In other words, it refers to the accuracy at which the lithography tool can align and print various layers on top of each other. These layers

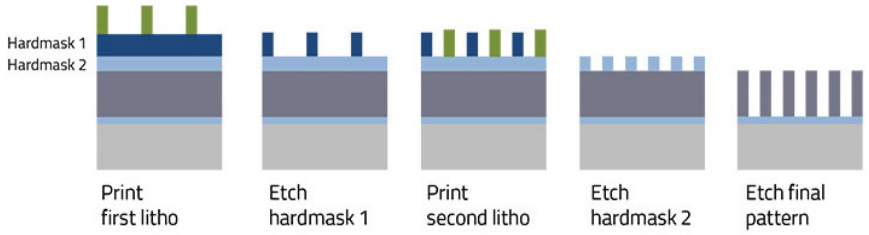
must be aligned correctly, or else the device may not perform as desired. Hence, the number should be as small as possible.

Considerations of DUV based multi-patterning vs. EUV

Multi-patterning involves patterning a single chip layer in two or more steps. Multi-patterning emerged as an application as DUV lithography had reached its resolution limits while EUV lithography technology was not ready. Chipmakers used two variations of multi-patterning techniques - litho-etch-litho-etch (LELE) and self-aligned patterning.

LELE is a form of double patterning. It splits a pattern into two separate lithography and etch steps. The first pattern is transferred onto a hardmask through exposure of photoresist to the UV light via lithography, followed by etching the hardmask. This process is repeated for the second pattern (see exhibit below). The end result is a pattern that is twice as dense as the original. This can be further extended, as explained earlier to Octuple patterning.

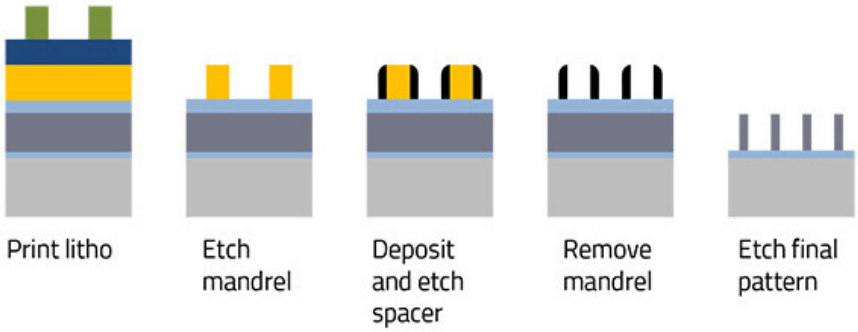
Exhibit 9: Litho-etch-litho-etch illustration



Source: Lam Research

In self-aligned patterning (SAP), spacers are formed on the sidewalls of a pre-defined feature, called a mandrel via deposition and etch steps. The mandrel is then removed by a further etch step, leaving only the spacers which then define the desired final structures. The final shapes are not defined by the mask shapes but are more residuals from the deposition and etch steps. There are two/four spacers for each mandrel, so feature density is doubled/quadrupled. (see exhibit below)

Exhibit 10: Self-aligned patterning illustration



Source: Lam Research

These techniques allowed the industry to continue scaling while EUV (extreme ultra violet) was in development. While traditional lithography patterning using DUV was able to produce a pattern with 80nm spacing (pitch), multi-patterning was capable of producing patterns with 20nm spacing i.e. four times as dense.

Which exact method (SAP or LELE or a combination of the two) was used in fabrication would have depended on the type of device being produced, manufacturers' levels of expertise/familiarity with various steps in the production process and economic considerations (higher yield with lowest cost/number of manufacturing steps).

EUV simplifies the manufacturing process flow

Although the above multi-patterning processes provided a solution for the industry as it awaited EUV, they are far from ideal. Multi-patterning is more complex, costly and ultimately more error prone than the comparative process using EUV.

Table 5: Number of process steps in 7nm multi-patterning vs. 7nm EUV

	7nm using multi-patterning	7nm using EUV
No. of lithography steps	34	9
Critical alignment overlay steps	59-65	12

Source: ASML

Table 6: EUV reduces wafer cost/increases yield in 7nm logic

Wafer cost reduction	-12%
Expected yield increase	9%
Expected reduction in time to market	-6 months

Source: ASML

The yield improvements/cost reductions are however a function of the device structure being produced and the throughput of the EUV tool.

How does EUV differ across logic, DRAM and NAND?

Logic/foundry: The first adopters of EUV

The performance of a logic chip is largely driven by the number of transistors (gates that turn charge flow on or off). Over the years, transistors have been made smaller which has allowed manufactures to fit more transistors into the same or smaller area.

Logic chips are built at more advanced, i.e. smaller node sizes compared to memory devices. This means that logic devices tend to move quicker to leading edge manufacturing processes when compared to memory devices.

Table 7: International technology roadmap for semiconductors

	2015	2017	2019	2021	2024
DRAM metal min lithography defined half pitch (nm)	24	22	18	15	12
Logic metal min lithography defined half pitch (nm)	26	18	12	10	6

Source: ITRS. Note metal pitch is illustrative of the node size. The smaller the metal pitch, the more advanced the device

Both TSMC and Samsung entered high volume manufacturing with their 5nm chips this year, while Intel is focusing on intra-node enhancements on its 10nm process. ASML has stated that EUV will be used for >10 layers at 5nm logic while 3nm will utilise >20 layers.

DRAM: the next driver of EUV demand

As shown in the table above, DRAM tends to lag logic by 2-3 years when it comes to adoption of the most leading edge nodes. Hence, in any given year, yield issues associated with shrinks tend to be less severe than those in logic devices. Further, memory devices usually tend to be more cost sensitive than logic devices. The low levels of initial EUV tool throughput meant that even if EUV was able to reduce process steps etc involved in producing a DRAM device, it did not ultimately reduce cost (due to lower tool throughput) and hence DRAM vendors have been slower to adopt EUV.

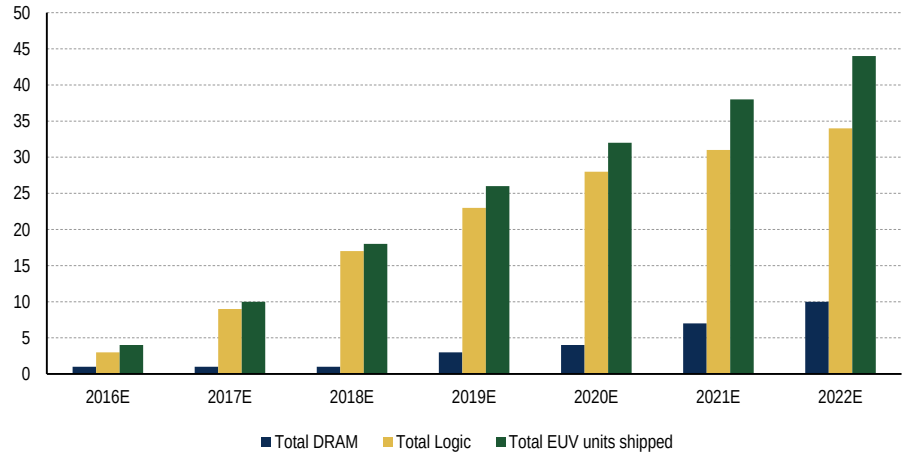
As ASML has improved the throughput of its EUV tools over time, EUV adoption in DRAM is now beginning. We understand that EUV tool productivity is now at levels that make adoption economical for most DRAM vendors. We further understand that EUV adoption can also improve the electrical performance distribution of chips across the wafer, ultimately delivering a higher quality batch of DRAM chips which DRAM vendors may be able to monetise.

DRAM will start by using 1 EUV layer at the 1 alpha node in 2021, with 5-6 layers expected at future nodes in 2022/23 (source: ASML 3Q20 and 2Q20 transcripts). Samsung is first manufacturer to introduce EUV in DRAM (1a node), trialling it this year with full ramp expected next year. SK Hynix is also expected to use EUV in DRAM in 2021.

Comparison of EUV shipments in logic and DRAM

Logic has thus far accounted for the largest portion of EUV tool shipments, and will continue to do so.

Chart 19: Total EUV shipments to logic and DRAM



Source: BofA Global Research estimates

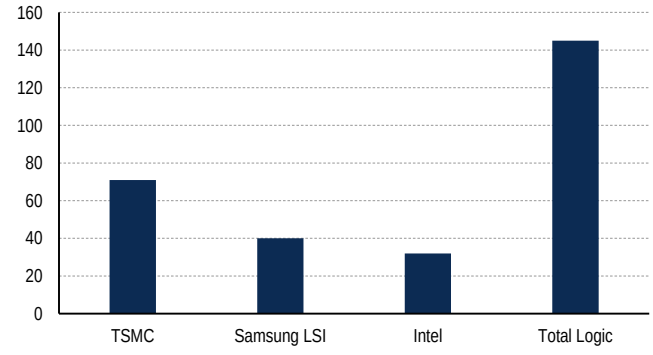
3D NAND: EUV is not required given node sizes

3D NAND chips scale differently to DRAM and logic. Instead of scaling by increasing density, they scale by vertically. As such they are built at less demanding node sizes (>30nm). Hence, DUV lithography tools are sufficient for the patterning steps used.

EUV usage by manufacturer

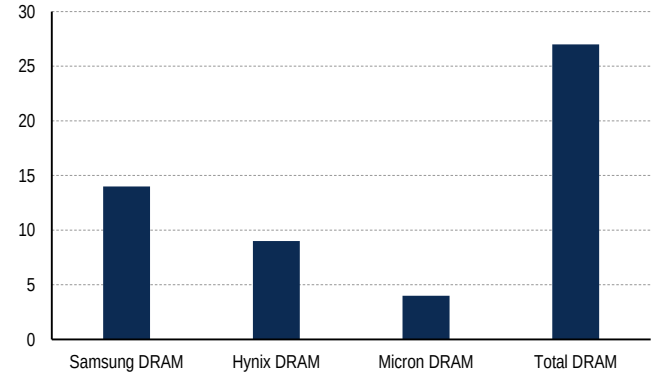
Each chip manufacturer takes a different approach in their process and chip recipes tend to be closely guarded secrets. Hence, it can be difficult to gain clarity into the exact processes/steps used by different vendors. However, we can draw some conclusions based on EUV tool deliveries.

Chart 20: Cumulative EUV shipments to key logic players 2016-22e



Source: BofA Global Research estimates

Chart 21: Cumulative EUV shipments to key DRAM players 2016-22e



Source: BofA Global Research estimates

TSMC is the largest purchaser of EUV tools today. In fact, this year TSMC claimed this year that c50% of all globally installed EUV systems are in TSMC's foundries (source: TSMC). We do not see this trend reversing given Intel's manufacturing delays and TSMC's current leading position in the foundry position.

Samsung LSI is the number two player in foundry. We expect Samsung to account for more EUV shipments than Intel over the 2016-22 period. Samsung aims to produce 3nm chips in 2022, the same year as TSMC. Further, Samsung intends to use the new gate all around transistor architecture at 3nm whereas TSMC will remain using finFET until 2nm.

In short, gate all around should in theory be able to more precisely control current flow, allow denser chip structures and reduce power consumption. However, it has never been mass produced and given the complexities involved, production yields may be an issue initially. Per Bloomberg, trying to catch up to TSMC is a key focus for Samsung.

Intel is not using EUV in its current 10nm process but is expected to use EUV in its 7nm process. This process has however been plagued by delays. Intel's 7nm process is expected to ramp in 2H22/early 2023. Over 2016-23e, we expect Intel to be the third largest user of EUV tools after TSMC and Samsung.

Potential implications of Intel's delays at leading edge nodes

While Intel has not dropped out of leading edge manufacturing, it has announced that it will consider outsourcing production of its most important chips (per Bloomberg). Given this possibility, arguably there is the possibility for Intel to relinquish leading edge manufacturing capabilities.

In such a scenario, while total demand for EUV tools should not decrease in the medium term given ultimate level of leading edge chip demand is likely to remain unchanged. However, less players at the leading edge will mean less competition. This could potentially cause leading edge vendors such as TSMC to slow down its chip scaling roadmap, ultimately reducing innovation in the entire technology industry – note TSMC manufactures the most advanced chips for many fabless semi companies that operate in as diverse verticals as AI, 5G, autonomous vehicles etc.

However, Samsung appears to be keeping competitive pressure on TSMC and in the future, if Chinese manufacturers such as SMIC are allowed access to EUV tools, the abovementioned concerns may not materialise.

China's heavy reliance on US equipment caps progress

Roughly 80% or more of the critical SPE/tools sourced for SMIC comes from US vendors like Applied Material, KLA Corp, and Lam Research – a potential issue as SMIC faces mounting difficulties in procuring this equipment under the foreign direct product (FDP) rule imposed by the US government.

In the meantime, local Chinese semicaps, like AMEC and Naura, are emerging but forming a local industry for advanced semicap equipment remains years away. As such, SMIC's ambition to further make node advancement is at risk, though it targets to have N+2 process ready (7nm equivalent) with meaningful revenue contribution in next 2-3 years. Even if the company is able to reach the target, there's still at least 4-5 years lag vs TSMC and Samsung who entered mass production of 7nm in 2018-19.

Also, as we mentioned above, if SMIC is not able to source EUV tools from ASML (due to US-originated content inside) it may have to fabricate with double/multi patterning with deep ultra-violet (DUV) tools. However, it may not be an efficient or plausible option for foundry/fabless likely resulting in lower yield and longer cycle time, which may also prevent the firm from gaining design-in/wins.

Table 8: Overview of critical semi/foundry equipment mapping (text in red for US vendors)

Process	Chinese companies	Most advanced node for Chinese companies	Overseas competitors (*Red for US companies)
Lithography	Kingsemi, SMEE	65nm	ASML, Nikon, Canon, TEL, DNS
Etching	AMEC, Naura	5nm	LAM (LRCX), TEL, AMAT
Thin-film (CVD/PVD)	Naura, Piotech	7nm	LAM (LRCX), TEL, AMAT
Ion Implantation	Zhongkexin, Naura, KingstoneSemi	28nm	AMAT, Axcelis
Wet process (Cleaning + Chemical Mechanical Polishing)	ACM Research, Hwatsing, 45 Institution, Naura, PNC, Kingsemi	14nm	DNS, TEL, KLA (KLAT), LAM (LRCX), AMAT, Ebara

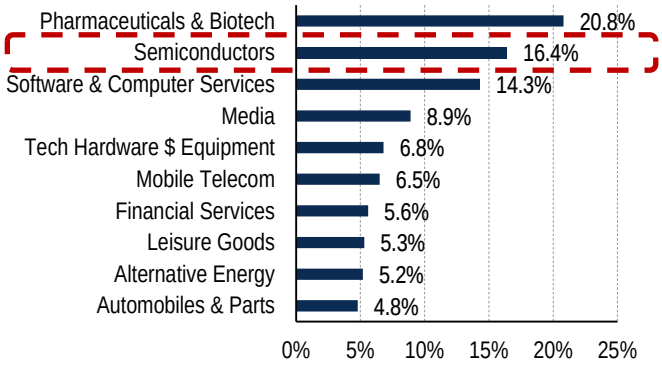
Source: BofA Global Research, company data

Design cost and dominance of IP

While the physical manufacturing of the chips is extremely important, to remain competitive in the semiconductor industry, firms must also continually invest a significant amount in designing chips. One could even argue, as Moore's Law continues to slow and process technology differentiation is harder to rely on, chipmakers will focus more on design architecture to gain power, cost, and performance benefits. This increased complexity and design cost has resulted in extremely high R&D intensity for the semiconductor industry. Indeed, in the US, semi industry R&D intensity is among the highest in major sectors, 2nd only to US pharmaceuticals & biotechnology.

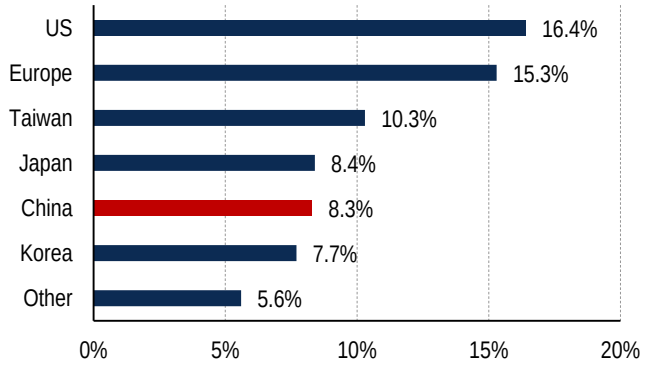
By region, the US is the largest semiconductor R&D investor at 16.4% of sales. By comparison China invests just 8.3% of its semi sales in to R&D. We do note that China R&D intensity estimate may be low due to government subsidies which we estimate to be roughly $4bn annually since 2014, or roughly 2x industry R&D (estimate based on $20bn IC Fund over 5 years), reliance on off the shelf IP, and China's focus on lower end consumer products with limited software.

Chart 22: US Semi R&D % of sales is 16.4%, 2nd to Pharma & Biotech



Source: 2019 EU Industrial R&D Investment Scorecard, SIA

Chart 23: US R&D intensity nearly 2x larger than China



Source: 2019 EU Industrial R&D Investment Scorecard

Still, to put this in context, at an R&D intensity of 8.3% China semiconductor companies spent roughly $2bn in R&D investment in 2019. This compares to the $13bn that Intel alone spent on R&D last year. High design costs and R&D requirements have resulted in extremely high barriers to entry for the semiconductor industry.

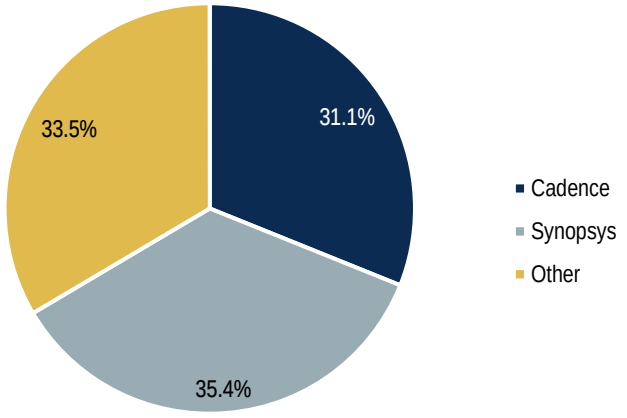
The design of modern day integrated circuits (some of which contain billions of transistors) would not be possible without the assistance of computer aided design software at every step in the design process. The tools and methods used to complete these steps are jointly called **electronic design automation (EDA)**. The EDA market is largely dominated by three US firms: Synopsys, Cadence, and Mentor Graphics (acquired by German headquartered Siemens in 2016).

China currently does not have any EDA vendors that have a full end-to-end design and verification solutions. As the US continues to restricts the supply of technology made with, or containing, US technology to China, it is clear that the US monopoly on leading-edge IC design software can be used to exert control on Chinese access to competitive semiconductor technology. This has now made domestic leading-edge competence in EDA a high priority for China. Previously established Chinese EDA companies, including Empyrean Software (2009) and Primarius Technologies (2010), were unable to catch up technically with US competitors and have made little impact on the market. However, more recently media reports (Nikkei) have identified three EDA startups that are part of China's attempt to reach self-sufficiency in the semiconductor market. The three companies are X-Epic (founded in March 2020), Hejian Industrial Software (founded in May 2020), and Amedac (founded in September 2020). Still any domestic grown EDA

industry will take a long time to effectively compete with the breadth and capabilities offered by US competitors, and over that time US vendors will continue to innovate.

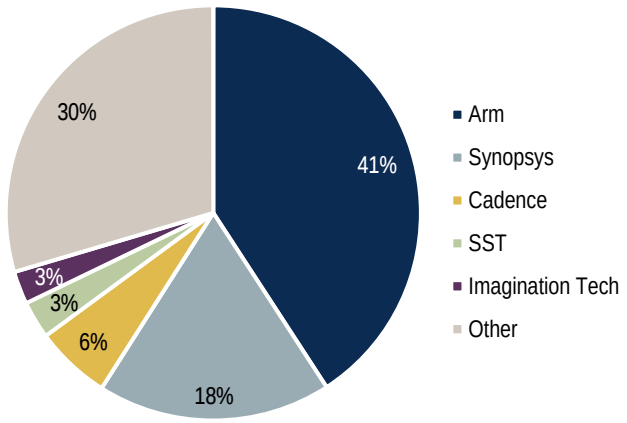
In lieu of developing unique internal designs, companies can also buy **semiconductor intellectual property (IP)** or pre-designed blocks of circuits for commonly used functions that can be used in the designs of complete semiconductor devices. The largest of these semiconductor IP vendors is by far British semiconductor and software design company, Arm (currently owned by Japanese conglomerate Softbank but in the process of being acquired by US fabless semiconductor vendor, Nvidia) with roughly 40% of the market share. Synopsys is the second largest with 18% share followed by Cadence with 6% share.

Chart 24: Synopsys and Cadence represent 65% of the EDA market



Source: BofA Global Research estimates, ESD Alliance

Chart 25: Arm, Synopsys and Cadence control 65% of the semi IP market



Source: BofA Global Research, IP Nest

Arm IP is likely most popular due to Arm's processor architecture that is widely used in smartphones but is also found in personal computers, servers, and other devices. Arm owns the designs, along with the architecture of their instruction sets (suh as 64-bit ARM64). Its business model is to license the intellectual property (IP) for these components and the instruction set to other companies, enabling them to build systems around them that incorporate their own designs as well as Arm's. For its customers who build systems around these chips, Arm has done the hard part for them. Many Samsung and Apple devices, and essentially all devices produced by Qualcomm, utilize some Arm IP. Arm has so far had limited success in PCs and the data center market compared to its main processor architecture competitor, known as x86 (used by Intel and AMD).

Arm vs. x86

There are two overarching categories of processor microarchitectures: **Complex Instruction Set Computing (CISC)** and **Reduced Instruction Set Computing (RISC)**. CISC includes x86 CPUs, which are supplied by Intel and AMD, while RISC includes ARM and Imagination Technology's MIPS, which are used by a number of different vendors (such as Marvell, via its recent acquisition of Cavium). RISC (Arm) utilizes smaller and simpler instructions making it highly efficient, but results in longer code. CISC (x86), on the other hand, utilizes larger and more complex instructions, which results in shorter code. Generally RISC is more efficient and consumes less power, while CISC has better performance – this is why RISC is more common in processors for mobile devices, but CISC continues to be the de facto architecture for most CPUs as we know them today (used mainly in PCs and servers).

The maker of an Intel or AMD based x86 computer does not design or own any portion of the IP for the CPU. It also cannot reproduce x86 IP for its own purposes. Instead the

device manufacturer is just given a license to build a machine around Intel's processor. An Arm-based device may be designed to incorporate the processor, perhaps even making adaptations to its architecture and functionality. For that reason, Arm processors are called system-on-a-chip (SoC) instead of a CPU. Much of the functionality of the device may be fabricated onto the chip itself rather than built around the chip in separate processors, accelerators, or expansions. Arm chip is also not necessarily a central processor. Depending on the design of the system, it can be the heart of a device controller, a microcontroller (MCU), or some other subordinate component in a system.

As we mentioned above, Arm processors have historically been less successful in the data center and PCs. However, Arm appears to be gaining some ground in these markets. Just last month, a Fujitsu Arm-powered supercomputer named Fugaku seized the #1 spot on the semi-annual Top 500 supercomputer list. Apple also just announced its new line of Macs powered by Apple's own M1 Arm-based chip (a shift from prior generations which all used Intel x86 processors).

Arm critical for China domestic semiconductor industry

In April 2018, Arm entered into a joint venture with a consortium of Chinese companies which included the state-backed China IC Fund with a majority stake collectively held in China, while Arm holds 49% in the joint venture.

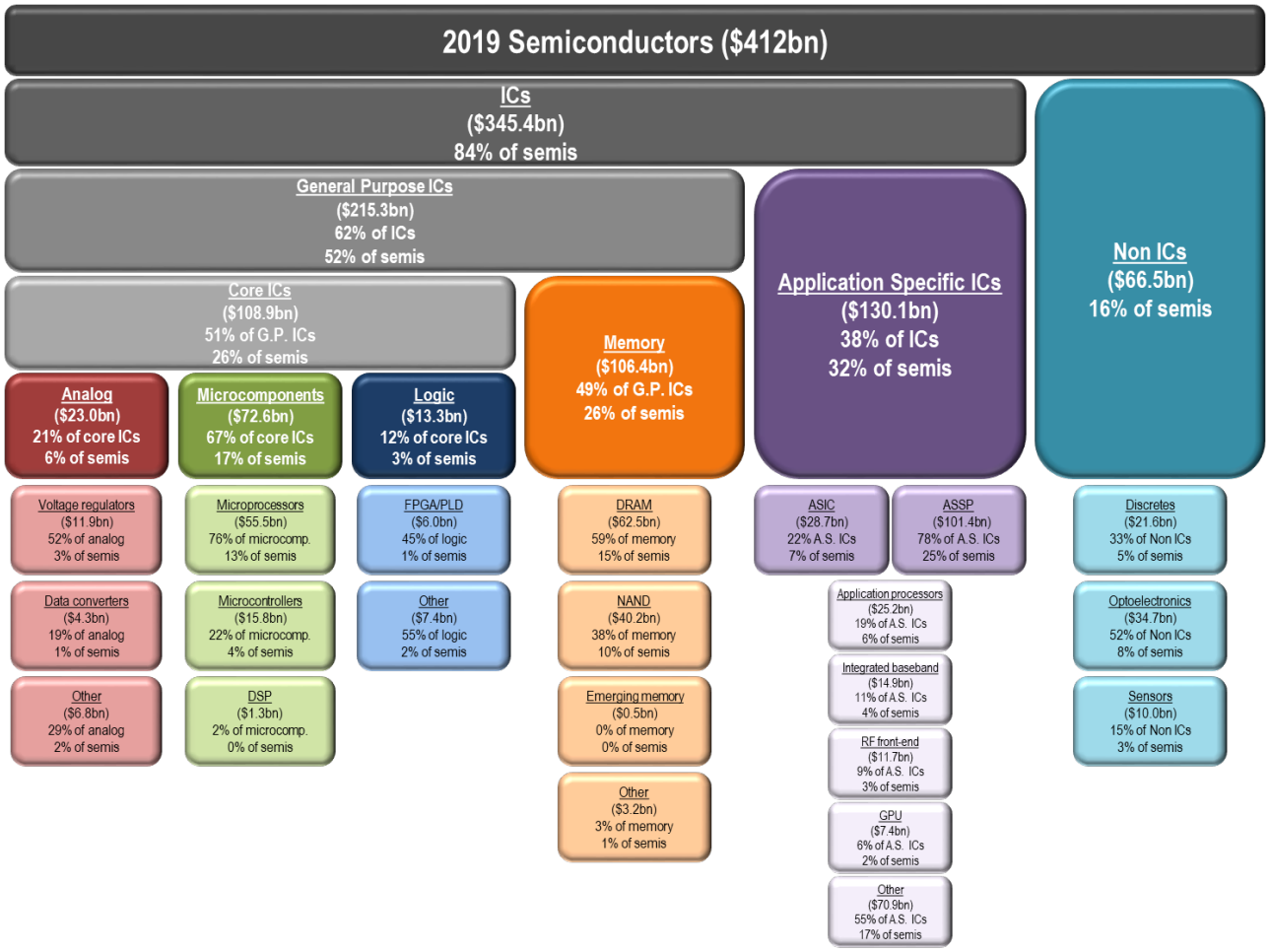
Arm architecture is critical to China's emerging chip design industry. Prior to US sanctions, China's largest fabless vendor, HiSilicon, used Arm designs to build its Kirin chips. China's other large fabless semiconductor companies, like UniSoC and Goodix, still heavily rely on Arm architecture. Indirectly, smartphone brands such as Oppo and Xiaomi rely on Arm as purchasers of chips based on designs made by Qualcomm and MediaTek. Additionally, AI, especially AI semiconductors, are a key part of China's self-development strategy, and China has some strong companies in the inference space like Horizon Robotics, Intellifusion, Iluvatar, Sensetime, Artosyn, all of which use Arm architecture.

As we mentioned earlier, US based semiconductor firm, Nvidia, has announced its intention to acquire Arm for $40bn. However, before the deal can go through it will need approval from China's Ministry of Commerce (MOFCOM) and China's State Administration for Market Regulation (SAMR) which may be tricky given US/China trade relations and the critical nature of this IP to China's domestic semi industry. Indeed, this would not be the first time Chinese regulators have prevented a US chip firm from buying a European company (in 2018 SAMR blocked Qualcomm's attempt to buy Dutch chipmaker NXP). While Nvidia CEO Jensen Huang promised the structure of Arm's China Joint Venture will not change, this deal may face significant regulatory scrutiny.

Types of Semis

In this section, we give a brief overview of each major semiconductor product category. We typically divide the semiconductor market into three overarching buckets: (1) core semis (or ICs ex-memory); (2) memory; and (3) discretes, optoelectronics, and sensors. The key categories within the core semis bucket are CPUs ($56bn TAM), Analog ($23bn), MCUs ($16bn), FPGAs ($6bn), Other General Purpose Logic ICs ($7bn), ASICs ($29bn), and ASSPs ($101bn). Memory is mostly comprised of DRAM ($63bn TAM) and NAND ($40bn). Lastly, discrete represents a $22bn TAM, Opto. ($35bn), and sensors ($10bn).

Exhibit 11: Summary of key semiconductor product categories and market sizes



Source: BofA Global Research, SIA/WSTS, Gartner

Interestingly, many semiconductor categories end up forming into duopolistic markets through rapid consolidation and difficult barriers to entry. Duopolistic semi categories include microprocessors (MPUs or CPUs), GPUs, and FPGAs. Other semi categories are more fragmented including ASICs, Microcontrollers (MCUs), Analog, and memory.

Duopolistic semi categories

Microprocessors (MPUs or CPUs)

Microprocessors ("MPUs"), also known as central processors ("CPUs"), perform one of the most important roles in any computing device – processing data and controlling the other chips in the device. This is the reason that CPUs are commonly referred to as the "brain" of an electronic device.

A CPU typically has at least one logic core, cache memory, I/O interconnects, and peripheral components such as audio and memory controllers. CPU manufacturers scale

system performance and efficiency by designing multiple cores into a single processor. Most CPUs are manufactured using leading-edge process technology.

The MPU market is largely dominated by Intel with roughly 90% share (per Gartner) while AMD has 5-10% share.

Discrete graphics processing units (GPUs)

A **discrete graphics processing unit**, or "GPU", is a general-purpose processor that was originally designed to render complex images for PC video games and films. Unlike a CPU, GPUs consist of hundreds to thousands of processing cores and each core is dedicated to perform a specific operation in parallel. In recent years engineers discovered that parallel computation could be used to handle big data applications more efficiently than just a CPU. So the GPU architecture has been extended into adjacent markets such as artificial intelligence (AI), self-driving cars, workstations, cloud data centers, and high performance computing applications. A GPU or multiple GPUs typically interface with one or more CPUs. The CPUs are responsible for general tasks like programming and data management or movement, and the GPU is used to handle the bulk of the complex parallel computations.

The GPU market is largely dominated by Nvidia with roughly 80% share (per Gartner), while AMD has most of the remaining 20% share.

Field Programmable gate arrays (FPGAs)

Field programmable gate arrays, or "FPGAs", are integrated circuits that are designed to be configured for different algorithms after manufacturing – hence the term "field programmable". FPGAs are based around a matrix of configurable logic blocks (CLBs) connected to input/output blocks (IOBs) and each other via programmable interconnects. Modern FPGA devices consist of millions of logic cells that can be configured to implement a variety of software algorithms. What makes FPGAs unique is the physical gates and wires are configured by the customer after manufacturing, using either a hardware description language (HDL) or a high-level synthesis (HLS) tool. This enables an infinite number of computational tasks to be handles by the same device.

The FPGA market is largely a duopoly although is more evenly split than the MPU and GPU markets. Xilinx is the market leader with roughly 54% share (per Gartner), followed by Intel (through the acquisition of Altera) with 32%, Microchip (through the acquisition of Microsemi) with 6%, and finally Lattice Semiconductor with 5% share.

Non-duopolistic semi categories

Application specific logic chips (ASICs & ASSPs)

Semiconductor devices characterized as application-specific are specially designed integrated circuits that are categorized into one of two product families: **ASICs (application specific integrated circuits)** or **ASSPs (application specific standard products)**. In general, the more customer specific the ASIC/ASSP approach is, the longer it takes to design, and the more expensive it is to produce. ASICs are ICs designed and manufactured for the exclusive use of a single customer.

The ASIC may be a digital, analog, or mixed signal chip, and typically combines functional blocks such as processor cores, memory, interface circuits, analog, and custom logic. Some more popular examples of ASICs include Google's artificial intelligence processor (Tensor Processing unit, or TPU), and Apple's A-series processors used in iPhones and iPads. These are both examples of OEM foundry-direct ASICs in which a traditional system company (e.g. Apple) goes directly to a foundry (e.g. TSMC) for device manufacturing, thereby bypassing traditional/merchant ASIC suppliers. Amazon, Huawei, Xiaomi, and Cisco are other OEMs who have employed the OEM foundry direct ASIC design model.

ASSPs, on the other hand, are ICs designed for use in one specific category of electronic equipment, but not necessarily for a single customer. Indeed, ASSPs are typically

designed and manufactured to a specified data sheet that can be marketed to a set of customers who share similar end-market and use case parameters. Like an ASIC, an ASSP may be a digital, analog, or mixed signal chip which combines multiple functional blocks such as processor cores, memory, interface circuits, etc.

The application specific semiconductor market is extremely fragment with the largest participants Broadcom, Qualcomm, and Intel all with 8-11% share. The top 20 companies cover 80% of the market.

Microcontrollers (MCUs)

A **microcontroller** unit (MCU) is a standalone integrated circuit (IC) that performs embedded computing function without the support of other ICs. MCUs are best suited to applications which require minimal power drain and processing power. MCUs, unlike CPUs, are dedicated to one task and run one specific program loaded onto the chip. MCU's can interface with real-world (e.g. processing sensor measurements) but can also supervise system functions (e.g. power management, display connections, etc.). MCUs are used in millions of electronic devices such as smartphones, tablets, PCs, wireless headsets, automobiles (power doors/windows, powertrain, ABS, traction control, security), industrial automation, consumer products (remote controls, electronic toys, stereos, DVD players), digital clocks, and medical monitors.

The microcontroller market is also fairly fragmented, although the top 4 vendors (Renesas, NXP, Microchip, STMicro) account for roughly 60% of the market.

Analog

Analog chips are distinctly different from the vast majority of semiconductors, which tend to be digital. To draw an analogy, they 'speak' different 'languages'. Digital chips rely on binary code – an ON condition or "1" and an OFF condition or "0" – and this code is processed using mathematics. Analog chips, on the other hand, have to decipher any values that can be between an OFF condition and an ON condition. Examples include recording audio in a microphone, playback through a speaker, video recording, etc. In other words, analog chip inputs and outputs are defined by electrical properties (i.e. real world signals) – typically voltages, currents, or signal frequencies – and the chip's transistors measure or regulate them. Analog and digital chips need to co coexist, because they complement one another. Analog chips 'interact' with the real world by processing physical (analog) signals and converting them into digital code, which is then processed a digital chip – or, similarly, a digital chip processes a code, which then needs to be converted to an analog signal, which is then sent back out to the real world.

The analog market is highly fragment with two clear leader, Texas Instruments (29% share) and Analog Devices (20% share) followed by a long-tail of vendors with 1-4% share.

Memory (DRAM, NAND, others)

Dynamic random-access memory (DRAM) and **NAND flash** are the two most common types of memory sold today (account for >95% of total memory sales). DRAM, the larger of the two markets, accounts for 60-65% of memory sales, followed by NAND, which accounts for 35%+. The main difference between the two is that DRAM is volatile, meaning it loses data when the power source is turned off, while NAND is non-volatile, meaning that it can retain data even when the power is off. Both devices are used across most electronic devices (PCs, phones, servers, etc.).

Each new generation of memory chips drives densities higher but requires more advanced and expensive tools to keep the size unchanged (more integrated circuits on the same size of the chip). Yet, "shrinking geometries", can also drive a 20% +/- cost reduction per bit every year, which in the long-run results in greater memory capacity. Memory density is typically measured in the number of bits or bytes in a chip. Bits and bytes are basic units used to measure amounts of data. Recall a bit represents a value of either 1 or 0. Bytes are bigger than bits (1 byte contains 8 bits). Bytes are the preferred

metric for measuring data storage. Given the vast amount of data that can be stored, memory/storage for most electronic devices today are characterized in gigabits (Gb) or gigabytes (GB) – "giga" means 1 billion. So a device with 1Gb of capacity means it can store 1 billion bits. Similarly, a device with 1GB of capacity can store 1 billion bytes.

The DRAM market is highly consolidated with 3 vendors accounting for 95% of the market. The market leader is Samsung with 43% share (per Gartner) followed by SK Hynix (28% share) and Micron (24% share).

The NAND market is also somewhat consolidated, although less so than DRAM, with the top 6 vendors accounting for 99% of the market. The market leader is also Samsung with 37% share (per Gartner) followed by Kioxia (18% share), Western Digital (14% share), Micron (13% share), SK Hynix (10% share) and Intel (7% share although is in the process of selling its NAND memory business to SK Hynix).

Discretes

A discrete chip only consists of a single circuit. There are different types of discrete chips, including diodes, small signal and switching transistors, power transistors, rectifiers and thyristors. Although multiple devices may be present in a package, they are still considered discretes if they have no internal functional interconnection and are applied in the same manner as other discrete devices.

The discrete semi market is highly fragmented with the top 5 vendors Infineon (15% share), ON Semiconductor (10% share), STMicro (7% share), Nexperia (6%), and Rohm (5% share), accounting for just 43% of the total market

Optoelectronics

Optoelectronic devices include light sensing products such as Photo sensors and CCDs as well as light emitting devices such as LEDs and Lasers.

The optoelectronics market is highly fragment with Sony (23% share) and Samsung (10% share) as the market leaders with another 20-25 companies with 1-5% share.

Sensors/actuators

Sensors provide an electrical signal output in response to a physical parameter. Items sensed can be temperature, pressure, force, acceleration, humidity and chemical or biological phenomena. The sensor category excludes optical sensors such as photodetectors or image sensors as they are included in the optical semiconductor category. Semiconductor actuators are micro-machined semiconductor devices that provide mechanical action in response to electrical signals.

The sensors market is highly fragment with only one company (Robert Bosch) with greater than 10% share and the top 16 companies accounting for just 75% of the market.

Semis End Market Exposure

Exhibit 12: 2019 Semiconductor End Market Exposure

Company	Ticker	Semi Sales (CY2019)	Auto	Consumer	PC	Ent./Cloud Data Ctr	Industrial	Wired Network	Wireless Network	Mobile	Key Customers
AMD	AMD	$6,731	0%	14%	70%	13%	2%	0%	0%	0%	Sony, Microsoft
Ambarella	AMBA	$229	19%	17%	0%	0%	63%	1%	0%	0%	Hikvision, Dahua
AMS	AMS	$5984	37%	5%	0%	0%	31%	0%	0%	26%	Apple
Analog Dev.	ADI	$5,754	15%	4%	4%	0%	51%	9%	14%	3%	Apple
Broadcom	AVGO	$17,185	1%	4%	1%	33%	4%	30%	0%	27%	Apple, Cisco
Cirrus Logic	CRUS	$1,242	2%	9%	1%	0%	2%	0%	0%	85%	Apple, Samsung
Cree	CREE	$1,008	13%	3%	0%	0%	81%	0%	3%	0%	-
Dialog	DLG	$1,684	2%	10%	1%	0%	12%	0%	0%	75%	Apple
Diodes	DIOD	$1,249	10%	23%	10%	6%	28%	4%	0%	18%	-
HiSilicon	*	$7,964	0%	7%	0%	0%	7%	25%	27%	35%	Huawei
Infineon	IFX	$11,154	43%	7%	3%	11%	25%	1%	3%	7%	-
Inphi	IPHI	$366	0%	0%	0%	57%	4%	39%	0%	0%	Microsoft, Huawei, Cisco
Intel	INTC	$71,965	1%	0%	51%	32%	3%	6%	5%	2%	Dell, Lenovo, HP, Apple
Knowles	KN	$855	0%	16%	2%	0%	0%	0%	0%	82%	Apple, Samsung
Lumentum	LITE	$1,745	0%	0%	0%	10%	21%	38%	5%	27%	Apple, Huawei, Ciena
M/A-COM	MTSI	$468	0%	0%	0%	20%	41%	12%	27%	0%	-
Macronix	*	$1,056	7%	53%	3%	8%	6%	16%	3%	4%	Megachips
Marvell	MRVL	$2,699	3%	7%	8%	38%	2%	33%	14%	0%	WDC, Toshiba, Seagate, Samsung
Maxim	MXIM	$2,183	26%	9%	3%	7%	29%	10%	12%	3%	Samsung
MaxLinear	MXL	$317	1%	35%	6%	7%	1%	47%	2%	0%	Arris
MediaTek	*	$7,986	1%	24%	13%	0%	1%	3%	0%	58%	Samsung, Huawei
Microchip	MCHP	$5,278	20%	12%	4%	9%	35%	12%	6%	2%	-
Micron	MU	$19,926	7%	4%	20%	30%	9%	4%	0%	27%	Huawei, Kingston, Apple
Monolithic Pwr	MPWR	$628	14%	26%	18%	12%	16%	0%	12%	2%	-
Murata	*	$14,037	32%	7%	0%	0%	11%	6%	21%	23%	Samsung
Nanya	*	$1,666	10%	44%	7%	8%	4%	16%	0%	12%	Kingston, HP, Lenovo
Novatek	*	$2,089	0%	20%	58%	2%	2%	0%	0%	17%	-
Nvidia	NVDA	$10,918	6%	4%	62%	27%	0%	0%	0%	0%	Dell, Asustek, Lenovo, HP
NXP	NXPI	$8,877	47%	7%	6%	3%	18%	2%	3%	13%	Continental, Apple
ON Semi	ON	$5,518	32%	11%	7%	4%	26%	5%	3%	12%	Robert Bosch, Denso
Qorvo	QRVO	$3,132	1%	3%	0%	2%	9%	6%	6%	73%	Apple, Samsung, Huawei
Qualcomm	QCOM	$14,391	3%	4%	2%	0%	1%	1%	0%	89%	Samsung, Apple
Renesas	*	$6,589	51%	12%	8%	2%	13%	10%	1%	4%	-
ROHM	*	$3,371	38%	32%	7%	1%	13%	1%	0%	8%	-
Samsung	*	$64,940	1%	6%	23%	20%	1%	2%	0%	48%	Apple
Semtech	SMTC	$554	3%	27%	14%	12%	33%	10%	0%	9%	Samsung, Trend-tek, Frontek
Silicon Labs	SLAB	$837	11%	20%	0%	0%	17%	11%	6%	36%	Samsung
Silicon Motion	SIMO	$457	0%	0%	76%	16%	0%	0%	6%	2%	SK Hynix, Intel, Samsung
SK Hynix	*	$23,169	1%	5%	28%	20%	1%	1%	0%	44%	Apple, Huawei
Skyworks	SWKS	$3,301	2%	11%	0%	0%	19%	0%	0%	68%	Apple, Samsung
Sony	*	$8,654	1%	11%	0%	0%	10%	0%	0%	78%	Apple, Samsung
STMicro	STM	$9556	30%	4%	5%	3%	30%	3%	3%	22%	Apple, Samsung, Bosch
Synaptics	SYNA	$1,357	0%	0%	6%	0%	0%	0%	0%	94%	Samsung
Texas Instr.	TXN	$14,383	20%	12%	8%	4%	37%	7%	7%	5%	Apple
Tsinghua Uni	*	$1,694	0%	0%	0%	0%	0%	0%	0%	100%	-
Vishay	VSH	$1,502	29%	5%	3%	3%	46%	7%	3%	4%	-
Western Digital	WDC	$6,353	2%	2%	52%	17%	1%	0%	0%	26%	Dell, Apple
Xilinx	XLNX	$3,235	9%	2%	0%	4%	45%	20%	20%	0%	ZTE

Source: BofA Global Research, IHS, Gartner

Sales and end market exposure for Infineon, STMicroelectronics, AMS, and Dialog Semiconductor are on a pro-forma basis

Glossary

Chiplet: a colloquial term which refers to a new type of semiconductor design in which a complete chip system is constructed from a "menu" of modular chips

Die: each individual integrated circuit on a wafer

Electronic Design Automation (EDA): a category of software tools for designing electronic systems such as integrated circuits and printed circuit boards

Extreme Ultraviolet Lithography: next-generation lithography technology that will enable the semiconductor industry to continue transistor shrinks using extreme ultraviolet light wavelength of 13.5nm

Fab: factory where semiconductors are manufactured

Fabless: semiconductor companies that only design their chips and outsource manufacturing to foundries

Foundry: company that only manufactures pre-designed chips for customers

Integrated Circuit: a singular semiconductor chip that is designed with many other discrete semiconductor components (resistors, capacitors, inductors, diodes) that are integrated into its geometry

Integrated Device Manufacturer: semiconductor companies that both design and manufacture their chips

Made In China 2025: Chinese government initiative pushing for leadership in robotics, information technology, and clean energy. Among its various goals, MIC 2025 sought to produce 40% of its own semiconductors by 2020 and 70% by 2025.

Moore's Law: the observation that the number of transistors per square millimeter on semiconductors should double approximately every 2 years

Semiconductor: a material that has a conductivity between that of an insulator (glass) and that of a conductor (metal), either due to the addition of an impurity or because of temperature effects. Semiconductors are integral components for virtually every electronic device

Semiconductor Intellectual Property: pre-designed blocks of circuits for commonly used functions that can be used in the designs of complete semiconductor devices

Technology Node: a specific generation of semiconductor manufacturing process and its design rules

Transistor: a semiconductor device that serves as the gate regulating the flow of electrons

Wafer: thin round silicon disk used for the fabrication of integrated circuits

Wafer Fab Equipment (WFE): critical tools used in the manufacturing of semiconductors

Special Disclosures

Information on securities which are listed on the exchanges where ML Securities (Taiwan) Limited is not permitted to trade or solicit trades for clients is for informational purposes only and is not a recommendation or a solicitation to trade such securities. ML Securities (Taiwan) Limited will not execute transactions for nor accept orders from clients to trade such securities. Foreign investment in Taiwan securities is regulated and restricted. Currently, foreign investment in Taiwan securities is permitted by investment through: (1) global depository receipts, (2) convertible bonds, (3) mutual funds issued offshore of Taiwan, and (4) a special foreign institutional investors (FINIs) and foreign individual investors (FIDIs) program supervised by the Taiwan SFB whereunder FINIs/FIDIs may apply for investment ID to invest in Taiwan securities by registration with Taiwan Stock Exchange. FINIs will additionally need consent from the foreign exchange authority, ie, the Central Bank of China. In addition to the limitations above, various industry-specific percentage-based limitations on foreign ownership of Taiwan companies (and in some cases prohibitions) may apply. Investments are subject to exchange rate and currency conversion restrictions and risks. Dividends and interest earned by foreign investors' Taiwan securities/instruments are generally subject to a 20% withholding tax. Ordinary shares are not available to ML private client accounts in the U.S.

This report is distributed in the Republic of China by Merrill Lynch Securities (Taiwan) Limited, which is regulated by the SFB of the Republic of China.

Disclosures

Important Disclosures

FUNDAMENTAL EQUITY OPINION KEY: Opinions include a Volatility Risk Rating, an Investment Rating and an Income Rating. *VOLATILITY RISK RATINGS*, indicators of potential price fluctuation, are: A - Low, B - Medium and C - High. *INVESTMENT RATINGS* reflect the analyst's assessment of a stock's: (i) absolute total return potential and (ii) attractiveness for investment relative to other stocks within its *Coverage Cluster* (defined below). There are three investment ratings: 1 - Buy stocks are expected to have a total return of at least 10% and are the most attractive stocks in the coverage cluster; 2 - Neutral stocks are expected to remain flat or increase in value and are less attractive than Buy rated stocks and 3 - Underperform stocks are the least attractive stocks in a coverage cluster. Analysts assign investment ratings considering, among other things, the 0-12 month total return expectation for a stock and the firm's guidelines for ratings dispersions (shown in the table below). The current price objective for a stock should be referenced to better understand the total return expectation at any given time. The price objective reflects the analyst's view of the potential price appreciation (depreciation).

Investment rating	Total return expectation (within 12-month period of date of initial rating)	Ratings dispersion guidelines for coverage cluster*
Buy	≥ 10%	≤ 70%
Neutral	≥ 0%	≤ 30%
Underperform	N/A	≥ 20%

* Ratings dispersions may vary from time to time where BofA Global Research believes it better reflects the investment prospects of stocks in a Coverage Cluster.

***INCOME RATINGS*, indicators of potential cash dividends, are: 7 - same/higher (dividend considered to be secure), 8 - same/lower (dividend not considered to be secure) and 9 - pays no cash dividend.** *Coverage Cluster* is comprised of stocks covered by a single analyst or two or more analysts sharing a common industry, sector, region or other classification(s). A stock's coverage cluster is included in the most recent BofA Global Research report referencing the stock.

BofA Global Research personnel (including the analyst(s) responsible for this report) receive compensation based upon, among other factors, the overall profitability of Bank of America Corporation, including profits derived from investment banking. The analyst(s) responsible for this report may also receive compensation based upon, among other factors, the overall profitability of the Bank's sales and trading businesses relating to the class of securities or financial instruments for which such analyst is responsible.

Other Important Disclosures

From time to time research analysts conduct site visits of covered issuers. BofA Global Research policies prohibit research analysts from accepting payment or reimbursement for travel expenses from the issuer for such visits.

Prices are indicative and for information purposes only. Except as otherwise stated in the report, for the purpose of any recommendation in relation to: (i) an equity security, the price referenced is the publicly traded price of the security as of close of business on the day prior to the date of the report or, if the report is published during intraday trading, the price referenced is indicative of the traded price as of the date and time of the report; or (ii) a debt security (including equity preferred and CDS), prices are indicative as of the date and time of the report and are from various sources including BofA Securities trading desks.

The date and time of completion of the production of any recommendation in this report shall be the date and time of dissemination of this report as recorded in the report timestamp.

Recipients who are not institutional investors or market professionals should seek the advice of their independent financial advisor before considering information in this report in connection with any investment decision, or for a necessary explanation of its contents.

Officers of BofAS or one or more of its affiliates (other than research analysts) may have a financial interest in securities of the issuer(s) or in related investments.

BofA Global Research policies relating to conflicts of interest are described at https://rsch.baml.com/coi

"BofA Securities" includes BofA Securities, Inc. ("BofAS") and its affiliates. Investors should contact their BofA Securities representative or Merrill Global Wealth Management financial advisor if they have questions concerning this report or concerning the appropriateness of any investment idea described herein for such investor. "BofA Securities" is a global brand for BofA Global Research.

Information relating to Non-US affiliates of BofA Securities and Distribution of Affiliate Research Reports:

BofAS and/or Merrill Lynch, Pierce, Fenner & Smith ("MLPF&S") may in the future distribute, information of the following non-US affiliates in the US (short name: legal name, regulator): Merrill Lynch (South Africa): Merrill Lynch South Africa (Pty) Ltd., regulated by The Financial Service Board; MLI (UK): Merrill Lynch International, regulated by the Financial Conduct Authority (FCA) and the Prudential Regulation Authority (PRA); BofASE (France): BofA Securities Europe SA is authorized by the Autorité de Contrôle Prudentiel et de Résolution (ACPR) and regulated by the ACPR and the Autorité des Marchés Financiers (AMF); BofA Europe (Milan): Bank of America Europe Designated Activity Company, Milan Branch, regulated by the Bank of Italy, the European Central Bank (ECB) and the Central Bank of Ireland (CBI); BofA Europe (Frankfurt): Bank of America Europe Designated Activity Company, Frankfurt Branch regulated by BaFin, the ECB and the CBI; Merrill Lynch (Australia): Merrill Lynch Equities (Australia) Limited, regulated by the Australian Securities and Investments Commission; Merrill Lynch (Hong Kong): Merrill Lynch (Asia Pacific) Limited, regulated by the Hong Kong Securities and Futures Commission (HKSFC); Merrill Lynch (Singapore): Merrill Lynch (Singapore) Pte Ltd, regulated by the Monetary Authority of Singapore (MAS); Merrill Lynch (Canada): Merrill Lynch Canada Inc, regulated by the Investment Industry Regulatory Organization of Canada; Merrill Lynch (Mexico): Merrill Lynch Mexico, SA de CV, Casa de Bolsa, regulated by the Comisión Nacional Bancaria y de Valores; Merrill Lynch (Argentina): Merrill Lynch Argentina SA, regulated by Comisión Nacional de Valores; BofAS Japan: BofA Securities Japan Co., Ltd., regulated by the Financial Services Agency; Merrill Lynch (Seoul): Merrill Lynch International, LLC Seoul Branch, regulated by the Financial Supervisory Service; Merrill Lynch (Taiwan): Merrill Lynch Securities (Taiwan) Ltd., regulated by the Securities and Futures Bureau; BofAS India: BofA Securities India Limited, regulated by the Securities and Exchange Board of India (SEBI); Merrill Lynch (Indonesia): PT Merrill Lynch Sekuritas Indonesia, regulated by Otoritas Jasa Keuangan (OJK); Merrill Lynch (Israel): Merrill Lynch Israel Limited, regulated by Israel Securities Authority; Merrill Lynch (Russia): OOO Merrill Lynch Securities, Moscow, regulated by the Central Bank of the Russian Federation; Merrill Lynch (DIFC): Merrill Lynch International (DIFC Branch), regulated by the Dubai Financial Services Authority (DFSA); Merrill Lynch (Spain): Merrill Lynch Capital Markets Espana, S.A.S.V., regulated by Comisión Nacional del Mercado De Valores; Merrill Lynch (Brazil): Merrill Lynch S.A. Corretora de Títulos e Valores Mobiliários, regulated by Comissão de Valores Mobiliários; Merrill Lynch KSA Company: Merrill Lynch Kingdom of Saudi Arabia Company, regulated by the Capital Market Authority.

This information: has been approved for publication and is distributed in the United Kingdom (UK) to professional clients and eligible counterparties (as each is defined in the rules of the FCA and the PRA) by MLI (UK), which is authorized by the PRA and regulated by the FCA and the PRA - details about the extent of our regulation by the FCA and PRA are available from us on request; has been approved for publication and is distributed in the European Economic Area (EEA) by BofASE (France), which is authorized by the ACPR and regulated by the ACPR and the AMF; has been considered and distributed in Japan by BofAS Japan, a registered securities dealer under the Financial Instruments and Exchange Act in Japan, or its permitted affiliates; is issued and distributed in Hong Kong by Merrill Lynch (Hong Kong) which is regulated by HKSFC; is issued and distributed in Taiwan by Merrill Lynch (Taiwan); is issued and distributed in India by BofAS India; and is issued and distributed in Singapore to institutional investors and/or accredited investors (each as defined under the Financial Advisers Regulations) by Merrill Lynch (Singapore) (Company Registration No 198602883D). Merrill Lynch (Singapore) is regulated by MAS. Merrill Lynch Equities (Australia) Limited (ABN 65 006 276 795), AFS License 235132 (MLEA) distributes this information in Australia only to 'Wholesale' clients as defined by s.761G of the Corporations Act 2001. With the exception of Bank of America N.A., Australia Branch, neither MLEA nor any of its affiliates involved in preparing this information is an Authorised Deposit-Taking Institution under the Banking Act 1959 nor regulated by the Australian Prudential Regulation Authority. No approval is required for publication or distribution of this information in Brazil and its local distribution is by Merrill Lynch (Brazil) in accordance with applicable regulations. Merrill Lynch (DIFC) is authorized and regulated by the DFSA. Information prepared and issued by Merrill Lynch (DIFC) is done so in accordance with the requirements of the DFSA conduct of business rules. BofA Europe (Frankfurt) distributes this information in Germany and is regulated by BaFin, the ECB and the CBI. BofA Securities entities, including BofA Europe and BofASE (France), may outsource/delegate the marketing and/or provision of certain research services or aspects of research services to other branches or members of the BofA Securities group. You may be contacted by a different BofA Securities entity acting for and on behalf of your service provider where permitted by applicable law. This does not change your service provider. Please use this link

http://www.bankofamerica.com/emaildisclaimer for further information
This information has been prepared and issued by BofAS and/or one or more of its non-US affiliates. The author(s) of this information may not be licensed to carry on regulated activities in your jurisdiction and, if not licensed, do not hold themselves out as being able to do so. BofAS and/or MLPF&S is the distributor of this information in the US and accepts full responsibility for information distributed to BofAS and/or MLPF&S clients in the US by its non-US affiliates. Any US person receiving this information and wishing to effect any transaction in any security discussed herein should do so through BofAS and/or MLPF&S and not such foreign affiliates. Hong Kong recipients of this information should contact Merrill Lynch (Asia Pacific) Limited in respect of any matters relating to dealing in securities or provision of specific advice on securities or any other matters arising from, or in connection with, this information. Singapore recipients of this information should contact Merrill Lynch (Singapore) Pte Ltd in respect of any matters arising from, or in connection with, this information.

General Investment Related Disclosures:

Taiwan Readers: Neither the information nor any opinion expressed herein constitutes an offer or a solicitation of an offer to transact in any securities or other financial instrument. No part of this report may be used or reproduced or quoted in any manner whatsoever in Taiwan by the press or any other person without the express written consent of BofA Securities.
This document provides general information only, and has been prepared for, and is intended for general distribution to, BofA Securities clients. Neither the information nor any opinion expressed constitutes an offer or an invitation to make an offer, to buy or sell any securities or other financial instrument or any derivative related to such securities or instruments (e.g., options, futures, warrants, and contracts for differences). This document is not intended to provide personal investment advice and it does not take into account the specific investment objectives, financial situation and the particular needs of, and is not directed to, any specific person(s). This document and its content do not constitute, and should not be considered to constitute, investment advice for purposes of ERISA, the US tax code, the Investment Advisers Act or otherwise. Investors should seek financial advice regarding the appropriateness of investing in financial instruments and implementing investment strategies discussed or recommended in this document and should understand that statements regarding future prospects may not be realized. Any decision to purchase or subscribe for securities in any offering must be based solely on existing public information on such security or the information in the prospectus or other offering document issued in connection with such offering, and not on this document.
Securities and other financial instruments referred to herein, or recommended, offered or sold by BofA Securities, are not insured by the Federal Deposit Insurance Corporation and are not deposits or other obligations of any insured depository institution (including, Bank of America, N.A.). Investments in general and, derivatives, in particular, involve numerous risks, including, among others, market risk, counterparty default risk and liquidity risk. No security, financial instrument or derivative is suitable for all investors. In some cases, securities and other financial instruments may be difficult to value or sell and reliable information about the value or risks related to the security or financial instrument may be difficult to obtain. Investors should note that income from such securities and other financial instruments, if any, may fluctuate and that price or value of such securities and instruments may rise or fall and, in some cases, investors may lose their entire principal investment. Past performance is not necessarily a guide to future performance. Levels and basis for taxation may change.
This report may contain a short-term trading idea or recommendation, which highlights a specific near-term catalyst or event impacting the issuer or the market that is anticipated to have a short-term price impact on the equity securities of the issuer. Short-term trading ideas and recommendations are different from and do not affect a stock's fundamental equity rating, which reflects both a longer term total return expectation and attractiveness for investment relative to other stocks within its Coverage Cluster. Short-term trading ideas and recommendations may be more or less positive than a stock's fundamental equity rating.
BofA Securities is aware that the implementation of the ideas expressed in this report may depend upon an investor's ability to "short" securities or other financial instruments and that such action may be limited by regulations prohibiting or restricting "shortselling" in many jurisdictions. Investors are urged to seek advice regarding the applicability of such regulations prior to executing any short idea contained in this report.
Foreign currency rates of exchange may adversely affect the value, price or income of any security or financial instrument mentioned herein. Investors in such securities and instruments, including ADRs, effectively assume currency risk.
UK Readers: The protections provided by the U.K. regulatory regime, including the Financial Services Scheme, do not apply in general to business coordinated by BofA Securities entities located outside of the United Kingdom.
BofAS or one of its affiliates is a regular issuer of traded financial instruments linked to securities that may have been recommended in this report. BofAS or one of its affiliates may, at any time, hold a trading position (long or short) in the securities and financial instruments discussed in this report.
BofA Securities, through business units other than BofA Global Research, may have issued and may in the future issue trading ideas or recommendations that are inconsistent with, and reach different conclusions from, the information presented herein. Such ideas or recommendations may reflect different time frames, assumptions, views and analytical methods of the persons who prepared them, and BofA Securities is under no obligation to ensure that such other trading ideas or recommendations are brought to the attention of any recipient of this information.
In the event that the recipient received this information pursuant to a contract between the recipient and BofAS for the provision of research services for a separate fee, and in connection therewith BofAS may be deemed to be acting as an investment adviser, such status relates, if at all, solely to the person with whom BofAS has contracted directly and does not extend beyond the delivery of this report (unless otherwise agreed specifically in writing by BofAS If such recipient uses the services of BofAS in connection with the sale or purchase of a security referred to herein, BofAS may act as principal for its own account or as agent for another person. BofAS is and continues to act solely as a broker-dealer in connection with the execution of any transactions, including transactions in any securities referred to herein.

Copyright and General Information:

Materials prepared by BofA Global Research personnel are based on public information. Facts and views presented in this material have not been reviewed by, and may not reflect information known to, professionals in other business areas of BofA Securities, including investment banking personnel. BofA Securities has established information barriers between BofA Global Research and certain business groups. As a result, BofA Securities does not disclose certain client relationships with, or compensation received from, such issuers. To the extent this material discusses any legal proceeding or issues, it has not been prepared as nor is it intended to express any legal conclusion, opinion or advice. Investors should consult their own legal advisers as to issues of law relating to the subject matter of this material. BofA Global Research personnel's knowledge of legal proceedings in which any BofA Securities entity and/or its directors, officers and employees may be plaintiffs, defendants, co-defendants or co-plaintiffs with or involving issuers mentioned in this material is based on public information. Facts and views presented in this material that relate to any such proceedings have not been reviewed by, discussed with, and may not reflect information known to, professionals in other business areas of BofA Securities in connection with the legal proceedings or matters relevant to such proceedings.
This information has been prepared independently of any issuer of securities mentioned herein and not in connection with any proposed offering of securities or as agent of any issuer of any securities. None of BofAS any of its affiliates or their research analysts has any authority whatsoever to make any representation or warranty on behalf of the issuer(s). BofA Global Research policy prohibits research personnel from disclosing a recommendation, investment rating, or investment thesis for review by an issuer prior to the publication of a research report containing such rating, recommendation or investment thesis.
Any information relating to the tax status of financial instruments discussed herein is not intended to provide tax advice or to be used by anyone to provide tax advice. Investors are urged to seek tax advice based on their particular circumstances from an independent tax professional.
The information herein (other than disclosure information relating to BofA Securities and its affiliates) was obtained from various sources and we do not guarantee its accuracy. This information may contain links to third-party websites. BofA Securities is not responsible for the content of any third-party website or any linked content contained in a third-party website. Content contained on such third-party websites is not part of this information and is not incorporated by reference. The inclusion of a link does not imply any endorsement by or any affiliation with BofA Securities. Access to any third-party website is at your own risk, and you should always review the terms and privacy policies at third-party websites before submitting any personal information to them. BofA Securities is not responsible for such terms and privacy policies and expressly disclaims any liability for them.
All opinions, projections and estimates constitute the judgment of the author as of the date of publication and are subject to change without notice. Prices also are subject to change without notice. BofA Securities is under no obligation to update this information and BofA Securities ability to publish information on the subject issuer(s) in the future is subject to applicable quiet periods. You should therefore assume that BofA Securities will not update any fact, circumstance or opinion contained herein.
Certain outstanding reports or investment opinions relating to securities, financial instruments and/or issuers may no longer be current. Always refer to the most recent research report relating to an issuer prior to making an investment decision.

In some cases, an issuer may be classified as Restricted or may be Under Review or Extended Review. In each case, investors should consider any investment opinion relating to such issuer (or its security and/or financial instruments) to be suspended or withdrawn and should not rely on the analyses and investment opinion(s) pertaining to such issuer (or its securities and/or financial instruments) nor should the analyses or opinion(s) be considered a solicitation of any kind. Sales persons and financial advisors affiliated with BofAS or any of its affiliates may not solicit purchases of securities or financial instruments that are Restricted or Under Review and may only solicit securities under Extended Review in accordance with firm policies.
Neither BofA Securities nor any officer or employee of BofA Securities accepts any liability whatsoever for any direct, indirect or consequential damages or losses arising from any use of this information.