



Global Semiconductor/Memory

Beyond Moore's Law: 3D Architecture with Material Innovation

- **Top picks in migration to 3D architecture** — To increase a semiconductor chip's capacity, future tech migration will increasingly adopt 3D architecture – entailing stacking of layers – rather than follow the past practice of advancing tech nodes. Our top Buys in this migration are Samsung, TSMC, and Sony for their 3D architecture technology leadership. Among SPE/material plays, we have Buys on LAM Research (CVD/Etch), TEL (CVD/Etch), Entegris (Chemicals), and ASM Pacific (Package). We believe 3D architecture, which is being significantly used in the NAND space already, will be adopted in DRAM and Logic products as well.
- **3D DRAM: HBM3 + High-K + 3D Architecture** — In DRAM, adoption of 3D architecture is expected to take place in the following order: 1) with HBM (High Bandwidth Memory), which stacks chips on other chips and connects them using the TSV method, for AI computing applications; 2) with innovations in semiconductor materials (such as HfO₂ and Nb); and 3) changes in the architecture itself, migrating from the current 2D to 3D architecture.
- **3D NAND: Multiple (Double/Triple) Stacking + Vertical Scaling + Cell on Peri** — In NAND, we expect 3D NAND architecture to develop further with 1) additional stacking of layers with COP (Cell-on-Peri) technology, and 2) adoption of double/triple stacking. For example, Samsung Electronics has employed only a single stacking method until now, but due to increasing difficulties in the etching process with the increased number of layers stacked, the company is expected to begin adopting the double stacking method from 176L 3D NAND products in 2021E.
- **3D Logic/Foundry: GAA + Nanosheet + EUV** — In Logic, we foresee a transition to 3D architecture beginning in earnest with the shift in transistor's architecture from FinFET to GAA (Gate All Around). GAA is expected to be widely adopted from sub-3nm nodes, and Samsung is projected to use MBCFET architecture to vertically stack nano sheets for chips under 3nm.
- **Market Impact 1: Escalating technological difficulties in Memory and Foundry** — We expect the adoption of 3D structure to materially impact the semiconductor market. In memory, we anticipate increased adoption of 3D DRAM and 3D NAND leading to a more complex fabrication process. In logic/foundry, we believe the shift in 3D architecture with EUV will further strengthen market leaders' technological / production edge and facilitate consolidation of the semiconductor market.
- **Market Impact 2: Higher demand for CVD/CMP/Etch process** — We project 3D architecture will have significant impacts on SPE and materials companies. In particular, we anticipate wider adoption of the 3D structure to lead to increased demand for etching, CMP, and ALD equipment/materials.

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See Appendix A-1 for Analyst Certification, Important Disclosures and non-US research analyst disclosures.

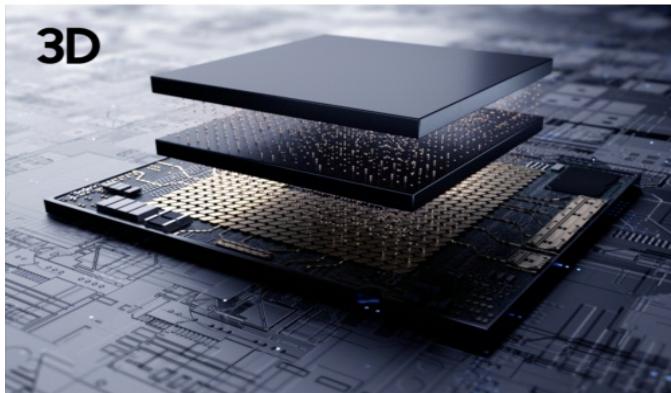
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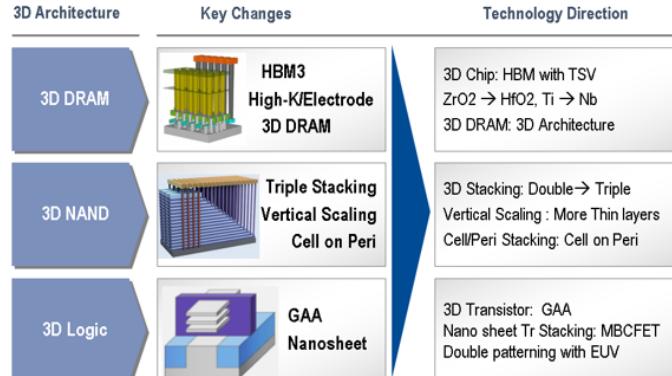
Key Charts

Figure 1. Technology Direction: 3D Structure + Material Innovation



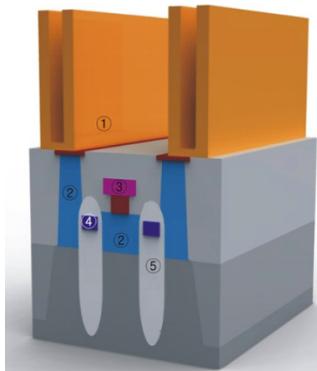
Source: Samsung Electronics

Figure 2. 3D DRAM + 3D NAND + 3D Logic Direction



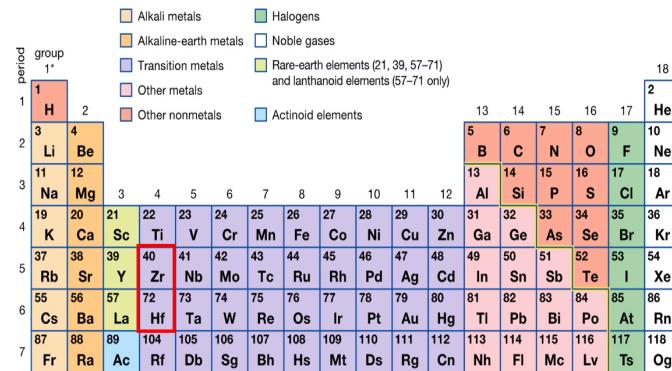
Source: Citi Research

Figure 3. 3D DRAM: HBM3 + High-K + 3D DRAM



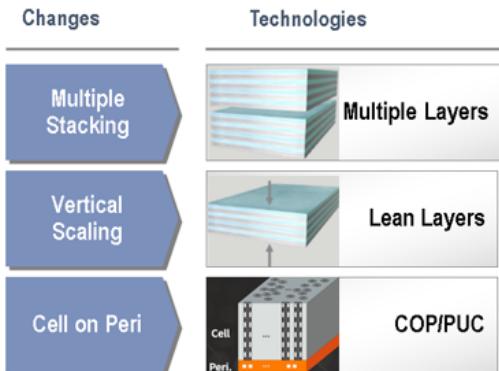
Source: Google search

Figure 4. DRAM High-K Material Changes: Zr → Hf



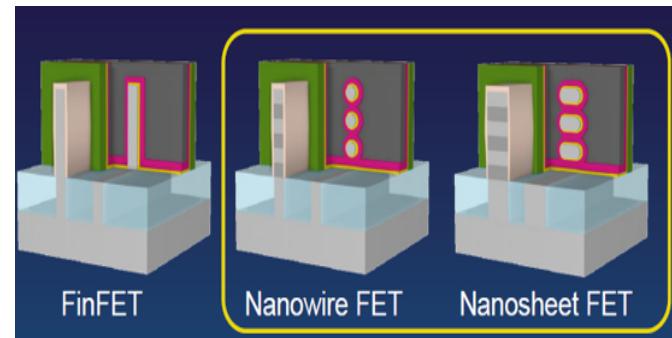
Source: Citi Research

Figure 5. 3D NAND: Multiple Stacking + Vertical Scaling + COP



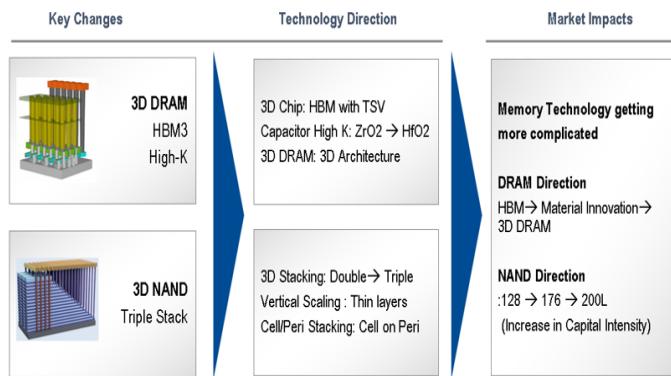
Source: Citi Research

Figure 6. 3D Logic/Foundry: : 3D Tr + Nano sheet + EUV with DPT



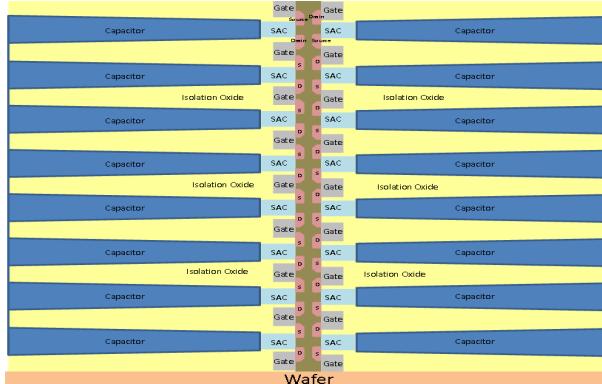
Source: Samsung Electronics

Figure 7. Market Impact 1: Memory Technology to be complicated



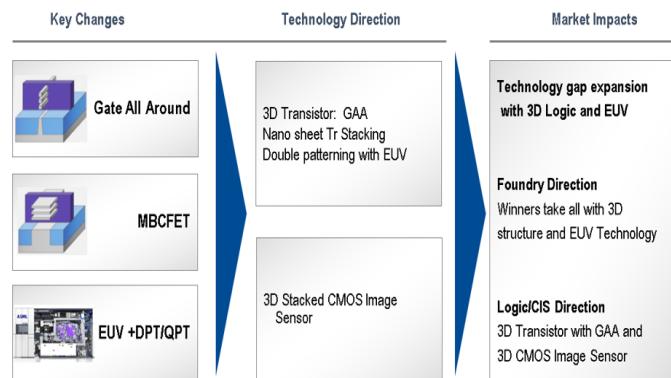
Source: Citi Research

Figure 8. 3D DRAM Scheme(Similar to 3D NAND)



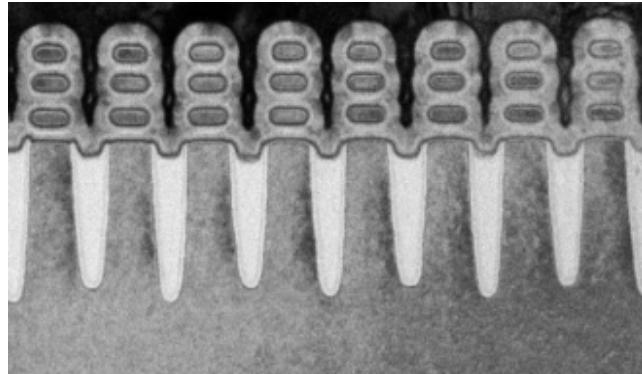
Source: Citi Research

Figure 9. Market Impact 2: Foundry/Logic Tech Gap expansion



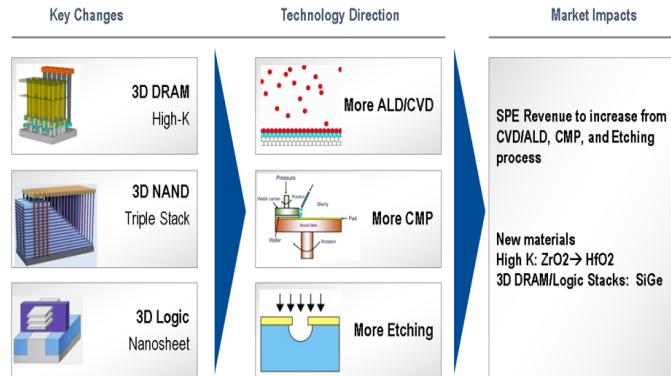
Source: Citi Research

Figure 10. 3D Logic Nano sheet



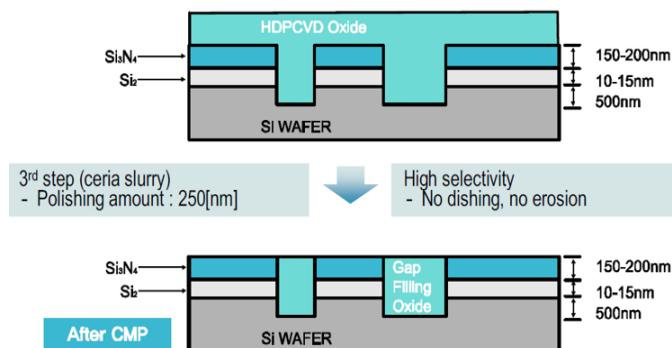
Source: Samsung Electronics

Figure 11. Market Impact 3: SPE/Material names to get benefit



Source: Citi Research

Figure 12.: CVD/ALD,CMP and Etching Process to increase



Source: Citi Research

Executive Summary

Technology Direction: 3D Architecture

We project the semiconductor industry will experience increased adoption of 3D architecture across different products. In particular, DRAM and Logic would gradually adopt 3D architecture, following NAND that has already adopted a 3D structure. In DRAM, adoption of 3D architecture is expected to take place in the following order: 1) firstly with HBM (High Bandwidth Memory), which stacks chips on other chips and connects them using the TSV method, 2) secondly with innovations in semiconductor materials (such as HfO₂ and Nb), and 3) lastly with the changes in the architecture itself, migrating from the current 2D architecture to 3D architecture that is similar to the 3D NAND architecture.

In NAND, we expect 3D NAND architecture will develop further with 1) additional stacking of layers with COP (Cell-on-Peri) technology, and 2) adoption of double/triple stacking. For example, Samsung Electronics has only employed a single stacking method until now, but due to increasing difficulties in the etching process with the increased number of layers, the company is expected to begin adopting a double stacking method from 176L 3D NAND products in 2021E.

Lastly, in Logic, we foresee transition to 3D architecture will begin in earnest with the shift in transistor's architecture from FinFET to GAA (Gate All Around). GAA is expected to be widely adopted from sub-3nm nodes, and Samsung is projected to use MBCFET architecture to vertically stack nano sheets for chips under 3nm.

3D DRAM: HBM3 + High-K + 3D Architecture

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Unlike NAND, DRAM architecture has remained in 2D structure until now. While HBM technology that utilizes TSV method has been already deployed, the HBM's architecture structurally differs from that of 3D NAND in that HBM achieves 3D architecture by stacking 2D DRAM chips on one another, rather than stacking layers within a DRAM chip.

Despite limited deployment of HBM structure, we consider HBM as an intermediary step to eventually reach 3D DRAM architecture. In addition, we believe innovations in materials will continuously take place in High-K and Electrode, especially for sub-1nm chips, to enhance permittivity and conductivity. While we believe DRAM structure will eventually evolve into a 3D structure similar to 3D NAND, the change will take place in the order of 1) HBM, 2) material innovation and 3) architecture change to 3D DRAM.

3D NAND: Multiple Stacking + Vertical Scaling + Cell on Peri

3D NAND: Multiple Stacking + Vertical Scaling + Cell on Peri

The first direction in NAND technology we project is the gradual adoption of multi stacking technology. Samsung Electronics, which has only relied on single stacking in the past, is expected to begin adopting double stacking from 176L, while other NAND producers are likely to adopt triple stacking amid continued competition to increase the number of layer stacking.

The second direction in NAND technology we foresee is vertical scaling. With the number of layers in 3D NAND exceeding 100, layers have begun to be affected by gravity. While 3D NAND was in the nano-scale in the past, thereby immune to gravity, from 100L and onward, 3D NAND has entered micro-scale stage and has begun to be impacted by gravity, which has forced producers to take gravity into consideration in the fabrication process.

The third direction we anticipate is Cell on Peri (forming Peri first and then placing cell on top of Peri). We project adoption of the new technology will result in the reduction of chip size by 20~30%.

3D Logic/Foundry: GAA + Nano sheet + EUV

3D Logic/Foundry: GAA + Nano sheet + EUV

We expect 3D structure will migrate to GAA (Gate All Around) technology in earnest from 3nm and onwards. In particular, Samsung Electronics has been preparing to launch MBCFET technology in logic fabrication process, which will adopt nano sheet technology in GAA structure. The vertical stacking technology is projected to be broadly similar to 3D NAND architecture, but for logic, we expect 1) sequential deposition of Si and SiGe, and 2) GAA structure formation through epitaxial growth process, to distinguish vertical logic structure from 3D NAND structure.

Market Impacts from 3D Architecture

Market Impact 1: Memory → Increased Technical difficulties with 3D Architecture

We expect the introduction of 3D structure and new semiconductor materials will lead to meaningful changes in the semiconductor market. In memory, we anticipate increased adoption of 3D DRAM and 3D NAND will lead to more complex fabrication process. We expect Samsung to lead 3D DRAM and 3D NAND structures with architecture innovation and material changes.

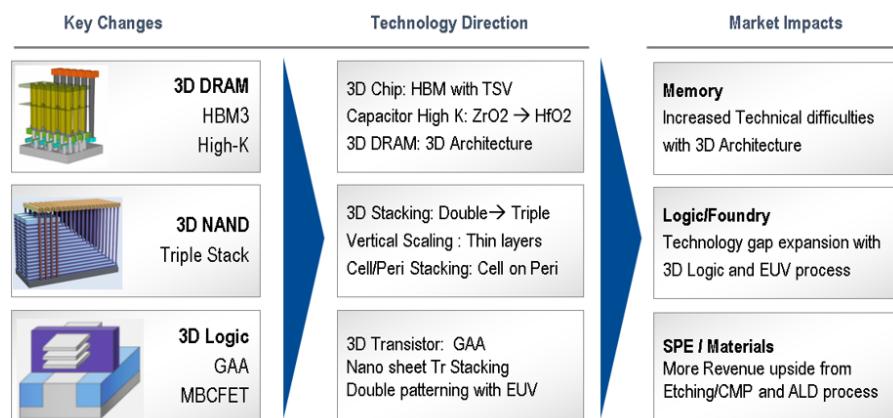
Market Impact 2: Logic/Foundry → Technology gap expansion with 3D Logic and EUV

In logic/foundry, we believe the shift in transistors' architecture from planar to FinFET, and then to GAA and Nano Sheet after 3nm would widen the technology gap between the industry's leaders and followers. In addition, we anticipate the introduction of EUV-based technologies to further strengthen market leaders' technological edge and facilitate consolidation of semiconductor market. We are positive on Samsung and TSMC, as we see them leading 3D architecture technology with EUV. In addition, we are positive on Sony; as it will lead 3D stacking technology revolutionized image sensors.

Market Impact 3: More CVD/ALD/CMP Etching Process, and New materials

Lastly, we project shifts in semiconductor technologies to have significant impacts on SPE and materials companies in semiconductor value chains. In particular, we anticipate wider adoption of 3D structure to lead to increased demand for etching, CMP, and ALD equipment/materials. Among SPE/material global plays, we are positive on LAM Research (CVD/Etch), TEL (CVD/Etch), Entegris (Chemicals) and ASM Pacific (Package).

Figure 13. Market Impacts from 3D Architecture



Source: Citi Research

Figure 14. Valuation Comps

Company	Ticker	Market Cap	Close Price	Target Price	Citi Rating	P/E (x)		P/B (x)		EV/EBITDA (x)		Div Yield (%)	
		US\$mn	Local ccy	Local ccy		2020	2021	2020	2021	2020	2021	2020	2021
TSMC	2330.TW	452,253	497	561	Buy	24.9x	22.5x	7.1x	6.8x	14.0x	11.7x	2.2%	2.3%
Samsung Elec.	005930.KS	378,756	69,800	86,000	Buy	17.8x	15.0x	1.7x	1.6x	4.9x	4.3x	2.0%	2.0%
ASML	ASML.AS	191,387	371	380	Buy	47.8x	38.5x	10.9x	10.0x	37.0x	30.1x	0.7%	0.8%
Sony	6758.T	115,364	9,765	11,300	Buy	20.7x	14.8x	2.9x	2.5x	8.7x	9.4x	0.5%	0.5%
Micron	MU.O	77,190	69	35	Sell	27.1x	20.2x	1.9x	1.7x	8.6x	6.9x	nm	nm
Lam Research	LRCX.O	69,012	479	420	Buy	30.1x	22.1x	13.4x	10.4x	22.7x	16.9x	0.9%	1.0%
Tokyo Electron	8035.T	55,910	37,550	32,000	Buy	32.4x	26.9x	7.0x	6.0x	20.0x	16.5x	1.6%	1.9%
SMIC	0981.HK	16,426	22	20	Sell	33.8x	243.3x	1.0x	1.1x	13.4x	12.5x	nm	nm
Western Digital	WDC.O	14,519	48	60	Buy	15.7x	15.8x	1.5x	1.5x	10.0x	9.8x	4.2%	nm
Entegris	ENTG.O	12,580	93	92	Buy	37.6x	33.0x	9.1x	7.1x	22.1x	20.0x	nm	nm
ASM Pacific	0522.HK	5,027	95	107	Buy	44.2x	23.1x	3.2x	3.0x	18.5x	12.5x	1.4%	2.2%
CMC Materials	CCMP.O	4,355	150	140	Sell	20.1x	22.4x	4.1x	3.7x	11.4x	11.6x	1.1%	1.1%

Source: dataCentral, Citi Research, as of Dec 3rd closing prices

Moore's Law

Moore's Law

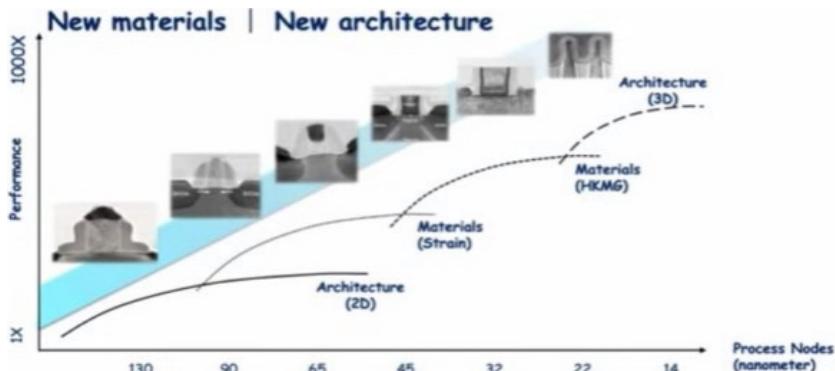
More than Moore's

Moore's Law turns 55 years old this year. It states that transistor density and chip performance will double every 18~24 months, and has been relevant to the semiconductor industry for over half a century. But, as the semiconductor industry faces ever-greater obstacles in further advancing semiconductor technologies, market participants are now wondering whether Moore's Law will remain valid.

In an effort to keep up with Moore's Law, the semiconductor industry has shifted focus to 3D structures. With the 3D structure era (for the semiconductor industry) now upon us, we predict that all semiconductor products including DRAM, NAND and Logic will adopt and evolve 3D Architectures.

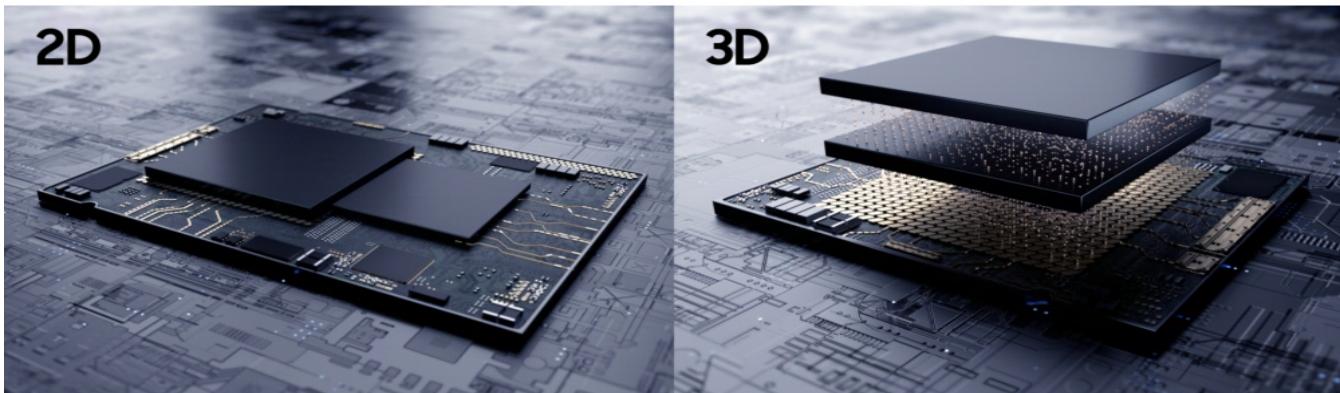
In the semiconductor chip manufacturing industry, we foresee a rapid technological advance towards 3D structures not only in front-end processes, but also in back-end processes. Currently, chip makers are striving to develop higher-stacked NAND, whilst tech migration continues for DRAM/logic, despite increasing technological challenges. In order to facilitate DRAM/logic tech migration, chip makers are aiming to apply 3D architecture for DRAM/Logic devices. At the same time, stacking is also being carried out in 3D structures, with 3D packaging technology set to expand in earnest.

Figure 15. Beyond Moore's Law with 3D Architecture



Source: Samsung Electronics

Figure 16. 3D Architecture



Source: Samsung Electronics

Technology Direction: 3D Architecture

3D DRAM + 3D NAND + 3D Logic

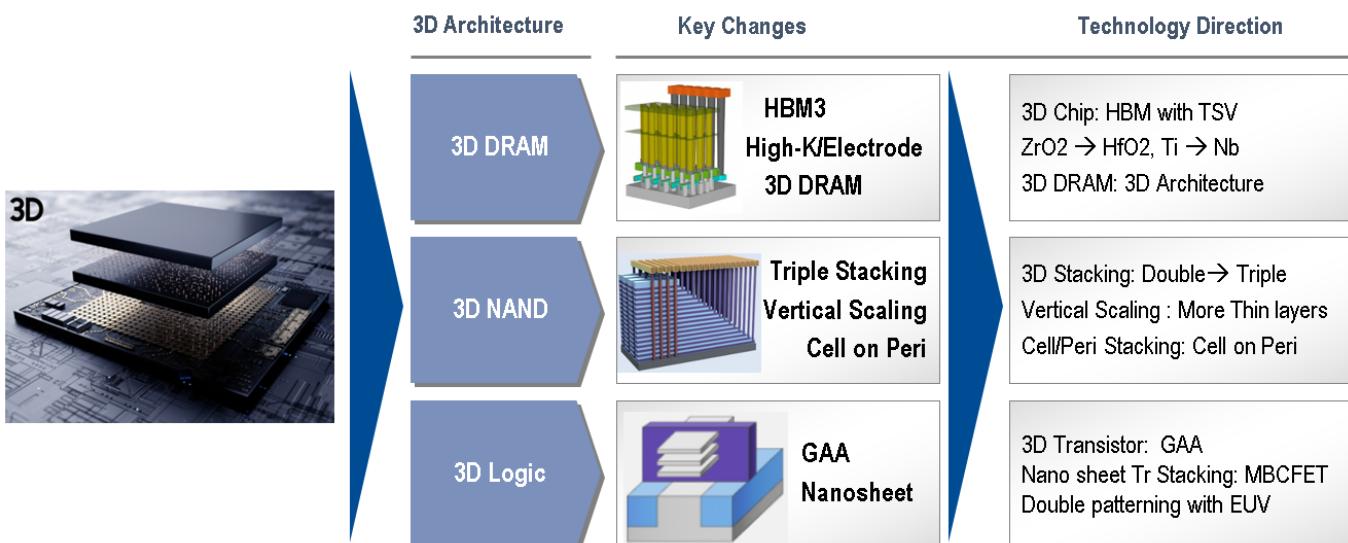
We project increased adoption of 3D architecture across different semiconductor products will drive tech migration in the future. In particular, we believe the 3D architecture, which has seen significant adoption in NAND space already, will be increasingly adopted in DRAM and Logic products as well.

In DRAM, adoption of 3D architecture is expected to take place in the following order: 1) firstly with HBM (High Bandwidth Memory), which stacks chips on other chips and connect them using TSV method, for AI and high performance computing applications, 2) secondly with innovations in semiconductor materials (such as HfO₂ and Nb), and 3) lastly with changes in the architecture itself, migrating from current 2D architecture to 3D architecture.

In NAND, we expect 3D NAND architecture will develop further with 1) additional stacking of layers with COP (Cell-on-Peri) technology, and 2) adoption of double/triple stacking. Of note, Samsung Electronics has employed only a single stacking method until now, but due to increasing difficulties in the etching process with the increased number of stacked layers, the company is expected to begin adopting a double stacking method from 176L 3D NAND products in 2021E.

Lastly, in Logic, we foresee transition to 3D architecture will begin in earnest with the shift in transistor's architecture from FinFET to GAA (Gate All Around). GAA is expected to be widely adopted from sub-3nm nodes, and Samsung is projected to use MBCFET architecture to vertically stack nano sheets for chips under 3nm.

Figure 17. 3D Architecture Direction: 3D DRAM + 3D NAND + 3D Logic



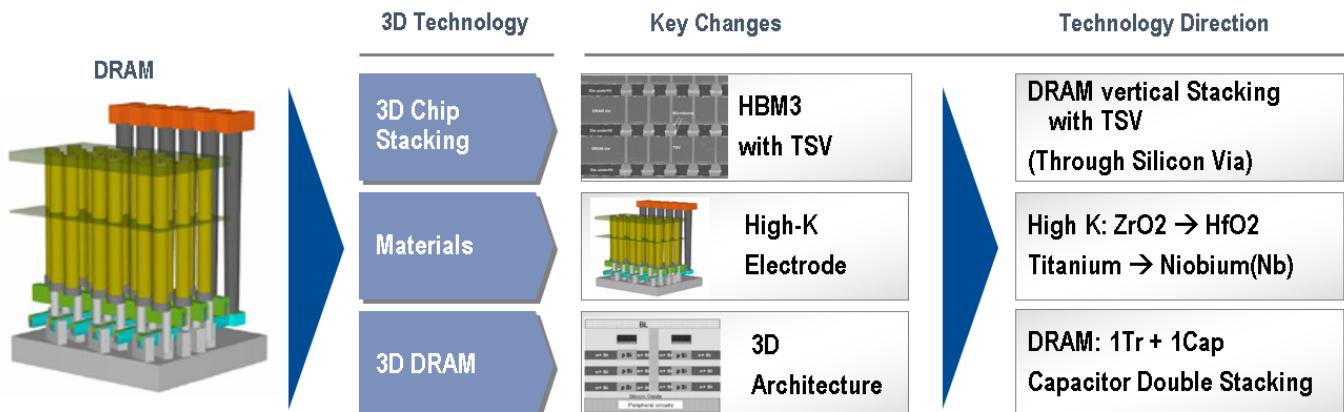
Source: Citi Research

3D DRAM: HBM3 + High-K + 3D Architecture

Unlike NAND, DRAM architecture has remained in 2D structure until now. While HBM technology that utilizes the TSV method has been already deployed, the HBM's architecture structurally differs from that of 3D NAND in that HBM achieves 3D architecture by stacking 2D DRAM chips on one another, rather than stacking layers within a DRAM chip. Despite limited deployment of HBM structure, we consider HBM as an intermediary step to eventually reach 3D DRAM architecture. In addition, we believe innovations in materials will continuously take place in High-

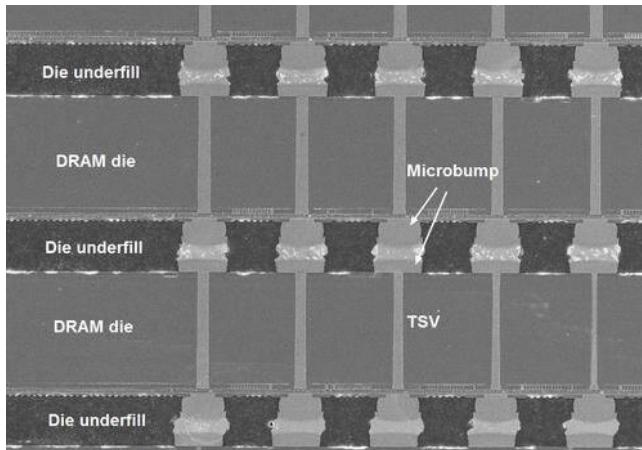
K and Electrode, especially for sub-1nm chips, to enhance permittivity and conductivity. While we believe DRAM structure will eventually evolve into 3D structure similar to 3D NAND, we project the change will take place in the order of 1) HBM, 2) material innovation and 3) architecture change to 3D DRAM.

Figure 18. DRAM Technology Direction



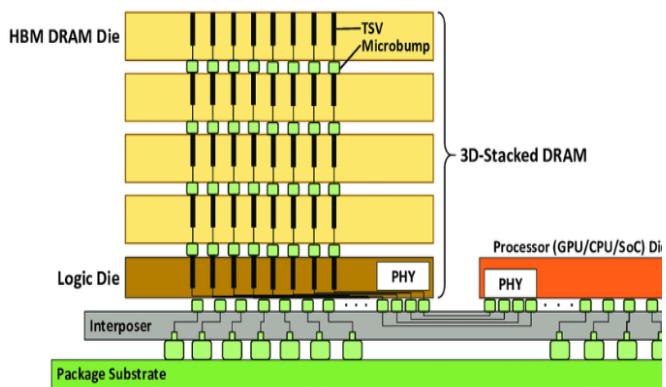
Source: Citi Research

Figure 19. HBM(High Bandwidth Memory) with TSV



Source: Samsung

Figure 20. 3D TSV(Through Silicon Via) DRAM



Source: Samsung

The first innovation direction in DRAM we project is 3D stacking of chips, namely HBM technology with TSV method.

HBM is an in-package memory where it is integrated with a SoC through a silicon interposer inside the same package. This allows it to overcome the maximum number of data I/O package pin limitations, which would otherwise exist in conventional off-chip packages.

HBM2, which has already been deployed in actual products, consists of 4 or 8-high stacks of 8Gb dies and 1,024 data pins running at 1.6~2.4Gbps each. This results in 4 or 8GB density and 204~307GB/s bandwidth per HBM stack.

TSV technology has now reached its maturity to some extent, being able to build state-of-the-art products such as HBM2Es with thousands of TSVs. In future, however, decreasing the TSV pitch/diameter/aspect-ratio and the die thickness,

while still maintaining high assembly yields, will become more challenging and essential for continued future device performance and capacity scaling.

Such improvements will allow decreased TSV loadings, reduced TSV relative die size portions, and the extended number of stacks beyond 12Highs while still maintaining the same total physical stack height.

Figure 21. Semiconductor Technology Direction

	HBM2	HBM2E	HBM3
Max Pin Data Rate	2.4Gbps	3.2Gbps	4Gbps (Expected)
Max Capacity	16GB	24GB	64GB
Max Bandwidth	307GB/s	410GB/s	512GB/s

Source: Citi Research

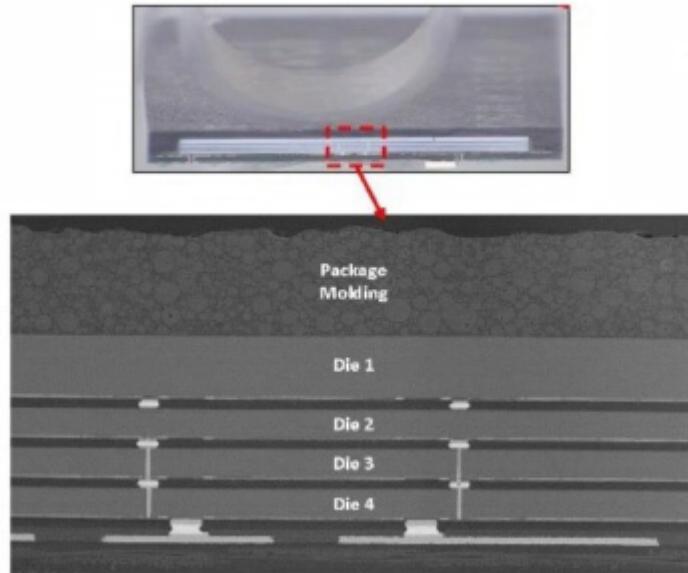
HBM3 will double the density of the individual memory dies from 8Gb to 16Gb (~2GB), and will allow for more than eight dies to be stacked together in a single chip. Graphics cards with up to 64GB of memory are possible. By using a 512bit bus with the higher clocks, the new standard can achieve the same higher bandwidth with much lower cost by not requiring a silicon interposer.

Figure 22. Samsung HBM3



Source: Samsung

Figure 23. HBM3

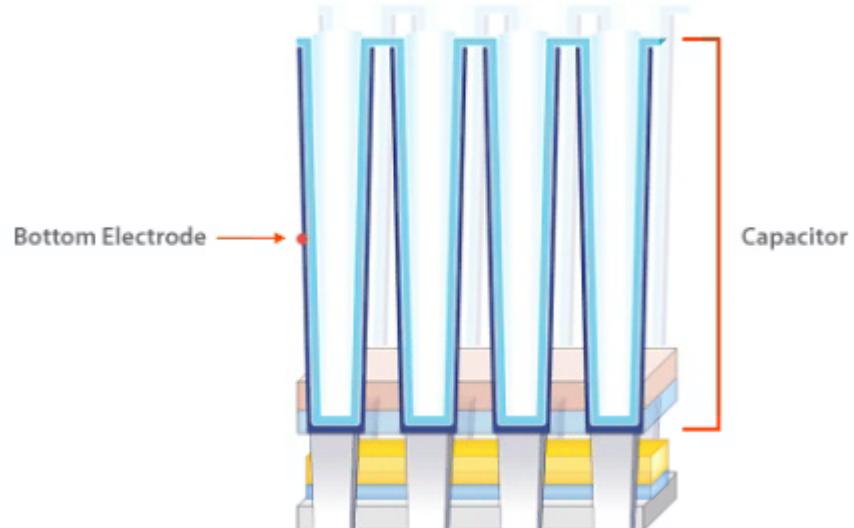


Source: Samsung

The second direction of DRAM innovation is in the materials, especially for materials used in the capacitor. With the aspect ratio nearing 100:1, DRAM producers need to consider either migrating capacitor architecture to double/triple stacking, thereby expanding the aspect ratio, or changing capacitor materials to High K material such as HfO₂ to improve capacitance.

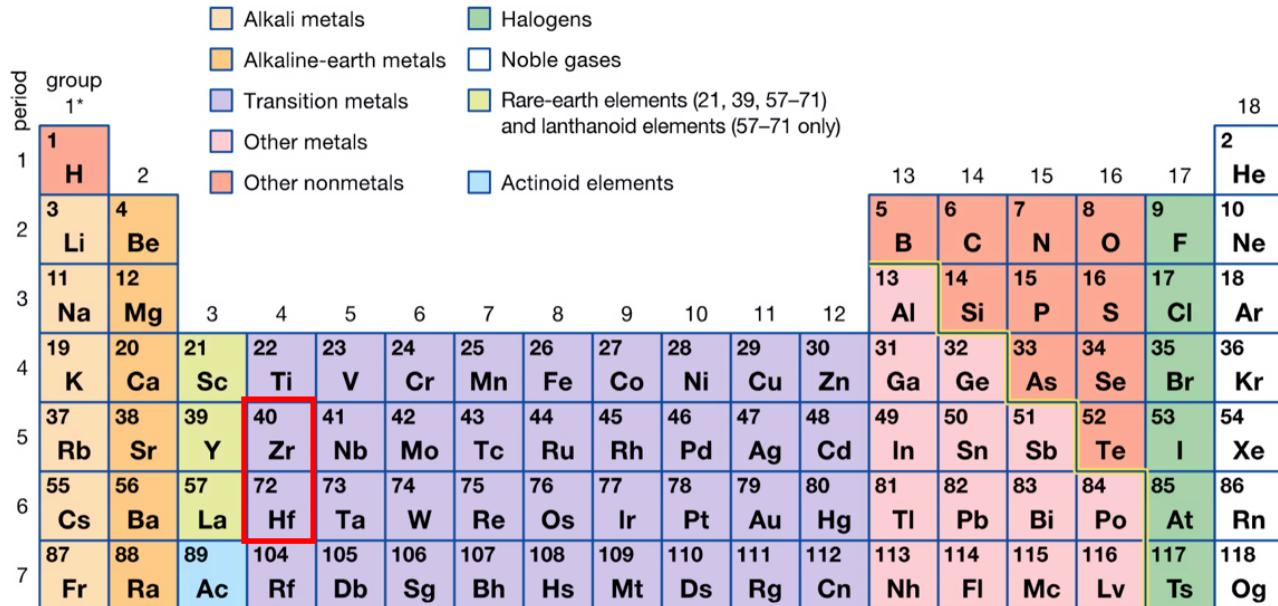
Current development efforts in materials is centered on replacing High K materials in capacitor from ZrO₂ to HfO₂ to increase permittivity. In addition, the method of double stacking capacitors is also being examined as a potential method to increase aspect ratio.

Figure 24. DRAM Electrode + DRAM Capacitor (High-K)



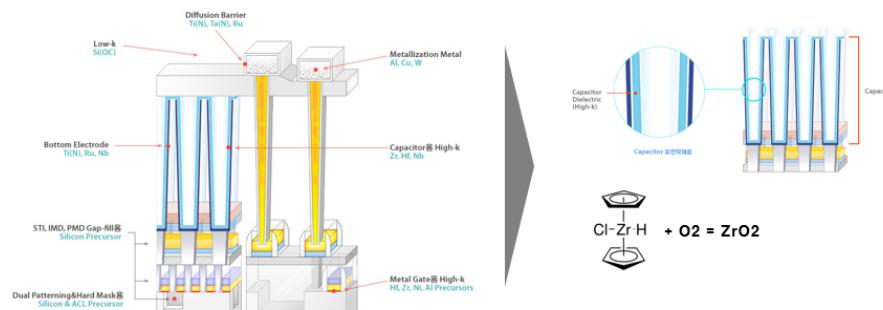
Source: Applied Materials

Figure 25. DRAM High-K Material change in DRAM Capacitor: Zr → Hf



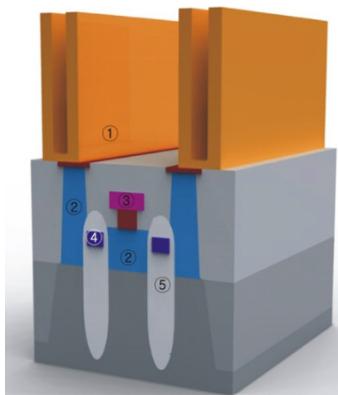
Source: Google search

Figure 26. DRAM Capacity with ALD Process and Precursor



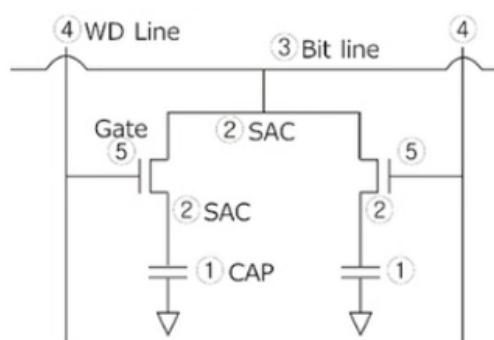
Source: DNF

Figure 27. DRAM Architecture Scheme



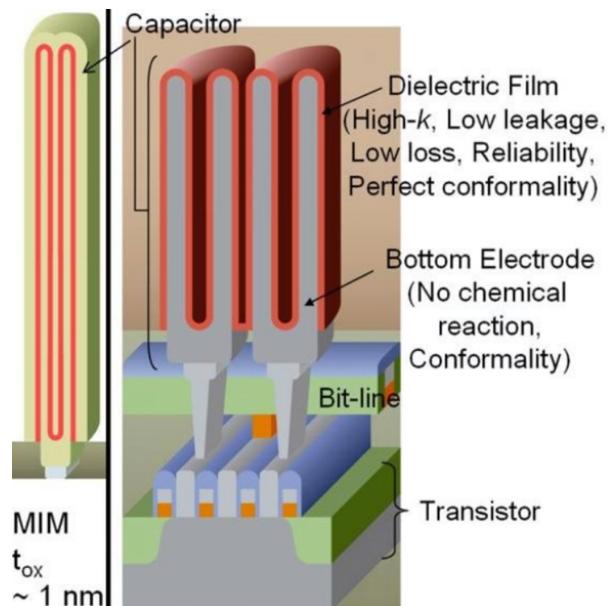
Source: Citi Research

Figure 28. DRAM Lay Out



Source: Citi Research

Figure 29. DRAM: Schematic Diagram of Stacked DRAM



Source: IMEC

We also expect changes in DRAM electrode materials. To improve conductivity for chips below 1nm, we foresee Nb-based or Ru-based materials to replace current Ti-based materials in precursor.

Figure 30. DRAM Electrode Material change : Ti → Nb / Ru

		Periodic Table of Elements																		
period	group	1*	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
1	1*	H																		He
2	3	Li	Be																	Ne
3	11	Mg																		Ar
4	19	K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr	
5	37	Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe	
6	55	Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn	
7	87	Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg	Cn	Nh	Fl	Mc	Lv	Ts	Og	
lanthanoid series		58	59	60	61	62	63	64	65	66	67	68	69	70	71					
actinoid series		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr					

Source: Google search

Figure 31. DRAM Electrode Materials

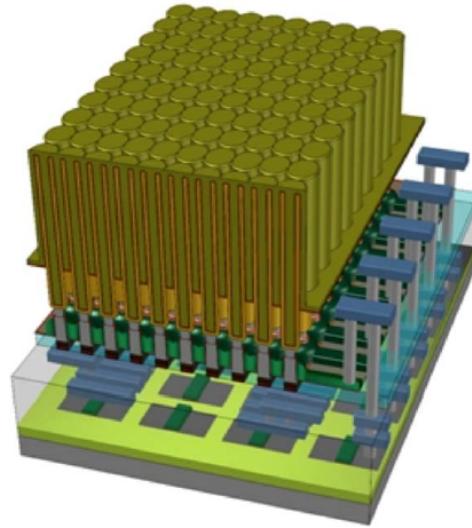
Product	Structure	Property
Ru(EtCp) ₂		Molecular Formula : C ₁₄ H ₁₈ Ru Molecular Weight : 287.37g/mol Melting Point : 6°C Vapor Pressure : 90°C/0.34torr Physical State/Color : Liquid (Yellow) Water Reactivity : React slowly
Ru-4		Molecular Formula : C ₁₆ H ₂₂ Ru Molecular Weight : 315.23g/mol Melting Point : - Vapor Pressure : 134°C/1.0torr Physical State/Color : Liquid (Yellow) Water Reactivity : React slowly
TDMATi		Molecular Formula : C ₆ H ₂₄ N ₄ Ti Molecular Weight : 224.18g/mol Boiling Point : 225°C Vapor Pressure : 25°C/0.1torr Physical State/Color : Liquid (Pale yellow) Water Reactivity : React Violently
TiCl ₄		Molecular Formula : TiCl ₄ Molecular Weight : 189.69g/mol Boiling Point : 136.4°C Melting Point : -24.1°C Vapor Pressure : 20°C/9.75torr Physical State/Color : Liquid (Colorless) Water Reactivity : React Violently

Source: DNF, Citi Research

The third and final direction we foresee in the 3D development process will be the transformation of chip architecture from 2D to 3D structure. Utilizing EUV, DRAM producers are expected to achieve node migration to 1nm, 1bnm and 1cnm, but from 1dnm, DRAM producers are highly likely to try altering DRAM chips' architecture to 3D structure to achieve further node migration, as NAND producers have done.

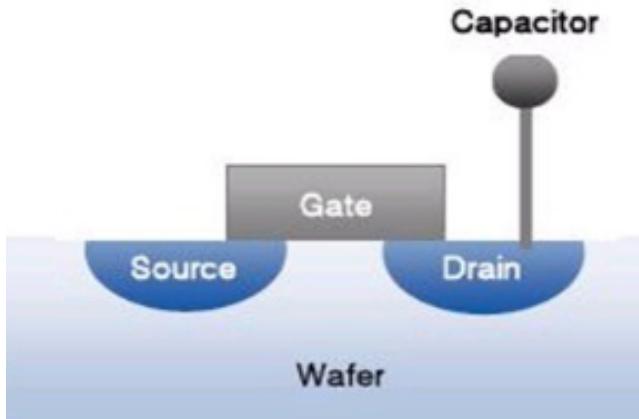
Transformation to 3D DRAM structure will progress in two key directions. The first direction will be the method of reducing chip size by placing Peri below Cell, similar to Cell on Peri method being adopted in 3D NAND architecture. While the method of stacking capacitor above transistor had been widely discussed as a potential alternative to Peri below Cell method, further development of the method has been halted due to excessive complexity of the structure.

Figure 32. 3D DRAM Direction 1: Peri Under Cell



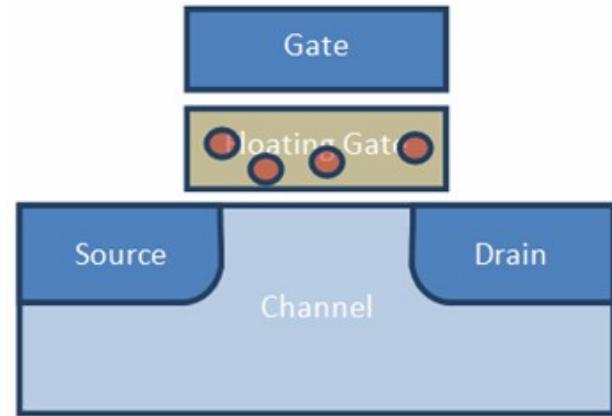
Source: Besang

Figure 33. DRAM Architecture: 1Tr +1Cap



Source: Citi Research

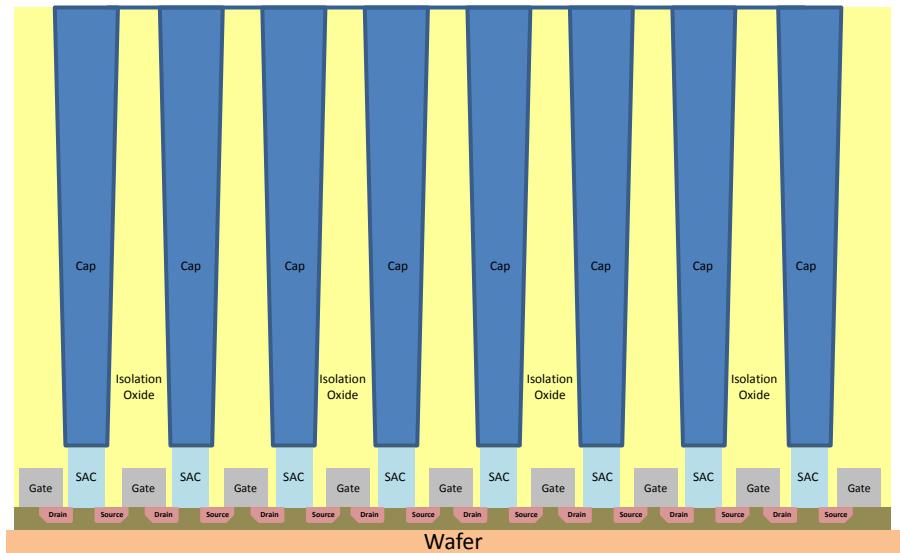
Figure 34. NAND Architecture: 1Tr(Control Gate + Floating Gate/CTF)



Source: Citi Research

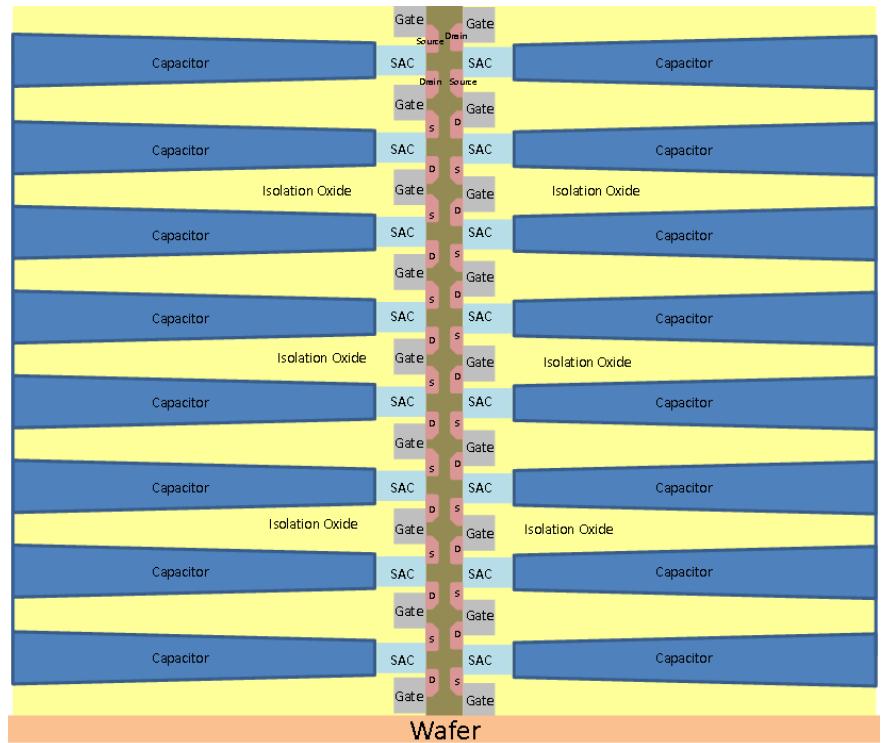
The second direction, which we anticipate to be a more realistic step to fully realize 3D DRAM structure, is rotating current DRAM architecture by 90° to achieve 3D DRAM structure, thereby creating a structure that highly resembles 3D NAND structure. The method does maintain current DRAM's 1Tr1Cap structure, but instead of positioning Caps vertically, it positions Caps laterally to enable stacking.

Figure 35. Current DRAM Scheme



Source: Citi Research

Figure 36. 3D DRAM Scheme

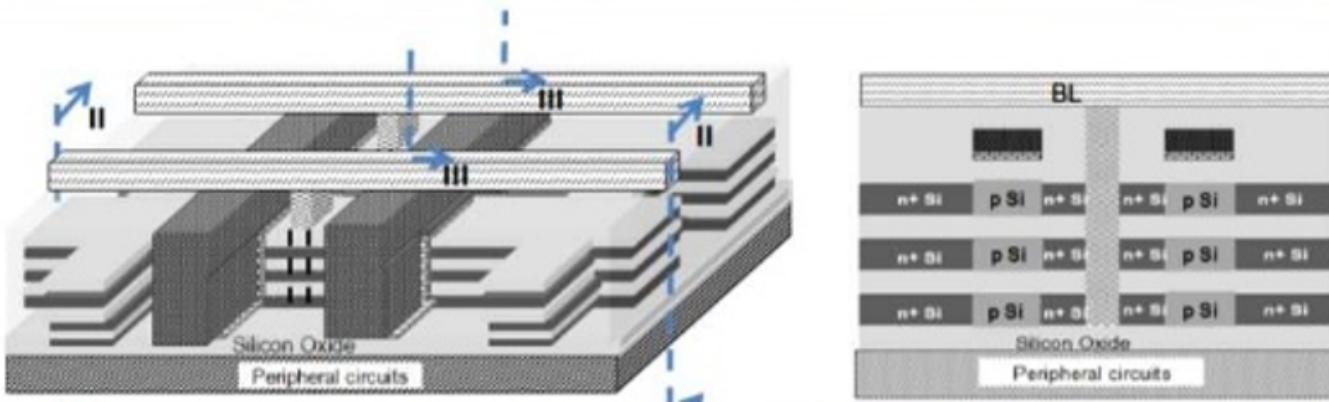


Source: Citi Research

The method stacks transistors vertically, as in GAA (Gate All Around), while repositioning capacitors laterally, thereby creating a structure that highly resembles 3D NAND structure.

3D DRAM is expected to resemble 3D NAND in the fabrication process also, adopting a process similar to 3D NAND ONO deposition structure. In the fabrication of 3D NAND, after repeated deposition of oxide and nitride, nitride is etched using H3Po4-based HSN (High Selectivity Nitride) etching solution, followed by deposition of tungsten in the space.

Figure 37. 3D DRAM Direction: Vertical Stacking



Source: Google Patent search

Figure 38. Semiconductor Material/Architecture Roadmap

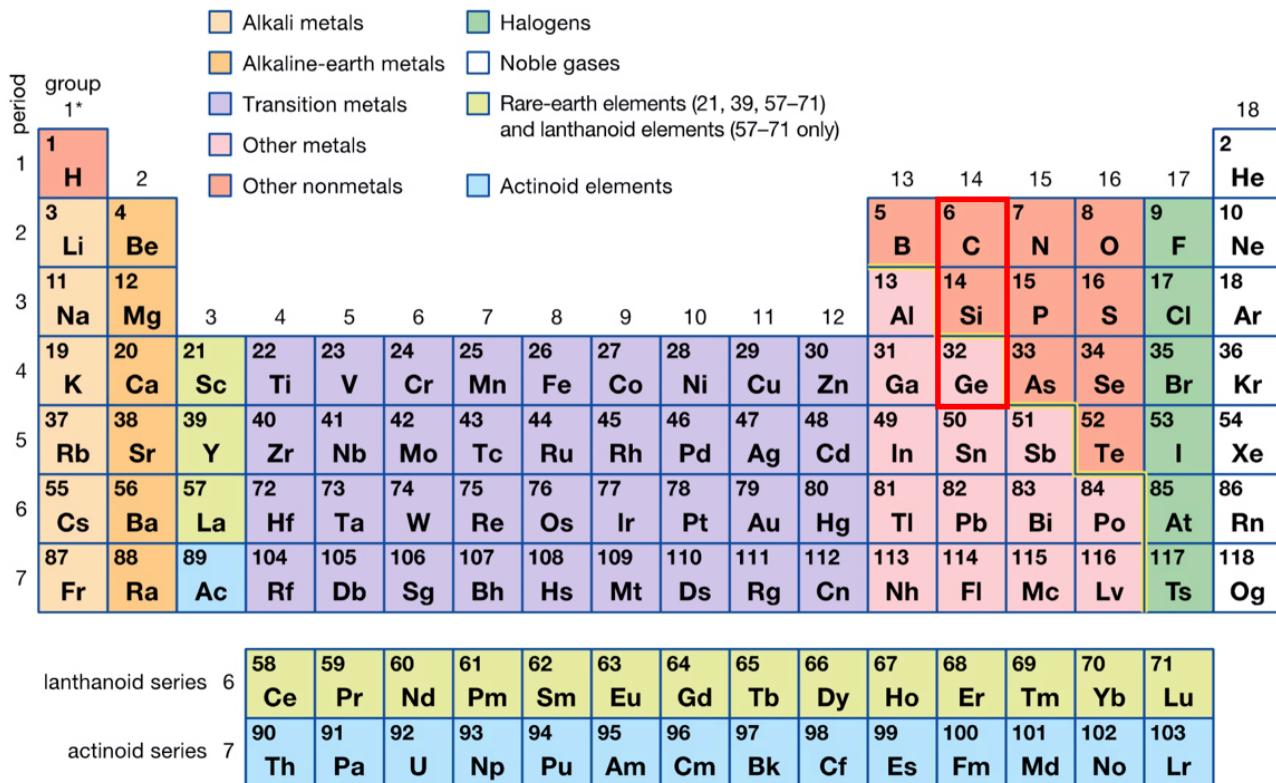
	Conventional stacked capacitor DRAM	Monolithic 3D DRAM with 4 memory layers
Cell size	$6F^2$	Since non self-aligned, $7.2F^2$
Density	x	3.3x
Number of litho steps	26 (with 3 stacked cap. masks)	~26 extra masks for memory layers, but no stacked cap. masks)

Source: Google Patent search

The structure of 3D DRAM is expected to be similar to that of 3D NAND in that it creates dummy layers first and then etches the dummy layers to create cells. However, in forming capacitors, 3D DRAM is expected to perform repeated oxide and SiGe depositions, rather than nitride deposition, and then use peroxide-type etchant for etching. Due to increased difficulties in the etching process, we expect 3D DRAM structure will begin to be adopted in earnest from nodes more advanced than 1dnm.

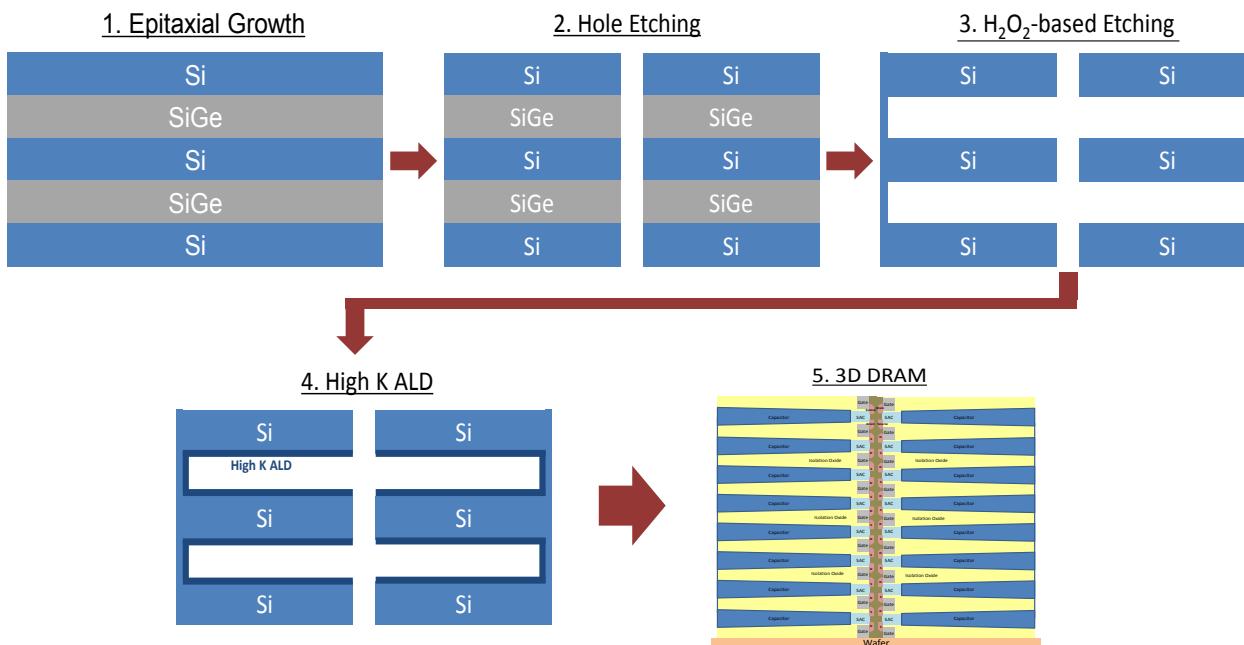
Key difference in the fabrication process of 3D DRAM from 3D NAND is that it goes through repeated epitaxial deposition of Si and SiGe. Although both Si and Ge are group 4 elements, Ge offers improved selectivity during etching process thanks to Ge's metalloid nature.

Figure 39. 3D DRAM Materials: Si vs. SiGe



Source: Google search

Figure 40. 3D DRAM Fabrication Process



Source: Citi Research

3D NAND: Multiple Stacking + Vertical Scaling + Cell on Peri

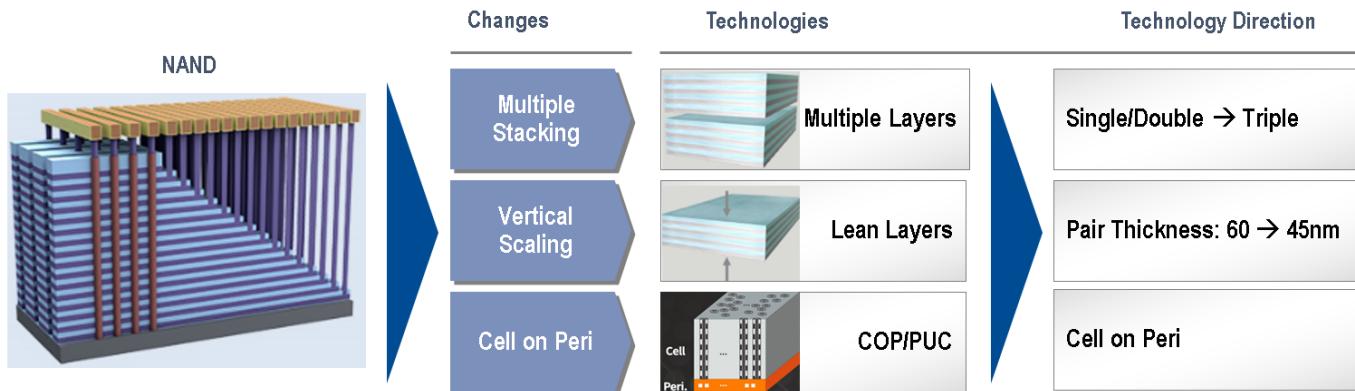
In NAND, we project facilitated adoption of 3D NAND structure. 3D NAND has witnessed continued increases in the number of layers; current 72~92 layers are expected to migrate to 128~176 layers in 2021E, and reach as high as 200 layers after 2021E.

The first direction in NAND technology we project is the increased adoption of multi stacking technology. Samsung Electronics, which has only relied on single stacking in the past, is expected to begin adopting double stacking from 176L, while other NAND producers are likely to adopt triple stacking amid continued competition to increase the number of layer stacking.

The second direction we foresee is vertical scaling. With the number of layers in 3D NAND exceeding 100, layers have begun to be affected by gravity. While 3D NAND was in the nano scale in the past, thereby immune to gravity, from 100L and onward, 3D NAND has entered micro scale and has begun to be impacted by gravity, which has forced producers to take gravity into consideration in the fabrication process. Mounting pressure on the lower layers of 3D NAND can result in collapse of the structure, which in turn can negatively impact NAND chips' characteristics and potentially deteriorate memory chips' quality.

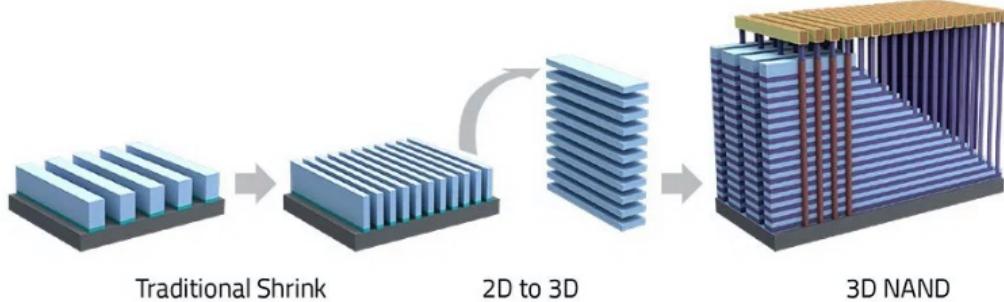
In addition, dry etching is used to etch a large number of holes in 3D NAND, but due to the increased depth of holes, it becomes increasingly more difficult to etch holes uniformly. As a result, we believe NAND producers will move towards the direction of reducing thickness of each layer in deposition process to lower the total height of the structure, and we project pair thickness to be reduced from 60nm to 45nm.

Figure 41. 3D NAND Direction: Multiple Stacking + Vertical Scaling + Cell on Peri



Source: Citi Research, Samsung Electronics

Figure 42. 3D NAND Concepts



Source: Samsung Electronics

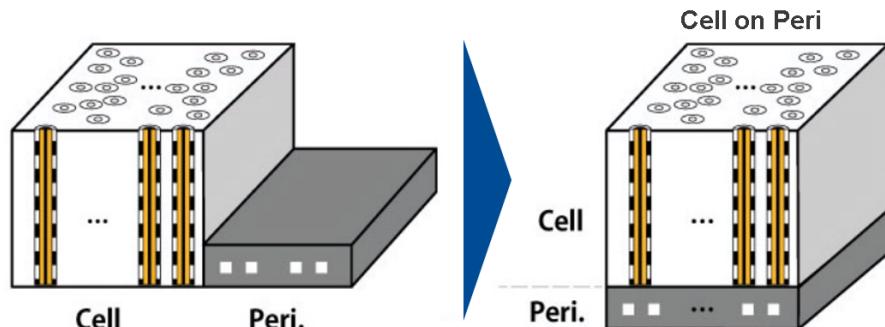
The third direction we anticipate is Cell on Peri (forming Peri first and then placing cell on top of Peri). Micron was the first producer to adopt the method, and we expect Samsung Electronics to follow Micron in adopting Cell on Peri technology from 176L. We project the adoption of the new technology will result in the reduction of the chip size by 20~30%.

Figure 43. 3D NAND Direction: Multiple Stacking



Source: Samsung Electronics

Figure 44. 3D NAND Direction: Cell on Peri

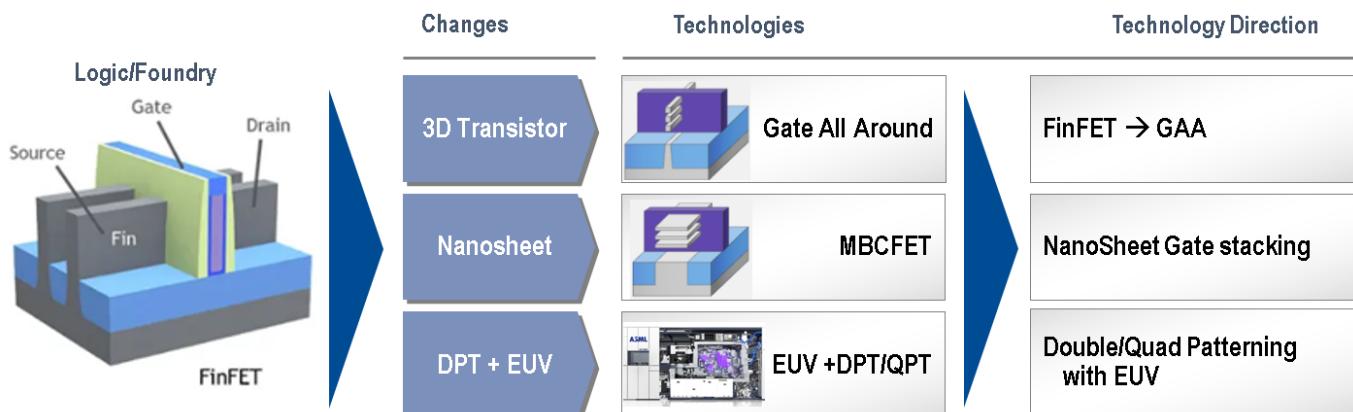


Source: Flash Memory Summit

3D Logic/Foundry: GAA + Nano Sheet + EUV

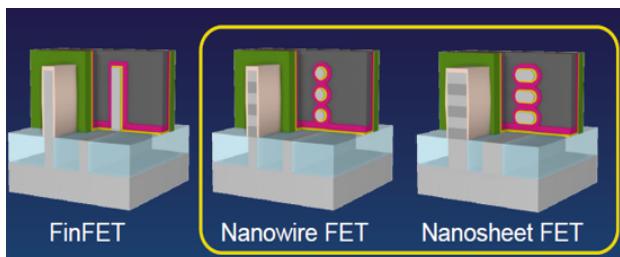
3D structure is being introduced rapidly in logic products as well. While the current FinFET technology, which uses EUV for 7nm and 5nm fabrication process, remains the mainstream 3D technology currently, we expect 3D structure will migrate to GAA (Gate All Around) technology in earnest from 3nm and onwards. In particular, Samsung Electronics has been preparing to launch MBCFET technology, which applies nano sheet technology on GAA structure, to advance its logic fabrication process.

Figure 45. Logic/Foundry Technology Direction: 3D transistor + Nano sheet + EUV with DPT



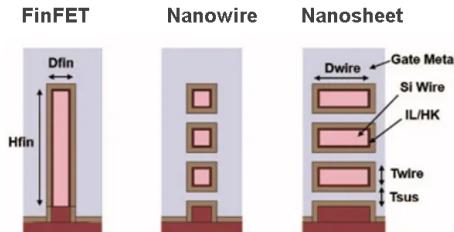
Source: Citi Research

Figure 46. 3D Logic/Foundry



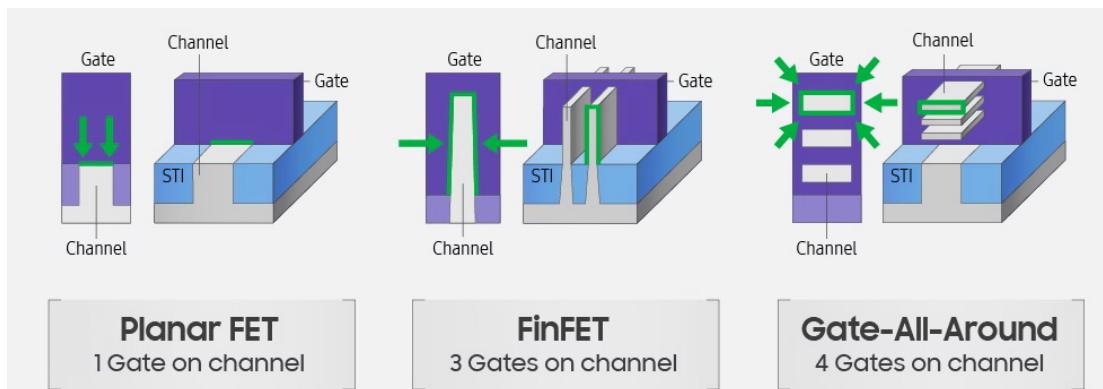
Source: Samsung

Figure 47. FinFET → Nanowire/Nanosheet



Source: Citi Research

Figure 48. Planar → FinFET → GAA



Source: Citi Research

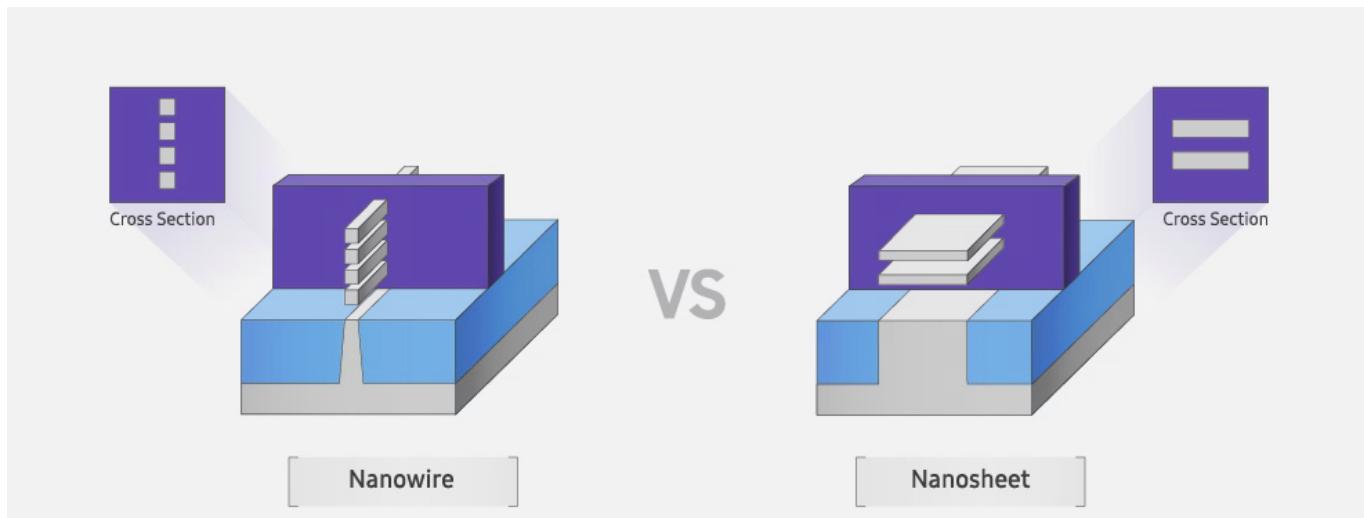
The structure of the transistor in Logic has evolved from planar to FinFET from 14nm, and the method of vertically stacking TR is expected to be adopted in earnest from 3nm. The vertical stacking technology is expected to be broadly similar to 3D NAND, but for logic, we expect 1) sequential deposition of Si and SiGe, and 2) GAA structure formation through epitaxial growth process, to distinguish the logic structure from 3D NAND structure.

To compare the fabrication process of nano sheet FET with GAA, while nano sheet FET removes dummy gate as FinFET does, nano sheet FET goes through additional steps to remove SiGe through dry chemical etch, followed by oxidation for rounding and oxide removal process. The last process of High-K dielectric and metal deposition process is common in both.

A typical GAA transistor takes the form of a thin and long nanowire. However, a channel needs to be as wide as possible in order to allow a large amount of current to flow through it, and the small diameter of the nanowire makes obtaining this higher current flow difficult.

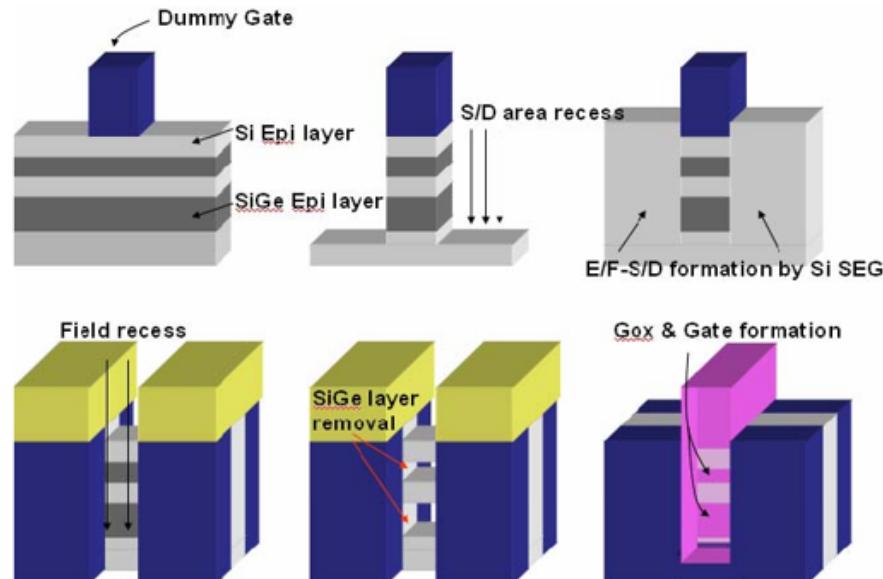
To overcome this, Samsung developed and patented its proprietary MBCFET™ (Multi-Bridge Channel Field Effect Transistor), an optimized version of the GAA transistor. Samsung announced its 3nm process a GAAFET device in 2020. The disclosure feels a little early but Samsung feels very confident that it has a highly-manufacturable disruptive technology planned for its 3 nm and it wants people to be aware of it well in advance.

Figure 49. FinFET Process vs. Nanowire/Nanosheet FET Process



Source: Samsung Electronics

Figure 50. MBCFET Fabrication Process

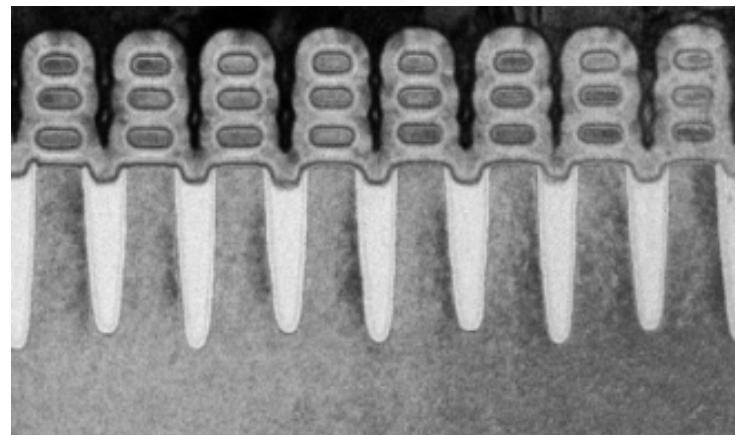


Source: Samsung

The MBCFET increases the areas that make contact with gates by aligning wire-formed channel structures as a 2-dimensional nanosheets, which enables simpler device integration as well as increasing the electric current. Samsung's MBCFET™ is a competitive transistor structure in that it not only includes the means to mitigate the short-channel effect thanks to the GAA structure, but it also increases performance by expanding the channel area.

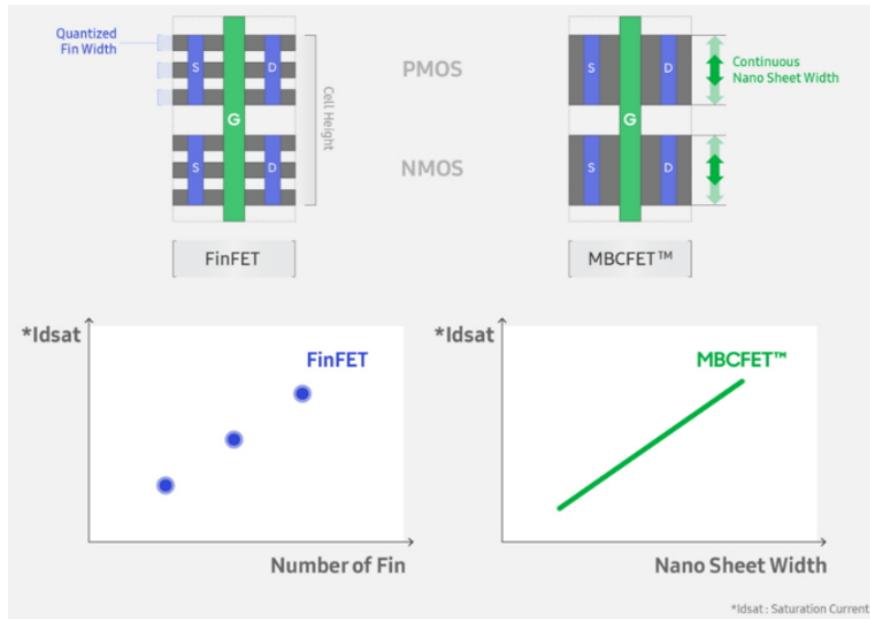
Compared with the existing 7-nanometer fin transistor process technology, the MBCFET decreases power consumption by 50%, improves performance by 30%, and reduces the area that the transistor takes up by 45%.

Figure 51. MBCFET



Source: Samsung

Figure 52. MBCFET



Source: Samsung

Figure 53. 2021/2022 Processes

	Intel	Samsung	TSMC
Process	7nm	3DDAE	3FF
Device type	FinFET	HNS	FinFET
M2P	26nm	32nm	22nm
Tracks	6.00	6.00	5.00
Cell Height	156nm	192nm	110nm
CPP	47nm	40nm [1]	45nm
SDB/DDB	SDB	SDB	SDB
Transistor density (MTx/mm ²)	212.48	202.85	314.73

Source: Citi Research

Market Impacts from 3D Architecture

We expect the adoption of 3D structure to have material impacts in the semiconductor market. In memory, we anticipate increased adoption of 3D DRAM and 3D NAND will lead to more complex fabrication process. We expect Samsung to lead 3D DRAM and 3D NAND development with architecture innovation and material changes. Additionally, increased technology complexity in memory fabrication will limit the memory supply growth in the long term, which will be positive for long-term memory pricing.

In logic/foundry, we believe the shift in transistors' architecture from planar to FinFET, and then to GAA and nano sheet after 3nm will widen the technology gap between the industry's leaders and followers. In addition, we anticipate the introduction of EUV-based technologies will strengthen incumbent market leaders' technology/production edge and facilitate further consolidation of semiconductor market.

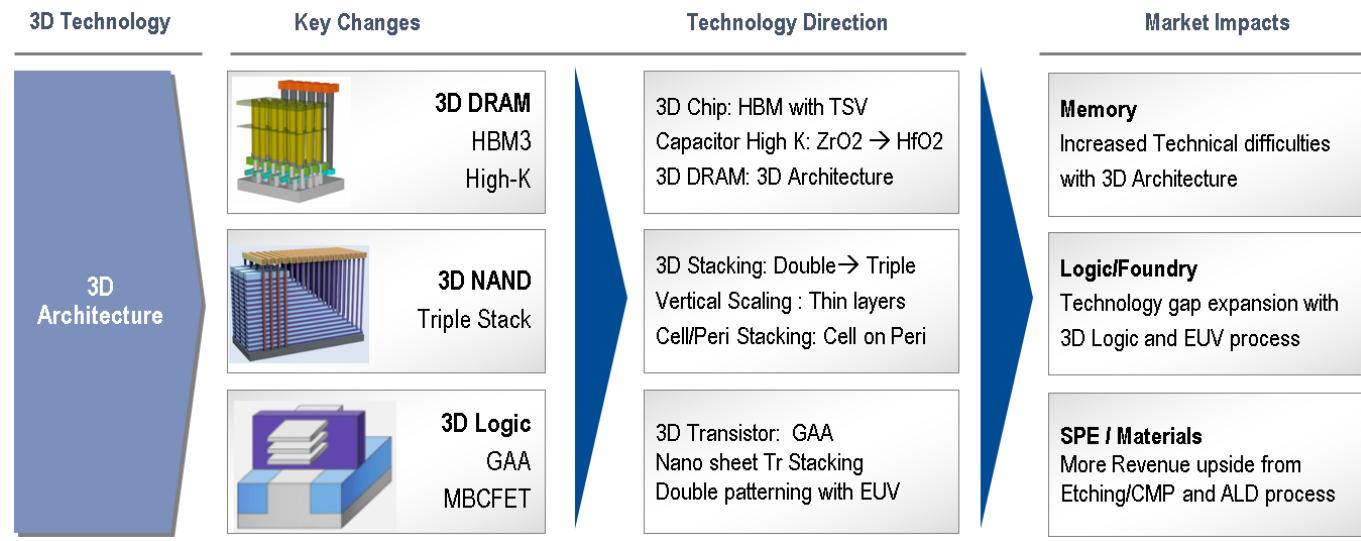
Positive on Samsung, TSMC and Sony

We believe the shift towards 3D structure will benefit incumbent technology leaders in the semiconductor market. We are positive on Samsung and TSMC as we see them leading 3D architecture technology with EUV. Both Samsung and TSMC will adopt 3D architecture with Gate All Around. In addition, we are positive on Sony as it will lead CMOS image sensor technology with 3D stacking technology revolutionized image sensors.

In addition, we project the shift in semiconductor technologies to result in industry-wide changes to the SPE and materials businesses in the semiconductor value chains. In particular, we anticipate wider adoption of 3D structure will lead to increased demand in etching, CMP, and ALD equipment. Among SPE/material global plays, we are positive on LAM Research (CVD/Etch), TEL (CVD/Etch), Entegris (Chemicals) and ASM Pacific (Package).

Related Korea SPE plays include Wonik IPS (CVD/ALD), Eugene Tech(CVD/ALD) and TES (CVD). Related Korea Material names are SK Materials (CVD gas/Precursor), KC Tech (CMP/CMP Slurries), Soulbrain (Etchant), and Hansol Chemical (H2O2).

Figure 54. Market Impacts from 3D Architecture



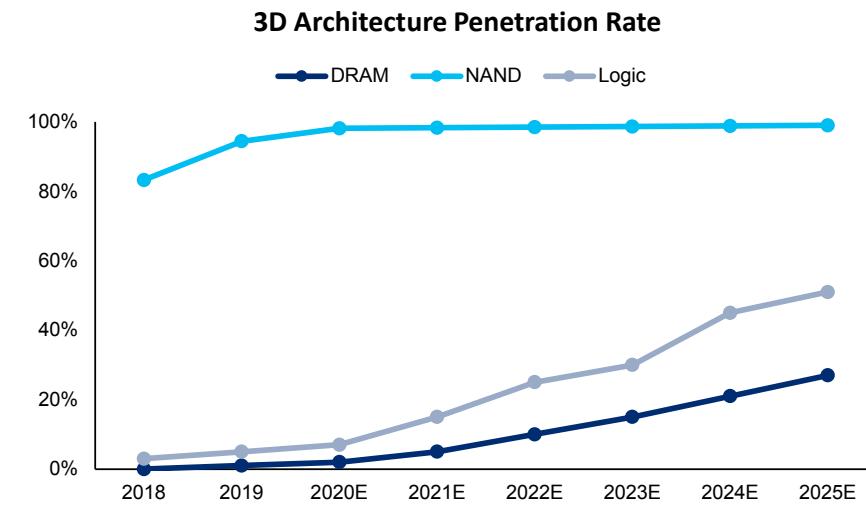
Source: Citi Research

Market Impact 1: Memory → Increased Technical difficulties with 3D Architecture

Market Impact 1: Memory → Increased Technical difficulties with 3D Architecture

Wider adoption of 3D structure in memory chips will lead to increased technical complexity in the memory chips' fabrication process. In DRAM, the technological development is expected to take place in the order of HBM, semiconductor material and 3D DRAM architecture. We anticipate increased difficulties in the fabrication process will strengthen incumbent market leaders' technological barrier and consolidate their leading positions.

Figure 55. 3D Architecture Penetration Rate by Semiconductor Product



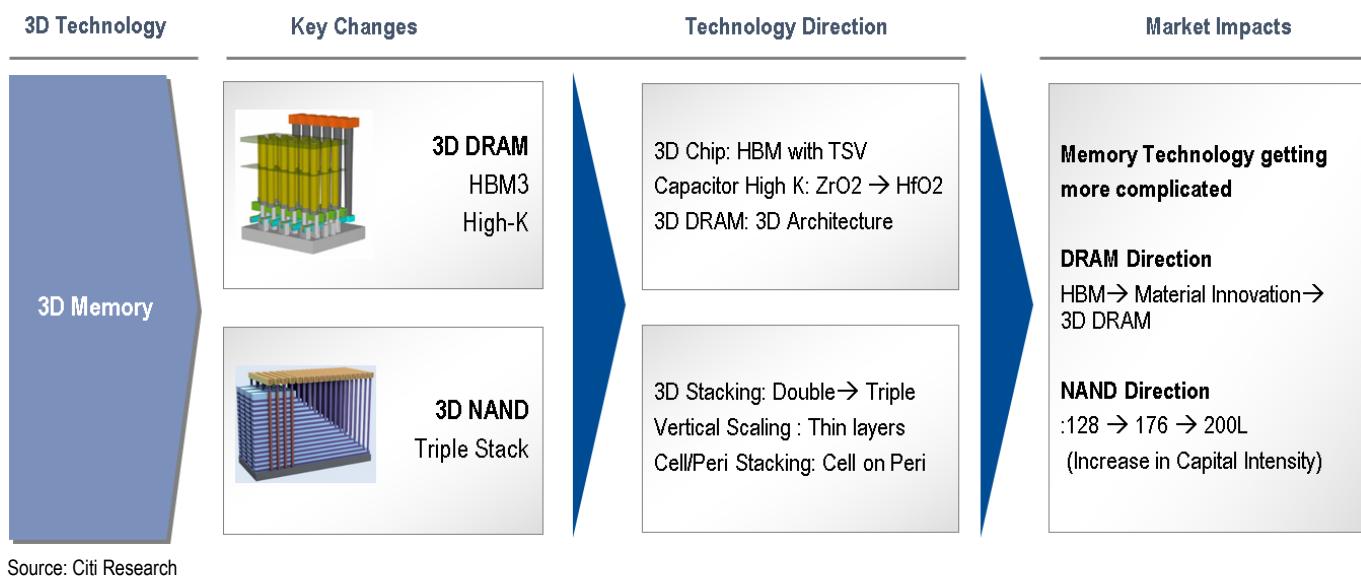
Source: Citi Research

Samsung to lead 3D Memory Architecture

In NAND, we expect competition among chip producers to intensify as the major producers, including Samsung Electronics, utilize double/triple stacking technologies and gradually adopt COP (Cell on Peri) technology. We foresee Samsung Electronics responding to the challengers by rapidly adding capacity, which is likely to result in oversupply conditions in the NAND industry.

We expect Samsung to lead 3D DRAM and 3D NAND with architecture innovation and material changes. In addition, increased technology complexity in memory fabrication would limit memory supply in the long term, which would be positive for memory pricing in the future.

Figure 56. Market Impacts from Memory



Source: Citi Research

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Samsung Electronics

Samsung Electronics is expected to begin the 3D DRAM chipset business using TSV technology from 2021E, after the company launches HBM2E and HBM3 products.

In semiconductor materials, Samsung Electronics is expected to utilize High-K materials, such as with HfO₂, to improve the quality of capacitors to facilitate node migration beyond 1znm. After 1dnm, the company is projected to consider developing 3D DRAM chips whose structures resemble 3D NAND.

In particular, we believe Samsung will sustain semiconductor technology leadership with EUV technology for DRAM. Samsung will adopt EUV in DRAM earlier than other DRAM makers, which would be positive for Samsung's DRAM cost structure and quality improvement for new DRAM Products (DDR5, GDDR6 and LPDDR5). And lastly, we expect other DRAM makers to research and develop EUV for 1znm or 1ann process and that EUV will become a big swing factor for technology migration after 2020.

In NAND, Samsung Electronics will move on to 176L products from 128L products, which is when the company is expected to begin producing chips using double-stacking technology and COP technology. We believe Samsung Electronics, already equipped with 200L technology in our view, will continue to sustain its technology leadership with continued development efforts and cost competitiveness.

Micron

While Micron has not publicly commented on 3D DRAM, we expect the company to deploy 3D DRAM roughly a year behind Samsung, similar to its timing of technology migration for 3D NAND. We would note Micron has already rolled out 3D NAND and its own 3D Xpoint memory architecture in tandem with Intel, so we have confidence the company can successfully develop their own 3D DRAM manufacturing.

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We also expect 3D DRAM to drive higher capital expenditures given the increased cost associated with the migration. We currently project Micron capex to sales at 25-27% over the long term and believe this could temporarily rise above 30% with the implementation of 3D DRAM.

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Western Digital

Western Digital remains enthusiastic on BiCS5 node (announced in January 2020); though a deliberate and steady ramp won't make BiCS5 a dominant node at the company until toward the end of CY21.

For now, BiCS5 still remains at a low percentage of its total, and is shipping largely into retail currently. As of September, the company produced just over 60% of BiCS on BiCS4 (96-layer). Overall, management cites multiple quarters of the usual 15% year-over-year cost declines, with the ability to continue such savings while shifting to BiCS5. The BiCS5 with 112 layers compares to 96 layers for BiCS4, and Western Digital management notes it chose BiCS5 112 layers versus 128 layers as the most capital-efficient way of achieving its long-term cost reduction goals.

At the time of the announcement, despite the seemingly low approximately 16% increase in layers from 96 to 112, trade reports pointed to density increases of up to 40% by bits per wafer, including additional design changes which compress horizontal dimensions, combined with memory interface speed increases of 50%, compared to 96 layer competitors. Additionally, reports indicate Western Digital designed its BiCS5 transition for lower capex requirements vs the prior 64 layer to 96 layer transition, resulting in an expected slower transition as mentioned in the timeline above.

When we hosted Western Digital at our September 2020 Technology Conference (virtual), management indicated the company had already been converting a lot of equipment and were able to do so quite efficiently, with good cost benefit and good capital benefit expected moving to BiCS5 through at least first half of CY21, after which we should start seeing more BiCS5.

Looking further out, the company doesn't see a limit to the number of layers achievable for the next five years or so. Moreover, beyond layers, overall bit growth and cost reductions are thought to be achievable through scaling its cell array densities though improved engineering processes and other lateral improvements – the roadmap of which is expected to project the company's scaling confidence forward for the next 5-7 years.

Given current demand and its product roadmap, Western Digital continues to see the importance of investing in Fab 7, whose construction is expected to commence in the spring of 2021. Importantly, compared to Kitakami, Japan (K1 project), Fab7 is only considered an expansion of an existing site – thus a less costly project. With construction slated for Spring 2021, the company doesn't expect it to then come online until after spring 2022, and it should still be a while before spending details are eventually figured, as plan details are still forthcoming.

However, costwise, since it's an additional fab on an existing major site, it should not be nearly the incremental cost as seen for K1. Recent management commentary indicates the storage market still requires sufficient ongoing investment to keep pace with the expected 30% demand increase in bit supply, though with a keen eye on oversupply. As recently as its September quarter earnings call, Western Digital management cited that on the demand side, multiple demand segments are seen to be ramping up, including gaming (which was 10% of Sept

quarter business), the 5G ramp is beginning, and demand commentary from cloud customers heading into 2021 bodes positively for Western Digital.

Market Impact 2: Logic/Foundry → Technology gap expansion with 3D Logic and EUV

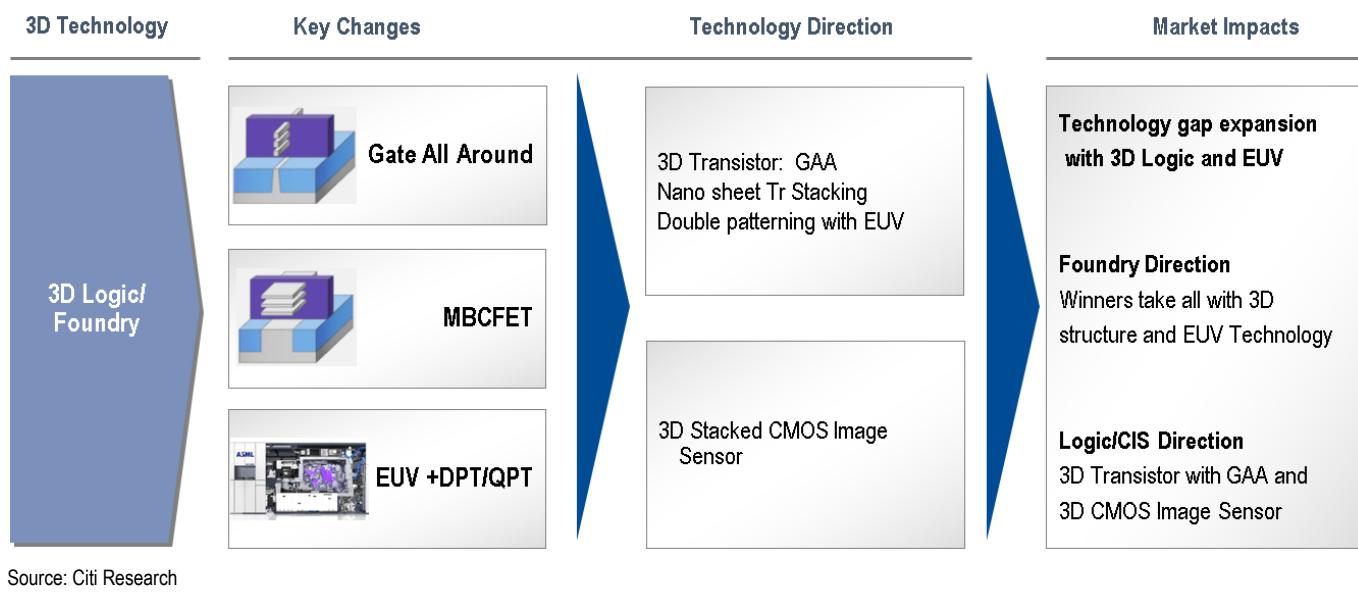
Market Impact 2: Logic/Foundry → Technology gap expansion with 3D Logic and EUV

In logic and foundry, the technology is expected to migrate from FinFET to GAA and nano sheet, a shift which we believe is likely to produce a winner-takes-all situation in logic/foundry space. In particular, the technology gap between companies equipped with EUV and 3D structure technology and companies that lack these technologies will widen further, consolidating technology leaders' position in the market.

Positive for Samsung, TSMC and Sony

We are positive on Samsung and TSMC as we see Samsung and TSMC will lead 3D architecture technology with EUV. Both Samsung and TSMC will adopt 3D architecture with Gate All Around. In addition, we are positive on Sony as Sony will lead CMOS image sensor technology with 3D stacking technology revolutionized image sensors.

Figure 57. Market Impacts from Logic/Foundry



Source: Citi Research

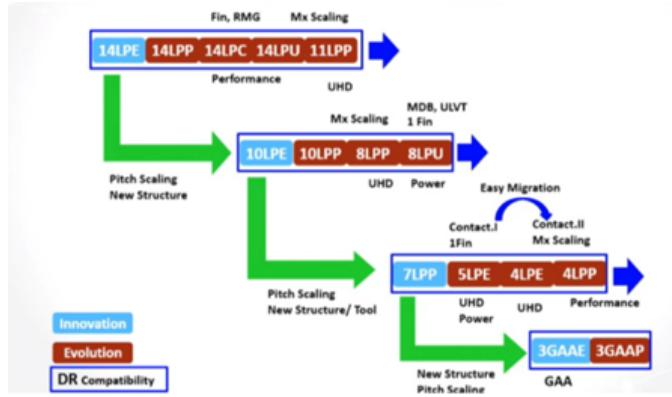
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Samsung Electronics

We expect Samsung to lead 3D Architecture with 3D nano sheet technology (MBCFET) with EUV process. Samsung held an investors forum virtually on November 30 2020, and emphasized its semiconductor technology leadership, highlighting EUV and 3D architecture technology for Foundry.

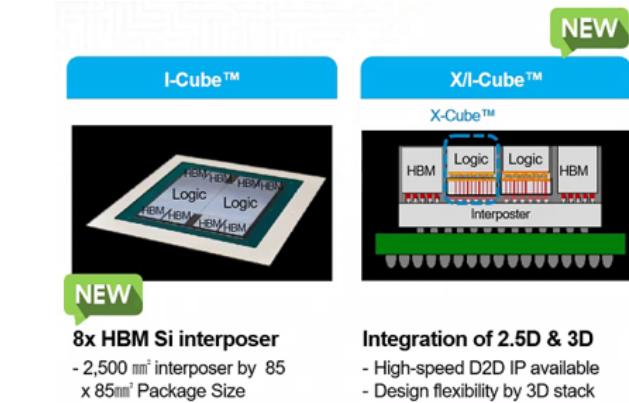
Samsung detailed its foundry growth strategy with its EUV ecosystem, 3D nano-sheet technology (MBCFET), and new packaging solutions (X/I Cube), for 3nm production. At System LSI session, Samsung showcased its 3D CIS technology with high-resolution ISOCELL and shared its plan to launch global shutter sensor products for automotive applications.

Figure 58. Samsung Foundry Tech Roadmaps



Source: Samsung Electronics

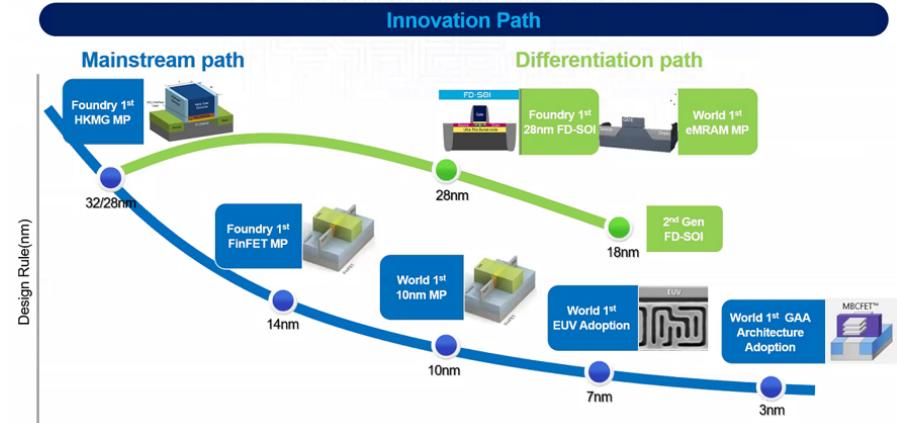
Figure 59. Samsung 3D Packaging



Source: Samsung Electronics

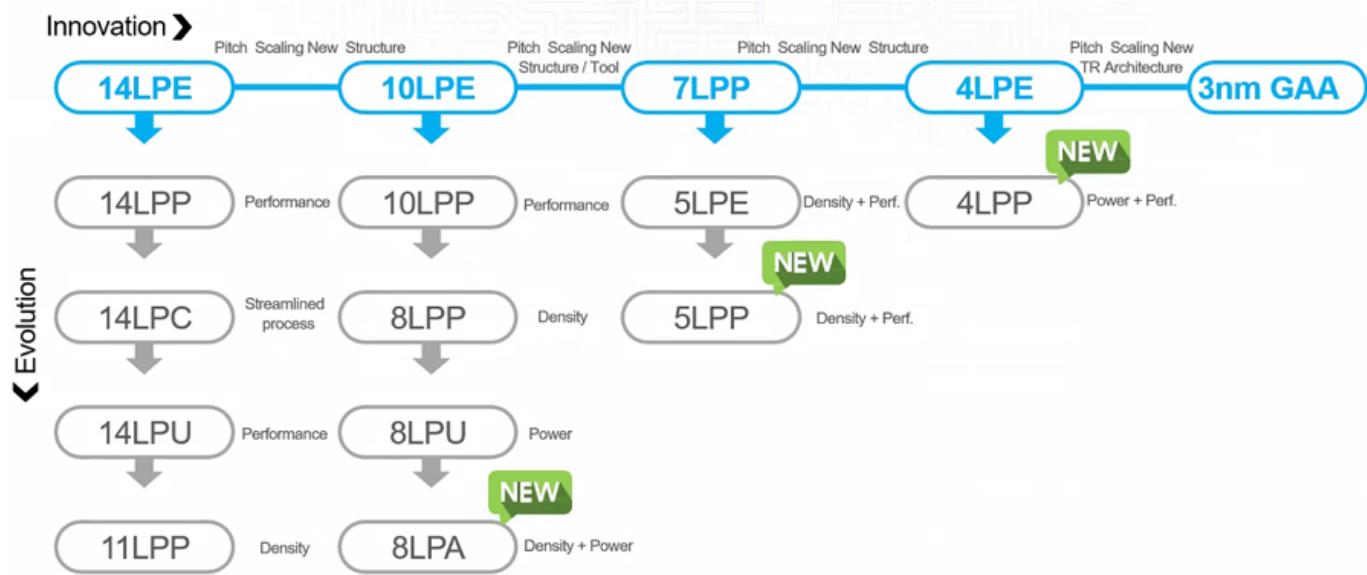
SEC will adopt 5LPE with 5nm, which will be easy migration from 7LPP. 5LPE will provide optimal performance and power by MDB (Mixed Diffusion Brake) and 1-Fin devices. For 4LPE/4LPP, SEC adopts extreme scaling MOL and BEOL with flexible gate contact placement.

Figure 60. Samsung Foundry Technology Direction: 3D Architecture with GAA



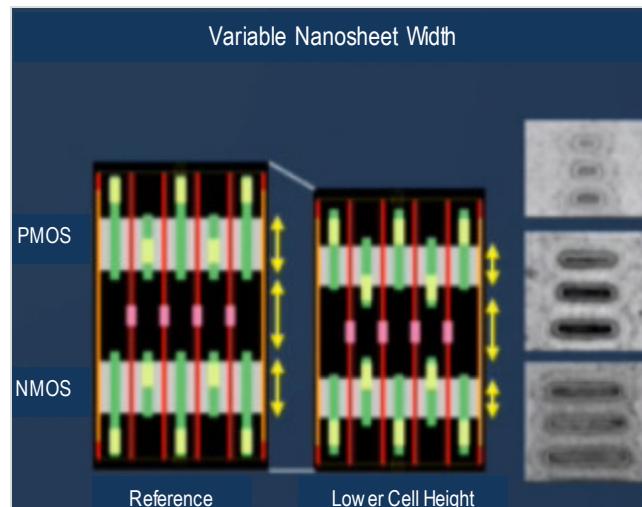
Source: Samsung Electronics, Citi Research

Figure 61. Samsung Foundry Technology Roadmap: Innovation and Evolution



Source: Samsung Electronics

Figure 62. 3nm: MBCFET the Most Realistic GAA Structure



Source: Samsung Electronics Investors Forum 2018

For the below 3nm, SEC will adopt 3D architecture with MBCEFET (Multi-Bridge Channel FET). With a FinFET compatible process, SEC will have better design flexibility through planner like variable Nano sheet width. Its 3D Architecture(GAA technology) will combine 3D NAND stacking technology from Memory process, so we expect SEC to utilize proven 3D stacking technology such as 3D NAND CVD (Chemical Vapor Deposition), Etch and ALD (Atomic Layer Deposition) process.

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TSMC: Working on Nano sheet for 2nm

TSMC migrated to FINFET from planar gate technologies since 16nm in 2015. It announced that its 3nm technology will still stay with the 6th generation of FINFET and is on track to mass production from 2H22. TSMC is working closely with key customers for the 3nm process qualifications and is building 3nm capacity for production in advance.

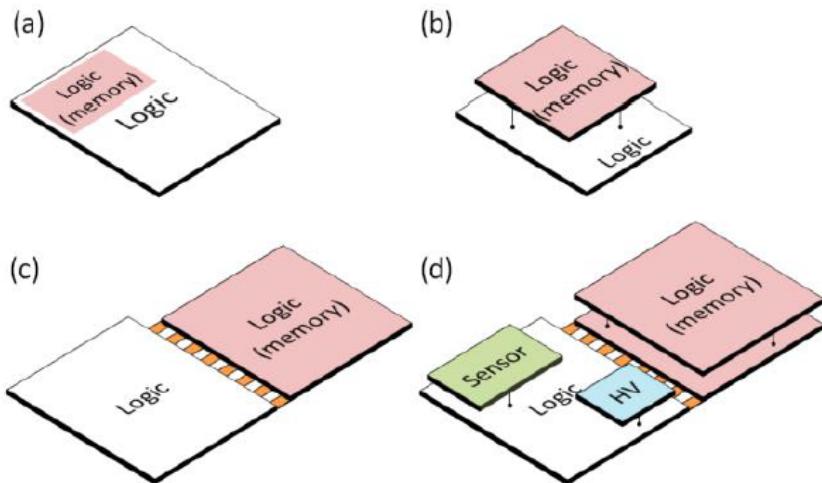
The FINFET technology and ecosystem are sophisticated and have matured after the industry's years of experience, especially for TSMC. TSMC has shipped billions of units of application processors sporting smartphones, tablets, GPUs, CPUs and other advanced applications using FINFET technologies for years. The extension of FINFET to 3nm ensures the smooth technology and production ramp at TSMC.

TSMC, however, decided to migrate to Nano sheet gate all around (GAA) technologies from 2nm. The nano sheet GAA is expected to offer a faster responding speed, less leakage and a relaxed gate pitch to the manufacturers to enhance the manufacturability of EUV and other technologies for making <3nm nodes of products.

Nevertheless, most of the GAA technologies include the SiGe etch, ALD deposition and metal gate deposition in the nano sheet are more arts than sciences from the time being. It's really at the premature stage for GAA adoptions for all of the players in the market. The learning curve for GAA ecosystem to be ready will be long from now. TSMC's 3nm FINFET technology will be the overwhelming technology in the market before the GAA ecosystem is ready by 2023 or later.

3D Fabric – integrated package solutions for novel heterogeneous IC manufacturing and integration

Figure 63. There are various methods to integrate chiplets with SoIC technology



Source: TSMC, Citi Research

* (a) SoC Before chip partition; (b), (c), (d) Variant partitioned chiplets and re-integrated schemes enabled by SoIC

TSMC's 3D Fabric technologies include InFO, COWOS and SoIC. The InFO has been mass produced for Apple's A-series application processors since 2016. InFO's productivity and effectiveness have been well proven by more than a billion units of A-series application processors for iPhones and iPads in the market. The COWOS technology, which was developed earlier than InFO, is mostly used for packaging for the high performance ICs such as FPGAs and GPUs. The networking ASICs,

which need the high computing power, have also adopted the COWOS packaging. The existing bumping, InFO and COWOS package/testing are expected to contribute >US\$3bn revenue to TSMC in 2020.

Besides InFO and COWOS, TSMC is working on a hybrid bonding to vertically connect different chips. The diffusion bonding between silicon oxides, the dielectric layer in a chip to separate/isolate the metal lines, or the direct copper pillar to copper pillar bonding are developed. The diffusion bonding between silicon oxide layers is entirely different from the conventional package die bonding technologies. It's a direct bonding under a specific ambient through the dangling OH (oxy-hydrogen) bonds on top of the silicon oxide surface.

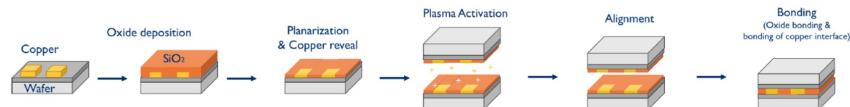
There are more chemical reactions between the bonding surfaces than the conventional mechanical bonding by the intermediate materials such as silver paste. TSVs are made in the bonded chips to make the metal interconnection among the chips.

A copper pillar to copper pillar direct bonding (copper to copper) is also being developed by TSMC. The chips are placed face to face through the high precision pick-and-place robot. The copper pillar direct bond eliminates the usage of TSV. It saves costs during manufacturing, enhances the performance by thinning down the overall thickness of the stacked dies.

Figure 64. Hybrid bonding can effectively save costs and enhance performance

Hybrid Bonding (Fusion Bonding, Cu-Cu Bonding, Monolithic Bonding)

Approach 1

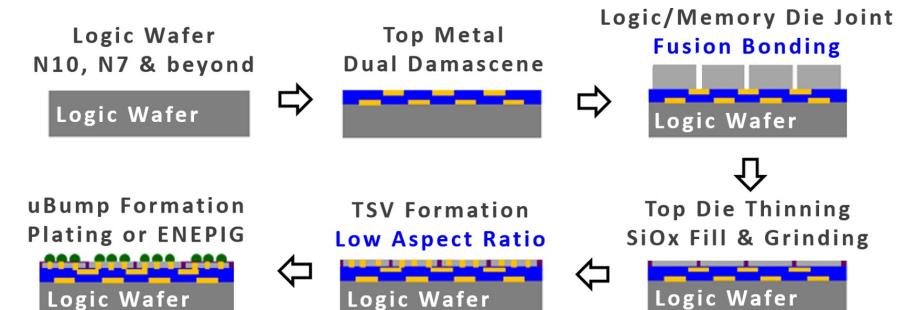


Approach 2



Source: Yole Development, Citi Research

Figure 65. SoIC manufacturing process

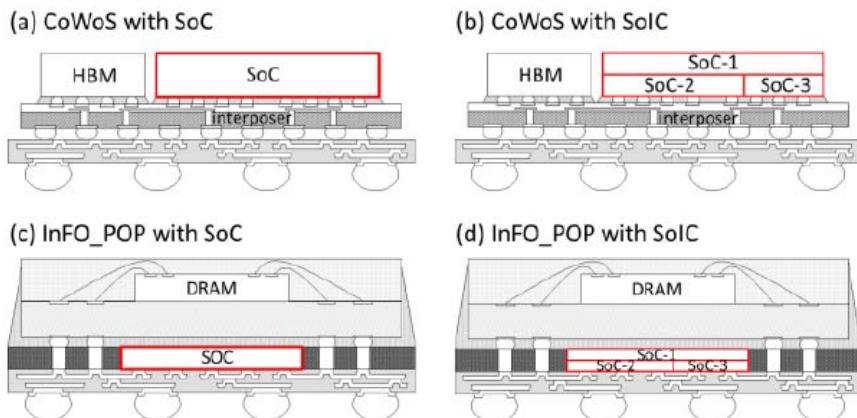


Source: Yole Development, Citi Research

Together with TSMC's COWOS and InFO package solutions, the fusion bonding and copper pillar direct bonding technologies enable TSMC to integrate different chips in a substrate. TSMC owns the advantages to engage with customer's designs before the chips are made. TSMC can also alter the I/O design to better fit with the subsequent 3D IC package flows.

Being a major foundry partner for the most leading edge technology manufacturing and the advanced package service providers in the industry, TSMC is the best candidate to offer a one stop shopping solution to achieve leading edge foundry manufacturing together with 3D integration through package to move the Moore's law further by achieving an acceptable cost for most of the customers.

Figure 66. TSMC's SoIC solutions vs SoC previously



Source: TSMC, Citi Research

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3D stacking technology revolutionized image sensors

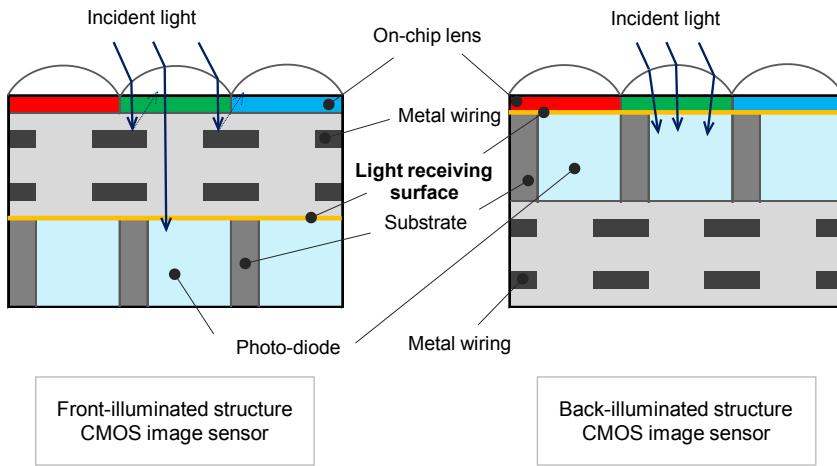
Sony

Sony has 3D CMOS image sensors and uses TSV- and Cu-Cu-interconnect 3D stacking technology. The introduction of 3D stacking technology in 2012 and Cu-Cu interconnect in 2015 has enabled Sony to reduce the CMOS image sensor package area, lower overall production costs, and improve light capture.

Sony's image sensors were mainly CCD until the 2000s. The company launched its first CMOS image sensor, the IMX001, in 2000, and went on to build CMOS into a larger business than CCD. A CMOS image sensor incorporating a column AD converter was developed in 2007, and in 2009 Sony launched a back-illuminated CMOS image sensor.

Development of a 3D stacked CMOS image sensor followed in 2012. The first products used TSV chip interconnection. Then in 2015 Sony developed a stacked CMOS image sensor using Cu-Cu interconnect technology.

Figure 67. Image sensor structure (LHS: Front illuminated, RHS: Back illuminated)



Source: Company data, Citi Research

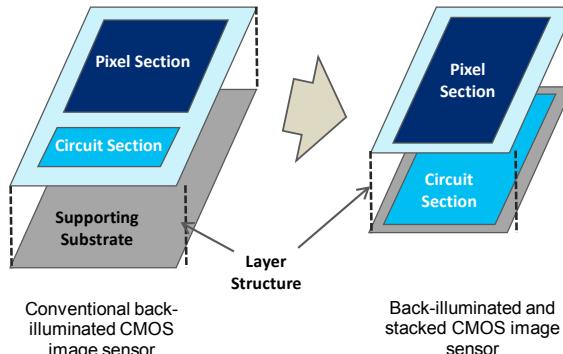
A key feature of Sony's CMOS image sensor development history is that each new technology milestone gave the company a two- to three-year advantage over competitors. The new technologies could not be easily copied, and although Sony did not have full patent protection it outstripped market growth and expanded market share over the years by moving early and shifting up from one technology to the next. Its current leading-edge semiconductor technology is Cu-Cu interconnect, and it is the chief reason Sony retains an advantage in the CMOS image sensor sector.

Technology trend of Sony's CMOS image sensors

A multi-layer CMOS image sensor separates the sensor responsible for imaging from the semiconductor (logic circuit) responsible for processing light-generated signal inputs and assigns the two functions to independent chips that are then laminated, one over the other, as in Figure 26. A feature of traditional BSI CMOS image sensor manufacturing is the need for a support substrate to reinforce the very thin image sensor.

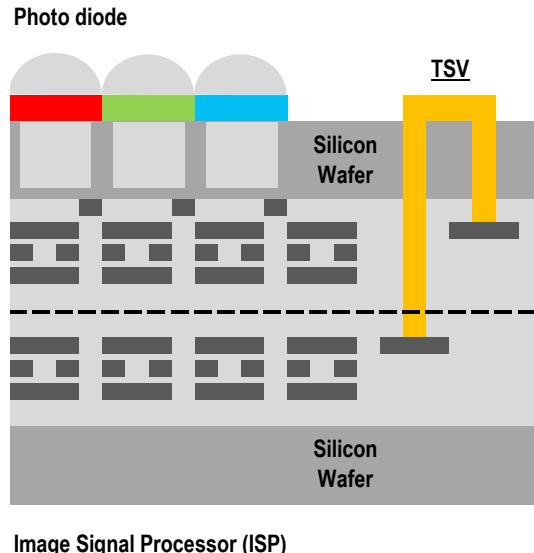
While the support is not necessary for the CMOS image sensor to function (it simply adds stiffness), it must be made of silicon, which has the disadvantage of adding cost. In a multi-layer CMOS image sensor, the silicon support substrate can be put to good use if the digital signal processor (DSP) circuit is created directly on the support, which eliminates waste and the need for a separate DSP section, which usually sits alongside the sensor semiconductor. That, in turn, allows the imaging area of the sensor to be smaller.

Figure 68. Multi-layer CMOS image sensor



Source: Company data, Citi Research

Figure 69. Structure of Multi-layer CMOS image sensor (TSV)



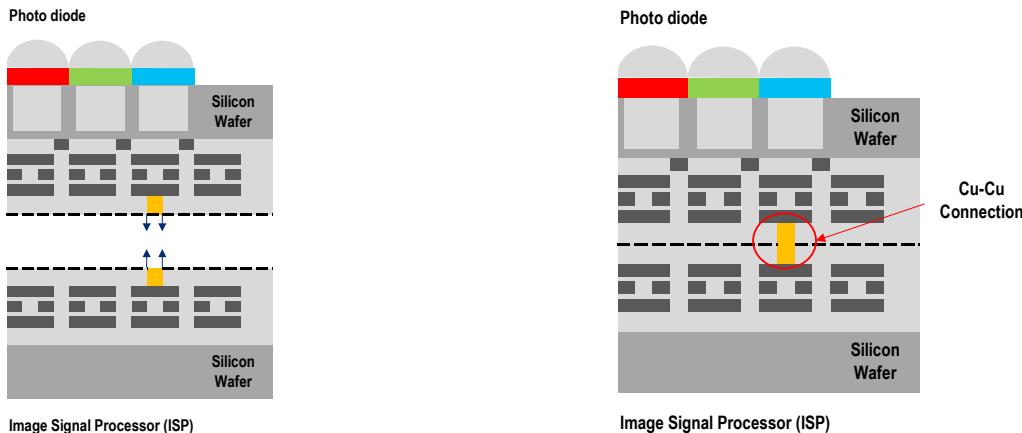
Source: Company data, Citi Research

Multi-layer CMOS image sensors were the result of an innovative idea. Sony first announced the technology in 2012. Many companies have now developed similar sensors and some CMOS image sensor makers are in the process of gearing up mass production, but connecting the sensor and the DSP sections is technologically challenging. Different companies are at different stages of advancement.

Connecting two semiconductors is usually done using through-silicon via (TSV) stacking and Cu-Cu bonding technology, which requires low noise levels and high-speed throughput.

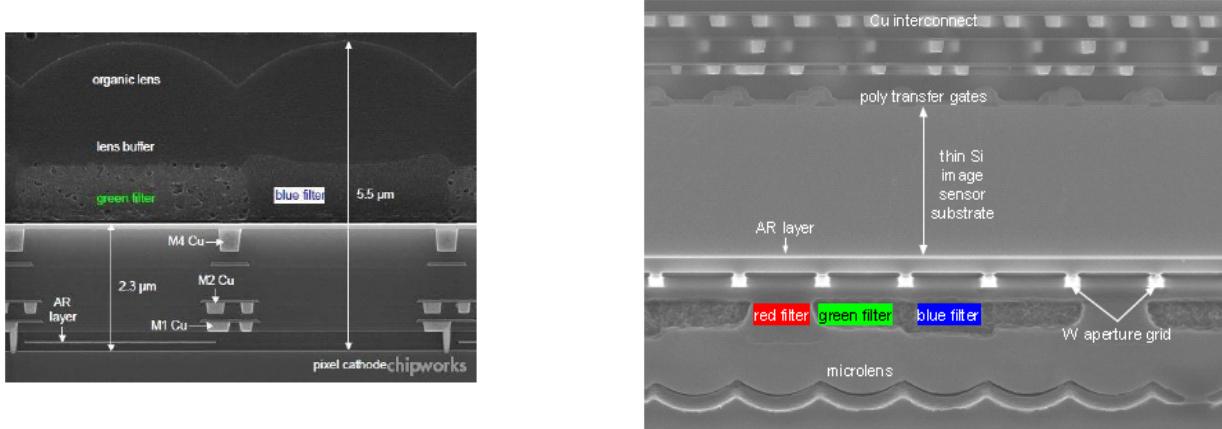
TSV and Cu-Cu bonding technologies were originally developed for multi-layer memory chip applications, but it is very difficult to accurately align and attach semiconductors with circuit patterns precisely etched at the sub-micron level. Among semiconductor technologies, TSV and Cu-Cu bonding are mechanical technologies and a field where expertise makes all the difference.

Figure 70. Structure of Multi-layer CMOS image sensor (Cu-Cu connection)



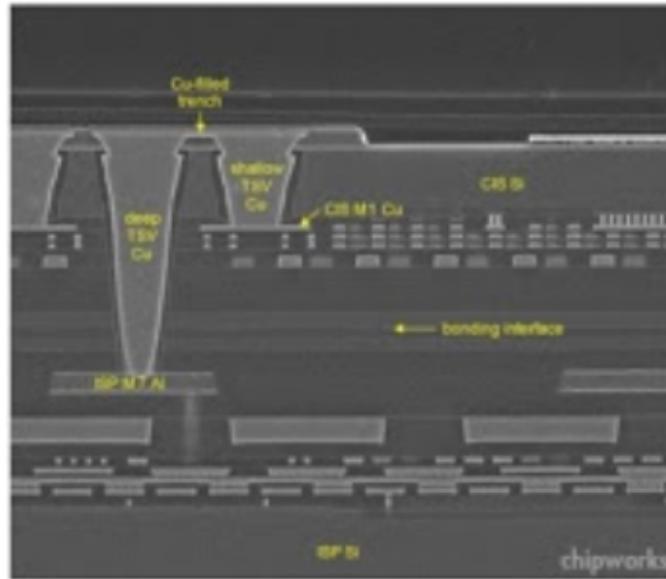
Source: Company data, Citi Research

Figure 71. CMOS image sensor cross-section (front illuminated LHS, back illuminated RHS)



Source: Chipworks, Citi Research

Figure 72. SEM picture of TSV BSI-CIS



Source: Chipworks

Sony's current thrust at the CMOS image sensor cutting edge is the development of a new product domain—intelligent vision sensors incorporating AI in the logic layer at the bottom of 3D structures.

Image sensors incorporating AI are a form of edge computing known as edge AI. Data extracted from the sensors can be confined to necessary data, which is said to facilitate data transmission efficiency, address privacy issues, realize low power consumption, and cut communication costs.

SPE/Semi Materials → More CVD/ALD/CMP and Etching Process and New materials

Market Impact 3: More CVD/ALD/CMP Etching Process, and New materials

In semiconductor material and equipment space, we project migration to 3D structure and innovations in semiconductor materials to generate significant changes and opportunities for material and equipment suppliers.

In particular, we expect increased deposition process, especially with the wider adoption of 3D structure, will facilitate adoption of CVD and ALD process. For example, as the number of layers in 3D NAND reaches 200, and eventually above 400 in the long-term, usage of CVD/ALD process is expected to increase by 30% per generation upgrade.

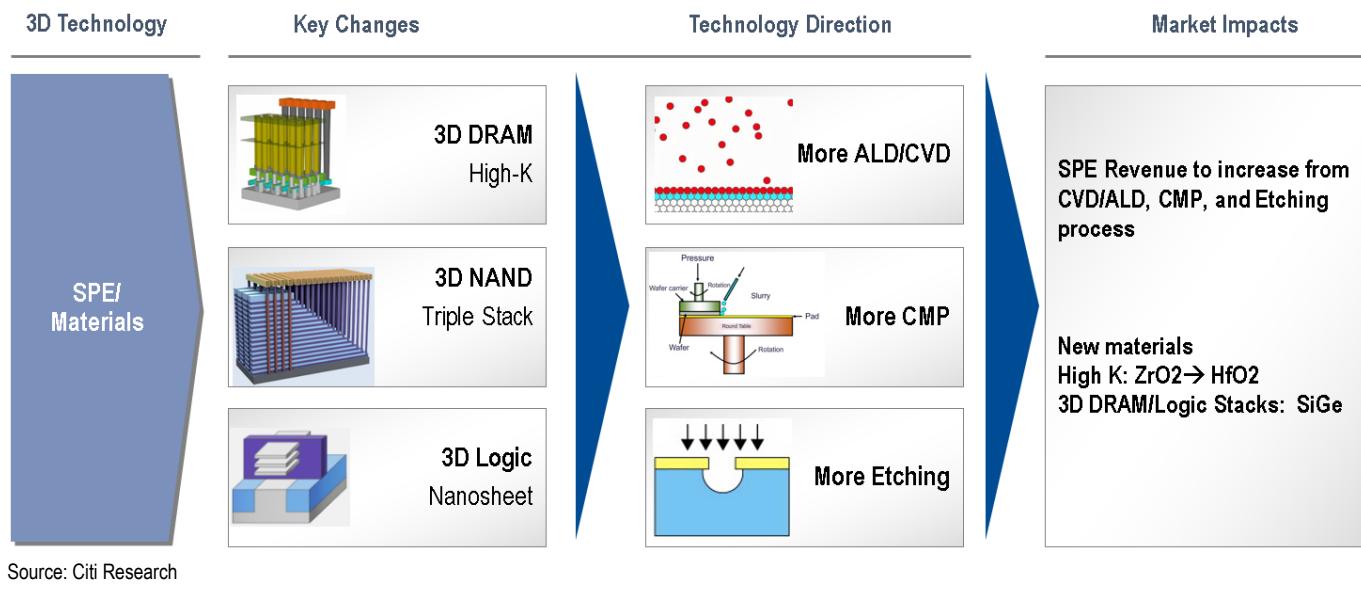
Positive on LAM Research, TEL, Entegris and ASM Pacific

Additionally, we foresee increased demand for CMP process on the back of increased ALD&CVD process as these processes require CMP process to flatten stacked layers. We also forecast increased demand for Dry Etch and Wet Etch process amid increased Hole etching process, such as HARC. Among SPE/material global plays, we are positive on LAM Research (CVD/Etch), TEL (CVD/Etch), Entegris (Chemicals) and ASM Pacific (Package).

Related Korea names are Wonik IPS, Eugene Tech, TES, SK Materials, KC Tech, Soulbrain, and Hansol Chemical

Related Korea SPE plays are Wonik IPS (CVD/ALD), Eugene Tech (CVD/ALD) and TES (CVD). Related Korea Material names are SK Materials (CVD gas/Precursor), KC Tech (CMP/CMP Slurries), Soulbrain (Etchant), and Hansol Chemical (H₂O₂).

Figure 73. Market Impacts: More CVD/ALD/CMP Etching Process, and New materials



Source: Citi Research

CVD and ALD Process to increase

CVD (Chemical Vapor Deposition)

Looking ahead, the use of CVD should increase further in line with the anticipated shift from 128 layers to 176 layers. In particular, we expect the use of PECVD to expand, noting that the rise in the number of layers in 3D NAND structures requires a 30% increase in the use of ONO PECVD-related materials. Of note, PECVD comes in three types: ONO PECVD, ACL PECVD, and ARC PECVD.

ONO PECVD is used to deposit ONO in the 3D NAND fabrication process via the gate last method—the method that most 3D NAND players have adopted. ACL

PECVD is designed to deposit amorphous carbon layers, while ARC PECVD deposits antireflective coating layers. We believe that: Applied Materials (PECVD overall), Wonik IPS (PECVD for ONO and ARC deposition) and TES (PECVD for ACL deposition) will be the main suppliers of the expected rise in PECVD use stemming from the shift from 128/176 layers to 200 layers.

Figure 74. Types of CVD

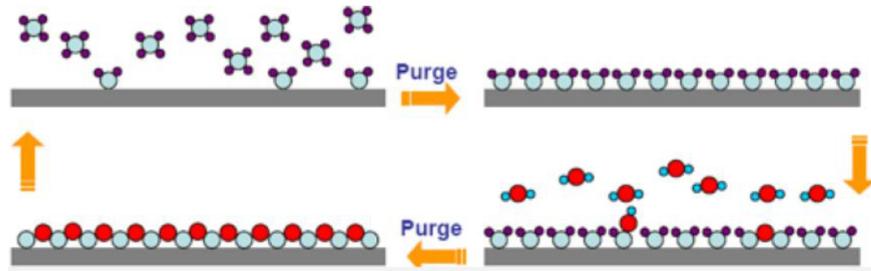
Type	LP CVD (low pressure CVD)	PE CVD (plasma enhanced CVD)	ALD (atom layer deposition)
Characteristics	Used to deposit wide range of possible film compositions with good conformal step coverage	Used to deposit SiN and amorphous Si film with the help of plasma added in the deposition chamber with reactive gasses PE-TEOS (PE-tetraethoxysilane)	Used to deposit thin film based on the sequential use of a gas phase chemical process
Film	SiO ₂ , Si ₃ N ₄ , Poly-Si		SiO ₂ , ZrO ₂
Film function	Nitride layer, dielectric layer	Insulating layer	Dielectric layer
Equipment makers	Eugene Technology, AMAT, TEL	Wonik IPS, AMAT, TES	AMAT, TEL, Wonik IPS, Jusung Engineering, Tera Semicon
Materials suppliers	Versum, Wonik Materials, SK Materials	Versum, Wonik Materials, SK Materials	DNF, Adeka, Hansol Chemical, Wonik Materials
Film thickness	Thin	Average	Very thin

Source: Citi Research

ALD (Atomic Layer Deposition)

We predict that the number of atomic layer deposition (ALD) processes will increase in line with the advance to higher-stacked 3D NAND. ALD is a thin film deposition technique based on the sequential use of a gas phase chemical process; ALD mainly uses chemicals (precursors) which react with the surface of a material. Via repeated exposure to different precursors, a thin film is slowly deposited. Of note, precursors—contain ligands and either silicon or metal materials—are used to create sacrificial (temporary) layers. During layer deposition, the ligands are removed from the precursor, leaving the silicon or metal behind.

Figure 75. ALD Process



Source: Citi Research

Precursors

Examples of silicon-based precursors include HCDS and DIPAS. These precursors can create: 1) insulation layers (such as SiO₂) in an oxygen atmosphere; or 2) nitride layers (such as SiON or Si₃N₄) in a nitride atmosphere. For the creation of high-K gate dielectrics, ZrO₂ was mainly used. In order to form a ZrO₂ layer, precursors fitted with large-size penta-ligands are used. Meanwhile, zirconium-based precursors allow ZrO₂ layers to be formed in an oxygen atmosphere. However, we see HfO₂ will become main materials for high-K in DRAM.

Depending on the layer made via the precursor-based deposition process, precursors are generally classified as: 1) diffusion barrier precursors; 2) electrode

precursors; 3) hard mask precursors; 4) high-K precursors for capacitors; or 5) high-K precursors for gate oxide layers. Of note, diffusion barriers are used to prevent insulation layers from being contaminated by metal molecules or other impurities during the metallization process.

Precursors names: SK Materials, DNF, Hansol Chemical and Wonik Materials

Until recently, the global semiconductor precursor market was dominated by a limited number of global players (mainly US and Japanese firms), but recently, domestic companies have been making rapid advances. Notable domestic players include DNF, Hansol Chemical, Wonik Materials, and SK Materials. DNF has developed a zirconium-based high-K precursor for DRAM capacitors and has been mass producing DIPAS (precursor material for the DPT process). SK Materials has recently established a JV (SK Trichem; with Tri Chemical (Japan)) for precursor manufacturing, and Hansol Chemical has also launched a precursor business

Figure 76. Types of Precursors

Types	High-K	DPT/QPT	HCDS	SOH (Spin-on Hardmask)	SOC (Spin-on Carbon)	SOD (Spin-on Dielectric)
Characteristics	Material with high dielectric constant	Material for patterning purpose	ALD precursor for formation of thin film layer	A membrane applied to the bottom of photoresists, and acts as a barrier in the follow-up etching process	Similar to SOH material	Material used for insulation within the transistors inside a memory chip,
Domestic producers	DNF Soulbrain Hansol Chemical ADEKA	DNF Hansol Chemical VERSUM	DNF Hansol Chemical Dow Chemical	Samsung SDI DNF	Dongjin Semichem DNF	Dongjin Semichem DNF

Source: Citi Research

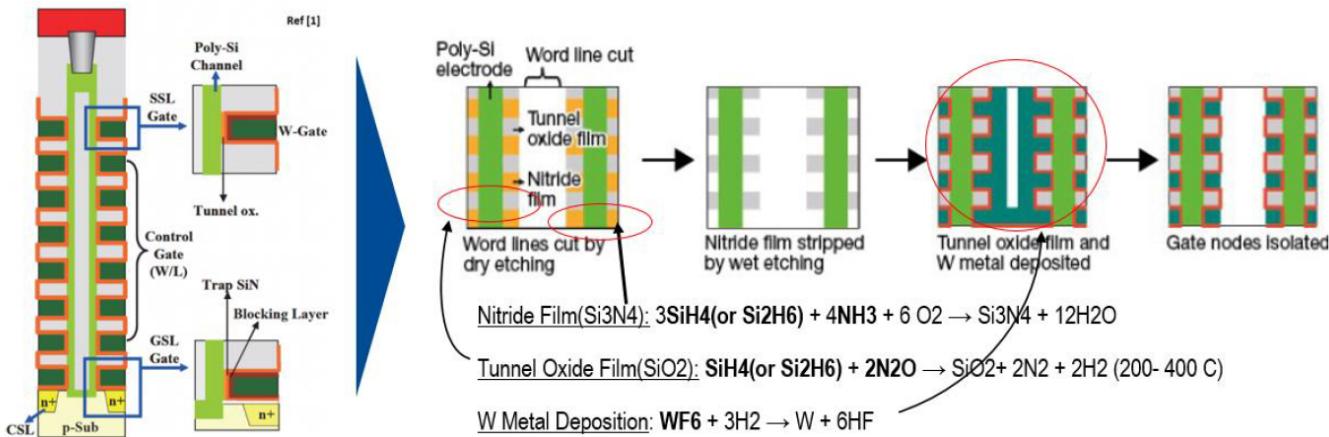
Tungsten CVD

The increase in the number of stacked layers for 3D Architecture products should lead to a hike in the number of tungsten CVD process steps. Given that within 3D Semiconductor structures, the tungsten layer comprises a control gate electrode contact, we expect consumption of WF6 gas to grow going forward.

Of note, WF6 is used in the CVD process for manufacturing semiconductor chips, and upon its decomposition, WF6 molecules leave a metallic tungsten residue. In the past, the PVD or the metal target sputtering process were the most commonly used process for metal layer deposition. However, in line with the nodes for semiconductor chips shrinking, metal CVD processes using gases have become more favored.

In fabricating 3D NAND chips, a tungsten metal gate is formed through: 1) deposition of an ONO layer; 2) HSN etching using high-selectivity phosphoric acid; and 3) the MOCVD process to fill the etched area with tungsten ($\text{WF}_6 + 3\text{H}_2\text{O} \rightarrow \text{WO}_3 + 6\text{HF}$). In our view, Applied Materials, Wonik IPS (metal CVD equipment), SK Materials (WF6), and Foosung (WF6) will prove to be the main suppliers of a hike in the number of tungsten CVD steps.

Figure 77. Increase in metal CVD steps leading to greater WF6 consumption



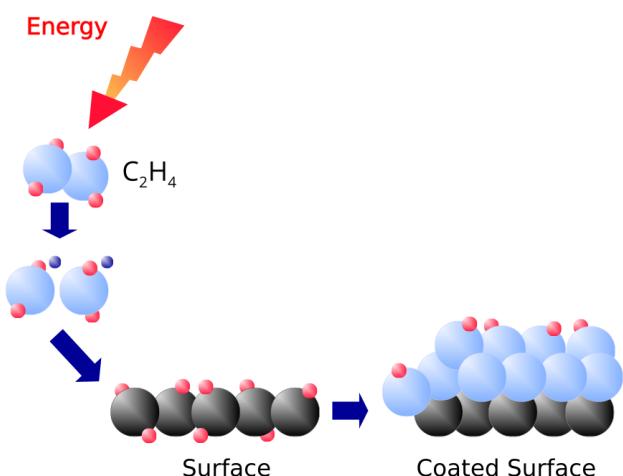
Source: Citi Research

What is Deposition process?

The deposition process includes both dielectric film deposition, using chemical vapor deposition (CVD), and metal deposition, via physical vapor deposition (PVD) or electrical plating (ECP). The dielectric film deposition is to produce high quality, highly conformal solid material to insulate all of the metal lines within the IC and to be as the main supporting materials to hold the entire physical architecture of IC. Similarly, metal deposition is to deposit a thin layer of metal, i.e., tungsten or copper, on top of the dielectric film by sputtering or by electric plating.

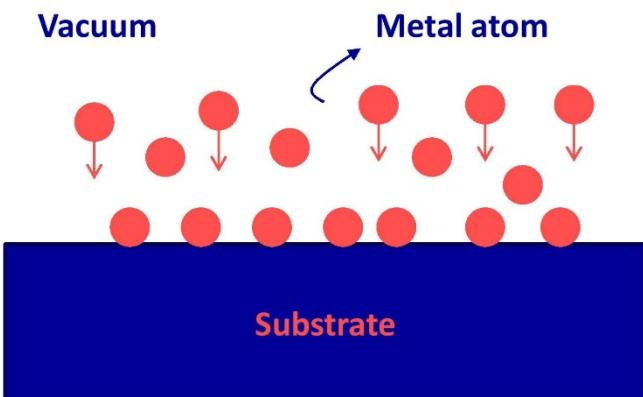
The thin layer of metal is subsequently defined as the metal lines by lithography and etch processes. AMAT is also the market share leader for both dielectric and metal thin film deposition. The largest player enjoys 44% of the total market share of deposition. The CVD for dielectric thin film and PVD/ECP for metal film plating contribute a big chunk of total revenue to the largest player. Key players of deposition equipment include Lam Research (LRCX), Tokyo Electron (TEL) and ASM International (ASMi).

Figure 78. Chemical vapor deposition (CVD) – Ions in the plasma formed the specific thin film and deposited on top of the object surface



Source: Plasma-electronics

Figure 79. Physical vapor deposition (PVD) process allows metallic atoms to be deposited on the substrate surface

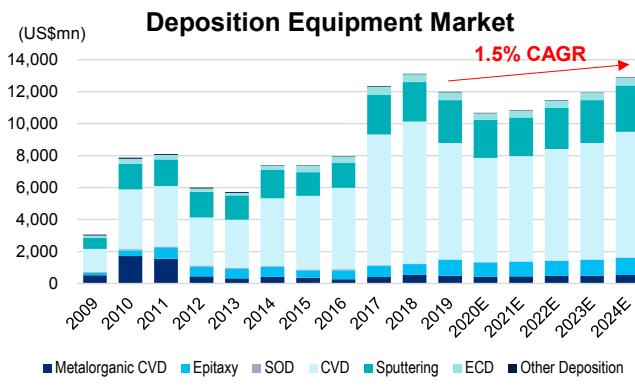


Source: Arco Engineering

ASMi is the major supplier of the epitaxy reactor for the ultra-thin film deposition. ASMi's epi reactor is one of the key components which needs US government's approval before shipping to users. LRCX, ASMi, and the deposition market leader are all US based WFE makers dominating 66% of the CVD deposition market, with the leader enjoying 85% of the PVD market and LRCX dominating 81% of the copper electroplating business.

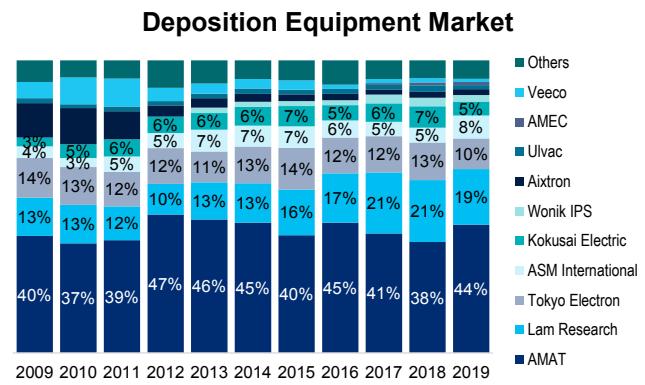
Besides US-based makers, Tokyo Electronic (TEL) in Japan is capable of providing mainly furnace types dielectric deposition equipment. In China, NAURA started to book revenue from CVD tools for legacy technology nodes deposition. NAURA's deposition WFEs are far from the quality requirements for advanced node, i.e., 28nm and belows, in our view.

Figure 80. Total market size of deposition equipment



Source: Gartner, Citi Research

Figure 81. Deposition equipment market share breakdown



Source: Gartner, Citi Research

Figure 82. Key companies in deposition (CVD, ALD) value chain

Process	Company Name	Ticker	Country	Type
LPCVD	Applied Materials	AMAT	US	Equipment
	Tokyo Electron	8035.JP	JP	Equipment
	Hitachi	6510.JP	JP	Equipment
	Wonik IPS	240810.KQ	KR	Equipment
	Eugene Tech	084370.KQ	KR	Equipment
	Jusung Engineering	036930.KQ	KR	Equipment
PECVD	Applied Materials	AMAT	US	Equipment
	Lam Research	LRCX	US	Equipment
	Tokyo Electron	8035.JP	JP	Equipment
	Wonik IPS	240810.KQ	KR	Equipment
	TES	095610.KQ	KR	Equipment
	Jusung Engineering	036930.KQ	KR	Equipment
ALD	Lam Research	LRCX	US	Equipment
	Tokyo Electron	8035.JP	JP	Equipment
	Applied Materials	AMAT	US	Equipment
	Jusung Engineering	036930.KQ	KR	Equipment
	Wonik IPS	240810.KQ	KR	Equipment
	Eugene Tech	084370.KQ	KR	Equipment
Specialty Gas	TES	095610.KQ	KR	Equipment
	DNF	092070.KQ	KR	Equipment
	Air Products	APD	US	Materials
	Mitsui	8031.T	JP	Materials
	SK Materials	036490.KQ	KR	Materials
	Kanto Denka Kogyo	4047.T	JP	Materials
Precursors	Showa Denko	4004.T	JP	Materials
	Wonik Materials	104830.KQ	KR	Materials
	Hoosung	093370.KS	KR	Materials
	Soulbrain	357780.KQ	KR	Materials
	Linde	LIN	US	Materials
	Adeka	4401.JP	JP	Materials
	SK Materials	036490.KQ	KR	Materials
	Soulbrain	357780.KQ	KR	Materials
	DNF	092070.KQ	KR	Materials
	Hansol Chemical	092070.KQ	KR	Materials
	Air Products	APD	US	Materials
	Linde	LIN	US	Materials

Source: Citi Research

CMP process steps to increase

CMP(Chemical Mechanical Polishing)

In line with advances towards higher-stacked 3D NAND and continued tech migration and transformation of 3D DRAM and 3D Logic devices, the number of CMP processes—the CMP process smooths wafer surfaces using chemical and mechanical forces after the CVD process—is set to expand.

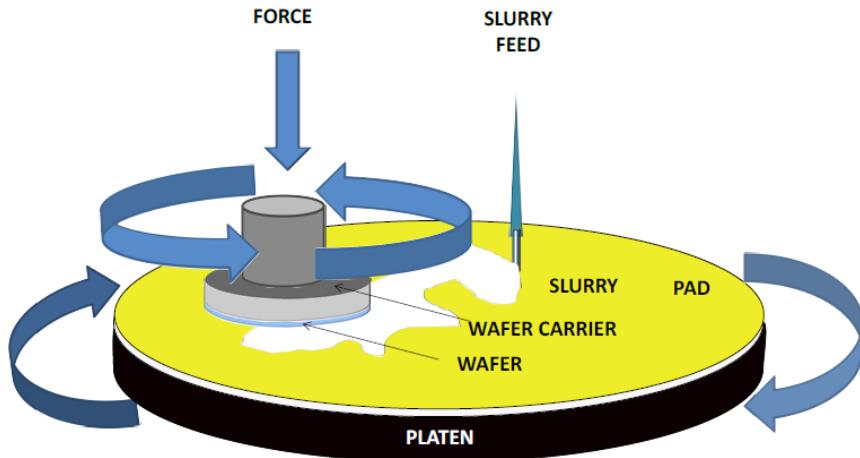
In particular, with chipmakers striving to produce higher-stacked 3D Semiconductor architecture with material changes, the increase in the number of stacks will eventually lead to a greater number of oxide CMP and tungsten CMP processes. Also, in line with additional hole etching and extra channel formation steps, more CMP processes will be needed. As slurry (an abrasive and corrosive chemical material that comes in the form of a fluid mixture of a pulverized solid with a liquid) plays a key role in the CMP process, CMP slurry is set to come into greater use in line with more CMP process steps

What is CMP(Chemical Mechanical Polishing)?

The CMP process uses an abrasive and corrosive slurry in conjunction with a polishing pad and a retaining ring, typically of a greater diameter than the wafer. The pad and the wafer are pressed together by a dynamic polishing head and held in place by a plastic retaining ring. The dynamic polishing head is rotated with different axes of rotation. This removes material and tends to even out any irregular topography, making the wafer flat (planar).

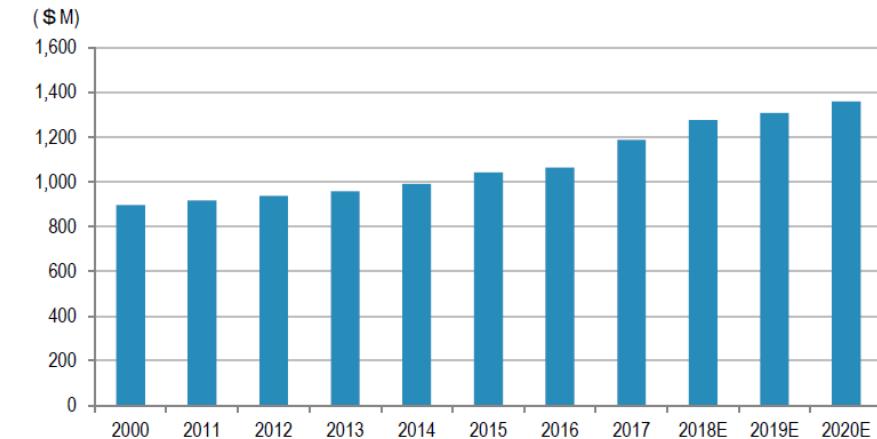
Chemical mechanical polishing is a process used to prepare the wafer surface for semiconductor fabrication. It uses an abrasive, CMP slurry, and acid and alkaline solvents to create a chemical reaction at the same time as using a polishing pad to mechanically smooth out the wafer surface.

Figure 83. CMP equipment schematic



Source: Citi Research

Figure 84. CMP Slurry Market size



Source: Citi Research

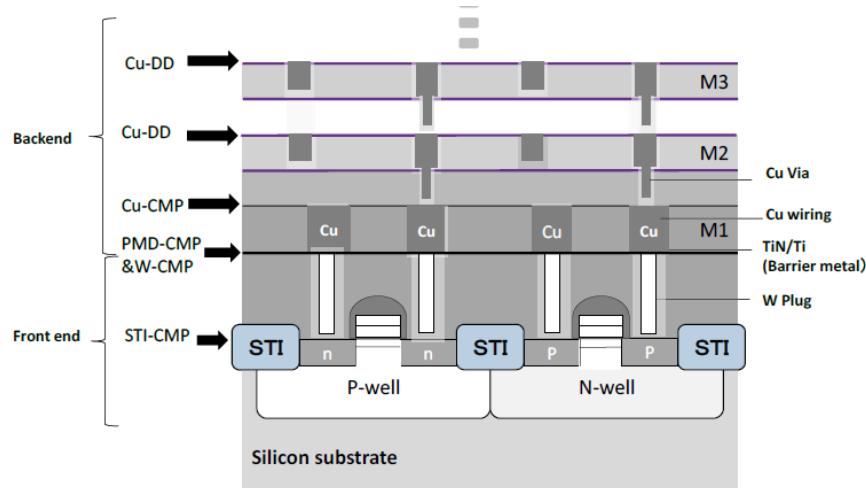
Figure 85. CMP Supply Chain



Source: Citi Research

Processes that use CMP slurry can be categorized into four: STI-CMP, W-CMP, metal-CMP (mainly copper), and ILD-CMP. And although we do not discuss it in this section of the report, there are also CMP slurries used in silicon wafer manufacturing processes and in rear-end semiconductor polishing processes.

Figure 86. Structure of logic chips and layers to which CMP is applied



Source: SEMI materials, Citi Research.

Types of CMP

Simply put, the CMP process evens out the topography of silicon oxide, poly silicon, and metal surfaces (commonly referred to as oxide CMP, poly CMP, and metal CMP, respectively). CMP is used to planarize oxide, poly silicon, or metal layers in order to prepare them for the next lithographic step.

Thus, the type of slurry used depends on the composition of the layers. Regardless of the layers' composition, CMP uses chemical and mechanical forces to smooth surfaces. Looking at the CMP process in more detail, the oxide CMP process can be categorized as: 1) STI CMP; or 2) ILD/IMD CMP. Of note, STI CMP entails more technological challenges compared to ILD/IMD CMP.

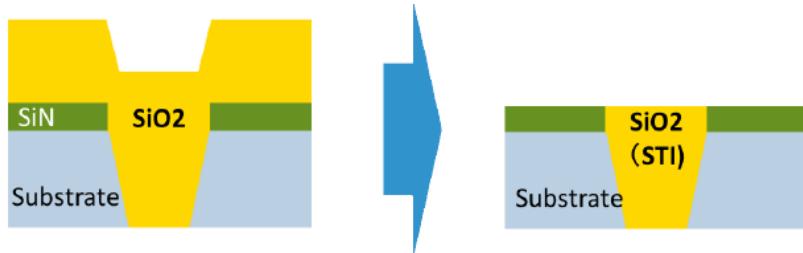
STI CMP

STI-CMP is used in a process known as shallow trench isolation. The STI process is used to create layers that electrically insulate neighboring transistors and the like. Nitride and oxide layers are formed on the wafer, and lithography and etching processes used to create the isolation trench between elements. An insulating oxide layer is then formed in this trench, and excess oxide removed by polishing with an abrasive. In STI-CMP, the transistor connections are polished, so tolerances for defects are the most demanding of any CMP process. STI structures are also in the

bottommost layer of the devices, so standards for planarity are also exceptionally demanding

Compared to the metal CMP process, the oxide CMP process is more likely to result in scratches or defects due to the inherent weakness of oxide layers. Thus, it is critical to use CMP slurry that has a low probability of causing scratches or defects. Nowadays, as a solution to the increasing number of defects/scratches seen on the wafer surface, oxide buffering steps (during the CMP process) have become more commonplace. In this regard, we note that KC Tech appears well positioned to benefit from growing demand for oxide buffering equipment—the company is the sole oxide buffering equipment maker in Korea.

Figure 87. STI-CMP Process



Source: Citi Research.

ILD CMP

ILD-CMP stands for interlayer dielectric CMP. An ILD is a layer used for insulation between copper and other circuits, and the main materials used are SiO₂ and SiN.

The main abrasive used in ILD-CMP slurry is fumed silica, because of its cost competitiveness, but there is also increasing use of ceria slurry, which is better suited to high speed polishing.

Cabot Microelectronics has the top market share of almost 40% in ILD-CMP slurry, and Dow/DuPont ranks second with around 20%. We think that Hitachi Chemical's market share was previously low here, but that chipmakers have given high marks to the polishing performance of its ceria slurry, and that since around 2016 it has been increasingly adopted for the polishing of silicon oxide layers in 3D NAND.

The uneven oxide layers have become thicker as the number of layers in 3D NAND has increased, so the amount of time required for polishing has also increased and therefore the amount of slurry used has grown. We also think chipmakers are also increasingly adopting Hitachi Chemical's nanoceria slurry for logic chips using processes of 10nm and finer, given its superiority in terms of polishing properties and polishing rates.

Meanwhile, tungsten CMP and copper CMP comprise the metal CMP process. As copper CMP entails serious contamination issues (relates to copper), the copper CMP process needs to be done in a separate clean room (apart from other front-end processes).

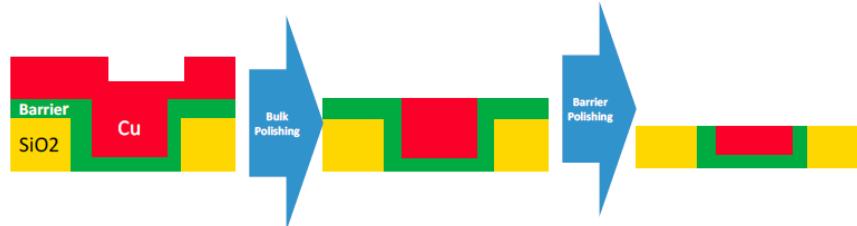
W CMP

W-CMP stands for W plug (tungsten plug) CMP. Tungsten is a very hard material, making processing difficult, but generally after the oxidization of the wafer surface, the oxide layer is removed using CMP. The main abrasive for W-CMP is fumed silica. Some manufacturers used colloidal silica for secondary polishing. Cabot Microelectronics has many patents in this area, and has a dominant market share of just over 80%.

Cu CMP

Metal CMP (mainly copper) can be categorized into either copper bulk CMP or copper barrier CMP. Copper bulk CMP is a process used to remove copper, while copper barrier CMP is a process used to remove the substrate barrier metal. Logic LSIs are fabricated by connecting up a range of circuit blocks, so multilayer interconnections are required. Mainly copper is used for the local interconnections in multilayer wiring. For logic semiconductors, 70% of all processes are multilayer interconnection processes, which are essentially backend processes. The more advanced the logic semiconductor the larger the number of layers tends to be, and high-end logic chips may have multilayer interconnections for around 10 layers. In contrast, most memory chips are one to three layers. So logic semiconductors are the main application for metal CMP.

Figure 88. STI-CMP Process



Source: Citi Research

CMP Slurry

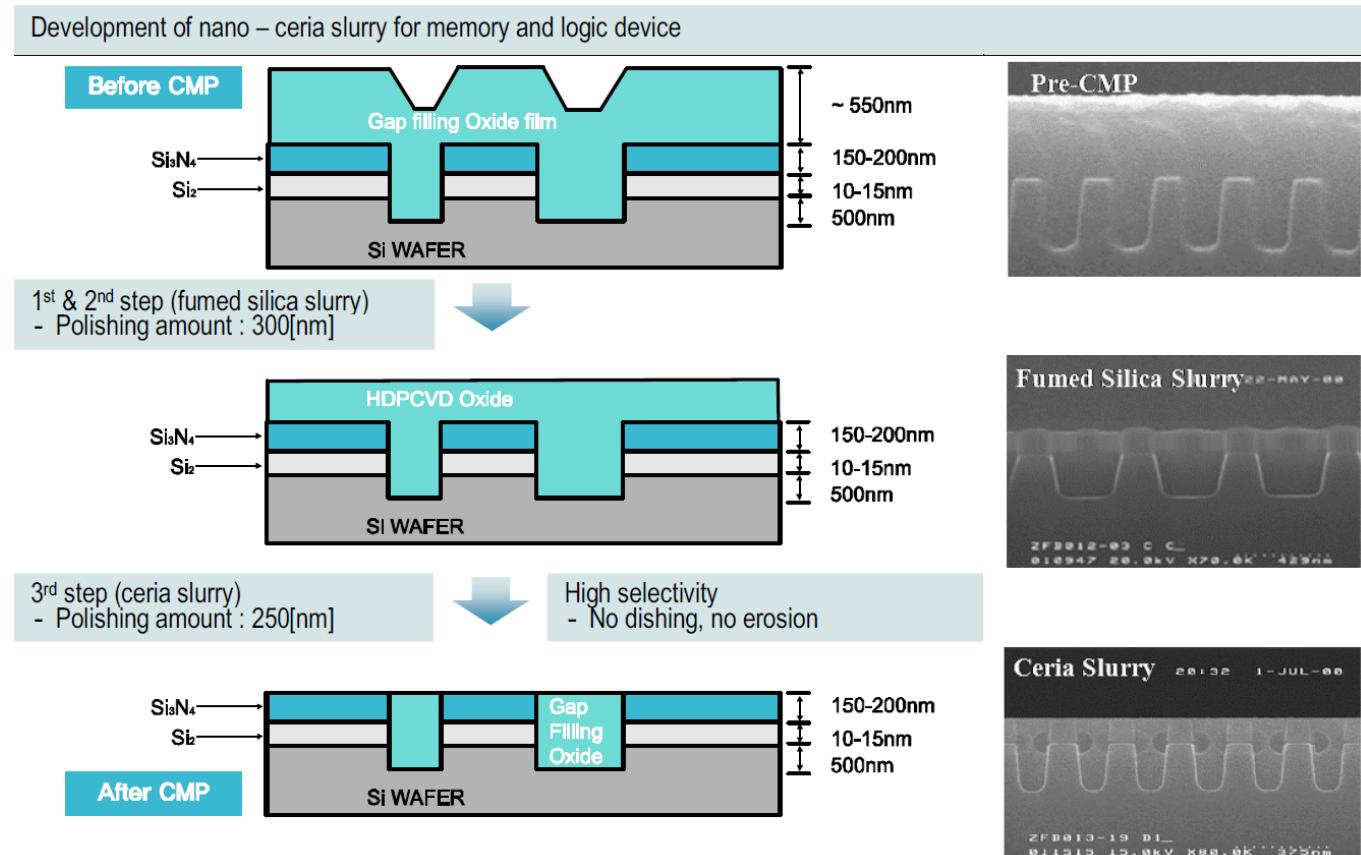
As mentioned previously, we believe that CMP slurry demand will grow in line with a hike in the number of CMP steps. An abrasive and corrosive chemical liquid (comprised of a pulverized solid with a liquid), slurry has a key role in the CMP process.

The type of pulverized particles in a slurry is mainly SiO₂ or CeO₂, and the kind of slurry used depends on the layer type. Silica type slurry is mainly used for polishing metallic film (eg, tungsten layers and copper layers), whereas ceria type slurry tends to be used for polishing insulation film (eg, SiO₂ layers and Si₃N₄ layers). The most widely used type of slurry is CeO₂, and this type comprises the lion's share of the slurry market.

As for oxide slurry that is used to polish insulation layers, a basic liquid (eg, KOH) is mixed with fumed silica or a neutral liquid is mixed with additives to make ceria slurry. When it comes to slurries used for polishing metal (tungsten) layers, an acidic fluid (eg, H₂O₂) tends to be used as a solvent.

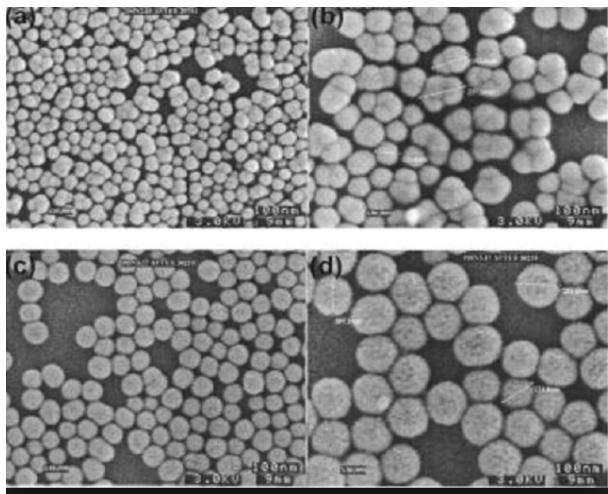
Global CMP slurry manufacturers include Cabot (US), Hitachi Chemical (Japan), and Fujimi (Japan). The only domestic CMP slurry makers are KC Tech (ceria/tungsten slurry), Soulbrain (ceria slurry), and Dongjin Semichem (tungsten slurry).

Figure 89. CMP process mechanism



Source: Citi Research

Figure 90. CMP Slurry(abrasive particle0



Source: Dongjin Semichem

Figure 91. CMP Slurry(Additive Mixed)



Source: KC Tech

Figure 92. CMP Process/Materials US Patent (co-invented by Peter Lee (Sei-Cheol Lee))



US007288212B2

(12) **United States Patent**
Kim et al.

(10) **Patent No.:** **US 7,288,212 B2**
(45) **Date of Patent:** **Oct. 30, 2007**

(54) **ADDITIVE COMPOSITION, SLURRY COMPOSITION INCLUDING THE SAME, AND METHOD OF POLISHING AN OBJECT USING THE SLURRY COMPOSITION**

(75) Inventors: **Nam-Soo Kim**, Suwon-si (KR); **Sang-Mun Chon**, Seongnam-si (KR); **Young-Sam Lim**, Seoul (KR); **Kyoung-Moon Kang**, Busan-si (KR); **Sei-Cheol Lee**, Seoul (KR); **Jae-Hyun So**, Seoul (KR); **Dong-Jun Lee**, Yongin-si (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon-si, Gyeonggi-do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 715 days.

(21) Appl. No.: **10/293,918**

(22) Filed: **Nov. 14, 2002**

(65) **Prior Publication Data**

US 2003/0092265 A1 May 15, 2003

(30) **Foreign Application Priority Data**

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Apr. 26, 2002 (KR) 2002-23087

(51) **Int. Cl.**

C09K 13/00 (2006.01)

C09K 13/04 (2006.01)

H01L 21/302 (2006.01)

(52) **U.S. Cl.** **252/79.1; 252/79.4; 438/692**

(58) **Field of Classification Search** 252/79.1,

252/79.4; 438/692

See application file for complete search history.

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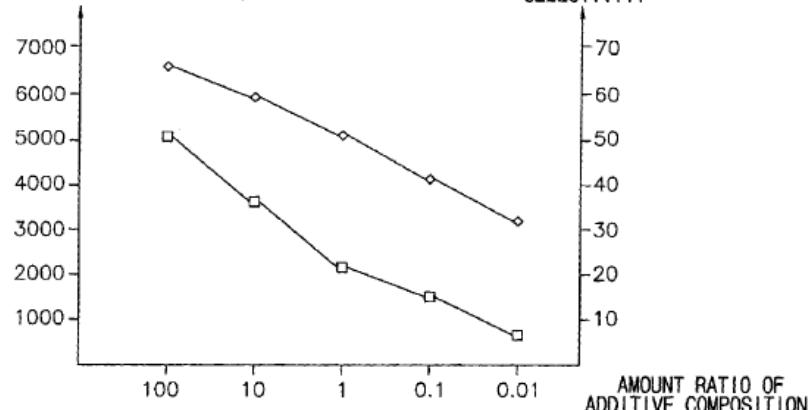
(74) Attorney, Agent, or Firm—Valentine & Whitt, PLLC

(57) **ABSTRACT**

An additive composition for a slurry contains a first salt of polymeric acid including a first polymeric acid having a first weight average molecular weight and a first base material, and a second salt of polymeric acid including a second polymeric acid having a second weight average molecular weight and a second base material. A slurry composition is prepared by mixing the additive composition, a polishing particle composition, and water. When implementing a chemical mechanical polishing using the slurry composition, a favorable polishing selectivity is realized.

8 Claims, 18 Drawing Sheets

POLISHING RATE OF SILICON OXIDE LAYER (Å/min)



POLISHING SELECTIVITY

Source: Google Patent Search, Peter Lee(Sei-Cheol Lee)

Figure 93. CMP Slurry US Patent (co-invented by Peter Lee (Sei-Cheol Lee))

U.S. Patent Oct. 30, 2007 Sheet 2 of 18 **US 7,288,212 B2**

FIG. 1C
(PRIOR ART)

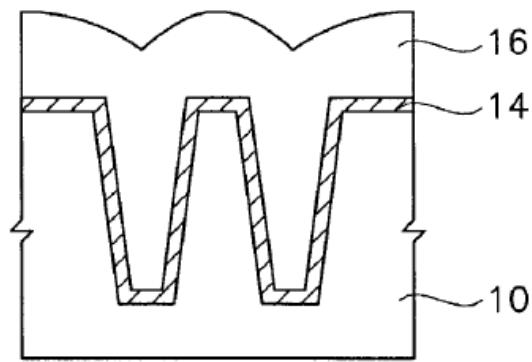
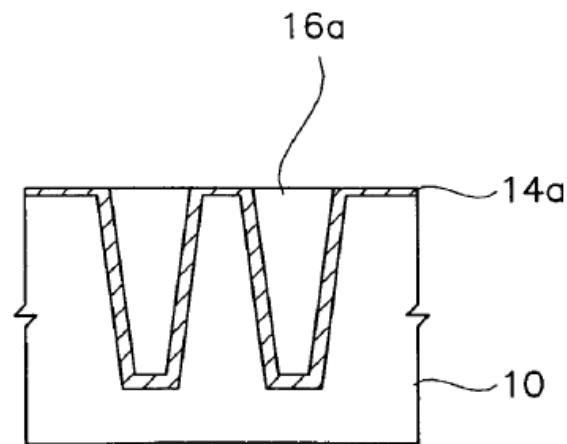


FIG. 1D
(PRIOR ART)



Source: Google Patent Search, Peter Lee(Sei-Cheol Lee)

Figure 94. Key companies in CMP value chain

Process	Company Name	Ticker	Country	Type
CMP	Applied Materials	AMAT	US	Equip
	Ebara	6361.T	JP	Equip
	Tokyo Seimitsu	7729.T	JP	Equip
	KCTech	281820.KS	KR	Equip
Cleaning	Tokyo Electron	8035.JP	JP	Equip
CMP Pad	Dow Chemical	DOW	US	Materials
	BASF	BAS.F	GER	Materials
	JSR	4185.T	JP	Materials
	Cabot	CBT	US	Materials
CMP Slurry	Dow Chemical	DOW	US	Materials
	3M	MMM	US	Materials
	Air Products	APD	US	Materials
	BASF	BAS.F	GER	Materials
	Fuji Film	4901.T	JP	Materials
	Asahi Chem	3407.T	JP	Materials
	Hitachi	6510.JP	JP	Materials
	Dongjin Semichem	005290.KQ	KR	Materials
	Soulbrain	357780.KQ	KR	Materials
	KCTech	281820.KS	KR	Materials
	SKC	011790.KS	KR	Materials

Source: Citi Research

Dry Etch and Wet Etch process steps to increase

In line with 3D NAND, and 3D DRAM/ 3D logic technology migration, demand for hole etching and selective etching will pick up. When it comes to hole etching processes, dry etching is set to be increasingly used, and demand for C4F6 as an etching gas should rise. Related players include SK Materials and Foosung.

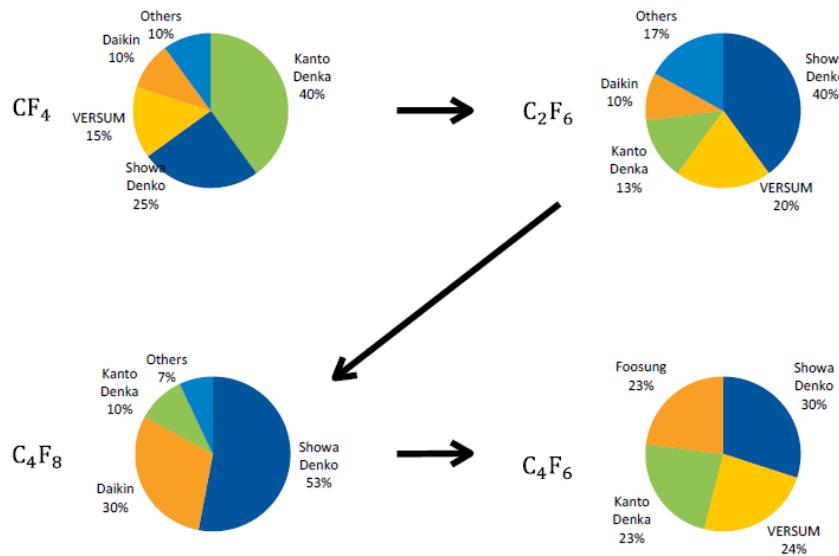
While concerns are mounting that dry etching will come to supplant wet etching as the main selective etching technique, we expect wet etching to continue to be used for selective etching for now. Of note, wet etching uses liquid-state etchants to selectively remove nitride layers. As high-selectivity phosphoric acids are a good choice for wet etching, demand for the materials should expand going forward. Related players include Soulbrain.

Semiconductor Gas

High-purity gases are used in a number of semiconductor manufacturing processes. Semiconductor gases are also referred to as “specialty gases” because they are of higher purity than general-use gases and because they differ chemically from ordinary industrial gases. Important applications include dry etching, ion implantation, and chamber cleaning after CVD processes. In this report, we focus on dry etching gases expected to grow more rapidly than growth in wafer input—gases that are benefitting from multilayer NAND production.

There are three main types of dry etching gas: fluorocarbon gases, chlorine gases, and hydrogen bromide (HBr). The fluorocarbon gases, as the name suggests, are mainly composed of fluorine and carbon. A higher ratio of carbon to fluorine is said to result in greater etching precision. New generations are developed periodically with higher carbon to fluorine ratios. We believe Showa Denko and Kanto Denka Kogyo supply most demand in almost all generations. Gases composed entirely of carbon and fluorine are mainly used for etching silicon oxide layers. Gases such as CHF3 that include hydrogen are used for etching silicon nitride layers.

Figure 95. Generational changes in fluorocarbon gases



Source: Citi Research

The most recent fluorocarbon gas introduced is C4F6. We believe C4F6 is about 10 times more expensive than the C4F8 gas of the previous generation, but demand appears to be rapidly expanding, mainly for use in 3D-NAND production. The ratio of carbon to fluorine is closer to being equal than in previously available fluorocarbon gases, making it suitable for anisotropic etching. We believe that explains expanding demand for use in 3D-NAND production, which requires etching at high aspect ratios. A doubling of the number of layers in a NAND device requires a tripling of the volume of gas used during production.

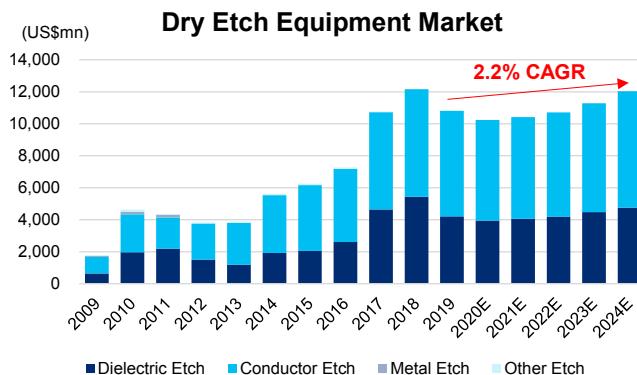
What is Etching process?

After the features are developed on the wafer surface by lithography, the wafer is subsequently put in the ambient with corrosive radicals or chemical to remove the dielectric film or metal layer away at the open area not protected by the photoresist. The process is so called "Etch". Etching process is to make the trench/via (hole) on the dielectric thin film or metal lines in the chip.

Lam Research (LRCX) and TEL are the key etch equipment suppliers worldwide. LRCX enjoys the lion's share on the critical layers etch of the leading edge technology nodes. TEL is also a meaningful supplier in the etch process, while the third largest player in the etch market is the largest WFE player in the world. The etching capability plays a critical role of the semiconductor manufacturing.

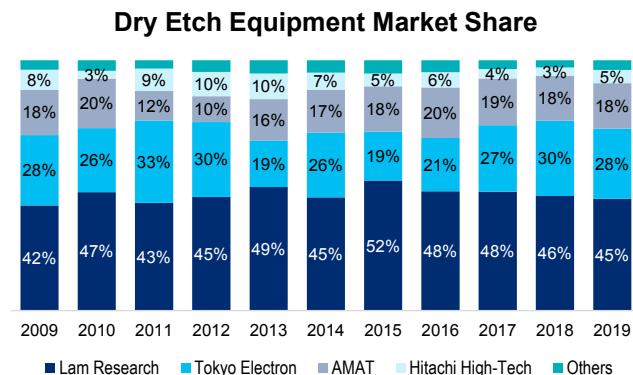
An inappropriate etching process may lead to circuit open or short and result in a low production yield rate. Most of the users are stick with the top tier of Etch suppliers for their critical layer etch process.

Figure 96. Dry etch market size



Source: Gartner, Citi Research

Figure 97. Dry etch market share breakdown



Source: Gartner, Citi Research

Figure 98. Key companies in Etching value chain

Process	Company Name	Ticker	Country	Type
Etcher	Tokyo Electron	8035.JP	JP	Equip
	Lam Research	LRCX	US	Equip
	Applied Materials	AMAT	US	Equip
	Ulvac	6728.T	JP	Equip
	Hitachi	6510.JP	JP	Equip
	TES	095610.KQ	KR	Equip
Asher	APTC	089970.KQ	KR	Equip
	PSK	319660.KQ	KR	Equip
	DMS	068790.KQ	KR	Equip
	Lam Research	LRCX	US	Equip
Cleaning	Axcelis	ACLS	US	Equip
	Ulvac	6728.T	JP	Equip
	Lam Research	LRCX	US	Equip
Etchant	Tokyo Electron	8035.JP	JP	Equip
	BASF	BAS.F	GER	Materials
	Fuji Film	4901.T	JP	Materials
	Soulbrain	357780.KQ	KR	Materials
	Dongjin Semichem	005290.KQ	KR	Materials
PR Stripper	ENF Technology	102710.KQ	KR	Materials
	Dow Chemical	DOW	US	Materials
	TOK	4186.T	JP	Materials
	Air Products	APD	US	Materials
	Fuji Film	4901.T	JP	Materials
Quartz/SiC/Si	ENF Technology	102710.KQ	KR	Materials
	Soulbrain	357780.KQ	KR	Materials
	Tosoh	4042.T	JP	Materials
	Shin-Etsu	4063.T	JP	Materials
	Tokai Carbon Korea (TCK)	064760.KQ	KR	Materials
	Hana Materials	166090.KQ	KR	Materials

Source: Citi Research

TEL

Tokyo Electron is positioned in the second group of SPE makers along with Lam Research (based on CY19 sales; VLSI) and has an extensive product line that includes coater/developers, dry etch systems, deposition systems, and wafer cleaning systems. Sales (new systems) are tilted more toward non-memory

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applications than Lam Research's at c40% DRAM/NAND to c60% logic/foundry (based on cumulative sales over most recent four quarters).

The medium-term business plan TEL announced in May 2019 targets higher profitability on the back of high-value-added system proposals aimed at driving market share for high-margin products. Etch systems have long been a particular focus for the company, and within this it looks especially to gain market share for the high aspect ratio contact (HARC) process. Specifically, it plans to increase share in word line isolation (slit) and eventually cut into Lam Research's current dominance in channel, all while maintaining its high share in multi-level contact. There has been no noticeable acquisition of new POR as yet, with the market share gains set to come in CY21 and beyond.

With memory capex looking set to expand in CY21, we see TEL as a potential standout among Japan's SPE names. The company is known for having high global market share in a growth business (SPE), but we also highlight its execution capabilities and enthusiasm for shareholder returns. Management's ability to accurately formulate and execute profit targets is evidenced by the fact that TEL has missed half-year OP guidance just once in the last 10 years. As for shareholder returns, TEL pays dividends commensurate with profits based on a 50% dividend payout ratio and also undertakes a large share buyback once every few years.

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LAM Research

Lam Research is the leading etch equipment supplier globally with more than 45% market share. Lam has a long successful history of developing innovative etch products especially memory. The company has high ~70% sales exposure to memory end markets, particularly 3D NAND. Lam is #2 in deposition market with ~20% market share. Historically, Lam has shown 2x the WFE rate of growth by participating in the faster growing etch and deposition 3D device opportunities. Management expects to gain 4-8% of share growth through 2023 in both etch and deposition through new capabilities and enhanced productivity. Management expects their SAM to reach 40% of WFE by 2023 with an additional 5-10% SAM expansion over the decade through the development of disruptive technologies and the conversion of opportunities with differentiated capabilities in ALD. Last year, Lam announced its new plasma etch tool called Sensai. The tool utilizes AI and machine learning to improve wafer output by 50% by increasing sensing performance, data monitoring, maintenance automation, and matching performance across multiple systems.

We are buy-rated on LRCX, our #1 equipment pick, as we expect stock to outperform the group on memory capex recovery in 2021. Longer-term, we expect US deposition and etch equipment suppliers to be major beneficiaries of 3D architecture adoption in DRAM and logic devices following adoption in 3D NAND.

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Entegris

Entegris has traditionally been more heavily exposed to logic and foundry due to the stricter materials purity requirements that shrinking nodes created. However, 3D NAND is poised to be a significant growth opportunity for Entegris due to the addition of new more conductive metals, new clean formulations, and new filtration requirements. Entegris expects to grow memory to 50% of sales, from 30% today, over the next 3 to 5 years.

Specific opportunities for Entegris include new metal precursors, selective etch chemicals, and filtration. Management recently highlighted filtration as one of the top drivers and noted that liquid filtration revenue per 3D NAND wafer increased

4.3x from 32L to 96L and they expect growth to continue in this market as new metals introduce new susceptibilities to contaminations and customers try to maximize yields while increasing long term device reliability. Entegris' solutions in this area include selective removal of new classes of contaminants, sieving and non-sieving methods, and tighter retention coupled with higher flow rates.

We are Buy rated on Entegris in part due to the SAM expansion and market share gains that they are experiencing, particularly in the 3D NAND market, which will allow them to continue to outgrow the market by 300-400bps for a CAGR of 9-10% from 2020-2023.

CMC Materials (Formerly Cabot Micro)

CMC Materials is the leading supplier of Tungsten slurries, an enabling metal for 3D NAND. CMC saw a significant step up in slurries revenue in 2018 due to the initial conversion to 3D NAND from planar, but that revenue has remained relatively stable over the last 2 years. That initial conversion saw a doubling of CMP steps, however the rate of expansion of CMP steps is expected to slow down as layer counts continue to rise in 3D NAND. We believe that efficiencies in slurries, a slowing of CMP step increases, the addition of new metals that could potentially replace some Tungsten, and new competition in Tungsten slurries present a risk to CMC's revenue opportunity in the future. Management expects that there will be a step up in slurries revenue in 2H21 as 3D NAND capacity expands.

We are Sell rated on CMC Materials as weakness on the top line lowers our confidence that CMC can sustain growth relative to other consumable stocks in our coverage which have been raising growth targets and beating topline estimates recently. We view competition and efficiencies in slurry usage as key threats for significant growth moving forward.

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ASML

ASML dominates the lithography landscape with a market share of ~88% in the stepper segment in 2019, according to data from industry research firm Gartner. We have a positive recommendation on the shares based on three core premises – 1) Faster digital transformation, 2) Higher operational profitability, and 3) Stronger platform. For more details on our thesis, please see our recent deep dive: [ASML Holding NV \(ASML.AS\) - Citius Altius Fortius](#)

In terms of the longer-term move to 3D architecture, below we outline the broad implications for lithography by segment:

- **Logic** — We expect the lithography intensity to continue to rise on a consistent basis as we go further down the nodes. We believe that the high NA EUV from ASML will be intensively adopted to resolve the finer pitch and complicated lithography in 3nm. We do not anticipate the potential shift to GAA (gate all around) or nanosheet at 2nm to trigger a meaningful shift in the level of intensity or composition of lithography systems needed for semiconductor fabrication.
- **DRAM** — We expect EUV adoption to accelerate at 1a node and gradually rise further at 1b and 1c nodes. The associated time frame is likely out to 2025. Beyond 2025, as we noted earlier in the report, we do see a potential path over to full 3D architecture. While we would expect the DRAM lithography intensity to continue to rise beyond 2025, the exact implications in terms of composition of the systems needed is less clear as compared to the logic roadmap in our view.

■ **NAND** — With respect to NAND, we note that the roadmap calls for greater level of stacking and ASML's DUV (led by immersion) portfolio is more relevant in this context, with a particular emphasis on the overlay capabilities. If we expand the discussion and call it non-volatile or storage memory (instead of NAND), then the migration to XPoint down the road will also result in lithography implications beyond 2025.

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ASM Pacific

After acquiring NEXX in 2018 from TEL (covered by Shibano san), ASMP (0522.HK) became a key player in the mid-end process equipment market. NEXX focuses on the PVD and ECD markets. Its machines are used for RDL (re-distribution layer) processes and clients are premium substrate makers such as Ibidien and Unimicron. There is a growing trend to use those machines in the substrate process as it can improve IC and substrate (for 3D architecture) assembly yield significantly.

NEXX currently only processes with an 8% market share, per Gartner. Looking forward, we expect NEXX to benefit from strong premium substrate makers' capex like Ibidien (4062.JP, covered by Takayuki Naito), Unimicron (3037.TW, covered by Grant Chi) and will drive advanced packaging to continue to grow in the long term. ASMP is also an important hybrid bonding solution provider for foundry customer like TSMC (2330.TW) for heterogenous integration related tools. Their current product is TCB (Thermal Compression Bonding) machines to Intel (covered by Chris Danely) and future to foundry makers.

We rate ASMP as Buy with a TP of HK\$107 based on 26x 2021E EPS. Our Buy recommendation is on a positive view for AP/CIS and Semi Solution, as AP revenue should reach a record high level in the next few years driven by HPC demand, and the recovery of smartphone and spec migration should benefit CIS. We expect ASMP to improve its mix with a margin uptrend in 2021/22E.

Top Buys and Sells

Top Buys

Samsung Electronics

Investment strategy: We rate Samsung Electronics shares as Buy (1). We expect Samsung will be the technology leader in Server DRAM and 3D NAND. Semi earnings should be higher on strong demand from the data-driven computing era, especially from enterprise servers and datacenters. Given its high cash holdings and abundant free cash flow generation, we believe Samsung has scope for higher capital returns, which could be another positive catalyst.

Valuation: Our 12-month target price for Samsung of W86,000 is derived using a sum-of-the-parts (SOTP) methodology, based on 2021E EBITDA. In calculating total operating value, we reference global peers in assigning fair-value EV/EBITDA multiples for the four main divisions (7.5x for Semiconductor, 3.6x for Display panel, 8.4x for Mobile and 4.5x for Consumer Electronics). On the non-operating side, we use 2Q20A book value of equity-method investment assets. The 7.5x EV/EBITDA multiple for Semiconductors (W331 EV) represents a 20% discount to the average target price-implied multiple of global semiconductor peers given Samsung's memory business' earnings volatility (vs. foundry players' superior/consistent earnings profile). We use a 3.6x multiple for Display panels (W40tr EV), which is a 10% premium to our TP-implied EV/EBITDA multiple for LG Display (3.3x) given Samsung's dominant market position in the mobile OLED panel market (80%+ market share). The 8.4x target multiple for Mobile (W99tr) represents a 60% discount to target price-implied multiple for Apple, given near-term high-end product cycle visibility under limited Operating System (OS) and ecosystem capability. For the Consumer Electronics division (W23tr), we apply a 40% discount to the average Bloomberg consensus multiple for global peers (7.4x) given the division's recent weak earnings momentum. After deriving the enterprise value of each division, we adjust for the entire company's debt/preferred equity and the residual net-equity value per/share to arrive at a TP.

Risks: Downside risks that could prevent the shares from reaching our target price include: 1) PC sales weaken more than our forecast and NAND demand fails to meet our expectations; 2) Aggressive investment by competitors in memory semiconductor/TFT-LCD could have a negative impact on prices; 3) Competition in the handset market intensifies, reducing SEC's handset margin; 4) Any major appreciation of the won would hit SEC's earnings; and 5) Greater-than-expected impact of COVID-19.

TSMC

Investment strategy: We rate TSMC shares as Buy. We believe that Intel's delay in 10nm and GF's halt in leading-edge node development reduce TSMC's competition and could mean more share gains for TSMC long-term. Competition from Samsung exists, but the impact should be less than what the market is expecting. The company, meanwhile, is confident of achieving the high end of its 5-10% revenue CAGR target for the upcoming five years thanks to a double-digit % ramp from HPC, IoT and automotive, and low to mid-single-digit % smartphone growth. CPU outsourcing to TSMC offers further growth upside. A rising cash dividend should also support the share price.

While TSMC has been increasing capex spending meaningfully since 2009, the cost structure is well maintained through continuous product mix improvement, efficiency enhancement and cost reduction. TSMC's operating level breakeven utilization is well maintained at around 35-38% of utilization. This means that TSMC would be still profitable even under our bear-case scenario assumption.

Valuation: Our DCF-based target price for TSMC is NT\$561, which translates to a P/E of 26x 2021E EPS and P/B of 7.8x 2021E BVPS. Factoring in a 1.39% risk-free rate, 7% risk premium, and 0.94 beta, we derive a WACC of 7.9% for our DCF model. We estimate 9% long-term revenue growth from 2023E and a gradual decline to mid-single-digits, compared to TSMC's forecast of long-term semiconductor foundry industry growth of mid-single-digit percentage. We assume a long-term EBIT margin to gradually decline to 36%. In our view, DCF is a good metric to value TSMC as it has been generating stable free cash flow from its operations.

Risks: Key downside risks that could impede the shares from achieving our target price include: 1) global semiconductor market weakness; 2) larger-than-expected margin contraction due to depreciation cost hikes; 3) increased competition from Globalfoundries, Samsung and Intel stepping into the foundry business; 4) longer-than-expected supply chain inventory digestion; and 5) macro impact from demand slowdowns amid the worldwide coronavirus outbreak.

Lam Research Corp

Investment strategy: We are Buy rated on LRCX as our top memory equipment pick and expect stock to outperform heading out of a memory bottom in 4Q20 given its outsized memory sales exposure.

Valuation: We value LRCX at \$420 using 17.5x P/E multiple on CY22E EPS of ~\$24. We view a 17.5x multiple vs Lam's 3-year average multiple of 13x as appropriate given higher services or 1/3rd of total sales contribution.

Risks: The key downside risks to our investment thesis and target price on LRCX include: 1) increasing competition in deposition and etch from Tokyo Electron and Applied Materials; 2) weaker-than-expected overall semi market demand, especially memory; 3) Slower than expected demand in China due to US-China trade and IP tensions.

Tokyo Electron

Investment strategy: We rate Tokyo Electron Buy (1), with a target price of ¥32,000. One of Japan's leading SPE manufacturers, TEL ranks third (alongside Lam Research) on a global scale, after Applied Materials (AMAT) and ASML. TEL had been preparing to merge with US firm AMAT from September 2013 through end-April 2015, but the merger plan was scrapped on April 27, 2015, and subsequently it has been seeking out a growth scenario on its own. In a global context, we believe TEL rivals the likes of Applied Materials and Lam Research.

TEL also actively returns profit to shareholders. As well as maintaining a 50% payout ratio, with dividend payments closely linked to profit, it maintains a flexible and bold approach to buybacks, spending ¥105.5bn in April–November 2015 and ¥150bn in May–December 2019 on buyback campaigns, for instance. If the share price adjusts in 2020 and out, we think TEL could again repurchase shares.

Valuation: Our ¥32,000 target price corresponds to an FY3/22E PBR of 4.6x. In periods of order growth, TEL's PBR has been 50%-250% above the market average but the market consensus peaked in spring 2018 and then corrected. It bottomed in 2019, though, and the outlook is again on a recovery track. In setting our target PBR, we reference the improvement in SPE earnings momentum and the PBR levels prevailing when the equity market has been envisaging a WFE market of around the same size as the current one. Our target price equates to an FY3/22E PER of 21x.

Risks: Risks that the share price might diverge from our target price on the downside include the following: 1) the global economy could slow down again, with fears emerging of reduced ardor for semiconductor capex, 2) new products from competitors substantially outperform TEL products, 3) the facility acquisition plans of major overseas customers could be changed to the disadvantage of TEL, 4) the R&D burden for EUV could be heavier than expected and investors expected rates of return over the longer run could fall, and 5) the emergence of negative impact on equipment demand if US-China trade friction spreads.

On the other hand upside risks include 1) semiconductor capex ardor recovering and increasing against a backdrop of a global economy accelerating faster than expected, 2) improved prospects for market share growth in areas such as etchers and cleaning equipment (including changes of strategy by competitors), 3) an increase in the number of cutting-edge semiconductor production processes that use equipment supplied by TEL, 4) clearer prospects for capex budget increases by major semiconductor makers, including makers in China, and 5) a dramatic enhancement in shareholder returns through active buybacks.

Entegris Inc

Investment strategy: We are Buy rated on Entegris. We view the stock as the best defensive play heading into macro uncertainty. Fundamentally, we expect to see limited cuts to wafer starts as utilization rates remain high at semiconductor manufacturers. Additionally, Entegris is benefiting from SAM expansion, market share gains, and revenue accretion from recent acquisitions which are helping to drive top line growth nearly double industry wafer start expectations.

Valuation: We value ENTG at 28x P/E on C22 EPS, yielding a target price of \$92. We continue to value ENTG above its 3-year average P/E of 17x. We choose to value it above its 3-year average as we believe the average multiple included a discount for equipment exposure and the new shareholder base views Entegris as a more quality specialty chemicals company with solid growth potential, thus a more favorable multiple akin to diversified semiconductor companies is appropriate.

Risks: Risk factors include: 1) ENTG derives the majority of its revenue from the highly cyclical semiconductor industry, and has exposure to other volatile markets such as flat panel display. Any unexpected drop in semiconductor demand or delays/cancellations in new fab projects or expansions could significantly lower demand for ENTG's products. 2) As wafer starts, fab utilization, and to a lesser extent, equipment, are closely linked to the stock price, any material differences to our supply/demand model may cause our valuation methodology to be inaccurate (up or down).

Should the risks outlined above not impact the company/or are greater than we anticipate, the shares could exceed/fall below our target price.

ASM Pacific Technology

Investment strategy: We rate ASMPT shares as Buy. ASMPT in recent years has undertaken a restructuring that has created a more balanced product mix to capitalize on key technology trends in 2019-21. ASMPT has a high operating leverage, and we forecast 2019-21E revenue growth and along with OPM expansion will translate to strong profit growth. We believe investors are now looking ahead to the next capex demand cycle driven by 5G-related demand and advanced packaging.

Valuation: P/E is a common valuation methodology the market uses to value technology companies such as ASML. Our target price of HK\$107 for ASML is based on a target P/E of 26x 2021E earnings. Our target multiple of 26x is 0.5stddev above the 5-year average forward P/E. With the semiconductor market looking set to grow from the 5G upgrade cycle and China capex demand, we believe investors will value ASML at a growth mode P/E and believe 26x P/E is not stretched.

Risks: Downside risks that could prevent the shares from reaching our target price include: slower active alignment (AA) equipment outsourcing from camera module makers; slower-than-expected triple camera adoption by smartphones; slower-than-expected semiconductor market recovery; stronger competition; and higher than expected impact from COVID-19.

ASML Holding NV

Investment strategy: Our Buy recommendation on ASML is based on three premises: 1) Faster digital transformation, and in particular the rise of Artificial Intelligence of Things (AIoT), driving increased demand, 2) Higher operational profitability, primarily as EUV matures and its share becomes significant across both systems & installed base management, and 3) Stronger computational platform of semiconductor fabrication leveraging Big Data.

Valuation: We value ASML using DCF reflecting confidence in longer-term earnings power and FCF generation profile. Our DCF-based target price of EUR 380 factors in 2025 top-line of ~EUR 22.5bn (trending ahead of the midpoint of the company's stated scenarios of EUR 15-24bn). We forecast reported gross margin of ~53% and EBIT margin of ~36% in 2025. Our WACC assumption of 7.6% is based on risk-free rate of 0.2%, and equity risk premium of 7.9%. We use terminal FCF growth of 3%.

Risks: We highlight the following risk factors for ASML. If the impact of these risk factors is more or less negative than we anticipate, the share price could deviate significantly from our target price:

Technological: Challenges in development of EUV technology could result in delays and lower margins.

Competition: A gain/loss in lithography and/or process control market share would result in upside/downside risk to our estimates.

Customer Risk: ASML derives significant share of its revenues from three largest customers, and an increase/cut in their capex could result in risk to our estimates.

Macroeconomic: A weak macroeconomic environment and /or escalation in geopolitical tensions resulting in subdued semiconductor growth/increase in cadence could cause downside to our estimates.

Top Sells

SMIC

Investment strategy: With intensified competition, continued R&D expenditure, and SMIC's target of high teens % of revenue growth in 2020E, we expect SMIC to have lower profitability vs peers with drags from the leading edge node contribution. We believe the relatively lower profitability will result in the underperformance on its share price. Accordingly, we rate SMIC as Sell.

Valuation: Our target price for SMIC of HK\$20.3 is based on P/B given our view that the company will generate thin FCF in the near-term. Our TP is based on 1x 2021E P/B, at the 5-year average, due to high utilization in 2020. However, we believe it might need to take a couple of quarters for the company's 4Q20/2021 revenues to gradually adjust to the impact from losing Huawei revenues.

Risks: Key upside risks that could push the stock above our target price include: 1) better than expected margin recovery on efficiency improvements, 2) strong policy support which helps SMIC to improve profit, 3) stronger than expected end-demand resulting in higher than expected earnings.

CMC Materials Inc

Investment strategy: We are Sell rated on CCMP. Weakness on the top line lowers our confidence that CMC can sustain growth relative to other consumable stocks in our coverage which have been raising growth targets and beating topline estimates recently. CMC lost some share in their pads business due to increased competition in Korea and their slurries business which is 43% of their portfolio has been hovering around \$120M/Q since 2018 at the height of the initial conversion to 3D NAND. We view competition and efficiencies in slurry usage as threats for significant growth moving forward. Additionally, uncertainty around the timing of a recovery in oil pipeline business, which is dependent upon increased travel in the US leaves us concerned around the growth opportunity in performance materials in 2021.

Valuation: Our \$140 target price reflects a 19x P/E multiple applied to C22 EPS, below peers due to macro risk in oil business coupled with increased competition and slowing growth in the semis business which are creating revenue and margin headwinds.

Risks: Upside risks to the shares reaching our target price: 1) technology inflections driving premium pricing; and 2) market share gains in pads and engineered surfaces. Downside risks to the shares reaching our target price: 1) weaker-than-anticipated demand; and 2) pricing pressure due to the increasing Moore's law.

Figure 99. Rated Companies Mentioned

Company	Ticker	Mkt Cap		Close	Target	P/E (x)		EV/EBITDA (x)		P/B (x)		Div yield (%)		Debt / equity (%)		
		US\$ (M)	Ccy			Price	Rating	2020	2021	2020	2021	2020	2021	2020	2021	
3M Co	MMM.N	99,479	US\$	172.46	185.00	2	20.1	18.4	13.5	12.8	8.3	7.8	3.4	3.6	197.6	210.4
Air Products and Chemicals	APD.N	60,508	US\$	273.76	302.00	1	32.0	29.1	17.6	16.5	5.0	4.7	2.0	2.0	65.0	75.7
Apple Inc	AAPL.O	2,078,470	US\$	122.25	125.00	1	35.5	30.0	24.7	21.7	33.5	37.8	0.7	0.7	179.6	210.7
Applied Materials	AMAT.O	81,136	US\$	88.84	80.00	1	20.7	18.0	16.0	13.6	7.5	6.4	1.0	1.0	50.0	42.6
ASM Pacific Technology	0522.HK	5,223	HK\$	99.00	107.00	1	45.9	24.0	19.2	13.0	3.3	3.1	1.4	2.1	33.4	26.8
ASML Hldg	ASML.AS	195,197	€	378.30	380.00	1	48.7	39.2	37.8	30.6	11.1	10.2	0.7	0.8	32.6	30.0
CMC Materials Inc	CCMP.O	4,429	US\$	152.29	140.00	3	21.0	22.1	11.6	11.6	4.1	3.6	1.1	1.1	83.4	74.5
Dow Inc	DOW.N	40,833	US\$	55.05	52.00	2	39.4	20.9	9.6	8.9	3.2	3.1	5.1	5.1	119.6	109.4
DuPont de Nemours	DD.N	48,449	US\$	66.02	68.00	1	20.7	19.3	13.1	12.9	1.3	1.2	1.8	1.8	59.9	53.1
Ebara	6361.T	3,186	¥	3,480.0	3,450.0	2	17.4	16.0	5.5	5.2	1.1	1.1	1.7	1.9	34.0	29.2
Entegris Inc	ENTG.O	12,989	US\$	96.22	92.00	1	38.8	34.0	22.8	20.6	9.4	7.4	NA	NA	71.3	33.9
Fujifilm Hldgs	4901.T	21,858	¥	5,695.0	6,800.0	1	17.5	14.6	4.5	3.7	1.1	1.0	1.7	1.9	29.3	24.8
Hitachi	6501.T	37,735	¥	4,065.0	5,600.0	1	11.5	9.9	5.6	5.2	1.2	1.1	2.4	2.3	54.5	52.7
Ibiden	4062.T	6,593	¥	4,915.0	4,500.0	1	36.3	26.7	9.6	6.2	2.4	2.3	0.7	0.7	52.4	48.8
Intel Corp	INTC.O	213,035	US\$	51.99	50.00	2	10.7	12.1	6.2	6.5	2.8	2.3	2.5	2.5	47.0	40.3
JSR	4185.T	5,814	¥	2,818.0	3,000.0	1	44.1	24.7	13.5	10.0	1.5	1.5	2.1	2.4	23.7	22.9
Lam Research	LCRX.O	72,002	US\$	499.98	420.00	1	26.6	22.0	20.2	16.7	12.2	9.3	0.9	0.9	98.0	75.1
LG Display	034220.KS	5,315	₩	16,100	20,000	1	-12.7	42.4	3.8	3.3	0.6	0.6	NA	NA	133.7	109.3
Linde PLC	LIN.N	131,390	US\$	250.62	284.00	1	31.0	27.1	25.0	20.7	2.9	2.9	1.5	1.6	32.8	37.3
Micron Technology	MU.O	81,914	US\$	73.34	35.00	3	25.8	14.4	8.4	6.0	2.0	1.7	NA	NA	16.5	14.4
Samsung Electronics	005930.KS	401,522	₩	72,900	93,000	1	18.6	14.6	5.2	4.3	1.8	1.7	1.9	1.9	7.0	6.5
Shin-Etsu	4063.T	68,971	¥	17,300.0	17,500.0	1	24.1	22.5	11.0	9.7	2.6	2.4	1.4	1.4	0.8	0.6
Semiconductor Manufacturing Int'l (SMIC)	0981.HK	16,168	HK\$	21.75	20.30	3	33.3	NA	13.2	12.3	1.0	1.1	NA	NA	15.9	18.6
Sony	6758.T	114,586	¥	9,675.0	11,300.0	1	15.8	17.5	9.1	8.3	2.6	2.3	0.5	0.6	49.3	48.4
Tokyo Electron	8035.T	55,065	¥	36,890.0	32,000.0	1	27.6	24.6	16.9	15.0	6.1	5.4	1.8	2.0	0.0	0.0
Tokyo Ohka Kogyo	4186.T	2,697	¥	6,770.0	6,300.0	2	26.4	24.1	11.3	10.5	2.0	2.0	2.2	2.0	6.4	5.5
TSMC	2330.TW	472,364	NT\$	514.00	607.00	1	25.7	23.0	14.4	12.1	7.4	7.1	2.1	2.2	11.2	11.8
Unimicron Technology	3037.TW	4,373	NT\$	82.00	135.00	1	33.8	29.6	11.4	9.6	2.8	2.8	1.6	1.8	80.2	81.3
Western Digital	WDC.O	15,745	US\$	51.75	60.00	1	17.1	11.3	10.5	8.0	1.6	1.6	1.9	NA	99.1	96.8

Source: Citi Research, and dataCentral. Financials and ratios are calendar year basis.

Appendix A-1

Analyst Certification

The research analysts primarily responsible for the preparation and content of this research report are either (i) designated by "AC" in the author block or (ii) listed in bold alongside content which is attributable to that analyst. If multiple AC analysts are designated in the author block, each analyst is certifying with respect to the entire research report other than (a) content attributable to another AC certifying analyst listed in bold alongside the content and (b) views expressed solely with respect to a specific issuer which are attributable to another AC certifying analyst identified in the price charts or rating history tables for that issuer shown below. Each of these analysts certify, with respect to the sections of the report for which they are responsible: (1) that the views expressed therein accurately reflect their personal views about each issuer and security referenced and were prepared in an independent manner, including with respect to Citigroup Global Markets Inc. and its affiliates; and (2) no part of the research analyst's compensation was, is, or will be, directly or indirectly, related to the specific recommendations or views expressed by that research analyst in this report.

IMPORTANT DISCLOSURES

Samsung Electronics (005930.KS)

Ratings and Target Price History
Fundamental Research

Analyst: Peter Lee



Date	Rating	Target Price	Closing Price
1 12-Jul-18 07:03:19	1	*78,000.00	45,500.00
2 19-Oct-18 04:21:22	1	*71,000.00	43,900.00
3 31-Oct-18 12:47:42	1	*63,000.00	42,400.00
4 06-Dec-18 11:03:16	1	*58,000.00	40,500.00
5 02-Jan-19 07:57:56	1	*56,000.00	38,750.00
6 30-May-19 08:48:34	1	*58,000.00	42,550.00
7 24-Oct-19 09:03:00	1	*65,000.00	50,700.00
8 06-Dec-19 05:24:47	1	*68,000.00	50,400.00

Date	Rating	Target Price	Closing Price
9 19-Dec-19 01:58:29	1	*70,000.00	56,000.00
10 31-Dec-19 08:47:29	1	*71,000.00	55,800.00
11 08-Jan-20 05:23:35	1	*72,000.00	56,800.00
12 18-Feb-20 03:44:42	1	*77,000.00	59,800.00
13 16-Mar-20 10:38:53	1	*75,000.00	48,900.00
14 24-Mar-20 08:59:53	1	*70,000.00	46,950.00
15 29-Apr-20 09:22:37	1	*68,000.00	50,000.00
16 25-Jun-20 15:35:46	1	*70,000.00	51,900.00

Date	Rating	Target Price	Closing Price
17 06-Jul-20 05:08:44	1	*75,000.00	55,000.00
18 13-Jul-20 15:55:44	1	*76,000.00	53,400.00
19 09-Sep-20 09:29:05	1	*80,000.00	58,400.00
20 11-Sep-20 03:24:04	1	*82,000.00	59,000.00
21 18-Sep-20 06:21:08	1	*83,000.00	59,300.00
22 08-Oct-20 08:03:09	1	*86,000.00	59,700.00
23 03-Dec-20 14:20:08	1	*93,000.00	69,700.00

*Indicates Change

Rating/target price changes above reflect Eastern Time

Samsung Electronics (005930.KS)

Catalyst Watch Research

Analyst: Peter Lee



Date	Expected Direction	Duration	Action	Closing Price
1 10-Jun-19 03:51:31	Upside	30 Days	Open	4,800.00
2 10-Jul-19 03:29:09	Upside	30 Days	Close	5,550.00

Date	Expected Direction	Duration	Action	Closing Price
3 13-Jul-20 15:55:44	Upside	30 Days	Open	6,400.00
4 13-Aug-20 03:23:24	Upside	30 Days	Close	7,000.00

Date	Expected Direction	Duration	Action	Closing Price
5 19-Nov-20 04:25:35	Upside	30 Days	Open	6,600.00

Rating/target price changes above reflect Eastern Time

Due to Citi's involvement in the tender offer by HKE Holdings G.K. for the common shares of Hitachi Kokusai Electric Inc., a consolidated subsidiary of Hitachi, Ltd. ("the Company"), Citi Research restricted publication of new research reports, and suspended the Company's ratings and target prices on April 26, 2017 ("the Suspension Date"). Please note that the Company price chart available on Citi Research's disclosure website does not reflect that Citi Research did not have a rating or target price between the Suspension Date and February 21, 2018, when Citi Research resumed full coverage.

Citigroup Global Markets Inc is advising KKR Japan on the announced sale of Hitachi Kokusai to Applied Materials.

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Unless stated otherwise neither the Research Analyst nor any member of their team has viewed the material operations of the Companies for which an investment view has been provided within the past 12 months.

Within the previous 12 months, Jim Suva, CPA, Analyst, and/or members of their team have viewed the material operations of Apple, Inc., Western Digital and were not reimbursed by the company for expenses associated with the visit.

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Data current as of 30 Sep 2020	12 Month Rating			Catalyst Watch		
	Buy	Hold	Sell	Buy	Hold	Sell
Citi Research Global Fundamental Coverage	55%	34%	11%	22%	68%	9%
<i>% of companies in each rating category that are investment banking clients</i>	65%	62%	59%	68%	62%	68%

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Risk rating takes into account both price volatility and fundamental criteria. Stocks will either have no risk rating or a High risk rating assigned.

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