

# Global Semiconductors

## Highlights From Expert Call On NVDA + Data Center Compute Landscape; Transcript Inside

### Equities

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### Conference call highlights

We hosted a call with Pete Foley, President and CEO at Ascenium and former founder and CEO of Wave Computing. Our conversation focused on the importance of NVDA's software moat including MLNX acquisition, Ampere/A100, and virtualized GPUs. Highlights from the transcript are included below and a replay is available at +1 (888) 286-8010 (code: 166120891) until 07/02/2020.

### Key takeaways from expert calls

Ampere (826mm<sup>2</sup>, monolithic die, TSMC 7nm w/o EUV) is a game changer for several reasons. First, after some initial heat-related challenges (maybe related to the addition of more high bandwidth memory stacks), NVDA has successfully used its software expertise to virtualize and create unique and separate firewalled resources on the chip to run both training and inference workloads and even though it consumes more power than its processor (400W v Volta 300W), it is 2x more power efficient – a major driver for hyperscalers. Second, the chip is a major step forward in allowing more general purpose processing tasks currently run on Intel Xeon host processors to be addressed by GPUs (e.g. fully autonomous acceleration of Apache Spark, used with Hadoop). Third, Mellanox will enable NVDA to build super-pods of computing capacity such that it could, eventually per our expert, choose to enter the data center business itself. Fourth, NVDA's decision to switch from INTC Xeon to AMD Epyc for DGX was due to INTC's lack of support for PCIe 4.0. Lastly, NVDA's software lead is so substantial it began proposing changes to industry standards for fundamental building blocks like C++. Relative to INTC, Mr. Foley sees the Habana acquisition as a pivot from innovation to execution. Relative to AMD, it continues to struggle to build necessary software infrastructure to effectively compete with NVDA broadly in the data center.

### Our take: Owning the Data Center with Ampere + MLNX + Software Stack

The call bolsters our view that Ampere + Mellanox together with its formidable software capabilities set the stage for NVDA to not only take new workloads, but start to also gain share from current workloads being done on CPU. The call should also quell any investor concerns around competition either from hyperscalers themselves or the myriad of high-profile startups. We remain positive on the stock.

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*We present below highlights from our recent call with Pete Foley, President and CEO at Ascenium and former founder and CEO of Wave Computing. The opinions expressed by Pete Foley herein do not necessarily reflect the views and opinions of UBS. UBS accepts no responsibility for the accuracy, reliability or completeness of the information and will not be liable either directly or indirectly for any loss or damage arising out of the use of this information or any part thereof.*

## **US Semiconductors**

**Moderators: Timothy Arcuri**

**Date: June 9, 2020 11:00am ET**

Timothy                      This is Tim Arcuri. I'm the semiconductor and the semi equipment analyst here at UBS, and we're very pleased to have Pete Foley with us. Pete is currently the CEO of Ascenium which is a Silicon Valley startup developing a new class of high-performance processor which is called an SDP, a software-defined processor. Pete is also an independent consultant in the deep learning and the machine learning spaces.

Prior to Pete's current role, he was the founder and CEO of Wave Computing which is a well-known Silicon Valley startup focused on massively parallel computing for deep learning. So, thanks for joining us, Pete.

Pete                         Good morning, and thank you.

Timothy                      I just wanted to first set the stage here, Pete, a little bit. You spent a long time in this industry building companies in the processor and the accelerated compute sectors. So, I just wanted to focus first on Nvidia. When you look at Nvidia and you try to compete with what they're doing, can you just walk through sort of what you see as the core elements of their competitive moat?

Pete                         Yes, it's actually multidimensional which makes them quite a force in the industry. I call them the freight train of the industry when it comes to accelerators. They hold 90%-plus of the accelerator market, and a lot of it has to do with their long history first as an accelerator graphics processor company. So, they have built tremendous experience stabbing chips, building large die, and

learning how to yield large chips. Then, of course, building really close relationships to the key foundries such as TSMC, and that pays huge dividends over the long term.

With regards to deep learning, it really goes back to 2002 when they made investments at Stanford in what became CUDA. CUDA now is almost 20 years old, and that points to the software moat that they have built in terms of massive tools, suites, mature tool suites, large numbers, tens of thousands of developers that program and are very fluent in their tool suites.

It's more than that. I think it's a real focus by the company on the software stack and the software side realizing how critical that is to market acceptance and adoption and how that creates very sticky, soft sockets and how it makes it difficult for new entries to break into the market just as Intel has a very sticky socket with the host processor.

There's a lot of focus on that. Starting several years ago, almost three years ago on the datacenter and all the virtualization tasks that you need to deal with in order to be a real datacenter player, especially in the hyperscalers, the cloud service providers, and that goes to being able to snapshot processes that are live and move them around the datacenter.

It has to do with reliability which they addressed in a recent announcement, just hosting or handling containerized operating system operation, virtualized provisioning. All those types of very important but seemingly perhaps subtle to new startups software focused. That's just on the software side.

Of course, for deep learning, this huge focus on compatibility with existing frameworks such as TensorFlow, building stacks both for the datacenter as well as mobile as well as Xavier for automotive is a big focus of theirs.

They've even gotten to the point where they're proposing modifications to the International Standards Committee to make changes to C, the main language that everybody

uses, in order to provide constructs needed to optimize performance for their processors. In the case of C it was some sort asynchronous barrier construct that they wanted added to C++20.

So, everywhere you look, they just seem like a phenomenal execution machine. They really have, I think, a focus on the right approach. Now, granted, there's some optimal aspects to the fact that they do come from the graphics world, and the original processors were streaming processors designed to render graphics images, three-dimensional images, so there's baggage there, and the streaming processor wasn't really kind of a general purpose focused, which is what they needed really to address deep learning workloads.

Generation after generation here, they make modifications, they improve, they make it more general purpose. They add more on chip memory. They make it more flexible. They add more data types so they can make it more efficient for doing inference with less precise operating types. I just sort of see this relentless march which makes it very tough for the incumbents, for new entrants like Groq or Graphcore or Cerebras or others or Wave even to break in.

Really, to my knowledge, no one really has made a significant dent other than Nvidia. I know that a lot of the large hyperscalers would love to see someone other than Nvidia, and you can understand why just because competition is good, but nothing to my knowledge has really made a dent.

I mean, some of the new players have pilot efforts and are maybe shipping to some degree, but you'll find in general that they're very workload-focused, so certain processors like Cerebras or Graphcore will work for certain workloads but really aren't nearly as broad as the kinds of workloads that surely the Ampere or the Volta or the T4, the recent announcements from Nvidia can address.

I can talk a little bit about the recent A100. I think it's important since it was just announced by Jensen. I don't know if any of you in the audience had a chance to watch his keynote. It's pretty well done. He's quite the showman. He did it from his kitchen given the lockdown

here, and he was pulling hardware out of oven behind him, so he would say, “These are hot out of the oven,” kind of tongue in cheek there.

It’s been three years since the announcement of the Volta, and this chip is even bigger than the Volta which I didn’t even think was possible. It’s 826 square millimeters, which if you’re in the chip business, that’s what we call the aircraft-sized die. They figured how to yield these things which is just real mind blowing.

It’s a testament to them, but they are a couple quarters later with this part, and the part is hotter than I know they would have liked. There’s a 400-watt part which means they cannot ship standard PCI graphics cards with it because it’s just too big, too hot, and they had to slow it down some. They had to lower the clock, and they had to make part of the chip go dark which means not power it in order to stay within their thermal envelope.

So, even someone like Nvidia can run into problems with these massive chips with 50 billion-plus transistors in bleeding-edge processes where you never know quite how much power it can draw until you build it.

If anybody can get it fixed and get it working, they can, and I expect this part is focused on deep learning. They want to both unify training and inference in the same part. Now, that’s quite a trick, and they’ve made some efforts to deal with that by virtualizing the actual resources on the chip so that you can run many different work threads or load threads through the chip simultaneously so that it can be provisioned to look as if it’s seven or eight instances of a GPU, so the cloud service providers can provide this virtual appearance to the users.

They’ve done a good job with the recent chip creating these instances, what they call—I think they call it MIG for multiple instance graphics or something. The key thing is they’ve actually on the die created unique separate kind of firewalled resources so that one task or one thread from one user cannot interfere with another.

So, that kind of attention to what is required in order to satisfy the needs of hyperscalers and CFPs is a big focus

of theirs. Very tough for a startup to match all the requirements, the software stack, the compatibility with the existing frameworks, the focus on the hyperscalers needs, the provisioning, Kubernetes, all these containerized, virtualized software aspects.

So, before I blather on, do you have any questions for me? I could talk a bit about the actual new features of Ampere which I think are fairly impressive and different and worth note, but before I do that, I thought I'd stop and see if you had any questions.

Timothy

I do. You're hitting on some things that I wanted to ask later, but since you're on a roll here on Ampere, why don't you just go on that? That'd be great to hear.

Pete

Okay, fine. So, as I said, it's kind of a do-everything chip. They're trying to mix both training and inference. It's really focused on training initially, and a lot of that had to do with the fact that graphics processors since they had to render three-dimensional graphics had to have floating point or otherwise you'd get artifacts in the rendering process.

It just so happened that Nvidia came along. They had this CUDA thing that was just nascent. They had the ability to do floating points, and they had a lot of experience, and this is something that's underestimated. They learned in a high-performance computing market, and this was before deeper [indiscernible - 11:20] in 2014 when Sanit Gupta [ph] got Jensen to pivot to deep learning. They were already in the high-performance computing market, and they were learning how to interconnect multiple GPUs together to work on really large jobs.

To do that, they created this NV link, high-performance communications link between the die. They can connect 8 to 16 of these things in these complex, three-dimensional toroidal topologies and get them all to cooperate on even bigger jobs. So, they carried and they learned how to do this in the high-performance computing market. They carried that all forward now into the deep learning market.

So, this chip is 7 nanometer. It's not EUV which I thought was really interesting. It doesn't use these

advanced light sources from ASML, and that may be one of the problems as to why it got hot, but obviously they were looking to save some money.

It's not a graphics part, so for them to have a graphics part, they need ray tracing now, so what I think you'll see is a focus on fixing the power issues, and they'll re-release this part with ray tracing and probably some of the advance floating point acceleration turned off since that's really only needed for the high-performance compute market, and that will be probably a new version of this part you'll see coming out for graphics.

Even though it is three years old, it is still the gold standard. It is the chip that everyone else chasing this market compares against. Some of the competitors claim for certain workloads and certain network types that they can be better or they can be more power-efficient. This latest offering pretty much blows those all out of the water. There's really nobody better right now, and they're shipping now.

So, they've learned that deep learning, unlike graphics, requires a lot of memory, especially training. So, they made some of the on-chip caches which are fast buffers of memory, seven times larger in this part than Volta, and they did active compression to make them appear virtually even larger.

That may be some place where they got into power trouble because memories leak. A term that's used in the industry is they leak. They burn power when they're not doing anything. So, it'd be interesting to know how much of the 400 watts they burn is leakage power as opposed to active power. That's probably proprietary.

So, they've increased a number of high bandwidth memory stacks. They talk to six right now which provides huge external memory bandwidth, and I think their bet is that by adding lots of SaaS on-chip memory very close and being able to talk to high bandwidth memory that that's going to be a better approach than trying to do wafer scale where you're trying to communicate across a very large wafer.

There's a thing called tyranny of distance in deep submicron where the memory assistance is so high at the geometries that it takes a long time to propagate signals any distance, so even though you're trying to put everything, for example, on a single wafer as Cerebras does, I don't think that performs as well as an approach where using these fast HPM stacks or where you go to optical interconnect between the chip and the next level memory.

I think that's going to be probably something you'll see from Nvidia in the near future. Even three years ago, at GDC Conference, Bill Dali [ph] was talking a lot about optical interconnect, and I think you'll see them doing that to reduce the power and to increase the bandwidth to near memory off-chip.

A couple things I thought were really important and something that I think should really—Intel is probably quite nervous about this is they announced full autonomous accelerate of Apache Spark using Rapids. Rapids is their analytics platform. That's a big deal because Apache Spark which everyone uses with Hadoop which is desegregation of sharding of data and doing a bunch of processing and then unifying everything back up.

That has previously been the domain of only Xeon host processors in the datacenters, and a lot of work is done using Apache spark, so you're starting to see Nvidia putting the software effort to make more general purpose processing tasks in the datacenter be acceleratable by their stuff.

He announced in his keynote that they can now accelerate PageRank, and that's a big task for datacenters, by 13X at 175<sup>th</sup> the costs using their new DGX A100. So, that's something I should mention is once they learn how to interconnect all these parts together using these toroidal interconnect topologies they announced DGX with the V100 which is this chassis that has 8 or 16 of these chips in it, and the new DGX A100 is selling for \$200,000.

It has 8 of these A100 chips in it, and it's a tour de force of packaging, and the engineering that's gone into this thing is just mind blowing. They have gone OCP which is open compute platform compatible, so they're in line with



Microsoft and Facebook are doing in terms of using kind of standardized hardware consortium and requirements and specifications which I thought was a very smart thing to do.

So, I mean, it's really focusing on the requirement to make AI as a service which is something the cloud service providers wanted to do. They virtualized the PCIe connections. Something that I think is interesting, too, is they're using EPYC now. They're using the AMD processor as the host processor for this DGX server chassis, and AMD capitalized on Intel's stumbling with their process and used TSMC's advanced process as 7 and 5 nanometer, and that actually gives them an advantage over Intel, although Intel is now catching up pretty quick.

For a window, at least of a year or two, the AMD processors are faster, and the EPYC supports PCIe gen 4 which, believe it or not, Xeon does not. Since the new A100 Ampere part used gen 4 PCIe and does this root virtualization technology which is all about creating AI as a service for these cloud service providers and virtualizing everything, they went with AMD. That's another thing that's not good for Intel, but good for AMD and Nvidia.

So, they've done something else which is really interesting. One of the analysts, I think it's Linley, called it they bend reality to their will, Jensen does, where a lot of these deep learning networks are sparse. By that I mean the weights for each node in the network can be very small, and these very small weights don't contribute much to the final answer when you're doing training or when you're doing inference.

A lot are small enough that you can just consider them to be zero value and not compute them and save space and save power. The problem is they're randomly located. You don't know where they're going to be in the network and where they're going to be in the memory. So, it's very tough to take advantage of this sparsity.

Well, Nvidia said, "We're just going to define where the sparsity has to be." They call it structured sparsity, so they're going to enforce structured sparsity on everybody else, and everyone's going to learn how to do it and use their tools to do it, and by doing that, they gain a two

times performance advantage. My guess is they'll adopt it.

They also are big enough and have enough weight in the industry where they can create their own new numeric format, so they implemented this thing call TF32 which is the range of 32-bit float, but the precision of 16-bit float.

That means people using the standard frameworks which still want to do everything FP32 which is the standard floating point, they can use this funky 19-bit version that they've created, but it allows them to do more in less power on the chip with very marginal negative effects on the computation result. So, that gives them another factor or two.

That's something to understand about deep learning workloads. You can play games with deep learning because it is a spectastastic process. It's the probabilistic process, so you can change the precision and the accuracy, for example for training, and you'll get to the right answer. It just might take slightly longer to train. If the overall speedup is much larger than the increase of the training time, it's a win. That's exactly what they've done here with this TF32 numeric format. It's definitely not industry standard. It's not an IEEE standard, but you know, they're Nvidia, so they can go ahead and do it.

So, they didn't completely ignore high-performance computing. They doubled the floating points 64, do those people doing oil field simulation or deep space analysis or bioengineering, or whatever, they'll be happy, but when you look at it, in three years, just doubling performance for FP64 is not that impressive, and it shows I think just how much of a lock they have in the industry in terms of high-performance computing in that whole market in general.

So, you see them attacking on many fronts. They didn't need to do all this virtualization work, all this software work. They didn't need to create this new structured sparsity, or they didn't need to compress operands into the caches. They didn't need to do all that to be very successful, but they did, and so that's something that is impressive about the company is that they have very

active research teams. Jensen said there were thousands of people working on the A100 part.

Anything they see that's going to give them an advantage, it gets in there. There just aren't that many players out there that can do that, and so it's really daunting. If you're an entrepreneur, and you want to go attack them, you have to find a niche in the market that's big enough that you can build a more specialized entry and hope to break in. That's tough to do.

Timothy

Great. Thank you for that. Maybe just to follow up, I was going to ask you about sparsity, but you talked about it. I guess I had two questions on that. First of all, sparsity is a pretty general issue that, while difficult to figure out, it's something that in theory, AMD could do as well.

So, one, can you talk about how difficult it will be to replicate what they're doing in respect to sparsity, and two, can you talk about whether or not you think that at some point Jensen has to bring other architectures into the fold? He's GPU, GPU, GPU, and they've really done a great job with that, but at some point do they need to have a new ASIC as well, for example?

Pete

Well, the GPU is pretty much full custom, so that's another barrier to entry, and it's leveraged for many, many years of building graphics chip. In terms of a new architecture, I haven't seen that. What I've seen is some doubling down on the approach they have because there's just so much invested in it, and adding things to it or taking things away that make it better suited for the market, for him to go with some completely different architecture, that might happen if they decide that they're going to go into [indiscernible - 24:33] inference.

I want to go and do the internet of things sort of market, perhaps. Don't see that. They might have to do something to get into the power envelope that the automotive guys want to see, so you might see something there in terms of the next generation Xavier.

They have announced next-generation—I can't remember the name of it off the top of my head. Clearly, they do have a lot of focus on that market, but if they want to go

do drones, or they want to go do automotive, they have to hit a power envelope that they've not really had to for graphics and deep learning markets, especially in the datacenter.

What else—what was your question?

Timothy

I was just asking, sparsity, how difficult it would be—

Peter

Sparsity, no it's not a deeply proprietary thing. It's just something that was well executed, so if you want to implement sparsity you have to think of it in kind of a holistic way that affects both the hardware and the software. Certainly, other players can do it. It will just take effort and time.

Some claim they do it; I'm not sure how. This was an approach that said I have a certain architecture. I have a certain way of doing things, and to make sparsity work for me, I'm going to have to structure it, so here we go. Other players probably take an approach that's not the same type of approach, but still take advantage of sparsity.

For Jensen, if he were to do that, then he would have to give up some other type software performance or have to change larger aspects of his architecture. You should not underestimate the ability to leverage the high volumes they have in the graphics market in order to get pricing and attention from the foundry and get pricing for these large die which probably no one else can get.

Jensen can call up TSMC and say, "Hey, I'll give you 300 million graphics parts, and you give me a bunch of Volta parts for \$1,000 each," or whatever the deal might have been. "They will be a loss market for me into the datacenter market, and I'm going to go ahead and do that, but I'll just leverage my huge volume in graphics." Everybody nods and says yes, sir, and it gets done.

That's just not something you can do as a Google or a Groq or Graphcore. So, these kinds of things really do matter. He said in his keynote that he got a 7 nanometer process that was tuned for Nvidia's needs. It's like wow.

Basically nobody can get TSMC to do anything for them except maybe Qualcomm and Apple and Nvidia.

Now, you may argue that Cerebras got Nvidia to draw metal between gi [ph] on a wafer to enable this wafer scale product, but that's with 16 nanometer, and 16 nanometer is very rapidly becoming an old process. The difference between 16 and 5 in terms of density is a pretty severe barrier in the market.

So, to get TSMC to do something at a bleeding-edge node for you, which Nvidia probably meant more metal airs and in particular faster metal airs. For somebody who's in the processor business like myself, it's a big deal because TSMC process sucks for building fast processors because they're really optimized for mobile, for cellphone processor-type applications, so the metal is not very fast. It's optimized for density and power and not speed.

So, the IBM power processors and even now what STMicro is offering are better suited for high-performance processors than what TSMC offers for the guys trying to build processors. You'll see that even Intel's process is pretty tuned for the needs of processors. So, if you were take an Intel design and move it over to TSMC, you'd see quite a reduction in performance.

Of course, that's one reason why Intel has a proprietary and keeps it proprietary on fab. Does that answer your question?

Timothy

Yes, it does. Let me just pivot a little bit. That was a great—we could talk about Ampere the whole time, but let me just pivot a little bit to Mellanox. Can you just spend five to ten minutes on what you think Mellanox brings to the table as well?

Pete

That's a great question, and it's really important. What you see now is with the absolute avalanche of data into the datacenters accelerated by 5G and also seeing sensors data coming into the datacenter, there's just simply too much data to compute in the host processor.

You also see rapid increases in bandwidth inside a datacenter in terms of networking speeds, and Mellanox plays a role here. You're also seeing very important new types of memory coming in. It used to be for many years, you had the processor itself and the DRAM next to it. Then, that was it. Then, you had to go out over the network to get the hard disk drive rotating media.

The access time difference between the rotating media and accessing DRAM was 10,000X. Entire architectures and software stacks and everything were all built around this dichotomy in access times and energy required to get that data.

Then, along comes solid-state disk drives as flash, and then along comes Intel with Optane which is a 3D cross point memory which is known as storage class memory. These really throw a rock into the mix and really change things because now you have something that acts like a rotating disk drive, but it's 100 times faster.

So, everything has to adjust to that, and a big part of that is the networking that virtualizes all these resources. So, there's new standard called NVMe-oF which is non-virtualized memory express over fabric. Companies like Fungible are going after this by moving processing out into the switch fabric. They have something called a DPU.

All of this is very attuned toward the types of network switches that you build. You start building smart switches that do part of the workload such as compression, decompression, encryption, decryption, memory allocation, stuff that's known as the datacenter tax. Having access to this networking technology which is what Mellanox does allows Jensen to, I think, become—first off, it helps him make much better and smarter decisions in terms of the designs in the next-generation parts. It allows him to essentially go into the datacenter business if he wants to as well.

He sort of alluded to that in his keynote where he talked about these SuperPods they've created where one of the knocks on Nvidia is well, you know, they can't do much beyond 8 processors. Well, he showed this SuperPod with 140 chassis with 8 processors per chassis, and he casually

mentioned the Saturn V collection of SuperPods, which is apparently [indiscernible - 33:17] to them that they're using internally for design, is now the world's fastest supercomputer which is mind blowing, and he just sort of casually dropped that.

Being able to do that and have the networking technology and know-how is really part and parcel. They're integrated to do these kind of events, to virtualize systems. There's a huge blurring between where the processors are and where the networking is. You really can't do one without the other, and they both have to be intelligent and understand what each and the other can do.

Now, Mellanox has this standard called InfiniBand, so there's still a bit of a war going on whether things are going to Ethernet-based or InfiniBand-based or fiber channel-based, and that has not yet settled out. That's kind of a big deal.

I know, for example, I mentioned Fungible. Fungible uses the Ethernet and not InfiniBand, and it all has to do with latency and predictability. Ethernet is not as predictable as some of these other approaches. So, that will settle out. I'm not really a networking expert, but it's important. You just can't ignore it and still really do a good job in terms of understanding what has to happen with the processors themselves.

I hope that added some color and was useful.

Timothy

It does, yes. I've gotten a couple of inbound questions from investors sort of asking you to dovetail this into Intel. Obviously, based on acquisitions they bought Nervana several years ago, they bought Habana recently who was doing a lot of work with Facebook. Can you just talk about where Intel is relative to what Nvidia is doing, and maybe—

Pete

Sure. Intel has a remarkably unblemished record of failure when it comes to acquisitions. They have a few successes, and they have to really spend big to get them, but Nervana was a failure. They built a bunch of additional parts based on Nervana technology, and it was not competitive in the market. I've heard an insider say

probably in the range of \$3 billion was spent on Nervana, and Nervana spinoff parts.

To make up for that, they had to spend \$2 billion for Habana. That's Avigdor's company. I know Avigdor. I had lunch with him when I was in Tel Aviv, and we talked about this. He's quite a guy, and his model is execute, execute, execute, and that is the Israeli model. They don't really innovate that much. They just execute [on] stuff, and they get to market quick, and they show it works.

So, Intel, I think, learned a lesson from Nervana where Nervana did not have working silicon when they bought them. They were not a force in the market, and they're not going to make that mistake again. They're going to pay what it takes to buy something that actually works. They did that with Altera. They did that with Mobile-I. Those were \$15 billion acquisitions. That's a lot of money, and they also spent \$2 billion for Habana.

I've talked to insiders who are investors in Cerebras and Graphcore who said that Intel paid \$1.4 billion too much. It was really a \$500 million or \$600 million acquisition that they just overpaid for because, well, they need to.

So, Intel has to protect the Xeon socket. It's the main cash cow for the company is the datacenter host processor, so anything that threatens that is an extensional issues for them. So, I think Jensen eating away at them by building the software infrastructure to allow major datacenter host tax, what were host tax, the acceleratable by his stuff, by A100 is an existential threat, and think, and indeed getting access to a process that was faster than what we have doesn't help with EPYC, but I think Intel will catch up there.

So, Intel has just—it's amazing. They brought in—what's his name who came over from Tesla? Jim Keller. Jim Keller is a hell of a guy. Jim Keller went from Apple to Tesla, and he is quite an execution engine. I think with him at the helm, he can be a bit dictatorial, but with him there, I think from an execution standpoint, they'll kind of get their act together.



So, I am a little bit more upbeat on Intel in the next few years with Jim at the helm in terms of execution and kind of figuring out what they need to do, but the past five-plus years have just not been impressive. There's just announcement after announcement of part, and I can go back and give you a litany of them, and they never showed up or they never appeared, or they never had the performance.

It's sad actually given the resources they have, but they still have a monopoly. Monopolies are wonderful, and they're able to take the cache from that and fly and try, and eventually they'll get there. I don't see them as a real threat to Nvidia, that's for sure. They'd like to be, but I just don't see it.

Timothy

Got it. Maybe I could ask you quickly about AMD, and then we can see if there's any questions on the line. AMD, they're the only one that today has discrete CPU and also GPU. How important is that? Obviously, their datacenter GPU business is tiny, but how do you rate their potential success in datacenter for both CPU and GPU?

Pete

AMD is a pretty well-managed company. They have to be because they don't have the depth of cash that some of the other players have. EPYC is a well-executed machine on the deep learning side. They took a different approach than Intel with Vega and the follow-ons where they have separate parts for inference and separate parts for training.

I know from talking to people who have worked with AMD and for AMD that they're really struggling to form the necessary critical mass of software teams to build the necessary software infrastructure. That just gets back to the strength of Nvidia and the legacy of sort of being in this market in the high-performance computing market for 20 years.

It's tough. It's tough to provide the full package in order to be competitive. I am not as familiar, to be straight up, I'm not as familiar with where they are right now versus where Nvidia is, so they could be better positioned than I realize, so I don't want to downplay them too much. I like AMD, they're scrappy. I wish them well in terms of competing against both Intel and Nvidia, but that's really all I can say at the moment.

Timothy                      Great. maybe we can open it up to the lines, and if not, then I can keep on asking questions, but let's open things up and see if anybody else has any questions.

Coordinator                [Operator instructions]. We do have our first question which is coming from Tim Lesch [ph]. Please go ahead. Your line is open.

Tim                            Thank you. Thank you for this call. It's been fascinating. Can you help me understand the implications of the virtualization on the A100? It seems like despite being a high-cost part that their ability to utilize it for multiple and different workloads at the same time can kind of lower the cost per workload versus having a single-purpose type approach.

How important or how game changing is that ability to virtualize the A100? Does it expand the workloads they can address and kind of increase their sort of share of compute in the datacenter? How do you see that playing out?

Pete                           Well, exactly. So, what Nvidia knows how to do is build really large die. Nobody can do it as well as they can. The problem is you don't want to dedicate an 800 square millimeter die to one task, and you're doing that when you're doing ray tracing in a very complex graphics rendering or something like that. There some large, high-performance compute load.

When you're dealing in a datacenter which is the cost service providers want to provision it any way they want, virtualize any way they want, and take all-comers coming in, and so you want to be able to slice and dice your every expensive large part. In order to do that, you need a lot of software support to virtualize that resource.

If you're virtualizing it for training, it's not as important as virtualizing it for inference because for inference, you have many more inference tasks coming in than training tasks, and these tasks are much smaller than training and require much less memory than training. They're not as compute-intensive as training by a large margin.

So, you really want to slice and dice your expensive, large, hot compute resource among hundreds of these inference tasks, and they get this, and they've been working for the last three years to really provide the software infrastructure and the hardware infrastructure on the chip to enable this virtualization. It's not really multithreading. It's even more than that, but this slicing and dicing to support many, many different tasks.

Pulling that off well then makes it tough to compete. To give you an example of another approach, Facebook for a while was taking the approach, "Well, if you guys are doing edge inference, give me the cheapest, smallest, lowest power even using analog compute techniques inference engine, the little, tiny chip." It's called the—the little, tiny board is called M.2 form factor. It's about the size of a thumb drive. "Give me a couple hundred of those, and I'll put that inside a chassis and I'll figure out all the software necessary to make that work."

So, that's a very different approach. That's the polar opposite where many small things, I'll figure out how to make it work, but they're all separate chips and separate boards versus the one, large graphics-based part that has been virtually sliced and diced, and it's done with software.

My bet is on the software. If you can do it in software and virtualize the hardware resource, that's what the computer industry has done for the last 40 years, and if you can do that well, it's tough to beat.

Tim

Thank you.

Coordinator

The next question is coming from Purdeep Rahmani [ph]. Please go ahead. Your line is open.

Purdeep

I had two questions, first on Intel and another one on Mellanox. I guess, given that software is so hard to do, and Intel even their GPU [indiscernible - 45:35] is probably going to come out in 2021, what are your views on their software capabilities and whether they're

spending enough time to even make a dent on Nvidia's software leadership?

The second question on Mellanox is, Mellanox has been a pretty good standard in high-performance computing with their InfiniBand solution. Do you think there are revenue dissynergies here as Mellanox gets absorbed into Nvidia and others balk at using an Nvidia solution per se?

Pete                      Okay, your question on Mellanox, you said something about revenue. I wasn't quite sure what your question was there regarding revenue.

Purdeep                I just said that are Mellanox's revenues to other customers, non-Nvidia customers, jeopardized because they become seen as more of an Nvidia solution after the acquisition?

Pete                      Okay, I got it. With regards to software, Intel does have good software capabilities. They're one of the few players that does, and obviously it's because they've been supporting processors for many years, and they have to build tools, mainly compilers and libraries and so on to support those softwares, and APIs to support graphics and communications and all of those things.

So, they have a very mature software infrastructure for doing all that. Intel is one of the few players that could put together a pretty good software effort, so that's—it's really a question for them of execution and direction and management and intensity, focus, making the right path, executing on that path, executing on time, for something other than processors because they've just been doing the drumbeat of processors for forever.

That's what they're lacking in anything other than their core business, and that's where I think management, something like a Jim Keller, can potentially really help. So, yes, Intel has the software capability, and I would say considerably more so than AMD.

Now, in terms of revenue fall off because of the Mellanox acquisition by Nvidia, you certainly saw this, for example,

when Intel acquired Altera. An awful lot of Altera users switched to Xilinx, so I'm sure Xilinx was thrilled with the acquisition of Altera by Intel. Frankly, I expected to see Intel make Altera reconfigurable technology very close to the processor at the L1 cache level and offer kind of reconfigurable, modifiable instruction sets a la a company called Tensilica.

I thought that was going to be the real value was to merge at a very intimate level this reconfigurable technology with the Intel processors, but it never happened. So, what they're using, the synergy that you thought was going to come between Intel processors and Altera just sort of never happened, and I don't know what their plans are moving forward.

In terms of Mellanox and InfiniBand, that's really a marketing and sales and execution on that side of the business not losing your customers, keeping them happy, keeping them informed about what's coming down the pike. That's a business execution thing largely, I think, and probably there will be some fall off, but there aren't too many other games in town, frankly, other than Mellanox. They had such a dominant market share, and that's one of the reasons they paid—what did they pay, \$15 billion for them or something? No, \$7 billion for Mellanox.

So, yes, time will tell. I don't have a definitive answer for that because I'm not an InfiniBand customer. I think you'd have to go out and survey the customer base to see whether they're loosening the socket to use the term in the valley, or they're nervous about whether they will be supported in the future or whether the direction of the technology will be strictly to support Jensen's wishes and needs as opposed to the needs of a broader audience. That's tough to answer.

Coordinator

The next question is coming from Mike Trexa [ph]. Please go ahead.

Mike

Hi. Thanks for taking this call. I just wanted to talk about TCO savings. How should we think about the magnitude of TCO savings for the A100 that TSTs are seeing? Is this just absolutely a no brainer like a rip and refresh, or as

Jensen says, the more you buy, the more you save?  
Thanks.

Pete

Fantastic question. So, TCO drives everything in the datacenter in terms of buying decisions, and it's all about energy efficiency, and being in the processor market, I've actually talked to senior architects of some of the multicore arm chips, and they've said the TCO ROI in the datacenter is so high that if you're 30% faster the CSPs will switch, which is mind blowing if you've been in the silicon business because to break into the silicon business, you need to be three to five times faster than your incumbent competitor, but it's all about energy.

The latest book that came out from Partha and the team at Google, which is a good read by the way, said that 61% of datacenter power is now processor power, and another 18% is DRAM power, and that's really quite a change from even five years ago when it was a lot of power in power provisioning and power management and cooling.

So, the hyperscalers were all getting that part of the equation under control. So, that means that really the only lever to turn left is processor power, and that's the main lever pulling the datacenter because if you can make the processors do your job, whatever task it might be, 10% faster or 20% faster, then the power to the entire datacenter is now 20% more efficient.

So, it's this huge, big lever, and Jensen made a big point about that about they can be more power efficient even though the part itself is higher power than the Volta. He made the point of saying the A100 is two times more power efficient than the V100 for training.

So, that being said, remember Nvidia carries the legacy of the graphics processor and that architecture, and so when you start looking at the microarchitecture of Nvidia's GPUs, and there's a company called Citadel that has really great microarchitecture teardowns if you're interested, you understand that there's an enormous amount of instruction state that's kind of hidden and under the covers.

That's one of the reasons why the GPUs have been so power hungry over the years is there really is a huge

amount of instructions state in there to sort of make them general purpose.

So, that's makes Nvidia vulnerable in a power cycle. So, somebody like a Groq or one of these other competitors can say, "Hey, look, I can do inference on a virtualized basis. I can handle hundreds of threads in the datacenter, and I have the software to seamlessly fit into the datacenter and migrate by tasks and deal with reliability and provisioning and all that stuff I can do all that, and I can be 30% more power efficient or 50% more power efficient than Nvidia."

Then, for that task, Nvidia is vulnerable because it's really all about power in the datacenter long term, so the purchasing decisions are driven, to a large extent, by power. If you're the only game in town, and you have to be water-cooled, well dammit, we'll put it into the datacenter.

Not only is it power, but if it's something that's different in terms of how the datacenter has to support it. So, datacenters don't like water-cooling that much because that's a special siloed area. They like everything to be homogenous, everything to be completely interchangeable, and sort of the Facebook model. The others are adopting it, and that's one of the reasons why OCP is so popular because it homogenizes everything and gets to the lower possible cost denominator.

Does that help?

Mike

Yes. That helps. Then, I guess, just in terms of access, it sounds like Nvidia is much more power efficient. People would want to switch to this right away, the A100.

Pete

Yes, for the task that the A100 is going to be used for, if it's more power efficient, yes, it's a very compelling case to do that because the power savings can rapidly dominate the upfront capital equipment expenditure to buy the new parts and install them much more so than almost any other business. You just didn't see this in the desktop CPU business or laptops or other things, but it's just in the datacenter, it's a whole different universe.

You really have to think of the datacenter as one giant computer, and there's more and more thinking and papers coming out along that line. There's this holistic thing, and power becomes a very, very important part of it.

Mike Thanks.

Pete Sure.

Coordinator We do not have any other questions in the queue.

Timothy Great. Maybe let me just ask one last question, Pete. So, can you talk just to that point about some of the internal silicon effort at some of the big datacenter and hyperscale guys themselves? Talk about PPU. What's that trying to solve, and how much of the workload that A100 is going after can be bitten off by these captives or work efforts?

Pete Good point. So, the PPU was originally an effort by Jonathan Ross and the guys that are now over at Groq, and these are software guys. The PPU was kind of an inflexible thing that the first generation PPU was not very useful. It didn't have floating points, for example. It was an integer thing, which they carried with them to Groq, by the way.

So, then they brought in some sort of real architects and the hardware guys, and the second-generation PPU was a floating point-based engine, but when you have Dave Patterson and Norm Jouppi in there, they're workload analysis types. So, their model has been for many years to take a look at the workload that you have, and standing here right by Google, they have tremendous visibility as the world's best workloads.

They built PPU2, and actually that proved to be not that popular because it is somewhat inflexible and hard to use. It's not that programmable for general purpose as Nvidia's GPUs. Nonetheless, because it's captive, Google has continued on with them and are using them internally, but they're just not that easy to use because it's this workload



analysis, let's build a specialized architecture focusing on that workload.

The key observation there is that the industry is so young, and deep learning is evolving so rapidly. The algorithms are changing, the data types are changing, the network sizes are changing, the training approaches are changing, so if you can't adapt to that, you're going to be in trouble. This is an issue, I think with Graphcore and the GPU. Graphcore made the decision they're going to move all the memory on-chip as opposed to off-chip. Well, that may not work if things change, and suddenly you need a lot more memory than you thought.

That's a good point is the more general purpose flexible approaches have been winning, and that is the GPU is one of those. Until the industry really settles, until the technology really matures to the point where you can put a stake in the ground and say okay, this is the way it's going to be done for the next five years, and I can build a specialized ASIC to do that, and this ASIC is going to be unbeatable in terms of power performance, but you just have to make sure you don't miss the mark and suddenly find yourself orphaned.

Now, AWS is an interesting case in point because they acquired Annapurna. That's another big door company, by the way, tee off of Habana, and they're all about execution, and they're really good at execution, so they've become the internal silicon team at Amazon. I don't know if it's going to continue to support them simply because they want to have that internal silicon capability, and they've built a multicore arm processor that is no faster than Xeon, but it's a little cheaper, and they did it themselves, so they're going to continue to use it internally.

So, you will see that. You will see them continue their own silicon effort. I understand Microsoft is off building silicon as well. The big guys can do that. Whether they're really be innovative enough to out-manuever startups or have enough of a kind of a freight train kind of presence the way Nvidia does to displace them in the market other than their internal captive datacenters is, I think, unlikely.

Timothy                      Got it, Pete. Well, we are over our time here. I really so much appreciate the time. I thought it was super, super interesting. We're going to wrap it up here, but I just wanted to say thank you, Pete, again.

Pete                          You're welcome. I appreciate it. Thank you, everyone, for attending. It was a pleasure.

*[END OF CALL]*

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Buy	FSR is > 6% above the MRA.	48%	32%
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Company Name	Reuters	12-month rating	Short-term rating	Price	Price date
<b>NVIDIA Corp</b> <sup>13, 16</sup>	NVDA.O	Buy	N/A	US\$351.85	11 Jun 2020

Source: UBS. All prices as of local market close.

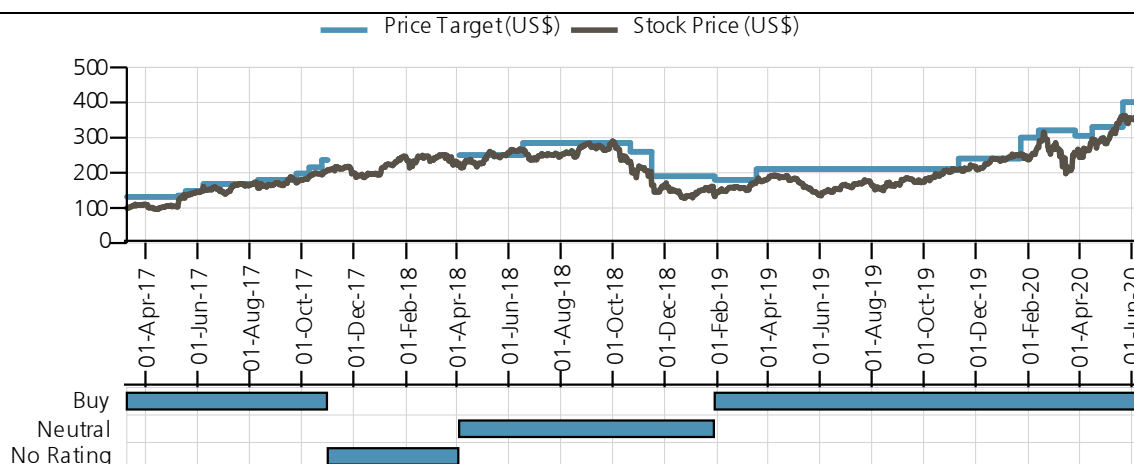
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### NVIDIA Corp (US\$)



Date	Stock Price (US\$)	Price Target (US\$)	Rating
2017-03-10	99.12	132.0	Buy
2017-05-09	102.94	135.0	Buy
2017-05-18	133.07	148.0	Buy
2017-06-08	159.94	168.0	Buy
2017-08-11	155.96	180.0	Buy
2017-09-25	171.0	198.0	Buy
2017-10-10	188.93	215.0	Buy
2017-10-25	193.66	236.0	Buy
2017-11-01	207.2	-	No Rating
2018-04-04	226.24	250.0	Neutral
2018-06-18	265.09	285.0	Neutral
2018-10-22	231.22	260.0	Neutral
2018-11-16	164.43	190.0	Neutral
2019-01-29	131.6	180.0	Buy
2019-03-19	175.71	210.0	Buy
2019-11-11	208.18	240.0	Buy
2020-01-23	252.86	300.0	Buy
2020-02-13	270.78	320.0	Buy
2020-03-27	252.73	305.0	Buy
2020-04-16	294.7	330.0	Buy
2020-05-22	361.05	400.0	Buy

Source: UBS; as of 11 Jun 2020

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