03-vivado

1. Pinout table

SW0-15 připojeny pomocí 10K rezistorů

SW	pin
SW0	J15
SW1	L16
SW2	M13
SW3	R15
SW4	R17
SW5	T18
SW6	U18
SW7	R13
SW8	T8
SW9	U8

SW	pin
SW10	R16
SW11	T13
SW12	H6
SW13	U12
SW14	U11
SW15	V10

LED0-15 připojeny pomocí 330R rezistorů

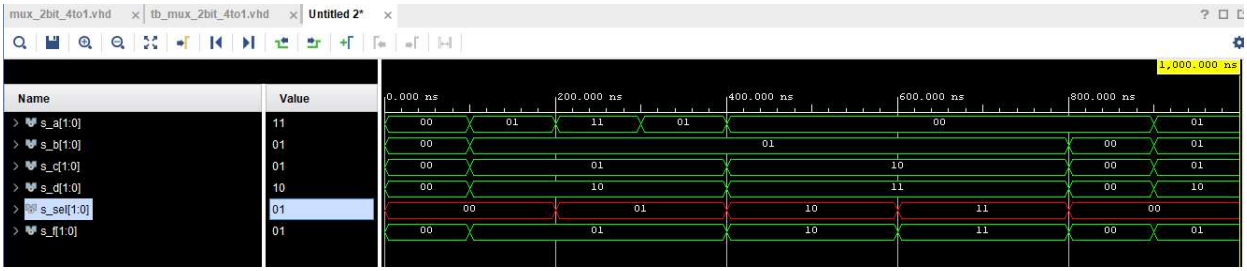
LED	pin
LED0	H17
LED1	K15
LED2	J13
LED3	N14
LED4	R18
LED5	V17
LED6	U17
LED7	U16
LED8	V16
LED9	T16
LED10	U14
LED11	T16
LED12	V15
LED13	V14
LED14	V12
LED15	V11

2. 2Bit 4to1 multiplexer

```
--mux_2bit_4to1.vhd

architecture Behavioral of mux_2bit_4to1 is

begin
    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end Behavioral;
```

```
--tb_mux_2bit_4to1.vhd

 p_stimulus : process
    begin
        -- Report a note at the begining of stimulus process
        report "Stimulus process started" severity note;

        -- First test values
        s_d <= "00"; s_c <= "00"; s_b <= "00"; s_a <= "00";
        s_sel <= "00";  wait for 100 ns;

        s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "01";
        s_sel <= "00";  wait for 100 ns;

        s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "11";
        s_sel <= "01";  wait for 100 ns;

        s_d <= "10"; s_c <= "01"; s_b <= "01"; s_a <= "01";
        s_sel <= "01";  wait for 100 ns;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "10";  wait for 100 ns;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "10";  wait for 100 ns;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "11";  wait for 100 ns;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "11";  wait for 100 ns;

        -- Report a note at the end of stimulus process
        report "Stimulus process finished" severity note;
    end process p_stimulus;
```

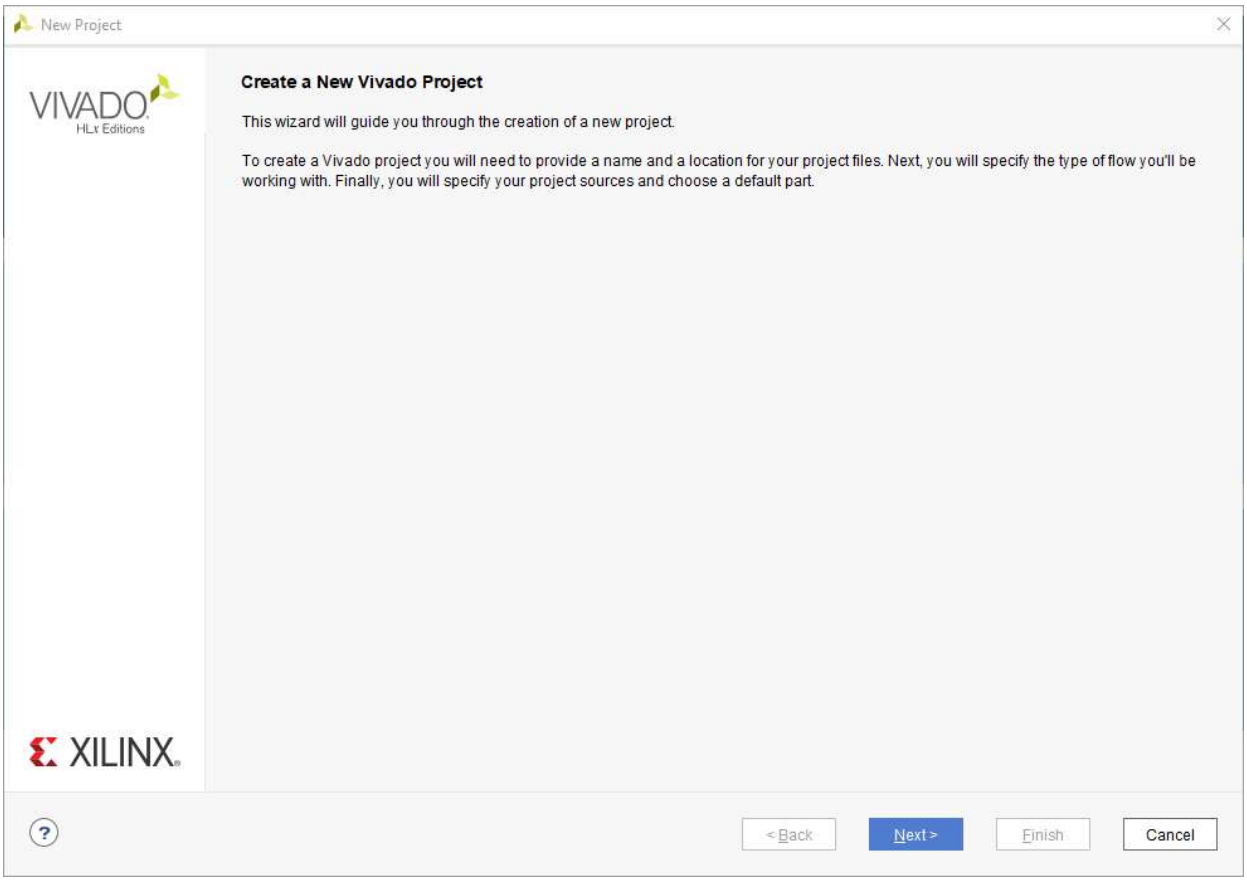
simulation



3. Tutorial

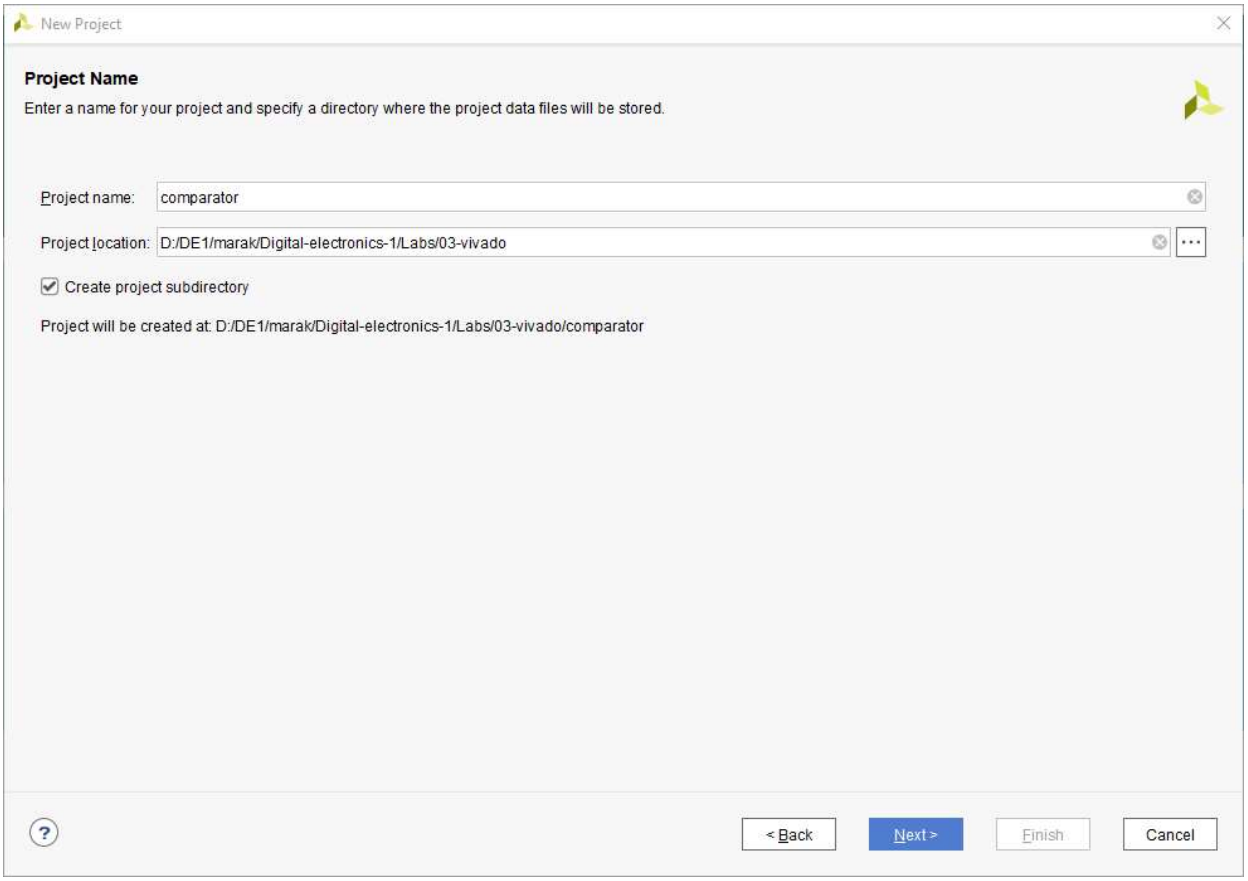
Založení projektu:

Pomocí wizardu projdeme založení projektu

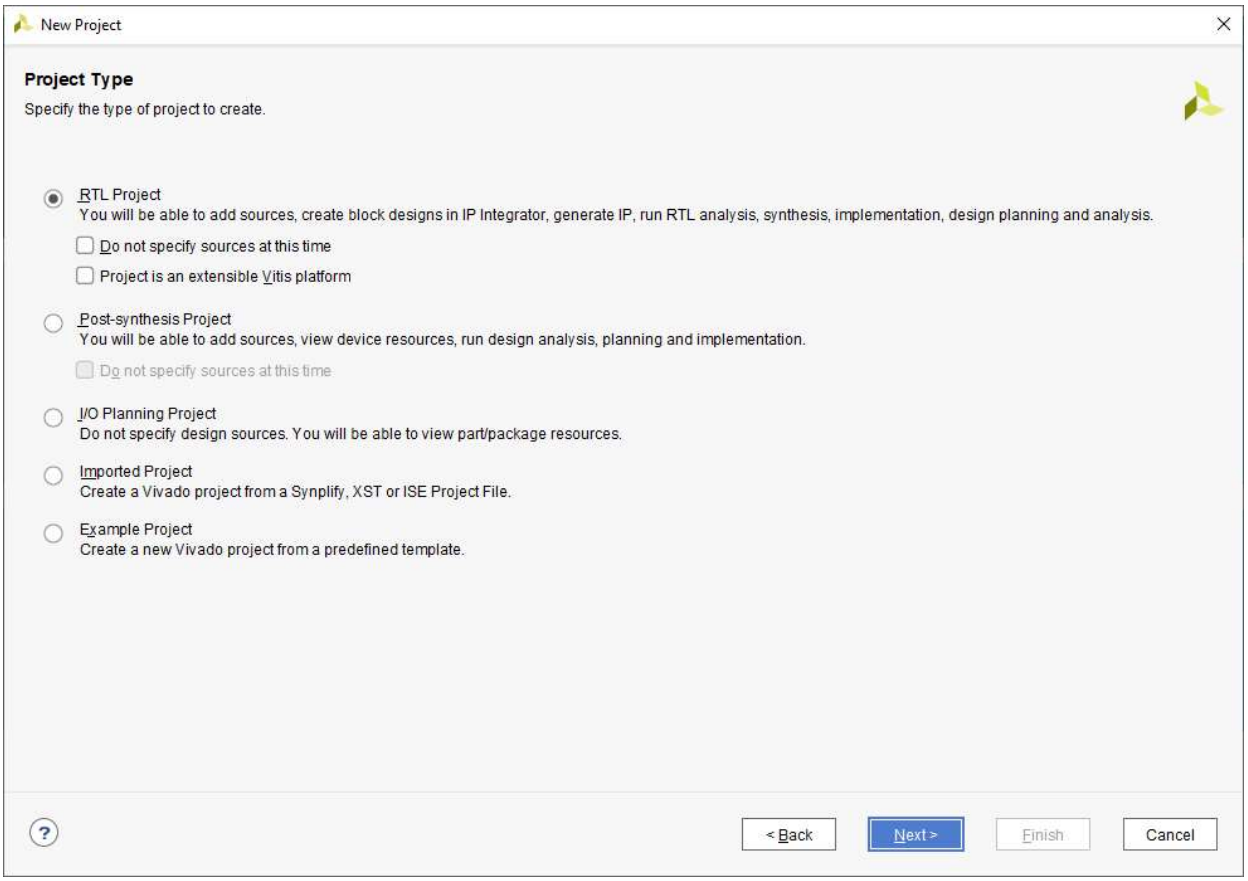


ve wizardu se pohybujeme šipkami next

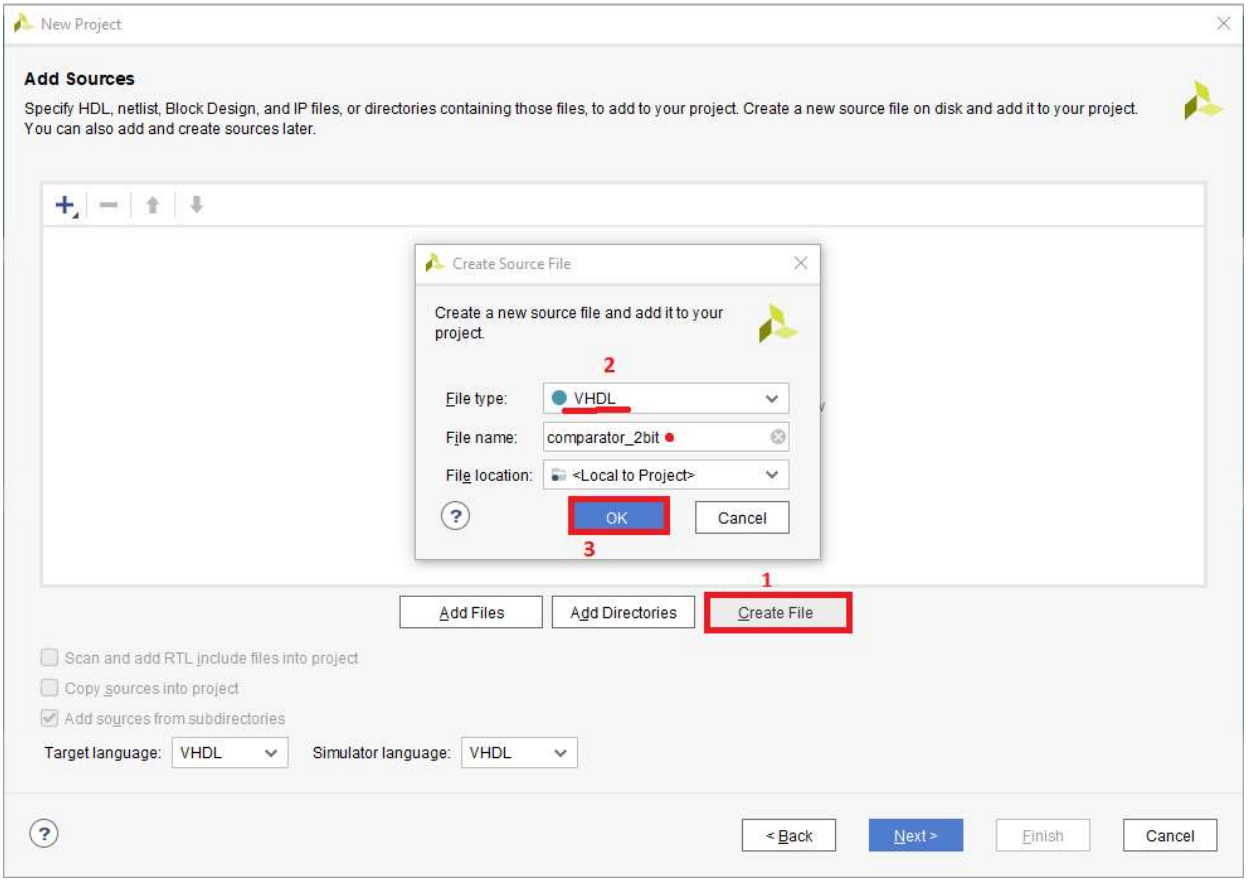
Pojmenování projektu a jeho umístění:



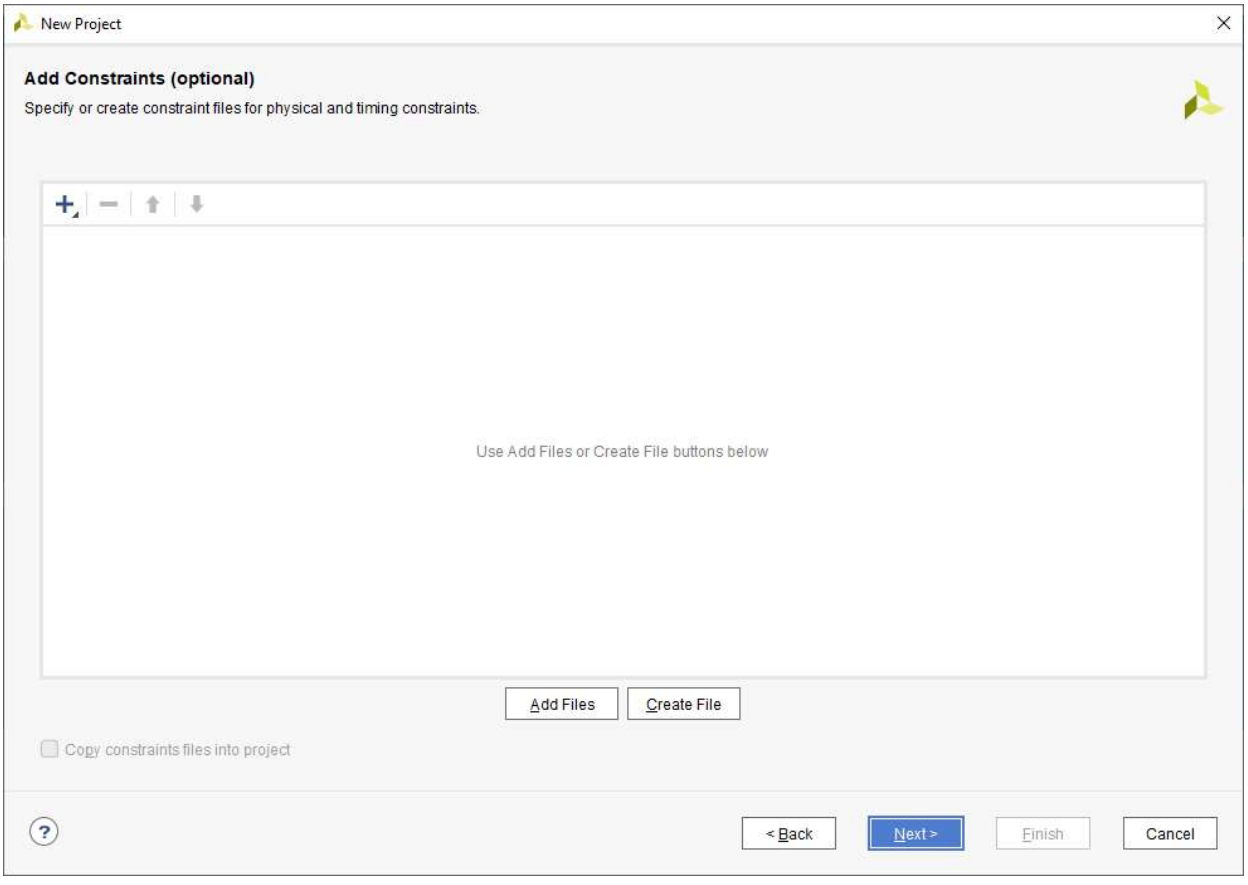
Vybereme RTL project



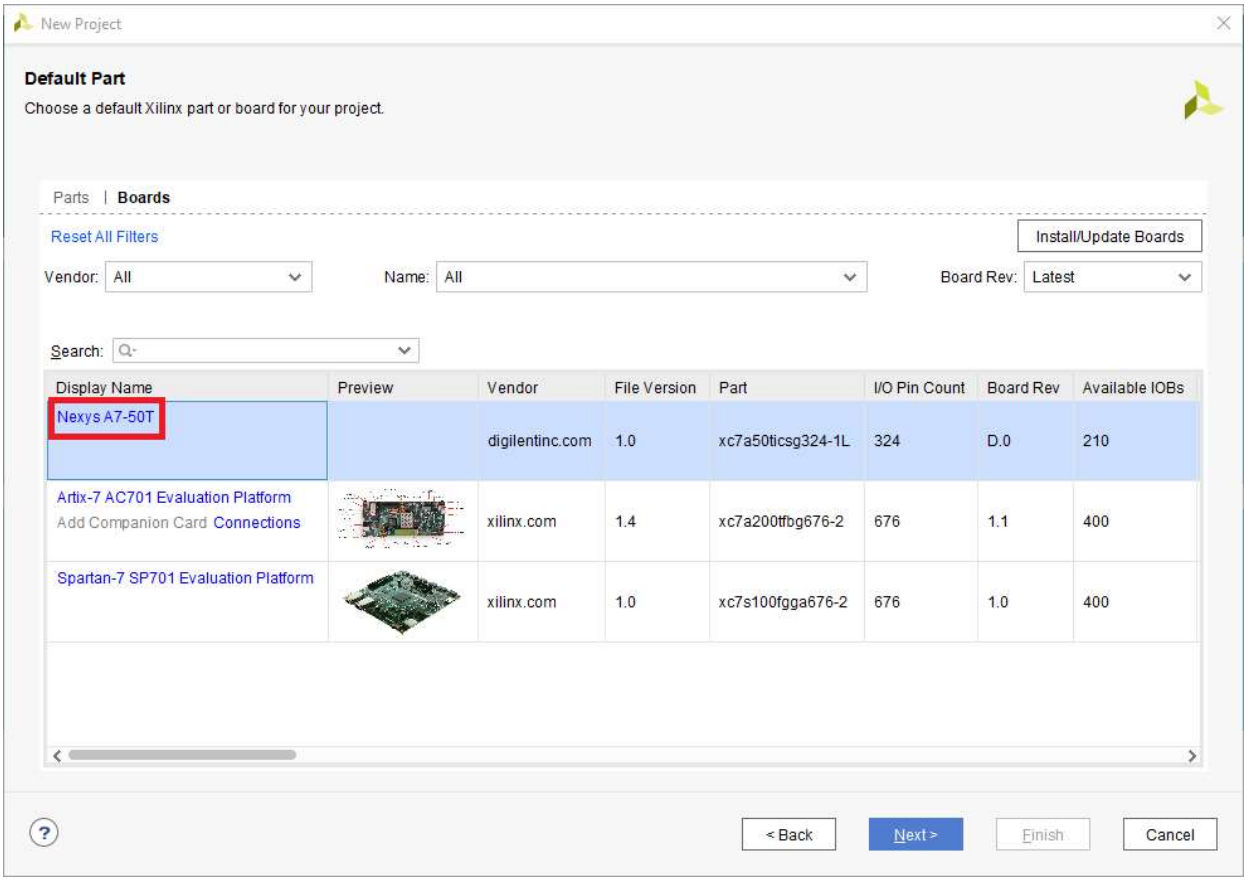
Následně přidáme zdrojové soubory vybráním create file a vybereme typ souboru VHDL



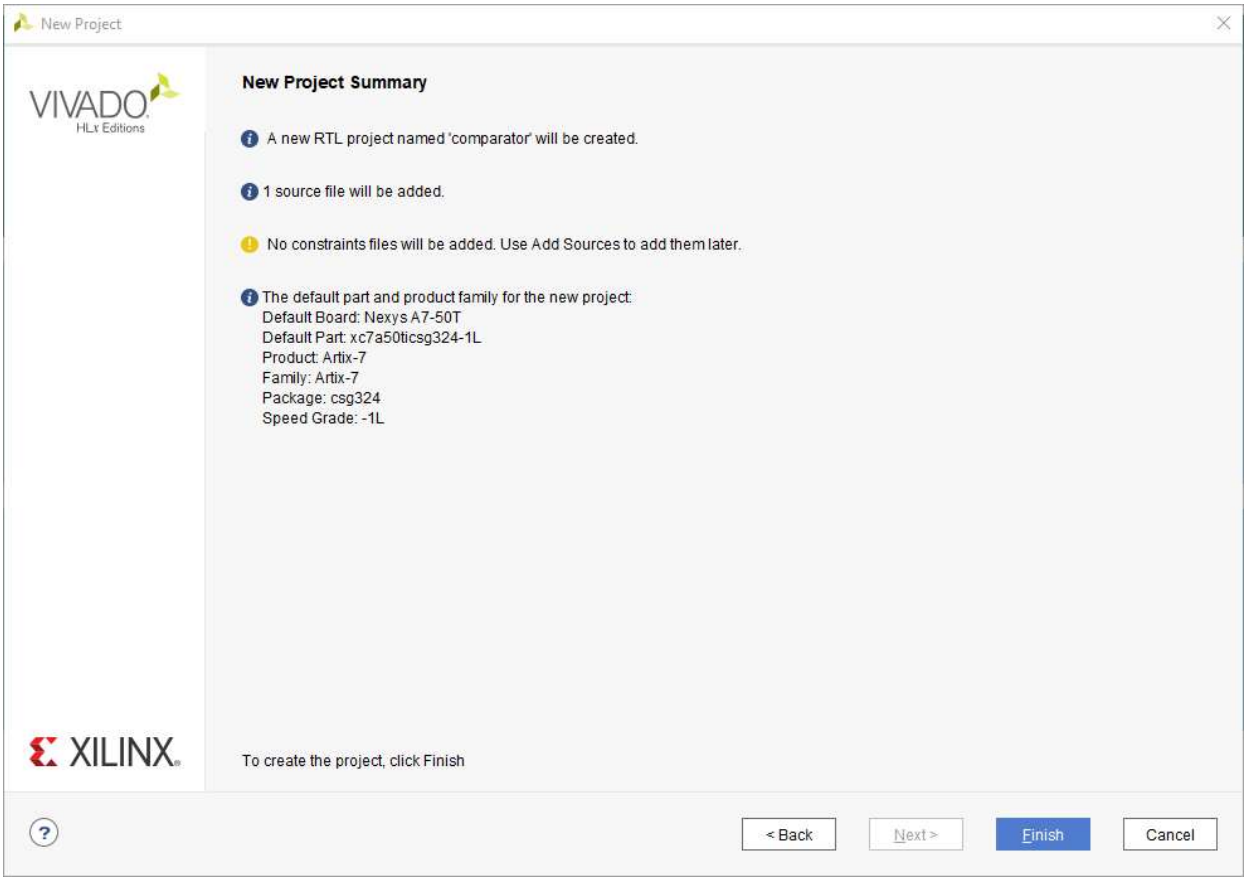
Můžeme přidat constraints files



Vybereme desku Nexys A7-50T

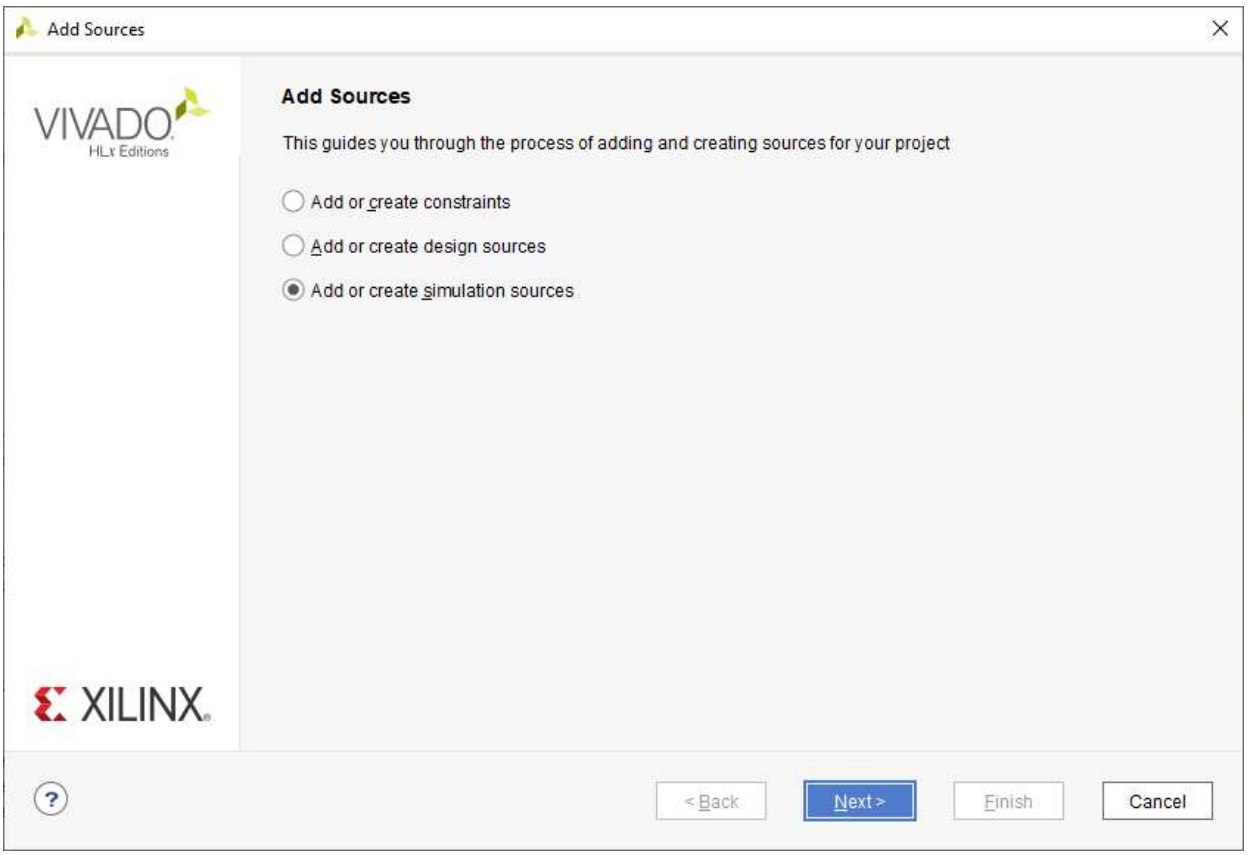


A nakonec tlačítkem Finish projekt vytvoříme

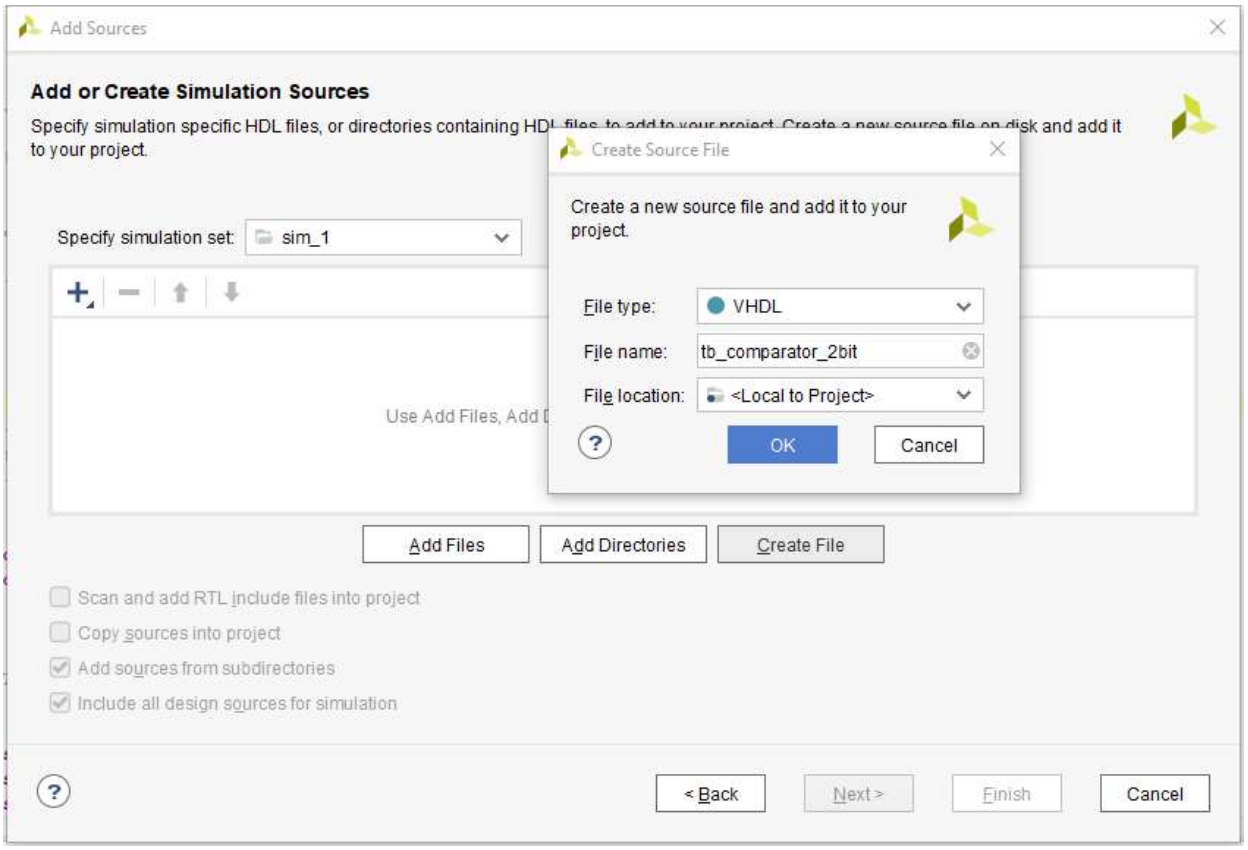


Přidání souboru

Pokud chceme přidat soubor, např testbench, tak pomocí File>Add source (nebo Alt+A) vyvoláme okno kde vyberem nejprve typ souboru:



Opět vybereme typ souboru a zadáme název



Simulace se spistí ze záložky Flow>Run Simulation>Run Behavioral Simulation nebo z bočního navigátoru v sekci Simulation