xmarek71 / Digital-electronics1

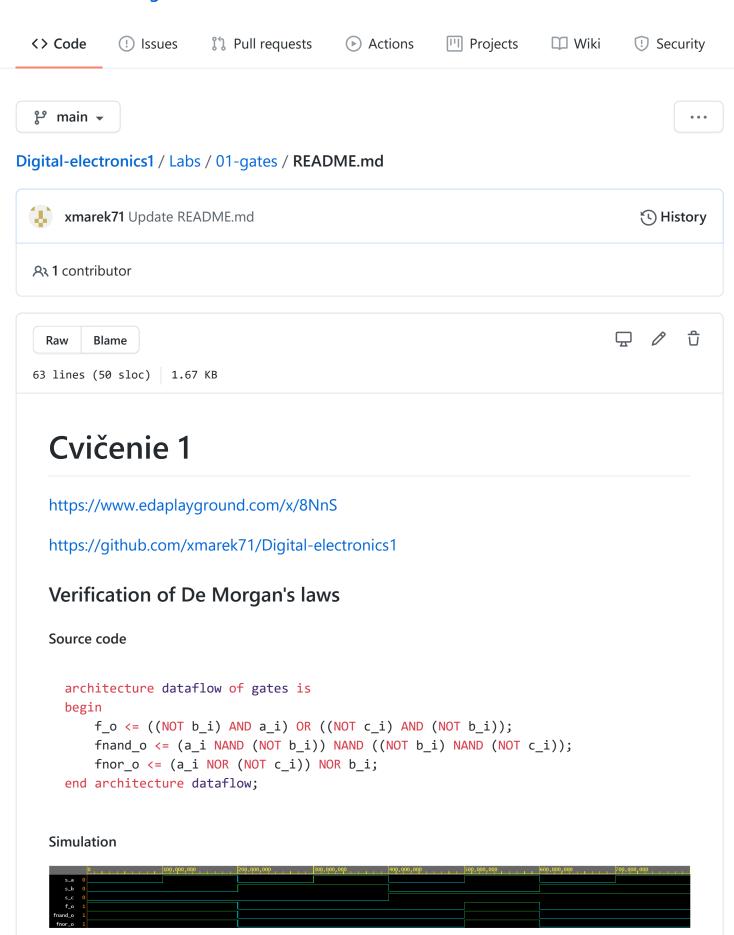


Table with logical values

С	b	a	f(c,b,a)	fnand(c,b,a)	fnor(c,b,a)
0	0	0	1	1	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	0	0

Verification of Distributive laws

Source code

```
architecture dataflow of gates is
begin
    f_dist1 <= (a_i AND b_i) OR (a_i AND c_i);
    f_dist11 <= a_i AND ( b_i OR c_i );
    f_dist2 <= ( a_i OR b_i ) AND ( a_i OR c_i );
    f_dist21 <= a_i OR ( b_i AND c_i );
end architecture dataflow;</pre>
```

Simulation



Table with logical values

С	b	a	fdist1(c,b,a)	fdist1.1(c,b,a)	fdist2(c,b,a)	fdist2.1(c,b,a)
0	0	0	0	0	0	0
0	0	1	0	0	1	1

С	b	a	fdist1(c,b,a)	fdist1.1(c,b,a)	fdist2(c,b,a)	fdist2.1(c,b,a)
0	1	0	0	0	0	0
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	1	1	1	1	1