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main Digital-electronics1 / Labs / **02-logic** /

xmarek71 Update README.md … 3 hours ago **History**

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README.md 3 hours ago

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Cvičenie 2

https://github.com/xmarek71/Digital-electronics1/

2-bit comparator

https://www.edaplayground.com/x/k7HT

2-bit comparator truth table

Dec. equivalent	B[1:0]	A[1:0]	B is greater than A	B equals A	B is less than A
0	0 0	0 0	0	1	0
1	0 0	0 1	0	0	1
2	0 0	1 0	0	0	1
3	0 0	1 1	0	0	1

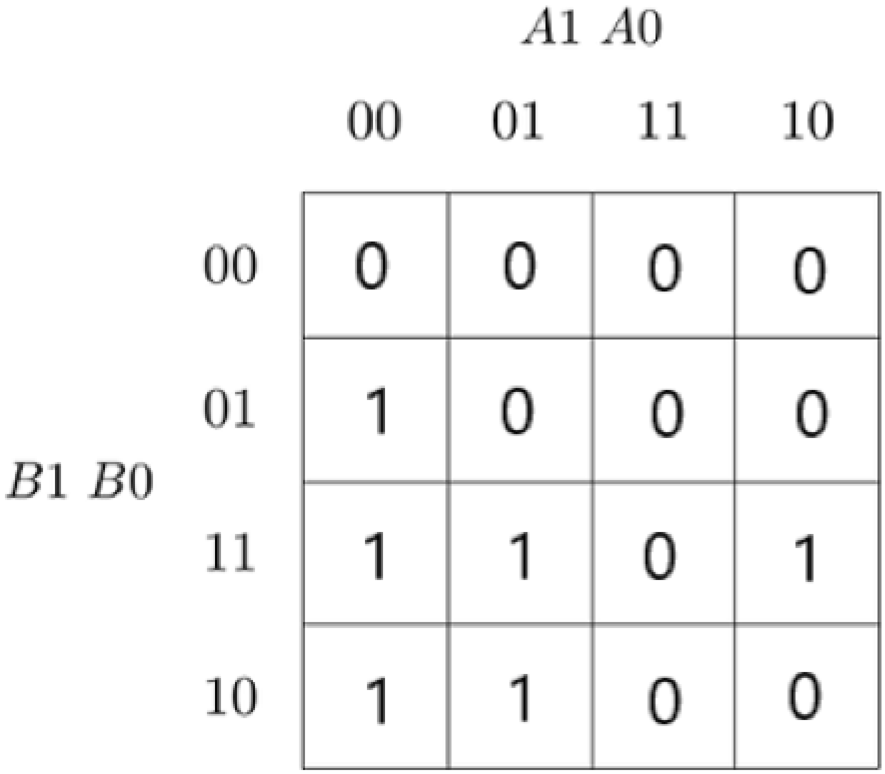
Dec. equivalent	B[1:0]	A[1:0]	B is greater than A	B equals A	B is less than A
4	0 1	0 0	1	0	0
5	0 1	0 1	0	1	0
6	0 1	1 0	0	0	1
7	0 1	1 1	0	0	1
8	1 0	0 0	1	0	0
9	1 0	0 1	1	0	0
10	1 0	1 0	0	1	0
11	1 0	1 1	0	0	1
12	1 1	0 0	1	0	0
13	1 1	0 1	1	0	0
14	1 1	1 0	1	0	0
15	1 1	1 1	0	1	0

Canonical SoP (Sum of Products) and PoS (Product of Sums) forms for "equals" and "less than" functions

$$equals_{\rm SoP} = (\overline{A_0} \cdot \overline{A_1} \cdot \overline{B_0} \cdot \overline{B_1}) + (A_0 \cdot \overline{A_1} \cdot B_0 \cdot \overline{B_1}) + (\overline{A_0} \cdot A_1 \cdot \overline{B_0} \cdot B_1) + (A_0 \cdot A_1 \cdot B_0 \cdot B_1)$$

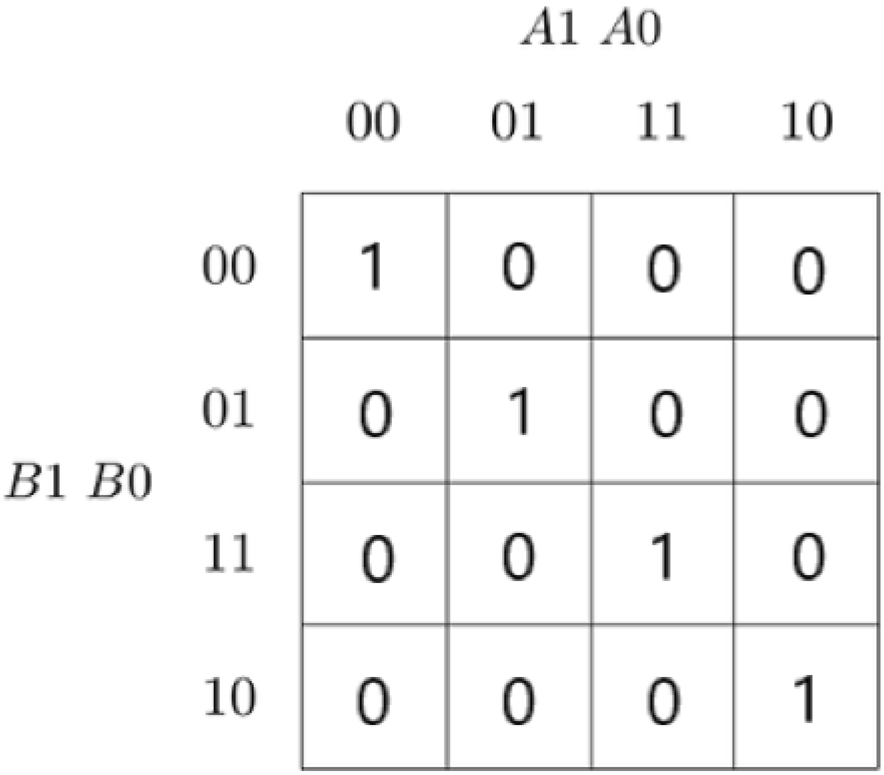
$$less_{PoS} = (A_0 + A_1 + B_0 + B_1) \cdot (A_0 + A_1 + \overline{B_0} + B_1) \cdot$$
$$(\overline{A_0} + A_1 + \overline{B_0} + B_1) \cdot (A_0 + A_1 + B_0 + \overline{B_1}) \cdot$$
$$(\overline{A_0} + A_1 + B_0 + \overline{B_1}) \cdot (A_0 + \overline{A_1} + B_0 + \overline{B_1}) \cdot$$
$$(A_0 + A_1 + \overline{B_0} + \overline{B_1}) \cdot (\overline{A_0} + A_1 + \overline{B_0} + \overline{B_1}) \cdot$$
$$(A_0 + \overline{A_1} + \overline{B_0} + \overline{B_1}) \cdot (\overline{A_0} + \overline{A_1} + \overline{B_0} + \overline{B_1})$$

Karnaugh map for B is greater than A



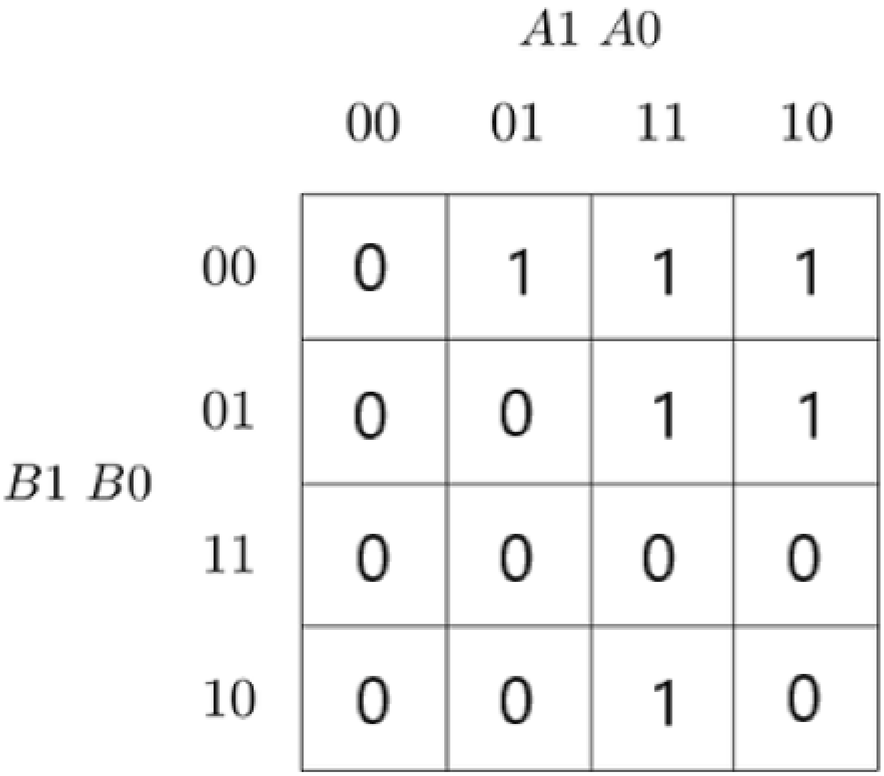
		A1 A0			
		00	01	11	10
B1 B0	00	0	0	0	0
	01	1	0	0	0
	11	1	1	0	1
	10	1	1	0	0

Karnaugh map for B equals A



		A1 A0			
		00	01	11	10
B1 B0	00	1	0	0	0
	01	0	1	0	0
	11	0	0	1	0
	10	0	0	0	1

Karnaugh map for B is less than A



B1 B0 \ A1 A0	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

Equations of simplified SoP form of the "greater than" function and simplified PoS form of the "less than" function

$$
\begin{aligned}
greater_{\text{SoP}} &= \overline{A1}\cdot B1 + \overline{A0}\cdot\overline{A1}\cdot B0 + \overline{A0}\cdot B0\cdot B1 \\
less_{\text{PoS}} &= (A0 + A1)\cdot(\overline{B0} + A1)\cdot(\overline{B1} + A1)\cdot(\overline{B1} + A0)\cdot(\overline{B1} + \overline{B0})
\end{aligned}
$$

4-bit binary comparator

Link

https://www.edaplayground.com/x/Zs7D

VHDL architecture from design file

```
entity comparator_4bit is
    port(
        a_i           : in  std_logic_vector(4 - 1 downto 0);
        b_i           : in  std_logic_vector(4 - 1 downto 0);
                B_greater_A_o : out std_logic;       -- B is greater than A
        B_equals_A_o  : out std_logic;       -- B equals A
        B_less_A_o    : out std_logic       -- B is less than A
    );
end entity comparator_4bit;

architecture Behavioral of comparator_4bit is
```

```
begin

    B_less_A_o   <= '1' when (b_i < a_i) else '0';
    B_greater_A_o <= '1' when (b_i > a_i) else '0';
    B_equals_A_o  <= '1' when (b_i = a_i) else '0';

end architecture Behavioral;
```

VHDL stimulus process from testbench file

```
p_stimulus : process
    begin
        report "Stimulus process started" severity note;

                s_b <= "0000"; s_a <= "0000"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '1') and (s_B_less
                report "Test failed for input combination: 0000, 0000" severity errc

                s_b <= "0000"; s_a <= "0001"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0001" severity errc

                s_b <= "0000"; s_a <= "0010"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0010" severity errc

                s_b <= "0000"; s_a <= "0011"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0011" severity errc

                s_b <= "0000"; s_a <= "0100"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0100" severity errc

                s_b <= "0000"; s_a <= "0101"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0101" severity errc

                s_b <= "0000"; s_a <= "0110"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0110" severity errc

                s_b <= "0000"; s_a <= "0111"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 0111" severity errc

                s_b <= "0000"; s_a <= "1000"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '0') and (s_B_less
                report "Test failed for input combination: 0000, 1000" severity errc
                s_b <= "0000"; s_a <= "1001"; wait for 100 ns;
                assert ((s_B_greater_A = '0') and (s_B_equals_A = '1') and (s_B_less
                report "Test failed for input combination: 0000, 1001" severity errc

        report "Stimulus process finished" severity note;
        wait;
    end process p_stimulus;
```

Simulator console output

```
analyze design.vhd
analyze testbench.vhd
elaborate tb_comparator_4bit
testbench.vhd:51:9:@0ms:(report note): Stimulus process started
testbench.vhd:91:16:@1us:(assertion error): Test failed for input combination: 0000, 1001
testbench.vhd:98:9:@1us:(report note): Stimulus process finished
Finding VCD file...
./dump.vcd
[2021-02-18 05:35:35 EST] Opening EPWave...
Done
```