

Final

● Graded

Student

Kyle Carbonell

Total Points

129 / 200 pts

Question 1

q1 1.5 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 2

q2 2 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 3

q3 1 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

 What kind of cache?

Question 4

q4

2 / 2 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 5

q5

0 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 6

q6

3 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 7

q7

2 / 3 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 8

q8

2 / 2 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 9

q9

4 / 4 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

✓ + 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

✓ + 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 10

q10

2 / 2 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 11

q11

2 / 2 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 12

q12

4 / 4 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

✓ + 4 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 13

q13

6 / 6 pts

+ 1 pt cycle time

+ 2 pts cycle time

+ 1 pt balanced?

+ 1 pt How to balance

+ 2 pts How to balance

+ 1 pt New cycle time

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

✓ + 6 pts Everything right

Question 14

q14

6 / 6 pts

+ 1 pt Click here to replace this description.

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

+ 5 pts Click here to replace this description.

✓ + 6 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 15

q15

7 / 8 pts

+ 1 pt A's & B's

✓ + 2 pts A's & B's

+ 1 pt P's & G's

✓ + 2 pts P's & G's

✓ + 1 pt Cin0 labeled, connected to CL unit

+ 2 pts Cin0 labeled, connected to CL unit

+ 1 pt Cin1 & Cin2 labeled, coming from CL

✓ + 2 pts Cin1 & Cin2 labeled, coming from CL

+ 8 pts Everything correct

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

- 1 pt Click here to replace this description.

Question 16

q16

2 / 3 pts

+ 1 pt Correct

✓ + 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 17

q17

7 / 8 pts

✓ + 1 pt Prop times used right

✓ + 1 pt Setup times used right

+ 1 pt WCP calculated correctly

+ 2 pts WCP calculated correctly

✓ + 3 pts WCP calculated correctly

+ 1 pt WCP marked

✓ + 2 pts Correct Min cycle time clearly stated

- 0.5 pts Click here to replace this description.

- 1 pt Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 18

q18

2 / 2 pts

+ 1 pt Click here to replace this description.

✓ + 2 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 19

q19

9 / 9 pts

19.1 (no title)

3 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

19.2 (no title)

3 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

19.3 (no title)

3 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 20

q20

15 / 15 pts

20.1 (no title)

+ 1 pt S

+ 2 pts S

✓ + 3 pts S

+ 1 pt R

+ 2 pts R

✓ + 3 pts R

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 6 pts Everything right

20.2 (no title)

6 / 6 pts

+ 1 pt J

+ 2 pts J

✓ + 3 pts J

+ 1 pt K

+ 2 pts K

✓ + 3 pts K

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 6 pts Everything right

20.3 (no title)

3 / 3 pts

+ 1 pt T

+ 2 pts T

✓ + 3 pts T

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 6 pts Everything right

Question 21

q21

8 / 10 pts

+ 1 pt number of states

+ 2 pts Number of states

+ 0.5 pts arcs

+ 1 pt arcs

+ 2 pts arcs

+ 1 pt Labels

+ 2 pts Labels

+ 4 pts Labels

+ 0 pts Labels

- 0.5 pts Click here to replace this description.

- 1 pt Click here to replace this description.

Question 22

q22

6 / 6 pts

+ 1 pt number of states

+ 2 pts Number of states

+ 1 pt arcs

+ 2 pts arcs

+ 3 pts arcs

+ 4 pts arcs

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 23

q23

1.5 / 10 pts

+ 1 pt PCoutB1

✓ + 1 pt PCoutB2

✓ + 1 pt MARin

+ 1 pt Zin

+ 1 pt ALUincB

✓ + 1 pt MemRead

✓ + 1 pt Zout

✓ + 1 pt PCin

+ 1 pt MDRout

+ 1 pt IRin

+ 0 pts Click here to replace this description.

✓ - 1 pt Click here to replace this description.

✓ - 1 pt Click here to replace this description.

✓ - 0.5 pts Click here to replace this description.

- 1 pt Nothing on B1 to increment

- 2 pts Can't have more than 1 thing driving the bus at a time

- 1 pt Never put PC on B2 bus into MAR

✓ - 1 pt Did not increment PC

Question 24

q24

1 / 8 pts

+ 1 pt RoutB1

+ 1 pt IRoutB2

+ 0.5 pts ALUAdd

+ 0.5 pts Zin

+ 1 pt Imm

+ 0.5 pts Zout

+ 0.5 pts MARin

+ 1 pt ACCoutB2

+ 1 pt MDRin

+ 1 pt MemWrite

+ 0 pts Click here to replace this description.

- 2 pts Can't have more than 1 thing driving the bus at a time

- 1 pt Click here to replace this description.

- 1 pt Click here to replace this description.

- 0.5 pts Click here to replace this description.

Question 25

q25

0.5 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 26

q26

0.5 / 4 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

✓ + 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 27

q27

0 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 28

q28

0 / 7 pts

+ 1 pt Entries in page table

+ 2 pts Entries in page table

+ 1 pt Width of page table

+ 2 pts Width of page table

+ 1 pt Problem

+ 1 pt How to fix

+ 2 pts How to fix

✓ + 0 pts Click here to replace this description.

- 0.5 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 29

q29

2.5 / 5 pts

+ 1 pt Entries in PT

+ 2 pts Entries in PT

+ 1 pt Width of entry

✓ + 2 pts Width of entry

✓ + 1 pt Problem?

+ 0 pts Click here to replace this description.

✓ - 0.5 pts Click here to replace this description.

- 0.5 pts Click here to replace this description.

Question 30

q30

10 / 10 pts

30.1 (no title)

4 / 4 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

✓ + 4 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

30.2 (no title)

6 / 6 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

+ 5 pts Click here to replace this description.

✓ + 6 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 31

q31

0 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 32

q32

6 / 6 pts

+ 1 pt Click here to replace this description.

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

+ 5 pts Click here to replace this description.

✓ + 6 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 33

q33

2 / 8 pts

33.1 (no title)

0 / 1 pt

+ 1 pt Physical Address

+ 0.5 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

33.2 (no title)

1 / 3 pts

+ 1 pt Entry correct

+ 1 pt Contents correct

✓ + 1 pt Valid bit set

+ 3 pts All Correct

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

33.3 (no title)

1 / 3 pts

+ 1 pt Entry correct

+ 1 pt Contents correct

✓ + 1 pt Valid bit set

+ 3 pts All Correct

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

33.4 (no title)

0 / 1 pt

+ 1 pt Physical Address

+ 0.5 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

Question 34

q37

0 / 9 pts

34.1 (no title)

 0 / 2 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

 Question states memory has been divided into 4 segments, so you need 2 bits to tell which segment you are dealing with.

34.2 (no title)

0 / 4 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

34.3 (no title)

0 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

✓ + 0 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

Question 35

q38

0.5 / 8 pts

+ 1 pt Data lines connected correctly

+ 2 pts Data lines connected correctly

+ 3 pts Data lines connected correctly

+ 4 pts Data lines connected correctly

+ 1 pt 4 chips connected to make 1 byte

+ 2 pts 4 chips connected to make 1 byte

+ 1 pt Correct decoder connected to chips

+ 1 pt Correct address line used

+ 8 pts Everything correct

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

- 1 pt Click here to replace this description.

- 0.5 pts Click here to replace this description.

Question 36

q39

4 / 4 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

+ 4 pts Click here to replace this description.

+ 0.5 pts Click here to replace this description.

+ 0 pts Click here to replace this description.

Question 37

q40

4 / 4 pts

- + 4 pts** 3 NOPs for each RAW

+ 2 pts 2 NOPs for each RAW

- 1 pt NOPs where they don't belong

- 1 pt NOPs where they don't belong

- 1 pt Not enough NOPs

+ 0 pts Click here to replace this description.

+ 2 pts 3 NOPs for 1 RAW

Question 38

q41

3 / 4 pts

+ 2 pts Two remaining NOPs after lw

- + 1 pt** 1 remaining NOP after lw

- + 2 pts** 1 remaining NOP after sub

+ 1 pt No remaining NOPs after sub

+ 1 pt 2 remaining NOPs after sub

+ 0 pts Click here to replace this description.

Question 39

q42

0 / 3 pts

+ 1 pt Correct

+ 2 pts Click here to replace this description.

+ 3 pts Click here to replace this description.

- + 0 pts** Click here to replace this description.

+ 0.5 pts Click here to replace this description.

University of California, Davis
Department of Computer Science

ECS-154A Computer Architecture

Professor Farrens

Fall 2024

Final Assessment

Cheating on exams is prohibited by the Academic Code of Conduct. I understand that if I am caught cheating on this exam my scores will be negated and I will receive no credit on the exam. Persons caught cheating will also face University disciplinary actions.

Name: Kyle Cartrell

Signature: M

Student ID number: 922 344 776

Very short answer questions - maximum of 5 words:

[2] Virtual Memory is a map from one address space to another.

[2] Caches, Virtual Memory, and in fact the entire memory hierarchy is possible because programs exhibit what principle?

Locality (spatial/temporal)

[2] What structure uses a dirty bit?

write-back cache caches

[2] What is one of the simplest (and oldest) techniques for exploiting parallelism among instructions?

Pipelining

[2] When dealing with control hazards, it is not enough to predict the branch direction - what else must we know?

The order of instructions

[3] What is the 3-term CPU time equation?

$\frac{\text{inst}}{\text{program}} \cdot \frac{\text{cycle}}{\text{inst}} \cdot \frac{\text{time}}{\text{cycle}}$

[3] What is the average memory access time equation?

$\text{AMAT} = (\text{hit rate}) + (\text{miss rate} \cdot \text{miss penalty})$

[2] When dealing with a write to a cache that hits, what are the two possible approaches?

write-back and write-through

[4] What are the 3 pipeline hazards? Which one can be eliminated by providing more resources?

control hazards, data hazards, structure hazards

~~control hazards can be eliminated~~

[2] What are the two main ways to define performance?

latency and bandwidth

[2] Which one is used more now when reporting the performance of a modern chip?

bandwidth

[4] What are the 3 types of data hazards? Which one can be dealt with by using forwarding?

- 1) read after write - dealt with forwarding
- 2) write after read
- 3) write after write

[6] In your first design of a 6-stage pipeline (F,D,E1,E2,M,W) F takes 24 time units, D takes 26, E1 takes 13, E2 takes 14, M takes 24, and W takes 25.

a) What will the clock cycle time be for this pipeline?

26 Time units

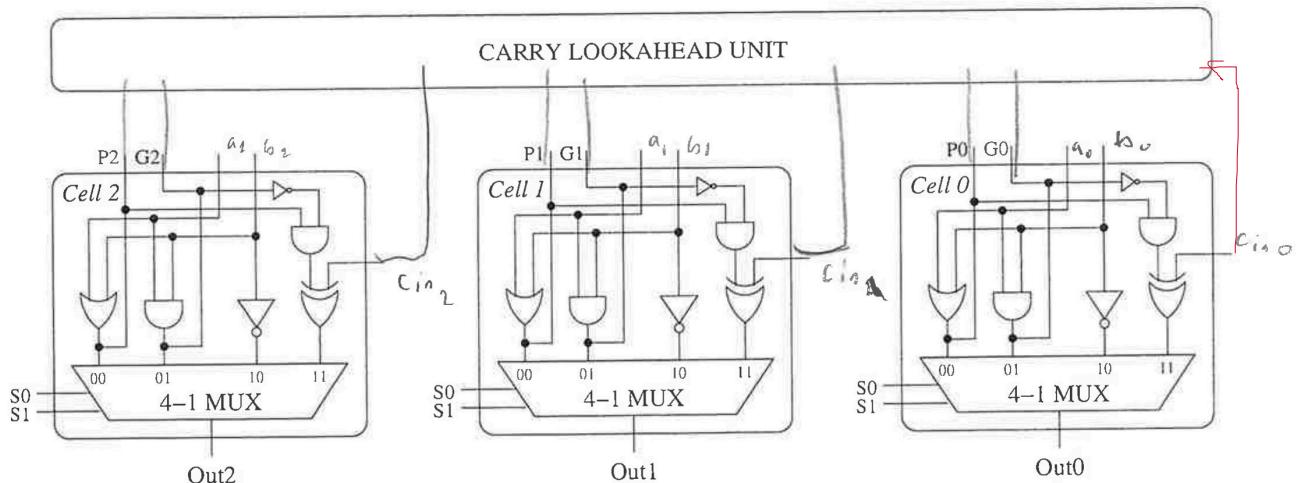
b) Is it a balanced pipeline? If not, explain what you could do to make it more balanced. What would the cycle time be now? *No, combine E₁ and E₂ | cycle time will be 27 time units
that way they will all be about 25 TU*

[6] An important program spends 60% of its time doing Integer operations, and 40% of its time doing floating point arithmetic. By redesigning the hardware you can make the Integer unit 70% faster (take 30% as long), or you can make the Floating Point unit 90% faster (take 10% as long). Which should you do, and why? (Show your work). **NOTE: Do not use Amdahl's equations to solve this. The use of that equation does not convey any understanding ... you will receive no credit if you use that equation.**

$$\text{Int: } 0.6 \rightarrow 0.6 \cdot 0.3 = 0.18 \cdot 0.4 = 0.54$$

$$\text{Float: } 0.4 \rightarrow 0.4 \cdot 0.1 = 0.04 + 0.6 = 0.64$$

- You should speed up the integer unit



[8] The diagram above shows 3 ALU cells and a Carry Lookahead Unit. In the above diagram, draw lines to show how you would connect this up to provide a 3-bit ALU which uses Carry Lookahead. Label all the (unlabeled) inputs and outputs accordingly. (You do not have to draw what is inside the Carry Lookahead Unit, and you do not need to worry about subtraction for this problem.)

[3] Write the equation for the carry into Cell 2 in this ALU, in terms of P's and G's.

$$C_{in_2} = G_1 + P_1 G_0 + P_0 C_{in_0}$$

[8] Assuming rising edge-triggered flipflops, what is the minimum cycle time (the minimum time between rising clock edges) that will still guarantee correct behavior for the following circuit? Use the following delay values, and assume all input signals become valid at time 0. (Tprop is the propagation time for the flipflop.)

AND: 4ns OR: 3ns NAND: 6ns NOR: 5ns NOT: 1ns MUX: 12ns XOR: 8ns

Tprop (TFF): 11ns Tsetup (TFF): 3ns Thold (TFF): 1ns

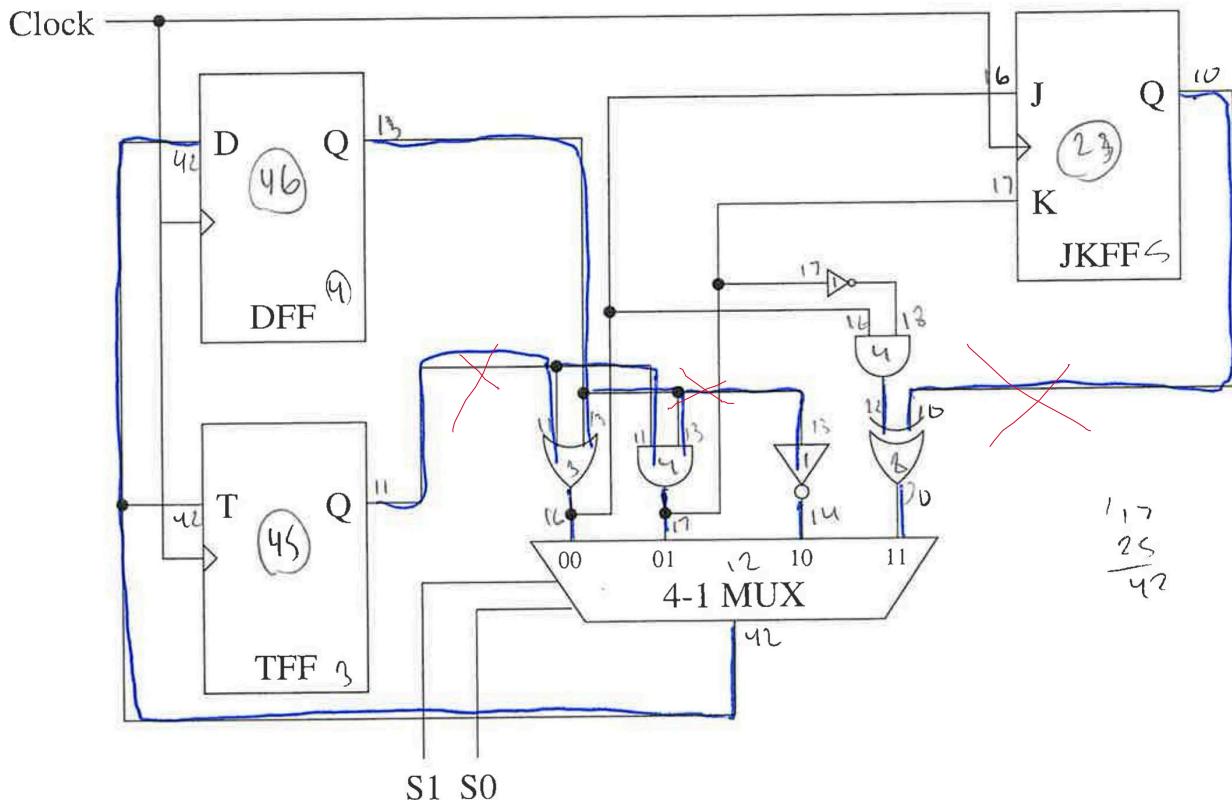
Tprop (DFF): 13ns Tsetup (DFF): 4ns Thold (DFF): 1ns

Tprop (JKFF): 10ns Tsetup (JKFF): 5ns Thold (JKFF): 1ns

Tprop (SRFF): 8ns Tsetup (SRFF): 4ns Thold (SRFF): 1ns

Note: You must show the path you used to get your answer in order to get credit.

46 ns is the minimum cycle time



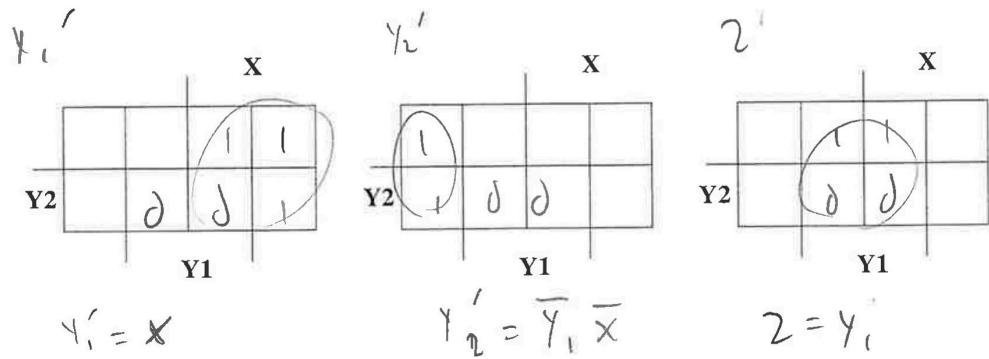
[2] What if the setup time for the JK FF was 25ns? Would the minimum cycle time change? If so, how?

No, the minimum cycle time would still be 46 ns
but JKFF would take 42 ns instead of 23 ns

[9] Given the following table, draw the Karnaugh maps for Y_1' , Y_2' and Z in terms of X , Y_1 and Y_2 , and then write **minimum** boolean equations for each. Do not worry about the fact that the machine might get stuck in a particular state and be unable to get out - just solve the problem as presented.

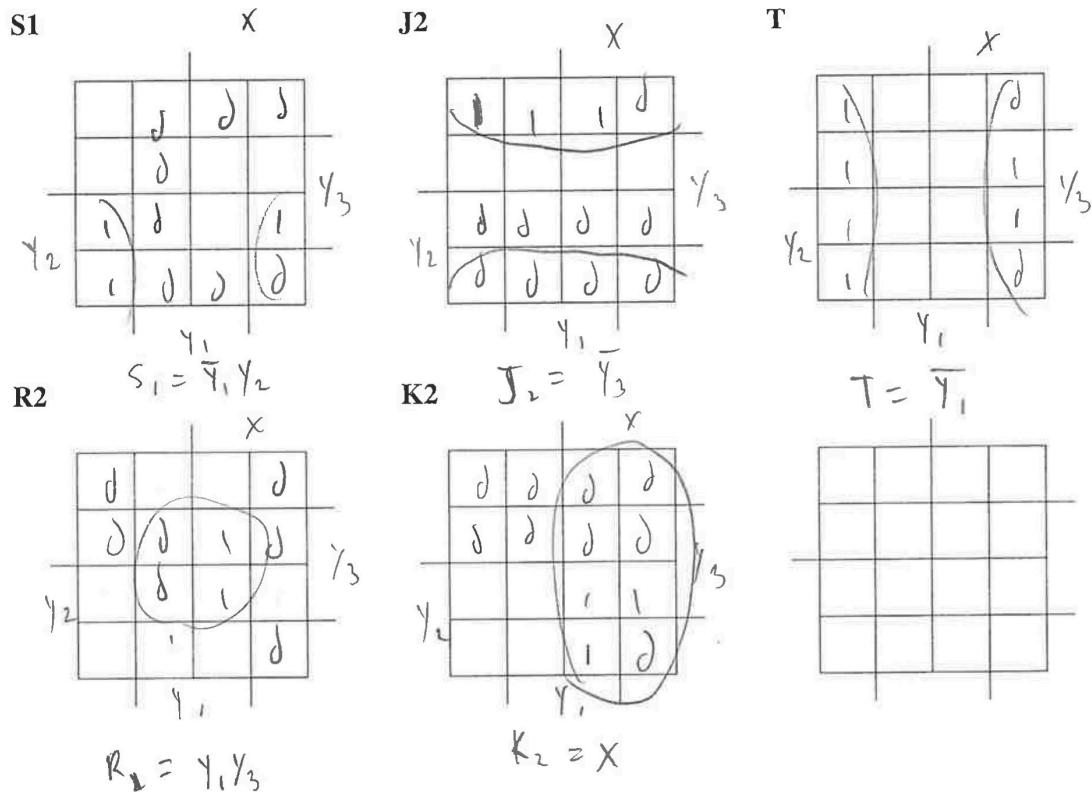
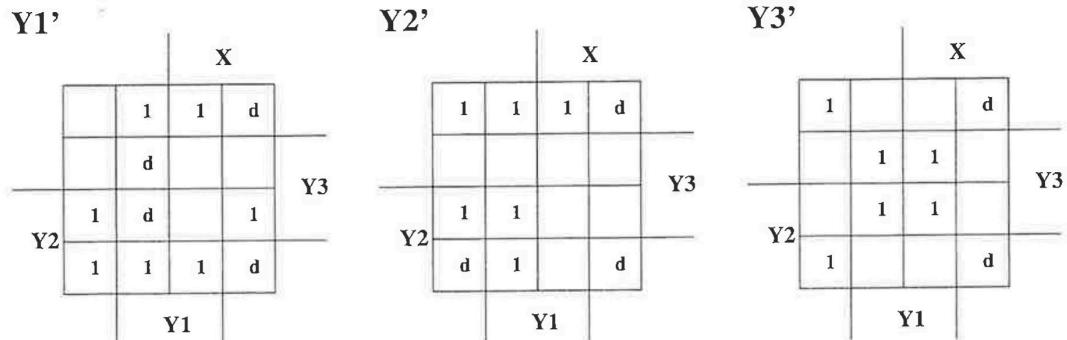
Present State ($Y_1 Y_2$)	Next State		Output	
	$X=0$ ($Y_1' Y_2'$)	$X=1$ ($Y_1' Y_2'$)	$X=0$	$X=1$
00	01	10	0	0
01	01	10	0	0
10	00	10	1	1

Don't care
 0 1 1 - 3
 1 1 1 - 7



Desired Transition $Y \rightarrow Y'$	SR FF S R	JK FF J K	T FF T	D FF D
0 \rightarrow 0	0 d	0 d	0	0
0 \rightarrow 1	1 0	1 d	1	1
1 \rightarrow 0	0 1	d 1	1	0
1 \rightarrow 1	d 0	d 0	0	1

[15] Given the following Karnaugh maps, implement the sequential machine using an SR FF for Y1, a JK FF for Y2, and a T FF for Y3. You do not need to draw the gates, but you do need to write down the **minimized** input equations for each of the inputs of each of the Flip Flops in the circuit.



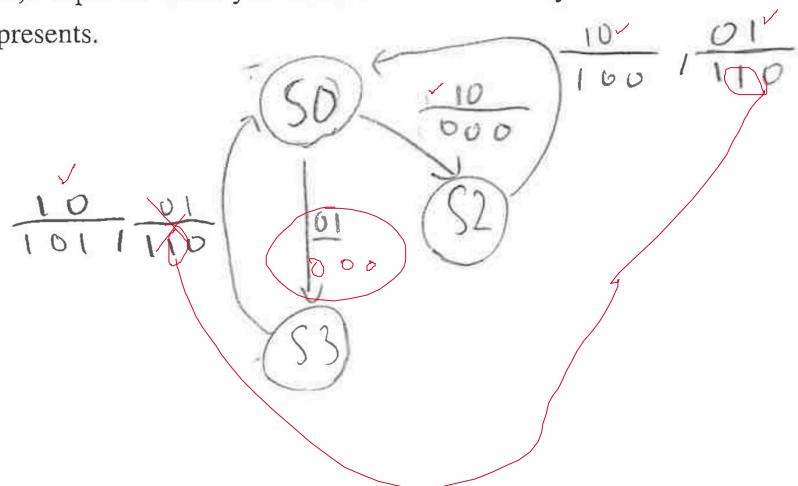
Desired Transition $Y \rightarrow Y'$	SR FF S R	JK FF J K	T FF T	D FF D
$0 \rightarrow 0$	0 d	0 d	0	0
$0 \rightarrow 1$	1 0	1 d	1	1
$1 \rightarrow 0$	0 1	d 1	1	0
$1 \rightarrow 1$	d 0	d 0	0	1

[10] A particularly unimaginative country has 3 types of coins - Ones, Twos, and Threes. A coin-operated machine there only takes Twos (X1) and Threes (X2), and dispenses merchandise ($Z_1=1$) when the sum of the inputs is greater than or equal to Four. Only 1 coin can be input at a time. The machine should give exact change.

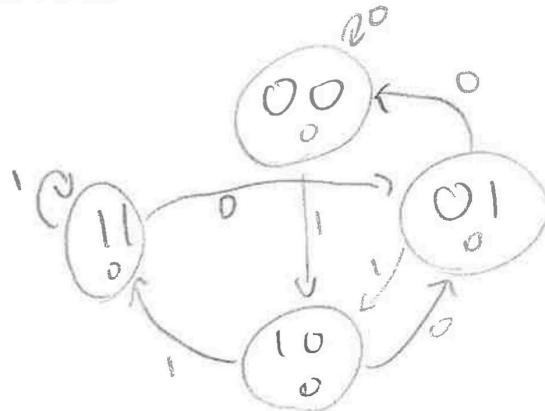
Using a Mealy model, draw the State Transition Diagram (the circles and the arcs) for this finite state machine. Label the transitions on the diagram using the format we used in class (inputs over outputs). Let state S_0 =no money input (the Start state). Input 00 sends you back to the same state you are in. Be sure to explain exactly what each output bit represents.

Key:

X_1, X_2	$X_1 = 2 \text{ coin inserted}$
Z_1, Z_2, Z_3	$X_2 = 3 \text{ coin inserted}$
	$Z_1 = \text{Merchandise}$
	$Z_2 = 1 \text{ coin change}$
	$Z_3 = 2 \text{ coin change}$



[6] Draw the state transition diagram for a 2-bit shifter that always shifts the input variable into the most significant bit and discards the least significant bit (it shifts right, in other words). $X=1$ indicates a 1 should be shifted in, $X=0$ indicates a 0 should be shifted in. Use a Moore model.



In this question, we are going to wire up a 12-bit machine. This machine will use a 1-operand format, meaning that instructions are of the type ACC=ACC+R. So, for example, "Add R" is ACC=ACC+R.

The machine is 12-bit addressable. Immediates are sign-extended, and jumps are done by adding the sign-extended Immediate field to the PC.

The machine has 2 different instruction formats: A and B.

A-type: Opcode extra
 11-7 6-0

B-type: Opcode Immediate
 11-7 6-0

The ALU can perform 8 functions, written this way: OP [ALU2 ALU1 ALU0]

Operation	ALU2	ALU1	ALU0	Operation	ALU2	ALU1	ALU0
And	0	0	0	Add	1	0	0
Or	0	0	1	Sub	1	0	1
Xor	0	1	0	IncB	1	1	0
NotA	0	1	1	PassB	1	1	1

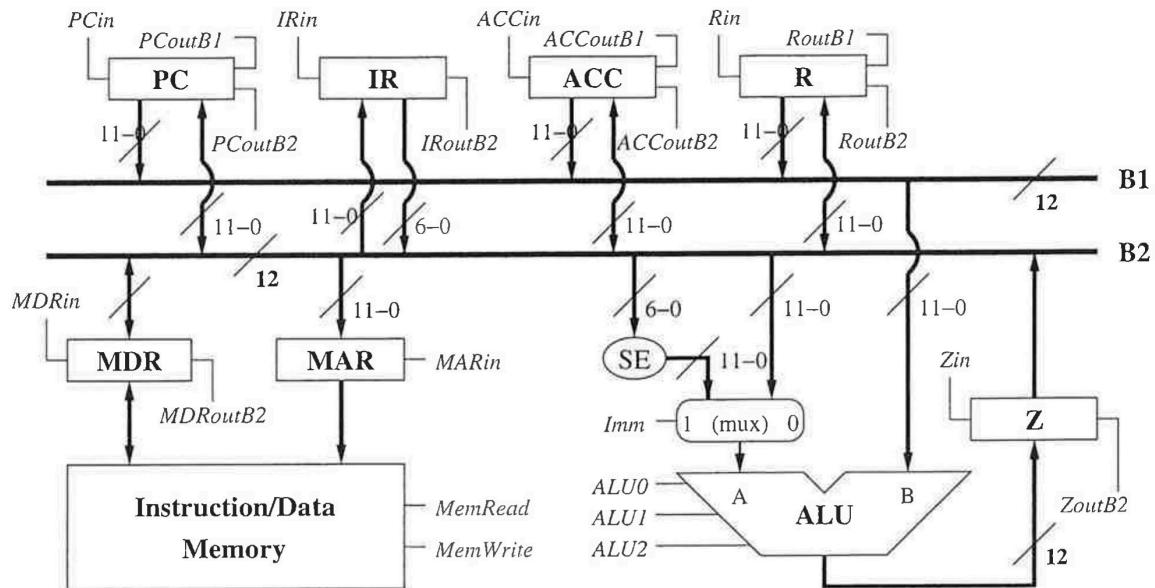
Here are a few of the instructions that have been defined:

Name	Opcode	Operation
ADD	00001	ACC=ACC+R
ADDM	00010	ACC=ACC+MEM[R+Imm]
ADDI	00011	ACC=ACC+Imm
COPYA2R	01000	R=ACC
COPYR2A	01001	ACC=R
LOADACC	01010	ACC=MEM[R+Imm] ; load ACC from mem address (R+Imm)
STOREACC	01011	MEM[R+Imm]=ACC ; store ACC to mem address (R+Imm)
JMP	11011	PC=PC+Imm

On the following page is a diagram of the machine. The control signals are in italics. The sign extend logic creates a 6-bit value which matches the contents of bit 6, so that the 12-bit value generated looks like 666666543210.

Here are the 22 control signals.

PCin	PCoutB1	PCoutB2	IRin	IRoutB2	
Rin	RoutB1	RoutB2	ACCin	ACCoutB1	ACCoutB2
MDRin	MDRoutB2	Zin	ZoutB2	MARin	
ALU0	ALU1	ALU2	MemRead	MemWrite	Imm



[10] Fill in the steps necessary to perform an instruction fetch (incrementing the PC is considered part of the process). Assume memory is ready during the **second** cycle after the MemRead signal.

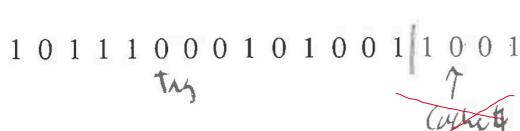
S t e p	P C o u t B 1	P C o u t B 2	A C o u t B 1	A C o u t B 2	R o u t B 1	R o u t B 2	I R o u t B 1	M D R o u t B 2	Z o u t B 2	P C i n	I R i n	A C C i n	R i n	M D R i n	M A R i n	Z i n	A L U 2	A L U 1	A L U 0	M e m R e a d	M e m W r i t e	I m m	
0																							
1																							
2																							
3	X	X	X	X																			
4																							

[8] Now that you have done the instruction fetch, fill in the microcode steps necessary to perform the following instruction: **STOREACC 9** You do not care how long memory takes when doing a store.

S t e p	P C o u t B 1	P C o u t B 2	A C o u t B 1	A C o u t B 2	R o u t B 1	R o u t B 2	I R o u t B 1	M D R o u t B 2	Z o u t B 2	P C i n	I R i n	A C C i n	R i n	M D R i n	M A R i n	Z i n	A L U 2	A L U 1	A L U 0	M e m R e a d	M e m W r i t e	I m m	
0																							
1																							
2																							
3																							



[3] Given the following 17-bit address and a 128-byte Direct Mapped cache with a linesize=8, show how an address is partitioned/interpreted by the cache.

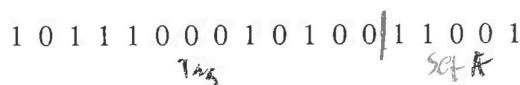


$$ls = 2^3$$

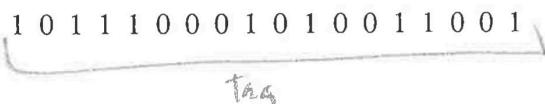
$$\frac{128}{8} = 16 = 2^4$$

[4] Assuming a 15-bit address and a 160-byte 5-way Set Associative cache with a linesize=4, show how an address is partitioned/interpreted by the cache.

$$\frac{160}{4} = 32 = 2^5$$



[2] Assuming a 19-bit address and a 240-byte Fully Associative cache with a linesize=16, show how an address is partitioned/interpreted by the cache.



[7] Given an 8 Megabyte physical memory, a 32 bit Virtual address, and a page size of 1K bytes,

$$1) \text{ entries} = \frac{2^{32}}{2^{10}} = 2^{22} \text{ entries}$$

How many entries are there in the page table?

How wide is each entry?

$$2) \text{ width} = 32 - 13 = 19 \text{ bits width}$$

Is there a problem with this configuration? If so, how can you fix it?

Yes the width of the entry is 19 bits and the amount of physical memory is 2²³ bits, which would make it inefficient to fix by making page size bigger

[5] Given a 2Mbyte physical memory, a 23 bit Virtual address, and a page size of 2K bytes,

1) How many entries are there in the page table?

$$1) \text{ entries} = \frac{2^{21}}{2^{11}} = 2^{10} \text{ entries}$$

2) How wide is each entry?

$$2) \text{ width} = 23 - 11 = 12 \text{ bits width}$$

Is there a problem with this configuration? If so, how can you fix it?

No problem

In this question we are dealing with a Direct Mapped cache. Assume 11-bit addresses are partitioned in the following manner:

Tag	Entry	Offset
<u>TTTTT</u>	<u>EEEE</u>	<u>LL</u>

(Tag is left most 5 bits, entry is middle 4, offset into line is right most 2 bits)

You are given the following address reference sequence (in Hex):

0x4B2,0x4A3,0x4B0,0x092,0x0B2

[10] In the table below, fill in the Cache's Tag values after each memory reference has been processed. If it is a miss, you should enter what the new tag should be in the appropriate slot. (X indicates the entry is invalid). If it is a hit, you should place an H in the correct location. There may be more Tag Array entries than you need. *Only write down things that change - do not fill in all the entries that remain the same.*

Tag Array		Contents of Tag Array after processing address (Time ->)					
Entry Number	Initial Contents	0x4B2	0x4A3	0x4B0	0x092	0x0B2	
0	X						
1	X						
2	X						
3	X						
4	X				00010		
5	X						
6	X						
7	X						
8	X		10010				
9	X						
10	X						
11	X						
12	X	10010		H		00010	
13	X						
14	X						
15	X						

[2] What set of memory addresses are sent to memory on the first miss?

0x4B2

Bar 32 = 5 measures
2-4 = B = 2nd

22] [6] Assume a 10-bit processor, with a 64-byte 2-way set associative cache and a linesize of 4. This is the contents of the cache (as always, there may be more information than you need):

Set 0								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
10101	3B	C1	43	86	3B	C1	43	86
11001	9D	90	B3	65	F4	EB	7A	BC

Set 7								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
00010	03	47	05	45	E8	39	39	9D
10101	51	FE	CF	B5	5D	2A	DE	D8

Set 1								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	72	9A	49	6F	84	CC	62	8D
11011	C4	25	C8	2E	75	E0	5A	F5

Set 6								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11111	5A	70	5C	18	15	52	ED	1C
01011	CF	7E	2E	F9	25	8C	9C	38

Set 2									
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)	
11110	E9	BA	C6	03	B8	AB	14	2B	
11011	17	09	5A	8B	8F	0D	25	CD	

Set 5								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	E0	C4	2C	B4	5D	AE	66	6E
11011	FF	D0	81	2E	4E	94	E5	20

Set 3								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	F8	E5	B4	AB	F4	50	6B	07
11011	FF	8C	99	9E	71	46	BF	0F

Set 4								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	F7	8B	4E	E6	E7	94	B9	2D
11011	F9	09	23	A1	7A	C5	65	35

a) If the processor issues the address

1 0 1 0 1 | 1 0 1 | 1 0

Is this a hit in the cache? (YES NO) If YES, circle the entry and the data value that is returned.

b) If the processor issues the address

1101101011

Is this a hit in the cache? (YES NO) If YES, circle the entry and the data value that is returned.

33

In this problem we have a machine that generates 12 bit Virtual Addresses, uses 256 byte pages, and has 1K bytes of memory. The TLB has 3 entries, and is fully associative.

$$\text{offset} = \frac{2^{10}}{2^8} = 2^2 = 2$$

The first address the CPU issues is

011011011010 (0x6D9)

The requested page is not currently resident in the memory, so a page fault is generated and the Operating System is called in. After consulting its internal data structures, it decides to put the requested page in frame number 1.

Here are the contents of the page table and the TLB before the address is sent to memory:

Page Table		
Entry	Contents	Valid
0000		N
0001		N
0010		N
0011		N
0100		N
0101	0110110110	Y N
0110		N
0111		N
1000		N
1001		N
1010		N
1011		N
1100		N
1101		N
1110		N
1111		N

TLB		
Tag	Contents	Valid
001	0101	Y N
		N
		N

[1] What is the physical address (in binary and hex) that gets sent to memory?

00101 \rightarrow 0x5

[3] Update the page table to show what it contains after the physical address is generated.

[3] Update the TLB to show what it contains after the physical address is generated.

Now, assume the following address is generated next:

011001111010

[1] What physical address gets sent to memory?

01010

$$\begin{aligned} nca &= 2^8 \\ ps &= 2^9 \end{aligned}$$

The following tables contain **some** of the information about a segmented, paged virtual memory system. Total physical memory size is 8K bytes, the page size is 512 bytes, and the OS has partitioned the memory into 4 segments. All numbers in this table are in decimal unless otherwise noted.

Segment Table		
Entry Number	Presence Bit	Page Table
0	1	5
1	1	2
2	1	0
3	0	7
4	1	5
5	1	3
6	1	1
7	0	4

Page Table 0			
Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x4
2	0	0893748	0x7
4	1	2489567	0x1
8	0	9623873	0x17
16	0	B0F6BD3	0x23
25	0	32829AA	0xA
29	1	56D87AC	0xC
31	1	10A876D	0x6

Page Table 2			
Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0xF
1	0	0893748	0x11
2	0	2489567	0x14
3	0	9623873	0x27
4	0	BC56BD3	0x29
6	0	832759E	0x15
17	0	46B37AC	0x24
31	0	810476D	0x16

Page Table 4			
Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x4
2	0	0893748	0x7
4	1	2489567	0x1
8	0	9623873	0x16
16	0	B0F6BD3	0x13
21	0	32829AA	0xA
29	1	56D87AC	0xD
31	1	10A876D	0x6

Page Table 5			
Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
1	1	1234123	0xD
3	0	0893748	0x13
9	0	2489567	0x19
15	0	9623873	0x20
18	0	AE76BD3	0x18
22	0	328759A	0xE
25	0	11D87BE	0x12
31	1	91C875D	0x0

Page Table 7			
Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x5
1	0	0893748	0x26
2	0	2489567	0x21
3	1	9623873	0x2
4	0	AE76BD3	0x1A
5	0	328759A	0x10
6	1	56D87AC	0x3
7	1	10A876D	0x8

[9] For each of the following convert the virtual address into a physical address (if possible) and write down the value of the memory location corresponding to the address. If it is not possible to do so, explain why. Be sure to circle the frame number in the table that you used to do the conversion.

0xCFA4 (1 1 0|0 1 1 1 1|1 0 1 0 0 1 0 0 in binary).

Page 1 is not given

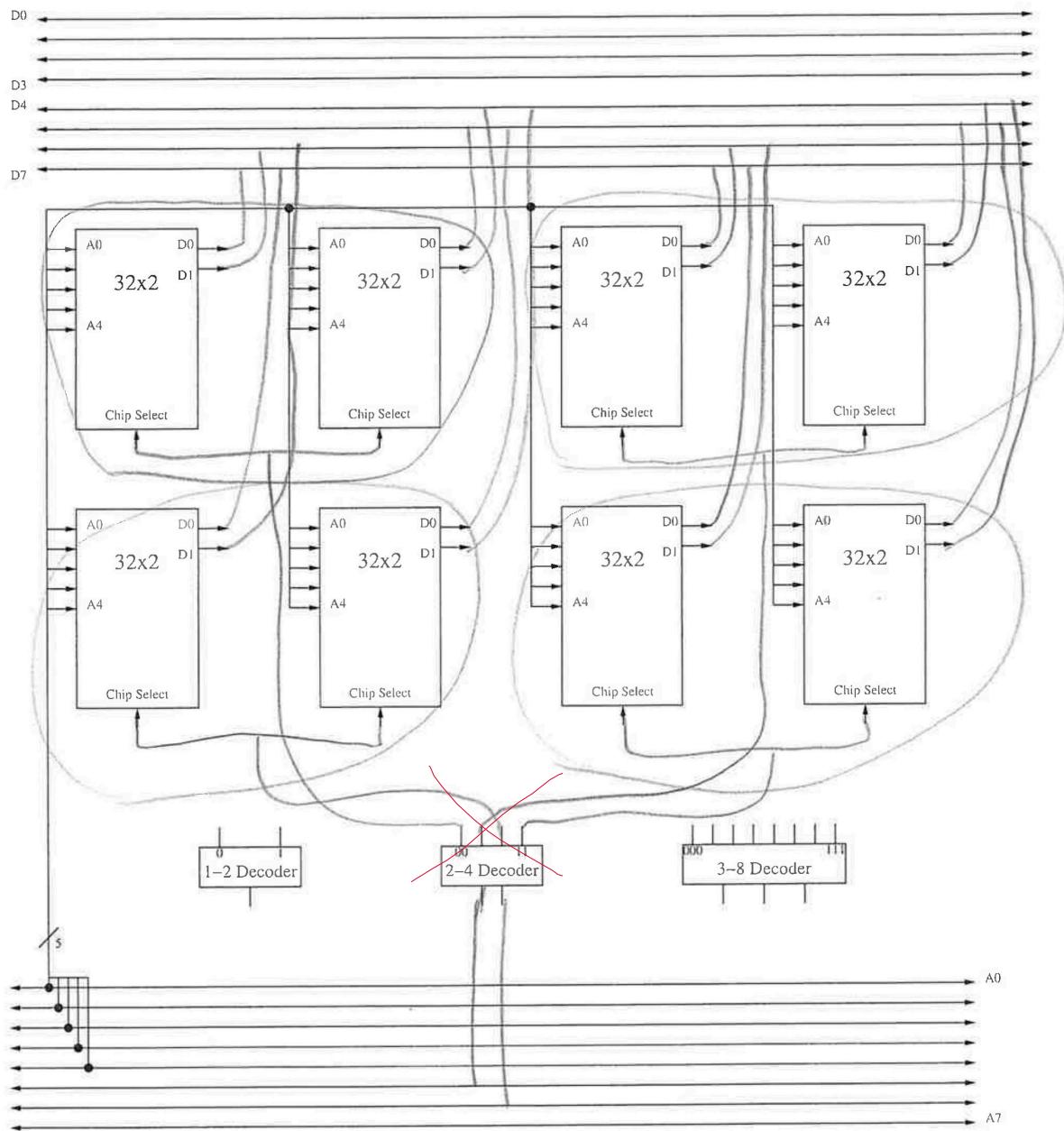
0x03A4 (0 0 0|0 0 0 1 1|1 0 1 0 0 1 0 0 in binary).

Presence bit for page 5 entry 3 is 0

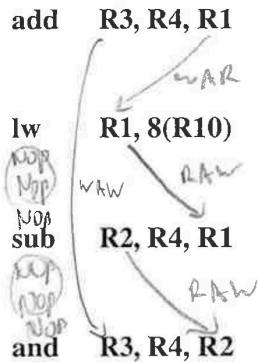
0x63A4 (0 1 1|0 0 0 1 1|1 0 1 0 0 1 0 0 in binary).

The presence bit for entry 3 of the segment table is 0

[8] Add the connections to the following diagram necessary to create a 64 byte memory (reminder - a "32x2" chip has 32 entries, each 2 bits wide). Not all of the hardware shown is required to perform this task.



Here is a code sequence. (Remember, operands are written Rdst, Rsrc1, Rsrc2)



[4] Indicate all data dependencies (draw lines/arrows between them).

Assuming a 6-stage pipeline (F, D, E1, E2, M, W) that does not support hazard detection and does no forwarding,

[4] Insert as many No Operations (NOPs) as required in order to ensure this code runs correctly. (Remember, writes to the register file occur on the first half of the W stage, and reads occur during the second half of the D stage).

[4] Circle the NOPs that can be removed if forwarding and hazard detection logic is implemented. Assume that data is ready after the E2 stage, and needed at the beginning of the E1 stage.

[3] What if the **add** instruction was a branch? Assuming the branch is resolved during E2 and found to be taken, how many instructions would have to be squashed?

2 instructions

Potentially useful information

F	D	E1	E2	M	W
○ F	D	E1	E2	M	W
○ F	D	E1	E2	M	W
○ F	D	E1	E2	M	W
	F	D	E1	E2	M W
	F	D	E1	E2	M W
	F	D	E1	E2	M W

$$\begin{aligned}
 2^4 &= 16 \\
 2^8 &= 256 \\
 2^{10} &= 1K \\
 2^{20} &= 1M \\
 2^{30} &= 1G
 \end{aligned}$$

$$\begin{aligned}
 0x1 &= 0001 \\
 0x2 &= 0010 \\
 0x4 &= 0100 \\
 0x8 &= 1000
 \end{aligned}$$

$$\begin{aligned}
 0xA &= 1010 \\
 0xC &= 1100 \\
 0xD &= 1110
 \end{aligned}$$

