

Registers

? Read

? Write

Control

? Halt

? Step

? Reset

? Break

Control

✓ Halt

✓ Step

✓ Reset

✓ Break

Memory

? Peek

? Poke

What Do We Need for a Debugger?

VexRiscv

Memory

? Peek
? Poke

Registers

? Read
? Write

Control

✓ Halt
✓ Step
✓ Reset
✓ Break

RISC-V Encoding

[Instruction]
add x0, x1, x0



[Conversion]

Assembly = add x0, x1, x0



Binary = 0000 0000 0000 0000 1000 0000 0011 0011



Hexadecimal = 0x00008033



Format = R-type

Instruction set = RV32I

<https://luplab.gitlab.io/rvcodecjs>