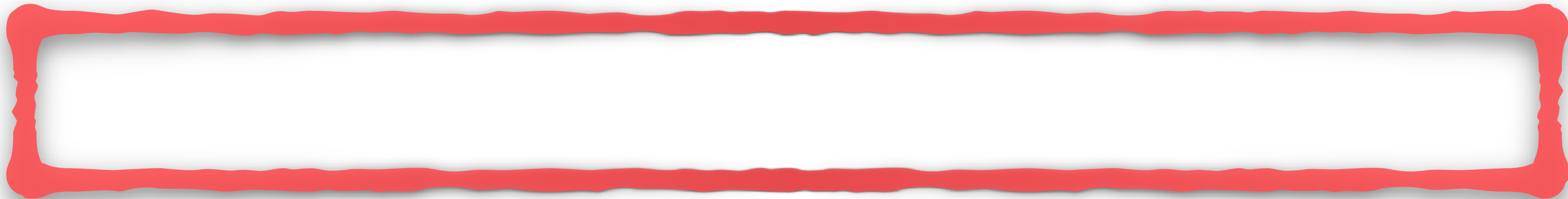| 4-bit IR instruction value	8-bit IR instruction value	Data register	DR scan length	Notes
0b0xxx	0b0xxxxxxx	-	-	*IMPLEMENTATION DEFINED extensions to the IR instruction set* on page B3-93.
-	0b10000000– 0b11110111	-	-	Reserved.
0b1000	0b11111000	ABORT	35	-
0b1001	0b11111001	-	-	Reserved.
0b1010	0b11111010	DPACC	35	See *DPACC and APACC, JTAG-DP DP, and AP Access registers* on page B3-98.
0b1011	0b11111011	APACC	35	
0b110x	0b1111110x	-	-	Reserved.
0b1110	0b11111110	IDCODE	32	-
0b1111	0b11111111	BYPASS	1	Required by JTAG specification.

Actually Using JTAG

Table B3-3 Standard IR instructions

4-bit IR instruction value	8-bit IR instruction value	Data register	DR scan length	Notes
0b0xxx	0b0xxxxxxx	-	-	*IMPLEMENTATION DEFINED extensions to the IR instruction set* on page B3-93.
-	0b10000000–0b11110111	-		Reserved.
0b1000	0b11111000	ABORT	35	-
0b1001	0b11111001	-	-	Reserved.
0b1010	0b11111010	DPACC	35	See *DPACC and APACC, JTAG-DP DP, and AP Access registers* on page B3-98.
0b1011	0b11111011	APACC	35	
0b110x	0b1111110x	-	-	Reserved.
0b1110	0b11111110	IDCODE	32	-
0b1111	0b11111111	BYPASS	1	Required by JTAG specification.

From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2

Actually Using JTAG
Bits on the wire

The operation of the DPACC and APACC registers is shown in the following figure: