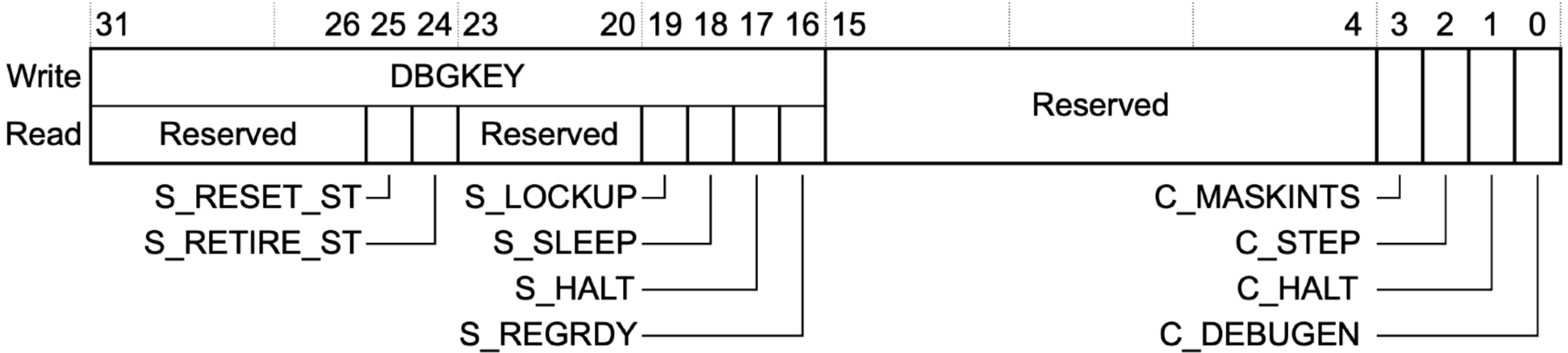
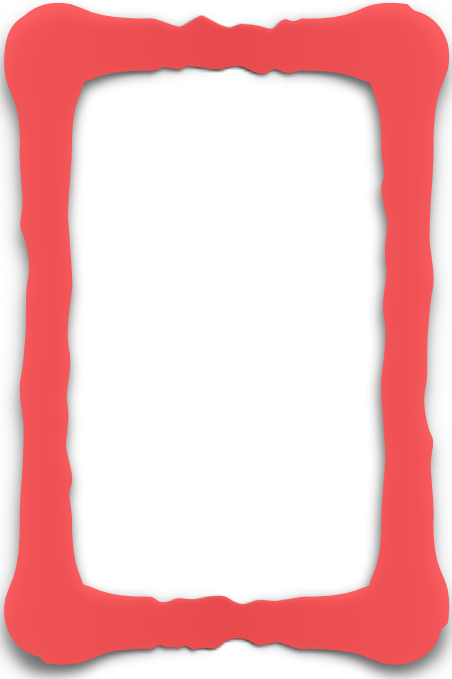


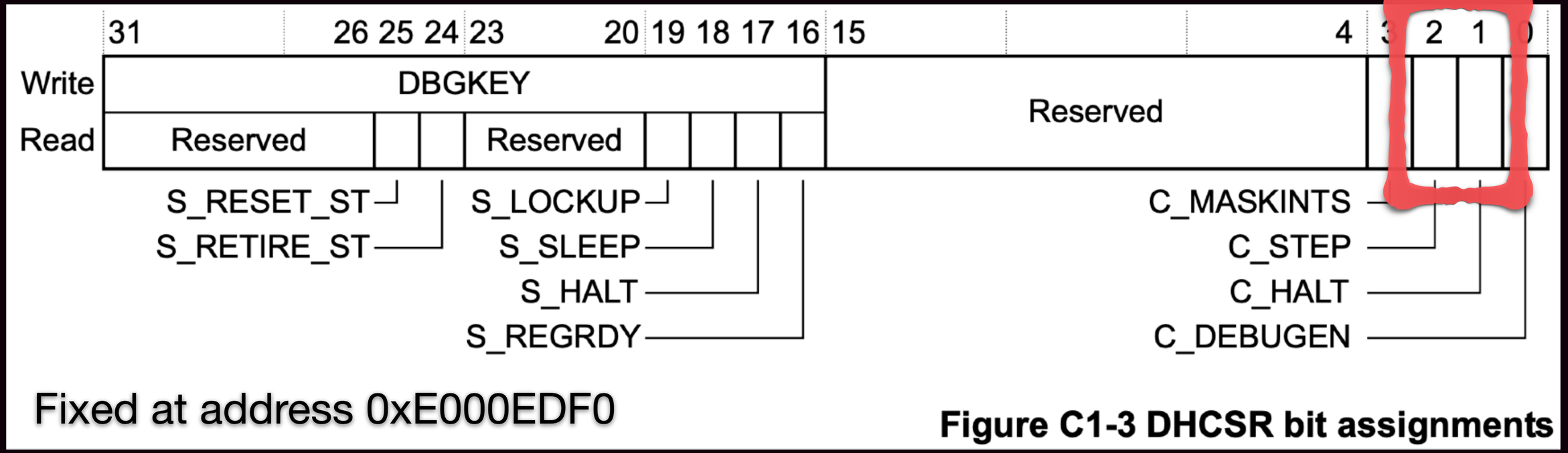
Figure C1-3 DHCSR bit assignments

Fixed at address 0xE000EDF0



CPU Control: Memory Mapping

DHCSR: Debug Halting, Control, and Status Register



Fixed at address 0xE000EDF0

Figure C1-3 DHCSR bit assignments

From: ARMv6-M Architecture Reference Manual

What Do We Need for a Debugger?

ARM Cortex-M via ADIv5 / MEM-AP