CPU Control: Memory Mapping

Controlling the CPU from RAM

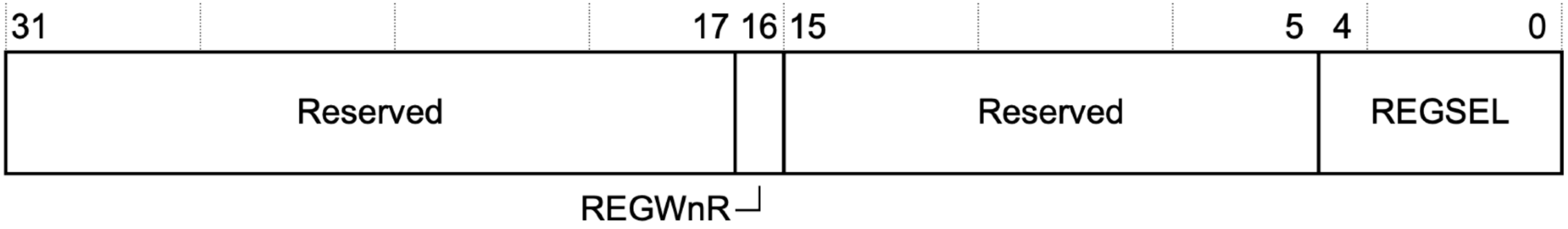
Table C1-10 DCB register summary

Address	Name	Type	Function
0xE000EDF0	DHCSR	RW	*Debug Halting Control and Status Register, DHCSR* on page C1-287.
0xE000EDF4	DCRSR	WO	*Debug Core Register Selector Register, DCRSR* on page C1-290.
0xE000EDF8	DCRDR	RW	*Debug Core Register Data Register, DCRDR* on page C1-292.

From: ARMv6-M Architecture Reference Manual

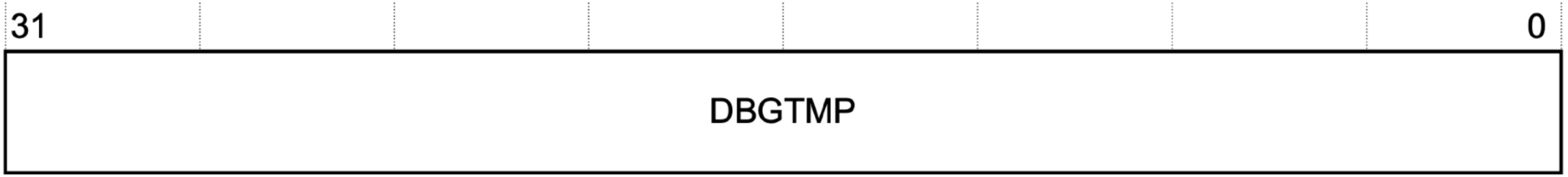
CPU Control: Memory Mapping

DCRDR/DCRSR: Debug Core Register Data / Selector Registers



Fixed at address 0xE000EDF4

Figure C1-4 DCRSR bit assignments



Fixed at address 0xE000EDF8

Figure C1-5 DCRDR bit assignments

From: ARMv6-M Architecture Reference Manual