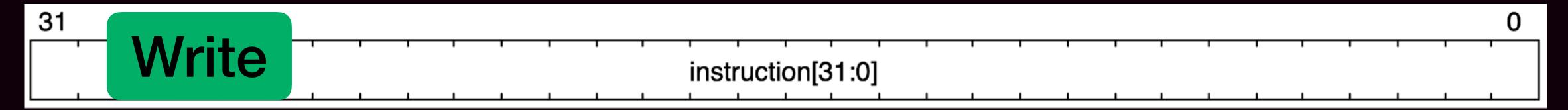
## RISC-V Encoding

```
[ Instruction ]
                  add x0, x1, x0
 Conversion ]
        Assembly = add x0, x1, x0
                     0000 0000 0000 0000 1000 0000 0011 0011
          Binary =
      Hexadecimal =
                     0x00008033
          Format =
                     R-type
  Instruction set =
                     RV32I
https://luplab.gitlab.io/rvcodecjs
```

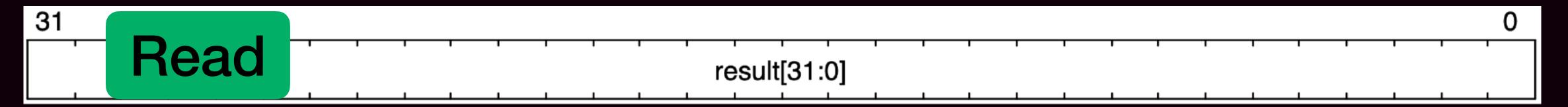
## VexRiscv Debug Interface

DebugPlugin.scala

## 0x04: Inject Instruction



## 0x04: RISC-V Rd Value



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