
Registers
? Read
? Write


Registers
✓ Read
✓ Write

Memory

? Peek

? Poke

Control

- ✓ Halt
- ? Step
- ✓ Reset
- ? Break

What Do We Need for a Debugger?

RISC-V Debug Specification

Memory	Registers	Control
? Peek	✓ Read	✓ Halt
? Poke	✓ Write	? Step
		✓ Reset
		? Break

“In order to be compatible with this specification an implementation must:

…

2. Implement at least one of Program Buffer, System Bus Access, or Abstract Access Memory

…

”

The RISC-V Debug Specification, Version 1.0.0-rc3