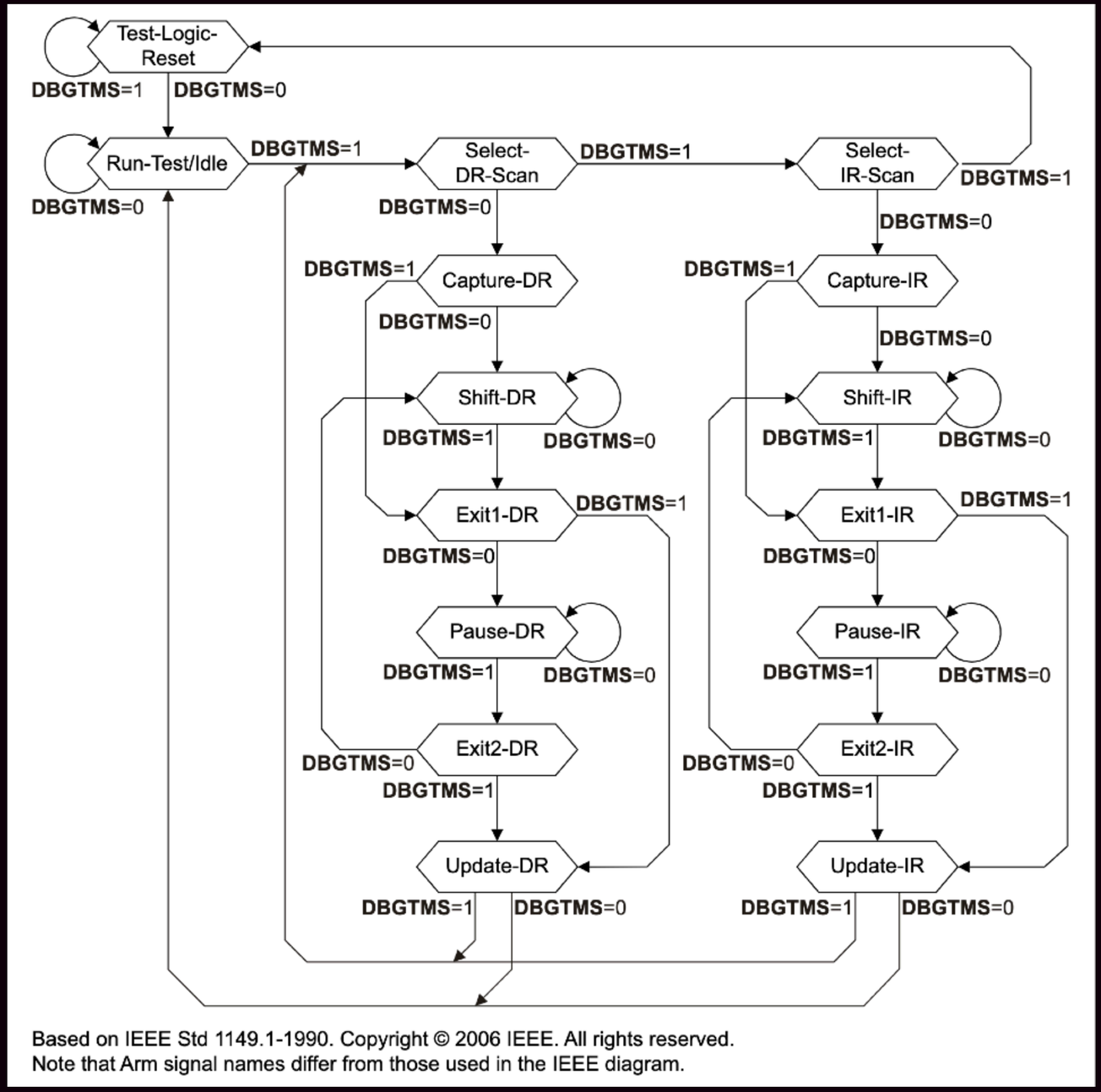
JTAG Overview

Whirlwind Tour

- 4 Wires: TCK, TDO, TDI, TMS
- Data captured on TCK rising edge



Based on IEEE Std 1149.1-1990. Copyright © 2006 IEEE. All rights reserved.
Note that Arm signal names differ from those used in the IEEE diagram.

From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2

JTAG (abridged)

Four states of operation

1. Two registers: IR (Instruction Register) and DR (Data Register)
2. Change states with a sequence of TMS patterns