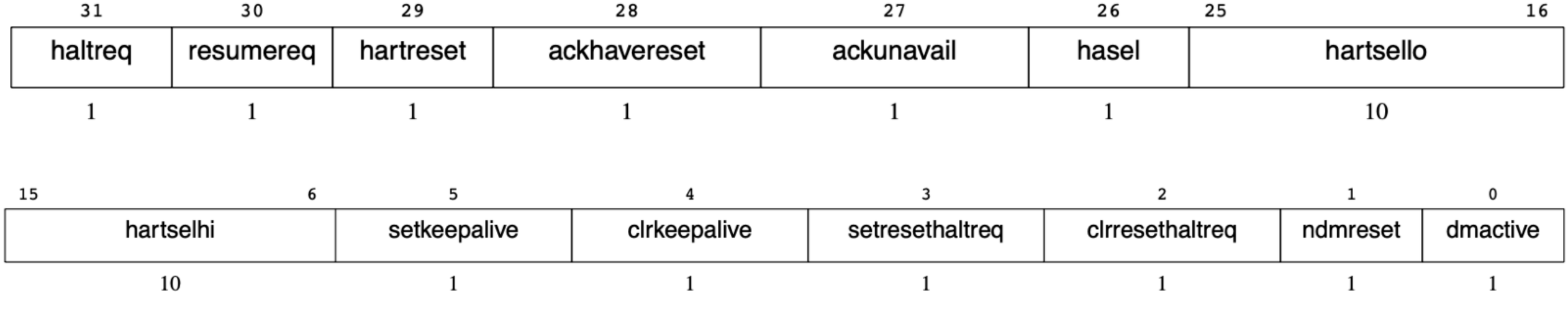
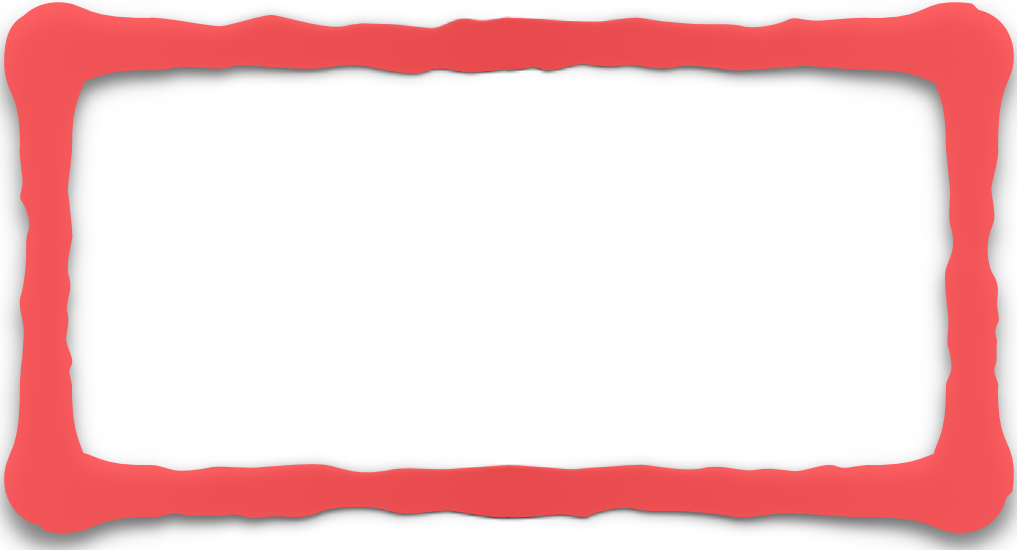
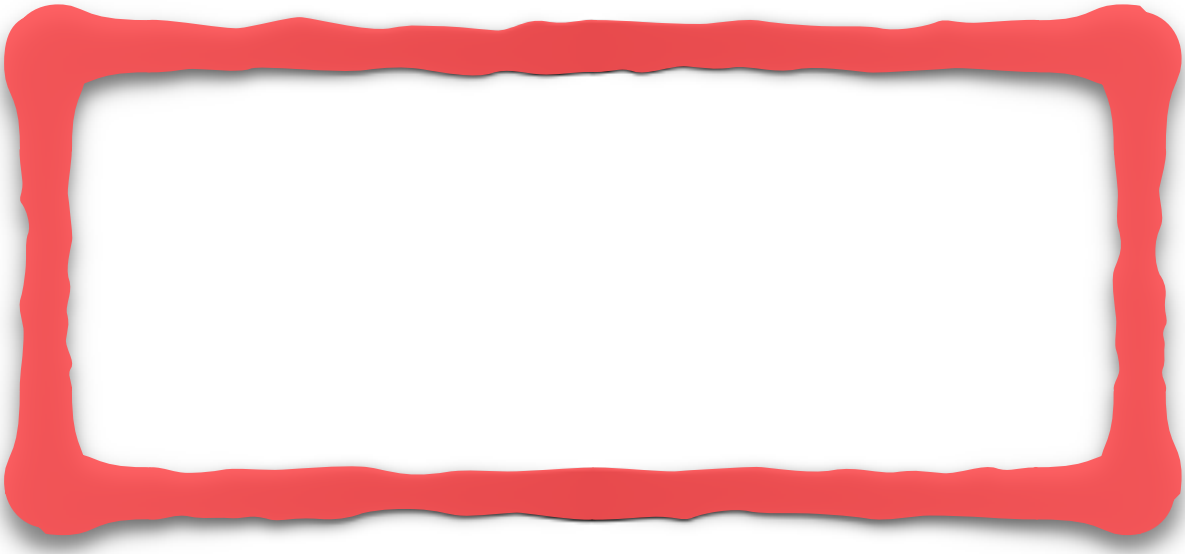
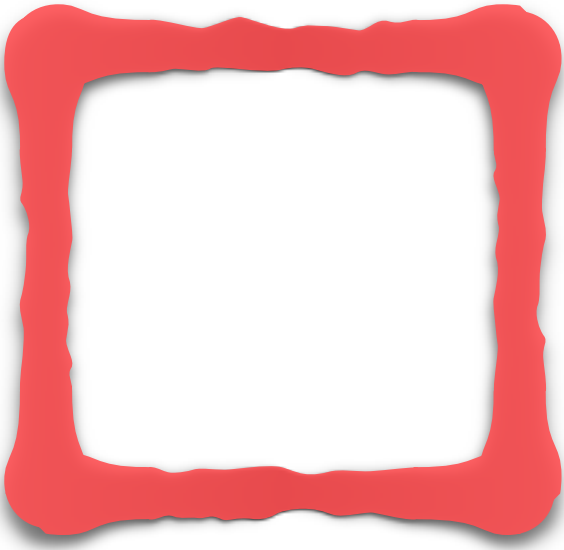

31
30
29
28
27
26
25
16
haltreq
resumereq
hartreset
ackhavereset
ackunavail
hasel
hartsello
1
1
1
1
1
1
10
15
6
5
4
3
2
1
0
hartselhi
setkeepalive
clrkeepalive
setresethaltreq
clrresethaltreq
ndmreset
dmactive
10
1
1
1
1
1
1

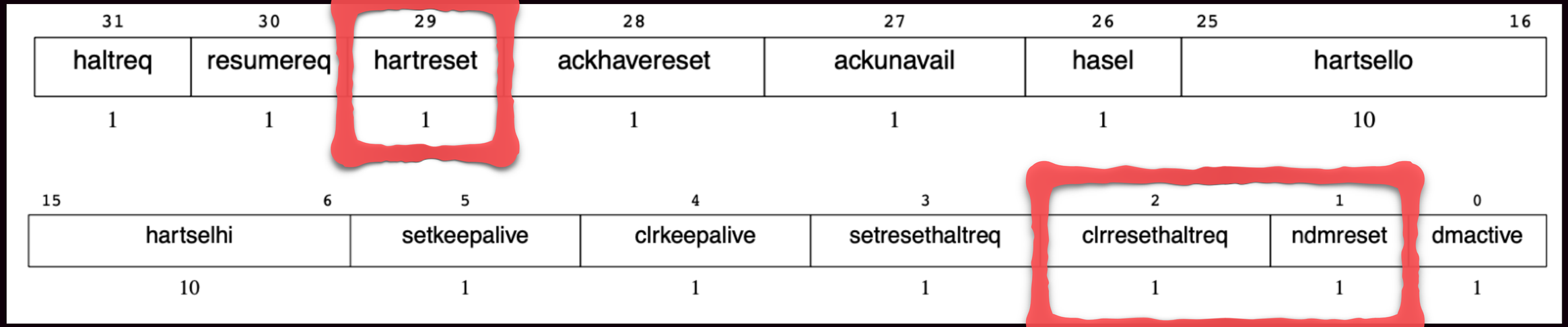






Debug Module Control

`dmcontrol: 0x10`



31	30	29	28	27	26	25 … 16
haltreq	resumereq	hartreset	ackhavereset	ackunavail	hasel	hartsello
1	1	1	1	1	1	10

15 … 6	5	4	3	2	1	0
hartselhi	setkeepalive	clrkeepalive	setresethaltreq	clrresethaltreq	ndmreset	dmactive
10	1	1	1	1	1	1

What Do We Need for a Debugger?

RISC-V Debug Specification

Memory	Registers	Control
? Peek	? Read	? Halt
? Poke	? Write	? Step
		? Reset
		? Break