The RISC-V Debug Specification

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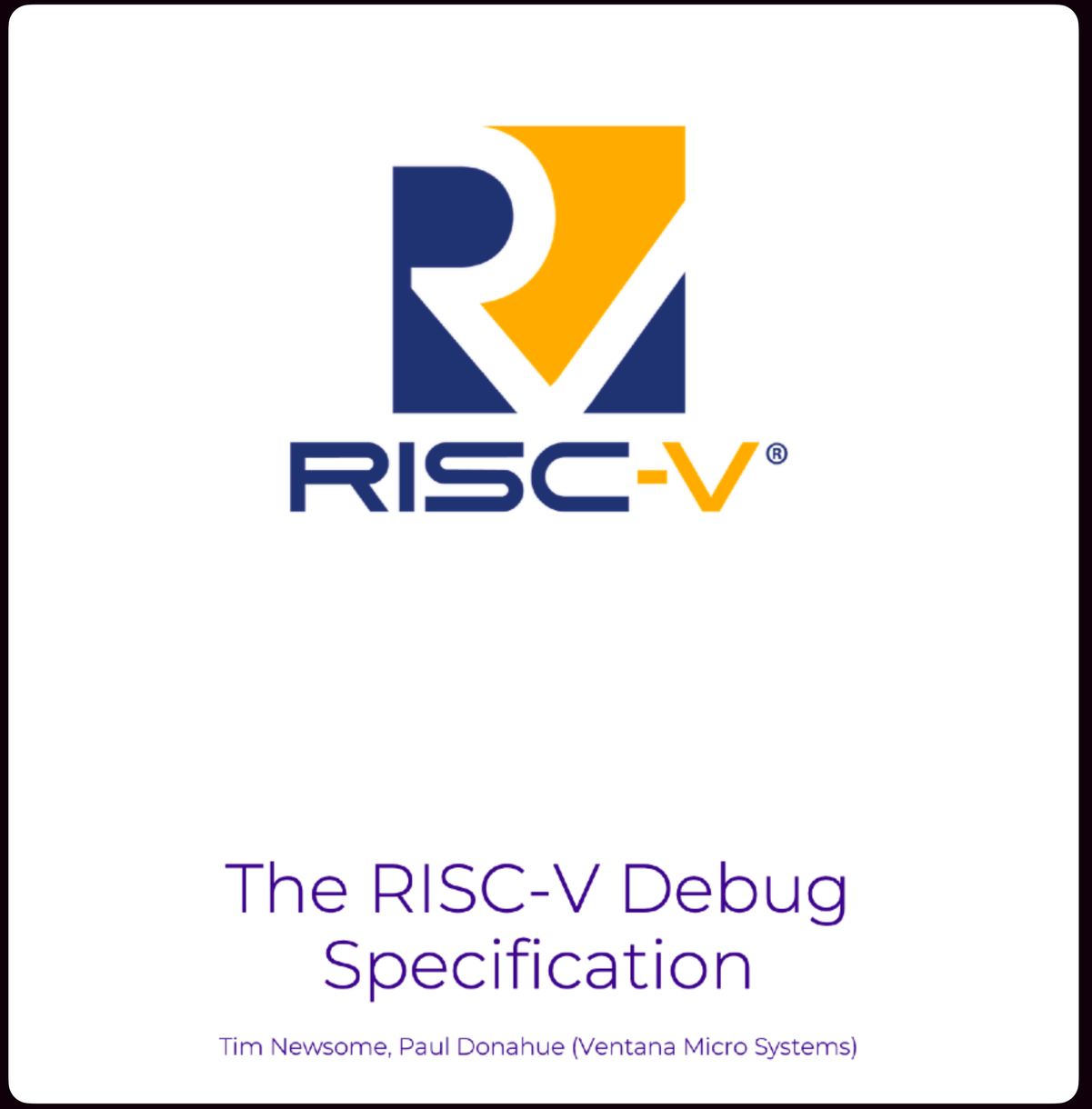
RISC-V Debug

Three different specifications in a trench coat



RISC-V JTAG Addresses

Address	Name	Description	Section
0x00	bypass	JTAG recommends this encoding	
0x01	idcode	To identify a specific silicon version	Section 6.1.3
0x10	DTM Control and Status (dtmcs)	For Debugging	Section 6.1.4
0x11	Debug Module Interface Access (dmi)	For Debugging	Section 6.1.5
0x12	reserved (bypass)	Reserved for future RISC-V debugging	
0x13	reserved (bypass)	Reserved for future RISC-V debugging	
0x14	reserved (bypass)	Reserved for future RISC-V debugging	
0x15	reserved (bypass)	Reserved for future RISC-V standards	
0x16	reserved (bypass)	Reserved for future RISC-V standards	
0x17	reserved (bypass)	Reserved for future RISC-V standards	
0x1f	bypass	JTAG requires this encoding	Section 6.1.6