DPACC

Data[31:0]	A[3:2]	RnW

APACC

Data[31:0]	A[3:2]	RnW

DP Registers[a]

0x00	0x04	0x08	0x0C
DATA LINK DEFINED	Control/Status (CTRL/STAT)	AP Select (SELECT)	Read Buffer (RDBUFF)

Generic Debug Port (DP)

[a] This is only a partial view of the DP registers. For more information, see chapter *DP Reference Information*.

Debug Port

APACC

DPACC

DP Access

Debug Port (DP)

Access Result and Status

APSEL decode

Data[31:0]	A[7:4]	A[3:2]	RnW

A[7:4] selects the register bank
A[3:2] selects register within bank

AP Access

AP Access

Access Port (AP)

Bank 0x0	0x00	0x04	0x08	0x0C	Bank 0x1	0x10	0x14	0x18	0x1C		Bank 0xF	0xF0	0xF4	0xF8	0xFC
	Control/Status Word (CSW)	Transfer Address (TAR)	Reserved	Data Read/Write (DRW)		Banked Data 0 (BD0)	Banked Data 1 (BD1)	Banked Data 2 (BD2)	Banked Data 3 (BD3)			Reserved	Configuration Reg. (CFG)	Debug Base Addr. (BASE)	Identification Register (IDR)

Address incrementer

Memory Access Port (MEM-AP)

Memory Access Port

Resource-specific Access

Resource-specific transport

Debug address decode

Addr[31:2]	Data[31:0]	RnW

Processor 4KB block

0x000	0x004	0x008	0x00C	0xFFC
Register 0	Register 1	Register 2	Register 3	Register 1023

ETM 4KB block

0x000	0x004	0x008	0x00C	0xFFC
Register 0	Register 1	Register 2	Register 3	Register 1023

ROM Table 4KB block

0x000	0x004	0x008	0x00C
Processor address	ETM address	0x00000000	Reserved

Debug Register Files

Resource Debug Registers

Note: Register field widths are not to scale.
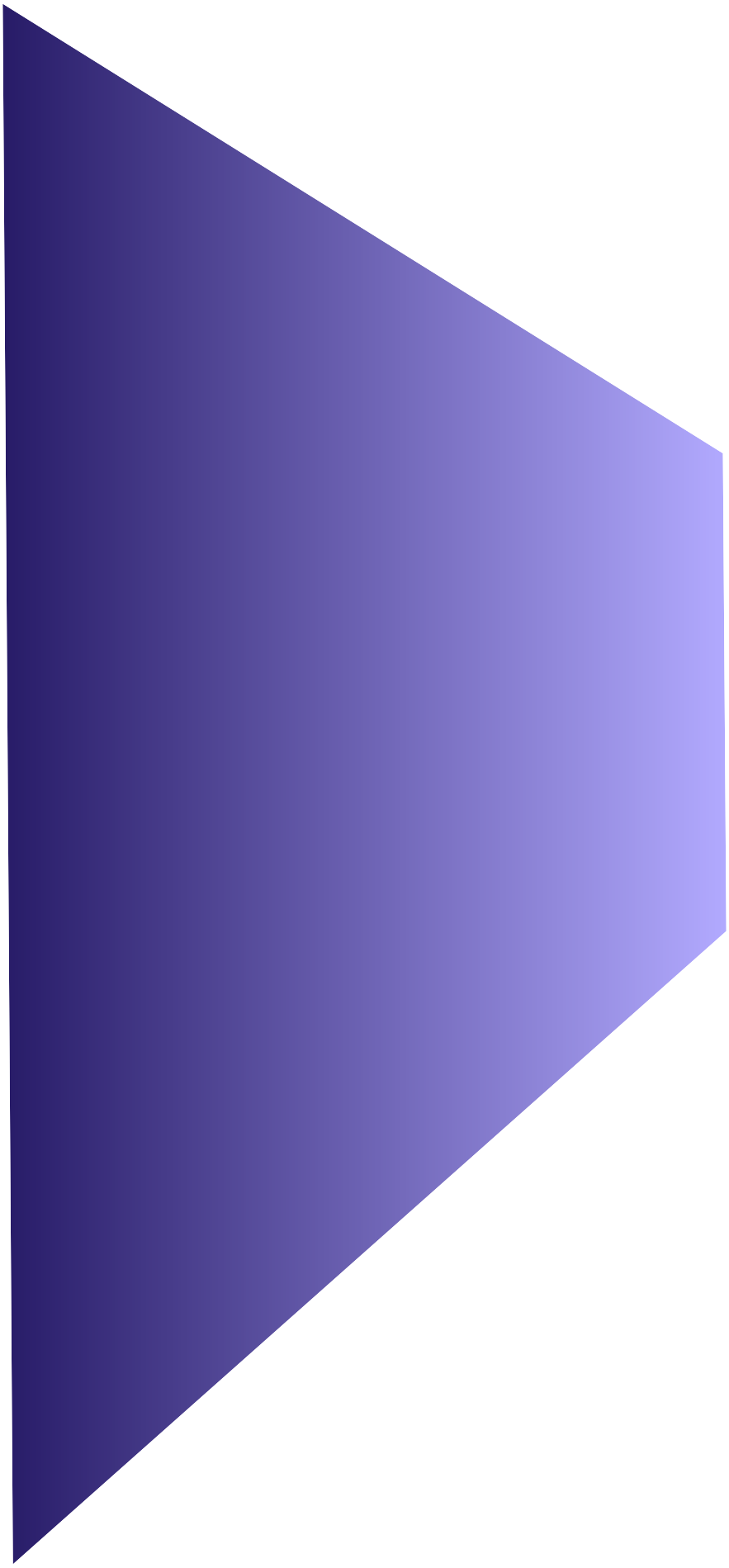
Bank 0x0	Control/Status Word (CSW)	0x00
	Transfer Address (TAR)	0x04
	Reserved	0x08
	Data Read/Write (DRW)	0x0C

CSW

TAR

TAR_HI

BDO

BD1

BD2

BD3

BASE_HI

CFG

BASE