
Memory
? Peek
? Poke


Registers
✓ Read
✓ Write

Memory

- ✓ Peek
- ✓ Poke

Control

- ✓ Halt
- ? Step
- ✓ Reset
- ? Break

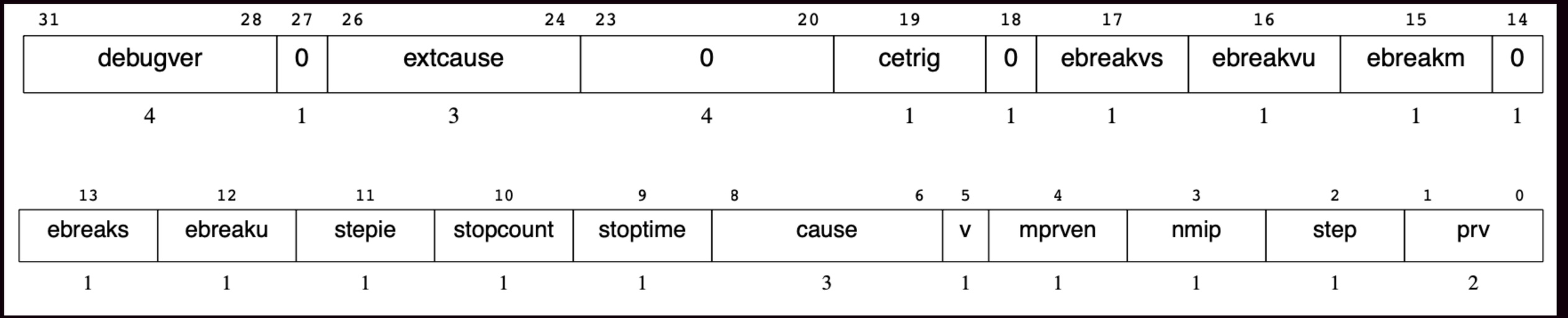
What Do We Need for a Debugger?

RISC-V Debug Specification

Memory	Registers	Control
✓ Peek	✓ Read	✓ Halt
✓ Poke	✓ Write	? Step
		✓ Reset
		? Break

Debug Control and Status Register

`dcsr`: 0x7b0



- step: set this bit to single-step
- cause: 1 is **`ebreak`**, 3 is debug request, 4 is step