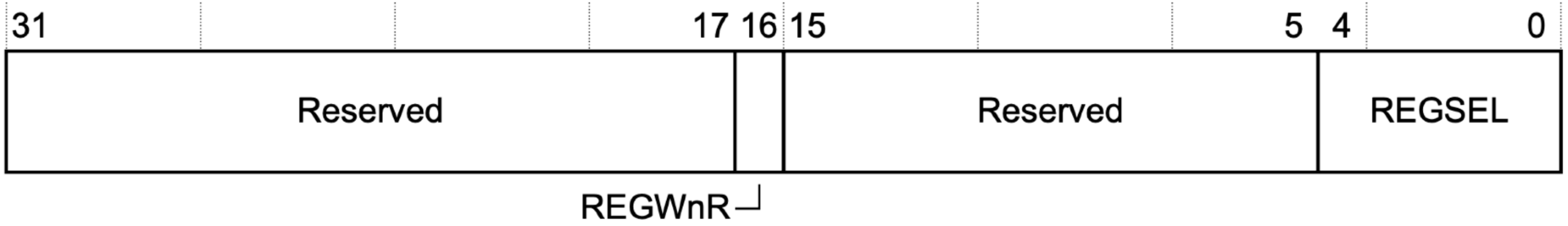


Figure C1-4 DCRSR bit assignments

Fixed at address 0xE000EDF4

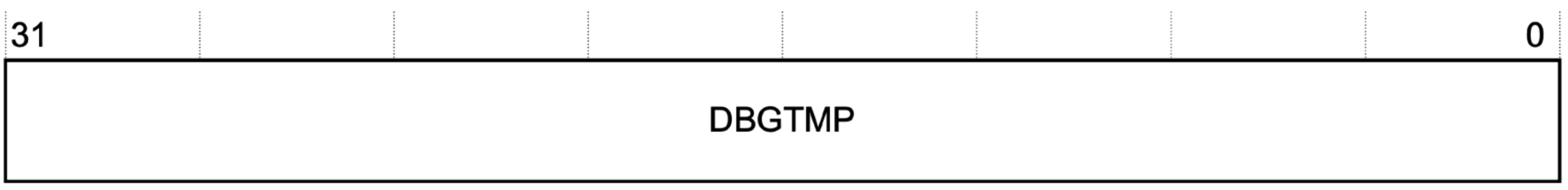
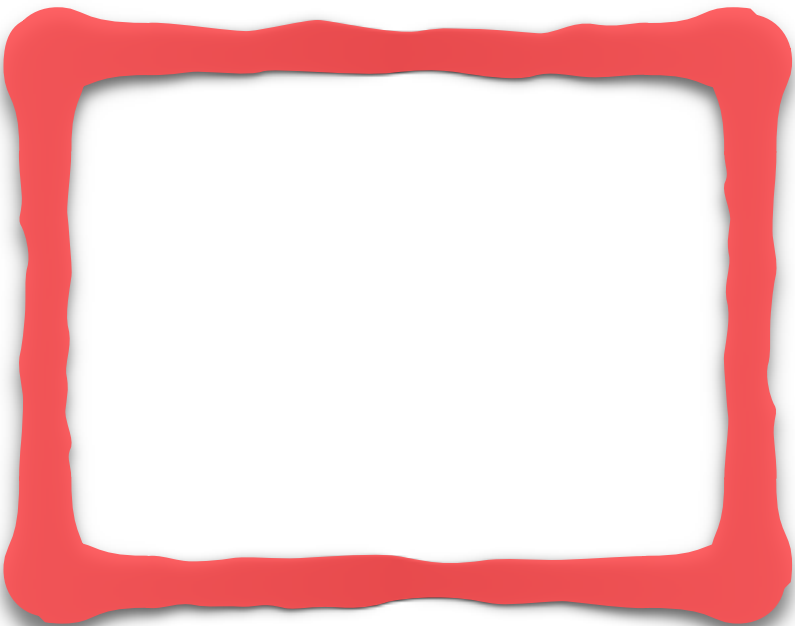
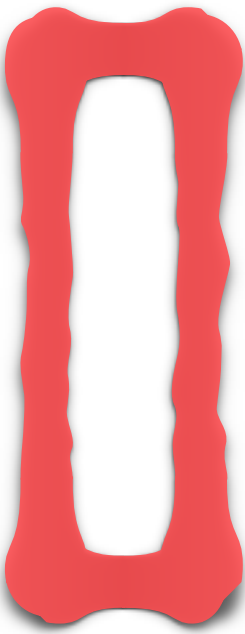
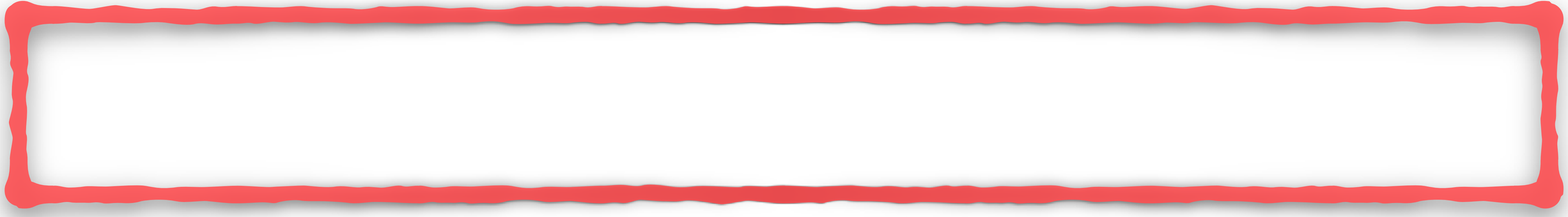


Figure C1-5 DCRDR bit assignments

Fixed at address 0xE000EDF8

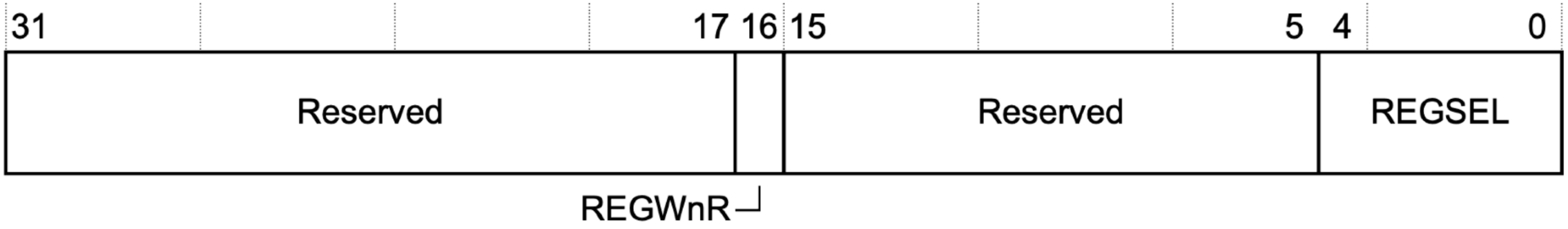






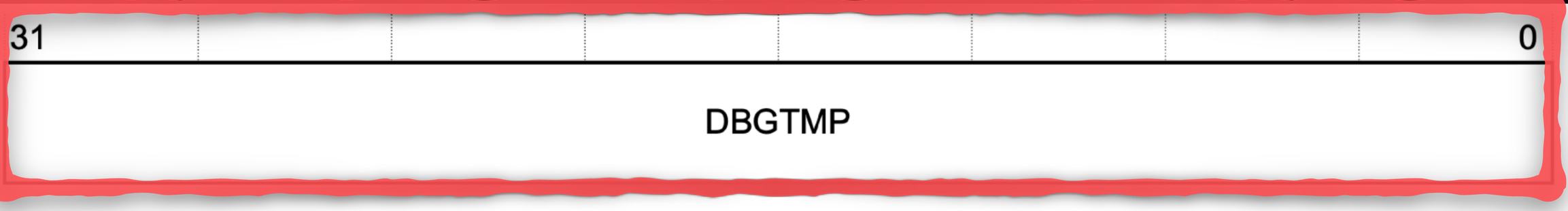
CPU Control: Memory Mapping

DCRDR/DCRSR: Debug Core Register Data / Selector Registers



Fixed at address 0xE000EDF4

Figure C1-4 DCRSR bit assignments



Fixed at address 0xE000EDF8

Figure C1-5 DCRDR bit assignments

From: ARMv6-M Architecture Reference Manual

What Do We Need for a Debugger?

ARM Cortex-M via ADIv5 / MEM-AP

Memory

- ★ Peek
- ★ Poke

Registers

- ? Read
- ? Write

Control

- ? Halt
- ? Step
- ? Reset
- ? Break