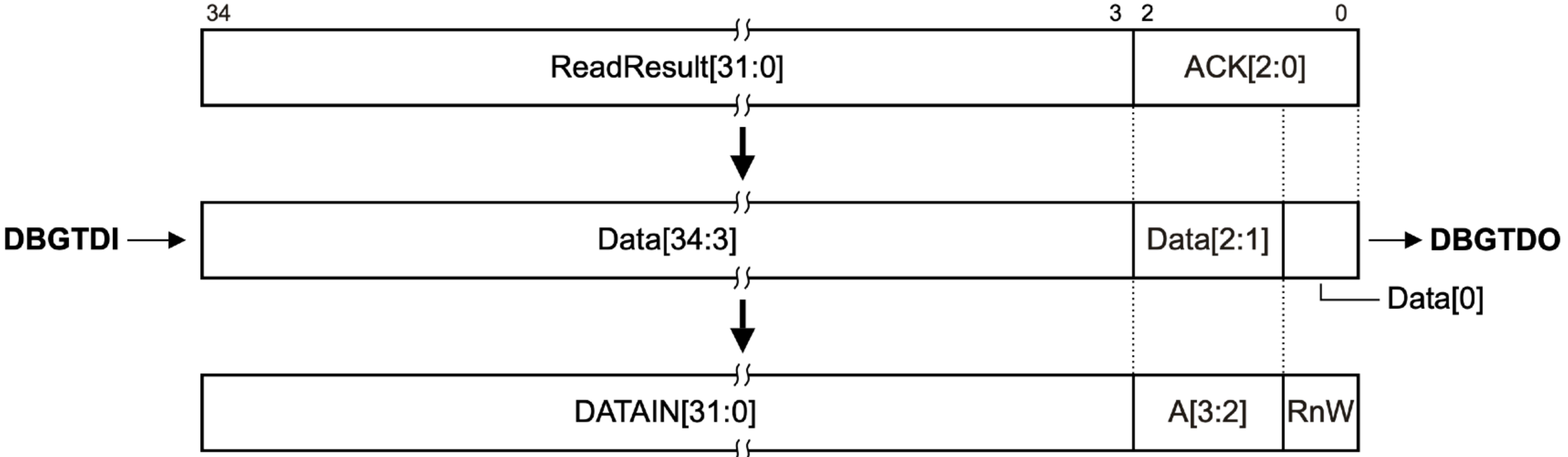
The operation of the DPACC and APACC registers is shown in the following figure:



Read

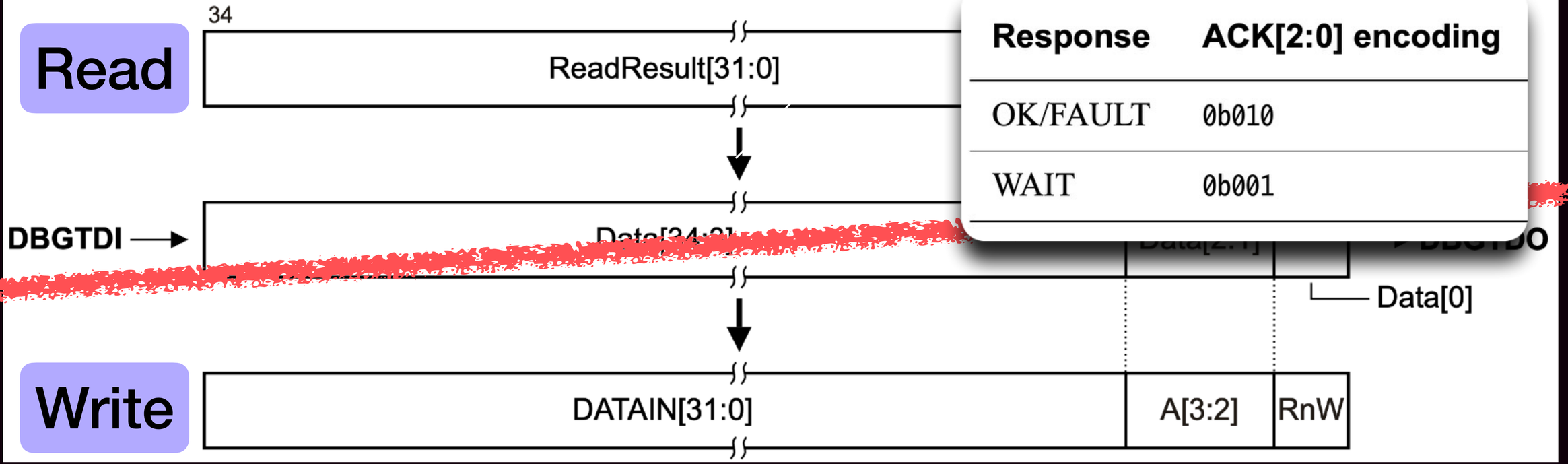
Write

Response	ACK[2:0] encoding
OK/FAULT	0b010
WAIT	0b001

Actually Using JTAG

Bits on the wire

The operation of the DPACC and APACC registers is shown in the following figure:



Response	ACK[2:0] encoding
OK/FAULT	0b010
WAIT	0b001

From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2

The DPACC Register

A[b]	Sticky?[c]	AP state[d]	Read result	ACK	
X	X	Busy	UNKNOWN	WAIT	If the Overrun Detect flag is `0b1`, this access and response sequence causes the Sticky Overrun flag to be set to `0b1`. See *CTRL/STAT, Control/Status register* on page B2-55.
`0b00`	X	Not Busy	UNKNOWN	OK/ FAULT	The return value depends on the DP version: **DPv1, DPv2** Returns the value of DPIDR. **DPv0** Returns UNKNOWN value.
`0b01`			CTRL/STAT		Returns CTRL/STAT value.
`0b10`			SELECT		Returns SELECT value.
`0b11`			`0x00000000`		Returns RDBUFF value, always zero.

From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2