### Memory

? Peek? Poke



# Registers



### Memory



### Control

✓ Halt ? Step Reset ? Break

#### What Do We Need for a Debugger?

RISC-V Debug Specification

### Memory

- Peek
- Poke

# Registers

- Read
- Write

### Control

- ✓ Halt
- ? Step
- Reset
- ? Break

#### Debug Control and Status Register

dcsr: 0x7b0

_ 3	1	28	27	26	24	23		20	19		18	17		16		15	14
	debug	gver	0	ex	tcause		)		cetrig		0	ebreak	vs ebr	eakvu	ebre	eakm	0
	4		1		3	4	1		1		1	1	•	1		1	1
	13	12		11	10	9	8		6	5		4	3	2		1	0
	ebreaks	ebreaku		stepie	stopcount	stoptime		cause		V	m	prven	nmip	ste	ер	prv	,
	1	1		1	1	1		3		1		1	1	1		2	

- step: set this bit to single-step
- cause: 1 is ebreak, 3 is debug request, 4 is step