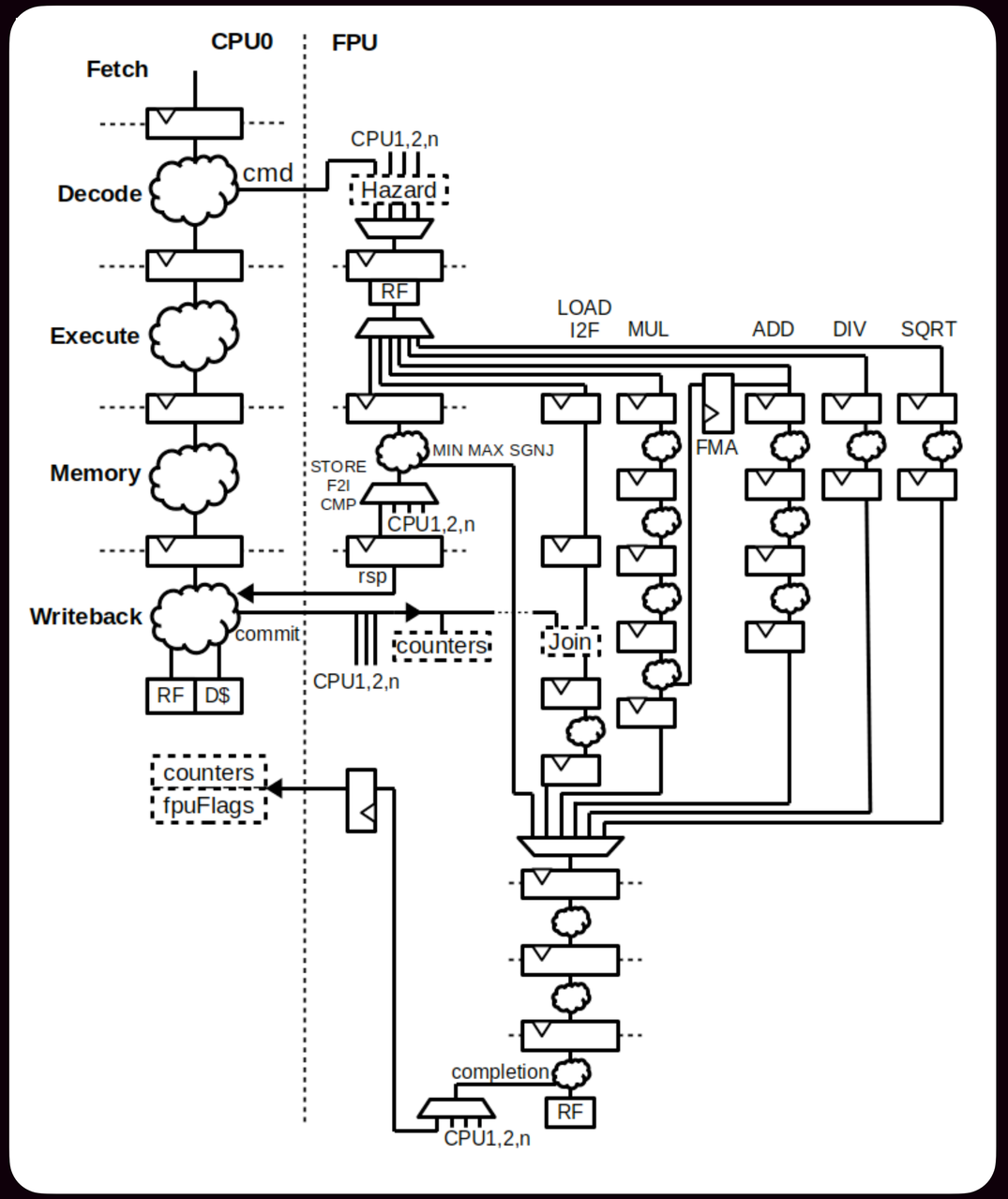
VexRiscv: A CPU in Scala

FPGA-targeted soft core

- 32-bit RISC-V core
- Plugin support
- FPUPlugin.scala
- DebugPlugin.scala
  - Only two registers!

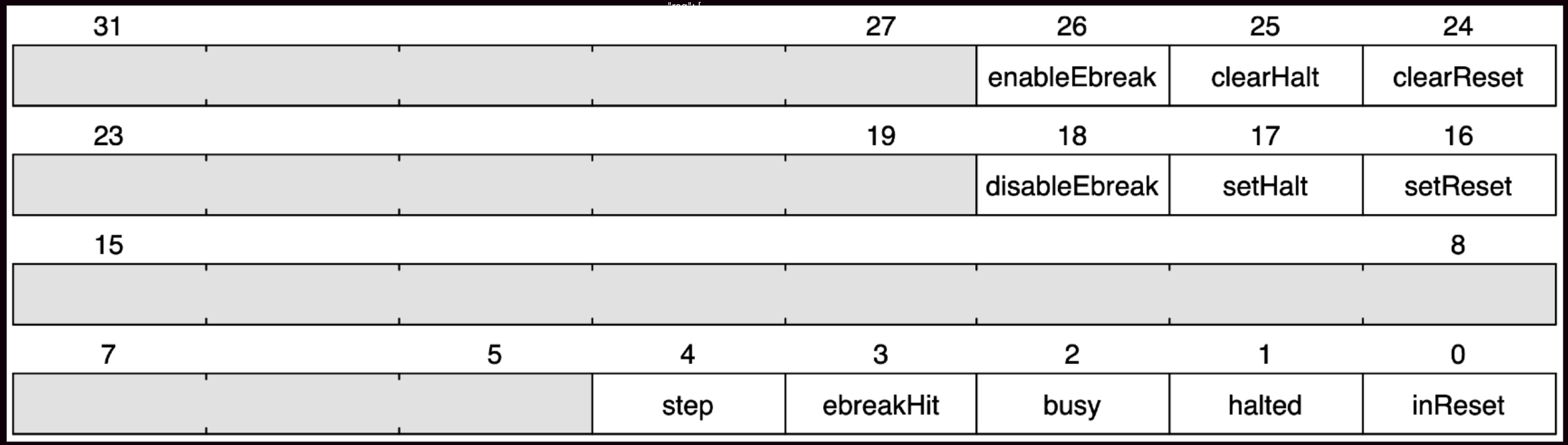


From: VexRiscv README.md

VexRiscv Debug Interface

DebugPlugin.scala

0x00: CPU control



Fomu Reference Manual — https://rm.fomu.im/