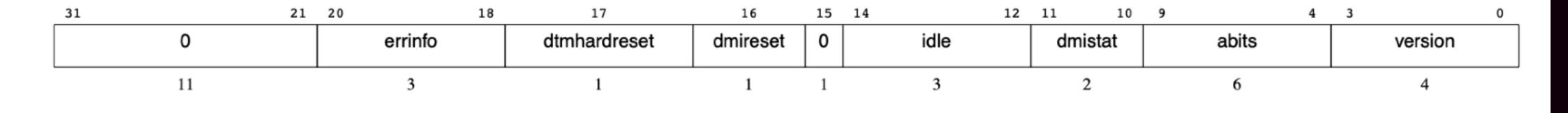
DTM Control and Status Register

JTAG dtmcs: 0x10

6.1.4. DTM Control and Status (dtmcs, at 0x10)

The size of this register will remain constant in future versions so that a debugger can always determine the version of the DTM.



- idle number of JTAG cycles to wait between commands
- abits size of address in DMI
- version revision of debug standard

Debug Module Interface

JTAG dmi: 0x11

0: success

2: failed

3: busy

abits+33	34	33	1	0
address		data		ор
abits		32	•	2

address: 7-32 bits data: 32 bits read/write 0: ig

0: ignore

1: read

2: write