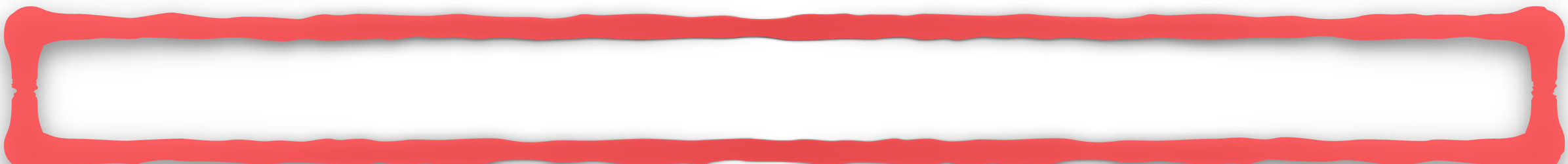
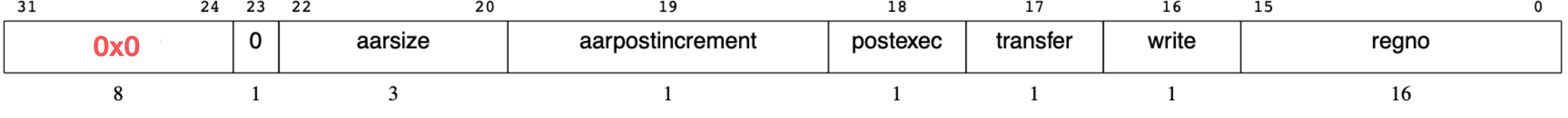
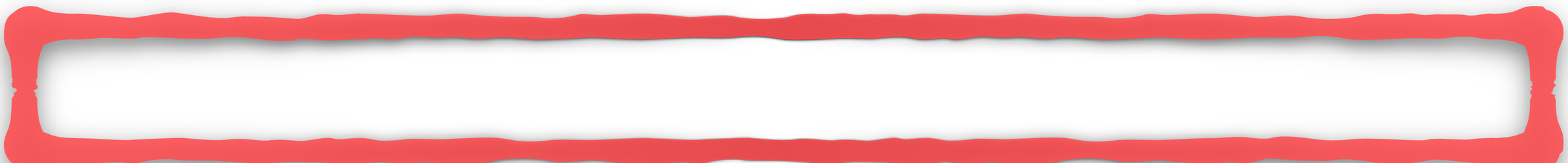
Numbers	Group Description
0x0000 — 0x0fff	CSRs. The `PC" can be accessed here through dpc.
0x1000 — 0x101f	GPRs
0x1020 — 0x103f	Floating point registers
0xc000 — 0xffff	Reserved for non-standard extensions and internal use.




31
24
23
22
20
19
18
17
16
15
0
0x0
0
aarsize
aarpostincrement
postexec
transfer
write
regno
8
1
3
1
1
1
1
16



Accessing CSRs

Control and Status Registers from RISC-V

Numbers	Group Description
0x0000 — 0x0fff	CSRs. The `PC" can be accessed here through dpc.
0x1000 — 0x101f	GPRs
0x1020 — 0x103f	Floating point registers
0xc000 — 0xffff	Reserved for non-standard extensions and internal use.

“In order to be compatible with this specification an implementation must:

…

3. Do at least one of:
    a. Implement the Program Buffer
    b. Implement Abstract Access to all registers…
    c. Implement Abstract Access to all GPRs, dcsr, and dpc…

”

The RISC-V Debug Specification, Version 1.0.0-rc3

What Do We Need for a Debugger?

RISC-V Debug Specification

Memory	Registers	Control
✓ Peek	✓ Read	✓ Halt
✓ Poke	✓ Write	? Step
		✓ Reset
		? Break