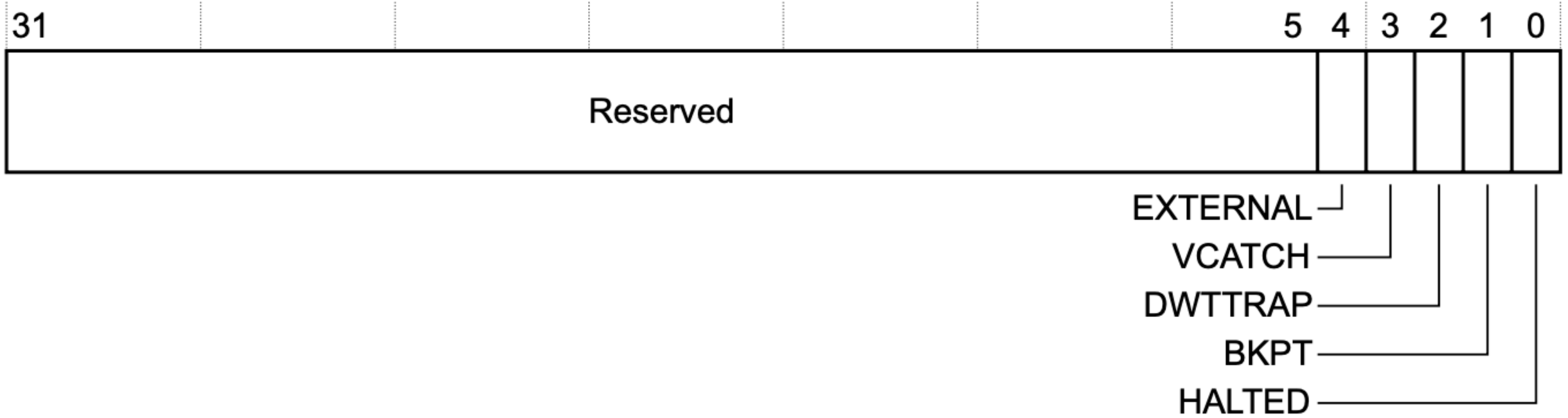
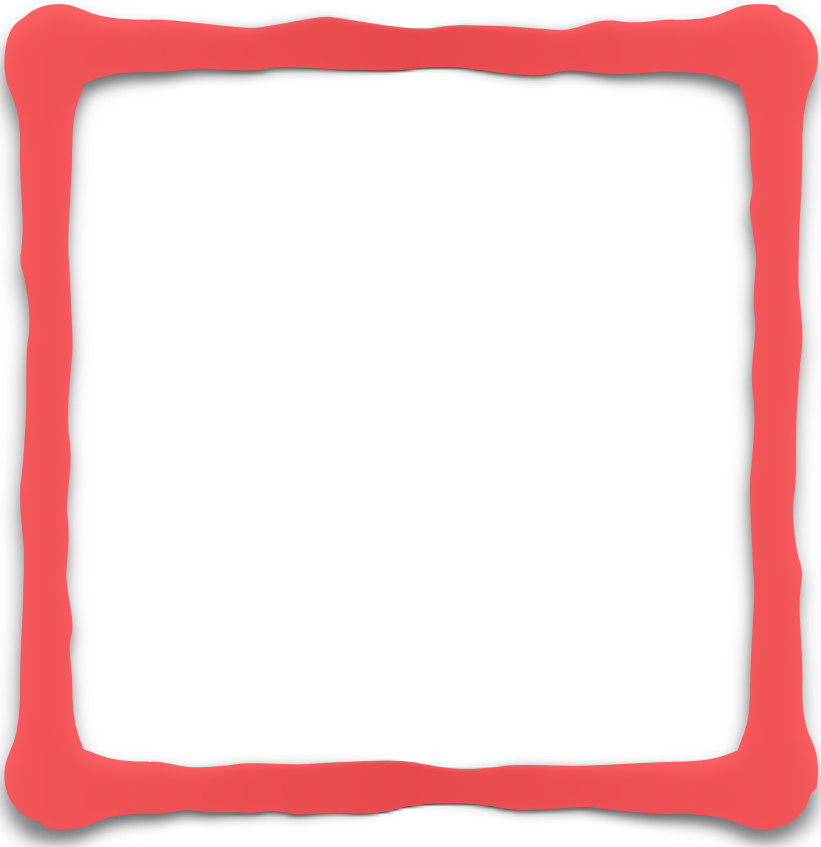


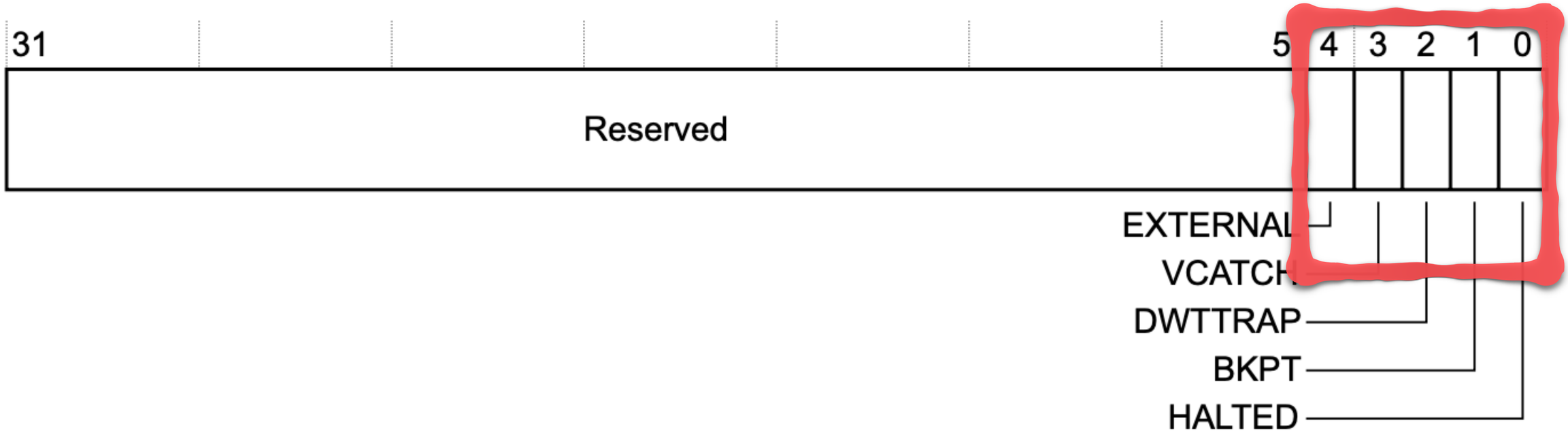
Figure C1-2 DFSR bit assignments



Fixed at address 0xE000ED30

CPU Control: Memory Mapping

DFSR: Debug Fault Status Register



Fixed at address 0xE000ED30

Figure C1-2 DFSR bit assignments

From: ARMv6-M Architecture Reference Manual

What Do We Need for a Debugger?

ARM Cortex-M via ADIv5 / MEM-AP

Memory

- ★ Peek
- ★ Poke

Registers

- ✓ Read
- ✓ Write

Control

- ✓ Halt
- ✓ Step
- ✓ Reset
- ? Break