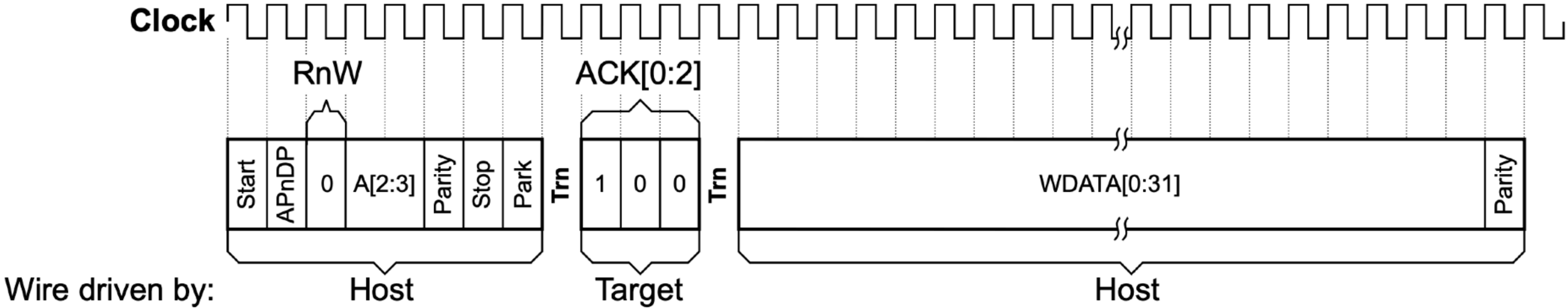
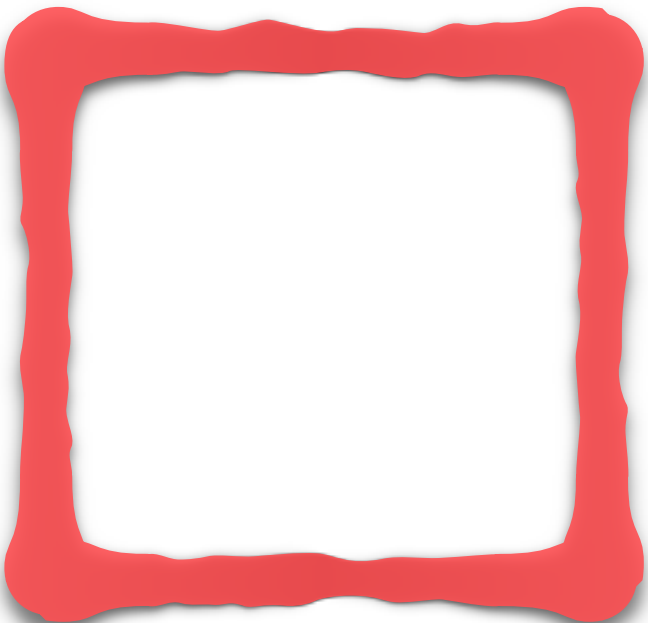
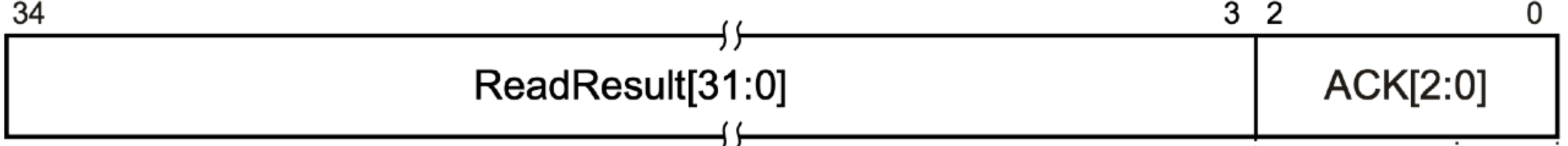

Clock
RnW
ACK[0:2]
Start
APnDP
0
A[2:3]
Parity
Stop
Park
Trn
1
0
0
Trn
WDATA[0:31]
Parity
Wire driven by:
Host
Target
Host



DATAIN[31:0]
A[3:2]
RnW

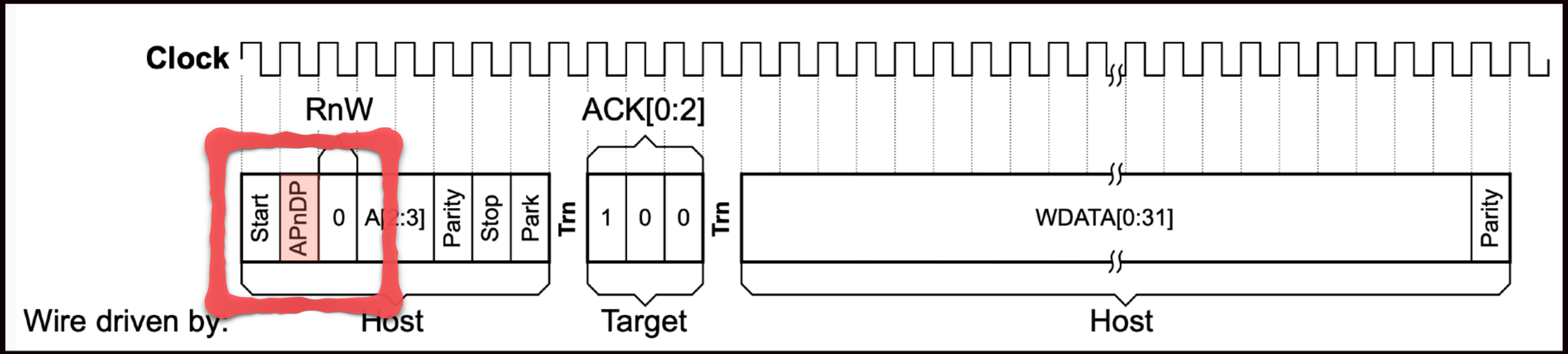

34
3
2
0
ReadResult[31:0]
ACK[2:0]

0b1010	0b11111010	DPACC	35	See *DPACC and APACC, JTAG-DP DP, and AP Access registers* on page B3-98.
0b1011	0b11111011	APACC	35	

ACK[0:2] encoding	Response
0b100	OK
0b010	WAIT
0b001	FAULT

SWD Protocol: Write

Similar wire representation to JTAG

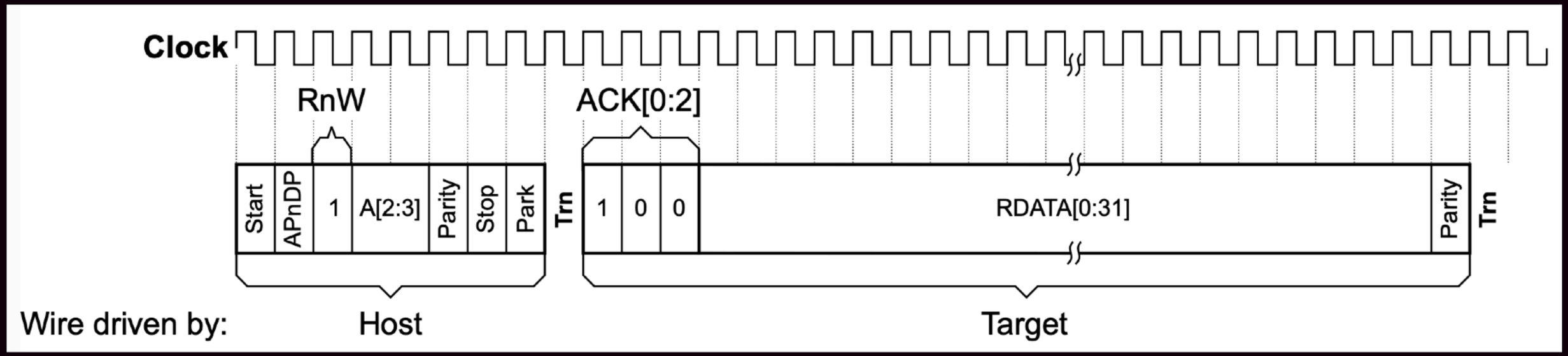


0b1010	0b11111010	DPACC	35	See *DPACC and APACC, JTAG-DP DP, and AP Access registers* on page B3-98.
0b1011	0b11111011	APACC	35	

From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2

SWD Protocol: Read

Why DPACC and APACC are 35 bits



From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2