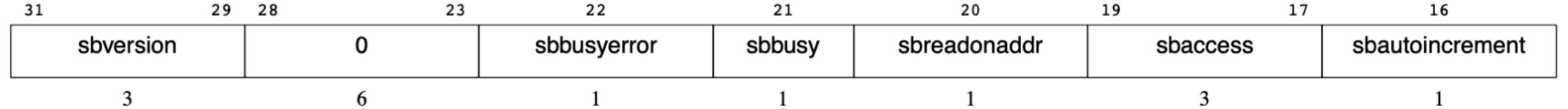
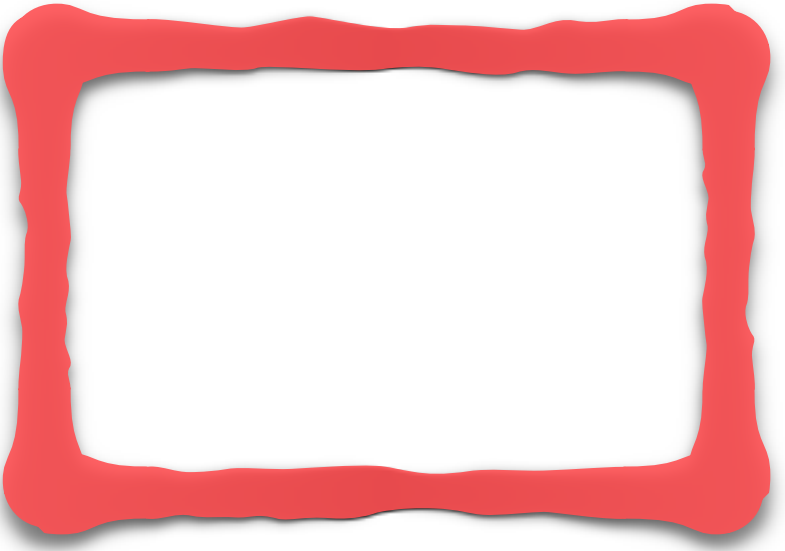
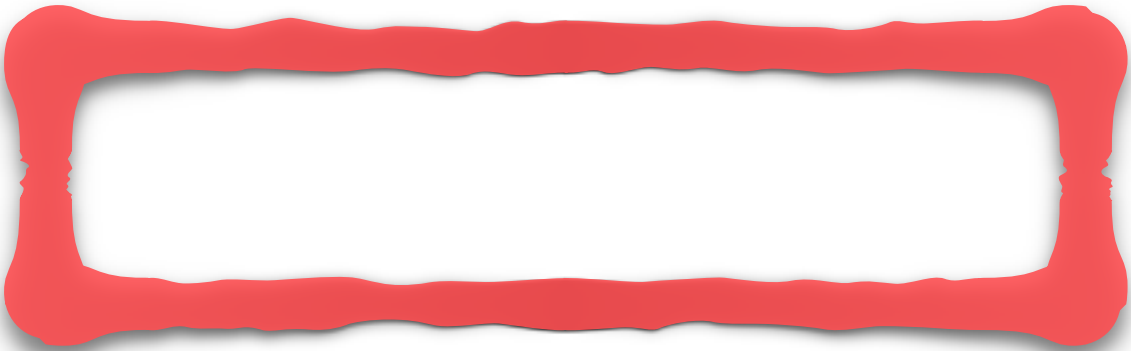
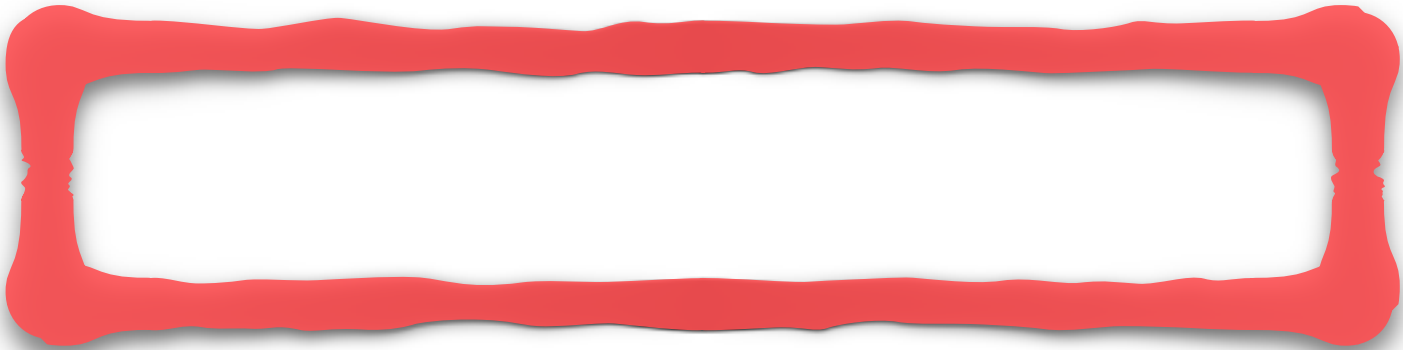

31
29
28
23
22
21
20
19
17
16
sbversion
0
sbbusyerror
sbbusy
sbreadonaddr
sbaccess
sbautoincrement
3
6
1
1
1
3
1
15
14
12
11
5
4
3
2
1
0
sbreadondata
sberror
sbasize
sbaccess128
sbaccess64
sbaccess32
sbaccess16
sbaccess8
1
3
7
1
1
1
1
1

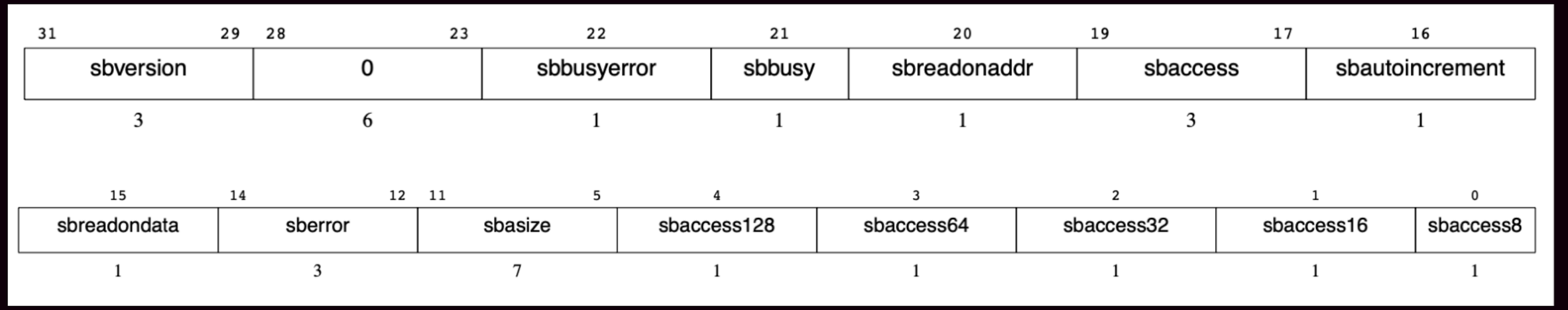






System Bus Access: Control and Status

`sbcs`: 0x38 / `sbaddress0`: 0x39 / `sbdata0`: 0x3c



- **`sbaddress0`**: Address to use for memory operations
- sbreadonaddr: Perform a read when **`sbaddress0`** is written
- **`sbdata0`**: Write to this register to write data at **`sbaddress0`**
- Works when core is not halted!

What Do We Need for a Debugger?

RISC-V Debug Specification

Memory	Registers	Control
? Peek	✓ Read	✓ Halt
? Poke	✓ Write	? Step
		✓ Reset
		? Break