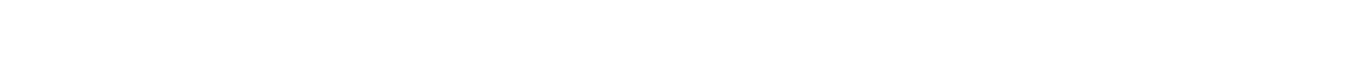
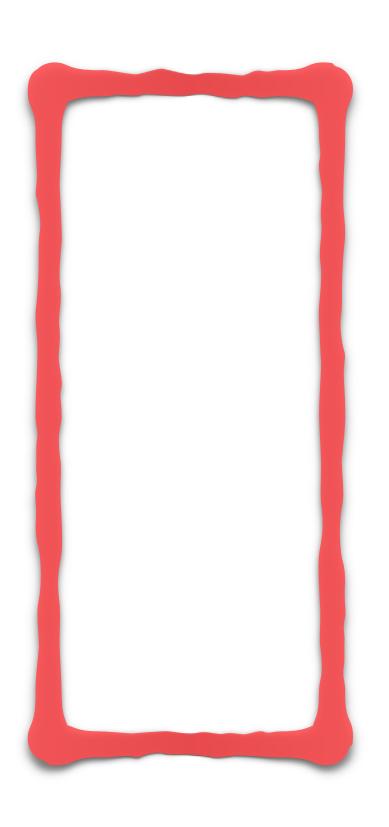
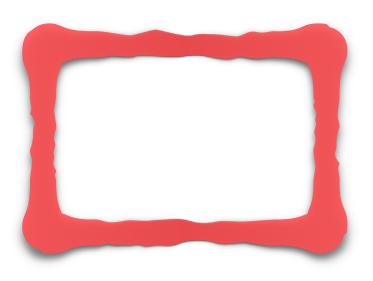


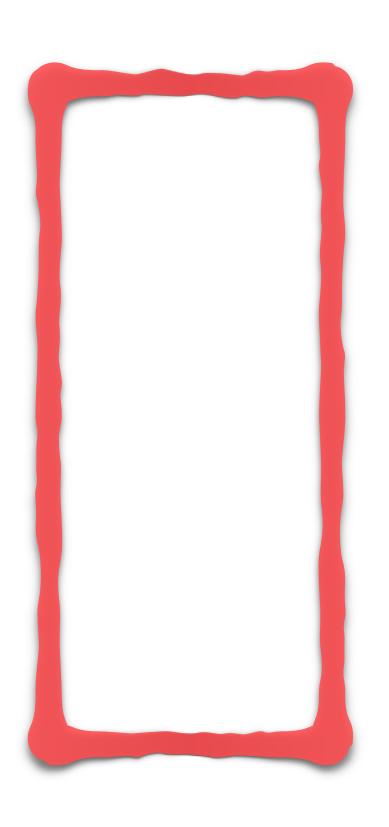
31			27	26	25	24
				enableEbreak	clearHalt	clearReset
23			19	18	17	16
				disableEbreak	setHalt	setReset
15						8
7	5	4	3	2	1	0
		step	ebreakHit	busy	halted	inReset

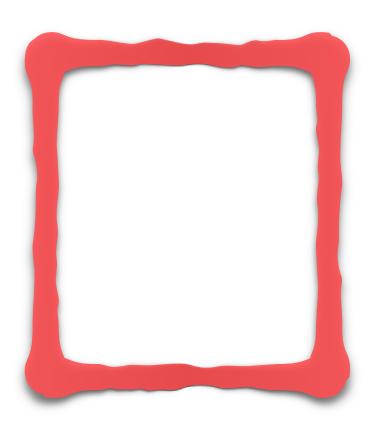


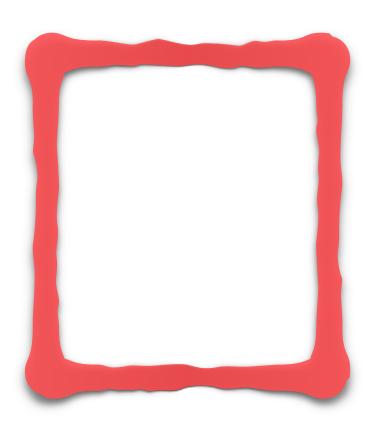








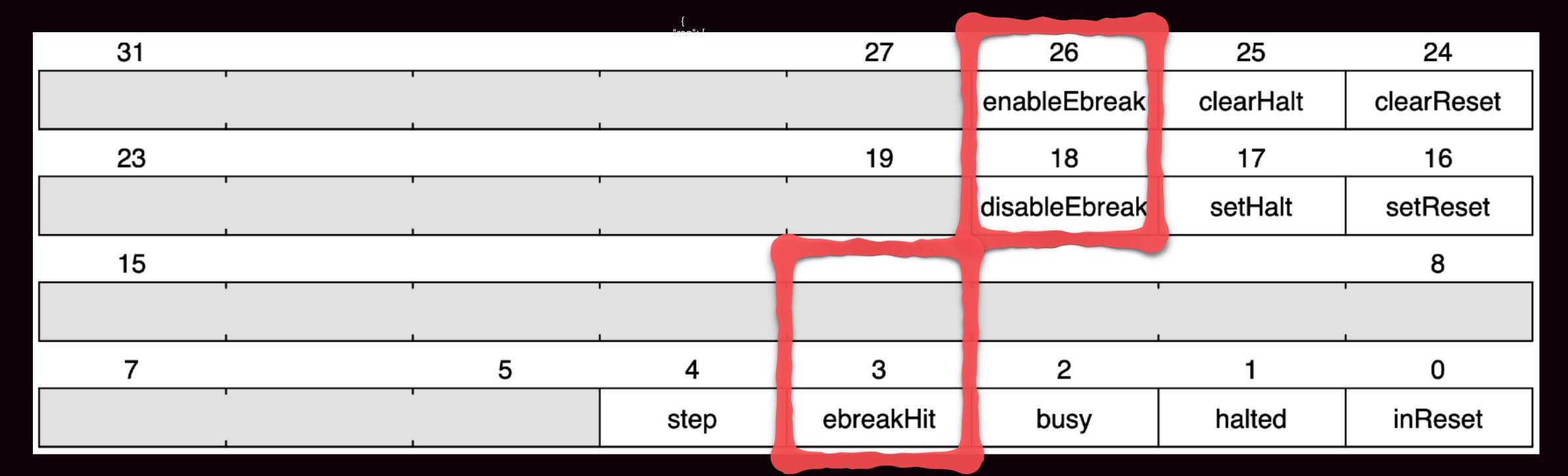




VexRiscv Debug Interface

DebugPlugin.scala

0x00: CPU control



Fomu Reference Manual — https://rm.fomu.im/

What Do We Need for a Debugger?

VexRiscv

Memory

- ? Peek
- ? Poke

Registers

- ? Read
- ? Write

Control

- ? Halt
- ? Step
- ? Reset
- ? Break