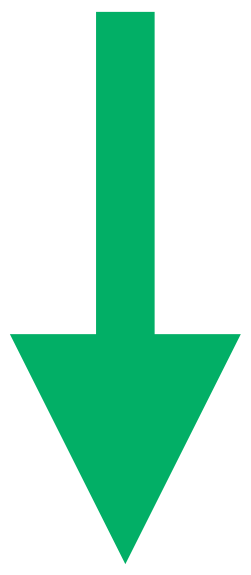
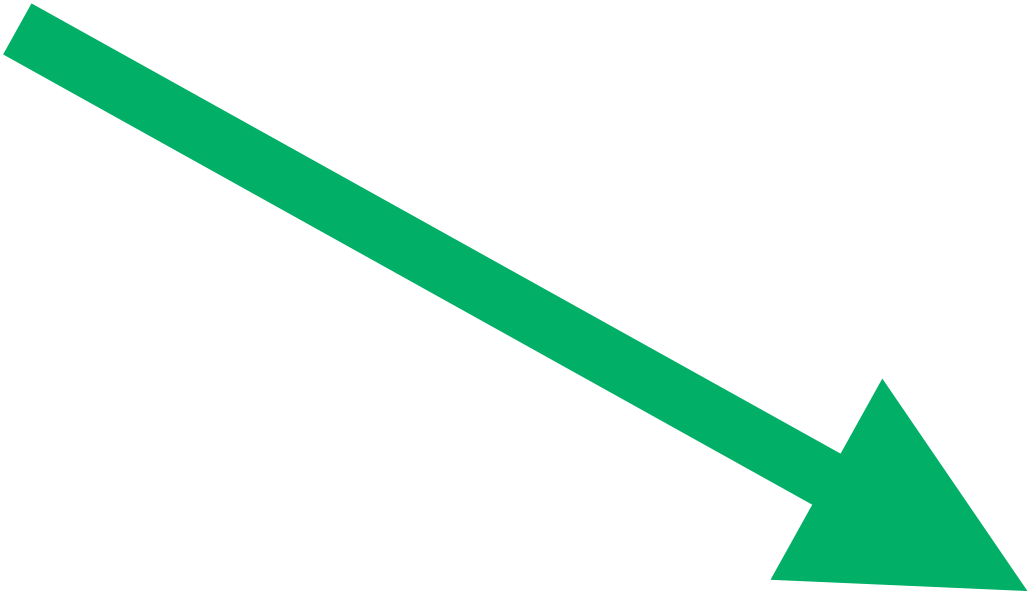
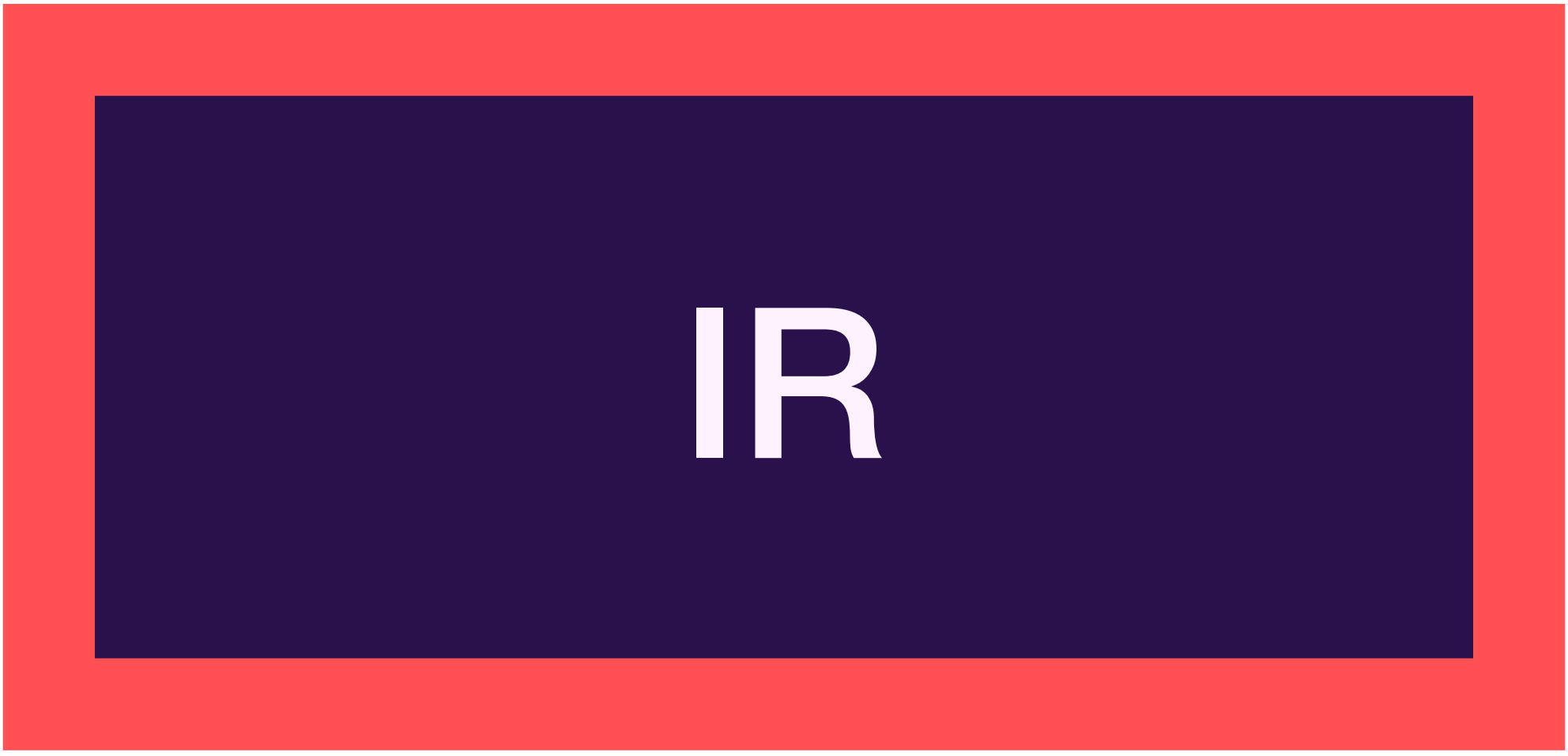





DR


IR


DPACC

APACC


DRW


TAR


DPBANKSEL

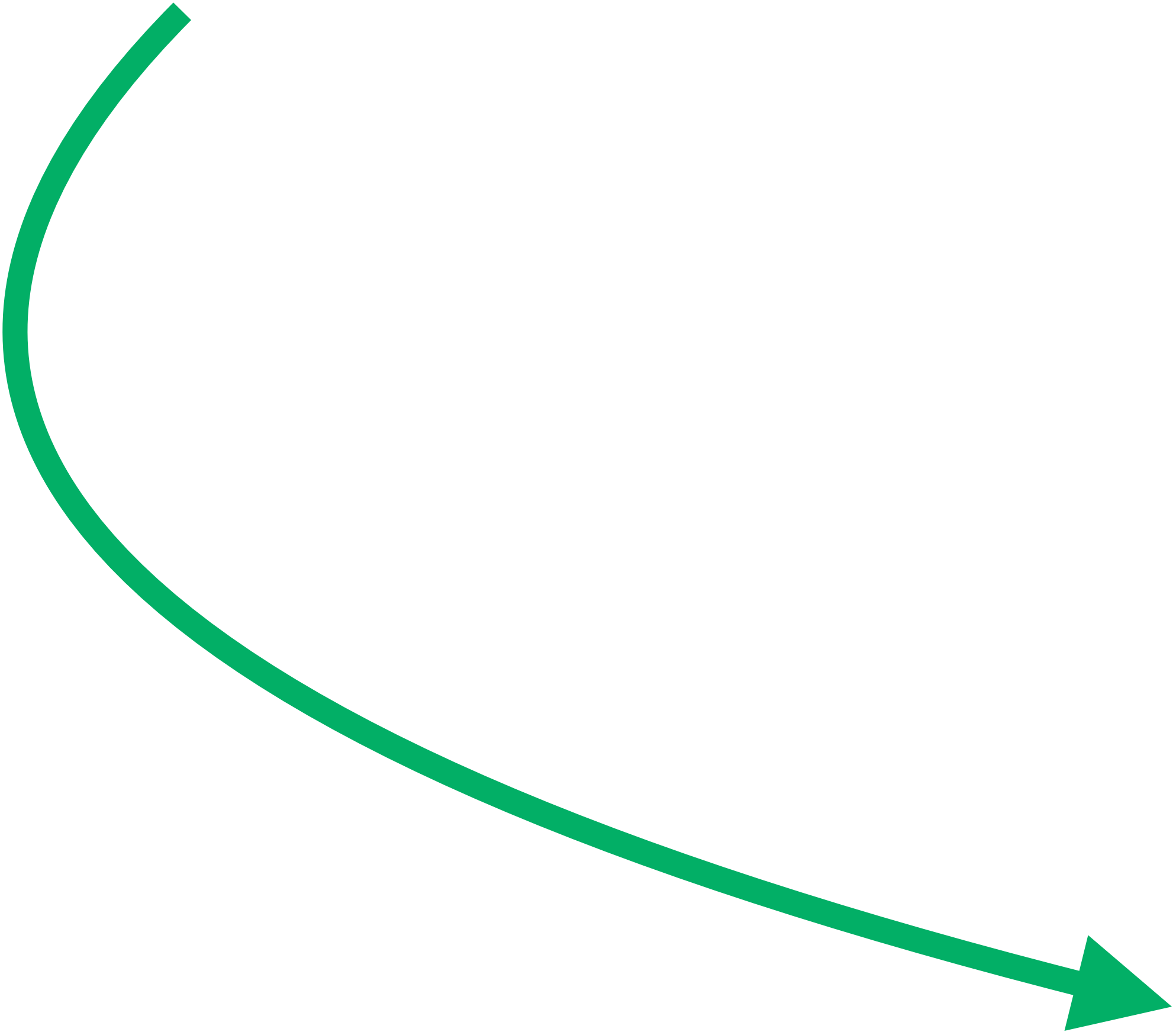

APBANKSEL

JTAG

ADIv5

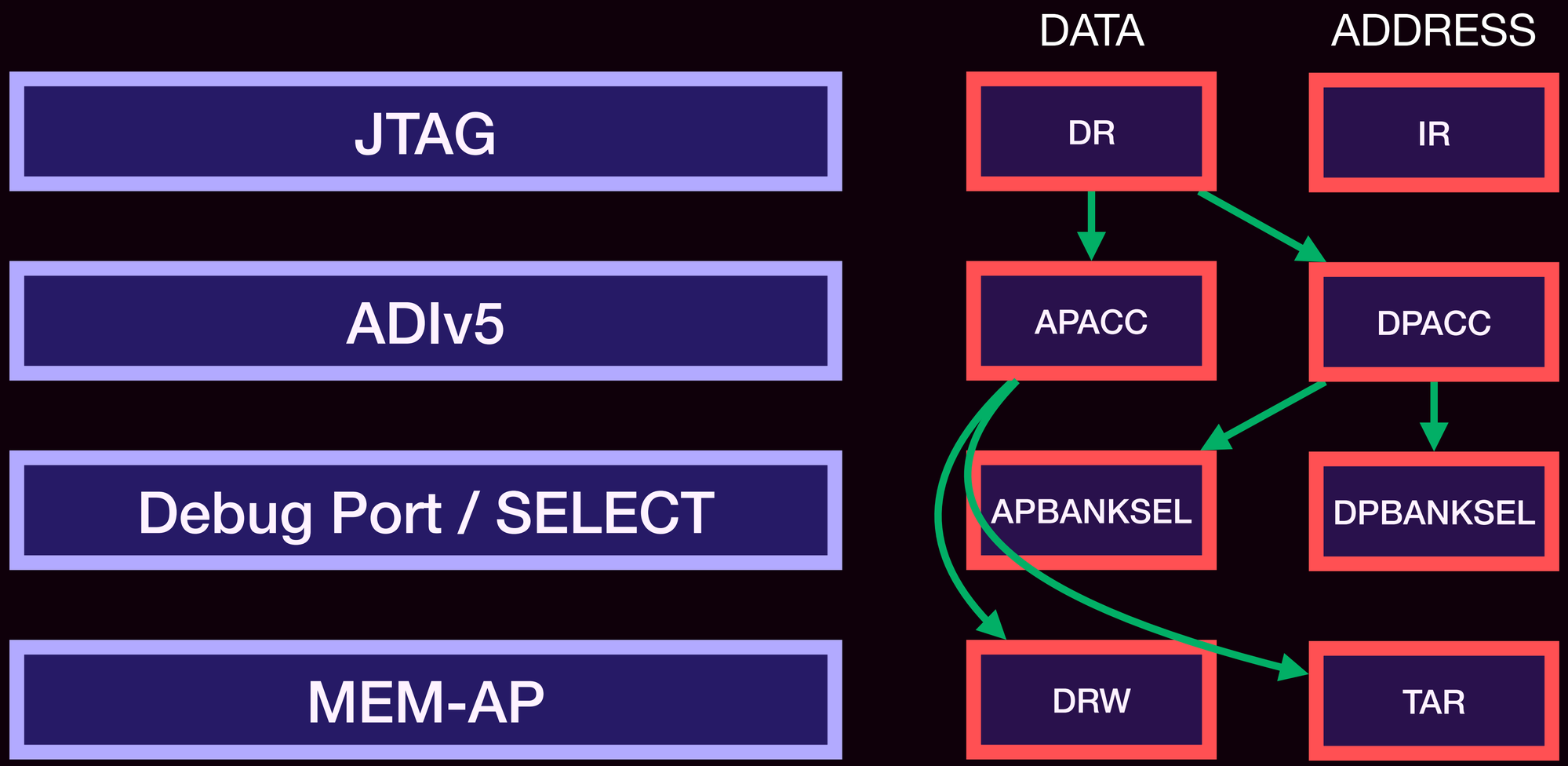
Debug Port / SELECT

MEM-AP



Putting It All Together

Accessing RAM from JTAG



What about SWD?