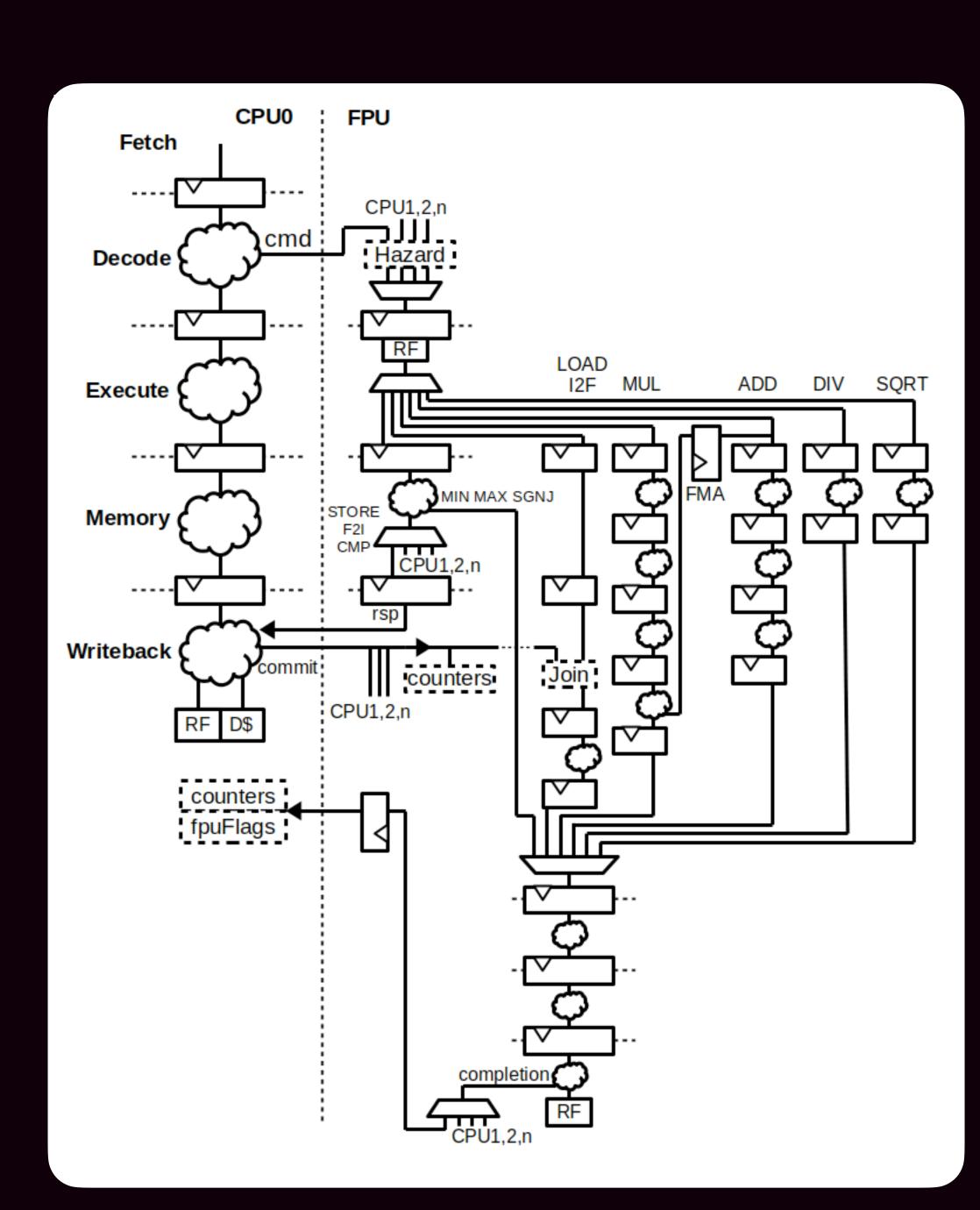
## VexRiscv: A CPU in Scala FPGA-targeted soft core

- 32-bit RISC-V core
- Plugin support
- FPUPlugin.scala
- DebugPlugin.scala
  - Only two registers!



From: VexRiscv README.md

## VexRiscv Debug Interface

## DebugPlugin.scala

0x00: CPU control

		\ "******				
31			27	26	25	24
				enableEbreak	clearHalt	clearReset
23			19	18	17	16
				disableEbreak	setHalt	setReset
15						8
7	5	4	3	2	1	0
		step	ebreakHit	busy	halted	inReset