RISC-V Control and Status Registers

dcsr: 0x7b0

Offset	Name	Info
0x300	MSTATUS	Machine status register
0x301	MISA	Summary of ISA extension support
0x302	MEDELEG	Machine exception delegation register. Not implemented, as no S-mode support.
0x303	MIDELEG	Machine interrupt delegation register. Not implemented, as no S-mode support.
0x304	MIE	Machine interrupt enable register
0x305	MTVEC	Machine trap handler base address.
0x306	MCOUNTEREN	Counter enable. Control access to counters from U-mode. Not to be confused with mcountinhibit.
0x30a	MENVCFG	Machine environment configuration register, low half
0x310	MSTATUSH	High half of mstatus, hardwired to 0.
0x31a	MENVCFGH	Machine environment configuration register, high half
0x320	MCOUNTINHIBIT	Count inhibit register for `mcycle`/`minstret`
0x323	MHPMEVENT3	Extended performance event selector, hardwired to 0.

From: RP2350 Reference Manual

Accessing CSRs

Control and Status Registers from RISC-V

Numbers	Group Description
0x0000 — 0x0fff	CSRs. The `PC" can be accessed here through dpc.
0x1000 — 0x101f	GPRs
0x1020 — 0x103f	Floating point registers
0xc000 — 0xffff	Reserved for non-standard extensions and internal use.

Abstract Access Register

`command: 0x17`