CSW

# TAR


TAR_HI


DRW

BD0

# BD1

BD2

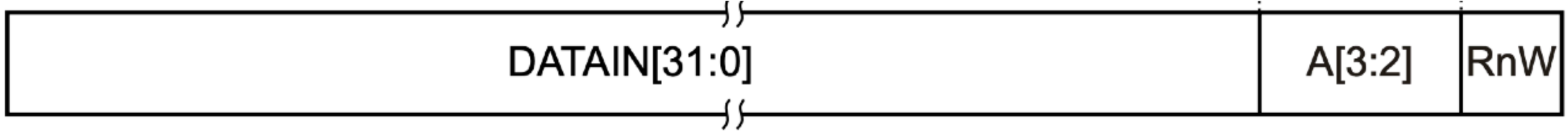
BD3

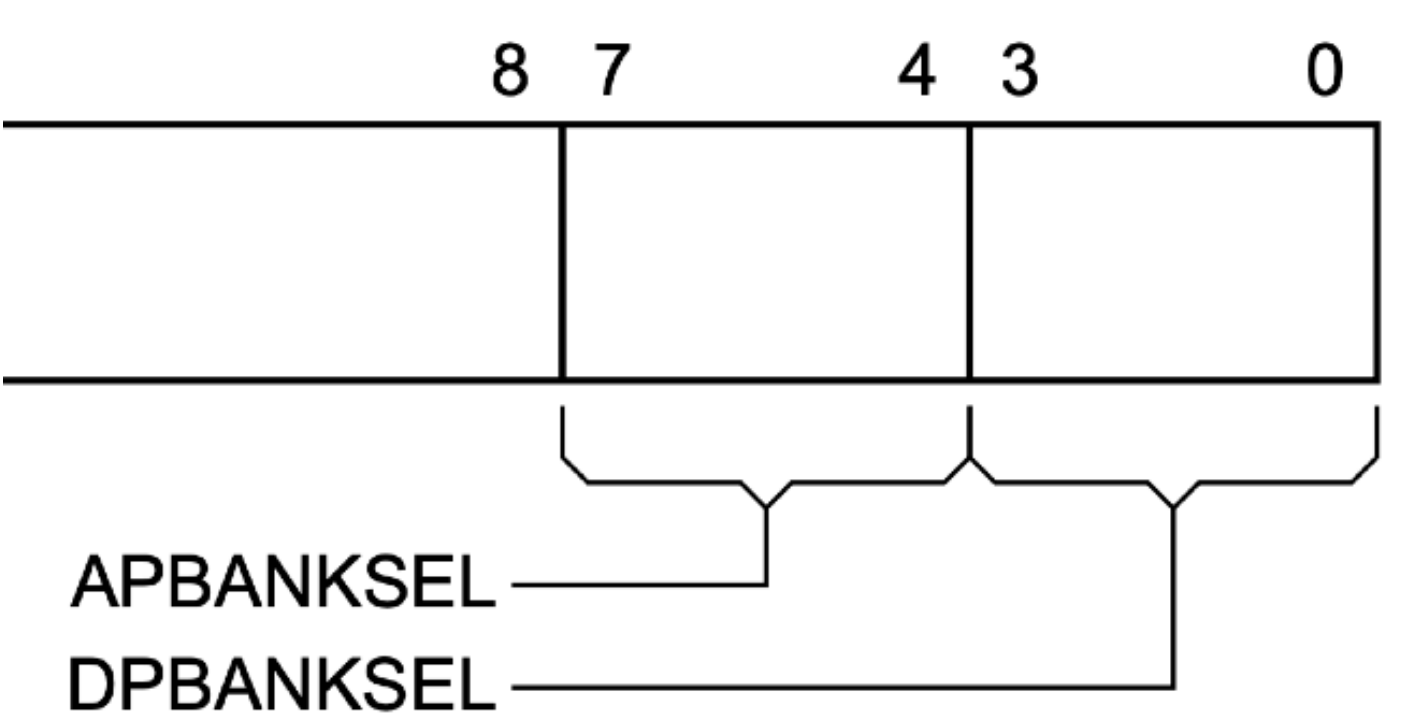

BASE_HI

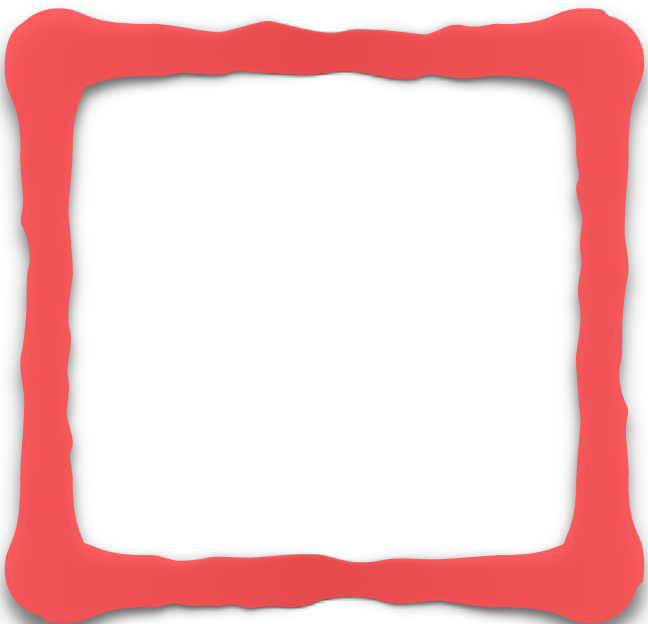
# CFG

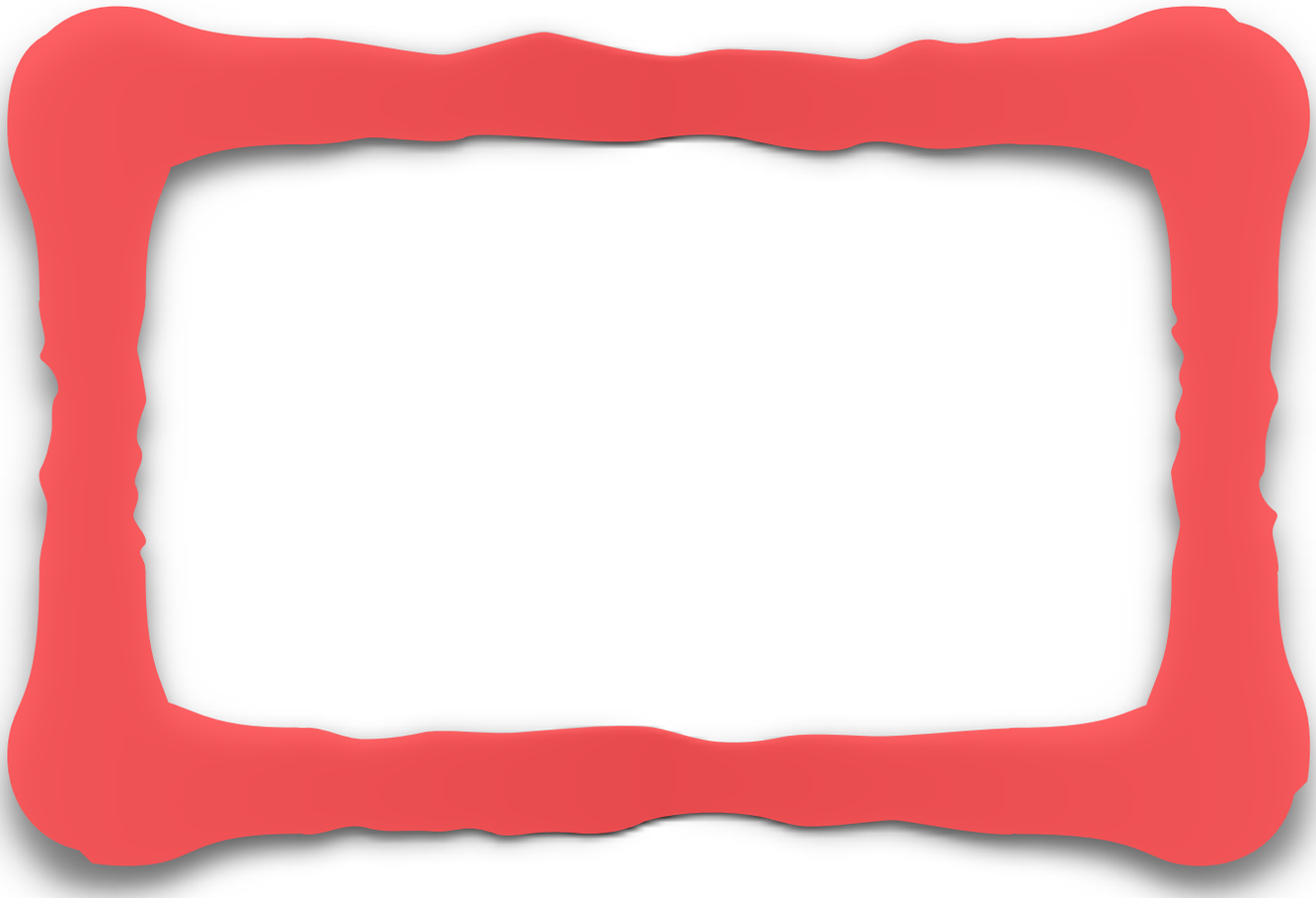

BASE

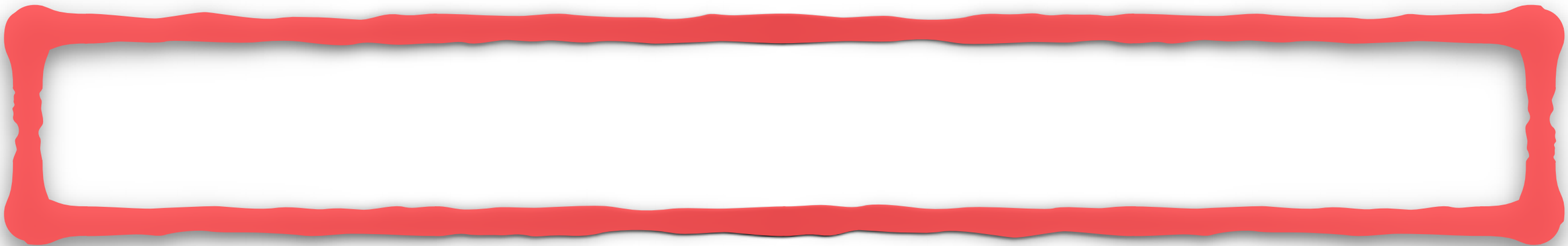
IDR


DATAIN[31:0]
A[3:2]
RnW

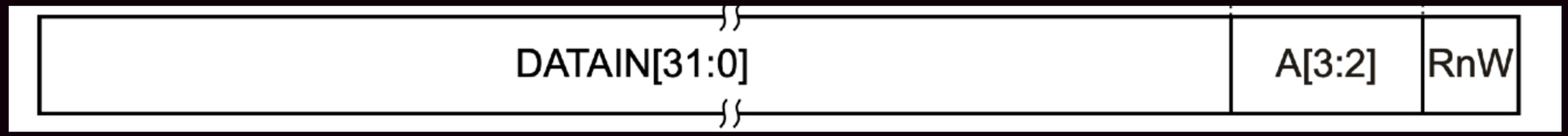

8
7
4
3
0
APBANKSEL
DPBANKSEL



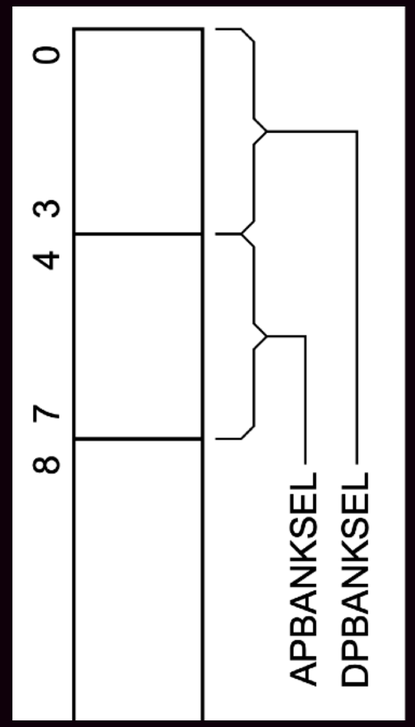


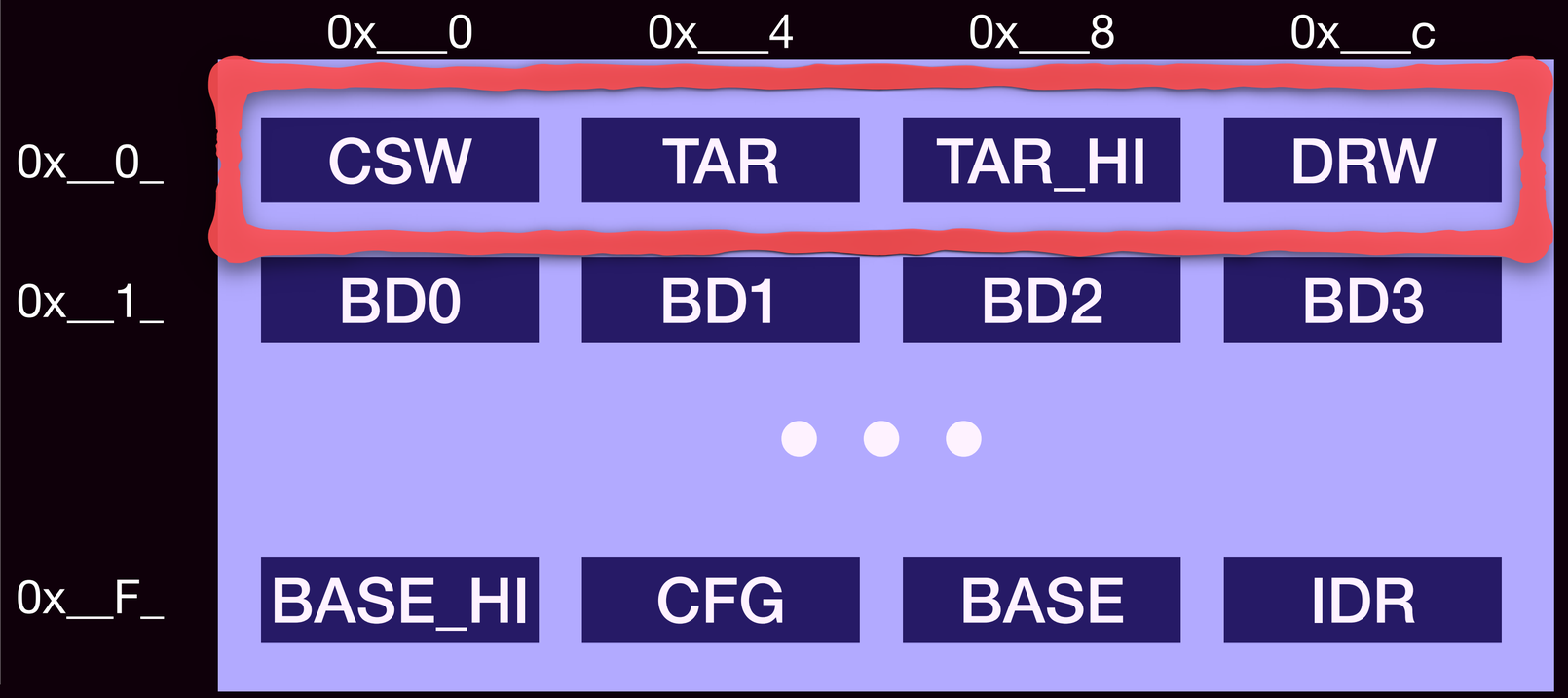


# ADIv5 MEM-AP




SELECT




From: Arm Debug Interface Architecture Specification ADIv5.0 to ADIv5.2

# Steps for Accessing RAM

1. Write target address to TAR
2. Read or write DRW