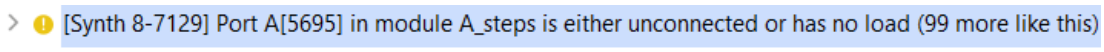
Warning: [Synth 8-7129]



Number of warnings: 100

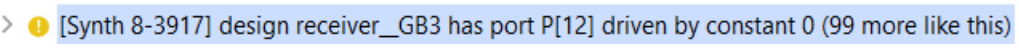
explanation:

The warning indicates that the synthesis tool has detected that some signals in the design may have been optimized, but they are not removed. This warning is usually generated when there are signals in the design that are not used or have no effect on the functionality of the design.

In our design:

The reason for the warning is that the compression function is built so that it does not use all the information, the information used depends on the constants $t_1 - t_4$. And because these constants in the algorithm do not have to be in the values, we gave them and are subject to change, then the information that is not used in the current design is consumed.

Warning: [Synth 8-3917]



Number of warnings: 100

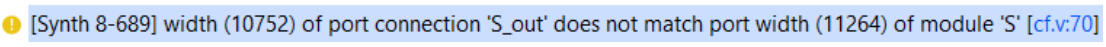
explanation:

The warning indicates that the synthesis tool has detected a condition that may cause contention or undefined behavior during the design operation. This warning is usually generated when there is a potential conflict between two or more signals in the design.

In our design:

The reason for the warning is that a value of 0 was entered for the signals at the beginning of the design, and there are no conflicts with other signals. Of course, the reset of the signals is consumed to use the design repeatedly.

Warning: [Synth 8-689]



Number of warnings: 1

explanation:

The warning indicates that the synthesis tool has detected that there is a mismatch between the width of a signal or port connection in the design and the width of the corresponding port in a module instance.

In our design:

The reason for the warning is that the last 512 bits received from the rom are not transferred to vector S. We do not transfer them because they are not part of the constants, and every bit there is equal to 0, by that, all the rom vectors would be the same size.

Warning: [Synth 8-6014]

[Synth 8-6014] Unused sequential element index_reg was removed. [tx.v:58] (2 more like this)

Number of warnings: 3

explanation:

The warning indicates that the synthesis tool has detected a continuous element in your design that is not in use and has been removed.

In our design:

The elements in question are necessary to initialize the program for reuse in all types of situations in the code.

Warning: [Synth 8-327]

[Synth 8-327] inferring latch for variable 'D_reg' [MD6_Mode.v:32]

Number of warnings: 1

explanation:

The warning indicates that the synthesis tool has inferred a latch for the variable named 'D_reg' in your design.

In our design:

the 'case(d)' statement implies that the behavior inside the case statement depends on the value of the signal 'd'. However, if 'd' does not have a defined value for some conditions, the synthesis tool may infer latches to retain the previous value until a condition is met where 'd' has a defined value.

Warning: [Route 35-447]

[Route 35-447] Congestion is preventing the router from routing all nets. The router will prioritize the successful completion of routing all nets over timing optimizations

Number of warnings: 1

explanation:

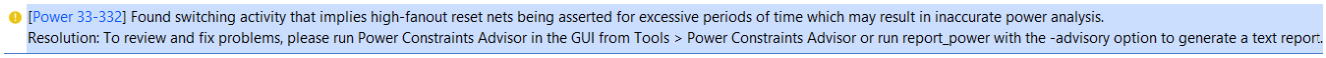
When a router encounters congestion, it means that there is too much traffic trying to pass through it, and the router is struggling to keep up with the demand. In this case, the congestion is preventing the router from successfully routing all nets, which refers to the individual connections between different components on a printed circuit board (PCB).

To address this issue, the router will prioritize the successful completion of routing all nets over timing optimizations. This means that the router will focus on completing the routing process for all the nets before attempting to optimize the timing of the connections. This approach can be helpful because it ensures that all connections are made, even if it takes longer than usual, and that the PCB will function as intended.

In our design:

we have made significant efforts to reduce the utilization of the routing capacity and alleviate congestion. However, despite these optimizations, we have reached a point where further reducing the load on the routing resources is challenging. The remaining option to mitigate congestion would involve utilizing an FPGA with a larger capacity, which unfortunately is not feasible within the scope of our current project.

Warning: [Power 33-332]



Number of warnings: 1

explanation:

The message indicates that there is a problem with the power analysis of the design. The message is warning that found switching activity that implies high-fanout reset nets being asserted for excessive periods of time which may result in inaccurate power analysis" is generated by the power analysis tool in Vivado. It indicates that there are certain reset signals in your design with high fanout (i.e., connected to a large number of elements) that remain asserted for extended durations.

In our design:

we receive a data stream of 4096 bits through the UART interface. These incoming bits are then categorized and directed to various sections within our design. To ensure proper functionality and facilitate the reusability of the design, we have incorporated a relatively higher number of reset signals. These reset signals are primarily used to initialize the relevant components during system startup or when a reset operation is required.

Although these reset signals are not utilized once all the information has been processed, they play a crucial role in ensuring correct initialization and reinitialization of the design when necessary. Consequently, these reset signals are connected to the RESET input of the respective components.