Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC **4950**)

REPORT

Objective: Design and simulate a 4-bit Ripple Adder using ModelSim.

Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:

C:/Modeltech_pe_edu_10.4a/examples/4bit-rippleadder.vhd (/ripple4/FA1)

File Edit View Tools Bookmarks Window Help

C:/Modeltech_pe_edu_10.4a/examples/4bit-rippleadder.vhd (/ripple4/FA1) - Default

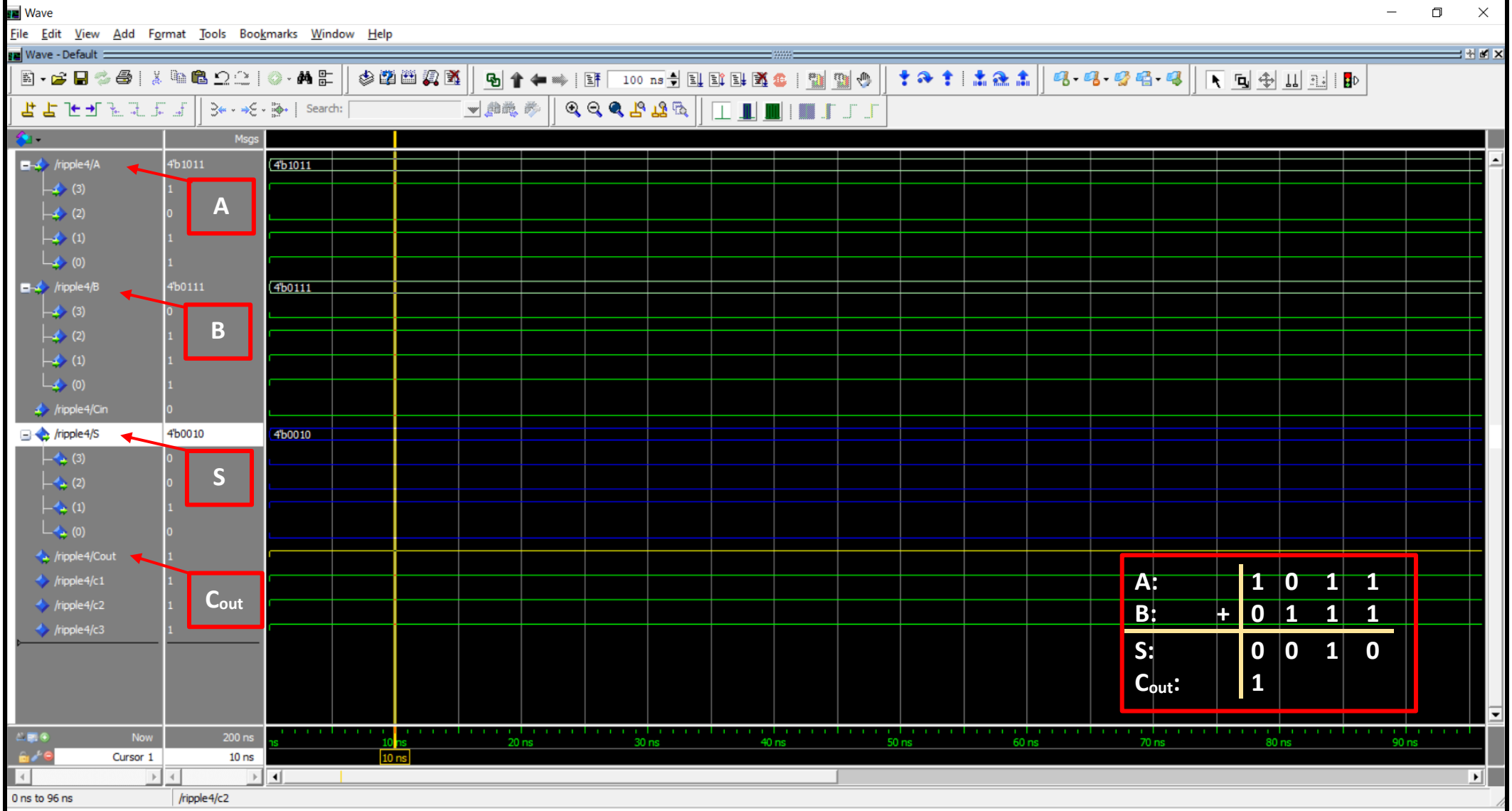
Ln# 4 Drivers (same line)

```
1  --Name: Ravi Sahni
2  --Faclty No.: 17 COB 085
3  --Enrol. No.: GJ 7718
4
5  library IEEE;
6  use IEEE.STD_LOGIC_1164.all;
7
8  entity ripple4 is
9  Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
10 B : in STD_LOGIC_VECTOR (3 downto 0);
11 Cin : in STD_LOGIC;
12 S : out STD_LOGIC_VECTOR (3 downto 0);
13 Cout : out STD_LOGIC);
14 end ripple4;
15
16 architecture Basic of ripple4 is
17 component FA
18 Port ( A : in STD_LOGIC;
19 B : in STD_LOGIC;
20 Cin : in STD_LOGIC;
21 S : out STD_LOGIC;
22 Cout : out STD_LOGIC);
23 end component;
```

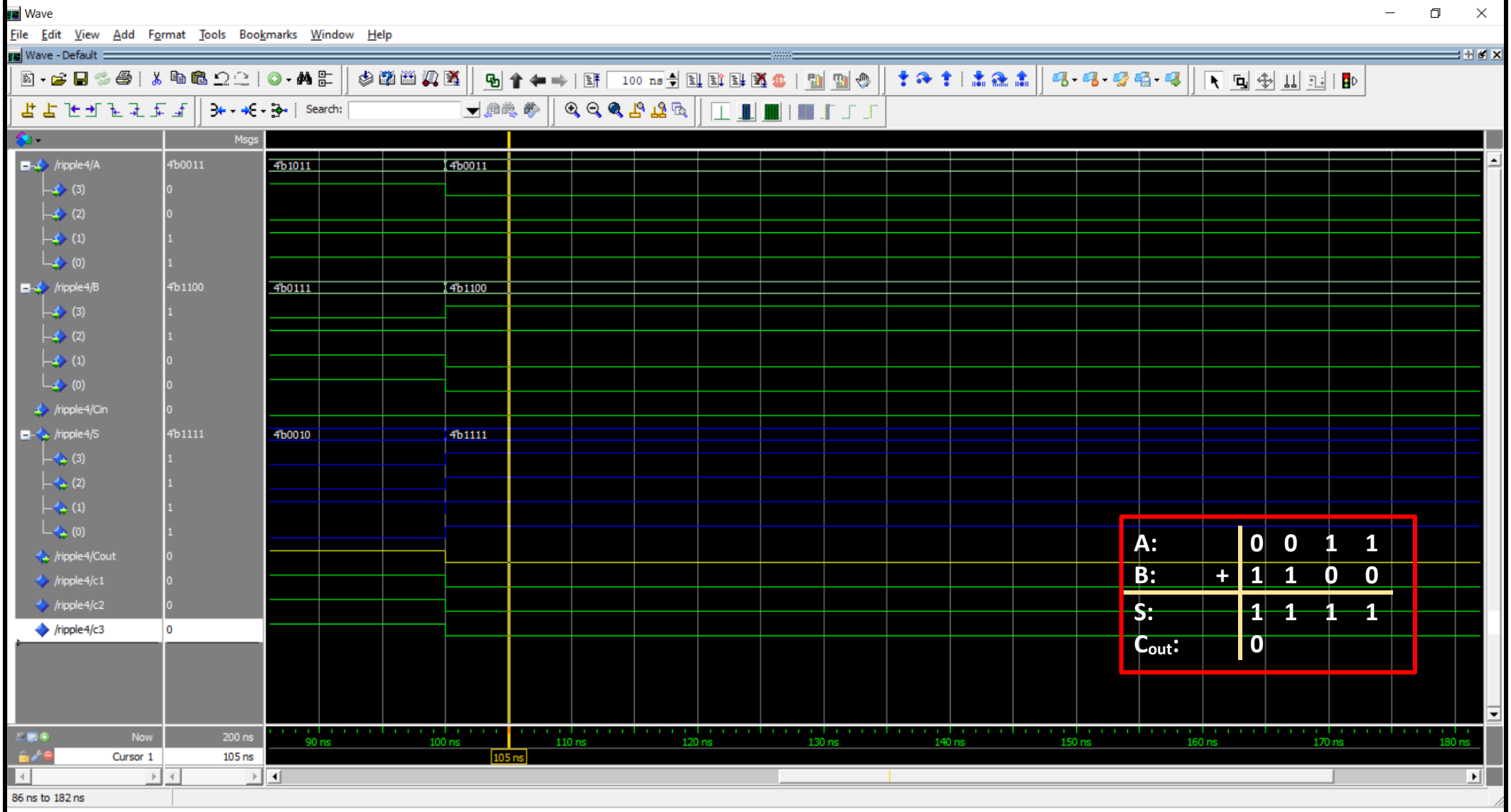
VHDL Code: *(contd.)*

```
24
25  signal c1,c2,c3: STD_LOGIC;
26
27  begin
28  FA1: FA port map( A(0), B(0), Cin, S(0), c1);
29  FA2: FA port map( A(1), B(1), c1, S(1), c2);
30  FA3: FA port map( A(2), B(2), c2, S(2), c3);
31  FA4: FA port map( A(3), B(3), c3, S(3), Cout);
32
33  end Basic;
34
35  --writing entity & architecture for FA component
36  library IEEE;
37  use IEEE.STD_LOGIC_1164.all;
38
39  entity FA is
40  Port ( A : in STD_LOGIC;
41  B : in STD_LOGIC;
42  Cin : in STD_LOGIC;
43  S : out STD_LOGIC;
44  Cout : out STD_LOGIC);
45  end FA;
46
47  architecture Basic of FA is
48  begin
49  S <= A XOR B XOR Cin;
50  Cout <= (A AND B) OR (Cin AND (A OR B));
51  end Basic;
52
```

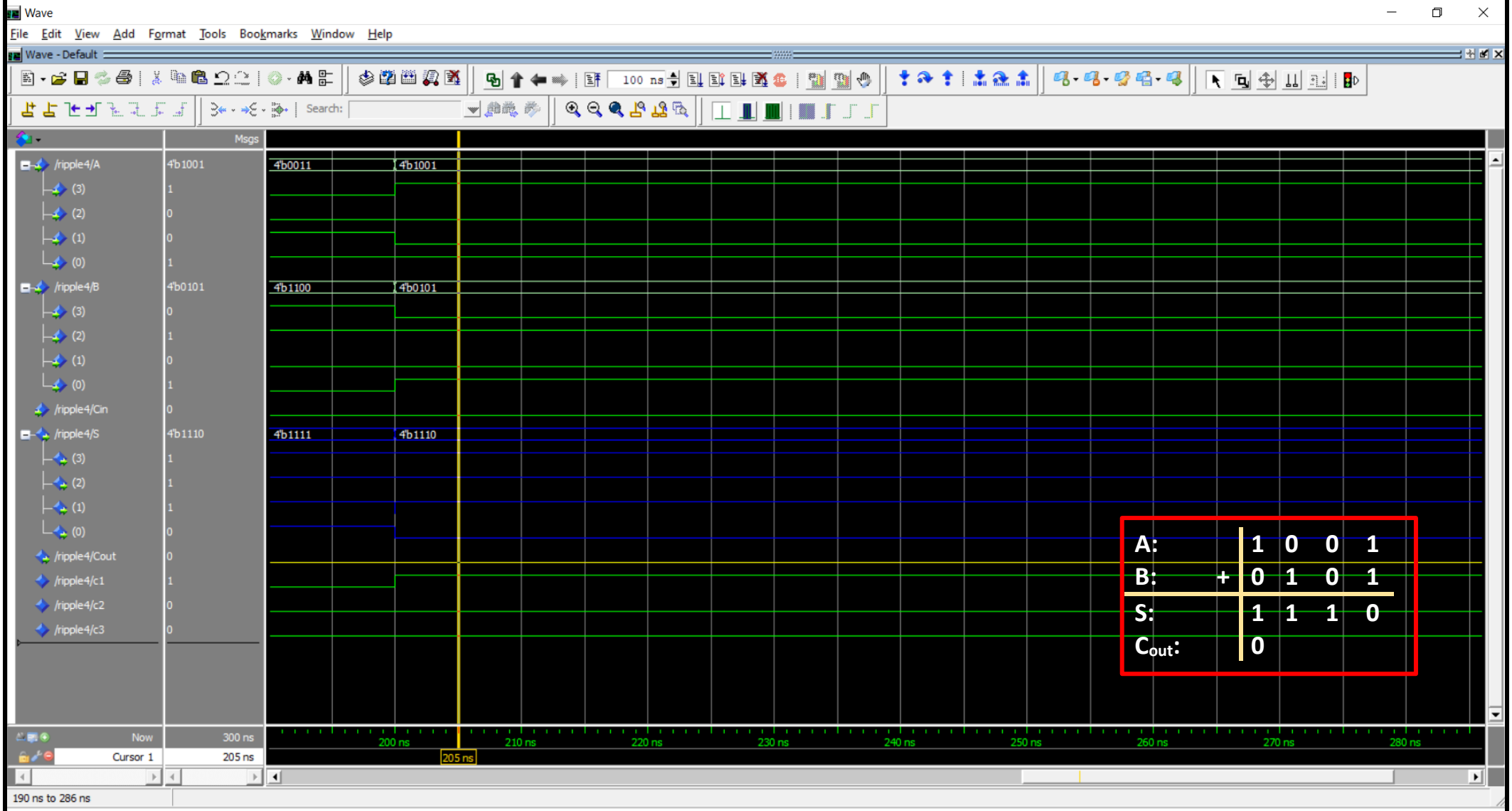
Waveform #1:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/ripple4/A
4'b1011
(3)
(2)
(1)
(0)
/ripple4/B
4'b0111
/ripple4/Cin
/ripple4/S
4'b0010
/ripple4/Cout
/ripple4/c1
/ripple4/c2
/ripple4/c3
A
B
S
Cout
Now
200 ns
Cursor 1
10 ns
0 ns to 96 ns
/ripple4/c2
A: 1 0 1 1
B: + 0 1 1 1
S: 0 0 1 0
Cout: 1

Waveform #2:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/ripple4/A
(3)
(2)
(1)
(0)
/ripple4/B
(3)
(2)
(1)
(0)
/ripple4/Cin
/ripple4/S
(3)
(2)
(1)
(0)
/ripple4/Cout
/ripple4/c1
/ripple4/c2
/ripple4/c3
4'b0011
4'b1100
4'b1111
4'b1011
4'b0011
4'b0111
4'b1100
4'b0010
4'b1111
Now
200 ns
Cursor 1
105 ns
90 ns
100 ns
110 ns
120 ns
130 ns
140 ns
150 ns
160 ns
170 ns
180 ns
105 ns
86 ns to 182 ns
A: 0 0 1 1
B: + 1 1 0 0
S: 1 1 1 1
Cout: 0

Waveform #3:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/ripple4/A
4'b1001
(3)
1
(2)
0
(1)
0
(0)
1
/ripple4/B
4'b0101
(3)
0
(2)
1
(1)
0
(0)
1
/ripple4/Cin
0
/ripple4/S
4'b1110
(3)
1
(2)
1
(1)
1
(0)
0
/ripple4/Cout
0
/ripple4/c1
1
/ripple4/c2
0
/ripple4/c3
0
4'b0011
4'b1001
4'b1100
4'b0101
4'b1111
4'b1110
A: 1 0 0 1
B: + 0 1 0 1
S: 1 1 1 0
Cout: 0
Now
300 ns
Cursor 1
205 ns
200 ns
210 ns
220 ns
230 ns
240 ns
250 ns
260 ns
270 ns
280 ns
205 ns
190 ns to 286 ns