Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC **4950**)

REPORT

Objective: Design and simulate a 4 to 1 multiplexer using ModelSim.

Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:

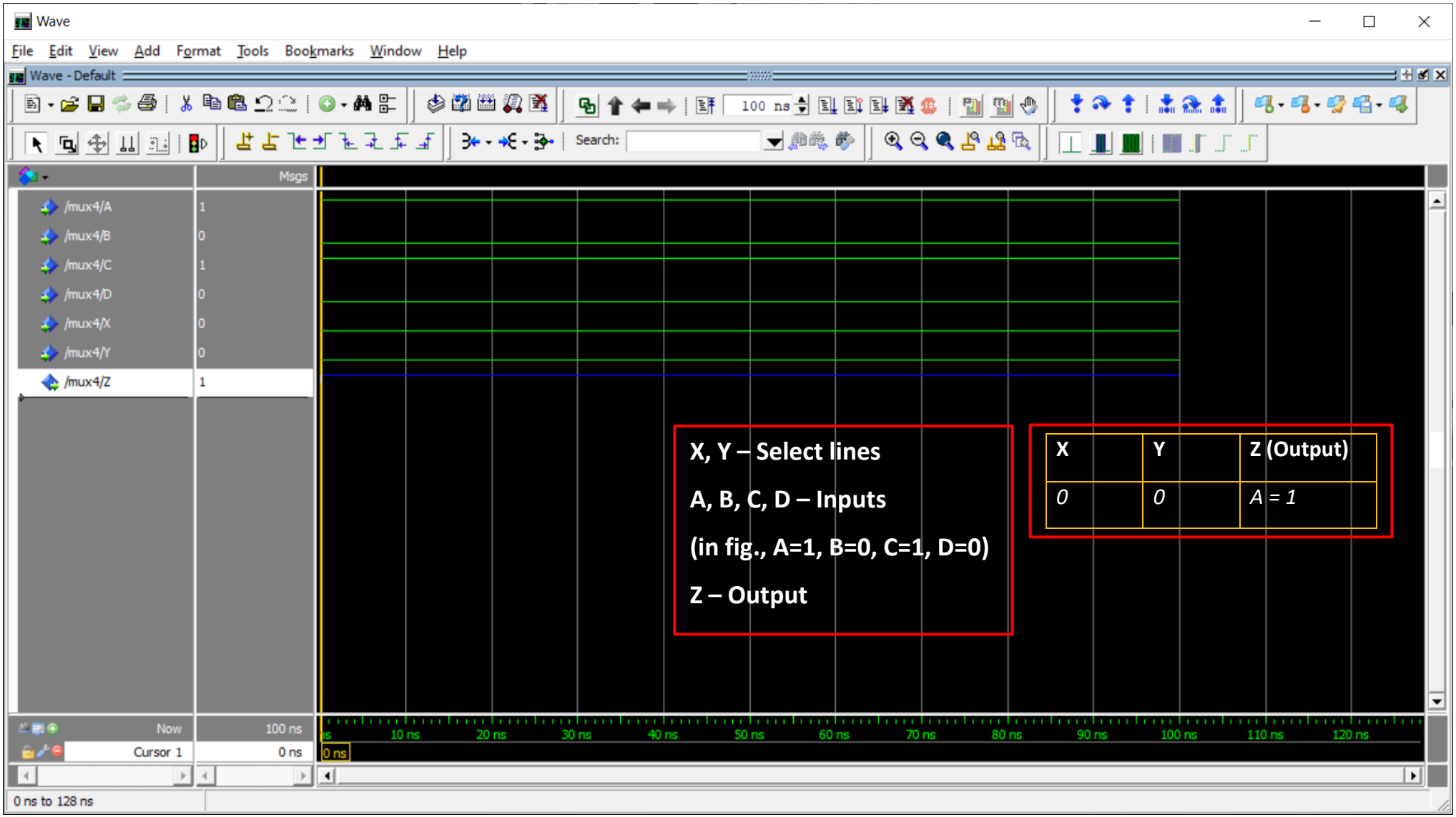
C:/Modeltech_pe_edu_10.4a/examples/4x1mux.vhd (/mux4)

File Edit View Tools Bookmarks Window Help

C:/Modeltech_pe_edu_10.4a/examples/4x1mux.vhd (/mux4) - Default *

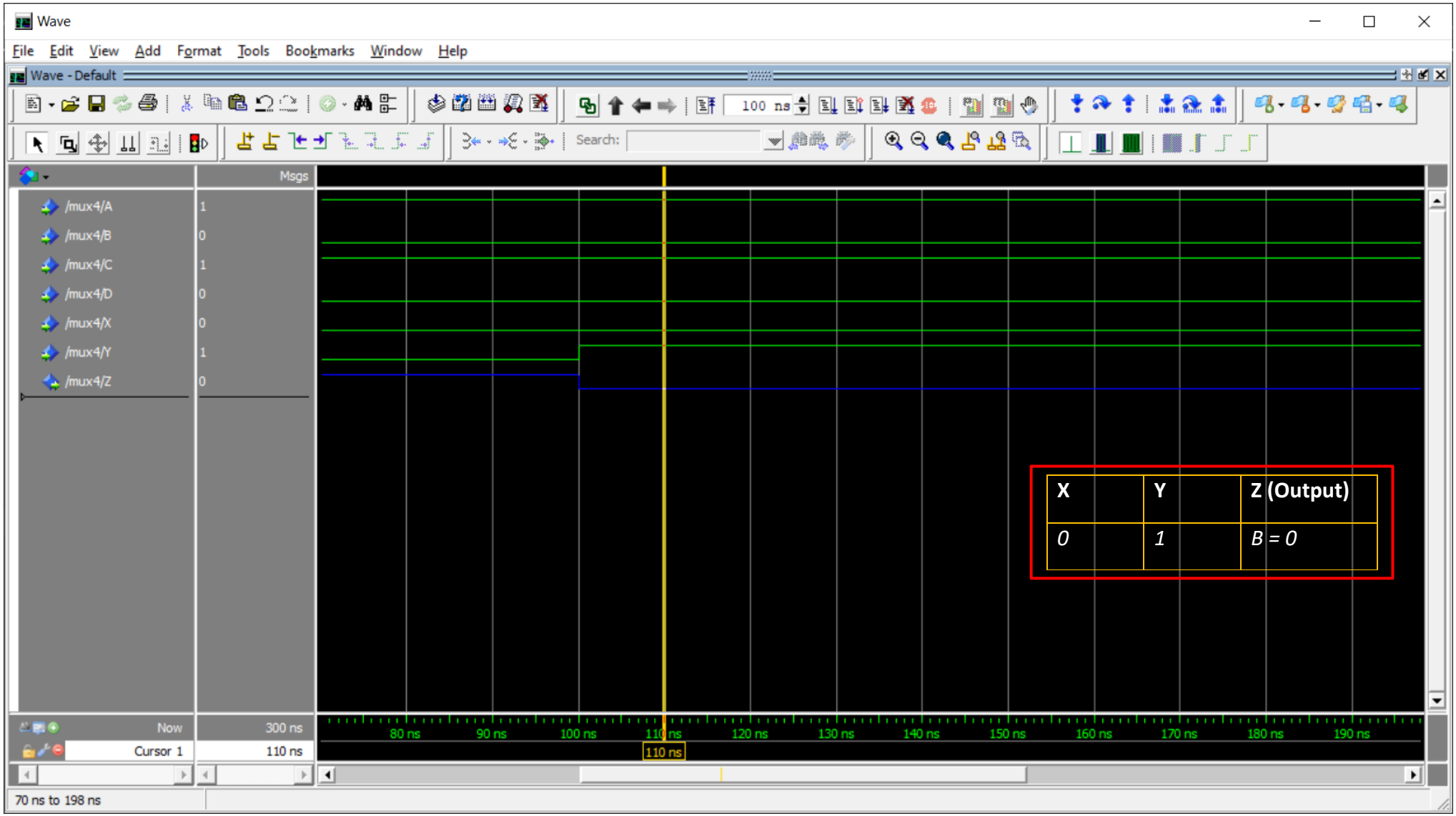
```
Ln#
 1  --Name: Ravi Sahni
 2  --Faclty No.: 17 COB 085
 3  --Enrol. No.: GJ 7718
 4
 5  library IEEE;
 6  use IEEE.STD_LOGIC_1164.all;
 7
 8  entity mux4 is
 9  port(
10          A,B,C,D: in STD_LOGIC;
11          X,Y: in STD_LOGIC;
12          Z: out STD_LOGIC
13  );
14  end mux4;
15
16  architecture Basic of mux4 is
17  begin
18          Z <= (NOT X AND NOT Y AND A) OR (NOT X AND Y AND B) OR (X AND NOT Y AND C) OR (X AND Y AND D);
19  end architecture basic;
20
```

Waveform #1:



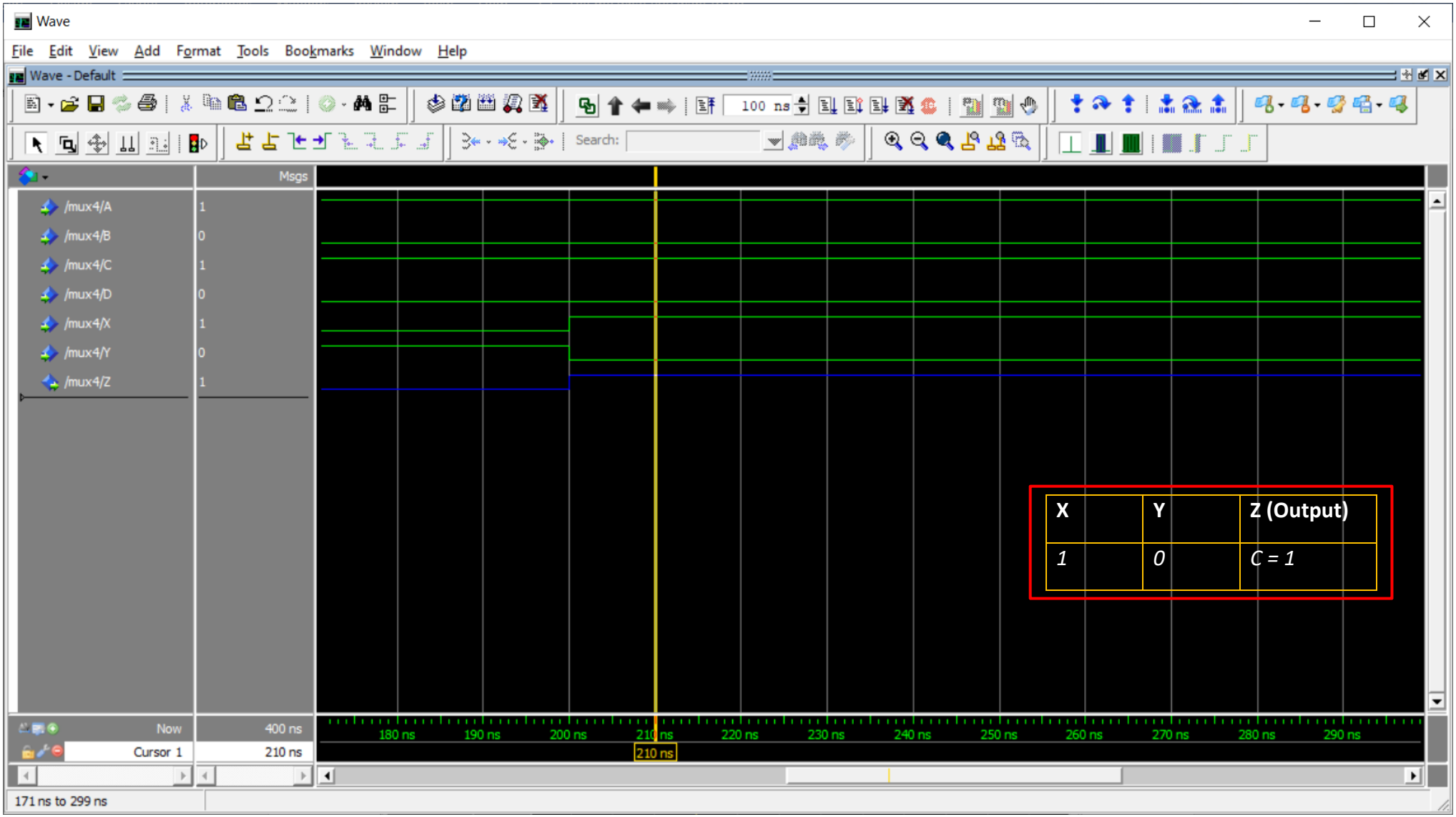
X	Y	Z (Output)
0	*0*	*A = 1*

Waveform #2:



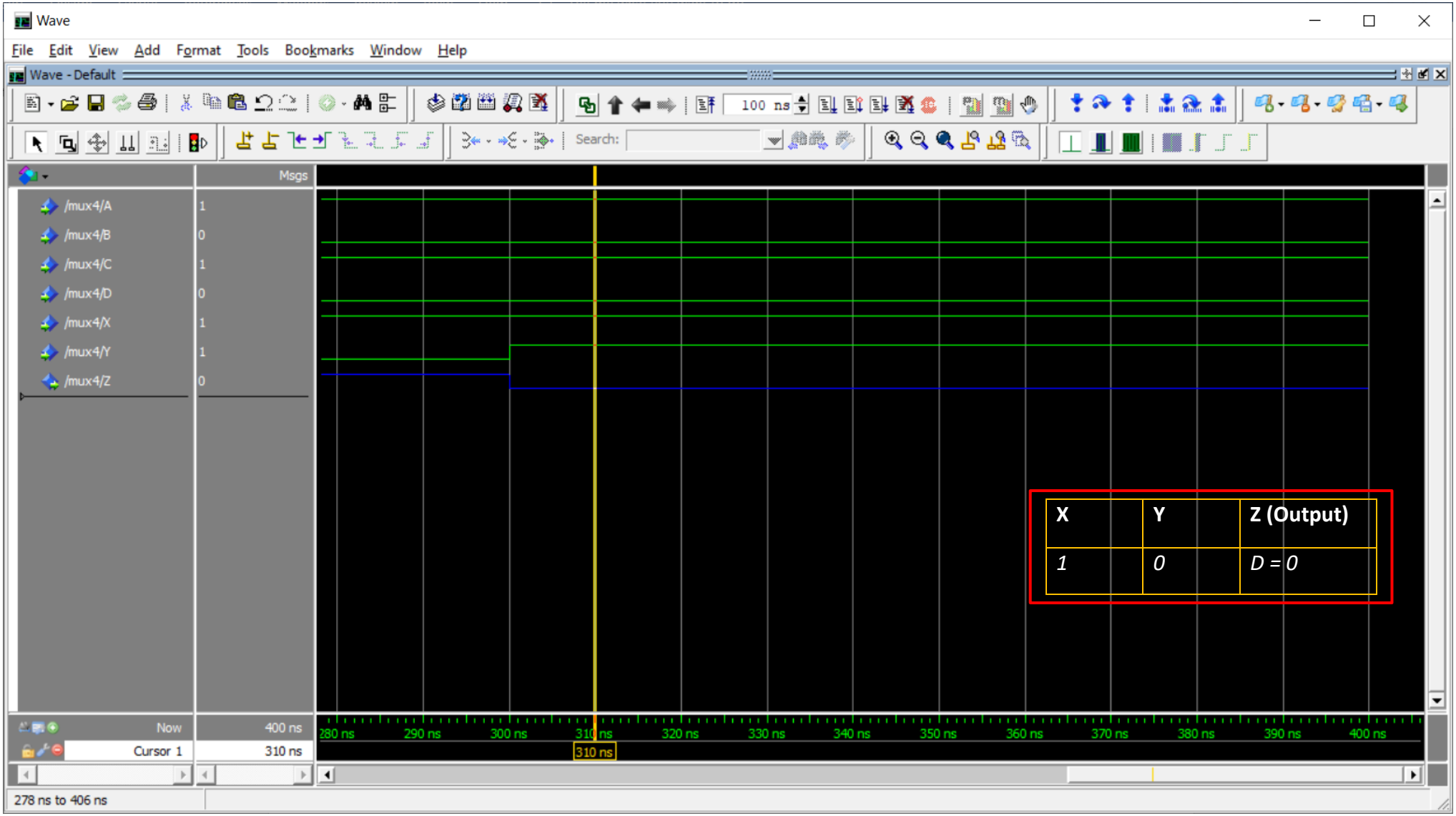
X	Y	Z (Output)
0	*1*	*B = 0*

Waveform #3:



X	Y	Z (Output)
1	*0*	*C = 1*

Waveform #4:



X	Y	Z (Output)
1	*0*	*D = 0*