Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC **4950**)

REPORT

Objective: Design and simulate a 5-bit Majority Circuit.

Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:

C:\Modeltech_pe_edu_10.4a\examples\5bitmajoritychecker.vhd

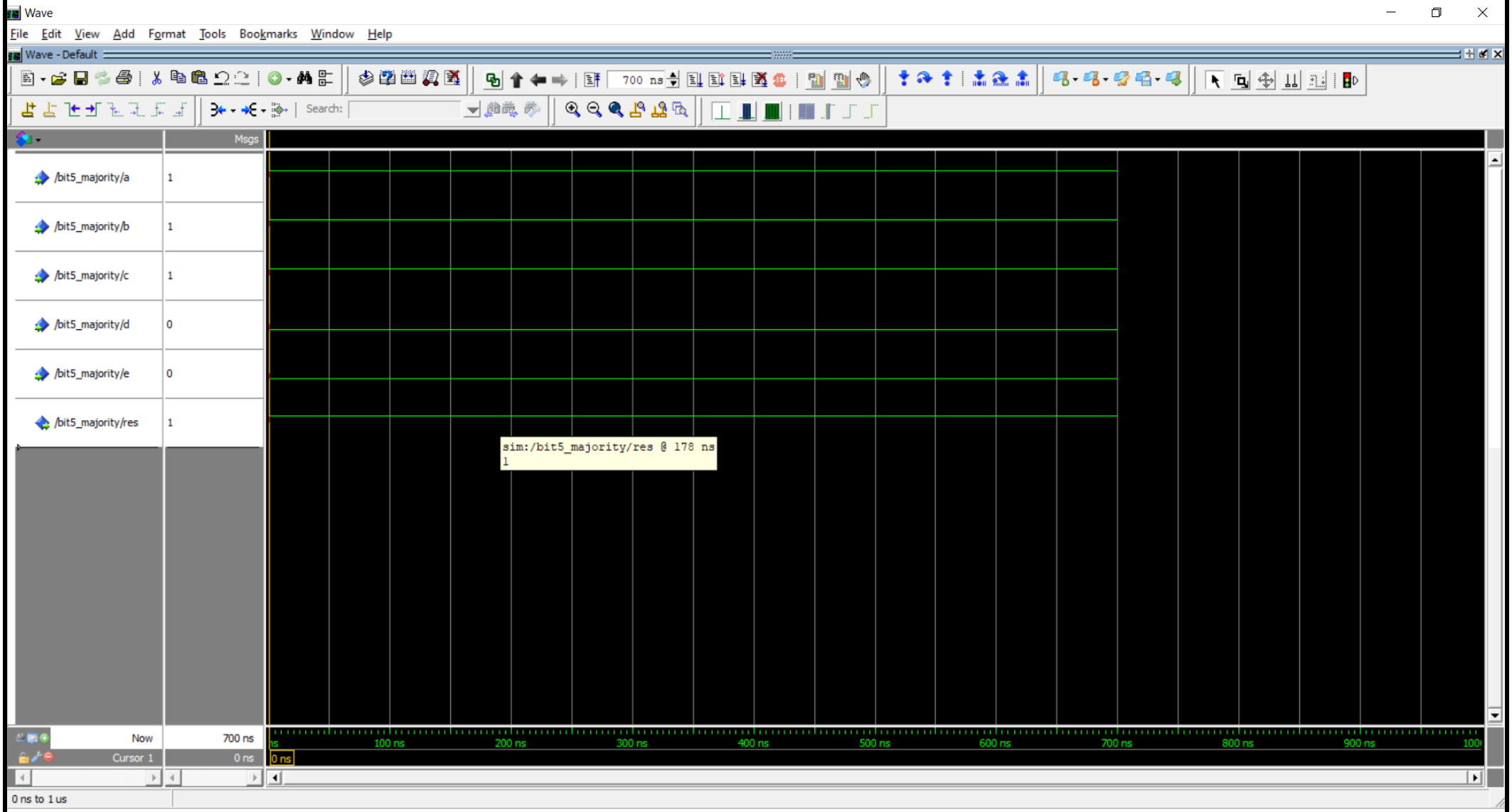
File Edit View Tools Bookmarks Window Help

C:\Modeltech_pe_edu_10.4a\examples\5bitmajoritychecker.vhd - Default *

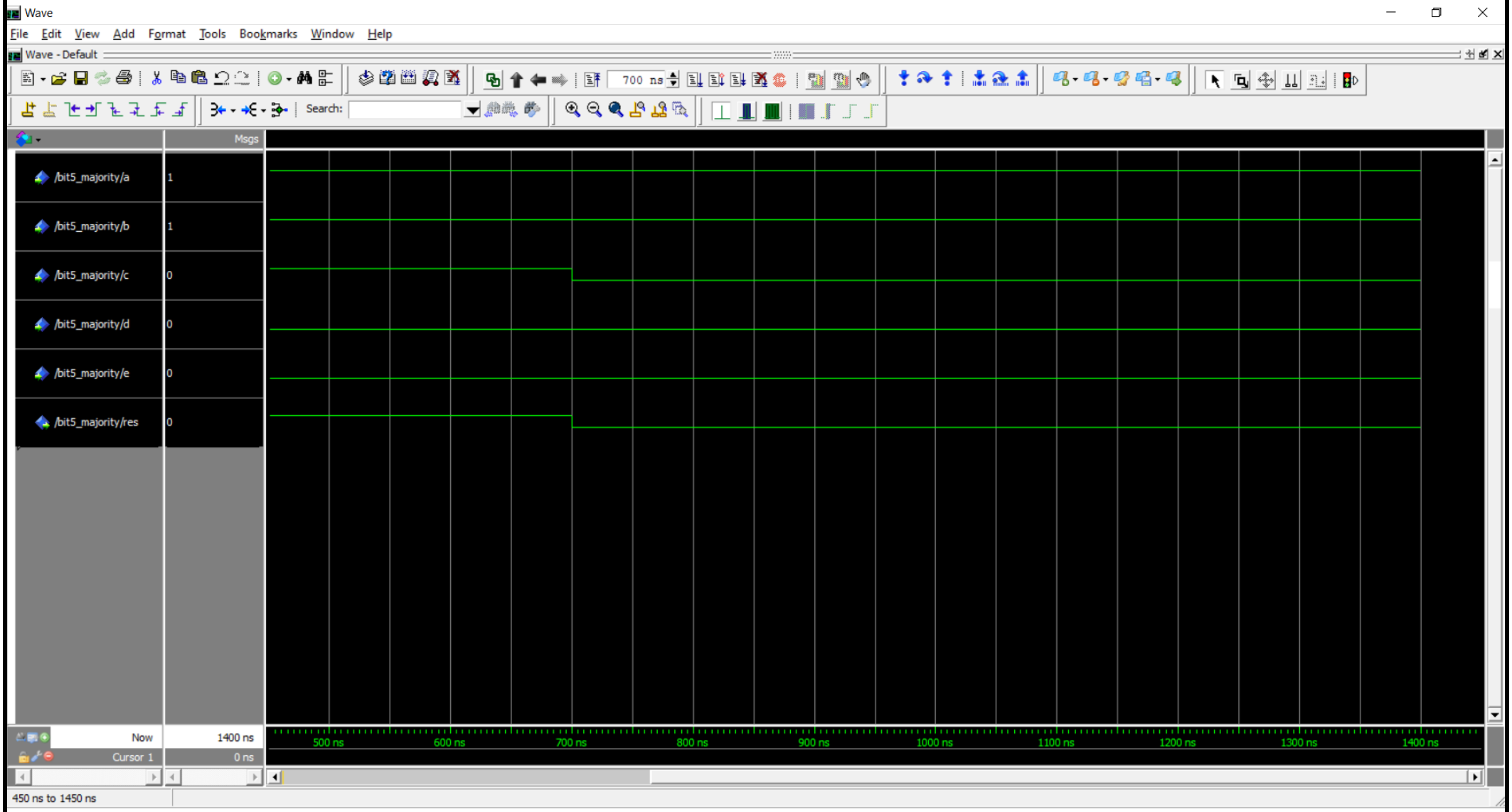
```
1  --Name: Ravi Sahni
2  --Faculty No.: 17 COB 085
3  --Enrol. No.: GJ 7718
4  --Assignment: Design and simulate a 5-bit Majority Circuit.
5
6  LIBRARY ieee;
7  USE ieee.std_logic_1164.ALL;
8
9  ENTITY bit5_Majority IS
10 PORT(
11 a, b, c, d, e : IN STD_LOGIC;
12 res : OUT STD_LOGIC);
13 END bit5_Majority;
14
15 ARCHITECTURE basic OF bit5_Majority IS
16 BEGIN
17 res <=  ((a and b and c)
18         or (a and b and d)
19         or (a and b and e)
20         or (a and c and d)
21         or (a and c and e)
22         or (a and d and e)
23         or (b and c and d)
24         or (b and c and e)
25         or (b and d and e)
26         or (c and d and e));
27
28 END basic;
29
```

Ln: 30 Col: 0

Waveform #1:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/bit5_majority/a
1
/bit5_majority/b
1
/bit5_majority/c
1
/bit5_majority/d
0
/bit5_majority/e
0
/bit5_majority/res
1
sim:/bit5_majority/res @ 178 ns
1
Now
700 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
0 ns
0 ns to 1 us

Waveform #2:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/bit5_majority/a
/bit5_majority/b
/bit5_majority/c
/bit5_majority/d
/bit5_majority/e
/bit5_majority/res
1
1
0
0
0
0
Now
1400 ns
Cursor 1
0 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1000 ns
1100 ns
1200 ns
1300 ns
1400 ns
450 ns to 1450 ns