Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC **4950**)

REPORT

Objective: Design and simulate a 9-bit Comparator using a 6-bit and a 3-bit comparator in ModelSim.

Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:

C:/Modeltech_pe_edu_10.4a/examples/9bitcomp.vhd (/bit9_comp)

File Edit View Tools Bookmarks Window Help

C:/Modeltech_pe_edu_10.4a/examples/9bitcomp.vhd (/bit9_comp) - Default

Ln# 1791 ns

```
1  --Name: Ravi Sahni
2  --Faculty No.: 17 COB 085
3  --Enrol. No.: GJ 7718
4  --Assignment: 9 bit Comparator using 6 bit & 3 bit Comparators.
5
6  --6 bit Comparator
7  library IEEE;
8  use IEEE.STD_LOGIC_1164.ALL;
9
10 entity bit6_comp is
11 Port (  a5,a4,a3,a2,a1,a0: in STD_LOGIC;
12         b5,b4,b3,b2,b1,b0: in STD_LOGIC;
13         g,l,e : out STD_LOGIC);
14 end bit6_comp;
15
16 architecture Behavioral of bit6_comp is
17 begin
18
19 g<= (a5 and (not b5))
20 or  ((a5 xnor b5) and (a4 and (not b4)))
21 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 and (not b3)))
22 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (a2 and (not b2)))
23 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (a2 xnor b2) and (a1 and (not b1)))
24 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (a2 xnor b2) and (a1 xnor b1) and (a0 and (not b0)));
25
26 l<= (b5 and (not a5))
27 or  ((a5 xnor b5) and (b4 and (not a4)))
28 or  ((a5 xnor b5) and (a4 xnor b4) and (b3 and (not a3)))
29 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (b2 and (not a2)))
30 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (a2 xnor b2) and (b1 and (not a1)))
31 or  ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (a2 xnor b2) and (a1 xnor b1) and (b0 and (not a0)));
32
33 e<= ((a5 xnor b5) and (a4 xnor b4) and (a3 xnor b3) and (a2 xnor b2) and (a1 xnor b1) and (a0 xnor b0));
34
35 end Behavioral;
36 ----------------------------------------------------------------------------------------------------
37 --3 bit Comparator
```

Ln: 5 Col: 0

VHDL Code: *(contd.)*

C:/Modeltech_pe_edu_10.4a/examples/9bitcomp.vhd (/bit9_comp)

File Edit View Tools Bookmarks Window Help

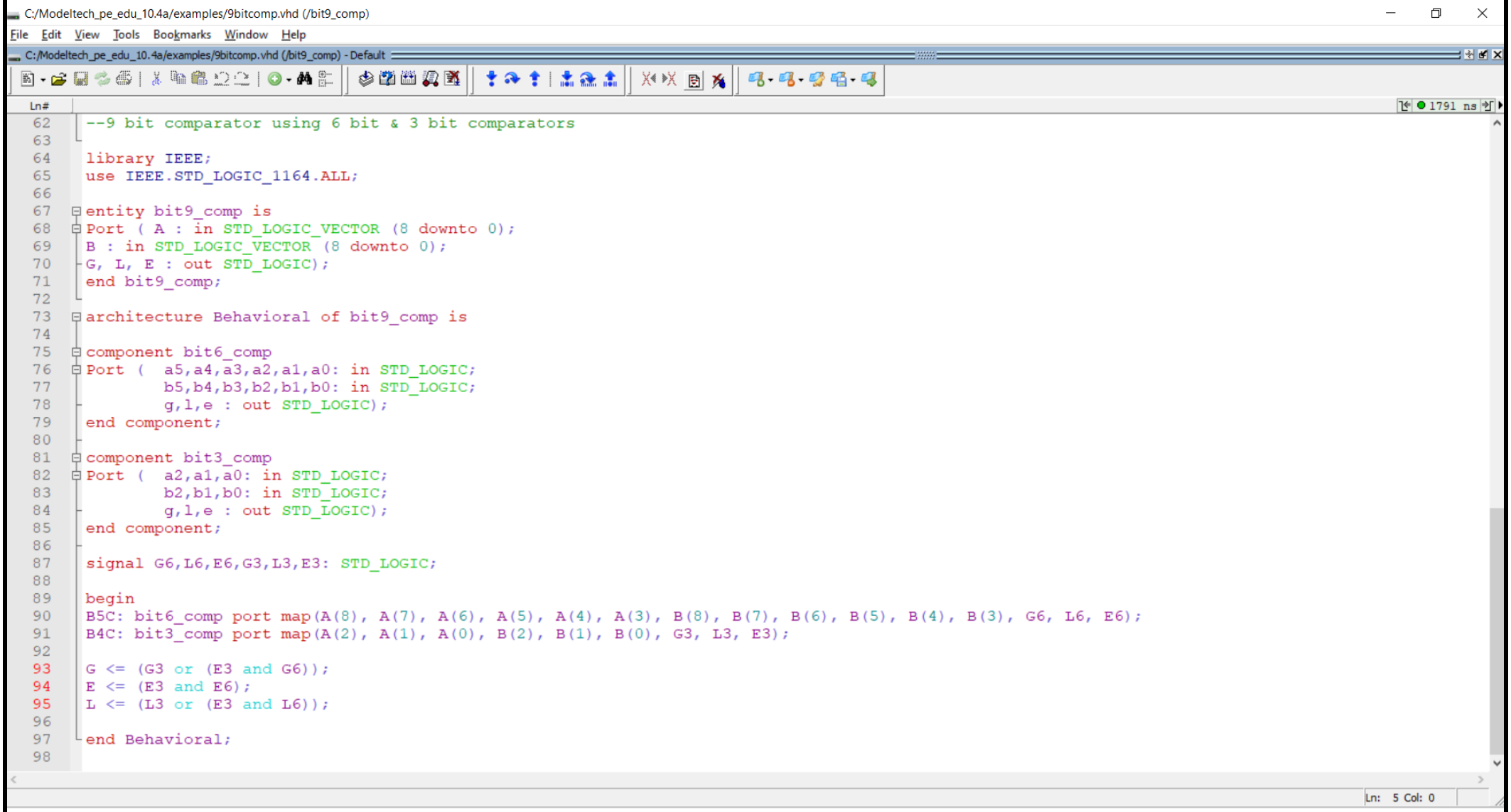
C:/Modeltech_pe_edu_10.4a/examples/9bitcomp.vhd (/bit9_comp) - Default

```
37  --3 bit Comparator
38  library IEEE;
39  use IEEE.STD_LOGIC_1164.ALL;
40
41  entity bit3_comp is
42  Port (  a2,a1,a0: in STD_LOGIC;
43          b2,b1,b0: in STD_LOGIC;
44          g,l,e : out STD_LOGIC);
45  end bit3_comp;
46
47  architecture Behavioral of bit3_comp is
48  begin
49
50  g<= (a2 and (not b2))
51  or  ((a2 xnor b2) and (a1 and (not b1)))
52  or  ((a2 xnor b2) and (a1 xnor b1) and (a0 and (not b0)));
53
54  l<= (b2 and (not a2))
55  or  ((a2 xnor b2) and (b1 and (not a1)))
56  or  ((a2 xnor b2) and (a1 xnor b1) and (b0 and (not a0)));
57
58  e<= ((a2 xnor b2) and (a1 xnor b1) and (a0 xnor b0));
59
60  end Behavioral;
61  ----------------------------------------------------------------------------------------------------
62  --9 bit comparator using 6 bit & 3 bit comparators
63
64  library IEEE;
65  use IEEE.STD_LOGIC_1164.ALL;
66
67  entity bit9_comp is
68  Port ( A : in STD_LOGIC_VECTOR (8 downto 0);
69  B : in STD_LOGIC_VECTOR (8 downto 0);
70  G, L, E : out STD_LOGIC);
71  end bit9_comp;
72
73  architecture Behavioral of bit9_comp is
```

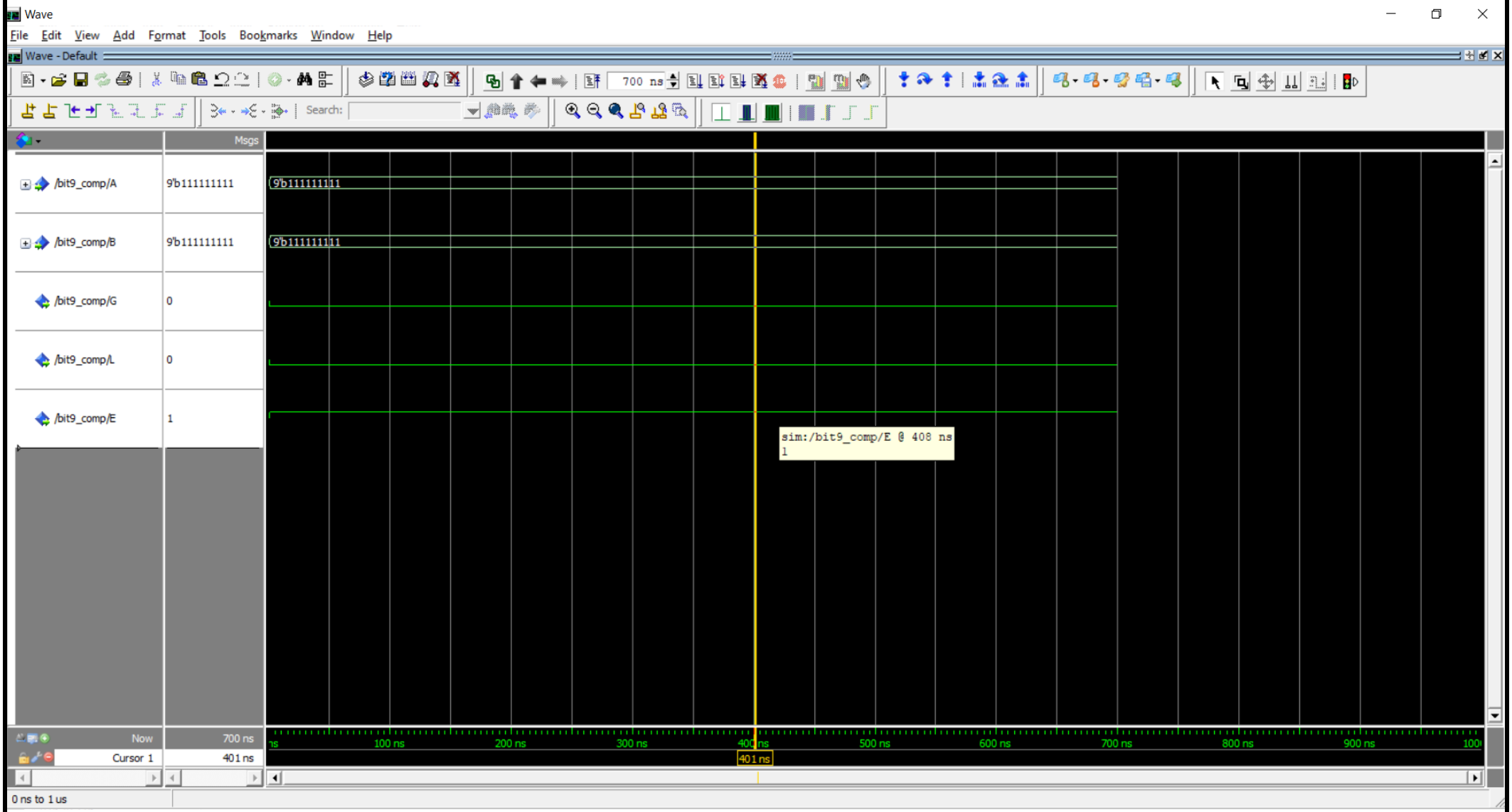
1791 ns

Ln: 5 Col: 0

VHDL Code: *(contd.)*



Waveform #1: *111111111 = 111111111*



Waveform #2: *101010101 > 010101010*