Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC **4950**)

REPORT

Objective: Design and simulate a 6-bit Carry Select Adder using ModelSim.

Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:

C:\Modeltech_pe_edu_10.4a\examples\6bitCSA.vhd

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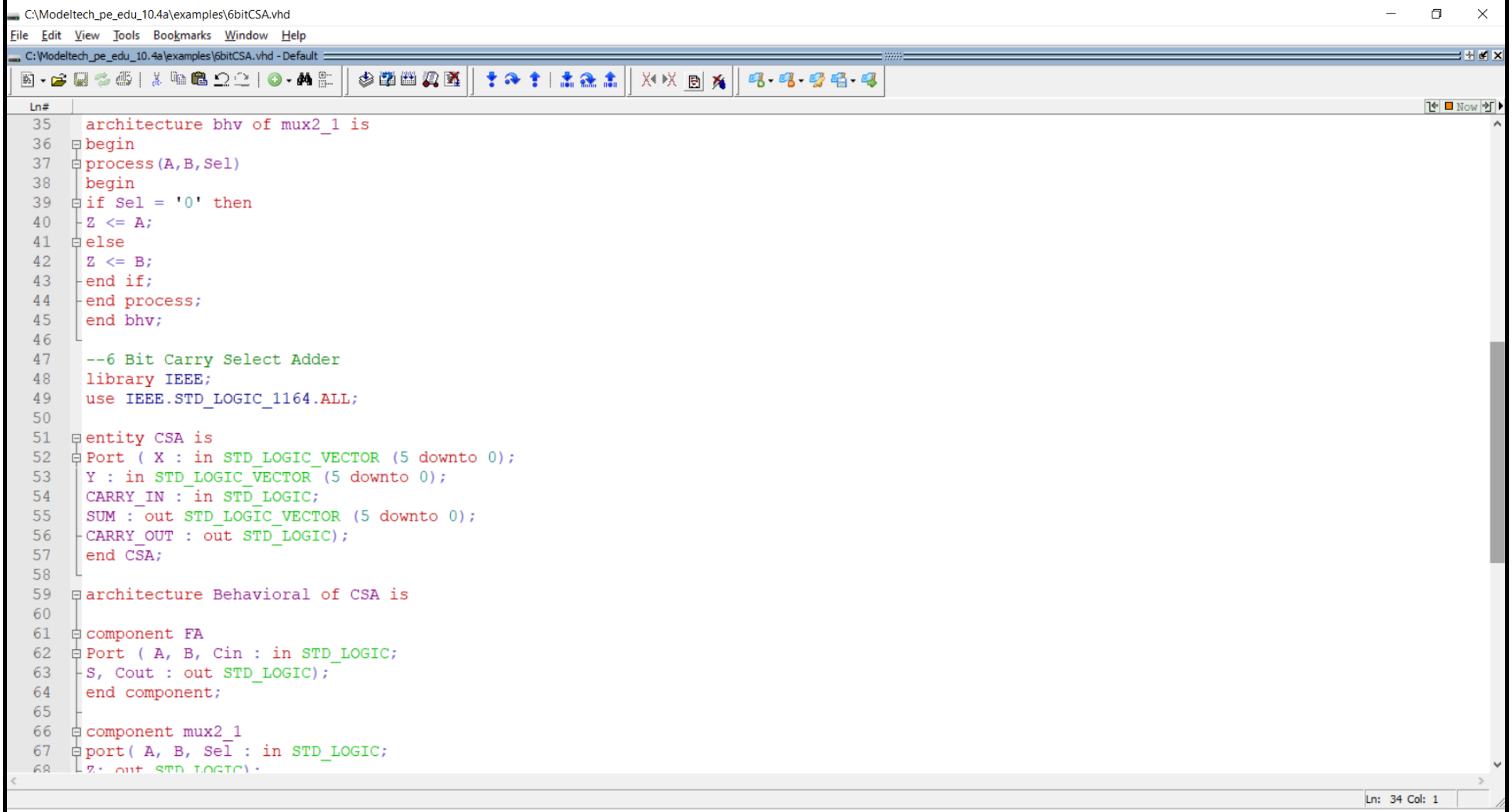
C:\Modeltech_pe_edu_10.4a\examples\6bitCSA.vhd - Default

```
1  --Name: Ravi Sahni
2  --Faculty No.: 17 COB 085
3  --Enrol. No.: GJ 7718
4  --Assignment: Design and simulate a 6-bit Carry Select Adder.
5
6  --Full Adder
7  library IEEE;
8  use IEEE.STD_LOGIC_1164.all;
9
10 entity FA is
11 Port ( A : in STD_LOGIC;
12 B : in STD_LOGIC;
13 Cin : in STD_LOGIC;
14 S : out STD_LOGIC;
15 Cout : out STD_LOGIC);
16 end FA;
17
18 architecture Basic of FA is
19 begin
20 S <= A XOR B XOR Cin;
21 Cout <= (A AND B) OR (Cin AND (A OR B));
22 end Basic;
23
24 --2x1 MUX
25 library IEEE;
26 use IEEE.STD_LOGIC_1164.all;
27
28 entity mux2_1 is
29 port(
30 A,B : in STD_LOGIC;
31 Sel: in STD_LOGIC;
32 Z: out STD_LOGIC);
33 end mux2_1;
34
```

Ln: 49 Col: 28

VHDL Code: *(contd.)*



VHDL Code: *(contd.)*

C:\Modeltech_pe_edu_10.4a\examples\6bitCSA.vhd

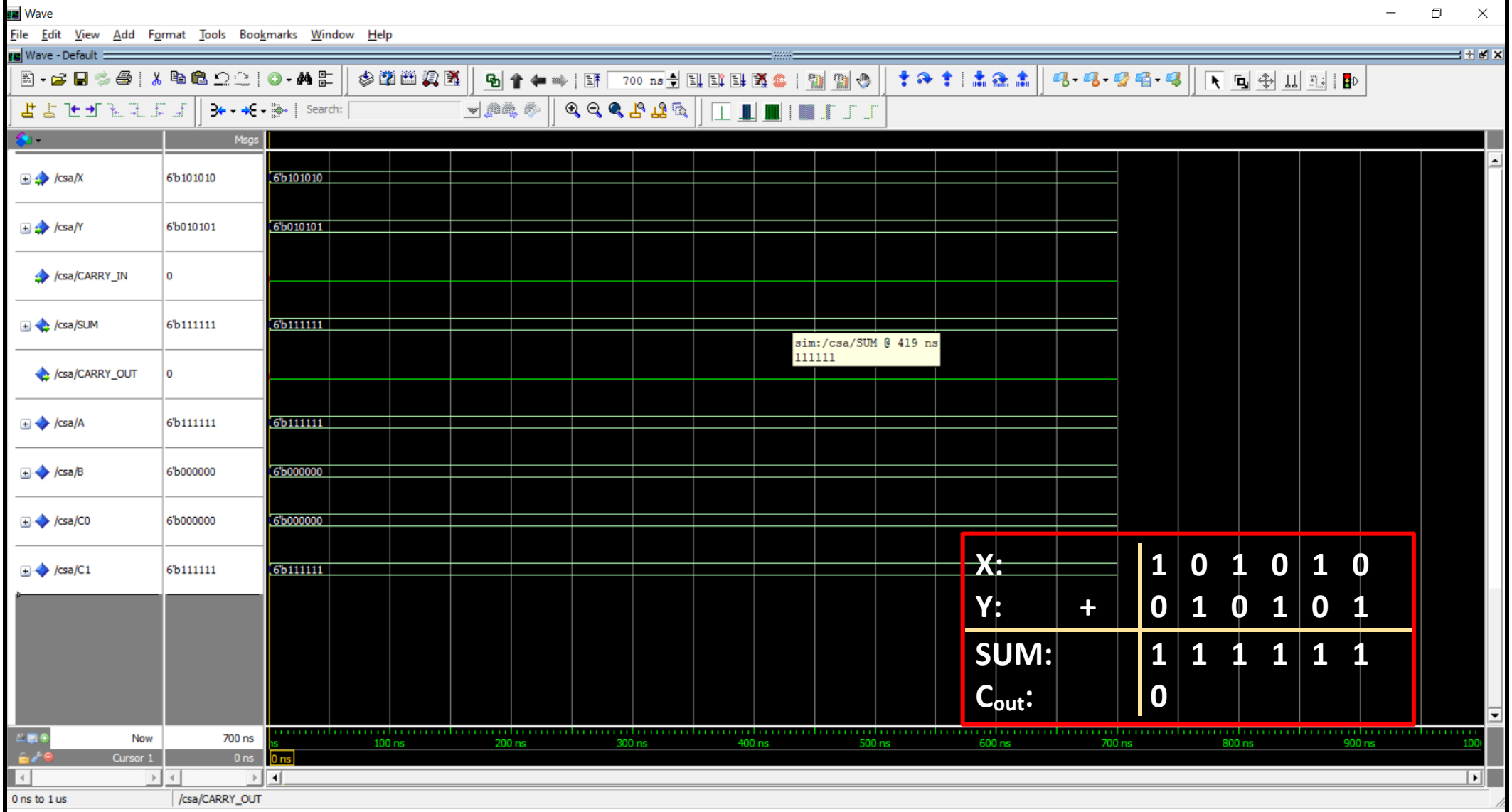
File Edit View Tools Bookmarks Window Help

C:\Modeltech_pe_edu_10.4a\examples\6bitCSA.vhd - Default

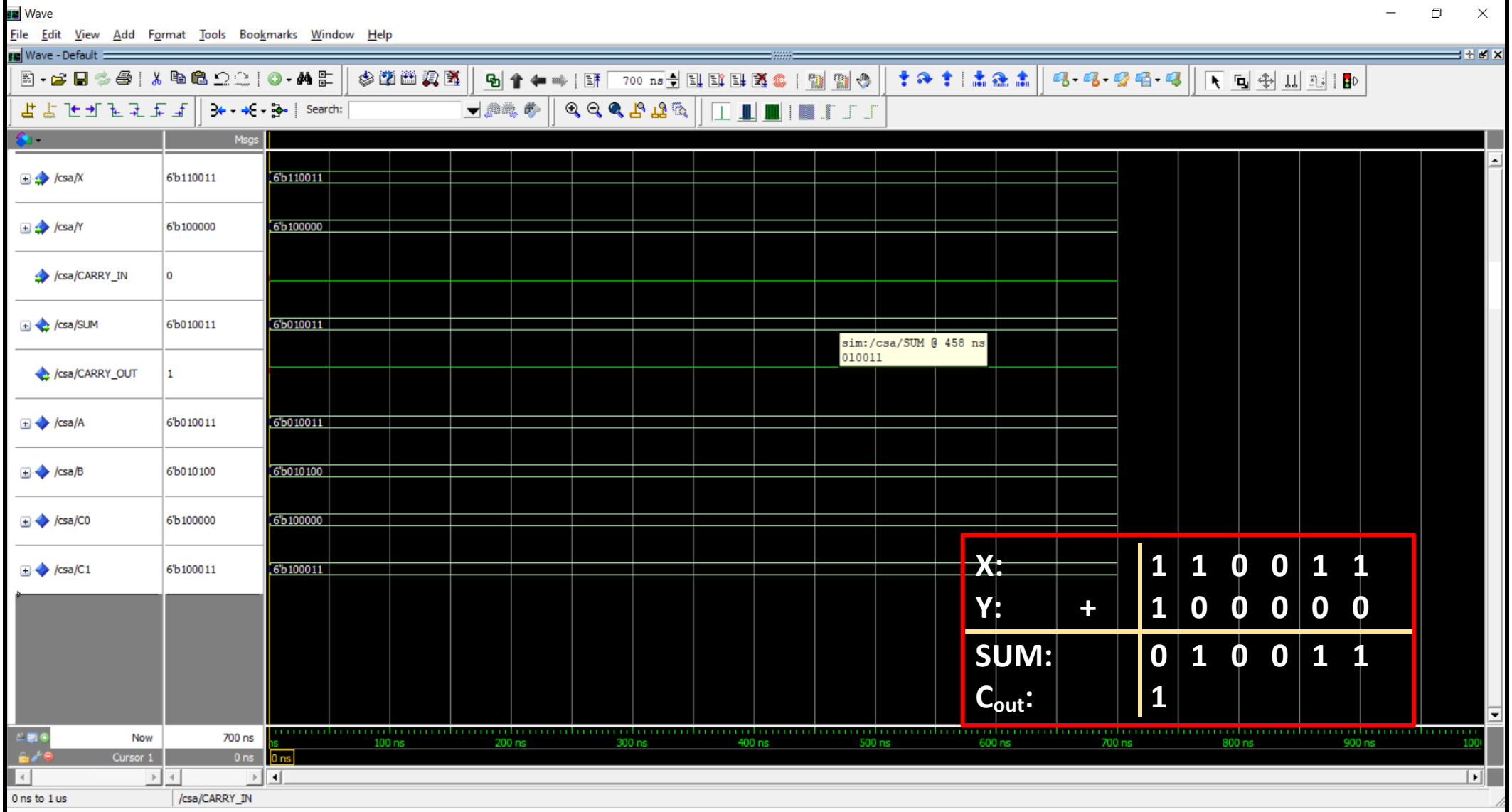
```
66  component mux2_1
67  port( A, B, Sel : in STD_LOGIC;
68  Z: out STD_LOGIC);
69  end component;
70
71  signal A,B,C0,C1: STD_LOGIC_VECTOR (5 DOWNTO 0);
72  begin
73
74  FA1: FA PORT MAP(X(0),Y(0),'0' ,A(0),C0(0));
75  FA2: FA PORT MAP(X(1),Y(1),C0(0),A(1),C0(1));
76  FA3: FA PORT MAP(X(2),Y(2),C0(1),A(2),C0(2));
77  FA4: FA PORT MAP(X(3),Y(3),C0(2),A(3),C0(3));
78  FA5: FA PORT MAP(X(4),Y(4),C0(3),A(4),C0(4));
79  FA6: FA PORT MAP(X(5),Y(5),C0(4),A(5),C0(5));
80
81  FA7: FA PORT MAP(X(0),Y(0),'1' ,B(0),C1(0));
82  FA8: FA PORT MAP(X(1),Y(1),C1(0),B(1),C1(1));
83  FA9: FA PORT MAP(X(2),Y(2),C1(1),B(2),C1(2));
84  FA10: FA PORT MAP(X(3),Y(3),C1(2),B(3),C1(3));
85  FA11: FA PORT MAP(X(4),Y(4),C1(3),B(4),C1(4));
86  FA12: FA PORT MAP(X(5),Y(5),C1(4),B(5),C1(5));
87
88  MUX1: mux2_1 PORT MAP(A(0),B(0),CARRY_IN,SUM(0));
89  MUX2: mux2_1 PORT MAP(A(1),B(1),CARRY_IN,SUM(1));
90  MUX3: mux2_1 PORT MAP(A(2),B(2),CARRY_IN,SUM(2));
91  MUX4: mux2_1 PORT MAP(A(3),B(3),CARRY_IN,SUM(3));
92  MUX5: mux2_1 PORT MAP(A(4),B(4),CARRY_IN,SUM(4));
93  MUX6: mux2_1 PORT MAP(A(5),B(5),CARRY_IN,SUM(5));
94
95  MUX7: mux2_1 PORT MAP(C0(5),C1(5),CARRY_IN,CARRY_OUT);
96
97  end Behavioral;
98
```

Ln: 34 Col: 1

Waveform #1:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/csa/X 6'b101010
/csa/Y 6'b010101
/csa/CARRY_IN 0
/csa/SUM 6'b111111
/csa/CARRY_OUT 0
/csa/A 6'b111111
/csa/B 6'b000000
/csa/C0 6'b000000
/csa/C1 6'b111111
6'b101010
6'b010101
6'b111111
sim:/csa/SUM @ 419 ns
111111
6'b111111
6'b000000
6'b000000
6'b111111
X: 1 0 1 0 1 0
Y: + 0 1 0 1 0 1
SUM: 1 1 1 1 1 1
Cout: 0
Now 700 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns
0 ns to 1 us
/csa/CARRY_OUT

Waveform #2:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/csa/X 6'b110011
/csa/Y 6'b100000
/csa/CARRY_IN 0
/csa/SUM 6'b010011
/csa/CARRY_OUT 1
/csa/A 6'b010011
/csa/B 6'b010100
/csa/C0 6'b100000
/csa/C1 6'b100011
6'b110011
6'b100000
6'b010011
sim:/csa/SUM @ 458 ns
010011
6'b010011
6'b010100
6'b100000
6'b100011
X: 1 1 0 0 1 1
Y: + 1 0 0 0 0 0
SUM: 0 1 0 0 1 1
Cout: 1
Now 700 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns
0 ns to 1 us
/csa/CARRY_IN