Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC **4950**)

REPORT

Objective: Design and simulate a 4-bit Ripple Adder using ModelSim.

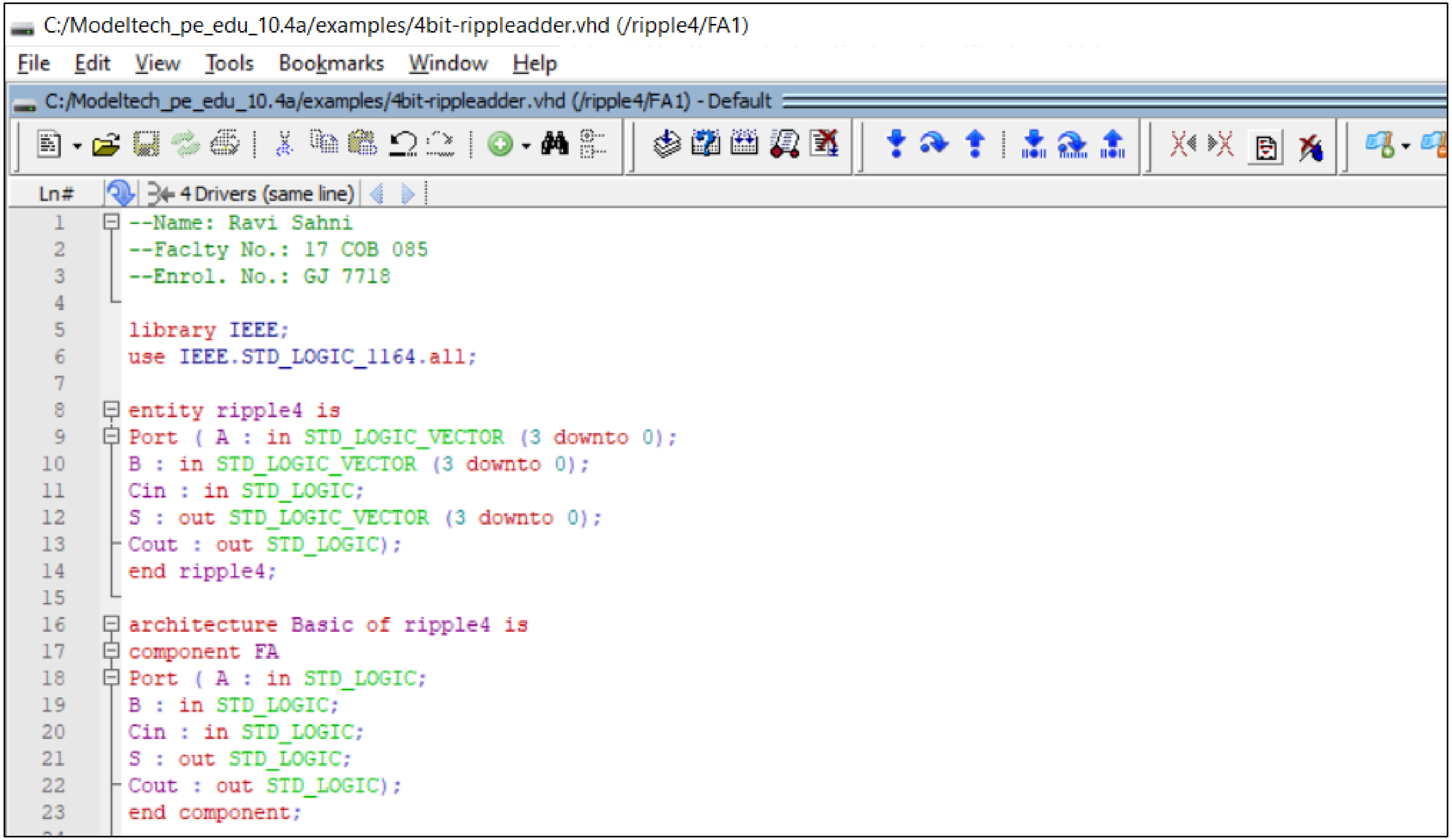
Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:



C:/Modeltech_pe_edu_10.4a/examples/4bit-rippleadder.vhd (/ripple4/FA1)
File
Edit
View
Tools
Bookmarks
Window
Help
C:/Modeltech_pe_edu_10.4a/examples/4bit-rippleadder.vhd (/ripple4/FA1) - Default
Ln#
4 Drivers (same line)

```
--Name: Ravi Sahni
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library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity ripple4 is
Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
B : in STD_LOGIC_VECTOR (3 downto 0);
Cin : in STD_LOGIC;
S : out STD_LOGIC_VECTOR (3 downto 0);
Cout : out STD_LOGIC);
end ripple4;

architecture Basic of ripple4 is
component FA
Port ( A : in STD_LOGIC;
B : in STD_LOGIC;
Cin : in STD_LOGIC;
S : out STD_LOGIC;
Cout : out STD_LOGIC);
end component;
```
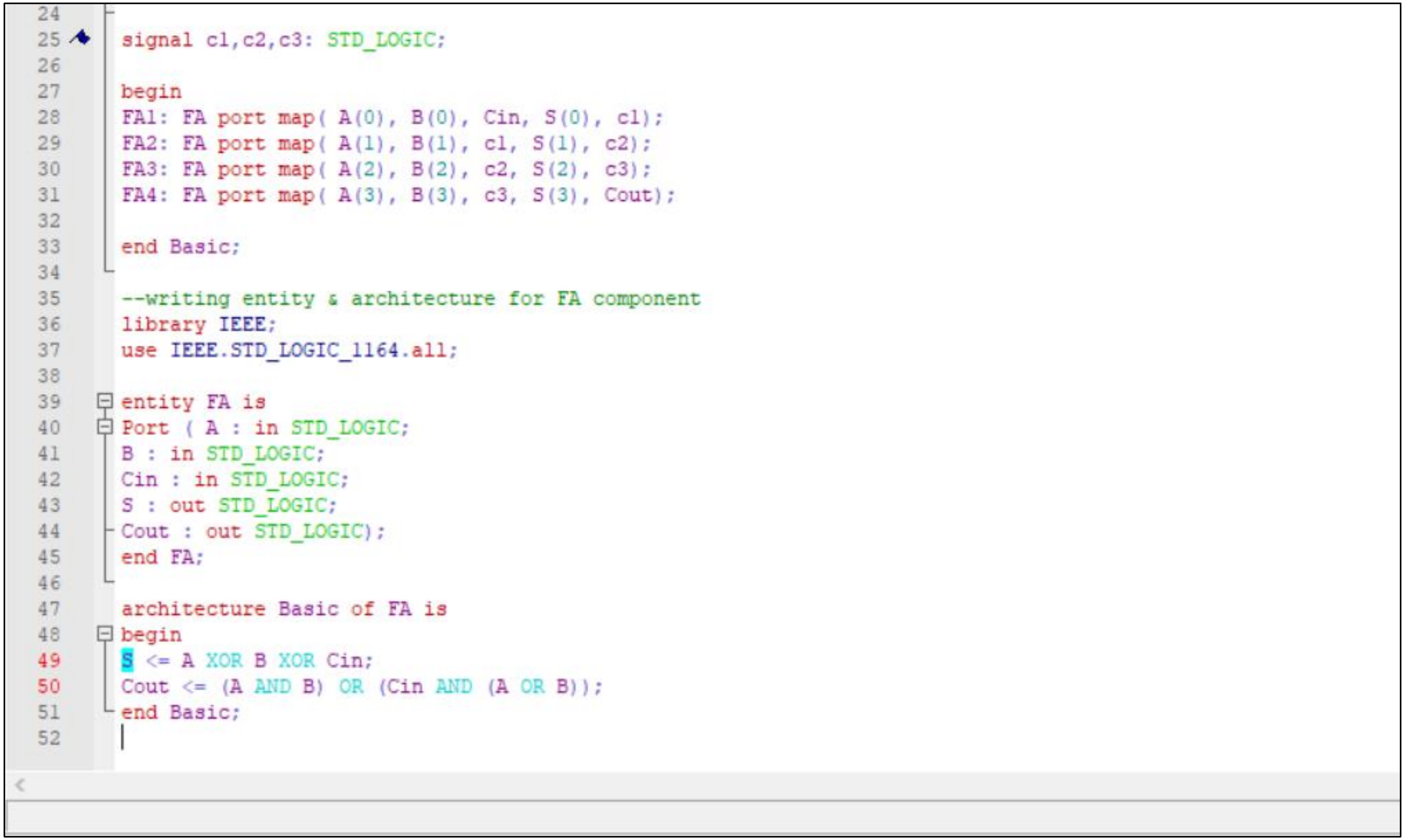
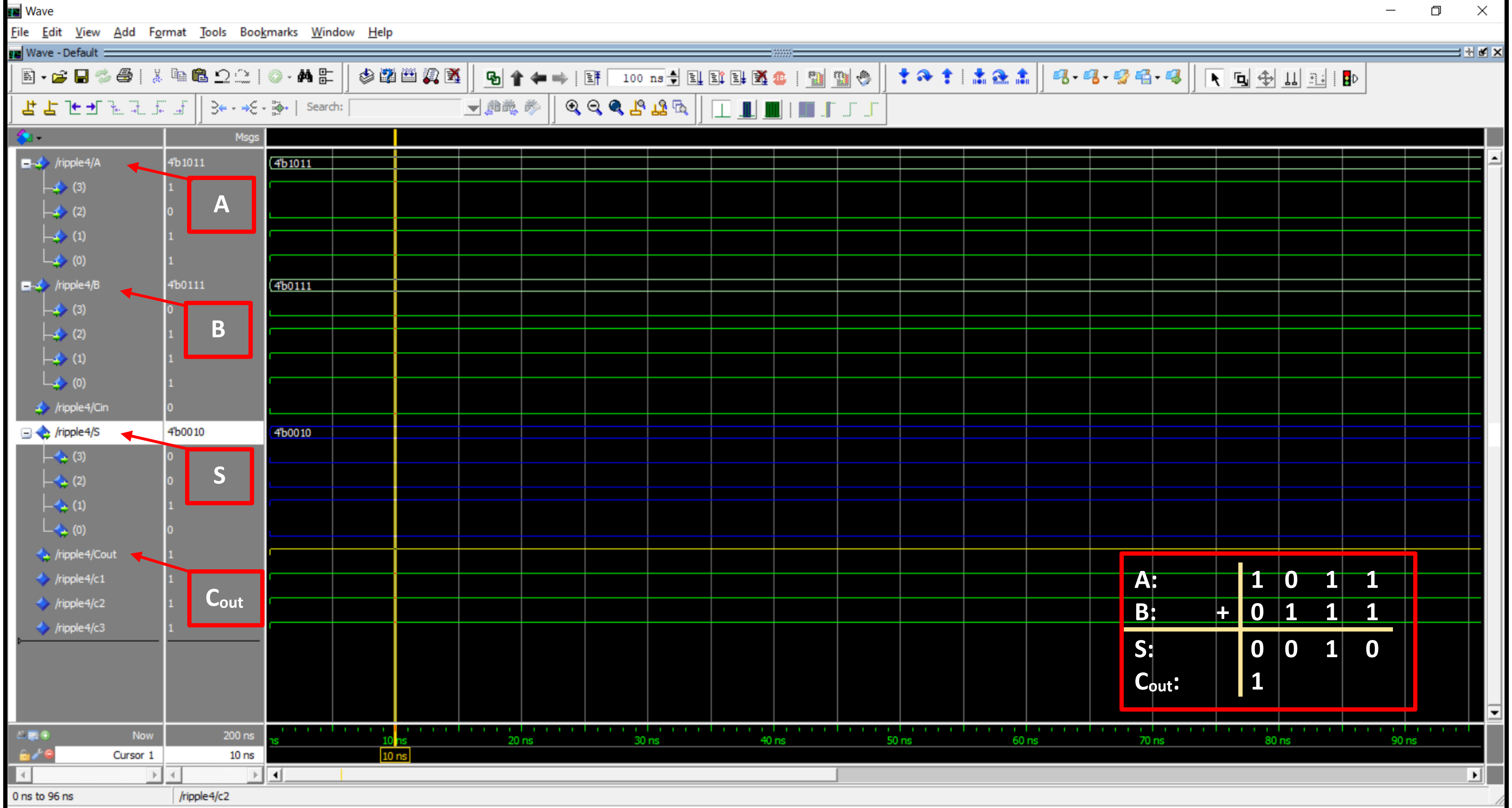

VHDL Code: *(contd.)*



```vhdl

signal c1,c2,c3: STD_LOGIC;

begin
FA1: FA port map( A(0), B(0), Cin, S(0), c1);
FA2: FA port map( A(1), B(1), c1, S(1), c2);
FA3: FA port map( A(2), B(2), c2, S(2), c3);
FA4: FA port map( A(3), B(3), c3, S(3), Cout);

end Basic;

--writing entity & architecture for FA component
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity FA is
Port ( A : in STD_LOGIC;
B : in STD_LOGIC;
Cin : in STD_LOGIC;
S : out STD_LOGIC;
Cout : out STD_LOGIC);
end FA;

architecture Basic of FA is
begin
S <= A XOR B XOR Cin;
Cout <= (A AND B) OR (Cin AND (A OR B));
end Basic;

```

Waveform #1:



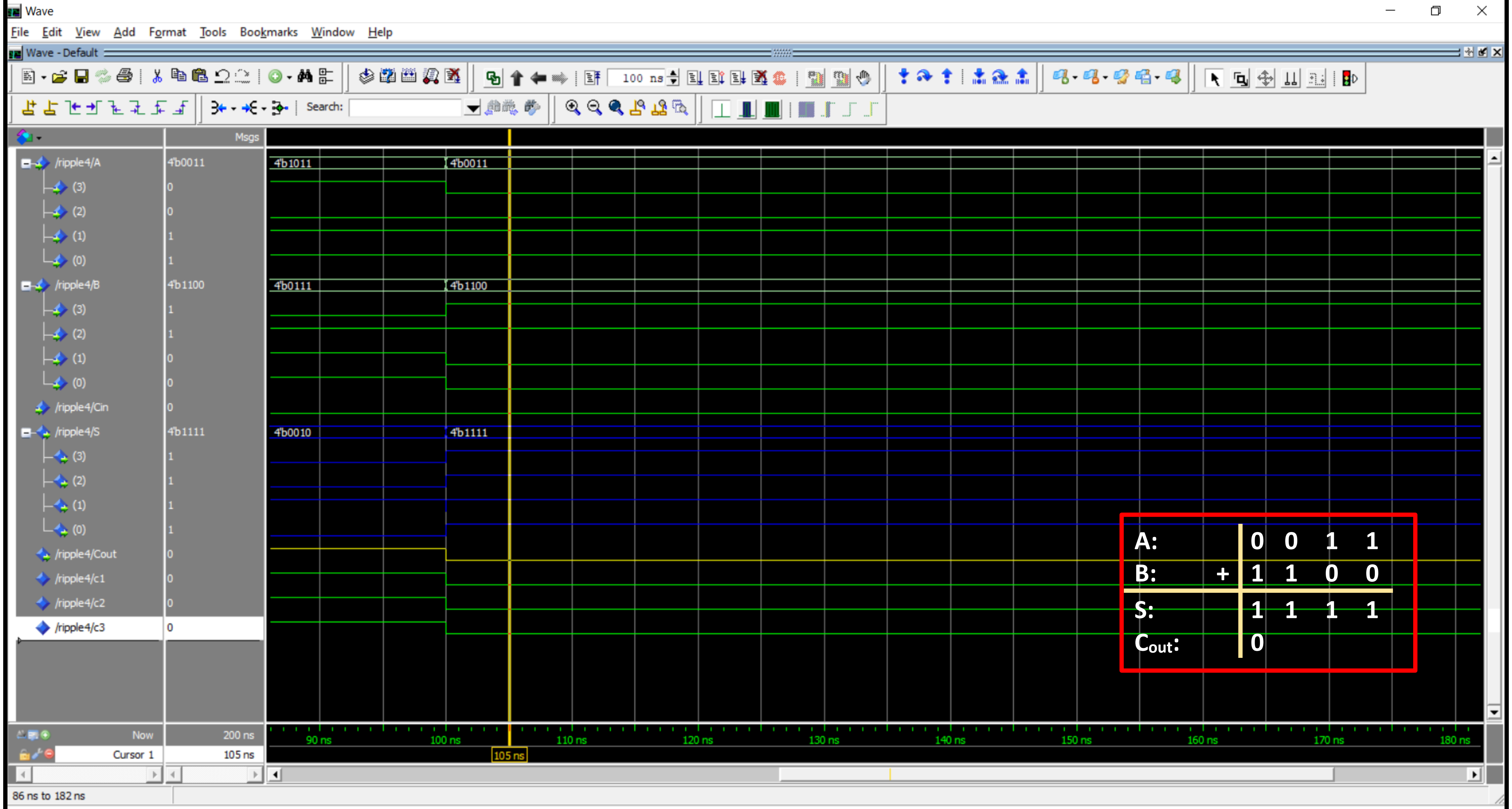
	Msgs
/ripple4/A	4'b1011
(3)	1
(2)	0
(1)	1
(0)	1
/ripple4/B	4'b0111
(3)	0
(2)	1
(1)	1
(0)	1
/ripple4/Cin	0
/ripple4/S	4'b0010
(3)	0
(2)	0
(1)	1
(0)	0
/ripple4/Cout	1
/ripple4/c1	1
/ripple4/c2	1
/ripple4/c3	1
Now	200 ns
Cursor 1	10 ns

0 ns to 96 ns

/ripple4/c2

A:		1	0	1	1
B:	+	0	1	1	1
S:		0	0	1	0
C_{out}:		1			

Waveform #2:

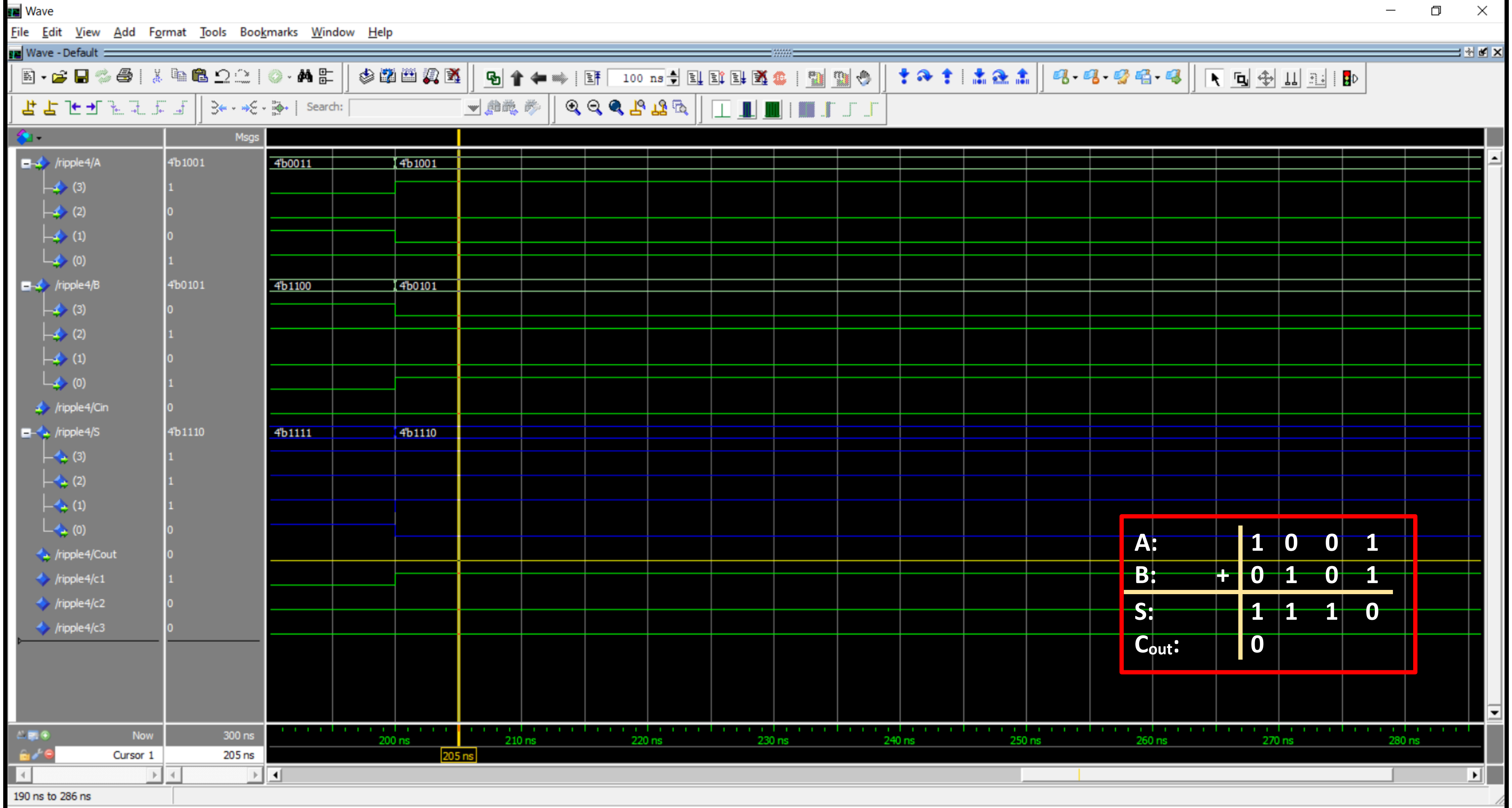


	Msgs
/ripple4/A	4'b0011
(3)	0
(2)	0
(1)	1
(0)	1
/ripple4/B	4'b1100
(3)	1
(2)	1
(1)	0
(0)	0
/ripple4/Cin	0
/ripple4/S	4'b1111
(3)	1
(2)	1
(1)	1
(0)	1
/ripple4/Cout	0
/ripple4/c1	0
/ripple4/c2	0
/ripple4/c3	0
Now	200 ns
Cursor 1	105 ns

86 ns to 182 ns

A:		0	0	1	1
B:	+	1	1	0	0
S:		1	1	1	1
C_{out}:		0			

Waveform #3:



Signal	Msgs
/ripple4/A	4'b1001
(3)	1
(2)	0
(1)	0
(0)	1
/ripple4/B	4'b0101
(3)	0
(2)	1
(1)	0
(0)	1
/ripple4/Cin	0
/ripple4/S	4'b1110
(3)	1
(2)	1
(1)	1
(0)	0
/ripple4/Cout	0
/ripple4/c1	1
/ripple4/c2	0
/ripple4/c3	0
Now	300 ns
Cursor 1	205 ns

190 ns to 286 ns

A:		1	0	0	1
B:	+	0	1	0	1
S:		1	1	1	0
C_{out}:		0			