

*Z.H.C.E.T., Aligarh Muslim University – Aligarh*

## **Network & Embedded Systems Lab**

(COC **4950**)

# **REPORT**

**Objective:** Design and simulate a 4 to 1 multiplexer using ModelSim.

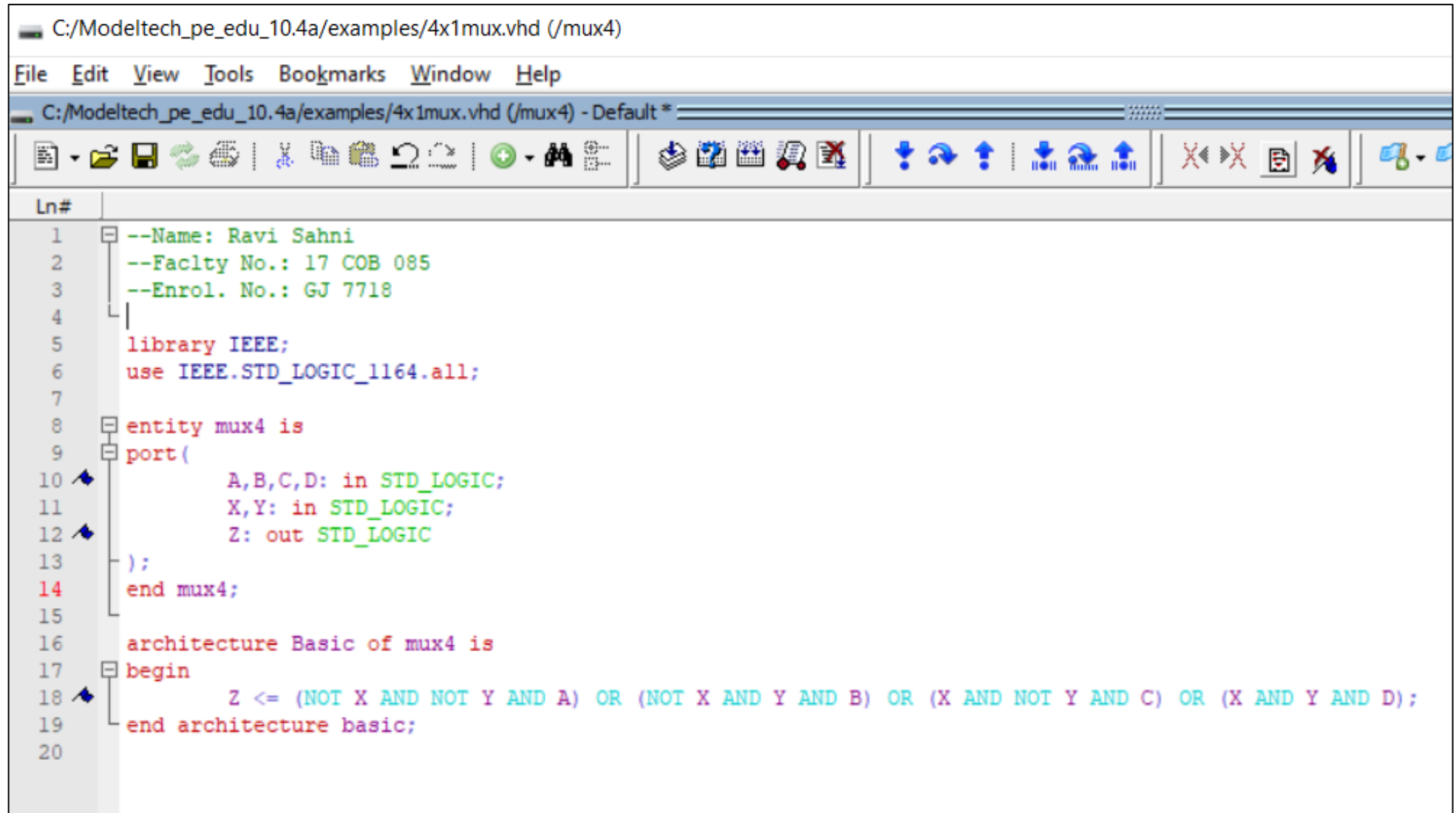
Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

## Simulation Environment: ModelSim PE Student Edition 10.4a

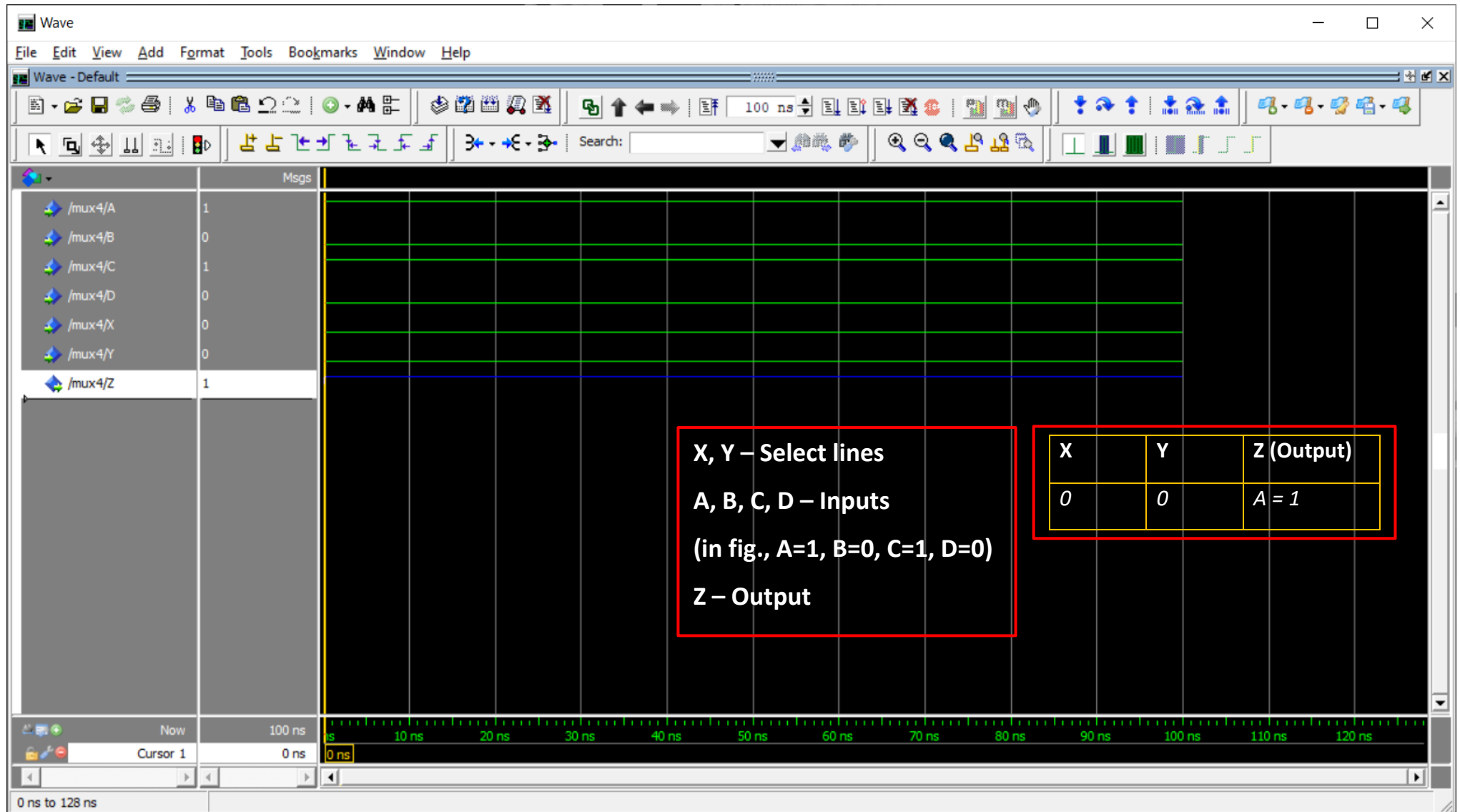
### VHDL Code:



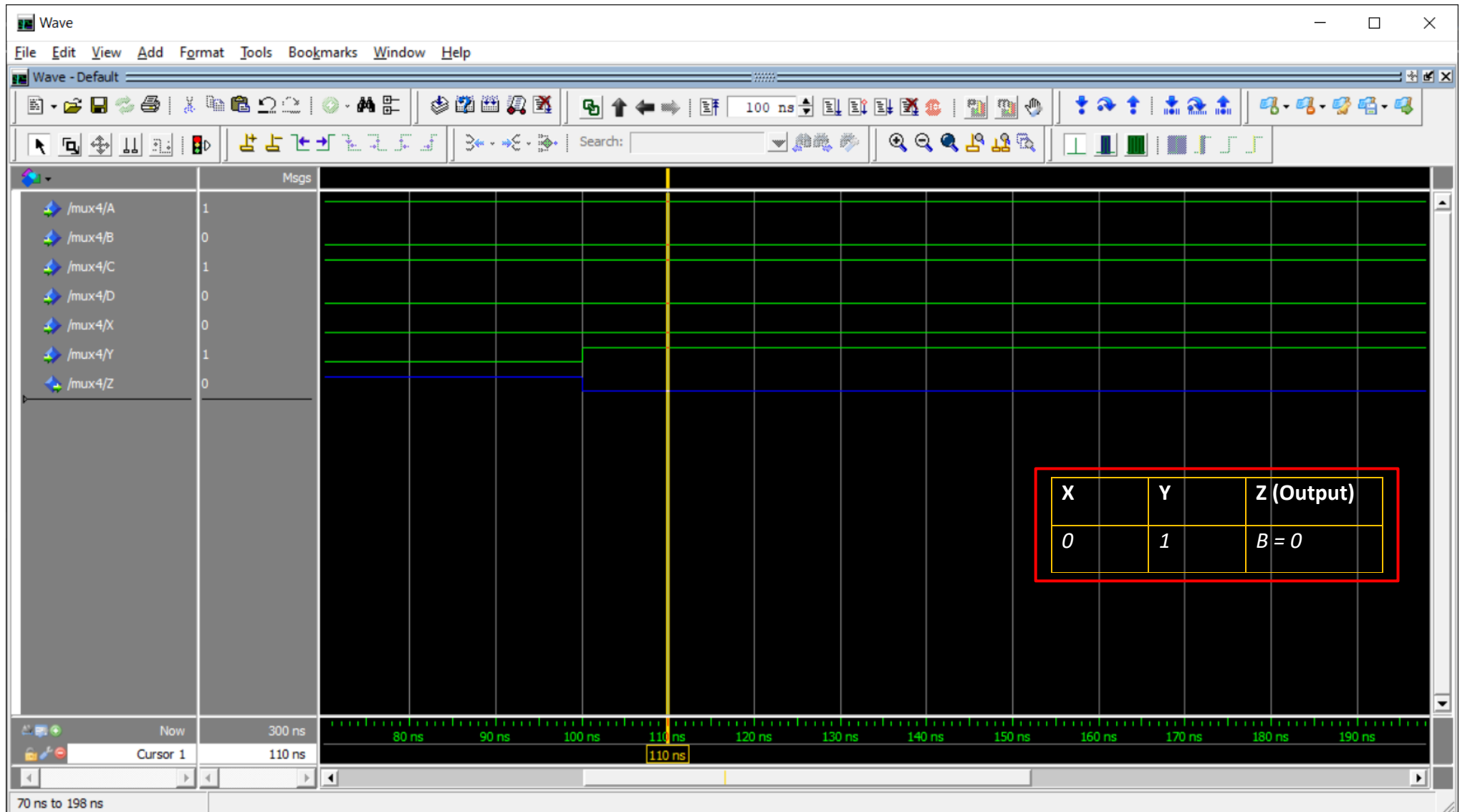
The screenshot displays the ModelSim PE Student Edition 10.4a interface. The title bar indicates the file path: C:/Modeltech\_pe\_edu\_10.4a/examples/4x1mux.vhd (/mux4). The menu bar includes File, Edit, View, Tools, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and debugging. The main text area shows the VHDL code for a 4x1 multiplexer, with line numbers (Ln#) on the left. The code includes comments for the author (Ravi Sahni), faculty number (17 COB 085), and enrollment number (GJ 7718). It uses the IEEE STD\_LOGIC\_1164.all library. The entity 'mux4' is defined with four input ports (A, B, C, D) and one output port (Z), all of type STD\_LOGIC. The architecture 'Basic of mux4' implements the logic for the multiplexer using a single OR gate expression.

```
Ln# 1  --Name: Ravi Sahni
    2  --Facilty No.: 17 COB 085
    3  --Enrol. No.: GJ 7718
    4
    5  library IEEE;
    6  use IEEE.STD_LOGIC_1164.all;
    7
    8  entity mux4 is
    9  port(
10      A,B,C,D: in STD_LOGIC;
11      X,Y: in STD_LOGIC;
12      Z: out STD_LOGIC
13  );
14  end mux4;
15
16  architecture Basic of mux4 is
17  begin
18      Z <= (NOT X AND NOT Y AND A) OR (NOT X AND Y AND B) OR (X AND NOT Y AND C) OR (X AND Y AND D);
19  end architecture basic;
20
```

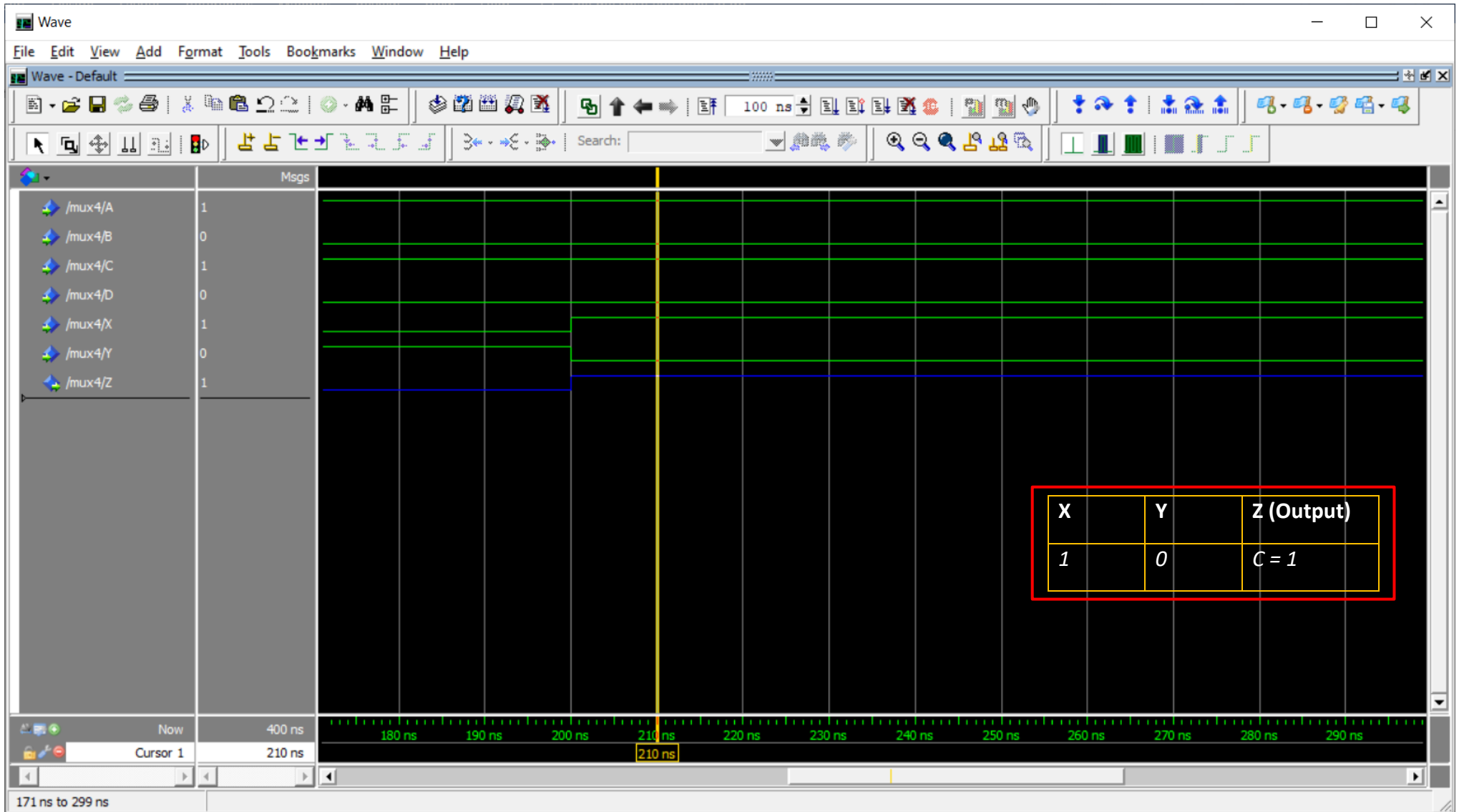
## Waveform #1:



## Waveform #2:



## Waveform #3:



## Waveform #4:

