*Z.H.C.E.T., Aligarh Muslim University – Aligarh*

**Network & Embedded Systems Lab**

(COC **4950**)

# REPORT

**Objective:** Design and simulate a 5-bit Odd-Down Counter.

Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

**Simulation Environment:** ModelSim PE Student Edition 10.4a

**VHDL Code:**

C:\Modeltech_pe_edu_10.4a\examples\oddcounter.vhd

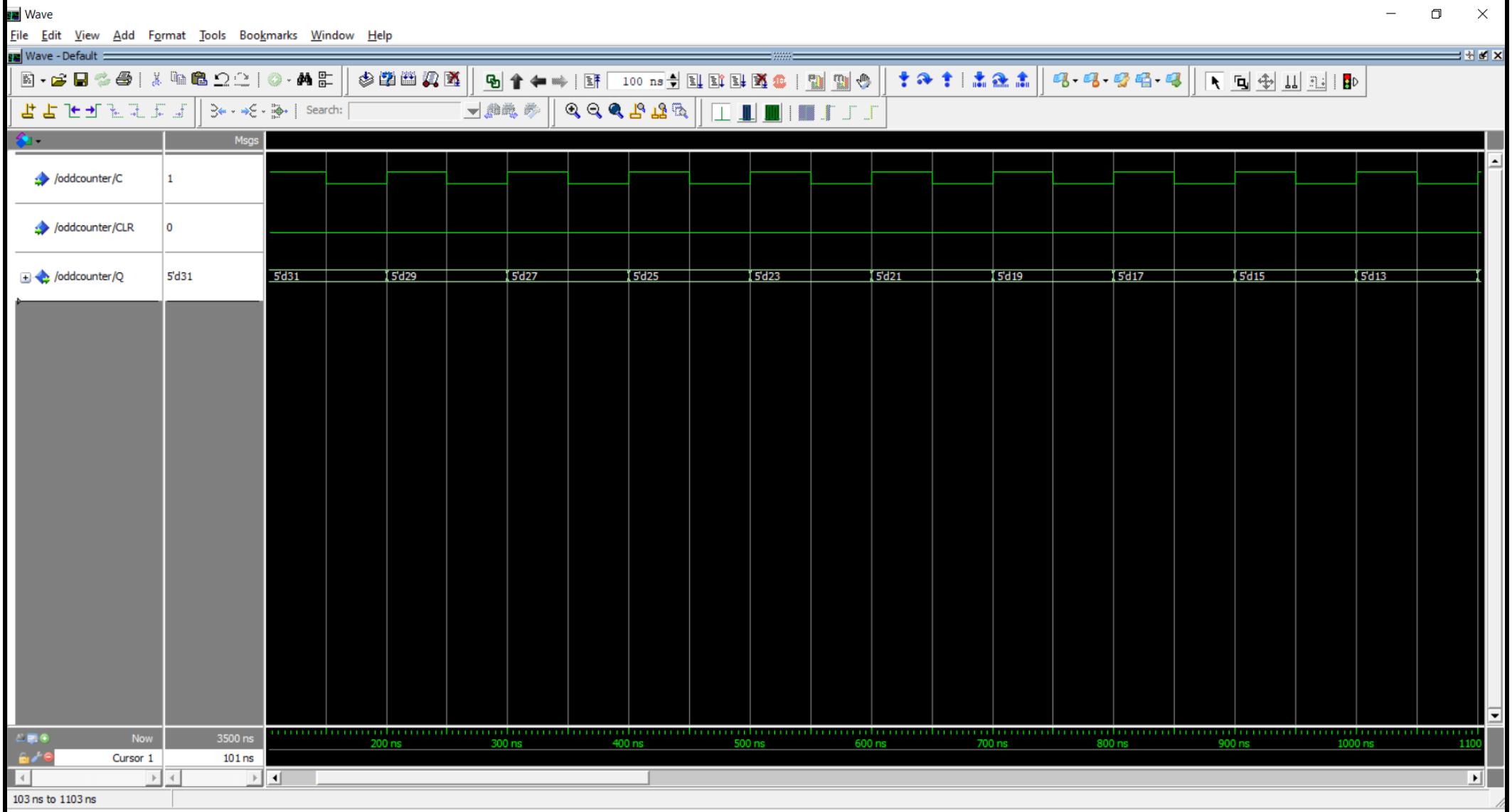
File Edit View Tools Bookmarks Window Help

C:\Modeltech_pe_edu_10.4a\examples\oddcounter.vhd - Default *

```
--Name: Ravi Sahni
--Faculty No.: 17 COB 085
--Enrol. No.: GJ 7718
--Assignment: Design and simulate a 5-bit Odd-Down Counter

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity oddcounter is
port
(       C, CLR : in  std_logic;
        Q : out std_logic_vector(4 downto 0)
);
end oddcounter;

architecture bhv of oddcounter is
        signal tmp: std_logic_vector(4 downto 0);
        begin
                process (C, CLR)
                        begin
                        if (CLR='1') then
                                tmp <= "11111";
                        elsif (C'event and C='1') then
                                tmp <= tmp - 2;
                        end if;
                end process;
      Q <= tmp;
end bhv;
```

Ln: 30 Col: 0

## Waveform #1:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/oddcounter/C
1
/oddcounter/CLR
0
/oddcounter/Q
5'd31
5'd31
5'd29
5'd27
5'd25
5'd23
5'd21
5'd19
5'd17
5'd15
5'd13
Now
3500 ns
Cursor 1
101 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1000 ns
1100
103 ns to 1103 ns

**Video Clip:**

https://drive.google.com/file/d/1IyfYRsUwWrXOJsMSFaccpQLc7lz6qf25/view?usp=sharing