

Z.H.C.E.T., Aligarh Muslim University – Aligarh

Network & Embedded Systems Lab

(COC 4950)

REPORT

Objective: Design and Simulate 5 Bit Carry Look-Ahead Adder using ModelSim.

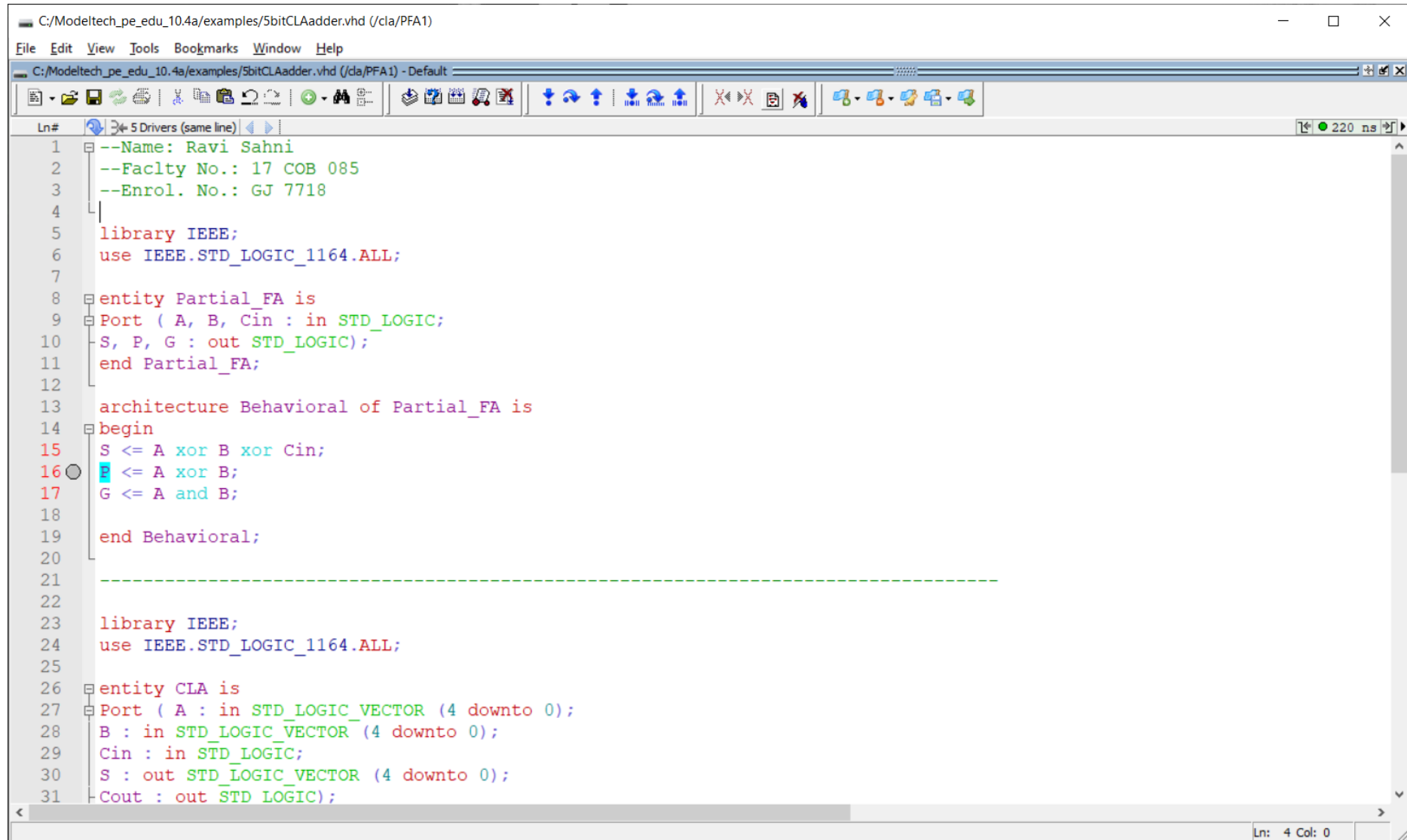
Submitted by: **Ravi Sahni**

Faculty No.: **17 COB 085**

Enrolment No.: **GJ 7718**

Simulation Environment: ModelSim PE Student Edition 10.4a

VHDL Code:



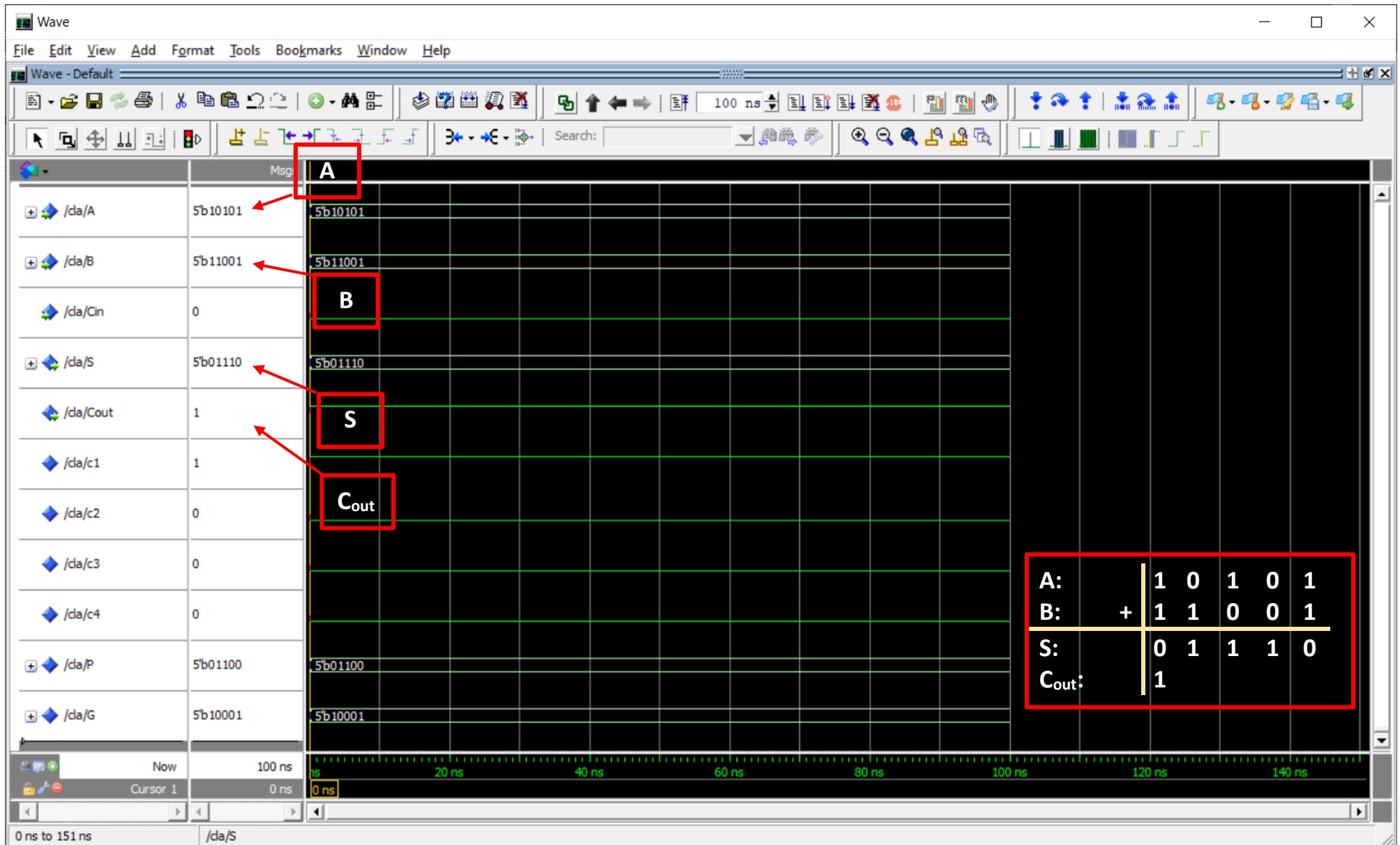
The screenshot shows the ModelSim PE Student Edition 10.4a interface. The title bar indicates the file path: C:/Modeltech_pe_edu_10.4a/examples/5bitCLAadder.vhd (/cla/PFA1). The menu bar includes File, Edit, View, Tools, Bookmarks, Window, and Help. The toolbar contains various icons for file operations, simulation, and debugging. The main text area displays the VHDL code for a 5-bit CLA adder. The code is organized into two entities: Partial_FA and CLA. The Partial_FA entity defines the logic for a single full adder, and the CLA entity defines the logic for the 5-bit carry lookahead adder. The code is color-coded, with keywords in red, identifiers in blue, and literals in green. A line number column on the left shows lines 1 through 31. The status bar at the bottom right indicates the current line and column: Ln: 4 Col: 0.

```
1  --Name: Ravi Sahni
2  --Facilty No.: 17 COB 085
3  --Enrol. No.: GJ 7718
4
5  library IEEE;
6  use IEEE.STD_LOGIC_1164.ALL;
7
8  entity Partial_FA is
9  Port ( A, B, Cin : in STD_LOGIC;
10       S, P, G : out STD_LOGIC);
11  end Partial_FA;
12
13  architecture Behavioral of Partial_FA is
14  begin
15      S <= A xor B xor Cin;
16      P <= A xor B;
17      G <= A and B;
18
19  end Behavioral;
20
21  -----
22
23  library IEEE;
24  use IEEE.STD_LOGIC_1164.ALL;
25
26  entity CLA is
27  Port ( A : in STD_LOGIC_VECTOR (4 downto 0);
28       B : in STD_LOGIC_VECTOR (4 downto 0);
29       Cin : in STD_LOGIC;
30       S : out STD_LOGIC_VECTOR (4 downto 0);
31       Cout : out STD_LOGIC);
```

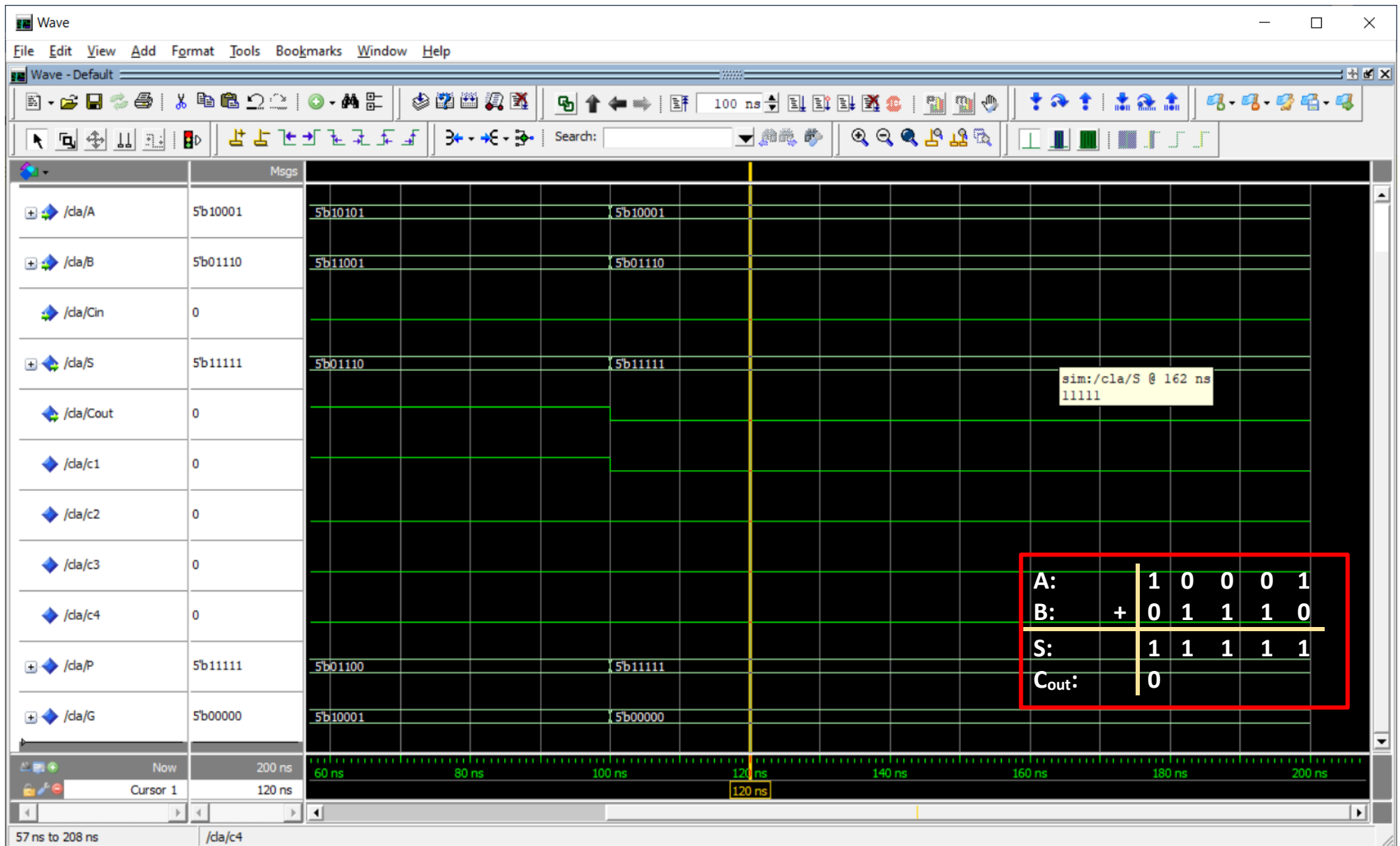
VHDL Code: (contd.)

```
C:/Modeltech_pe_edu_10.4a/examples/5bitCLAadder.vhd (/cla/PFA1)
File Edit View Tools Bookmarks Window Help
C:/Modeltech_pe_edu_10.4a/examples/5bitCLAadder.vhd (/cla/PFA1) - Default
Ln# 5 Drivers (same line) 220 ns
30 S : out STD_LOGIC_VECTOR (4 downto 0);
31 Cout : out STD_LOGIC;
32 end CLA;
33
34 architecture Behavioral of CLA is
35
36 component Partial_FA
37 Port ( A, B, Cin : in STD_LOGIC;
38 S, P, G : out STD_LOGIC);
39 end component;
40
41 signal c1,c2,c3,c4: STD_LOGIC;
42 signal P,G: STD_LOGIC_VECTOR(4 downto 0);
43 begin
44
45 PFA1: Partial_FA port map( A(0), B(0), Cin, S(0), P(0), G(0));
46 PFA2: Partial_FA port map( A(1), B(1), c1, S(1), P(1), G(1));
47 PFA3: Partial_FA port map( A(2), B(2), c2, S(2), P(2), G(2));
48 PFA4: Partial_FA port map( A(3), B(3), c3, S(3), P(3), G(3));
49 PFA5: Partial_FA port map( A(4), B(4), c4, S(4), P(4), G(4));
50
51 c1 <= G(0) OR (P(0) AND Cin);
52 c2 <= G(1) OR (P(1) AND G(0)) OR (P(1) AND P(0) AND Cin);
53 c3 <= G(2) OR (P(2) AND G(1)) OR (P(2) AND P(1) AND G(0)) OR (P(2) AND P(1) AND P(0) AND Cin);
54 c4 <= G(3) OR (P(3) AND G(2)) OR (P(3) AND P(2) AND G(1))
55 OR (P(3) AND P(2) AND P(1) AND G(0)) OR (P(3) AND P(2) AND P(1) AND P(0) AND Cin);
56 Cout <= G(4) OR (P(4) AND G(3)) OR (P(4) AND P(3) AND G(2)) OR (P(4) AND P(3) AND P(2) AND G(1))
57 OR (P(4) AND P(3) AND P(2) AND P(1) AND G(0)) OR (P(4) AND P(3) AND P(2) AND P(1) AND P(0) AND Cin);
58
59 end Behavioral;
60
Ln: 4 Col: 0
```

Waveform #1:



Waveform #2:



Waveform #3:

