EE2016 - Microprocessor Theory + Lab

Experiment-1

1 Introduction

This experiment involves (i) simulating a half-adder using Xilinx Vivado (ii) realizing the half-adder on the FPGA board (iii) extending the half-adder design to a full-adder, simulating the same (in Xilinx Vivado) and testing of the design on the FPGA board and (iv) designing a 4-bit ripple-carry adder in Verilog and implementing on the FPGA board.

2 Half-Adder Simulation and Realization on the FPGA Board

Write a half-adder module and stimulus (testbench) module to do a simulation in Xilinx Vivado. Then realize the half-adder on the FPGA board.

3 Full-Adder Simulation and Realization on the FPGA Board

A (partially-filled) Verilog module for the full-adder is given below. Complete the module, write a testbench module and perform a simulation in Xilinx Vivado. Then write a suitable Xilinx design constraints file (.xdc file) and combine it with the full-adder description module to implement the design on the FPGA board.

Note: You can define the full-adder in some other way if you wish (and write a suitable testbench file).

```
module fulladd(s, cout, a,b, cin);

input a;
input b;
input cin;
output s;
output cout;
wire s1, c1, c2;

xor (........);
and (..........);
xor (.........);
and (............);
xor (.................);

endmodule
```

4 Ripple Carry Adder

Design a 4-bit ripple carry adder in Verilog and extend the Xilinx design constraints file (.xdc file) you have written for the full adder to show the solution on the FPGA board. You may give inputs using the sliding switches (or hard code the input numbers). The output should appear on the LEDs on the board.

Note: Xilinx Vivado can be obtained free from the web and installed on your laptop/desktop. Please go to https://www.xilinx.com/support/download.html and take a look at the various versions available (you will need the Standard Edition and not the Lab Edition). If your laptop is old/does not support Windows, please do not worry ! Just visit the IE Lab (in ESB2) anytime you are free and use the desktops in the lab.

5 Report

Submit a report on the experiment on Moodle (within a week of this experiment). One report per group (with the names of the group members) is sufficient. The report should contain details of the solution (including the code) and your observations and experience (in programming and debugging). Please note that reports that closely match those of other groups will be penalized.