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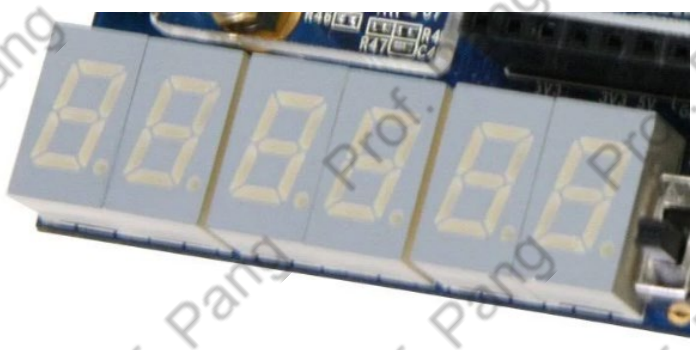
CPE166 Advanced Logic Design
Lab 3 Part 1
By Prof. Pang

Lab 3

Part 1: Seven Segment Display

Utilize four input switches and one seven-segment display device on the FPGA board to show numbers 0 through 9.

For example, if the binary value of the four input switches is "0011", then the decimal number 3 should be displayed on the seven-sgement display device.



<u>Demo</u>:

You need to download your SystemVerilog design on the FPGA board and show the result to your lab instructor.

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SystemVerilog

In SystemVerilog, you can use “logic” to replace both “wire” and “reg”.
You can utilize “always_comb” for designing combinational logic circuit.
SystemVerilog is a superset of Verilog and is compatible with it.

Sample SystemVerilog Syntax

```
module mycir ( input logic [1:0] a, output logic [3:0] f );
always_comb
 case(a)
  2'b00:  f = 4'b0001;
  2'b01:  f = 4'b0010;
  2'b10:  f = 4'b0100;
  2'b11:  f = 4'b1000;
  default: f = 4'b0000;
 endcase

endmodule


module svinv_tb;
logic [1:0] a;
logic [3:0] f;

mycir uut(a, f);

initial begin
  for(int i= 0; i<= 3; i++)
  begin
    a = i;
    #5;
  end
  #10 $stop;
end

endmodule
```