Lab4. Simplified Microprocessor Design

The purpose of parts 1, and part 2 of Lab 4 is to design s simplified microprocessor in **Verilog or SystemVerilog**. Figure 4- 1 shows a simplified microprocessor diagram having M0, M1, M2, and Cin inputs, one input SW1 and also clock input. The SW1 serves as an asynchronous reset input.

Your design should finally implement the following operation:

$$R2 = M0 + (\text{not } M1) + Cin$$

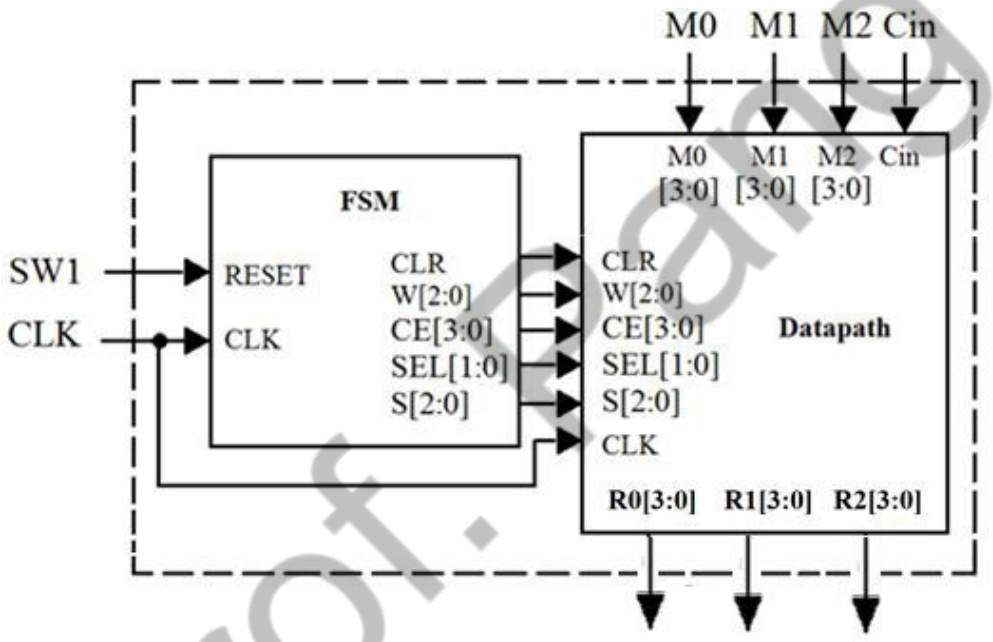


Figure 4-1. Simplified microprocessor block diagram

Part 1. Microprocessor Data Path Design

The detailed data path circuit is shown in Figure 4-2.

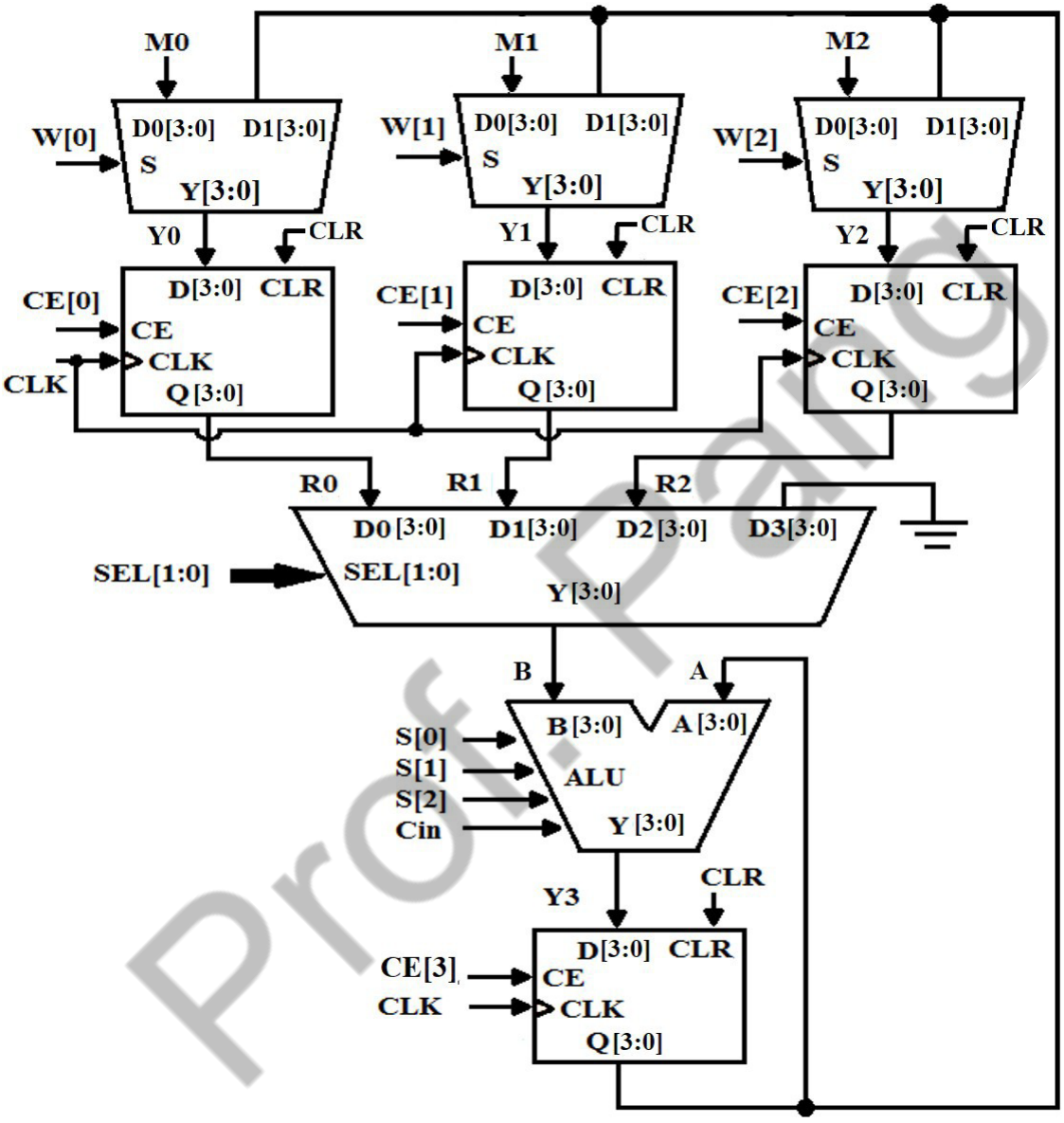


Figure 4-2. Simplified microprocessor data path circuit

The truth table of the ALU unit inside the data path circuit is shown in Table 4-1.

Table 4-1. ALU truth table

S[2]	S[1]	S[0]	ALU Output F
0	0	0	F=A+B+Cin
0	0	1	F=A+B'+Cin
0	1	0	F= B
0	1	1	F=A
1	0	0	F= A AND B
1	0	1	F= A OR B
1	1	0	F= A'
1	1	1	F = A XOR B

Use a structural hierarchical design method to implement the data path circuit. Design and simulate each individual sub-design. Wire each sub-design together to implement your final data path circuit.

For this simplified design, all inputs and outputs are only required to be 4 bits, carry output signal won't be used. For example, A=$(0110)_2$, B=$(1100)_2$, Cin =1, then A+B+ Cin =$(0011)_2$.

Demo Requirement:

Show your testbench simulation of the top-level microprocessor data path design to your lab instructor.

Part 2. Microprocessor Control Path Design

Microprocessor Control Path Design

Draw your finite state machine diagram for the "FSM" unit, which is used to implement the control path for the simplified microprocessor design shown in Figure 4-1. The control path block diagram is shown in Figure 4-3.

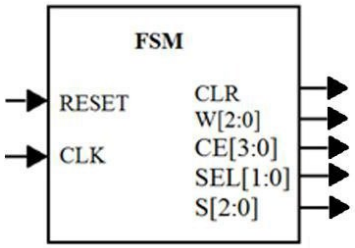


Figure 4-3. Simplified microprocessor control path block diagram

R0 and R1 are used to store operands M0 and M1 values.
R2 is used to store the final microprocessor operation result value, which is equal to:

M0 + (not M1) + Cin

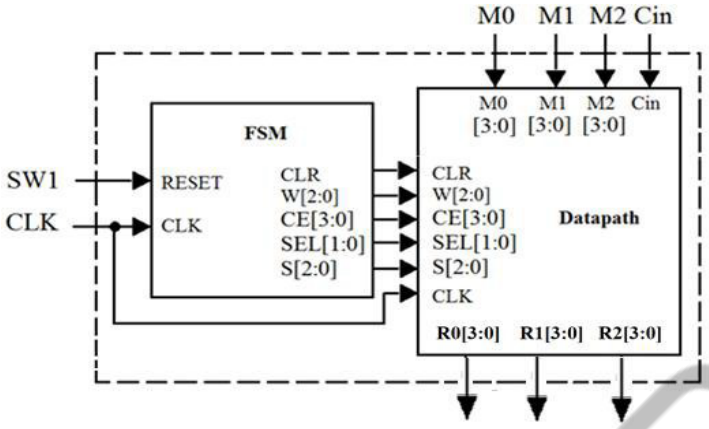
Demo Requirement:

Show your testbench simulation of the microprocessor control path design to your lab instructor.

Part 3. Microprocessor Design

Final 4-bit Microprocessor Design

This part is to complete the design shown in Figure 4-1 for the simplified 4-bit microprocessor.



Your microprocessor design should finally implement the following operation:

$$R2 = M0 + (\text{not } M1) + Cin$$

Demo Requirement:

Demo the final design on the FPGA board to your lab instructor.