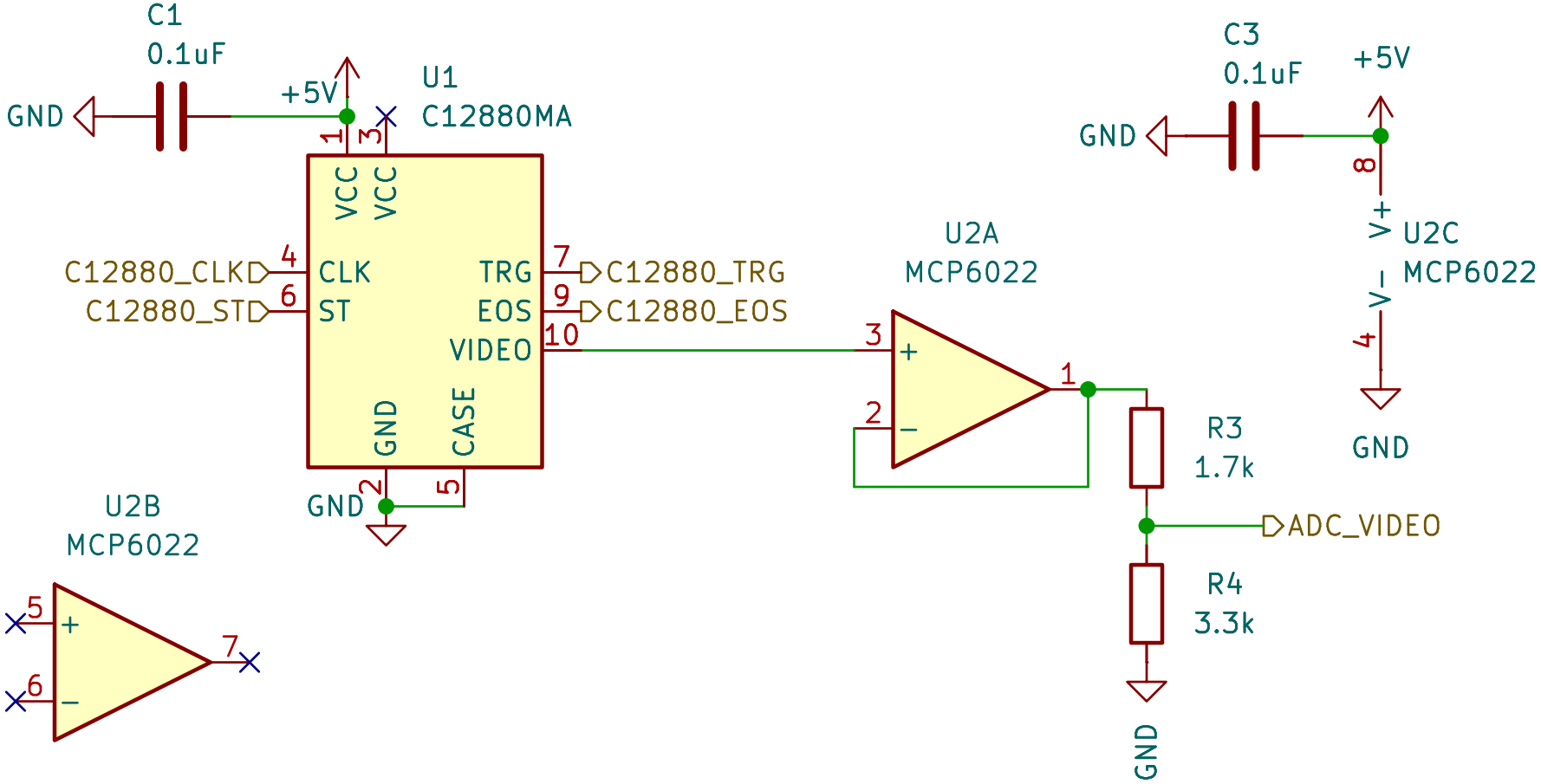

DESIGN RATIONALE:
C12880MA 5V digital outputs (TRG/EOS) connect directly to 5V-tolerant MCU pins.
A divider is avoided on the high-speed TRG signal to maintain edge integrity.
The 5V analog VIDEO output is buffered by U2A and scaled down by R3/R4 to fit the MCU's 3.3V ADC input range.