# EC601

# Project #1 Literature and Product Review

## -- Photonics chip for machine learning

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## Problem statement:

Machine learning is a key area in Artificial Intelligence, which uses large sets of data and algorithms to make predictions or decisions. Machine learning/deep learning tools such as Convolutional Neural Network requires an extremely high computing power of hardware. Now there are more and more transistors being put in a chip, with the integrated circuits' manufacture process reaching to 5nm below. When transistors are made even smaller than 2nm, it will demand much more precise manufacturing techniques and negative physical effects (heat & tunnelling) will occur. As a result, electronic chip will possibly have its computing limit in the near future. Meanwhile, all kinds of applications, for example, Internet of Things, automatic drive and computer vision, have higher and higher requirements of computing power. Therefore, researchers turn to use photons to deliver information in the circuits, which will be faster and more stable. Photonics chip has now been built to support machine learning, partly based on the fact that capacity of an optical fiber is 1,000 times that of an electrical wire, and that the signal loss in fiber optics is about 1,000 times lower than electrical wires [1].

Researchers around the world has develop several benign silicon photonic technologies. At present, chip-level devices that have been matured based on silicon photonic processes mainly include optical waveguides, multiplexer devices, external modulation devices, APD receivers, etc. [2]. Several new kits have also been implemented for layout, design, verification, simulation for Photonics chips. For example, SiEPIC provides solutions to build a photonics chip for machine learning. Synopsys also provides photonics solutions for photonics integrated circuit (PIC). With a combination between photons and CMOS logical circuit, power and cost of chip will be continuously optimized.

## Application:

Different from electronics chip, photonics chip processes optical signals using optical waveguides, beam couplers, electro-optic modulators, photodetectors and lasers. With the advantage on low power, low cost and high speed, photonics chip can be implemented in plenty of front AI applications as below:

Ultrafast artificial neural networks for deep learning, which helps greatly on medical diagnosis, 6G communication, automatic driving, pattern cognition and so on.

Neuromorphic computing, matching hardware to algorithms will potentially lead to faster and more energy-efficient information processing [3]. As a result, photonics chip is well suited to data centers.

## My Focus:

Silicon photonics circuits design solutions

To be specific, this area involves physical theory of design and software tools for PIC design, simulation, verification, test and final tapeout. It follows a similar overall process with digital/analog IC design.

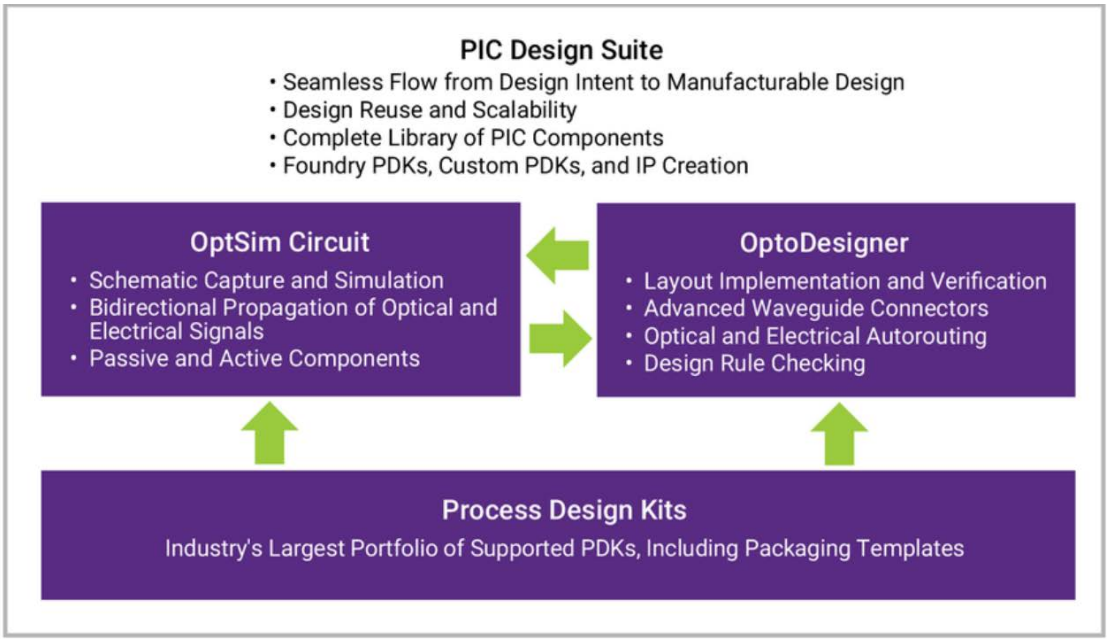


Figure 1. Synopsys PIC Design Suite

Source: https://www.synopsys.com/photonic-solutions/pic-design-suite.html

## Literature Review:

1. Photonic Integrated Circuits from Small Batches to Volumes: Standardization and Automation of Test [4]

Scaling up Photonic Integrated Circuits from prototyping and small batch fabrication to volume production requires revision and improvements of many processes across the full manufacturing chain. These efforts include automation and standardization of electronic-photonic test processes, tools and methods.

Standardization of PIC layout enables efficient utilization of automated, modular tools and equipment, allows to confine the space of possible design parameters and paves the way towards design for test (DFT), design for packaging and makes generic test services feasible.

A fully automated, modular test system (Test-Line TL-500) is currently being installed at TU/e laboratory. The modular architecture enables accommodation of the standard PIC layouts and deployment of the open standards test framework. These provide support to the DFT and user defined test sequences that can be used for generic test services.

2. Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip [5]

It introduces photonics into bulk silicon complementary metal–oxide–semiconductor (CMOS) chips using a layer of polycrystalline silicon deposited on silicon oxide (glass) islands fabricated alongside transistors. This single deposited layer is used to realize optical waveguides and resonators, high-speed optical modulators and sensitive avalanche photodetectors. The photonic platform is integrated with a 65-nanometre-transistor bulk CMOS process technology inside a 300-millimetre-diameter-wafer microelectronics foundry. Then integrated high-speed optical transceivers are implemented in this platform that operate at ten gigabits per second, composed of millions of transistors, and arrayed on a single optical bus for wavelength division multiplexing, to address the demand for high-bandwidth optical interconnects in data centres and high-performance computing. By decoupling the formation of photonic devices from that of transistors, this integration approach can achieve many of the goals of multi-chip solutions, but with the optimal performance, complexity and scalability of ‘systems on a chip’.

3. Silicon Photonics Circuit Design: Methods, Tools and Challenges [6]

As circuit-oriented (and EDA-based) design flows are gradually being adopted, a number of challenges are becoming clearer. These are now, or will soon be, limiting the scaling of the complexity of silicon photonic circuits, both in the front-end and in the back-end of the design flow. The current flows are also limited in applicability: as the PIC market today is largely driven by communications, the emerging design and simulations tools are primarily supporting these applications. But there are numerous other applications in sensing, signal processing, spectrometry, and quantum information processing that cannot be captured with the design paradigms of transceivers or switch fabrics. Both for the scaling of complex circuits and new applications, some of the key challenges in the realm of design automation are identified:

Capturing the effects of variability to enable accurate yield prediction. Circuit and signal representation for photonic circuits to accurately capture wavelength dependence, nonlinear effects, etc. Building reliable compact models that can also be qualified against fabricated structures. Photonic-Electronic co-design, similar to analog-mixed signal approaches in electronics. Photonic Routing.

4. DSENT - A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling [7]

DSENT is written in C++ and utilizes the object-oriented approach and inheritance for hierarchical modeling. The DSENT framework can be separated into three distinct parts: user-defined models, support models, and tools. To ease development of user-defined models, much of the inherent modeling complexity is off-loaded onto support models and tools. As such, most user-defined models involve just simple instantiation of support models, relying on tools to perform analysis and optimization. Like an actual electrical chip design, DSENT models can leverage instancing and multiplicity to

reduce the amount of repetitive work and speed up model evaluation.

5. The AIM Photonics MPW: A Highly Accessible Cutting-Edge Technology for Rapid Prototyping of Photonic Integrated Circuits [8]
The AIM Photonics MPW program fabricated at the SUNY Polytechnic Institute (SUNY-Poly) is enabled by an extensive process design kit (PDK), produced by Analog Photonics (Boston, MA). Analog Photonics (AP) draws upon years of experience with the SUNY-Poly fab and silicon photonics technology to provide devices that have been verified on wafers. The information provided by SUNY-Poly includes design guide, technology file, and design rule check (DRC) deck which will provide sufficient information about the foundry process to design, layout, and tapeout. The design guide includes mask layer names, types (negative or positive), opacities, thicknesses, purposes, stress gradients, and tolerances. The technology file provides the layer map that transfers the design intent layers to fabrication ready layer numbers and shows interactions between these layers. This layermap is used to convert the designs to a graphic database system (GDSII) or OASIS file formats that are recognized by the design rule check (DRC) deck. After passing the DRC, designs will be ready to submit to SUNY-Poly for mask generation.

## Open Source:

Synopsys' PIC Design Suite – photonic integrated circuit design software that includes the OptSim Circuit and OptoDesigner tools – offers a seamless PIC design flow from concept to manufacturable design, as well as access to a single, world-class support channel.
Silicon Photonics Design Software - OptoCompiler | Synopsys

SiEPIC-Tools - for silicon photonics layout, design, verification and circuit simulation
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Now it has 124 releases, with the latest release as v0.3.80.
SiEPIC/SiEPIC-Tools: Package for KLayout to add integrated optics / silicon photonics functionality (waveguides, netlist extraction, circuit simulations, etc) (github.com)

Klayout - KLayout chip mask layout viewing, editing and more.
Copyright (C) 2007 Free Software Foundation, Inc. <http://fsf.org/>
Now it has 33 releases, with the latest release as 0.27.3.
KLayout/klayout: KLayout Main Sources (github.com)

Simphony - a simulator for photonic circuits, is a fundamental package for designing and simulating photonic integrated circuits with Python.
MIT License

Copyright (c) 2019-2020 Simphony Project Contributors and others (see AUTHORS.txt)
Now it has 3 releases, with the latest release as v0.4.0.
BYUCamachoLab/simphony: A simulator for photonic integrated circuits. (github.com)

Noxim - the Network-on-Chip Simulator developed at the University of Catania (Italy). V. Catania, A. Mineo, S. Monteleone, M. Palesi and D. Patti, "Improving the energy efficiency of wireless Network on Chip architectures through online selective buffers and receivers shutdown," 2016 13th IEEE Annual Consumer Communications & Networking Conference (CCNC), Las Vegas, NV, 2016, pp. 668-673, doi: 10.1109/CCNC.2016.7444860.
Now it has 9 releases, with the latest release as 2020.02.21
davidepatti/noxim: Network on Chip Simulator (github.com)

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https://gigalight.medium.com/the-challenges-and-opportunities-of-silicon-photonics-in-the-application-of-optical-modules-9b24046a3ce7

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