2024 超大型積體電路電腦輔助設計概論

2024 Introduction to VLSI CAD

Lab 9

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※作業要求的圖請使用**電腦截圖程式**截取，請勿用手機拍照的方式繳交

※Report 檔請以 pdf 的格式繳交

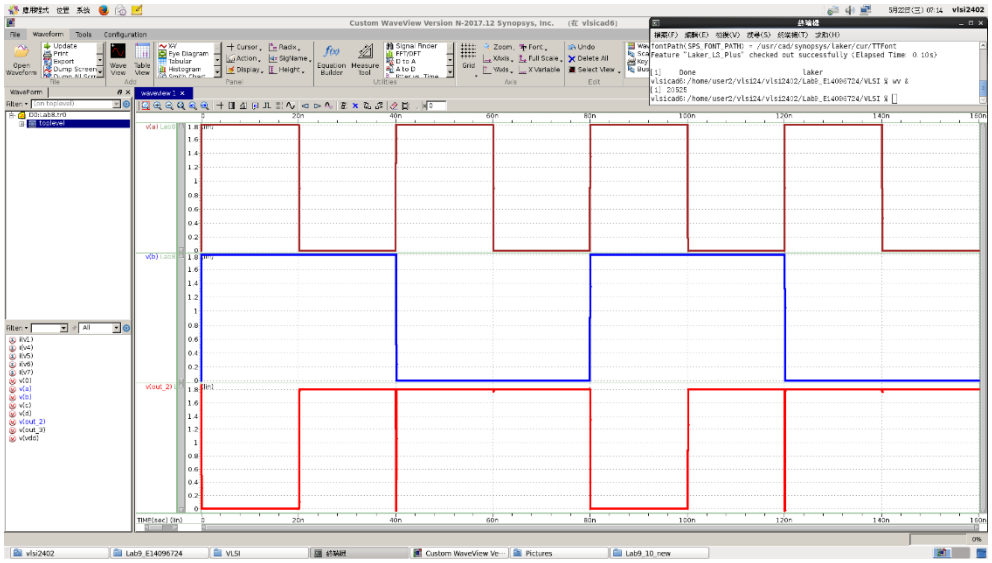
A. NAND

1. Presim

i. 請截取 terminal 顯示 job concluded 的圖

```
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab8_E14096724 % hspice testbench.sp -o Lab
8.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.sp' -o Lab
8.lis

>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab8_E14096724 %
```

ii. 請截取 WaveView 中的波形

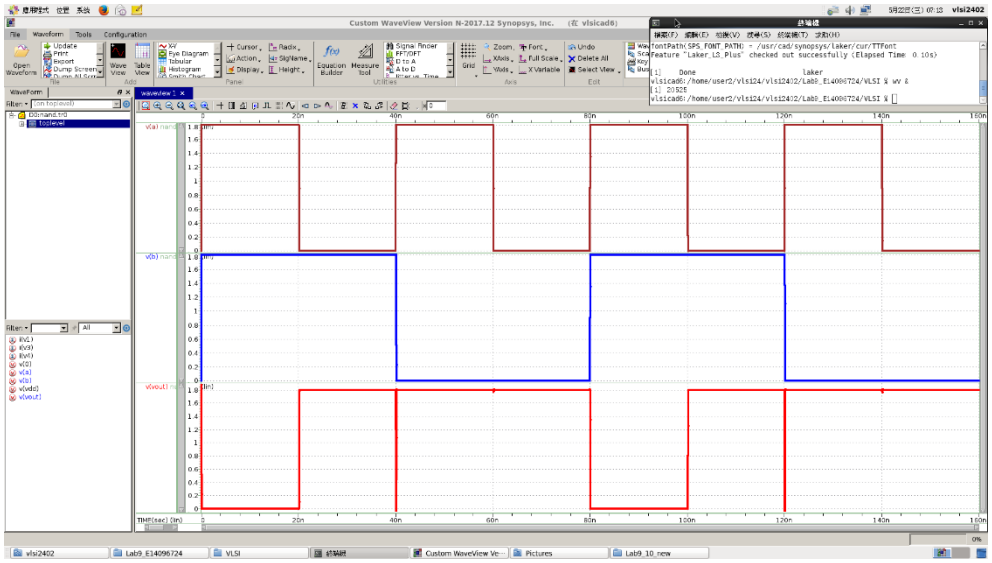


2. Post-sim

i. 請截取 terminal 顯示 job concluded 的圖

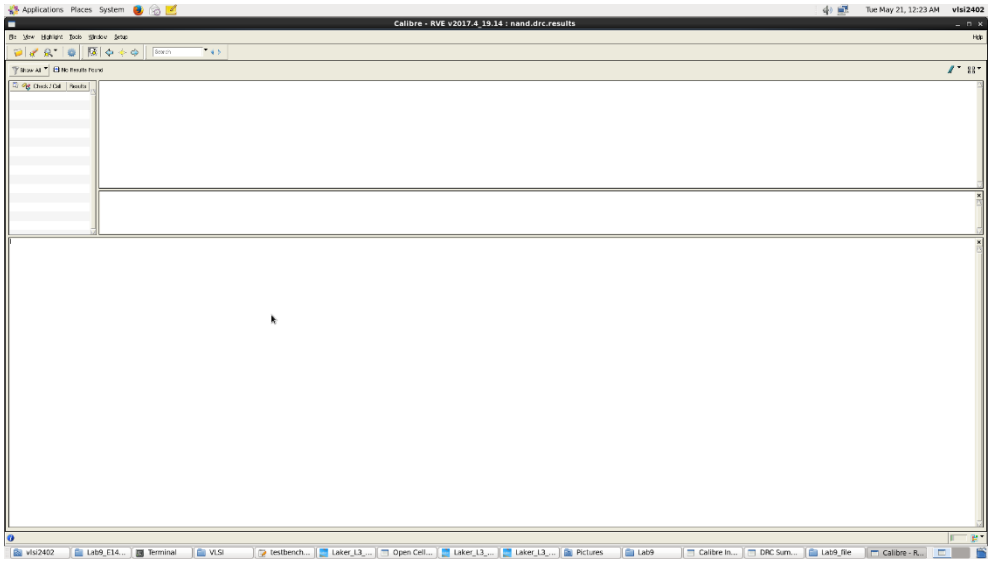
```
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab9_E14096724/VLSI % hspice nand_tb.sp -o
nand.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'nand_tb.sp' -o nand.
lis
Warning(s) associated with encrypted block(s) were suppressed due to encrypted c
ontent.

>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab9_E14096724/VLSI % wv &
```

ii. 請截取 WaveView 中的波形

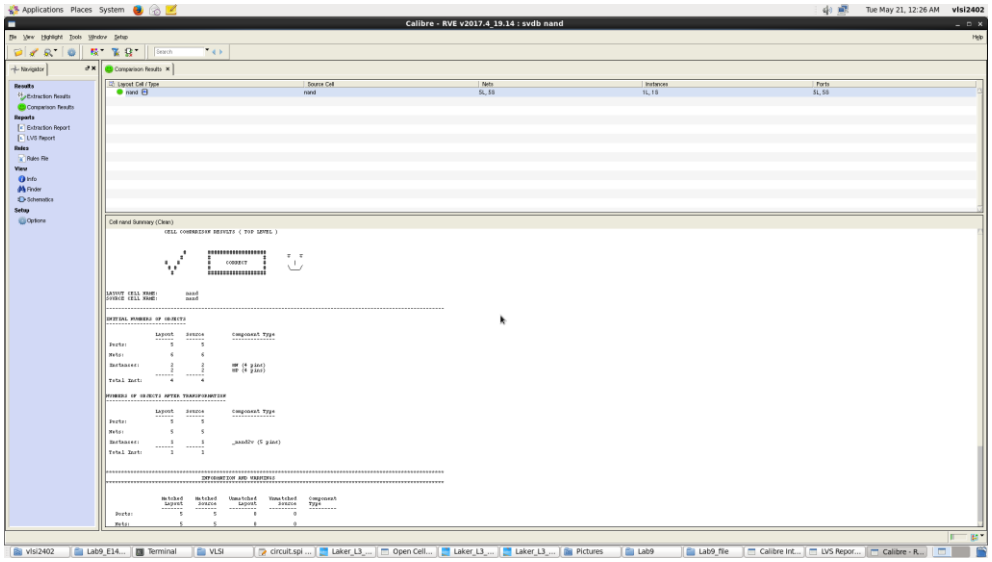


iii. DRC/LVS 結果

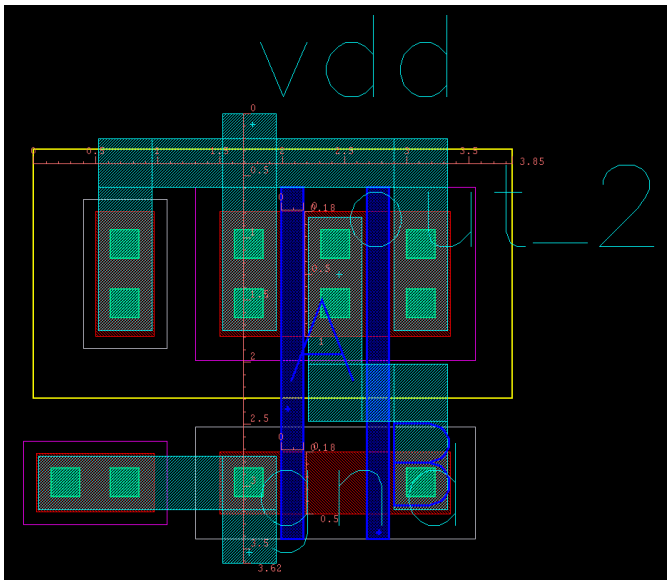
DRC:



LVS:



iv. Layout 截圖



長:3.62um　　寬:3.85um　　面積:13.937um^2

3. 嘗試簡單說明 Presim 與 Post-sim 結果比較

Presim 中忽略寄生效應較為理想，所以在電壓改變時 overshoot 比較小也比較穩定；但是 Post-sim 畫出的 layout 有考慮寄生效應，比較接近真實情況所以會有更大的 overshoot 也比較不穩定。

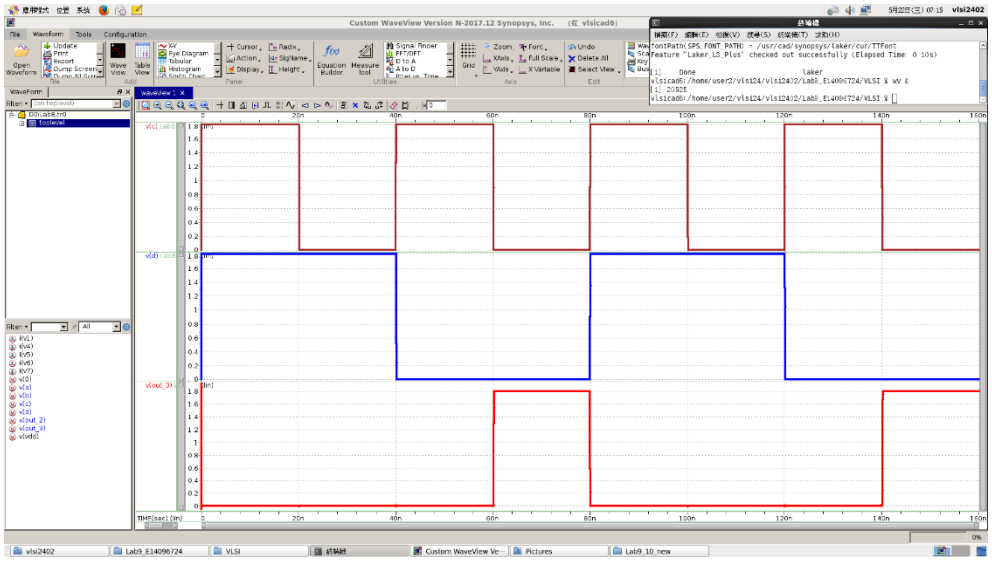
B. NOR

1. Presim

i. 請截取 terminal 顯示 job concluded 的圖

```
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab8_E14096724 % hspice testbench.sp -o Lab
8.lis
Using:  /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice  'testbench.sp'  -o Lab
8.lis

>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab8_E14096724 %
```

ii. 請截取 WaveView 中的波形

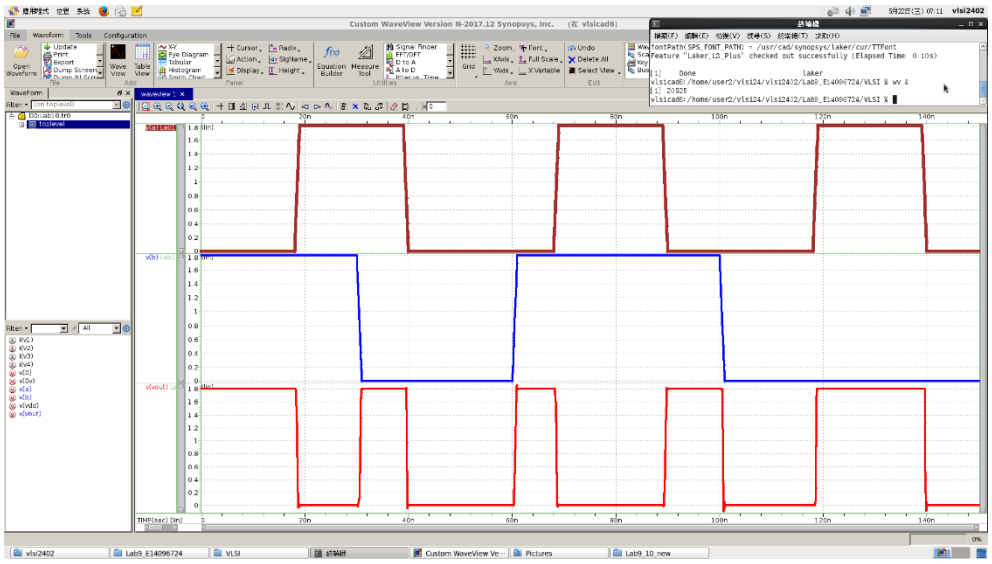


2. Post-sim

i. 請截取 terminal 顯示 job concluded 的圖

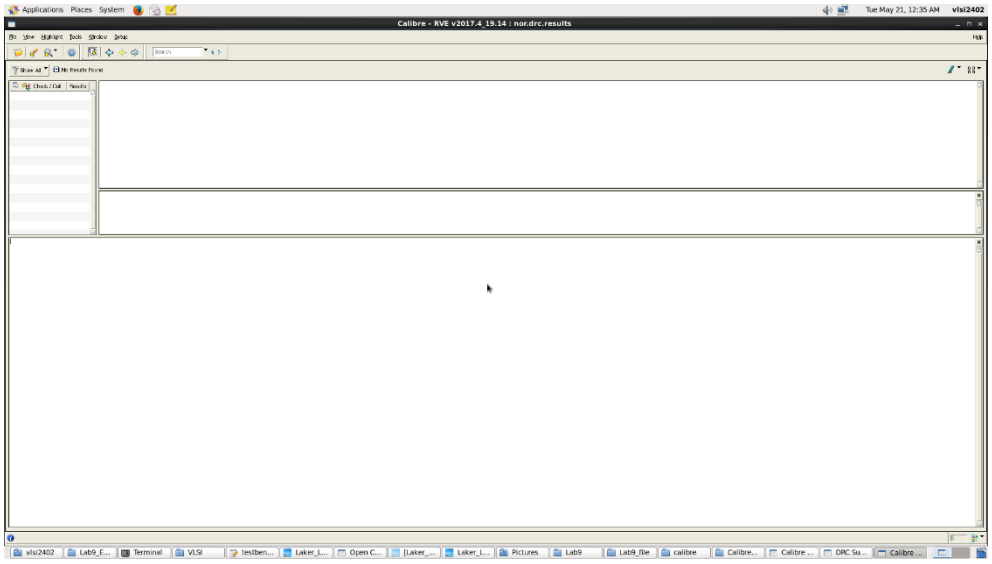
```
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab9_E14096724/VLSI % hspice nor_tb.sp -o nor.lis
Using:  /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice  'nor_tb.sp'  -o nor.lis
Warning(s) associated with encrypted block(s) were suppressed due to encrypted content.

>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2402/Lab9_E14096724/VLSI %
```

ii. 請截取 WaveView 中的波形

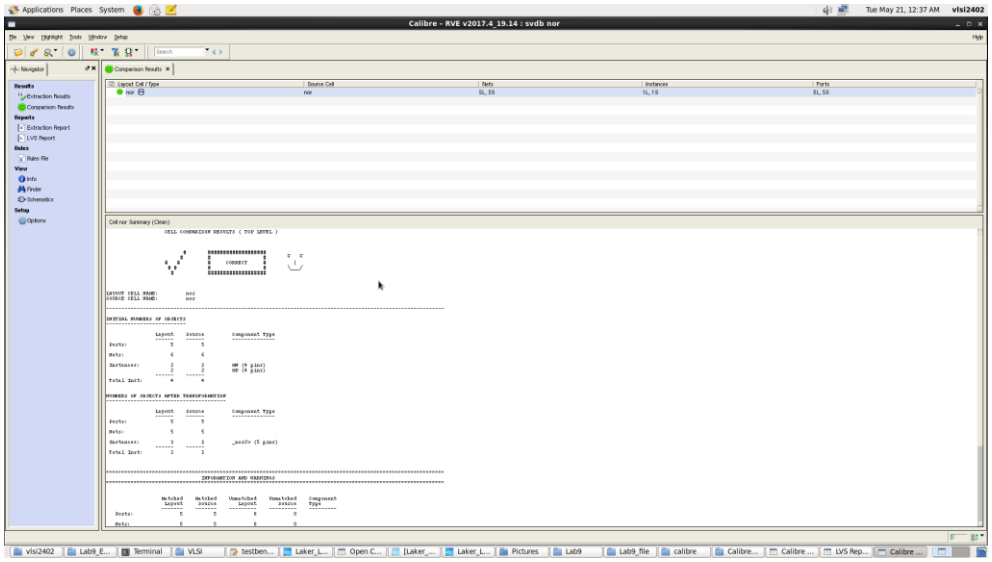


iii. DRC/LVS 結果

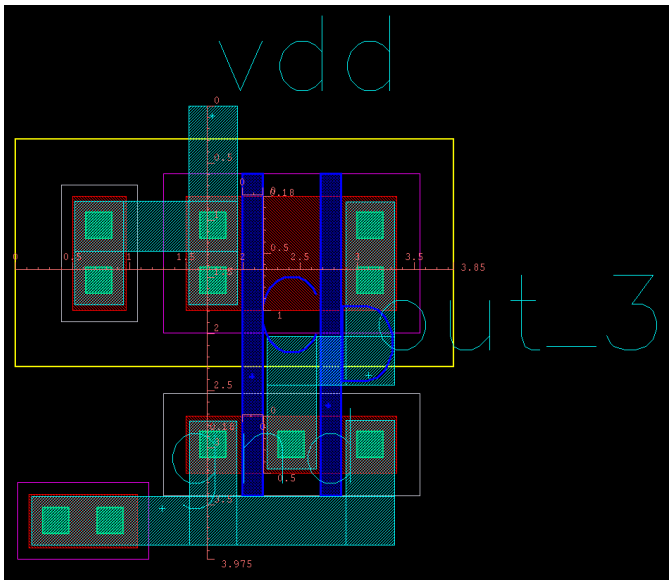
DRC:



LVS:



iv. Layout 截圖



長:3.975um　　寬:3.85um　　面積:15.30375um^2

3. 嘗試簡單說明 Presim 與 Post-sim 結果比較

Presim 中忽略寄生效應較為理想，所以在電壓改變時 overshoot 比較小也比較穩定；但是 Post-sim 畫出的 layout 有考慮寄生效應，比較接近真實情況所以會有更大的 overshoot 也比較不穩定。

C. 心得討論

這次的 Lab 是我第一次畫 layout，在過程中我深刻體會到一些在畫 layout 的規則，在畫完之後還要再檢查哪裡有沒有不符合規則的，在使用一些工具來幫我驗證，也了解了電路設計從理論和實際的差異，透過進行 Presim 和 Post-sim 的波形比較，我學到了許多關於電路設計和驗證的知識，並且對 layout 有了更深入的理解。