

## Homework #6

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### (1) The test program and its explanation

我在 instruction set 中加入的兩個新的 instruction 是 ADDONE 和 ADDTWO，ADDONE 是將 REG 或是 IMM 的數加 1 存入到另一個 REG 中，ADDTWO 是將 REG 或是 IMM 的數加 2 存入到另一個 REG。

CPU 的 test program 有兩的檔案，sisc.prog 有 20 行程式會被儲存在 MEM 中的 InstructionMEM[0] ~ InstructionMEM[10]，另外還有 data.prog 有 2 行程式會被儲存在 MEM 中的 DataMEM[0] ~ DataMEM[10]，以下是每一行程式的解釋：

sisc.prog：

1. 讀取 0 到 R1
2. 讀取 NMBR ( DataMEM[0] ) 的 5555aaaa 到 R0
3. 有標籤 START，當滿足條件是否為偶數時會跳至標籤 L1
4. 將 R1 加 1 存至 R1
5. 有標籤 L1，將 R0 向右 shift 1 bit 存至 R0
6. 當滿足條件是否為零時會跳至標籤 L2
7. 跳至標籤 START
8. 有標籤 L2，儲存 R1 至 RSLT ( DataMEM[1] )
9. 將 R1 乘 2 存至 R1
10. 儲存儲存 R1 至 DataMEM[2]
11. 將 R1 取反存至 R1
12. 儲存儲存 R1 至 DataMEM[3]
13. 將 R1 向右旋轉 1 bit 存至 R1
14. 儲存儲存 R1 至 DataMEM[4]
15. 將 4 加 1 存至 R1
16. 儲存儲存 R1 至 DataMEM[5]
17. 將 R1 加 2 存至 R1
18. 儲存儲存 R1 至 DataMEM[6]
19. NOP 無操作
20. 停止程式

data.prog：

1. 儲存 NMBR:5555aaaa
2. RSLT 儲存結果的位置

```

≡ sisc.prog
1  0010_1000_0000_0000_0000_0000_0000_0001 // LD R1,#0
2  0010_0000_0000_0000_0000_0000_0000_0000 // LD R0,NMBR
3  0001_0010_0000_0000_0000_0000_0000_0100 // START:BRA L1,CCE
4  0100_1000_0000_0000_0001_0000_0000_0001 // ADD R1,#1
5  0111_1000_0000_0000_0001_0000_0000_0000 // L1:SHF R0,#1
6  0001_0100_0000_0000_0000_0000_0000_0111 // BRA L2,ZERO
7  0001_0000_0000_0000_0000_0000_0000_0010 // BRA START,ALW
8  0011_0000_0000_0000_0001_0000_0000_0001 // L2:STR RSLT, R1
9  0101_1000_0000_0000_0010_0000_0000_0001 // MUL R1,#2
10 0011_0000_0000_0000_0001_0000_0000_0010 // STR 2, R1
11 0110_0000_0000_0000_0001_0000_0000_0001 // CMP R1,R1
12 0011_0000_0000_0000_0001_0000_0000_0011 // STR 3, R1
13 1000_1000_0000_0000_0001_0000_0000_0001 // ROT R1,#1
14 0011_0000_0000_0000_0001_0000_0000_0100 // STR 4, R1
15 1001_1000_0000_0000_0100_0000_0000_0001 // ADDONE R1,#4
16 0011_0000_0000_0000_0001_0000_0000_0101 // STR 5, R1
17 1010_0000_0000_0000_0001_0000_0000_0001 // ADDTWO R1,R1
18 0011_0000_0000_0000_0001_0000_0000_0110 // STR 6, R1
19 0000_0000_0000_0000_0000_0000_0000_0000 // NOP
20 1011_1111_1111_1111_1111_1111_1111_1111 // HLT

```

Fig. 1. sisc.prog 中的程式

```

≡ data.prog
1  0101_0101_0101_0101_1010_1010_1010_1010 // NMBR:5555aaaa
2  0000_0000_0000_0000_0000_0000_0000_0000 // RSLT:00000000

```

Fig. 2. data.prog 中先儲存的資料

## (2) Simulation results and explanation

第 1 行程式先讀取 0 到 R1，第 2 行程式讀取 NMBR ( DataMEM[0] )就是 5555aaaa 到 R0，第 3 行有標籤 START，在滿足條件是否為偶數時會跳至有標籤 L1 的第 5 行；在不滿足條件是否為偶數時會繼續執行第 4 行，第 4 行是將 R1 加 1，接著繼續執行第 5 行。第 5 行有標籤 L1 是將 R0 向右 shift 1 bit，執行第 6 行時，在滿足條件是否為零時會跳至有標籤 L2 的第 8 行；在不滿足條件是否為零時會繼續執行第 7 行，第 7 行是跳至有標籤 START 的第 3 行，接著繼續重新執行第 3 行，繼續執行時會執行到第 4 行是將 R1 加 1 和第 5 行將 R0 向右 shift 1 bit 直到滿足第 6 行的條件是否為零時才會跳至有標籤 L2 的第 8 行。第 8 行有標籤 L2 是儲存 R1 至 RSLT ( DataMEM[1] )。第 9 行是將 R1 乘 2 存至 R1，第 10 行是儲存儲存 R1 至 DataMEM[2]。第 11 行是將 R1 取反存至 R1，第 12 行是儲存儲存 R1 至 DataMEM[3]。第 13 行是將 R1 向右旋轉 1 bit 存至 R1，第 14 行是儲存儲存 R1 至 DataMEM[4]。第 15 行是將 4 加 1 存至 R1，第 16 行是儲存儲存 R1 至 DataMEM[5]。第 17 行是將 R1 加 2 存至 R1，第 18 行是儲存儲存 R1 至 DataMEM[6]。第 19 行是 NOP 無操作，第 20 行是停止程式

```
DataMEM[0]=01010101010101011010101010101010
DataMEM[1]=0000000000000000000000000000000010001
DataMEM[2]=00000000000000000000000000000000100010
DataMEM[3]=1111111111111111111111111111111011101
DataMEM[4]=111111111111111111111111111111101110
DataMEM[5]=000000000000000000000000000000000000101
DataMEM[6]=000000000000000000000000000000000000111
Halt ...
```

Fig. 3. test program 的模擬結果

### (3) Synthesis results and explanation

Domain: LINT (122)		
Category: CODINGSTYLE (79)		
Tag: AWR_MS_ORIG (1)		
"Inconsistent ordering of bits in range declarations in design-unit CPU - should be all Descending ranges"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	25
Tag: OPT_NR_READ (2)		
"Output port 'pc' is read in the design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	82
"Output port 'pc' is read in the design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	93
Tag: ASO_NR_ORF (1)		
"Potential overflow in assignment in design-unit/block 'CPU'. LHS 'next_pc' (unsigned) is of 12 bit(s), RHS '(pc + 12'd1)' ...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	93
"Potential overflow in assignment in design-unit/block 'CPU'. LHS 'result' (unsigned) is of 32 bit(s), RHS 'src1 * src2' (unsi...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	173
"Potential overflow in assignment in design-unit/block 'CPU'. LHS 'src2' (unsigned) is of 32 bit(s), RHS 'src2 << WDT' (un...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	234
Tag: MOD_NR_ESTIM (3)		
"Design-unit 'CPU' contains an empty statement"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	99
"Design-unit 'CPU' contains an empty statement"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	100
"Design-unit 'CPU' contains an empty statement"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	295
Tag: ASO_MS_BRD (2)		
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	103
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	108
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'write_data' (u...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	121
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	150
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	154
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	169
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	173
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	188
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	189
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	204
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	208
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	209
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	215
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	228
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	233
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	237
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	242
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	246
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	262
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	263
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'src1' (unsigne...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	278
"Unequal length operands in assignment in design-unit/block 'CPU'. Length of RHS is less than LHS. LHS 'result' (unsig...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	279
Tag: TOP_NR_LSZ (20)		
"Reduction 'xor' operation performed on '32' bit expression 'imp' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	114
"Reduction 'or' operation performed on '32' bit expression 'tmp' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	115
"Reduction 'or' operation performed on '32' bit expression 'tmp' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	134
"Reduction 'xor' operation performed on '32' bit expression 'tmp' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	135
"Reduction 'xor' operation performed on '32' bit expression 'tmp' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	136
"Reduction 'xor' operation performed on '32' bit expression 'tmp' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	144
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	163
"Reduction 'or' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	164
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	182
"Reduction 'or' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	183
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	188
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	189
"Reduction 'or' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	218
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	219
"Reduction 'or' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	237
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	257
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	272
"Reduction 'or' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	273
"Reduction 'xor' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	288
"Reduction 'or' operation performed on '32' bit expression 'result' in design-unit 'CPU'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	289
Tag: OPR_NR_LCMP (10)		
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	149
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	151
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	155
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	164
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	170
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	174
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	187
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	190
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	218
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	219
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	223
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	225
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	231
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	261
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	264
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	273
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	280
"Unequal length operands in equality operator encountered in design-unit/block CPU. LHS operand is 1 bits, RHS oper...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	283
Tag: OPR_NR_UREL (2)		
"Unequal length operands in relational operator (padding produces incorrect result) in design-unit/block CPU - LHS o...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	228
"Unequal length operands in relational operator (padding produces incorrect result) in design-unit/block CPU - LHS o...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	243
Tag: OPR_NR_TERM (1)		
"Unequal length operand in ternary operator in design-unit/block CPU. First operand 'src1' is 32 bits, Second operand ...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	229
Tag: VAR_NR_RDBA (2)		
"Variable 'src2', assigned using blocking assignment, is being read before getting assigned"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	234
"Variable 'src2', assigned using blocking assignment, is being read before getting assigned"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	243
Tag: OPR_NR_UOPR (2)		
"Unequal length operand in bit operator bit-wise inclusive or in design-unit/block CPU. LHS operand 'result' is 32 bits, ...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	235
"Unequal length operand in bit operator bit-wise inclusive or in design-unit/block CPU. LHS operand 'result' is 32 bits, ...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	244
Tag: CAS_NR_DEFX (1)		
"Signal 'x', used in case statement is not assigned to X in default case"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	98
Tag: IDX_NR_DTTY (1)		
"Variable 'x' used as index in expression 'RFILE'[11:0]' should be 2-state data type"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	303
Category: SIM_SYNTH (2)		
Tag: AWR_NR_UNIV (2)		
"Signal 'n23:12' appearing in the sensitivity list is not used in the 'always' block"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	82
"Signal 'n25:247' appearing in the sensitivity list is not used in the 'always' block"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	96
Category: SYNTHESIS (31)		
Tag: AWR_IC_SEN (16)		
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	111
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	126
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	140
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	149
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	152
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	168
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	171
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	187
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	203
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	206
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	223
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	226
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	261
"Sensitivity list of always block is incomplete in design-unit CPU, missing variable(s): RFILE"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	277
Tag: MOD_NR_ORG (1)		
Tag: IDX_NR_ORNG (14)		
"Variable index/range selection of 'n[11:0]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	11
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	121
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	140
"Variable index/range selection of 'n[11:0]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	149
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	156
"Variable index/range selection of 'n[11:0]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	17
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	18
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	19
"Variable index/range selection of 'n[11:0]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	201
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	221
"Variable index/range selection of 'n[11:0]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	226
"Variable index/range selection of 'n[23:12]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	277
Tag: LAT_NR_BLAS (1)		
"In design-unit CPU, latch is assigned by blocking assignments"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	96
Tag: IDX_NR_ORG (1)		
"Variable index/range selection in LHS of assignment of 'n[11:0]' is potentially outside the defined range"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	301
Tag: LAT_NR_MCB (1)		
"The latches 'x' in the always block are mixed with combinational logic"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	96
Category: STRUCTURAL (9)		
Tag: FLIP_NO_ASRP (2)		
"Flip-Rop 'RFILE' does not have any asynchronous set or reset"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	301
"Flip-Rop 'pc' does not have any asynchronous set or reset"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	73
Tag: REG_NO_LOAD (4)		
"Flip-Rop/latch 'dir' declared in design-unit 'CPU' does not have any load"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	30
"Flip-Rop/latch 'dir' declared in design-unit 'CPU' does not have any load"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	31
"Flip-Rop/latch 'result[2]' declared in design-unit 'CPU' does not have any load"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	27
"Flip-Rop/latch 'src1' declared in design-unit 'CPU' does not have any load"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	27
Tag: MOD_NR_ORG (1)		
"Input port 'sr' of top-level design-unit is not registered"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	20
Tag: LAT_IS_FLSE (1)		
"Latch 'src2' is feeding latch 'src2' having same enable 'tmp_116777'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	96
Tag: MOD_IS_SYNS (1)		
"The design-unit 'CPU' contains synchronous as well as asynchronous logic. Asynchronous logic is present at 'write_da...	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	23
Category: RACES (1)		
Tag: REG_NR_RWRNC (1)		
"A read/write race exists for signal: 'sr'"	/home/ncu_class/vsd2023/vsd202335/Homework#6/CPU.v	28

Fig. 4. Superlint result of the screenshot

timing report:

```
*****
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : CPU
Version: Q-2019.12
Date   : Mon Dec  4 09:35:48 2023
*****

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Startpoint: pc_reg[0] (rising edge-triggered flip-flop clocked by clk)
Endpoint: pc_reg[11] (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----
CPU                  tsmc18_wl10             slow

Point              Incr              Path
-----
clock clk (rise edge)                2.50              2.50
clock network delay (ideal)           0.00              2.50
pc_reg[0]/CK (DFFHQX1)                 0.00              2.50 r
pc_reg[0]/Q (DFFHQX1)                  0.54              3.04 r
add_93/A[0] (CPU_DW01_inc_1)           0.00              3.04 r
add_93/U1_1_1/CO (ADDHXL)               0.34              3.38 r
add_93/U1_1_2/CO (ADDHXL)               0.32              3.70 r
add_93/U1_1_3/CO (ADDHXL)               0.32              4.01 r
add_93/U1_1_4/CO (ADDHXL)               0.32              4.33 r
add_93/U1_1_5/CO (ADDHXL)               0.32              4.64 r
add_93/U1_1_6/CO (ADDHXL)               0.32              4.96 r
add_93/U1_1_7/CO (ADDHXL)               0.32              5.27 r
add_93/U1_1_8/CO (ADDHXL)               0.32              5.59 r
add_93/U1_1_9/CO (ADDHXL)               0.32              5.91 r
add_93/U1_1_10/CO (ADDHXL)              0.31              6.22 r
add_93/U2/Y (XOR2X1)                   0.30              6.52 f
add_93/SUM[11] (CPU_DW01_inc_1)         0.00              6.52 f
U2721/Y (OAI2BB2X1)                    0.30              6.81 f
pc_reg[11]/D (DFFHQX1)                  0.00              6.81 f
data arrival time                       6.81

clock clk (rise edge)                7.50              7.50
clock network delay (ideal)           0.00              7.50
pc_reg[11]/CK (DFFHQX1)                 0.00              7.50 r
library setup time                     -0.37              7.13
data required time                      7.13

-----
data required time                      7.13
data arrival time                      -6.81
-----
slack (MET)                            0.32

***** End Of Report *****
```

Fig. 5. timing report 的截圖

## area report:

```
*****
Report : area
Design : CPU
Version: Q-2019.12
Date   : Mon Dec  4 09:36:07 2023
*****

Library(s) Used:

slow (File: /home/ncku_class/vsd2023/vsd202300/Desktop/vsd2023/synopsys/slow.db)

Number of ports:          642
Number of nets:           5136
Number of cells:          4376
Number of combinational cells: 3725
Number of sequential cells:  638
Number of macros/black boxes:  0
Number of buf/inv:        527
Number of references:      48

Combinational area:       78453.144543
Buf/Inv area:             3572.553646
Noncombinational area:    43981.661987
Macro/Black Box area:     0.000000
Net Interconnect area:    594302.986176

Total cell area:          122434.806530
Total area:               716737.792706

**** End Of Report ****
```

Fig. 6. area report 的截圖

## power report:

```
*****
Report : power
        -analysis_effort low
Design : CPU
Version: Q-2019.12
Date   : Mon Dec  4 09:36:23 2023
*****

Library(s) Used:

slow (File: /home/ncku_class/vsd2023/vsd202300/Desktop/vsd2023/synopsys/slow.db)

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design      Wire Load Model      Library
-----
CPU          tsmc18_wl10         slow

Global Operating Voltage = 1.62
Power-specific unit information :
  Voltage Units = 1V
  Capacitance Units = 1.000000pf
  Time Units = 1ns
  Dynamic Power Units = 1mW (derived from V,C,T units)
  Leakage Power Units = 1pW

Cell Internal Power = 7.1853 mW (82%)
Net Switching Power = 1.5498 mW (18%)
-----
Total Dynamic Power = 8.7351 mW (100%)
Cell Leakage Power  = 4.2874 uW

-

Power Group      Internal      Switching      Leakage      Total
                  Power        Power          Power        Power  ( % ) Attrs
-----
io_pad           0.0000         0.0000         0.0000         0.0000 ( 0.00%)
memory           0.0000         0.0000         0.0000         0.0000 ( 0.00%)
black_box        0.0000         0.0000         0.0000         0.0000 ( 0.00%)
clock_network    0.0000         0.0000         0.0000         0.0000 ( 0.00%)
register         6.4734         8.7719e-03     9.5083e+05     6.4831 ( 74.18%)
sequential       0.1286         0.1172         8.7785e+04     0.2458 ( 2.81%)
combinational     0.5833         1.4239         3.2488e+06     2.0105 ( 23.00%)
-----
Total            7.1853 mW      1.5498 mW      4.2874e+06 pW  8.7394 mW

**** End Of Report ****
```

Fig. 7. power report 的截圖