Revision History

V1.0 Initial Released

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Title: E8_II_TQIMX6Q		
Size: A	Document Number: <Doc>	Rev: 1
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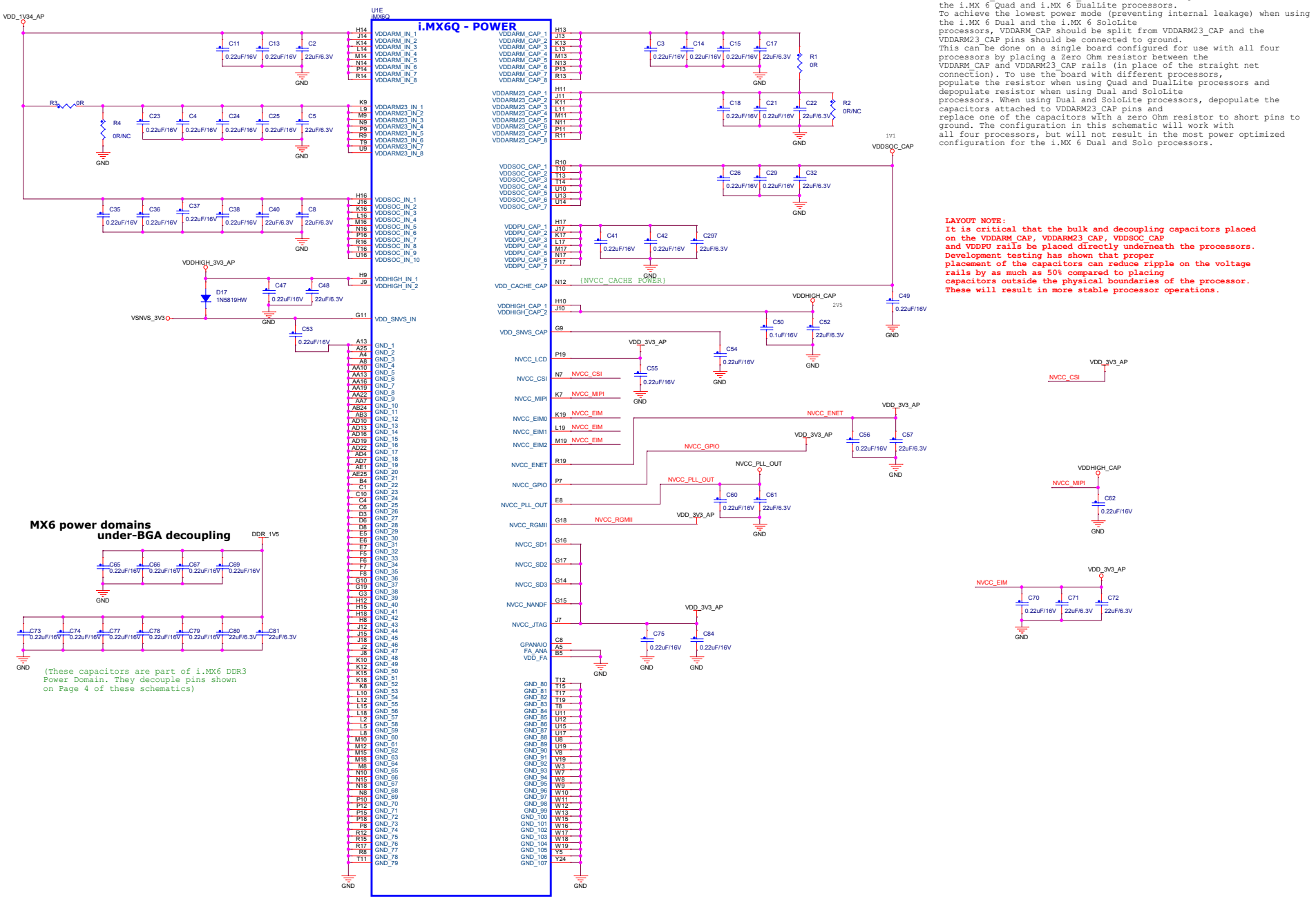
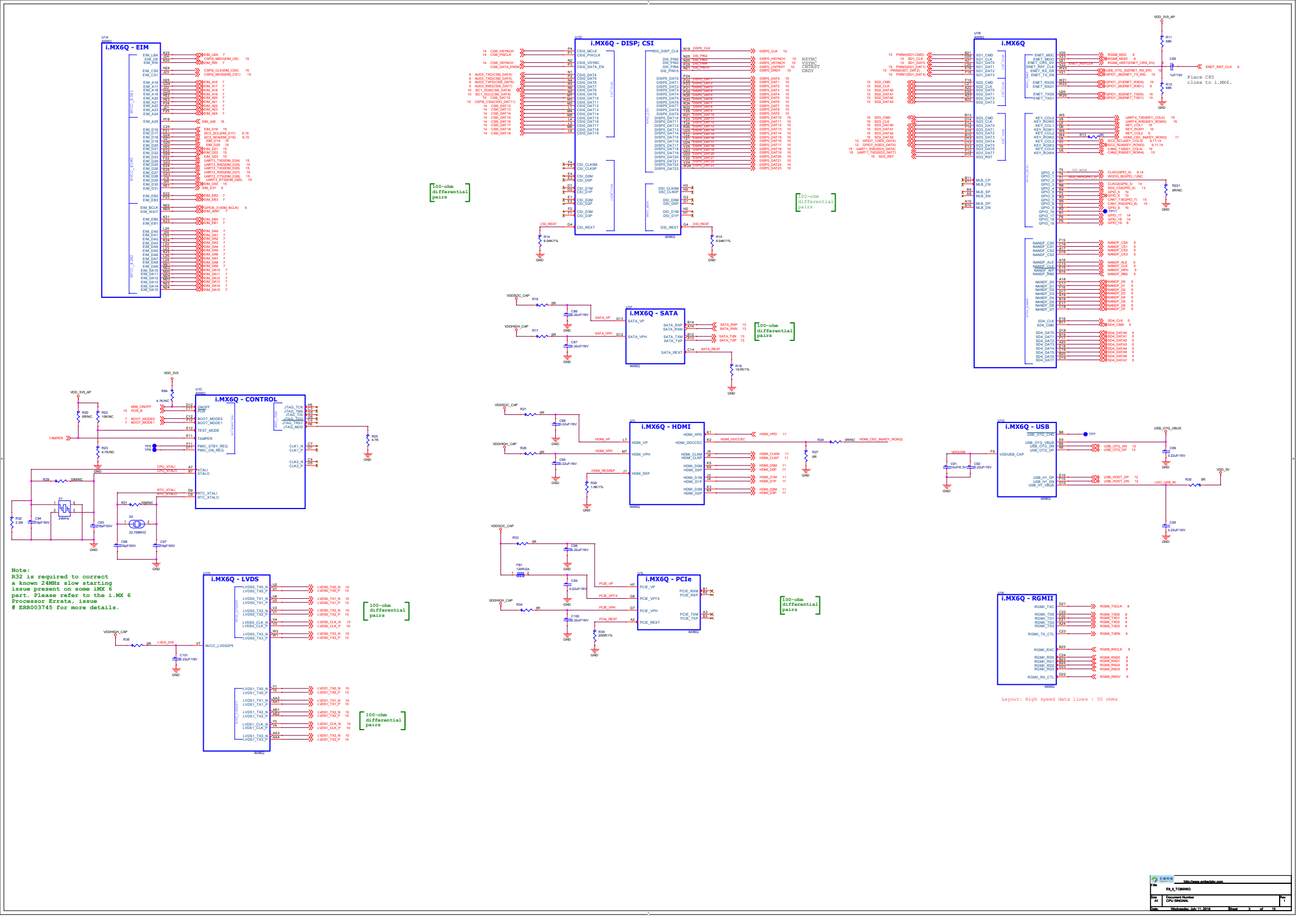


NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors.
To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground.
This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.


i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q
i.MX6Q - CONTROL
i.MX6Q - SATA
i.MX6Q - HDMI
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - PCIe
i.MX6Q - RGMII
100-ohm differential pairs
Note:
R32 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
Place C85 close to i.MX6.
Layout: High speed data lines : 50 ohms
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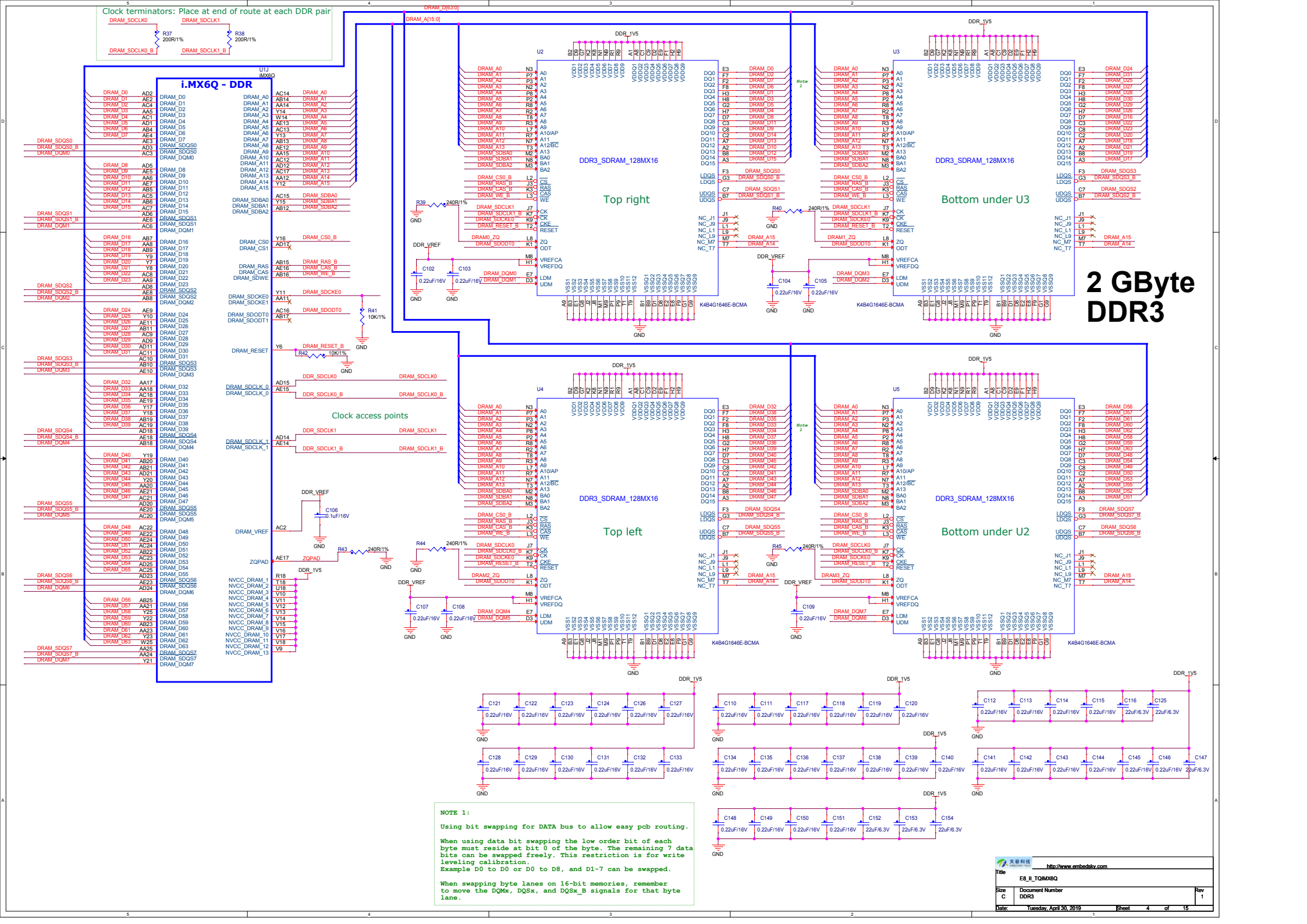
Clock terminators: Place at end of route at each DDR pair
DRAM_SDCLK0
DRAM_SDCLK1
R37 200R/1%
R38 200R/1%
DRAM_SDCLK0_B
DRAM_SDCLK1_B
i.MX6Q - DDR
U1J iMX6Q
DRAM_D[63:0]
DRAM_A[15:0]
DDR_1V5
DDR3_SDRAM_128MX16
K4B4G1646E-BCMA
U2
Top right
U3
Bottom under U3
U4
Top left
U5
Bottom under U2
Note 1
2 GByte DDR3
Clock access points
DDR_VREF
R39 240R/1%
R40 240R/1%
R41 10K/1%
R42 10K/1%
R43 240R/1%
R44 240R/1%
R45 240R/1%
C102
C103
C104
C105
C106 0.1uF/16V
C107
C108
C109
0.22uF/16V
GND
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
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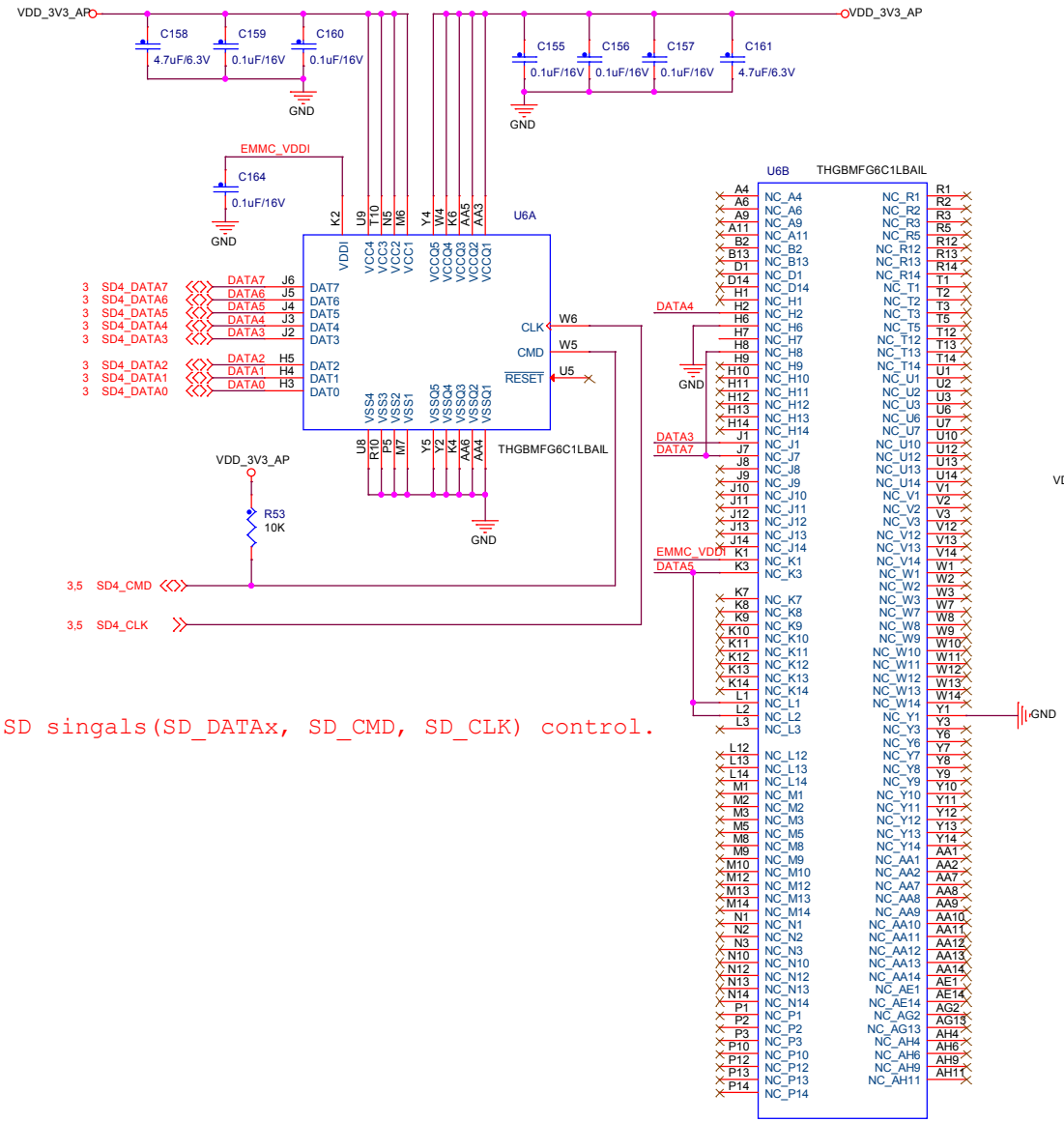
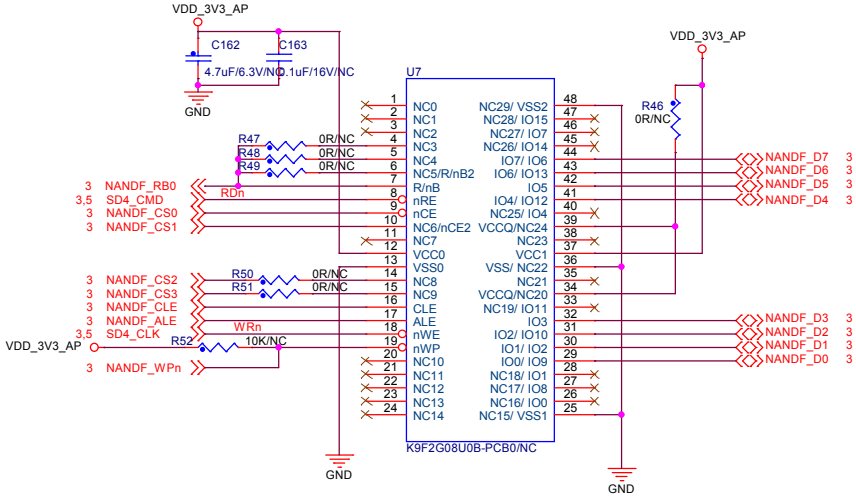
8GB eMMC MEMORY



NAND Flash memory



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

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Title	E8_II_TQIMX6Q		
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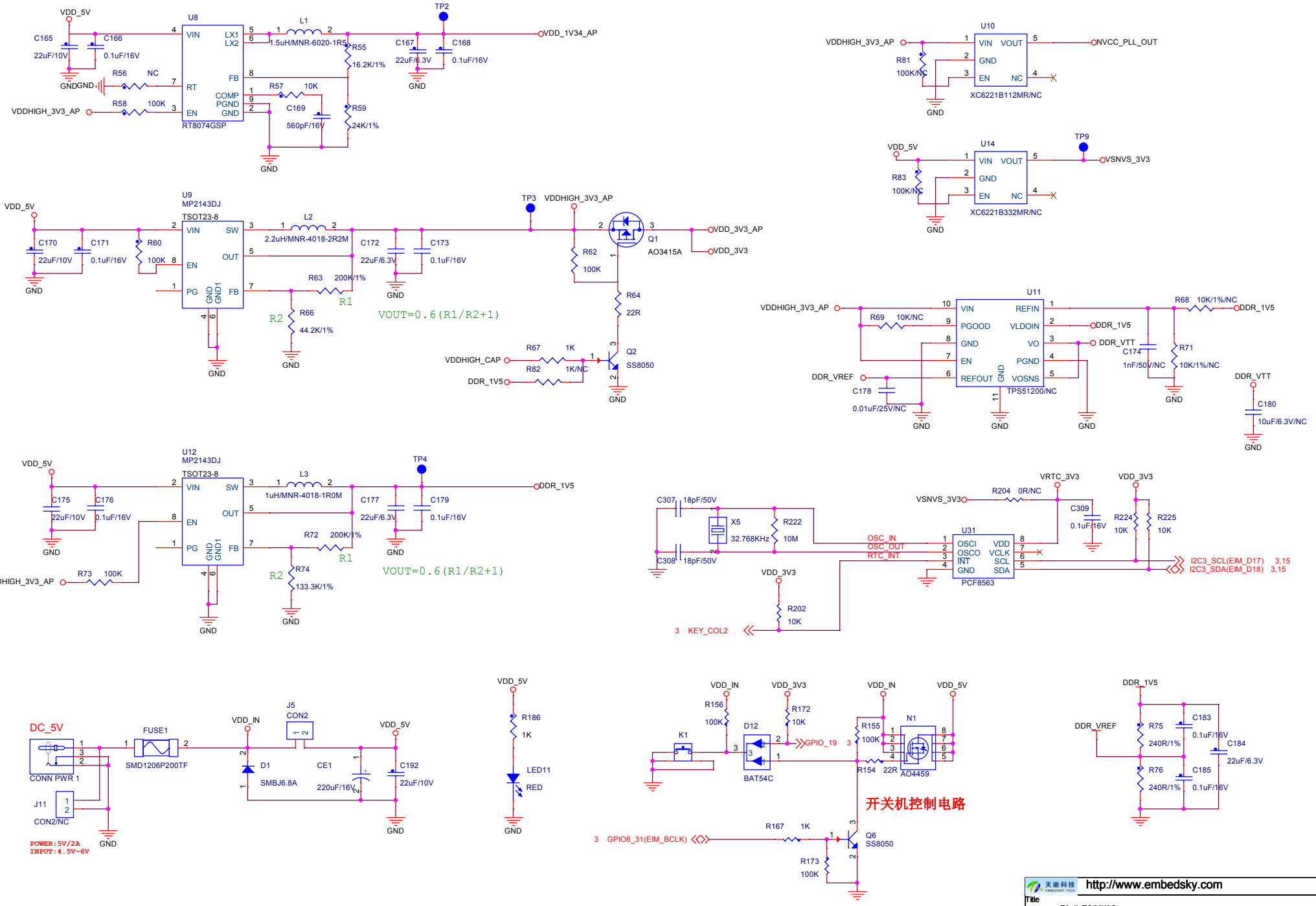

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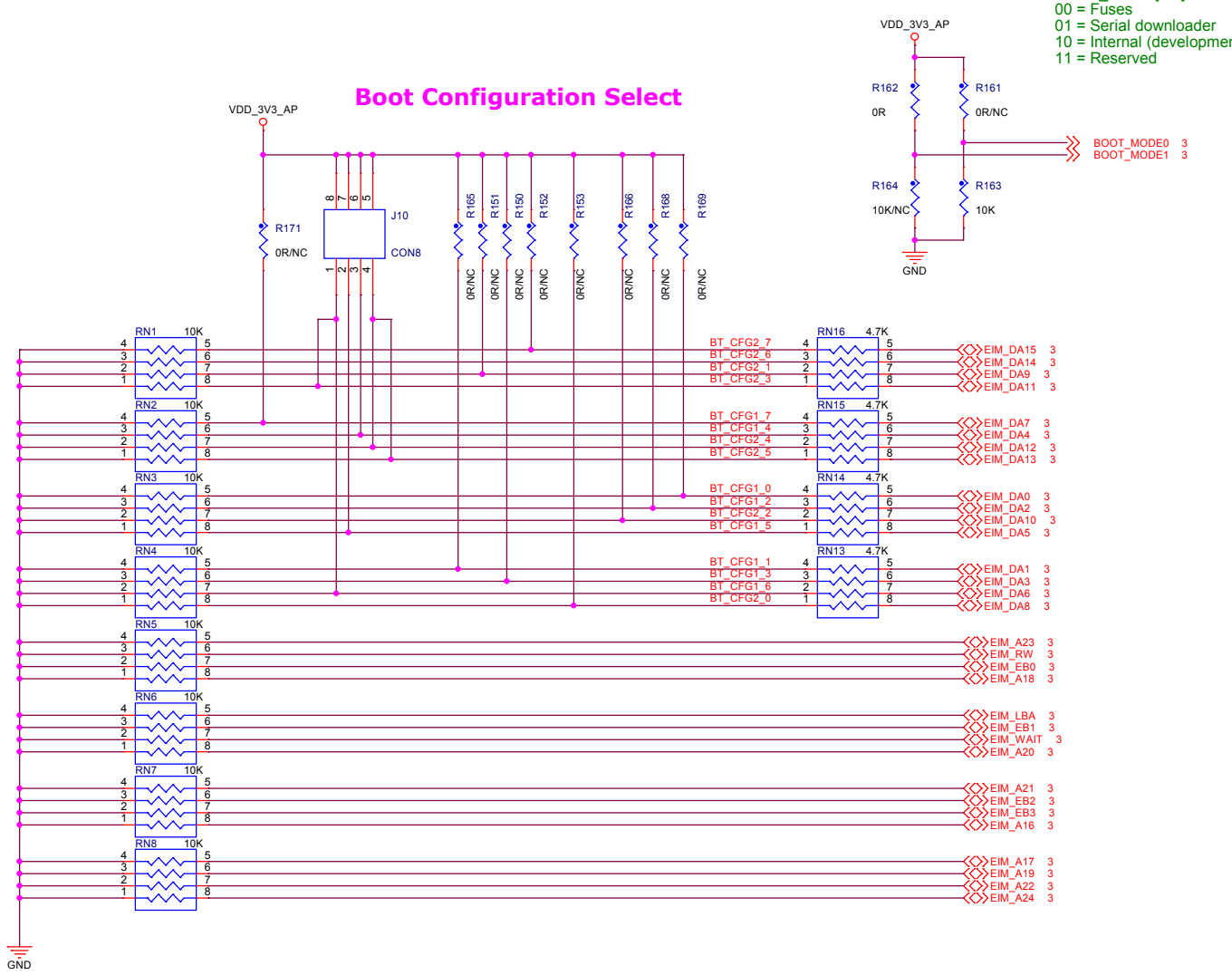
BOOT_MODE[1:0] SETTINGS
00 = Fuses
01 = Serial downloader
10 = Internal (development)
11 = Reserved



Boot Configuration Select

G1-6 G2-3	G1-5	G1-4	G2-5 G2-4	MODE
1	0	0	0	SD2_Boot
1	1	0	1	eMMC_Boot
0	1	1	0	DownLoad

BT_CFG2_3 BT_CFG1_6 BT_CFG1_5 BT_CFG1_4 BT_CFG2_4 BT_CFG2_5

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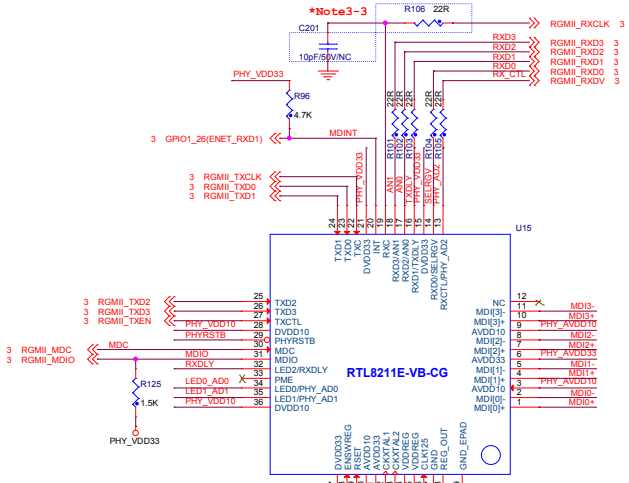
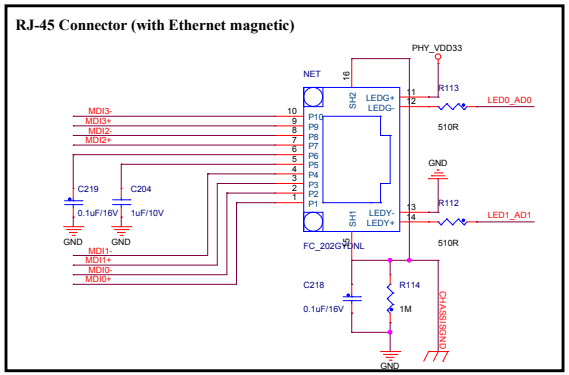
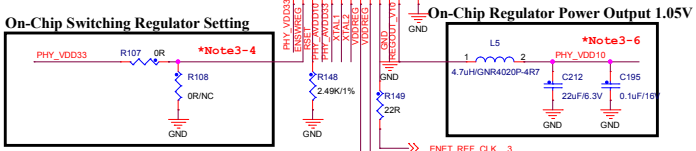
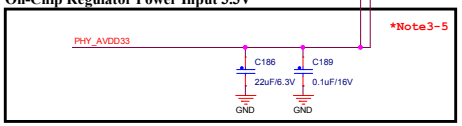
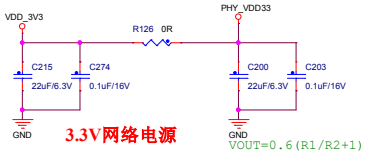


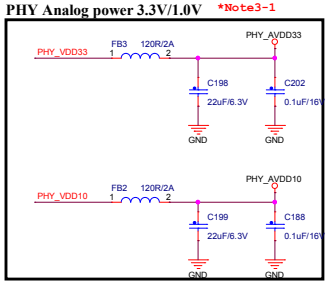




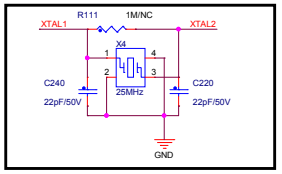




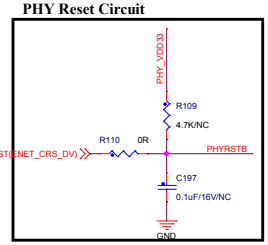
PHY Analog power 3.3V/1.0V *Note3-1

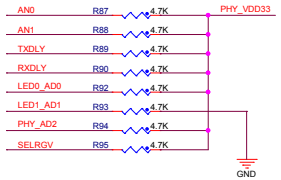


25MHz +- 50ppm Crystal



PHY Reset Circuit





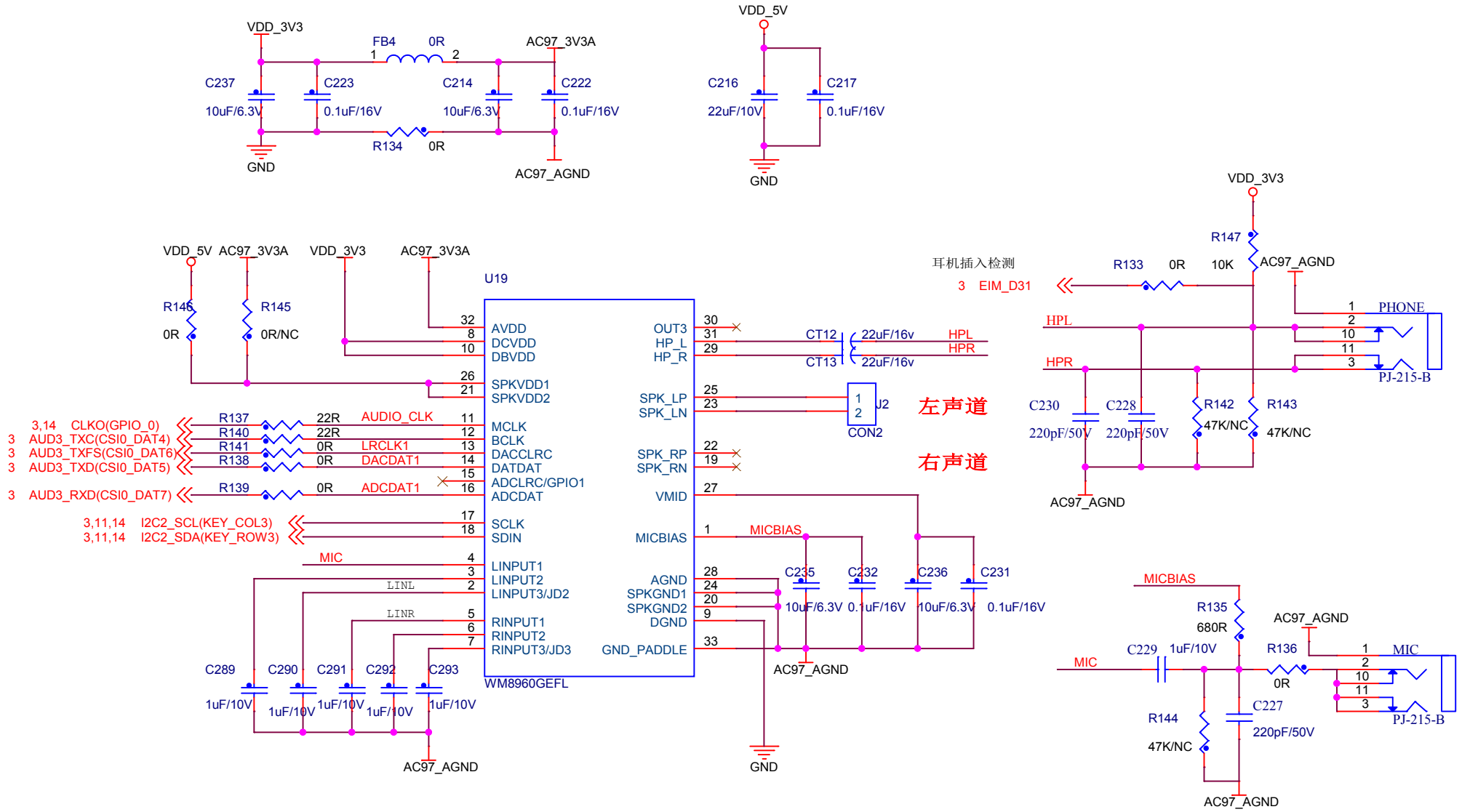
	AN0 Pull High	AN1 Pull High	Enable all Nway capabilities
	TXDLY Pull High	RXDLY Pull High	Delay TXCLK/RXCLK 2ns
AD2 Pull Low	AD1 Pull Low	AD0 Pull High	PHY Address=001 (0x01)
		SELREG Pull High	Pull Up for 3.3V GMII/RGMII

*Note3-3
The R19 and C24 are reserved for EMI, please close to PHY as possible.

*Note3-4
1. Enable On-chip Switch Regulator: (Default)
Connect ENSWREG to PHY_VDD33 (i.e. Mount R44and unmount R41)
2. Disable On-chip Switch Regulator:
Connect ENSWREG to GND (i.e. Mount R41 and unmount R44)

*Note3-5
The 3.3V power input VDDREG trace should be wider than 100mils (Keep floating while disabling on-chip switching regulator)
The capacitors C16 and C17 as close to the VDDREG pin (within 200mils) for good power effeciency.
C16 must be a ceramic (X5R) capacitor
C17 is recommended to be ceramic capacitor

*Note3-6
L2 (4.7uH) should be as close to RTL8211E REG_OUT pin (within 200mils).
The 1.05V power output REG_OUT trace should be wider than 60 mils.
The C7 and C6 capacitors as close to L2 if possible. (Keep floating while disabling on-chip switching regulator)
C7 must be a ceramic (X5R) capacitor
C6 is recommended to be ceramic capacitor



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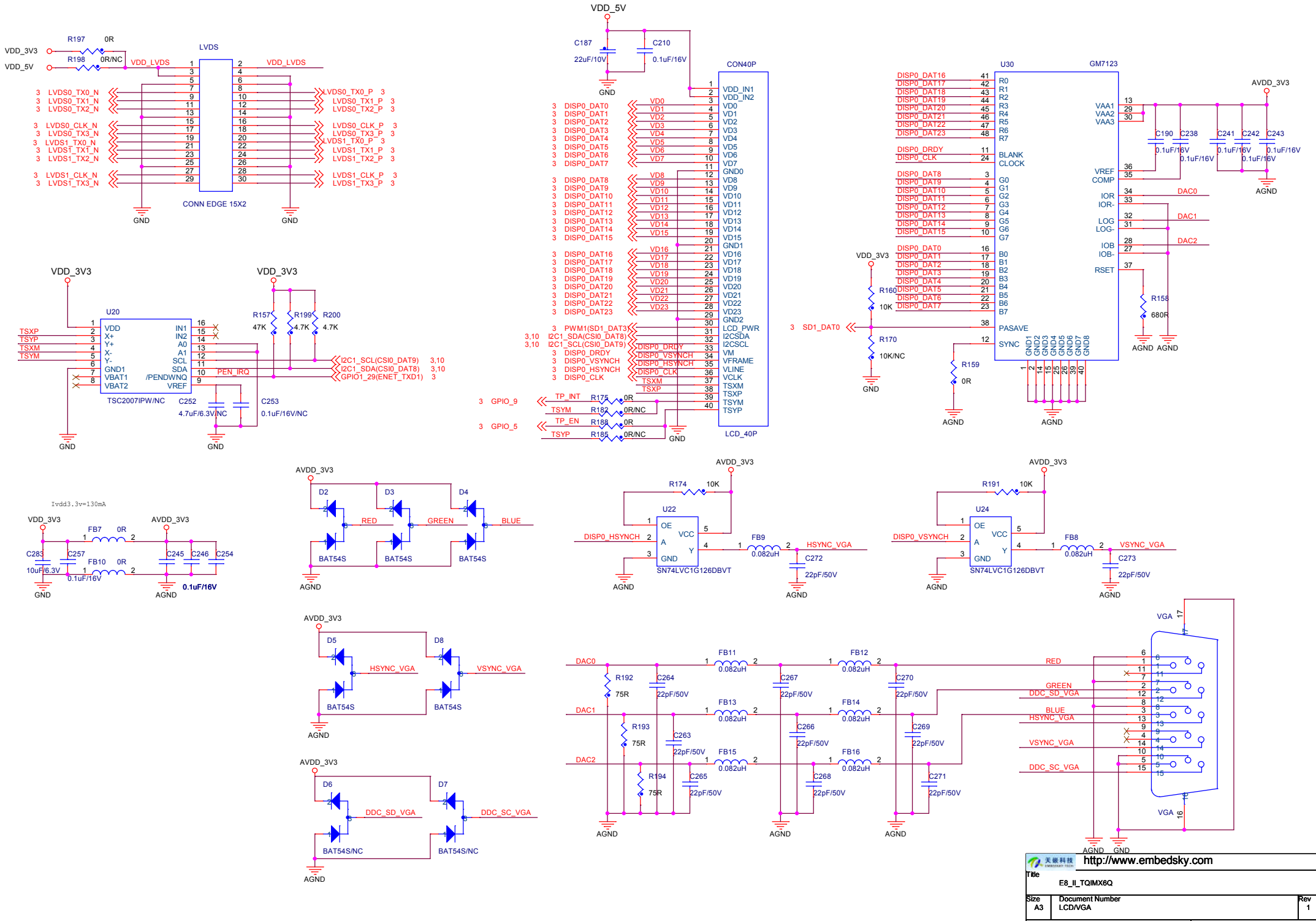
LVDS
CONN EDGE 15X2
CON40P
LCD_40P
U30
GM7123
U20
TSC2007IPW/NC
U22
U24
SN74LVC1G126DBVT
VGA
BAT54S
BAT54S/NC
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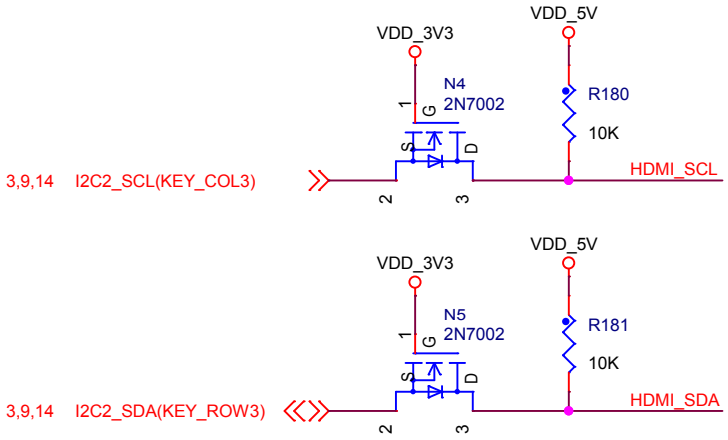
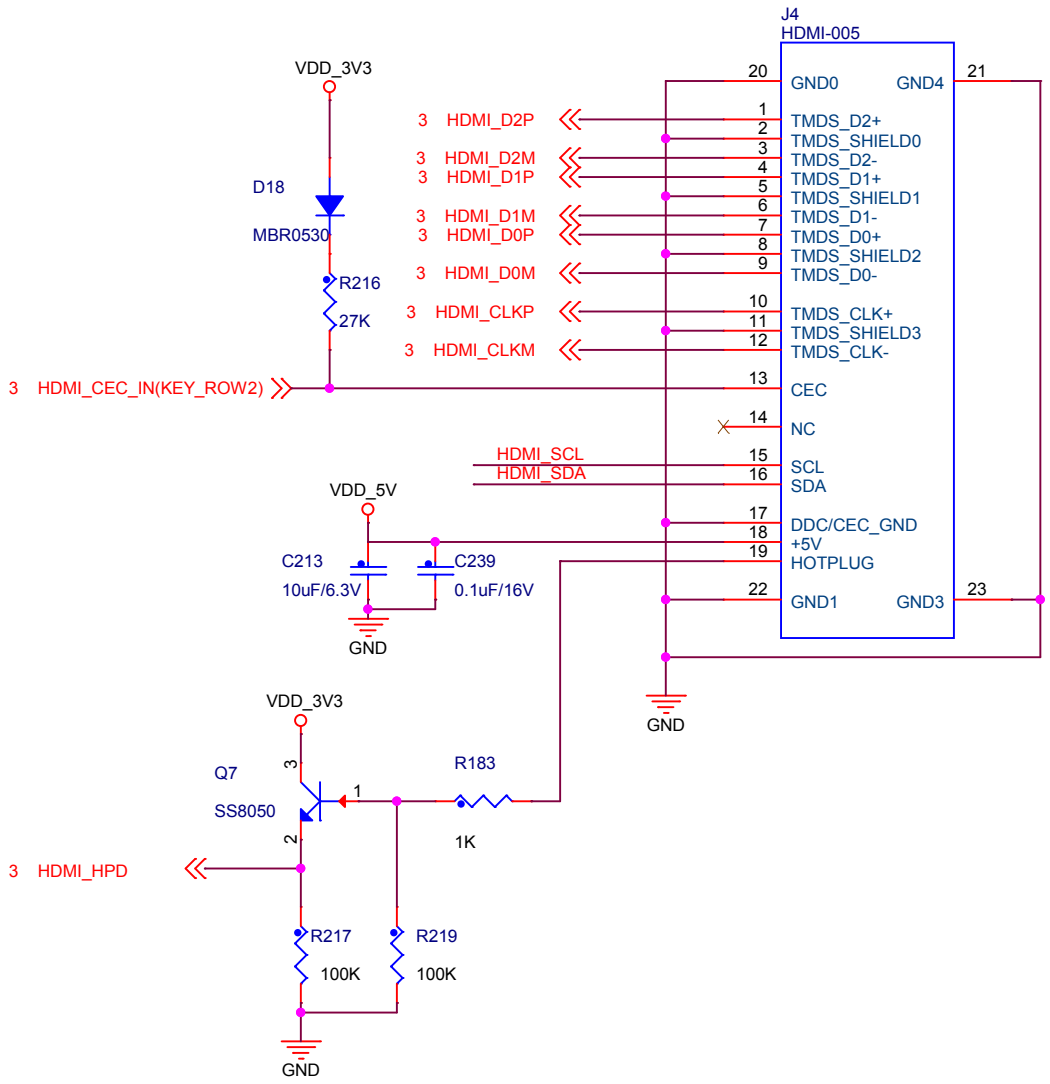
HDMI



HDMI A TYPE



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Title: E8_II_TQIMX6Q		
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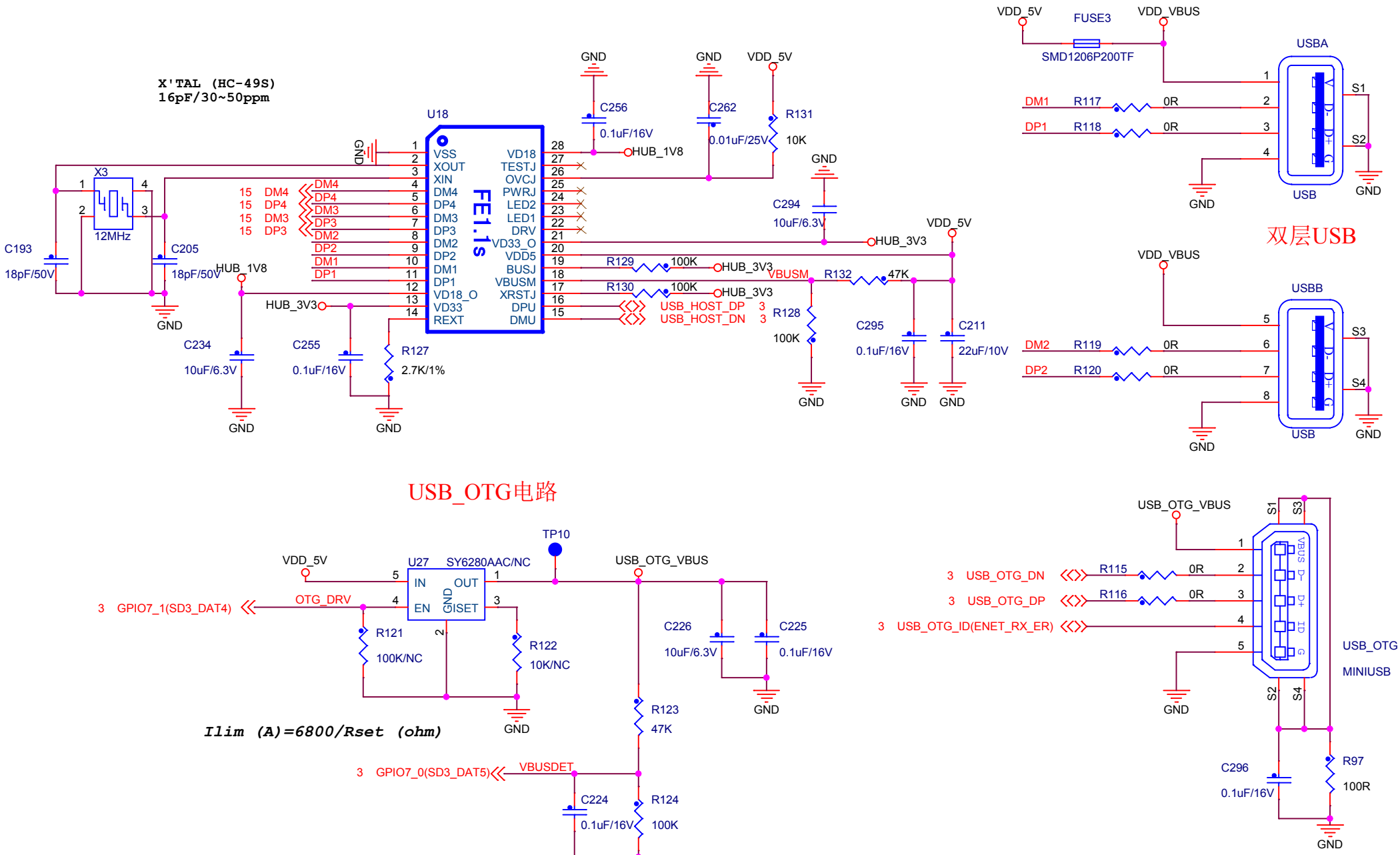

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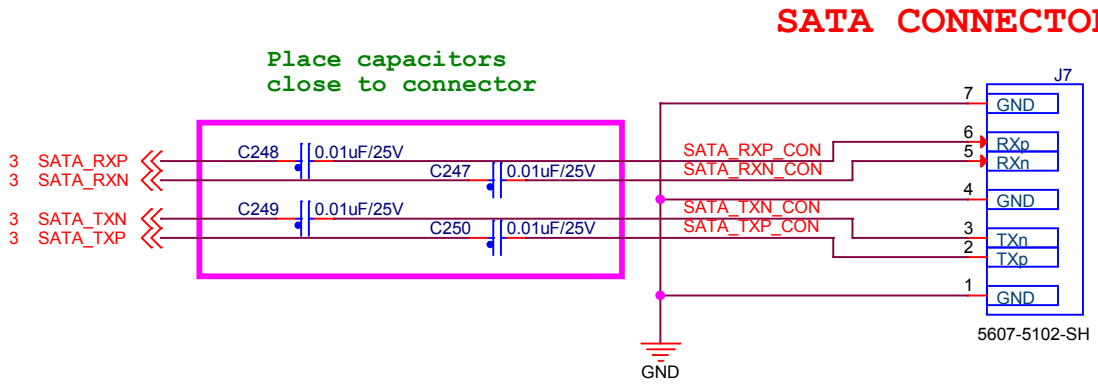
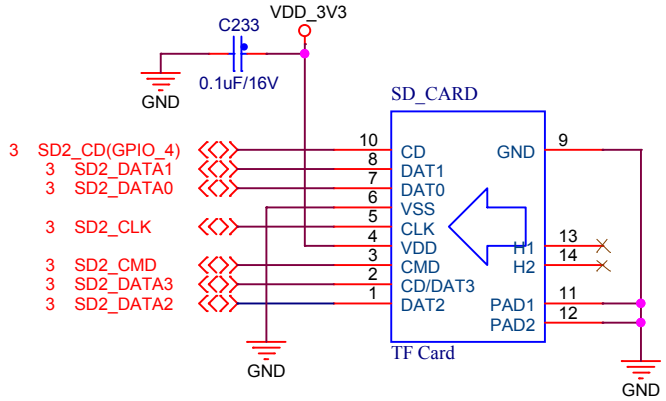
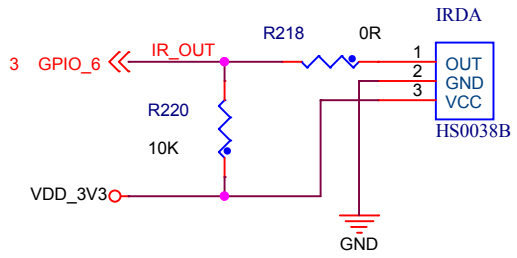
SATA CONNECTOR





红外电路



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Title: E8_II_TQIMX6Q		
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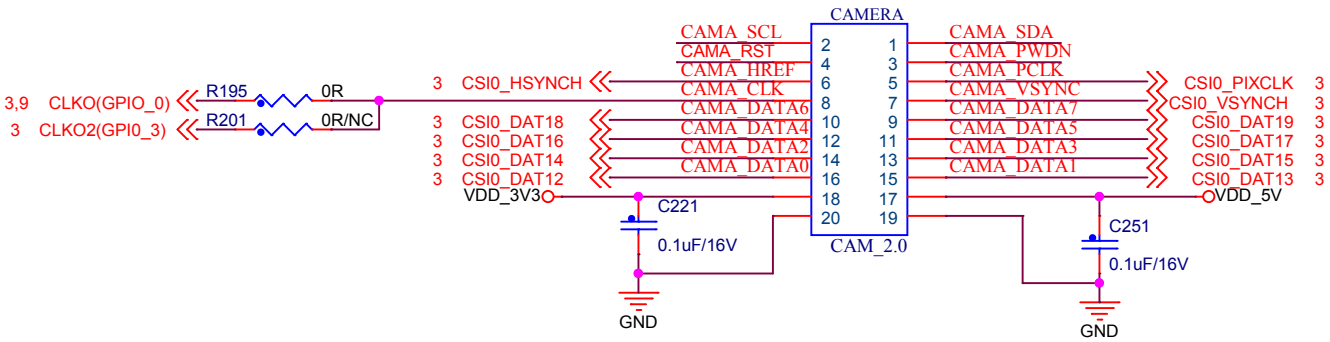
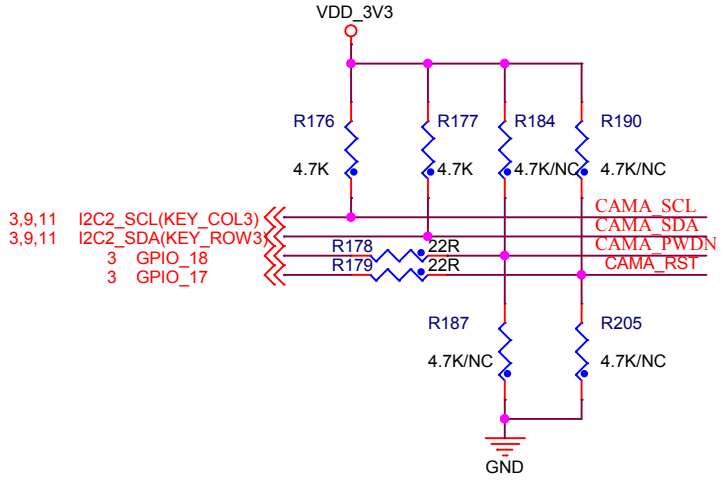
CAMMER A





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Title: E8_II_TQIMX6Q		
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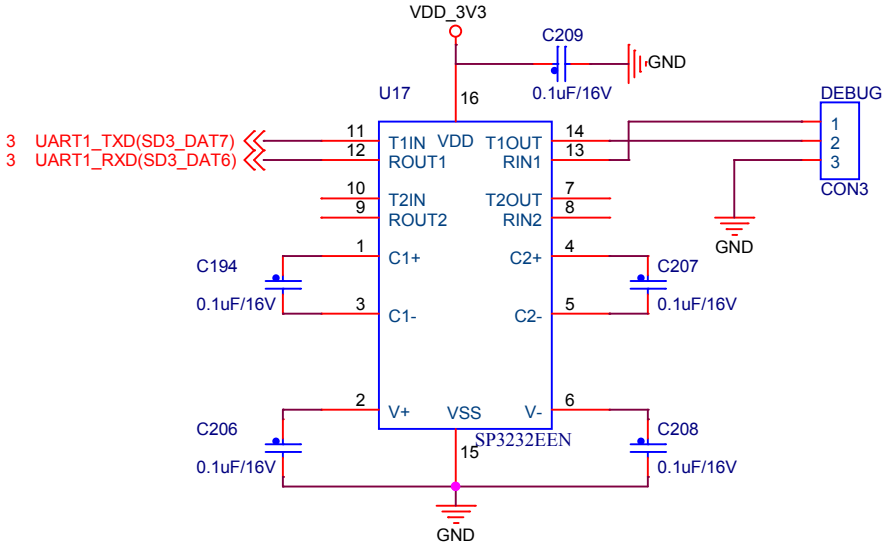
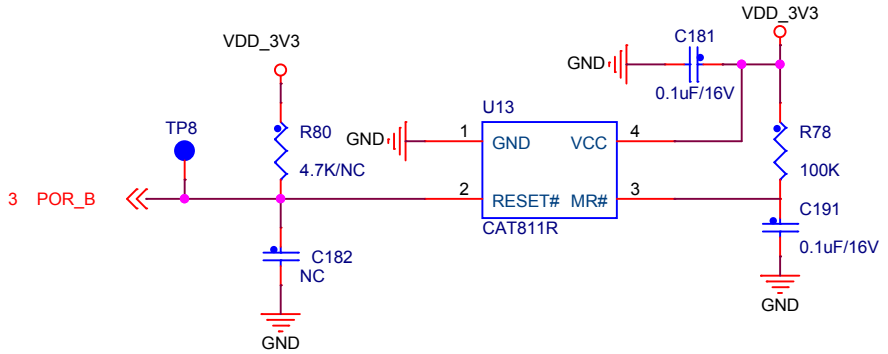
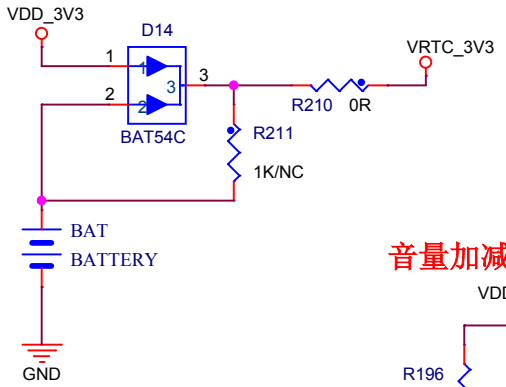
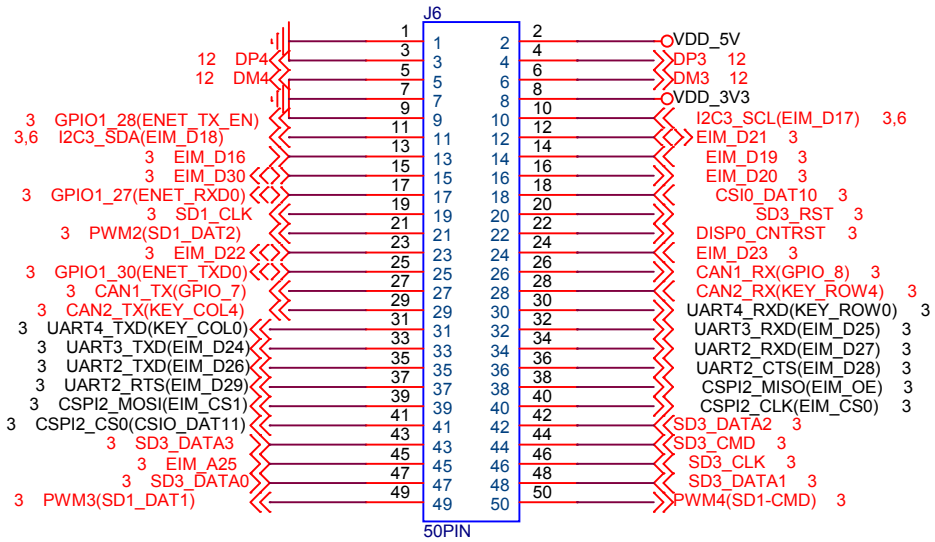




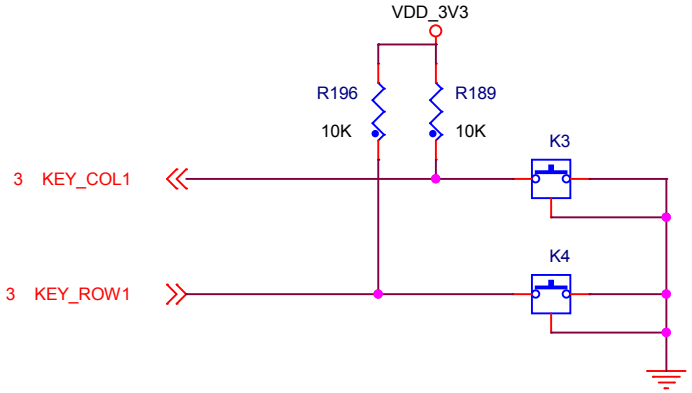
RTC电路



扩展接口



音量加减控制按键



H1
H2
H3
H4

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