4. Circuit Design

4.1 Universal Gates

$$F(X, Y, Z, W) = (\overline{X} + \overline{Y}) \cdot (Z + W)$$

(By De Morgan, $\overline{X} + \overline{Y} = \overline{XY}$)

$$= \overline{XY} \cdot (Z + W)$$

(By distributive law,

$$= \overline{XY}\,Z + \overline{XY}\,W$$

negate the function twice

$$= \overline{\overline{XY}\,Z + \overline{XY}\,W}$$

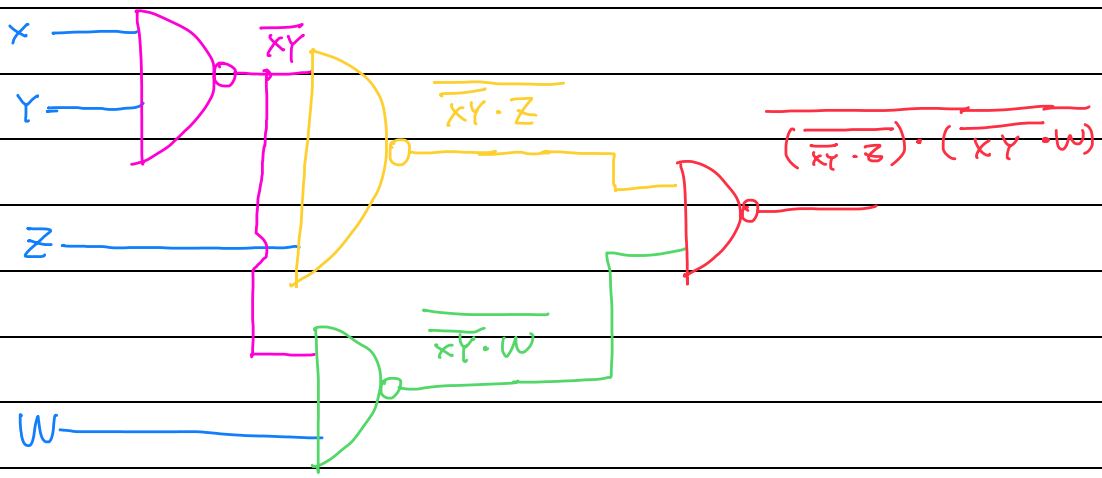
since $\overline{A} = A$ & De Morgan

$$= \left(\overline{\overline{XY}\,Z}\right)\left(\overline{\overline{XY}\,W}\right)$$

↑ NAND gates apply.

$$\left[\overline{(\overline{XY}) \cdot Z}\right] \cdot \left[\overline{(\overline{XY}) \cdot W}\right]$$

Design:



This is the end of my Question 4.1 explaination;
This is implemented in the Logism file