COMP-273 Assignment 1

School of Computer Science
McCall University
Available On: Friday, January 18th, 2019.
Due Date: Monday, January 28th, by 11:59 pm.

Hand in your solutions using *mycourses*, following the instructions at the end of this assignment, on page 3. Before starting create a folder on your computer system and call it *answer-folder*. **late policy: 10% off per day late, for upto 2 days. If submitted 48 hrs or more after the deadline, your assignment will not be accepted!.**

1 Number Representation (15 marks)

Complete the table below. You must show your work to get full credit for an answer.

Decimal	Binary	Hexadecimal
-243	give 16-bit signed representation	
728	give 16-bit signed representation	
	1101.0111 (unsigned)	
	11011100 (unsigned)	
		7D.8
		1B5

2 Floating Point Number Representation (15 marks)

1. Represent -76.678595 as an IEEE single precision floating point number (binary and hexadecimal).
2. Represent 19.459931 as an IEEE single precision floating point number(binary and hexadecimal).
3. Add the signed binary fixed point versions of the above two floating numbers using binary arithmetic and report your answer, showing your working.

You must show your work to get full credit.

3 Boolean Algebra (10 marks)

Assume that F is a Boolean function, as defined below, and all the other Boolean variables are inputs. Derive and give:

i. The truth table,

ii. A sum of products expression for F that is minimized.

iii. A product of sums expression that F is minimized. By "minimized" we mean an expression that cannot be further simplified while retaining its form (sum of products or product of sums).

(a) $F(A, B, C, D) = (\overline{A} + B \cdot \overline{D}) \cdot (C \cdot B \cdot A + \overline{C} \cdot D)$

(b) $F(W, X, Y, Z) = \overline{(W + \overline{X})(Z\overline{Y} + X)}$

4 Circuit Design (60 marks)

4.1 Universal Gates (10 marks)

A NAND gate or a NOR gate is a universal logic gate, because it can be used to construct all other logic gates. What is the minimum number of two input NAND gates required to implement the following Boolean expression $F(X, Y, Z, W) = (\overline{X} + \overline{Y}) \cdot (Z + W)$, where X, Y, Z and W are inputs? Explain your reasoning. One you have figured out the minimum number of required NAND gates, draw the circuit in *Logisim* using **only** NAND gates and test it. The TAs should be able to change the logical values of the inputs while obtaining the correct output.

4.2 Parity Counter (30 marks)

You are asked to design a 4-to-3 parity counter. Such a circuit has 4 input bits, A, B, C, D and 3 output bits F_2, F_1, F_0. The value that the circuit outputs is the number of its input bits that are set to 1. For example if the input is 1010, then the circuit will output 010 (which is the binary representation of 2 as the unsigned 3-digit binary number $F_2F_1F_0$). Similarly, if the input is 1111, then the output will be 100. Consider F_2 as the highest order bit of the result and F_0 as the lowest order bit.

i. Construct the truth table for this circuit.

ii. Write down the Boolean expressions for each of the three outputs in sum of products form. Now, simplify each expression using the laws of Boolean algebra to derive minimized sum-of-products forms.

iii. Design this circuit in *Logisim* and test it. The TAs should be able to change the logical values of the inputs while obtaining the correct output.

4.3 Full-adders and half-adders (20 marks)

What is the minimum number of full-adders and half-adders that are needed to count the total number of ones in an unsigned 7-bit binary number $A_6A_5A_4A_3A_2A_1A_0$? You are allowed to use only full-adders and half-adders in your solution. You must show your work to get full credit. Draw the corresponding circuit diagram in *Logisim* and test it. For this you are allowed to use the built in "adder" module in logism-evolution, i.e., you don't have to first build an adder from simpler gates.

5 ASSIGNMENT SUBMISSION INSTRUCTIONS

Everything should be handed in electronically on *mycourses*. Each student is to submit his or her own unique solution to these questions.

i. The circuit diagrams must be in LOGISIM while text can be in PDF, RTF or TXT file formats. Zip all the files if your submission has more than 1 file.

ii. The Logisim circuits must run under logism-evolution, to be graded.

iii. Zip your *answer-folder*, rename it with your student ID number. For example, 260763964.zip

iv. Submit this single compressed file on *myCourses* under Assignment 1.

v. Make sure that you submit a single file (the zipped file), not many files.

vi. Make sure that the file is in your assignment folder following your intended upload. In other words, make sure what is present in your assignment folder it was what you intended us to grade. Unfortunately, if it is not there or it is corrupted, you cannot submit a corrected one after the deadline.