NOVATEK 聯詠科技

Data Sheet

NT98530BG

Imaging Processor

Datasheet

Table of Contents

Revision History

Rev.	Date	Contents
V0.1	2021/07/11	draft
V0.2	2021/09/11	draft
V0.3	2022/01/06	Add pin description

Features

■ High Performance 32-bit CPU

- □ Quad Core ARM® Cortex™ A53
- □ NEON™ and FPU acceleration
- □ 32 KB instruction cache, 32 KB data cache and 512 KB L2 cache
- □ Embedded ICE makes firmware debugging easier

■ Power Management features

- □ Firmware configurable operating frequency of each functional block to meet best power budget

■ Integrated Clock Generator

- □ Internal PLL with spread spectrum capability
- □ 12MHz system
- □ 32768Hz RTC oscillator

■ Scalable Memory Bus Architecture

- □ One 32-bits DDR4/LPDDR4/LPDDR4X SDRAM interface, supporting up to 16Gb+16Gb
- □ DRAM operating data rate up to DDR4 3200/LPDDR4/LPDDR4X 3733(TBD)

□ Sensor Interface Engine

- □ Support high speed serial interface like MIPI/sub-LVDS /HiSPi up to 12 channels and 5 clocks (5C12D) : 1C4D(2.5G) + 2C4D(1.5G) x2
- □ Support parallel sensor interface Input
- □ Support maximum input width up to 8188
- □ BT.601/656(8-bit)/BT.1120 x2
- □ Support 12-bit sensor data input
- □ Support companding HDR sensor
- □ Built-in color pattern generation
- □ Sensor black level clamping
- □ Efficient defect concealment algorithm
- □ Flexible image analysis flow for AE, AWB purpose
- □ Programmable histogram analysis
- □ In-pipeline color shading compensation technology
- □ Support EIS with gyro-sensor input
- □ Support RGBIr4x4, RCCB format
- □ Support up to 8Mp75 or 640M pixel/sec for typical case
- □ Support up to 3 HDR sensor (Two HDR with 3 frames or three HDR with 2 frames)

- Support h/w motion detection to wake up system
- Support additional digital gain up to 256x
- Support DVS sensor
- Support Bayer scaling down
- Support PDAF sensor

Image Processing Engine

- Support up to 8Mp75 or 600M pixel/sec for typical case
- Support maximum resolution up to 8188x8188
- Support on-line mode direct from Sensor Interface Engine
- Support bayer input compression
- Support YUV output compression
- Support 3 frames HDR with ghost reduction
- Support crop and H/V flip
- Support dynamic defect pixel concealment
- Powerful temporal and spatial noise reduction technology
- In-pipeline lens shading compensation technology
- Support radial crop
- Wide dynamic range (WDR) for global/local illumination enhancement
- Proprietary advanced anti-alias CFA color interpolation for Bayer and RGBIr4x4
- False color suppression
- In-pipeline geometric distortion correction
- In-pipeline color aberration correction
- R/G/B Gamma LUT
- Advanced edge rendering control and continuity enhancement
- Specific color control technology (Patented)
- Brightness/contrast and hue/saturation adjustment
- High precision color correction matrix for sRGB or specific color requirement
- Support defog function
- Support purple fringe reduction
- Support advanced motion compensated temporal filtering (MCTF) for efficient video noise reduction
- Support local contrast enhancement

Video Processing Engine

- Two VPE engines: VPE and VPE lite

- Support maximum performance up to 4Kp30 for both VPE and VPE lite
- Support geometric distortion correction
- Support 257x257 2DLUT warping
- Support sharpen after distortion correction
- VPE support 4 sets scaling output and VPE lite support 1 set scaling output
- Support YUV output compression
- VPE lite support PTZ function

DRE (Decomposition & Reconstruction Engine)

- Pyramid image fusion for image stitching usage

Stereo Depth Engine

- Support maximum image size up to 1080p20
- Support depth map by input left and right image
- Support max 64 disparity (0~63)
- Support sub-pixel accuracy
- Support confidence map

Image Manipulation Engine

- High quality anti-aliasing scaling engine from 1/16x to 32x
- Support 4 sets scaling output
  - Path 1: 420 separate planar and YUV420
  - Path 2/3/4: YUV420 and YUV422
- Support 8 sets privacy mask
  - Maximum 2048x2048 pixel

High Performance Image/Video DSP

- CEVA Senspro DSP
- Computing Capability, 0.5T neural network computing performance
  - 512 8x8 MACs per cycle
  - 128 8x16/16x8 MACs per cycle
  - 128 16x16 MACs per cycle
  - 16 32x32 MACs per cycle
  - 32 single-precision FP MACs per cycle
  - 64 half-precision FP MACs per cycle
- Fixed-point & floating-point operations for scalar/vector engine
- Internal data memory 512K & Internal program memory 32K & I cache 128K

DLA module

- □ DLA engine with computing power up to 2.0 TOPS
- □ NUE Network utility engine to accelerate post-processing and classification tasks
- □ NUE2 Network utility engine to accelerate pre-processing tasks

□ Computer Vision Acceleration

- □ IVE General intelligent video analysis operation
- □ DIS Digital image stabilization and object tracking engine
- □ TRKE tracking engine supports optical flow feature point tracking
- □ MDBC Motion detection and background construction engine

■ LCD Display

- □ Supports two independent video outputs
  IDE0 4Kp60
  IDE1 1080p60
- □ Support one HDMI 2.0, up to 4Kp60 outputs
- □ High performance scaling up/down engine, programmable gamma correction, color transform and color management for LCD display
- □ Two video windows(YUV422 / YUV420 UVPack)
- □ One OSD windows(8bit palette with alpha plane / ARGB4444 / ARGB1555 / ARGB8565 / ARGB8888)
- □ Programmable width & height to meet LCD resolution exactly
- □ Support digital LCD for 8bit-Serial-RGB, 6bit-Serial-RGB, 8bit-Serial-YUV, 16bit YUV, Memory (MCU) and MIPI-DSI interface (1/2/4 data lane & 1 clock lane)
- □ Support RGB565/RGB666/RGB888 parallel interface
- □ Support 16-bit RGB interface.
- □ Support Flip function
- □ Support rectangle about 16 (Face detection rectangle)sets with global alpha
- □ Support output YUV (422/420) data to dram(not including data in video2 path)
- □ Support digital interface BT.601/BT.656/BT.1120 output port (8bits Double-Data-Rate capable)
- □ Support progressive to interlace
- □ Support YCC 420 compress input
- □ Support programmable 64x64 hardware cursor
- □ Support display and write back to DRAM
- □ LCD / Digital video out

□ Graphic Engine

- □ Geometric operation including mirror, flip and rotation

- Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending
- OSD blending on YUV
- RGB invert
- Rotate 90/180/270 degrees
- Horizontal/ Vertical Flip
- Support YCC compress/decompress

True Random Number Generator

- Generate true random number
- 32-bits Random number generator

Video CODEC

- Support H.264/AVC codec BP/MP/HP, level 5.2
- Support H.265/HEVC codec MP, level 5.1
- Support encoding with performance up to 8-megapixel@60fps main stream + 720p@30fps sub stream
- Support decoding with performance up to fullHD@240fps
- Support picture resolutions up to 8192x8192 Support low latency video encoding
- Support post sharpen
- Support CBR, VBR and Macro block QP table
- Support adaptive quantization
- Support frame rotation by 90, 180 and 270 degrees
- Support ROI (10 sets) enhancing picture quality
- Support OSG function
- Support video format MP4, AVI, MOV
- Support full frame still capture while video recording

H/W Audio CODEC

- stereo 16-bits ADC audio recording
- stereo 16-bits DAC audio playback (only mono output)
- Programmable ALC / Noise Gate (for recording)
- Audio sampling rate : 8K, 11.025K, 12K, 16K, 22.05K, 24K, 32K, 44.1K, 48KHz
- Support dual microphone inputs
- Support 4-channel Digital microphone (MEMS-microphone) inputs

JPEG CODEC

- Supports Motion JPEG 8 megapixel@60fps encoding

- □ Max. pixel clock 480Mpixel / sec
- □ Support ISO/IEC 10918-1 baseline JPEG compression/decompression.
- □ Still image maximum resolutions will be up to 64Kx64K pixels
- □ Support encoder input format 420 and output format 2h11/411
- □ Support Encode/Decode rotation mode of 90, 180, 270 degree
- □ Support Encode/Decode mode, rotate 90, 180, 270 degree
- □ Support decode scaling 1/2, 1/4, 1/8 for width and height
- □ Support OSG
- □ Support Mask

■ Digital Audio Interface

- ■ Contains 2 DAI
- ■ Support 2 I2S codec interface
- ■ Support 1CH/2CH playback to HDMI(DAI2)

■ Dual Graphic-based OSD (OSG)

- □ Support 1/2/4-bit palette and ARGB(1555/4444) & RGB565 format / Color key
- □ Support 2 layers OSD
- □ Fixed OSD layer priority (top to down: OSD1->OSD2->Image)
- □ Support max. size up to 8192x8192(H.264/H.265) per layer(depend on encoder)
- □ Support Codec video encode OSD function
- □ Support up to 16 regions per layer
- □ Support Pixel alpha (ARGB1555, ARGB4444 and Palette) and Global alpha (RGB565)
- □ Support OSD QP

■ Storage Memory Controller

- □ Three SD/MMC Controllers for SD card, MMC and SDIO devices

  SDIO/SDIO2 support SD memory card protocol ver3.0 and SDIO protocol ver3.0

  SDIO3 support eMMC protocol ver5.1, SD memory card protocol ver3.0 and SDIO protocol ver3.0
- □ Support UHS-I: UHS50 (Max. freq. 160MHz)
- □ Hot insertion/removal for SD/MMC Card
- □ Built-in generation and checks for CRC data

■ USB 2.0

- □ Fully compliant with USB2.0 device/host (1 set)
- □ Support Control / Isochronous / Interrupt and Bulk transfer
- □ Support PC camera mode

■ USB 3.0

- □ Compliant with USB specification revision 3.0 and 2.0
- □ Compliant to eXensible Host Controller Interface (XHCI) version 1.0
- □ Support Control / Isochronous / Interrupt and Bulk transfer
- □ Supports aggressive power management, including U0/U3 for USB3.0 device

■ Timers

- □ RTC can be powered by separate backup battery and operating from 1.5V to 3.3V
- □ Watch dog timer
- □ 20 programmable HW timers support resolution up to 3MHz and 32 bits counter
- □ 2 high-resolution HW timers with dedicate interrupts, and support resolution up to 120MHz and 64 bits counter

■ Peripheral Interface

- □ Support I2C interface (11 sets)
- □ Support 12 channels PWM including built-in 2 (2 sets) pattern generators for μ-Stepping motor control
- □ Support GPIO and flexible PWM interface with micro-stepping
- □ Support programmable 3-wired serial interface (with DMA transfer)
- □ Support SPI interface (only PIO)
- □ Dedicated SPI for gyroscope reading(only PIO)
- □ Support NFC & BLE4.0 interface
- □ Support UART interface (9 set, 1 with PIO and 8 with DMA transfer and support RS485 standard)
- □ Support Remote interface
- □ Support 4 channels of 8-bit ADC, the max. sample rate up to 9.615 KHz per channel
- □ Two embedded Ethernet 10M/100M/1000M MAC and support RMII/RGMII interface. PHY clock output
- □ Support IPv4/IPv6/TCP/UDP/ICMP checksum offload
- □ Support TSO (TCP Segmentation Offload)
- □ Support UFO (UDP Fragmentation Offload)
- □ Support external PHY with RMII/RGMII
- □ Embedded temperature sensor for obtaining the internal chip temperature.

■ On-chip Boot Strap Loader

- □ Built-in on-chip mask ROM
- □ User program can be stored in NAND-type flash and external static memory is not necessary
- □ On-chip mask ROM can be disabled

- System can boot from SPI NOR/ NAND flash, memory cards, eMMC, Ethernet

■ Voltage Power Supply

- 0.95V core logic voltage (TBD)
- 1.2V for DDR4, 1.1V for LPDDR4, 1.1V/0.6V for LPDDR4X
- 1.8V I/O interface and analog circuit voltage
- 3.3V I/O interface and analog circuit voltage

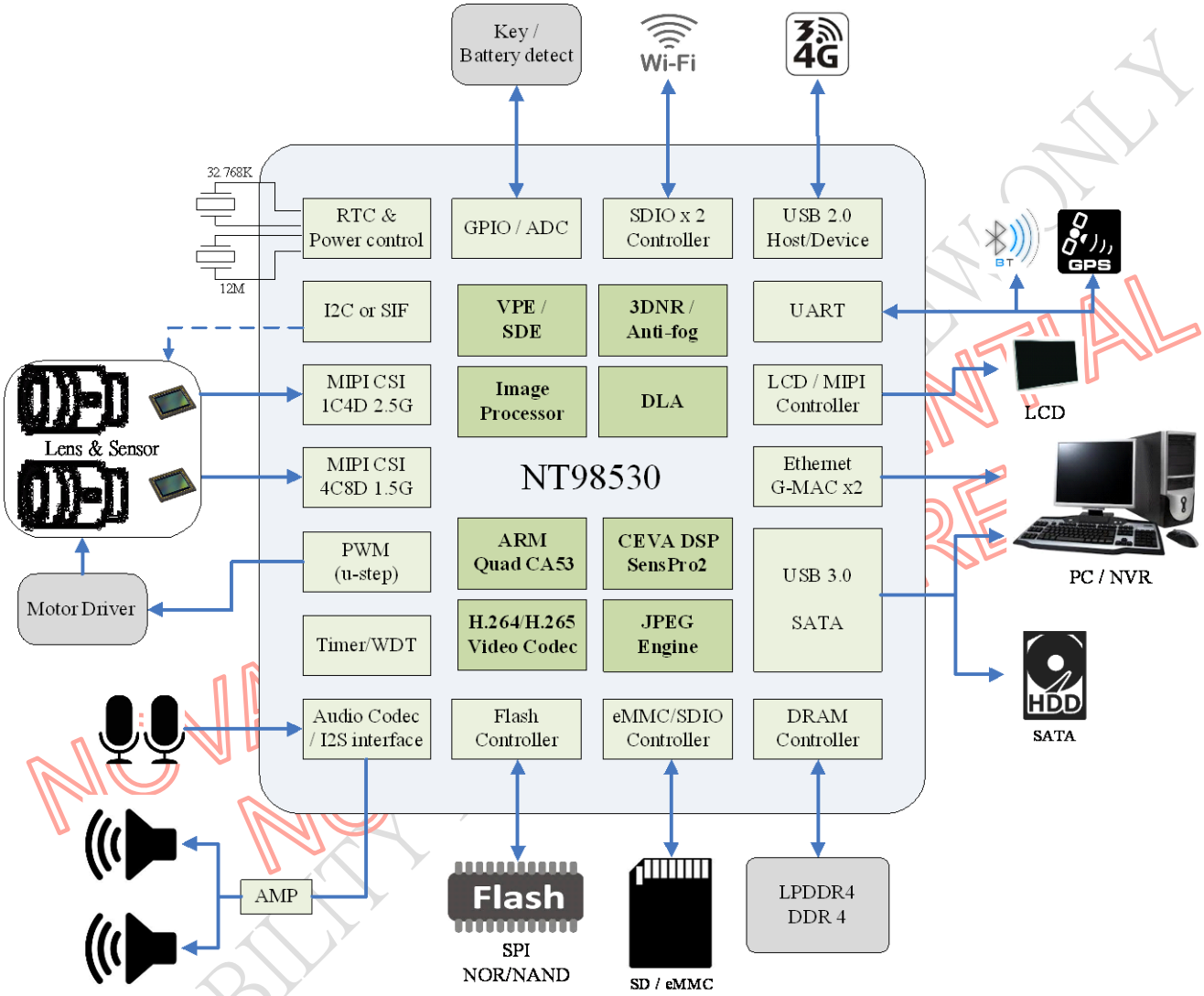
■ Package

- NT98530BG: 437 ball FC-CSP 15x15 mm^2

General Description

Novatek NT98530 is a highly-integrated SoC with high image quality, low bitrate, low power consumption, targets on 8Mp60 Edge-Computing IP camera application. The SoC integrates ARM Quad Cortex A53 CPU core, new generation ISP, H.265/H.264 video compression encoder, DSP, high performance hardware DLA module, graphic engine, dual display controller, Ethernet GMAC, USB3.0 and USB 2.0 Host/Device, audio codec, RTC and SD/SDIO 3.0 to provide best cost performance Edge-Computing IP camera solution.

Block Diagram



Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	GND	DDR1_DQL2/DQS_B	DDR1_DQL6/DQ4_B	DDR1_DQU4/DQ8_B	MC10	MC0	P_GPO34	HSI1_D1P	HSI1_D3P	HSI1_CK0P	HSI1_D0P	HSI1_D2P	HSI2_D7P	HSI2_CK3P	HSI2_CK2P	HSI2_CK0P	HSI2_CK1P	HSI2_D3P	S_GPIO3	S_GPIO4	S_GPIO7	GND	A
B	DDR1_DQL0/DQ7_B	DDR1_DQL4/DQ6_B	DDR1_DQU6/DMI1_B	GND	MC9	MC1	SYS_RSTO#	HSI1_D1N	HSI1_D3N	HSI1_CK0N	HSI1_D0N	HSI1_D2N	HSI2_D7N	HSI2_CK3N	HSI2_CK2N	HSI2_CK0N	HSI2_CK1N	HSI2_D3N	S_GPIO2	S_GPIO5	S_GPIO11	S_GPIO13	B
C	DDR1_DQSLt/DQS0_t_B	DDR1_DQSLc/DQS0_c_B	DDR1_DMUn/DQ14_B	DDR1_DQU0/DQ15_B	MC8	MC2	P_GPIO30	P_GPIO27	P_GPIO24	GND	P_GPIO32	P_GPIO33	HSI2_D6P	HSI2_D5P	HSI2_D4P	HSI2_D0P	HSI2_D1P	HSI2_D2P	S_GPIO1	S_GPIO6	S_GPIO12	S_GPIO14	C
D	DDR1_DQL7/DQ0_B	GND	DDR1_DQU2/DQ9_B	GND	MC7	MC5	P_GPIO31	P_GPIO26	P_GPIO25	P_GPIO22	P_GPIO20	P_GPIO21	HSI2_D6N	HSI2_D5N	HSI2_D4N	HSI2_D0N	HSI2_D1N	HSI2_D2N	S_GPIO10	S_GPIO17	S_GPIO16	S_GPIO15	D
E	DDR1_DQL1/DQ1_B	DDR1_DMLn/DMI0_B	DDR1_DQSUt/DQS1_t_B	DDR1_DQSUc/DQS1_c_B	MC6	MC4	MC3	P_GPIO29	P_GPIO28	P_GPIO23	HSI1_REXT			S_GPIO0	GND	S_GPIO8	S_GPIO9	S_GPIO18	S_GPIO20	S_GPIO21	S_GPIO22	S_GPIO23	E
F	DDR1_DQL5/DQ3_B	DDR1_DQL3/DQ2_B	DDR1_DQU7/DQ10_B	DDR1_DQU3/DQ11_B	DDR1_DQU1/DQ13_B		ETP										S_GPIO19	S_GPIO26	S_GPIO25	S_GPIO24	P_GPIO4	P_GPIO10	F
G	GND	DDR_A3	DDR_ODT	GND	DDR1_DQU5/DQ12_B		AVDDK_DDR	VDDM_MC	VDD18_MCP2	VCC33_PIO2	AVDDK_HSI1	AVDD18_HSI1	AVDD18_HSI2	AVDDK_HSI2	VDD18_SNP1		P_GPIO3	P_GPIO0	P_GPIO5	P_GPIO8	P_GPIO9	P_GPIO11	G
H	DDR_WEn	DDR_ACTn	DDR_A10	DDR_A1	DDR_A12		VDDQX_DDR	GND	GND	GND	GND	GND	GND	GND	VDDM_SN		P_GPIO2	P_GPIO1	P_GPIO6	P_GPIO7	P_GPIO12	P_GPIO13	H
J	DDR_CK1t	DDR_CK1c	DDR_A9	DDR_CKE1	GND		VDDQ_DDR	GND	VDDK1	VDDK1	VDDK1	VDDK1	VDDK1	GND	VDDM_PIO1		P_GPIO17	P_GPIO18	P_GPIO19	P_GPIO15	P_GPIO16	P_GPIO14	J
K	DDR_BG0	GND	DDR_A4	DDR_A13	DDR_CS1n		VDDQ_DDR	GND	VDDK1	VDDK1	VDDK1	VDDK1	VDDK1	GND	SD2_CAP		VCC33_LDO2	MC23	MC22	MC20	MC21	MC19	K
L	DDR_A2	DDR_A11	DDR_BA1	DDR_CKE0	DDR_A7		AVDD18_LDO_DDR	GND	VDDK1	VDDK1	VDDK	VDDK	VDDK1	GND	SD1_CAP	VDD18_SDSN	VCC33_LDO1	MC18	MC17	MC15	MC14	MC16	L
M	DDR_A5	GND	DDR_CASn	DDR_TEN	GND		VDDQX_DDR	GND	VDDK1	VDDK1	VDDK	VDDK	VDDK1	GND	VDD18_ADC		MC13	MC11	AD_IN1	AD_IN0	AD_IN3	AD_IN2	M
N	DDR_CK0t	DDR_CK0c	DDR_VREF	GND			VDDQ_DDR	GND	VDDK1	VDDK	VDDK	VDDK	VDDK	GND	VCC33_RTC		VDD18_VBAT	MC12	RESET#	PWR_EN2	XTAL_RTCO	XTAL_RTCI	N
P	GND	DDR_A8	DDR_BG1	DDR_ZQ_TEST			VDDQ_DDR	GND	GND	GND	GND	GND	GND	GND	AVDD18_MPLL	AVDD18_MPLL	PWR_SEQ1	PWR_SW3	PWR_SW4	PWR_SEQ0	PWR_SEQ2	PWR_EN3	P
R	DDR_A0	DDR_RESETn	DDR_RASn	DDR_CS0n			VDDQX_DDR	AVDD18_AU	AVDDK_DSI	AVDD18_HDMI_1	VCC33_LCD	VCC33_DIO	GND_ARMPLL	VCC33_STBC	AVDD18_U3	GND	VDD18_STBC	PWR_SW2	PWR_SW1	GND_MPLL	XTAL_SYSO	XTAL_SYSI	R
T	DDR_A6	DDR_BA0	GND	DDR0_DQU7/DQ11_A			AVDDK_DDR	AVDD18_AAD	AVDD18_DSI	AVDD18_HDMI_2	VCC33_LCD	VDD18_LD	AVDD18_ARMPLL	VCC33_U2	AVDD18_U2	AVDDK_U3	VDDK_STBC	STBC_PWR1	JTAG_TMS	TESTEN	STBC_RST	JTAG_TDO	T
U	GND	DDR0_DMLn/DQ3_A	DDR0_DQU5/DQ13_A	DDR0_DQU3/DQ10_A	DDR0_DQU1/DQ12_A	AUD_VCM				GND							STBC_PWR2	STBC_RSTO	STBC_PWR0	JTAG_TDI	JTAG_TCK	JTAG_TRST	U
V	DDR0_DQL1/DQ2_A	DDR0_DQL5/DQ1_A	DDR0_DQSUt/DQS1_t_A	DDR0_DQSUc/DQS1_c_A	GND	LCD1	LCD0	AGND_DSI	LCD3	LCD5	LCD7	LCD8	LCD10	LCD30	LCD29	HDMI_HPD	HDMI_I2C_SDA	HDMI_I2C_SCL	D_GPIO4	D_GPIO8	D_GPIO7	D_GPIO6	V
W	DDR0_DQL3/DMI0_A	GND	DDR0_DQL7/DQ0_A	DDR0_DQU6/DQ14_A	LINE_OUT_L	LCD2	DSI_D3P	DSI_D0P	LCD4	LCD6	HDMI_TX0N	LCD11	HDMI_TX2N	LCD26	LCD25	LCD27	LCD28	LCD23	D_GPIO1	USB3/SATA_TXP	D_GPIO0	D_GPIO5	W
Y	DDR0_DQSLt/DQS0_t_A	DDR0_DQSLc/DQS0_c_A	DDR0_DMUn/DQ15_A	DDR0_DQU0/DMI1_A	LINE_OUT_R	AGND_AUD	DSI_D3N	DSI_D0N	DSI_GPIO10	GND	HDMI_TX0P	GND	HDMI_TX2P	LCD13	LCD15	LCD24	LCD22	LCD21	GND	USB3/SATA_TXN	GND	D_GPIO2	Y
AA	DDR0_DQL2/DQ7_A	DDR0_DQL6/DQ6_A	DDR0_DQU2/DQ9_A	GND	MIC_L_INP	MIC_R_INP	DSI_D1P	DSI_CKP	DSI_D2P	HDMI_TXCN		HDMI_TX1N		LCD14	LCD16	LCD20	LCD18	USB2_DP1	USB2_DP0		USB3/SATA_RXP	D_GPIO3	AA
AB	GND	DDR0_DQL0/DQ5_A	DDR0_DQL4/DQ4_A	DDR0_DQU4/DQ8_A	MIC_L_INN	MIC_R_INN	DSI_D1N	DSI_CKN	DSI_D2N	HDMI_TXCP		HDMI_TX1P		LCD9	LCD12	LCD17	LCD19	USB2_DM1	USB2_DM0		USB3/SATA_RXN	GND	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Pin Configuration

1.

FC-CSP 437

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
A1	GND	F3	DDR1_DQU7/DQ10_B	L22	MC16	U20	JTAG_TDI
A2	DDR1_DQL2/DQ5_B	F4	DDR1_DQU3/DQ11_B	M1	DDR_A5	U21	JTAG_TCK
A3	DDR1_DQL6/DQ4_B	F5	DDR1_DQU1/DQ13_B	M2	GND	U22	JTAG_TRST
A4	DDR1_DQU4/DQ8_B	F7	ETP	M3	DDR_CASn	V1	DDR0_DQL1/DQ2_A
A5	MC10	F17	S_GPIO19	M4	DDR_TEN	V2	DDR0_DQL5/DQ1_A
A6	MC0	F18	S_GPIO26	M5	GND	V3	DDR0_DQSUt/DQS1_t_A
A7	P_GPO34	F19	S_GPIO25	M7	VDDQX_DDR	V4	DDR0_DQSUc/DQS1_c_A
A8	HSI1_D1P	F20	S_GPIO24	M8	GND	V5	GND
A9	HSI1_D3P	F21	P_GPIO4	M9	VDDK1	V6	LCD1
A10	HSI1_CK0P	F22	P_GPIO10	M10	VDDK1	V7	LCD0
A11	HSI1_D0P	G1	GND	M11	VDDK	V8	AGND_DSI
A12	HSI1_D2P	G2	DDR_A3	M12	VDDK	V9	LCD3
A13	HSI2_D7P	G3	DDR_ODT	M13	VDDK1	V10	LCD5
A14	HSI2_CK3P	G4	GND	M14	GND	V11	LCD7
A15	HSI2_CK2P	G5	DDR1_DQU5/DQ12_B	M15	VDD18_ADC	V12	LCD8
A16	HSI2_CK0P	G7	AVDDK_DDR	M17	MC13	V13	LCD10
A17	HSI2_CK1P	G8	VDDM_MC	M18	MC11	V14	LCD30
A18	HSI2_D3P	G9	VDD18_MCP2	M19	AD_IN1	V15	LCD29
A19	S_GPIO3	G10	VCC33_PIO2	M20	AD_IN0	V16	HDMI_HPD
A20	S_GPIO4	G11	AVDDK_HSI1	M21	AD_IN3	V17	HDMI_I2C_SDA
A21	S_GPIO7	G12	AVDD18_HSI1	M22	AD_IN2	V18	HDMI_I2C_SCL
A22	GND	G13	AVDD18_HSI2	N1	DDR_CK0t	V19	D_GPIO4
B1	DDR1_DQL0/DQ7_B	G14	AVDDK_HSI2	N2	DDR_CK0c	V20	D_GPIO8
B2	DDR1_DQL4/DQ6_B	G15	VDD18_SNP1	N3	DDR_VREF	V21	D_GPIO7
B3	DDR1_DQU6/DMI1_B	G17	P_GPIO3	N4	GND	V22	D_GPIO6
B4	GND	G18	P_GPIO0	N7	VDDQ_DDR	W1	DDR0_DQL3/DMI0_A
B5	MC9	G19	P_GPIO5	N8	GND	W2	GND
B6	MC1	G20	P_GPIO8	N9	VDDK1	W3	DDR0_DQL7/DQ0_A
B7	SYS_RSTO#	G21	P_GPIO9	N10	VDDK	W4	DDR0_DQU6/DQ14_A
B8	HSI1_D1N	G22	P_GPIO11	N11	VDDK	W5	LINE_OUT_L
B9	HSI1_D3N	H1	DDR_WEn	N12	VDDK	W6	LCD2
B10	HSI1_CK0N	H2	DDR_ACTn	N13	VDDK	W7	DSI_D3P
B11	HSI1_D0N	H3	DDR_A10	N14	GND	W8	DSI_D0P
B12	HSI1_D2N	H4	DDR_A1	N15	VCC33_RTC	W9	LCD4
B13	HSI2_D7N	H5	DDR_A12	N17	VDD18_VBAT	W10	LCD6
B14	HSI2_CK3N	H7	VDDQX_DDR	N18	MC12	W11	HDMI_TX0N
B15	HSI2_CK2N	H8	GND	N19	RESET#	W12	LCD11
B16	HSI2_CK0N	H9	GND	N20	PWR_EN2	W13	HDMI_TX2N
B17	HSI2_CK1N	H10	GND	N21	XTAL_RTCO	W14	LCD26
B18	HSI2_D3N	H11	GND	N22	XTAL_RTCI	W15	LCD25
B19	S_GPIO2	H12	GND	P1	GND	W16	LCD27
B20	S_GPIO5	H13	GND	P2	DDR_A8	W17	LCD28
B21	S_GPIO11	H14	GND	P3	DDR_BG1	W18	LCD23
B22	S_GPIO13	H15	VDDM_SN	P4	DDR_ZQ_TEST	W19	D_GPIO1
C1	DDR1_DQSLt/DQS0_t_B	H17	P_GPIO2	P7	VDDQ_DDR	W20	USB3/SATA_TXP
C2	DDR1_DQSLc/DQS0_c_B	H18	P_GPIO1	P8	GND	W21	D_GPIO0
C3	DDR1_DMUn/DQ14_B	H19	P_GPIO6	P9	GND	W22	D_GPIO5
C4	DDR1_DQU0/DQ15_B	H20	P_GPIO7	P10	GND	Y1	DDR0_DQSLt/DQS0_t_A
C5	MC8	H21	P_GPIO12	P11	GND	Y2	DDR0_DQSLc/DQS0_c_A
C6	MC2	H22	P_GPIO13	P12	GND	Y3	DDR0_DMUn/DQ15_A
C7	P_GPIO30	J1	DDR_CK1t	P13	GND	Y4	DDR0_DQU0/DMI1_A

C8	P_GPIO27	J2	DDR_CK1c	P14	GND	Y5	LINE_OUT_R
C9	P_GPIO24	J3	DDR_A9	P15	AVDD18_MPLL	Y6	AGND_AUD
C10	GND	J4	DDR_CKE1	P16	AVDD18_MPLL	Y7	DSI_D3N
C11	P_GPIO32	J5	GND	P17	PWR_SEQ1	Y8	DSI_D0N
C12	P_GPIO33	J7	VDDQ_DDR	P18	PWR_SW3	Y9	DSI_GPIO10
C13	HSI2_D6P	J8	GND	P19	PWR_SW4	Y10	GND
C14	HSI2_D5P	J9	VDDK1	P20	PWR_SEQ0	Y11	HDMI_TX0P
C15	HSI2_D4P	J10	VDDK1	P21	PWR_SEQ2	Y12	GND
C16	HSI2_D0P	J11	VDDK1	P22	PWR_EN3	Y13	HDMI_TX2P
C17	HSI2_D1P	J12	VDDK1	R1	DDR_A0	Y14	LCD13
C18	HSI2_D2P	J13	VDDK1	R2	DDR_RESETn	Y15	LCD15
C19	S_GPIO1	J14	GND	R3	DDR_RASn	Y16	LCD24
C20	S_GPIO6	J15	VDDM_PIO1	R4	DDR_CS0n	Y17	LCD22
C21	S_GPIO12	J17	P_GPIO17	R7	VDDQX_DDR	Y18	LCD21
C22	S_GPIO14	J18	P_GPIO18	R8	AVDD18_AU	Y19	GND
D1	DDR1_DQL7/DQ0_B	J19	P_GPIO19	R9	AVDDK_DSI	Y20	USB3/SATA_TXN
D2	GND	J20	P_GPIO15	R10	AVDD18_HDMI_1	Y21	GND
D3	DDR1_DQU2/DQ9_B	J21	P_GPIO16	R11	VCC33_LCD	Y22	D_GPIO2
D4	GND	J22	P_GPIO14	R12	VCC33_DIO	AA1	DDR0_DQL2/DQ7_A
D5	MC7	K1	DDR_BG0	R13	GND_ARMPLL	AA2	DDR0_DQL6/DQ6_A
D6	MC5	K2	GND	R14	VCC33_STBC	AA3	DDR0_DQU2/DQ9_A
D7	P_GPIO31	K3	DDR_A4	R15	AVDD18_U3	AA4	GND
D8	P_GPIO26	K4	DDR_A13	R16	GND	AA5	MIC_L_INP
D9	P_GPIO25	K5	DDR_CS1n	R17	VDD18_STBC	AA6	MIC_R_INP
D10	P_GPIO22	K7	VDDQ_DDR	R18	PWR_SW2	AA7	DSI_D1P
D11	P_GPIO20	K8	GND	R19	PWR_SW1	AA8	DSI_CKP
D12	P_GPIO21	K9	VDDK1	R20	GND_MPLL	AA9	DSI_D2P
D13	HSI2_D6N	K10	VDDK1	R21	XTAL_SYSO	AA10	HDMI_TXCN
D14	HSI2_D5N	K11	VDDK1	R22	XTAL_SYSI	AA12	HDMI_TX1N
D15	HSI2_D4N	K12	VDDK1	T1	DDR_A6	AA14	LCD14
D16	HSI2_D0N	K13	VDDK1	T2	DDR_BA0	AA15	LCD16
D17	HSI2_D1N	K14	GND	T3	GND	AA16	LCD20
D18	HSI2_D2N	K15	SD2_CAP	T4	DDR0_DQU7/DQ11_A	AA17	LCD18
D19	S_GPIO10	K17	VCC33_LDO2	T7	AVDDK_DDR	AA18	USB2_DP1
D20	S_GPIO17	K18	MC23	T8	AVDD18_AAD	AA19	USB2_DP0
D21	S_GPIO16	K19	MC22	T9	AVDD18_DSI	AA21	USB3/SATA_RXP
D22	S_GPIO15	K20	MC20	T10	AVDD18_HDMI_2	AA22	D_GPIO3
E1	DDR1_DQL1/DQ1_B	K21	MC21	T11	VCC33_LCD	AB1	GND
E2	DDR1_DMLn/DMI0_B	K22	MC19	T12	VDD18_LD	AB2	DDR0_DQL0/DQ5_A
E3	DDR1_DQSUt/DQS1_t_B	L1	DDR_A2	T13	AVDD18_ARMPLL	AB3	DDR0_DQL4/DQ4_A
E4	DDR1_DQSUc/DQS1_c_B	L2	DDR_A11	T14	VCC33_U2	AB4	DDR0_DQU4/DQ8_A
E5	MC6	L3	DDR_BA1	T15	AVDD18_U2	AB5	MIC_L_INN
E6	MC4	L4	DDR_CKE0	T16	AVDDK_U3	AB6	MIC_R_INN
E7	MC3	L5	DDR_A7	T17	VDDK_STBC	AB7	DSI_D1N
E8	P_GPIO29	L7	AVDD18_LDO_DDR	T18	STBC_PWR1	AB8	DSI_CKN
E9	P_GPIO28	L8	GND	T19	JTAG_TMS	AB9	DSI_D2N
E10	P_GPIO23	L9	VDDK1	T20	TESTEN	AB10	HDMI_TXCP
E11	HSI1_REXT	L10	VDDK1	T21	STBC_RST	AB12	HDMI_TX1P
E14	S_GPIO0	L11	VDDK	T22	JTAG_TDO	AB14	LCD9
E15	GND	L12	VDDK	U1	GND	AB15	LCD12
E16	S_GPIO8	L13	VDDK1	U2	DDR0_DMLn/DQ3_A	AB16	LCD17
E17	S_GPIO9	L14	GND	U3	DDR0_DQU5/DQ13_A	AB17	LCD19
E18	S_GPIO18	L15	SD1_CAP	U4	DDR0_DQU3/DQ10_A	AB18	USB2_DM1
E19	S_GPIO20	L16	VDD18_SDSN	U5	DDR0_DQU1/DQ12_A	AB19	USB2_DM0
E20	S_GPIO21	L17	VCC33_LDO1	U6	AUD_VCM	AB21	USB3/SATA_RXN
E21	S_GPIO22	L18	MC18	U10	GND	AB22	GND
E22	S_GPIO23	L19	MC17	U17	STBC_PWR2	U20	JTAG_TDI
F1	DDR1_DQL5/DQ3_B	L20	MC15	U18	STBC_RSTO	U21	JTAG_TCK
F2	DDR1_DQL3/DQ2_B	L21	MC14	U19	STBC_PWR0	U22	JTAG_TRST

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt input

I/OD = bi-directional port with open drain output and Schmitt input

mvI/O = multi voltage bi-direction port with Schmitt input

I/O_{18D} = 1.8V bi-directional port with Schmitt input

I/O_{5VT} = bi-directional port with normal driving/sinking and 5V tolerance input

I/O_{SD} = SD Card interface bi-direction port with different driving/sinking capability

HSIO = high speed serial interface with bi-directional port

LVD = low voltage detection function pin

p/u = internal pull-up

p/d = internal pull-down

AI = analogue input port

AO = analogue output port

AI/O = analogue bi-directional port

H = output high

L = output low

P = power or ground

Note: * means this pin has interrupted function.

2. NT98530 437 pins

Total:437 pins

2.1. System interface (10)

Pin No.	Name	Type	Reset	Descriptions
R22	XTAL_SYSI	AI	-	Crystal input for system oscillator. (12MHz)
R21	XTAL_SYSO	AO	-	Output for system oscillator
N19	RESET#	LVD	p/u	System Reset. Connect a capacitor to ground for reset time control.
B7	SYS_RSTO#	OD	OD	Reset signal output for peripheral.
T20	TESTEN	I	I p/d	Enable test mode. Keep low for normal operation.
U22	JTAG_TRST / D_GPIO[9]*	I/O_{18D}	I p/u	CPU's JTAG test interface
T19	JTAG_TMS / D_GPIO[10]*	I/O_{18D}	I p/d	
U21	JTAG_TCK / D_GPIO[11]*	I/O_{18D}	I p/d	
U20	JTAG_TDI / D_GPIO[12]*	I/O_{18D}	I p/d	
T22	JTAG_TDO / D_GPIO[13]*	I/O_{18D}	I p/d	

2.2. RTC & Power Button Controller (11)

Pin No.	Name	Type	Default	Descriptions
N22	XTAL_RTCI	AI	-	Crystal input for real time clock oscillator. (32.768KHz).
N21	XTAL_RTCO	AO	-	Output for real time clock oscillator.
R19	PWR_SW1	AI	I p/d	Power on/off signal input. (ON/OFF switch use)
R18	PWR_SW2#	AI	I p/u	Power on/off signal input. (falling edge trigger)
P18	PWR_SW3	AI	I p/d	Power on/off signal input.
P19	PWR_SW4	AI	I p/d	Power on/off signal input. (Battery in use)
P20	PWR_SEQ0	AO	-	Power enable signal output.
P17	PWR_SEQ1	AO	-	
P21	PWR_SEQ2	AO	-	
N20	PWR_EN2	AO	-	Power enable signal output.(DRAM self-refresh mode use)
P22	PWR_EN3	AO	-	Power enable signal output.(special WiFi mode use)

Note: If those PWR_SW pins aren't used, Novatek recommends each PWR_SW connect to default level by a resistor.

2.3. STBC (5)

Pin No.	Name	Type	Default	Descriptions

T21	STBC_RST#	I	p/u	Reset signal input for standby mode controller
U18	STBC_RSTO	OD	OD	Reset signal output of standby mode
U19	STBC_PWR0	IO_{18D}	p/d	Power enable signal output of standby mode
T18	STBC_PWR1	IO_{18D}	p/d	
U17	STBC_PWR2	IO_{18D}	p/d	

2.4. DRAM interface (79)

Pin No.	Name	Type	Reset	Descriptions
R1	DDR_A0	O	-	DRAM address bus
H4	DDR_A1	O	-	
L1	DDR_A2	O	-	
G2	DDR_A3	O	-	
K3	DDR_A4	O	-	
M1	DDR_A5	O	-	
T1	DDR_A6	O	-	
L5	DDR_A7	O	-	
P2	DDR_A8	O	-	
J3	DDR_A9	O	-	
H3	DDR_A10	O	-	
L2	DDR_A11	O	-	
H5	DDR_A12	O	-	
K4	DDR_A13	O	-	
R2	DDR_RESETn	O	-	DRAM reset signal output for the DDR4/LPDDR4
T2	DDR_BA0	O	-	DRAM Command signal output
L3	DDR_BA1	O	-	
H2	DDR_ACTn	O	-	
R4	DDR_CS0n	O	-	
K5	DDR_CS1n	O	-	
K1	DDR_BG0	O	-	
P3	DDR_BG1	O	-	
R3	DDR_RASn	O	-	
M3	DDR_CASn	O	-	
L4	DDR_CKE0	O	-	
J4	DDR_CKE1	O	-	
G3	DDR_ODT	O	-	
H1	DDR_WEn	O	-	
M4	DDR_TEN	O	-	
N3	DDR_VREF	AI	-	DDR PHY reference voltage input or test pin
P4	DDR_ZQ_TEST	AO	-	DDR PHY test pin
N2	DDR_CK0c	D I/O	-	DRAM differential clock output
N1	DDR_CK0t	D I/O	-	
J2	DDR_CK1c	D I/O	-	
J1	DDR_CK1t	D I/O	-	
Y2	DDR0_DQSLc/DQS0_c_A	D I/O	-	DRAM data strobe.
Y1	DDR0_DQSLt/DQS0_t_A	D I/O	-	
V4	DDR0_DQSUc/DQS1_c_A	D I/O	-	

V3	DDR0_DQSUt/DQS1_t_A	D I/O	-	
C2	DDR1_DQSLc/DQS0_c_B	D I/O	-	
C1	DDR1_DQSLt/DQS0_t_B	D I/O	-	
E4	DDR1_DQSUc/DQS1_c_B	D I/O	-	
E3	DDR1_DQSUt/DQS1_t_B	D I/O	-	
U2	DDR0_DMLn/DQ3_A	I/O	-	DRAM data bus input/output
Y3	DDR0_DMUn/DQ15_A	I/O	-	
E2	DDR1_DMLn/DMI0_B	I/O	-	
C3	DDR1_DMUn/DQ14_B	I/O	-	
AB2	DDR0_DQL0/DQ5_A	I/O	-	
V1	DDR0_DQL1/DQ2_A	I/O	-	
AA1	DDR0_DQL2/DQ7_A	I/O	-	
W1	DDR0_DQL3/DMI0_A	I/O	-	
AB3	DDR0_DQL4/DQ4_A	I/O	-	
V2	DDR0_DQL5/DQ1_A	I/O	-	
AA2	DDR0_DQL6/DQ6_A	I/O	-	
W3	DDR0_DQL7/DQ0_A	I/O	-	
Y4	DDR0_DQU0/DMI1_A	I/O	-	
U5	DDR0_DQU1/DQ12_A	I/O	-	
AA3	DDR0_DQU2/DQ9_A	I/O	-	
U4	DDR0_DQU3/DQ10_A	I/O	-	
AB4	DDR0_DQU4/DQ8_A	I/O	-	
U3	DDR0_DQU5/DQ13_A	I/O	-	
W4	DDR0_DQU6/DQ14_A	I/O	-	
T4	DDR0_DQU7/DQ11_A	I/O	-	
B1	DDR1_DQL0/DQ7_B	I/O	-	
E1	DDR1_DQL1/DQ1_B	I/O	-	
A2	DDR1_DQL2/DQ5_B	I/O	-	
F2	DDR1_DQL3/DQ2_B	I/O	-	
B2	DDR1_DQL4/DQ6_B	I/O	-	
F1	DDR1_DQL5/DQ3_B	I/O	-	
A3	DDR1_DQL6/DQ4_B	I/O	-	
D1	DDR1_DQL7/DQ0_B	I/O	-	
C4	DDR1_DQU0/DQ15_B	I/O	-	
F5	DDR1_DQU1/DQ13_B	I/O	-	
D3	DDR1_DQU2/DQ9_B	I/O	-	
F4	DDR1_DQU3/DQ11_B	I/O	-	
A4	DDR1_DQU4/DQ8_B	I/O	-	
G5	DDR1_DQU5/DQ12_B	I/O	-	
B3	DDR1_DQU6/DMI1_B	I/O	-	
F3	DDR1_DQU7/DQ10_B	I/O	-	

PIN name (DDR4)	LPDDR4	PIN name (DDR4)	LPDDR4	PIN name (DDR4)	LPDDR4
A0	A_CA5	DQS0c	A_DQS1c	DQ6	A_DQ8
A1	B_CA0	DQS0t	A_DQS1t	DQ7	A_DQ15
A2		DQS1c	A_DQS0c	DQ8	A_DQ5
A3	B_CA3	DQS1t	A_DQS0t	DQ9	A_DQ1
A4		DQS2c	B_DQS1c	DQ10	A_DQ4

A5		A_CA1		DQS2t		B_DQS1t		DQ11		A_DQ0	
A6				DQS3c		B_DQS0c		DQ12		A_DQ6	
A7		B_CA5		DQS3t		B_DQS0t		DQ13		A_DQ3	
A8				CS0n		A_CS0n		DQ14		A_DQ7	
A9		B_CA1		CS1n		B_CS0n		DQ15		A_DQ2	
A10				CK0c		A_CLKc		DQ16		B_DQ9	
A11				CK0t		A_CLKt		DQ17		B_DQ13	
A12		B_CS1		CK1c		B_CLKc		DQ18		B_DM1	
A13		B_CA4		CK1t		B_CLKt		DQ19		B_DQ12	
ACTn				RESETn		RESETn		DQ20		B_DQ8	
BA0		A_CA4		VREF		VREF		DQ21		B_DQ11	
BA1		A_CKE1		DM0		A_DQ12		DQ22		B_DQ10	
BG0				DM1		A_DM0		DQ23		B_DQ15	
BG1		A_CA2		DM2		B_DQ14		DQ24		B_DQ7	
RASn		A_CS1		DM3		B_DQ1		DQ25		B_DQ2	
CASn		A_CA3		DQ0		A_DQ9		DQ26		B_DQ0	
WEn		B_CKE1		DQ1		A_DQ11		DQ27		B_DQ5	
CKE0		A_CKE0		DQ2		A_DM1		DQ28		B_DQ6	
CKE1		B_CKE0		DQ3		A_DQ14		DQ29		B_DQ4	
TEN		A_CA0		DQ4		A_DQ10		DQ30		B_DM0	
ODT		B_CA2		DQ5		A_DQ13		DQ31		B_DQ3	

2.5. Sensor interface (62)

Pin No.	Name	Type	Reset	Descriptions
E11	HSI1_REXT	AI	-	
B11	HSI1_D0N	MIPI	I p/d	MIPI CSI D-PHY Transmitter
A11	HSI1_D0P			
B8	HSI1_D1N			
A8	HSI1_D1P			
B10	HSI1_CK0N			
A10	HSI1_CK0P			
B12	HSI1_D2N			
A12	HSI1_D2P			
B9	HSI1_D3N			
A9	HSI1_D3P			
D16	HSI2_D0N / HSI_GPIO0*	HSIO	I p/d	High speed differential sensor interface and parallel interface. (When sensor interface is configured as high speed differential sensor interface, the clock lane should be a dedicated differential lane. And each data lanes may be permuted in established group, refer to below table)
C16	HSI2_D0P / HSI_GPIO1*			
D17	HSI2_D1N / HSI_GPIO2*			
C17	HSI2_D1P / HSI_GPIO3*			
B16	HSI2_CK0N / HSI_GPIO4*			
A16	HSI2_CK0P / HSI_GPIO5*			
D18	HSI2_D2N / HSI_GPIO6*			
C18	HSI2_D2P / HSI_GPIO7*			
B18	HSI2_D3N /			

	HSI_GPIO8*			
A18	HSI2_D3P / HSI_GPIO9*			
B17	HSI2_CK1N / HSI_GPIO10*			
A17	HSI2_CK1P / HSI_GPIO11*			
D15	HSI2_D4N / HSI_GPIO12*	HSIO	I p/d	High speed differential sensor interface and parallel interface. (When sensor interface is configured as high speed differential sensor interface, the clock lane should be a dedicated differential lane. And each data lanes may be permuted in established group, refer to below table)
C15	HSI2_D4P / HSI_GPIO13*			
D14	HSI2_D5N / HSI_GPIO14*			
C14	HSI2_D5P / HSI_GPIO15*			
B15	HSI2_CK2N / HSI_GPIO16*			
A15	HSI2_CK2P / HSI_GPIO17*			
D13	HSI2_D6N / HSI_GPIO18*			
C13	HSI2_D6P / HSI_GPIO19*			
B13	HSI2_D7N / HSI_GPIO20*			
A13	HSI2_D7P / HSI_GPIO21*			
B14	HSI2_CK3N / HSI_GPIO22*			
A14	HSI2_CK3P / HSI_GPIO23*			
E14	SN1_MCLK / S_GPIO[0]*	mvI/O	I p/d	General Purpose IO (refer to below table)
C19	S_GPIO[1]*	mvI/O	I p/d	
B19	S_GPIO[2]*	mvI/O	I p/d	
A19	S_GPIO[3]*	mvI/O	I p/d	
A20	S_GPIO[4]*	mvI/O	I p/d	
B20	S_GPIO[5]*	mvI/O	I p/d	
C20	S_GPIO[6]*	mvI/O	I p/d	
A21	S_GPIO[7]*	mvI/O	I p/d	
E16	S_GPIO[8]*	mvI/O	I p/d	
E17	S_GPIO[9]*	mvI/O	I p/d	
D19	S_GPIO[10]*	mvI/O	I p/d	
B21	S_GPIO[11]*	mvI/O	I p/u	
C21	S_GPIO[12]*	mvI/O	I p/u	
B22	S_GPIO[13]*	mvI/O	I p/u	
C22	S_GPIO[14]*	mvI/O	I p/u	

D22	S_GPIO[15]*	mvI/O	I p/u	
D21	S_GPIO[16]*	mvI/O	I p/u	
D20	S_GPIO[17]*	mvI/O	I p/d	
E18	S_GPIO[18]*	mvI/O	I p/d	
F17	S_GPIO[19]*	mvI/O	I p/d	
E19	S_GPIO[20]*	mvI/O	I p/d	
E20	S_GPIO[21]*	mvI/O	I p/d	
E21	S_GPIO[22]*	mvI/O	I p/d	
E22	S_GPIO[23]*	mvI/O	I p/u	
F20	S_GPIO[24]*	mvI/O	I p/u	
F19	S_GPIO[25]*	mvI/O	I p/u	
F18	S_GPIO[26]*	mvI/O	I p/u	

Note1 : The mvI/O voltage of Sensor interface corresponds to VDDM_SN.

Pin Name	MIPI/LVDS/HiSPi (1C4Dx2)		MIPI / HiSPi (1C2Dx4)		LVDS (1C8D)		Parallel (RAW12)					
HSI_GPIO[0]	HSI_D0N	I	HSI2_D0N	I	LVDS_D0N	I	SN_D2	I				
HSI_GPIO[1]	HSI_D0P	I	HSI2_D0P	I	LVDS_D0P	I	SN_D3	I				
HSI_GPIO[2]	HSI_D1N	I	HSI2_D1N	I	LVDS_D1N	I	SN_D4	I				
HSI_GPIO[3]	HSI_D1P	I	HSI2_D1P	I	LVDS_D1P	I	SN_D5	I				
HSI_GPIO[4]	**HSI_CK0N**	I	**HSI2_CKN**	I	**LVDS_CKN**	I	SN_D6	I				
HSI_GPIO[5]	**HSI_CK0P**	I	**HSI2_CKP**	I	**LVDS_CKP**	I	SN_D7	I				
HSI_GPIO[6]	HSI_D2N	I	HSI3_D0N	I	LVDS_D2N	I	SN_D8	I				
HSI_GPIO[7]	HSI_D2P	I	HSI3_D0P	I	LVDS_D2P	I	SN_D9	I				
HSI_GPIO[8]	HSI_D3N	I	HSI3_D1N	I	LVDS_D3N	I	SN_D10	I				
HSI_GPIO[9]	HSI_D3P	I	HSI3_D1P	I	LVDS_D3P	I	SN_D11(MSB)	I				
HSI_GPIO[10]			**HSI3_CKN**	I			SN_D0	I				
HSI_GPIO[11]			**HSI3_CKP**	I			SN_D1(LSB)	I				
HSI_GPIO[12]	HSI_D0N	I	HSI4_D0N	I	LVDS_D4N	I						
HSI_GPIO[13]	HSI_D0P	I	HSI4_D0P	I	LVDS_D4P	I						
HSI_GPIO[14]	HSI_D1N	I	HSI4_D1N	I	LVDS_D5N	I						
HSI_GPIO[15]	HSI_D1P	I	HSI4_D1P	I	LVDS_D5P	I						
HSI_GPIO[16]	**HSI_CK0N**	I	**HSI4_CKN**	I								
HSI_GPIO[17]	**HSI_CK0P**	I	**HSI4_CKP**	I								
HSI_GPIO[18]	HSI_D2N	I	HSI5_D0N	I	LVDS_D6N	I						
HSI_GPIO[19]	HSI_D2P	I	HSI5_D0P	I	LVDS_D6P	I						
HSI_GPIO[20]	HSI_D3N	I	HSI5_D1N	I	LVDS_D7N	I						
HSI_GPIO[21]	HSI_D3P	I	HSI5_D1P	I	LVDS_D7P	I						
HSI_GPIO[22]			**HSI5_CKN**	I								
HSI_GPIO[23]			**HSI5_CKP**	I								

Pin Name	General Control Function						Parallel RAW12 (SIE 2)		CCIR 16 bits (SIE 2)		CCIR 8 bits x 2 (SIE 2)	
S_GPIO[0]	SN1_MCLK	O										
S_GPIO[1]	SN2_MCLK	O										
S_GPIO[2]	SN3_MCLK	O									CCIR8B_PXCLK	I
S_GPIO[3]							SN_PXCLK	I				
S_GPIO[4]					LVDS_VS(X)	I/O						
S_GPIO[5]					LVDS_HS(X)	I/O						
S_GPIO[6]							SN2_PXCLK	I	CCIR16_PXCLK	I	CCIR8A_PXCLK	I
S_GPIO[7]	I2C8_2_SCL	O					SN2_VS	I	CCIR16_VS(X)	I		
S_GPIO[8]	I2C8_2_SDA	I/O					SN2_HS	I	CCIR16_HS(X)	I		
S_GPIO[9]							SN2_D0	I	CCIR16_C0	I	CCIR8B_YC0	I
S_GPIO[10]							SN2_D1	I	CCIR16_C1	I	CCIR8B_YC1	I
S_GPIO[11]	I2C3_2_SCL	O			SIF2_2_CLK	O	SN2_D2	I	CCIR16_C2	I	CCIR8B_YC2	I
S_GPIO[12]	I2C3_2_SDA	I/O			SIF2_2_DAT	O	SN2_D3	I	CCIR16_C3	I	CCIR8B_YC3	I
S_GPIO[13]	I2C4_2_SCL	O			SIF3_2_CLK	O	SN2_D4	I	CCIR16_C4	I	CCIR8B_YC4	I
S_GPIO[14]	I2C4_2_SDA	I/O			SIF3_2_DAT	O	SN2_D5	I	CCIR16_C5	I	CCIR8B_YC5	I
S_GPIO[15]	I2C5_2_SCL	O			SIF2_2_CS	O	SN2_D6	I	CCIR16_C6	I	CCIR8B_YC6	I

S_GPIO[16]	I2C5_2_SDA	I/O			SIF3_2_CS	O	SN2_D7	I	CCIR16_C7	I	CCIR8B_YC7	I
S_GPIO[17]	SPI2_2_CLK	O					SN2_D8	I	CCIR16_Y0	I	CCIR8A_YC0	I
S_GPIO[18]	SPI2_2_CS	O					SN2_D9	I	CCIR16_Y1	I	CCIR8A_YC1	I
S_GPIO[19]	SPI2_2_DO	I/O					SN2_D10	I	CCIR16_Y2	I	CCIR8A_YC2	I
S_GPIO[20]	SPI2_2_DI	I/O					SN2_D11	I	CCIR16_Y3	I	CCIR8A_YC3	I
S_GPIO[21]			SN4_MCLK_1	O			SN2_PXCLK	I	CCIR16_Y4	I	CCIR8A_YC4	I
S_GPIO[22]			SN5_MCLK_1	O			SN2_VS	I	CCIR16_Y5	I	CCIR8A_YC5	I
S_GPIO[23]	I2C6_2_SCL	O			SIF4_2_CLK	O	SN2_HS	I	CCIR16_Y6	I	CCIR8A_YC6	I
S_GPIO[24]	I2C6_2_SDA	I/O			SIF4_2_DAT	O	SN2_D0	I	CCIR16_Y7	I	CCIR8A_YC7	I
S_GPIO[25]	I2C7_2_SCL	O	TRIG_IN_1	I	SIF4_2_CS	O						
S_GPIO[26]	I2C7_2_SDA	I/O	TRIG_OUT_1	O								

2.6. PWM and Peripheral I/O (35)

Pin No.	Name	Type	Reset	Descriptions
G18	P_GPIO[0]*	mvI/O	I p/d	
H18	P_GPIO[1]*	mvI/O	I p/d	
H17	P_GPIO[2]*	mvI/O	I p/d	
G17	P_GPIO[3]*	mvI/O	I p/d	
F21	P_GPIO[4]*	mvI/O	I p/d	
G19	P_GPIO[5]*	mvI/O	I p/d	
H19	P_GPIO[6]*	mvI/O	I p/d	
H20	P_GPIO[7]*	mvI/O	I p/d	
G20	P_GPIO[8]*	mvI/O	I p/d	
G21	P_GPIO[9]*	mvI/O	I p/d	
F22	P_GPIO[10]*	mvI/O	I p/d	
G22	P_GPIO[11]*	mvI/O	I p/d	
H21	P_GPIO[12]*	mvI/O	I p/u	
H22	P_GPIO[13]*	mvI/O	I p/u	
J22	P_GPIO[14]*	mvI/O	I p/u	
J20	P_GPIO[15]*	mvI/O	I p/u	
J21	P_GPIO[16]*	mvI/O	I p/u	General Purpose I/O (refer to below table)
J17	P_GPIO[17]*	mvI/O	I p/u	
J18	P_GPIO[18]*	mvI/O	I p/u	
J19	P_GPIO[19]*	mvI/O	I p/u	
D11	P_GPIO[20]*	I/O	I p/d	
D12	P_GPIO[21]*	I/O	I p/u	
D10	P_GPIO[22]*	I/O	I p/u	
E10	P_GPIO[23]*	I/O	I p/u	
C9	P_GPIO[24]*	I/O	I p/u	
D9	P_GPIO[25]*	I/O	I p/u	
D8	P_GPIO[26]*	I/O	I p/d	
C8	P_GPIO[27]*	I/O	I p/u	
E9	P_GPIO[28]*	I/O	I p/u	
E8	P_GPIO[29]*	I/O	I p/u	
C7	P_GPIO[30]*	I/O	I p/u	
D7	P_GPIO[31]*	I/O	I p/u	
C11	UART_TX	I/O_{5VT}	O	UART Transmit
C12	UART_RX	I/O_{5VT}	I p/u	UART Receive
A7	P_GPIO[34]	OD	OD	

Note1: The mvI/O voltage of P_GPIO0~19 interface corresponds to VDDM_PIO1.

Name	UART		PWM / I2C		SIF / SPI		Parallel RAW12 (SIE 3)		CCIR 16 bits (SIE 3)		CCIR 8 bits x 2 (SIE 3)	
P_GPIO[0]	UART9_1_TX	O	PWM0_1	O			SN3_D4	I	CCIR16_Y0	I	CCIR8A_YC0	I
P_GPIO[1]	UART9_1_RX	I	PWM1_1	O			SN3_D5	I	CCIR16_Y1	I	CCIR8A_YC1	I
P_GPIO[2]	UART9_1_RTS	O	PWM2_1	O			SN3_D6	I	CCIR16_Y2	I	CCIR8A_YC2	I
P_GPIO[3]	UART9_1_CTS	I	PWM3_1	O			SN3_D7	I	CCIR16_Y3	I	CCIR8A_YC3	I
P_GPIO[4]	UART8_1_TX	O	PWM4_1	O			SN3_D8	I	CCIR16_Y4	I	CCIR8A_YC4	I
P_GPIO[5]	UART8_1_RX	I	PWM5_1	O			SN3_D9	I	CCIR16_Y5	I	CCIR8A_YC5	I
P_GPIO[6]	UART8_1_RTS	O	PWM6_1	O			SN3_D10	I	CCIR16_Y6	I	CCIR8A_YC6	I
P_GPIO[7]	UART8_1_CTS	I	PWM7_1	O			SN3_D11	I	CCIR16_Y7	I	CCIR8A_YC7	I
P_GPIO[8]	UART7_1_TX	O	PWM8_1	O	SIF5_1_CLK	O	SN3_PXCLK	I	CCIR16_PCLK	I	CCIR8A_PCLK	I
P_GPIO[9]	UART7_1_RX	I	PWM9_1	O	SIF5_1_CS	O	SN3_VS	I	CCIR16_VS(X)	I		
P_GPIO[10]	UART7_1_RTS	O	PWM10_1	O	SIF5_1_DAT	O	SN3_HS	I	CCIR16_HS(X)	I		
P_GPIO[11]	UART7_1_CTS	I	PWM11_1	O			SN3_D0	I		I	CCIR8B_PCLK	I
P_GPIO[12]	UART6_1_TX	O	I2C3_1_SCL	IO	SPI1_1_CLK	O	SN3_D1	I	CCIR16_C0	I	CCIR8B_YC0	I
P_GPIO[13]	UART6_1_RX	I	I2C3_1_SDA	O	SPI1_1_CS	O	SN3_D2	I	CCIR16_C1	I	CCIR8B_YC1	I
P_GPIO[14]	UART6_1_RTS	O	I2C4_1_SCL	IO	SPI1_1_DO	IO	SN3_D3	I	CCIR16_C2	I	CCIR8B_YC2	I
P_GPIO[15]	UART6_1_CTS	I	I2C4_1_SDA	O	SPI1_1_DI	IO			CCIR16_C3	I	CCIR8B_YC3	I
P_GPIO[16]	UART5_1_TX	O	I2C5_1_SCL	IO	SPI2_1_CLK	O	SIF1_1_CLK	O	CCIR16_C4	I	CCIR8B_YC4	I
P_GPIO[17]	UART5_1_RX	I	I2C5_1_SDA	O	SPI2_1_CS	O	SIF1_1_CS	O	CCIR16_C5	I	CCIR8B_YC5	I
P_GPIO[18]	UART5_1_RTS	O	I2C6_1_SCL	IO	SPI2_1_DO	IO	SIF1_1_DAT	O	CCIR16_C6	I	CCIR8B_YC6	I
P_GPIO[19]	UART5_1_CTS	I	I2C6_1_SDA	O	SPI2_1_DI	IO			CCIR16_C7	I	CCIR8B_YC7	I
P_GPIO[20]	UART4_1_TX	O	I2C7_1_SCL	IO	SPI3_1_CLK	O	SIF2_1_CLK	O			SN5_MCLK_2	O
P_GPIO[21]	UART4_1_RX	I	I2C7_1_SDA	O	SPI3_1_CS	O	SIF2_1_CS	O	PICNT1	I		
P_GPIO[22]	UART4_1_RTS	O	I2C8_1_SCL	IO	SPI3_1_DO	IO	SIF2_1_DAT	O	PICNT2	I	RTC_DIV_OUT	O
P_GPIO[23]	UART4_1_CTS	I	I2C8_1_SDA	O	SPI3_1_DI	IO			PICNT3	I	RTC_EXT_CLK	I
P_GPIO[24]	UART3_1_TX	O	I2C9_1_SCL	IO	SPI4_1_CLK	O	SIF3_1_CLK	O	I2S_1_BCLK	IO		O
P_GPIO[25]	UART3_1_RX	I	I2C9_1_SDA	O	SPI4_1_CS	O	SIF3_1_CS	O	I2S_1_SYNC	IO	DMIC_1_DAT1	I
P_GPIO[26]	UART3_1_RTS	O	I2C10_1_SCL	IO	SPI4_1_DO	IO	SIF3_1_DAT	O	I2S_1_SDATAO	O	DMIC_1_CLK	O
P_GPIO[27]	UART3_1_CTS	I	I2C10_1_SDA	O	SPI4_1_DI	IO		I	I2S_1_SDATAI	I	DMIC_1_DAT0	I
P_GPIO[28]	UART2_1_RTS	O	I2C1_1_SCL	IO	SPI5_1_CLK	O	SIF4_1_CLK	O	I2S_1_MCLK	O		
P_GPIO[29]	UART2_1_CTS	I	I2C1_1_SDA	O	SPI5_1_CS	O	SIF4_1_CS	O				
P_GPIO[30]	UART2_1_TX	O	I2C2_1_SCL	IO	SPI5_1_DO	IO	SIF4_1_DAT	O				
P_GPIO[31]	UART2_1_RX	I	I2C2_1_SDA	O	SPI5_1_DI	IO						
P_GPIO[32]	UART1_TX	O										
P_GPIO[33]	UART1_RX	I										
P_GPIO[34]	DR_RST#	D										

2.7. Memory Card interface (26)

Pin No.	Name	Type	Reset	Descriptions
L15	SD1_CAP	P	-	Internal Supply Voltage decoupling for SDIO1 interface. (3.3/1.8V switchable, default 3.3V)
K15	SD2_CAP	P	-	Internal Supply Voltage decoupling for SDIO2 interface. (3.3/1.8V switchable, default 3.3V)
A6	MC0 / C_GPIO[0]*	mvI/O	I p/u	Memory Card interface (refer to below table)
B6	MC1 / C_GPIO[1]*	mvI/O	I p/u	
C6	MC2 / C_GPIO[2]*	mvI/O	I p/u	
E7	MC3 / C_GPIO[3]*	mvI/O	I p/u	

E6	MC4 / C_GPIO[4]*	mvI/O	I p/u	
D6	MC5 / C_GPIO[5]*	mvI/O	I p/u	
E5	MC6 / C_GPIO[6]*	mvI/O	I p/u	
D5	MC7 / C_GPIO[7]*	mvI/O	I p/u	
C5	MC8 / C_GPIO[8]*	mvI/O	I p/d	
B5	MC9 / C_GPIO[9]*	mvI/O	I p/u	
A5	MC10 / C_GPIO[10]*	mvI/O	I p/d	
M18	MC11 / C_GPIO[11]*	I/O_{SD}	I p/d	Memory Card interface (see below table)
N18	MC12 / C_GPIO[12]*	I/O_{SD}	I p/u	
M17	MC13 / C_GPIO[13]*	I/O_{SD}	I p/u	
L21	MC14 / C_GPIO[14]*	I/O_{SD}	I p/u	
L20	MC15 / C_GPIO[15]*	I/O_{SD}	I p/u	
L22	MC16 / C_GPIO[16]*	I/O_{SD}	I p/u	
L19	MC17 / C_GPIO[17]*	I/O_{SD}	I p/d	Memory Card interface (refer to below table)
L18	MC18 / C_GPIO[18]*	I/O_{SD}	I p/d	
K22	MC19 / C_GPIO[19]*	I/O_{SD}	I p/d	
K20	MC20 / C_GPIO[20]*	I/O_{SD}	I p/d	
K21	MC21 / C_GPIO[21]*	I/O_{SD}	I p/d	
K19	MC22 / C_GPIO[22]*	I/O_{SD}	I p/d	
K18	MC23 / C_GPIO[23]*	I/O_{18D}	I p/d	

Note1: The mvI/O voltage of MC0~10 corresponds to VDDM_MC.

Note2: The I/O_{SD} voltage of MC11~16 corresponds to SD1_CAP and MC17~22 corresponds to SD2_CAP. It could be switched between 3.3/1.8V by the register.

Memory card interface pinmux table

Name	SD/MMC/eMMC (BS*)		SPI flash(1~4 bits) (BS*)									
MC0	eMMC_D0	I/O	SPI_DO/D0	I/O								
MC1	eMMC_D1	I/O	SPI_DI/D1	I/O								
MC2	eMMC_D2	I/O	SPI_WP/D2	I/O								
MC3	eMMC_D3	I/O	SPI_HOLD/D3	I/O								
MC4	eMMC_D4	I/O										
MC5	eMMC_D5	I/O										
MC6	eMMC_D6	I/O										
MC7	eMMC_D7	I/O										
MC8	eMMC_CLK	O	SPI_CLK	O								
MC9	eMMC_CMD	I/O	SPI_CS0#	O								
MC10	eMMC_STROBE	I	SPI_CS1#	O								
Name	SD Card (BS*)											
MC11	SD_CLK	O										
MC12	SD_CMD	I/O										
MC13	SD_D0	I/O										
MC14	SD_D1	I/O										
MC15	SD_D2	I/O										
MC16	SD_D3	I/O										
Name	SDIO											
MC17	SDIO2_CLK	O										
MC18	SDIO2_CMD	I/O										
MC19	SDIO2_D0	I/O										
MC20	SDIO2_D1	I/O										
MC21	SDIO2_D2	I/O										
MC22	SDIO2_D3	I/O										

Note BS*: In general, it is a resident device. Please choose one of them as boot source(FW).

2.8. LCD interface (31)

Pin No.	Name	Type	Reset	Descriptions
V7	LCD0 / L_GPIO[0]* / BS0	I/O	I p/d	LCD Signal Bus (refer to below table) **BS3..0 : BOOT_SRC[3..0]** 0x0: SPI (NOR) 0x1: SDIO 0x2: SPI_NAND with on die ECC (2 kbytes) 0x3: SPI_NAND with BCH ECC (2 kbytes) 0x4: ETHERNET 0x5: USB high speed 0x6: SPI_NAND with on die ECC (4 kbytes) 0x7: Reserved 0x8: eMMC (4 bits data bus) 0x9: eMMC (8 bits data bus) 0xA: SPI_NAND with BCH ECC (4 kbytes) 0xB: USB full speed 0xC: UART Others: Reserved **BS4 : EJTAG_CH_SEL** 0: EJTAG_1 (DGPIO9~13) 1: EJTAG_2 (CGPIO2~3, PGPIO32~33)
V6	LCD1 / L_GPIO[1]* / BS1	I/O	I p/d	
W6	LCD2 / L_GPIO[2]* / BS2	I/O	I p/d	
V9	LCD3 / L_GPIO[3]* / BS3	I/O	I p/d	
W9	LCD4 / L_GPIO[4]* / BS4	I/O	I p/d	
V10	LCD5 / L_GPIO[5]* / BS6	I/O	I p/d	
W10	LCD6 / L_GPIO[6]* / BS12	I/O	I p/d	

V11	LCD7 / L_GPIO[7]* / BS5	I/O	I p/d	**BS5 : EJTAG_SEL** 0: GPIO (TRST, TMS, TCK, TDI, TDO are GPIO) 1: EJTAG (**EJTAG_CH_SEL** to JTAG on boot) **BS6 : MPLL_CLK_SEL** 0: MPLL clock output (From MPLL clock) 1: Bypass MPLL (From external clock P_GPIO[29])
V12	LCD8 / L_GPIO[8]* / BS13	I/O	I p/d	
AB14	LCD9 / L_GPIO[9]*	I/O	I p/d	
V13	LCD10 / L_GPIO[10]*	I/O	I p/d	
W12	LCD11 / L_GPIO[11]*	I/O	I p/d	
AB15	LCD12 / L_GPIO[12]*	I/O	I p/d	LCD Signal Bus (refer to below table) **BS9..8 : ETH_MODE_SEL** 0x0: RMII (refclk output mode) 0x1: RMII (refclk input mode) 0x2: RGMII 0x3: Reserved **BS11..10 : CPU_DEBUG_MODE_SEL** Enable NT98530 enters CPU debug mode. 2'b00: Normal mode Others: Debug mode **BS12：WDT_FAIL_RESET_FUNC** Enable WDT fail reset function. Enable this function can skip internal storage when internal storage boot failed. (boot from SPI nand/SPI nor /eMMC) 0: Enable 1: Disable **BS13 : VDDIO_SN_SEL** Select voltage of Sensor control/AHD input (SGPIO0~26) **BS14 : VDDIO_P1_SEL** Select voltage of Peripheral/AHD input (PGPIO0~19) **BS15 : VDDIO_SD3_SEL** Select voltage of SPI NAND/eMMC (CGPIO0~10) 0: 3.3V 1: 1.8V
Y14	LCD13 / L_GPIO[13]*	I/O	I p/d	
AA14	LCD14 / L_GPIO[14]*	I/O	I p/d	
Y15	LCD15 / L_GPIO[15]*	I/O	I p/d	
AA15	LCD16 / L_GPIO[16]*	I/O	I p/d	
AB16	LCD17 / L_GPIO[17]* / BS14	I/O	I p/d	
AA17	LCD18 / L_GPIO[18]*	I/O	I p/d	
AB17	LCD19 / L_GPIO[19]* / BS10	I/O	I p/d	
AA16	LCD20 / L_GPIO[20]* / BS11	I/O	I p/d	
Y18	LCD21 / L_GPIO[21]*	I/O	I p/d	
Y17	LCD22 / L_GPIO[22]* / BS8	I/O	I p/d	
W18	LCD23 / L_GPIO[23]* / BS9	I/O	I p/d	
Y16	LCD24 / L_GPIO[24]* / BS15	I/O	I p/d	
W14	LCD25 / L_GPIO[25]*	I/O	I p/d	
W15	LCD26 / L_GPIO[26]*	I/O	I p/d	

W16	LCD27 / L_GPIO[27]*	I/O	I p/u	
W17	LCD28 / L_GPIO[28]*	I/O	I p/d	
V15	LCD29 / L_GPIO[29]*	I/O	I p/d	
V14	LCD30 / L_GPIO[30]*	I/O	I p/u	

LCD interface pinmux table

Name	LCD / LCD2 (8 bits)		CCIR / RGB (16 bits)		RGB (24 bits)		MI Parallel		MI Serial / Parallel		RGMII	
LCD0	LCD_D0	O	CCIR_Y0	O	C0_0	O	CSTN_1_D0	I/O				
LCD1	LCD_D1	O	CCIR_Y1	O	C0_1	O	CSTN_1_D1	I/O				
LCD2	LCD_D2	O	CCIR_Y2	O	C0_2	O	CSTN_1_D2	I/O				
LCD3	LCD_D3	O	CCIR_Y3	O	C0_3	O	CSTN_1_D3	I/O			RGMII2_TX_CTL	O
LCD4	LCD_D4	O	CCIR_Y4	O	C0_4	O	CSTN_1_D4	I/O			RGMII2_TXD0	O
LCD5	LCD_D5	O	CCIR_Y5	O	C0_5	O	CSTN_1_D5	I/O	MI_1_SDO	I/O	RGMII2_TXD1	O
LCD6	LCD_D6	O	CCIR_Y6	O	C0_6	O	CSTN_1_D6	I/O	MI_1_SDI	I/O	RGMII2_TXD2	O
LCD7	LCD_D7	O	CCIR_Y7	O	C0_7	O	CSTN_1_D7	I/O	MI_1_SDIO	I/O	RGMII2_TXD3	O
LCD8	LCD_CLK	O	CCIR_CLK	O	DCLK	O	CSTN_1_CS	O	MI_1_CLK	O	RGMII2_TX_CLK	O
LCD9	LCD_VD	O	CCIR_VD	O	VD	O	CSTN_RS	O	MI_1_RS	O	RGMII2_RX_CLK	I
LCD10	LCD_HD	O	CCIR_HD	O	HD	O	CSTN_1_WR#	O	MI_1_CS	O	RGMII2_RX_CTL	I
LCD11	LCD_DE	O	CCIR_DE	O			CSTN_1_RD#	O	MI_1_TE	I	RGMII2_RXD0	I
LCD12			CCIR_C0	O	C1_0	O	CSTN_1_D8	I/O	CSTN_2_D0	I/O	RGMII2_RXD1	I
LCD13			CCIR_C1	O	C1_1	O	CSTN_1_D9	I/O	CSTN_2_D1	I/O	RGMII2_RXD2	I
LCD14			CCIR_C2	O	C1_2	O	CSTN_1_D10	I/O	CSTN_2_D2	I/O	RGMII2_RXD3	I
LCD15	LCD2_D0	O	CCIR_C3	O	C1_3	O	CSTN_1_D11	I/O	CSTN_2_D3	I/O	RGMII2_MDC	O
LCD16	LCD2_D1	O	CCIR_C4	O	C1_4	O	CSTN_1_D12	I/O	CSTN_2_D4	I/O	RGMII2_MDIO	I/O
LCD17	LCD2_D2	O	CCIR_C5	O	C1_5	O	CSTN_1_D13	I/O	CSTN_2_D5	I/O	PHY_CLK	O
LCD18	LCD2_D3	O	CCIR_C6	O	C1_6	O	CSTN_1_D14	I/O	CSTN_2_D6	I/O	PHY_RSTn	O
LCD19	LCD2_D4	O	CCIR_C7	O	C1_7	O	CSTN_1_D15	I/O	CSTN_2_D7	I/O	RGMII_TX_CTL	O
LCD20	LCD2_D5	O			C2_0	O	CSTN_1_D16	I/O	CSTN_2_D8	I/O	RGMII_TXD0	O
LCD21	LCD2_D6	O			C2_1	O	CSTN_1_D17	I/O	CSTN_2_CS	O	RGMII_TXD1	O
LCD22	LCD2_D7	O			C2_2	O	CSTN_1_TE	I	CSTN_2_RS	O	RGMII_TXD2	O
LCD23	LCD2_CLK	O			C2_3	O			CSTN_2_WR#	O	RGMII_TXD3	O
LCD24	LCD2_VD	O			C2_4	O			CSTN_2_RD#	O	RGMII_TX_CLK	O
LCD25	LCD2_HD	O			C2_5	O			CSTN_2_TE	I	RGMII_RX_CLK	I
LCD26	LCD2_DE	O			C2_6	O					RGMII_RX_CTL	I
LCD27					C2_7	O					RGMII_RXD0	I
LCD28											RGMII_RXD1	I
LCD29											RGMII_RXD2	I
LCD30											RGMII_RXD3	I

2.9. Dedicated I/O (9)

Pin No.	Name	Type	Reset	Descriptions
W21	DGPIO0*	I/O	I p/u	Dedicated IO (refer to below table)
W19	DGPIO1*	I/O	I p/u	
Y22	DGPIO2*	I/O	I p/d	
AA22	DGPIO3*	I/O	I p/d	
V19	DGPIO4*	I/O	I p/d	
W22	DGPIO5*	I/O	I p/d	
V22	DGPIO6*	I/O	I p/d	
V21	DGPIO7*	I/O	I p/d	

V20	DGPIO8*	I/O	I p/d	

Name	UART / LED		I2C / PWM / CLK		SPI		RGMII		RMII		Fucntion	
DGPIO0			I2C10_2_SCL	O							(SD1_CD)	I
DGPIO1			I2C10_2_SDA	IO							(SD1_WP)	I
DGPIO2			PWM4_2	O	SPI4_2_CLK	O						
DGPIO3			PWM5_2	O	SPI4_2_CS	O						
DGPIO4	SATA_LED	O	PWM6_2	O	SPI4_2_DO	IO						
DGPIO5	UART9_2_TX	O	PWM7_2	O	SPI4_2_DI	IO	RGMII_MDC	O	RMII_MDC	O	(SD2_CD)	I
DGPIO6	UART9_2_RX	I	SP_CLK_1	O			RGMII_MDIO	I/O	RMII_MDIO	I/O	(SD2_WP)	I
DGPIO7	UART9_2_RTS	O					ETH_25MHz	O	ETH_25MHz	O	(VBUSI)	I
DGPIO8	UART9_2_CTS	I					ETH_RESETn	O	ETH_RESETn	O	(VBUSI)	I

2.10. ADC interface (4)

Pin No.	Name	Type	Reset	Descriptions
M20	AD_IN0 / AGPIO0*	AIO	-	General ADC 0 Input with buffer General Purpose IO
M19	AD_IN1* / AGPIO1*	AIO	-	General ADC 1 Input with configurable trigger function General Purpose IO
M22	AD_IN2* / AGPIO2*	AIO	-	General ADC 2 Input with configurable trigger function General Purpose IO
M21	AD_IN3 / AGPIO3*	AIO	-	General ADC 3 Input with buffer General Purpose IO

2.11. Audio Codec(7)

Pin No.	Name	Type	Reset	Descriptions
U6	AUD_VCM	AO	-	Decoupling for audio codec reference voltage.
AA6	MIC_R_INP	AI	-	Right channel microphone differential input positive side.
AB6	MIC_R_INN	AI	-	Right channel microphone differential input negative side.
AA5	MIC_L_INP	AI	-	Left channel microphone differential input positive side.
AB5	MIC_L_INN	AI	-	Left channel microphone differential input negative side.
Y5	LINE_OUT_R	AO	-	Right channel Line output.
W5	LINE_OUT_L	AO	-	Left channel Line output.

2.12. HDMI (11)

Pin No.	Name	Type	Reset	Descriptions
AB10	HDMI_TXCP	AO	-	TMDS Low Voltage Differential Signal Output Clock
AA10	HDMI_TXCN			
Y11	HDMI_TX0P	AO	-	TMDS Low Voltage Differential Signal Output Data
W11	HDMI_TX0N			
AB12	HDMI_TX1P			
AA12	HDMI_TX1N			
Y13	HDMI_TX2P			
W13	HDMI_TX2N			
V17	DDC_SDA / P_GPIO[35]	I/OD_{5VT}	I p/u	Display Data Channel SDA. DDCSDA is 5V tolerance input.
V18	DDC_SCL /	I/OD_{5VT}	I p/u	Display Data Channel SCL. DDCSCL is 5V tolerance

	P_GPIO[36]			input.
V16	HDMI_PLUG / P_GPIO[37]*	I/O_{5VT}	I p/d	Hot Plug Detect. HOTPLUG is 5V tolerance input.

2.13. MIPI DSI (11)

Pin No.	Name	Type	Reset	Descriptions
AB9	DSI_D2N / DSI_GPIO0*	AIO	-	MIPI DSI or MIPI CSI differential data lane input / output
AA9	DSI_D2P / DSI_GPIO1*	AIO	-	
Y8	DSI_D0N / DSI_GPIO2*	AIO	-	
W8	DSI_D0P / DSI_GPIO3*	AIO	-	
AB8	DSI_CKN / DSI_GPIO4*	AIO	-	MIPI DSI or MIPI CSI differential clock lane output
AA8	DSI_CKP / DSI_GPIO5*	AIO	-	
AB7	DSI_D1N / DSI_GPIO6*	AIO	-	MIPI DSI or MIPI CSI differential data lane input / output
AA7	DSI_D1P / DSI_GPIO7*	AIO	-	
Y7	DSI_D3N / DSI_GPIO8*	AIO	-	
W7	DSI_D3P / DSI_GPIO9*	AIO	-	
Y9	DSI_GPIO10* / BS7	AIO	-	**BS7 : DSI_PROT_EN** Enable DSI function. 0: DSI PHY function disabled 1: DSI PHY function available

Name	MIPI DSI		MIPI CSI		Peripheral		UART / SIF					
DSI_GPIO0	DSI_D2N	O	CSI_D2N	O	SPI1_2_CLK	O	UART5_2_TX	O				
DSI_GPIO1	DSI_D2P	O	CSI_D2P	O	SPI1_2_CS	O	UART5_2_RX	I				
DSI_GPIO2	DSI_D0N	O	CSI_D0N	O	SPI1_2_DO	IO	UART5_2_RTS	O				
DSI_GPIO3	DSI_D0P	O	CSI_D0P	O	SPI1_2_DI	IO	UART5_2_CTS	I				
DSI_GPIO4	DSI_CKN	O	CSI_CKN	O	I2C4_3_SCL	O	UART6_2_TX	O				
DSI_GPIO5	DSI_CKP	O	CSI_CKP	O	I2C4_3_SDA	IO	UART6_2_RX	I				
DSI_GPIO6	DSI_D1N	O	CSI_D1N	O	PWM0_2	O	UART6_2_RTS	O				
DSI_GPIO7	DSI_D1P	O	CSI_D1P	O	PWM1_2	O	UART6_2_CTS	I				
DSI_GPIO8	DSI_D3N	O	CSI_D3N	O	PWM2_2	O	SIF0_3_CLK	O				
DSI_GPIO9	DSI_D3P	O	CSI_D3P	O	PWM3_2	O	SIF0_3_CS	O				
DSI_GPIO10	DSI_TE	I			SP_CLK2_1	O	SIF0_3_DAT	O				

2.14. USB device interface (8)

Pin No.	Name	Type	Reset	Descriptions
W20	USB3/SATA_TXP	AI/O	-	USB3.0 SS Differential Transmit Data Plus (TX+)
Y20	USB3/SATA_TXN	AI/O	-	USB3.0 SS Differential Transmit Data Minus (TX-)

AA21	USB3/SATA_RXP	AI/O	-	USB3.0 SS Differential Receive Data Plus (RX+)
AB21	USB3/SATA_RXN	AI/O	-	USB3.0 SS Differential Receive Data Minus (RX-)
AA19	USB2_DP0	AI/O	-	USB2.0 FS/HS Differential Data Plus (D+)
AB19	USB2_DM0	AI/O	-	USB2.0 FS/HS Differential Data Minus (D-)
AA18	USB2_DP1	AI/O	-	USB2.0 FS/HS Differential Data Plus (D+)
AB18	USB2_DM1	AI/O	-	USB2.0 FS/HS Differential Data Minus (D-)

2.15. Power (128)

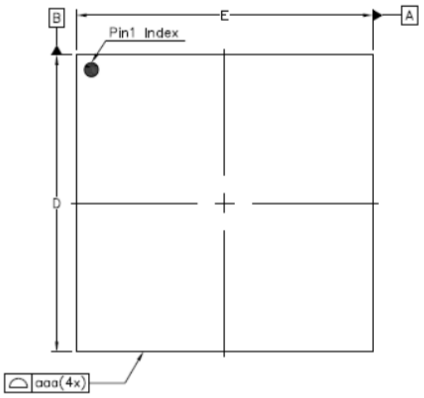
Pin No.	Name	Type	Descriptions
L11, L12, M11, M12, N10, N11, N12, N13	VDDK(8)	P	Core Power
J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, L9, L10, L13, M9, M10, M13, N9	VDDK1(17)	P	Core Power
G15	VDD18_SNP1	P	Digital 1.8V power for IO post driver
L16	VDD18_SDSN	P	Digital 1.8V power for IO post driver
G9	VDD18_MCP2	P	Digital 1.8V power for IO post driver
T12	VDD18_LD	P	Digital 1.8V power for IO post driver
R11, T11	VDDM_LCD(2)	P	Multi-level IO power for LCD interface
H15	VDDM_SN	P	Multi-level IO power for sensor interface
G8	VDDM_MC	P	Multi-level IO power for Memory Card
J15	VDDM_PIO1	P	Multi-level IO power for Peripheral
G10	VCC33_PIO2	P	3.3V IO power for Peripheral
L17	VCC33_LDO1	P	3.3V power for SD LDO
K17	VCC33_LDO2	P	3.3V power for SD LDO
R12	VCC33_DIO	P	General 3.3V I/O Power
A1, A22, B4, C10, D2, D4, E15, G1, G4, H8, H9, H10, H11, H12, H13, H14, J5, J8, J14, K2, K8, K14, L8, L14, M2, M5, M8, M14, N4, N8, N14, P1, P8, P9, P10, P11, P12, P13, P14, R16, T3, U1, U10, V5, W2, Y10, Y12, Y19, Y21, AA4, AB1, AB22	GND(52)	P	Digital Ground
N17	VDD18_VBAT	P	Battery input power for power button controller
N15	VCC33_RTC	P	RTC Power
T17	VDDK_STBC	P	Core Power for Power Management Controller
R17	VDD18_STBC	P	Digital 1.8V power for Power Management Controller

R14	VCC33_STBC	P	Digital 3.3V power for Power Management Controller
T13	AVDD18_ARMPLL	P	Analog 1.8V power for CPU PLL
R13	GND_ARMPLL	P	Ground for CPU PLL
P15, P16	AVDD18_MPLL	P	Analog 1.8V power for Multiple PLL
R20	GND_MPLL	P	Ground for Multiple PLL
G7, T7	AVDDK_DDR (2)	P	Analog core power for DDR PHY
J7, K7, N7, P7	VDDQ_DDR (4)	P	IO power for DDR4/LPDDR4/LPDDR4X
J7, K7, N7	VDDQX_DDR (3)	P	Low IO power for DDR4/LPDDR4/LPDDR4X
L7	AVDD18_LDO_DDR	P	Analog 1.8V power for DDR LDO
G11	AVDDK_HSI1	P	Analog core power for HSI PHY
G14	AVDDK_HSI2	P	Analog core power for HSI PHY
G12	AVDD18_HSI1	P	Analog 1.8V power for HSI Receiver
G13	AVDD18_HSI2	P	Analog 1.8V power for HSI Receiver
M15	VDD18_ADC	P	Digital 1.8V power for General Purpose ADC
T8	AVDD18_AAD	P	Analog 1.8V power for Audio ADC
R8	AVDD18_AU	P	Analog 1.8V power for Audio DAC
Y6	AGND_AUD	P	Ground for Audio Codec
R10	AVDD18_HDMI_1	P	Analog 1.8V power for HDMI Transmitter
T10	AVDD18_HDMI_2	P	Analog 1.8V power for HDMI Transmitter
R9	AVDDK_DSI	P	Analog core power for MIPI DSI circuit
T9	AVDD18_DSI	P	Analog 1.8V power for MIPI DSI Transmitter
V8	AGND_DSI	P	Ground for DSI
T15	AVDD18_U2	P	Analog 1.8V power for USB 2.0 interface
T14	VCC33_U2	P	3.3V power for USB 2.0 interface
T16	AVDDK_U3	P	Analog core power for USB 3.0 circuit
R15	AVDD18_U3	P	Analog 1.8V power for USB 3.0 interface
F7	ETP	-	Connected 100K Ohm resistor to ground

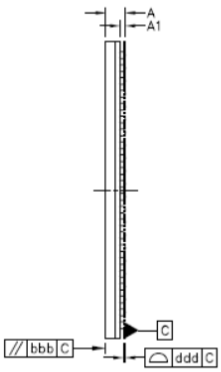
Package Information

3.

FC-CSP-437, 15 x 15 mm^2

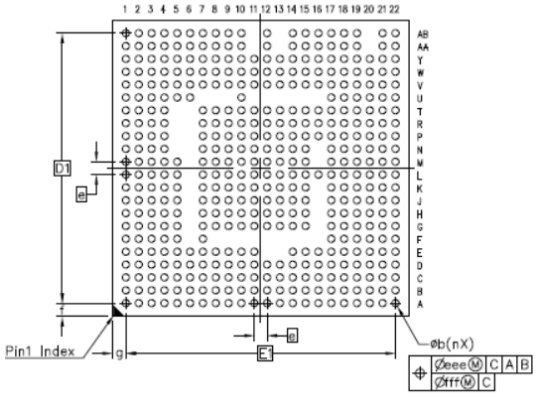


Top View



Side View

	Axis	Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Body Size:	X	E	14.90	15.00	15.10
	Y	D	14.90	15.00	15.10
Ball Pitch:		e		0.65	
Total Thickness:		A	---	---	1.20
Mold Thickness:			0.425	0.450	0.475
Substrate Thickness:			0.234	0.264	0.294
Ball Diameter:				0.35	
Stand Off:		A1	0.23	0.28	0.33
Ball Width:		b	0.31	0.36	0.41
Package Edge Tolerance:		aaa		0.1	
Mold Flatness:		bbb		0.15	
Coplanarity:		ddd		0.1	
Ball Offset (Package):		eee		0.15	
Ball Offset (Ball):		fff		0.08	
Ball Count:		n		437	
Edge Ball Center to Center:	X	E1		13.65	
	Y	D1		13.65	
Edge Ball Center to Package Edge:	X	g		0.675 Ref.	
	Y	f		0.675 Ref.	



Bottom View

Important Notice

NT98530 is a product that is not specifically designed and marketed, and shall not be directly and/or knowingly sold or used as to be incorporated into, any of the following products:

(i) military products or proliferation application (including but not limited to missiles, nuclear, chemical and biological weapons); or

(ii) commercial space products or applications that are controlled under the U.S. Munitions List (USML); or

(iii) medical appliances; and

(iv) automotive driver safety assistant system

furthermore, NT98530 shall not be directly and knowingly shipped to any country subject to "embargo" or exported to, re-exported to, transferred to, or used by any restricted entity, including but not limited to those listed on the U.S. Department of Commerce Entity List, under the U.S. laws and or its applicable regulations (e.g., the U.S. Export Administration Regulations) in effect from time to time.