

Digital System Fundamental

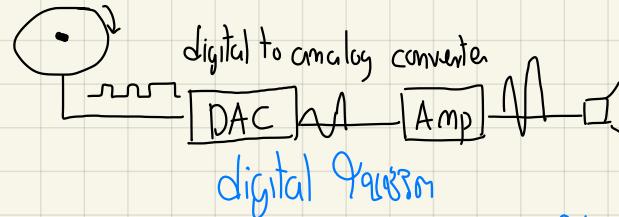
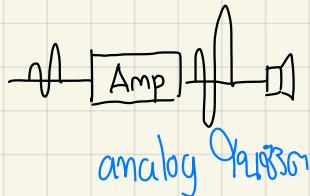
Introduction to digital system

analog and digital quantities

- ↳ សម្រាប់ analog & digital "សម្រាប់"
- ↳ analog និង digital noise នៅក្នុងបន្ទាន់
- ↳ digital តាមដែលបានបង្កើតឡើង និងចំណេះដឹង
- ↳

នីមួយៗ?

(a) digital life



↳ មនុសា គឺសែន្យា សែន្យា + ADC → digital system → + DAC → ភាពខ្លួន

↳ digital ឬជាស៊ូលិក analog តាមដឹកនាំបានបង្កើតឡើង

↳ ADC DAC noise

↳ ថាមធម៌ទិន្នន័យ x-ray នៅវិធាននៃរឿងឱ្យបាន analog

↳ ពេន្ធគម្មិតិយោប់ និងពេន្ធតុលាជាផ្ទៃ (ឯកសារ image processing)

↳ ការប្រើប្រាស់ ឬ matrix

↳ បានក្រឡាយចិញ្ញា → ឲ្យបាន digital

↳ ទូទៅដែលកំបងចាំនាមួយ

↳ សេដ្ឋកិច្ច ឬ ឈើសេដ្ឋកិច្ច

Binary Digits

↳ ឯកសារ ធម៌ទិន្នន័យ និងការប្រើប្រាស់

Logic level

↳ Logic High → ចំណាំលុយលក្ខណ៍និងការប្រើប្រាស់
↳ Logic Low → មិនចំណាំលុយលក្ខណ៍និងការប្រើប្រាស់

កំណត់ត្រាគារពេញលេញបាន

digital waveform → និងកំណត់ត្រាគារ logic នៅក្នុង

"កំណត់ត្រាគារ" (periodic)

Ideal pulses = signal such as square wave.

↳ មិនចំណាំលុយលក្ខណ៍និងការប្រើប្រាស់

↳ Duty cycle = $\frac{\text{ពេលវេលាដែលបានប្រើ}}{\text{ពេលវេលាតូលេខ}} \times 100\%$

↳ ទូទៅបានប្រើប្រាស់ motor ការងារការងារ

រហូត (មិន) + ក្នុងក្នុង (មិន) → ផ្លូវការ

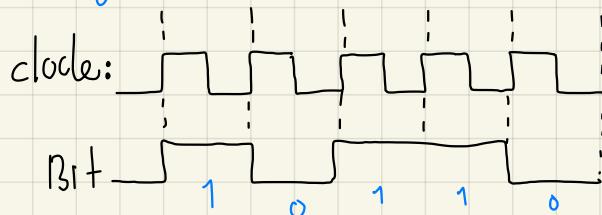
nonperiodic

ໄວ້ອານ

 period ?
 frequency ?
 duty cycle ?

$T = 10 \text{ s}$ #ອຸດກະກຸບ
 $f = \frac{1}{T} = 0.1 \text{ Hz}$
 duty cycle = $\frac{1}{10} = 0.1 = 10\%$

A digital Waveform Carries Binary



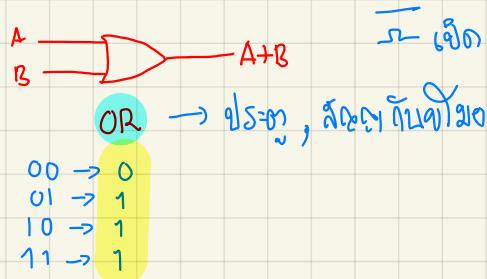
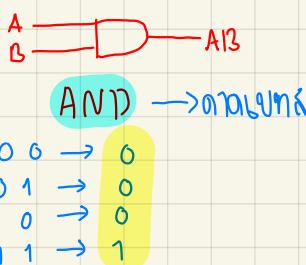
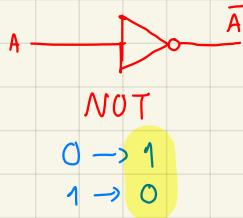
- ↳ timing diagram
- ↳ ເລີ່ມຕົ້ນທີ່ມີຄວາມສໍາເລັດຂອງຕົ້ນທີ່ມີຄວາມສໍາເລັດ

ສູງລາຍລະອຽດ periodic

- ↳ ດາວໂຫຼນຈະມີຄວາມສໍາເລັດກັບ clock
- ↳ ກາງສິ່ງແລ້ວ synchronized

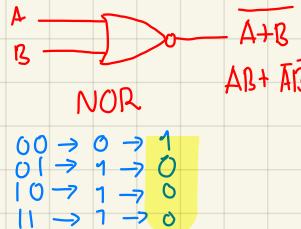
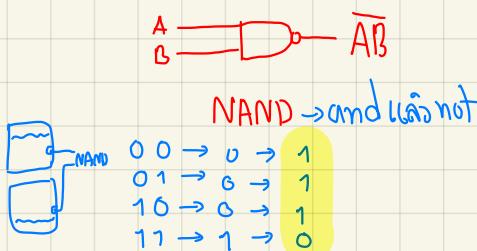
Basic Logic Operation → Logic Gate

- ↳ ລັບຮັດເອົາໃຫຍ່ໂລກໂດຍຕາ logic gate ອັນນີ້ສໍາມາດອະນຸມາດ computer

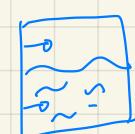
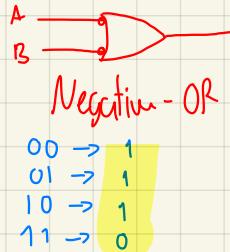
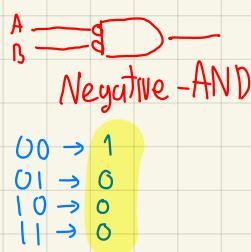
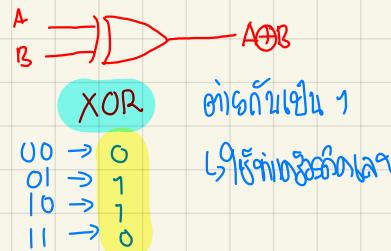


—
— ເກືດ

↳ ອີເຕີຕົກມີ 1's complement



$\overline{AB} + \overline{AB}$



↳ ດັວນດີ່ນທີ່ມີຄວາມສໍາເລັດໃນ IC (ເຊື່ອມວິວແລ້ວ)

IC 74XX

↳ ອີເຕີຕົກມີ gate 4 gate ພົມຕົວກັນ

↳ ໂດຍສິ່ງແລ້ວຕະຫຼາດກົງຫາ

“ຕ່າວ IC ເຮັດກົງຫາແດ່”

$$A(\bar{A} + B)$$

$$A + A\bar{B} = A$$

$$A + \bar{A}B = A + B$$

$$(A+B)(A+C) = A+BC$$

$$(\bar{A} + \bar{B} + \bar{C} + \bar{D})(\bar{A} + \bar{B} + \bar{C} + D)(\bar{A} + \bar{B} + C + D)(\bar{A} + \bar{B} + \bar{C} + \bar{D})$$

$$(\bar{A} + B + C + \bar{D})(\bar{A} + B + C + D)(A + \bar{B} + \bar{C} + \bar{D})(A + \bar{B} + C + \bar{D})(A + \bar{B} + C + D)$$

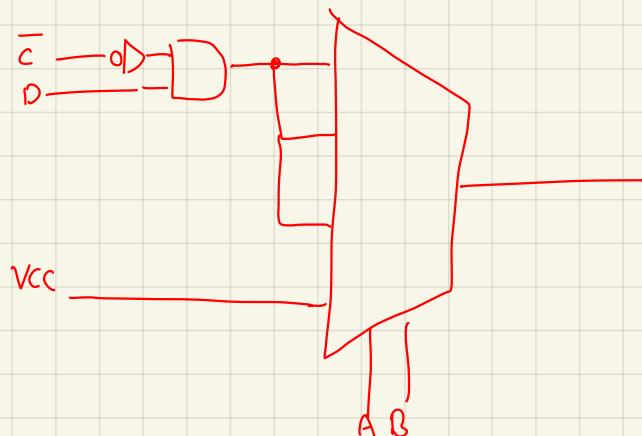
$$\begin{array}{l} \cancel{\bar{A} + AB + AC + AD + \bar{B}\bar{A}} + \cancel{\bar{B} + \bar{B}\bar{C} + \bar{B}\bar{D}} \\ \cancel{\bar{A} - \bar{A}(\bar{C} + D)} \quad \cancel{\bar{B}(\bar{A} + 0)} \\ (\bar{A} + \bar{B}) \end{array}$$

$$\begin{array}{l} \cancel{\bar{A} + \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}\bar{C} + \bar{A}\bar{D}} + \cancel{\bar{B} + \bar{B}\bar{C} + \bar{B}\bar{D}} \\ \cancel{\bar{A}} \quad \cancel{\bar{A}} \\ A + \bar{B}\bar{C} + \bar{B}\bar{D} \end{array}$$

$$\begin{array}{l} \cancel{\bar{A} + \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}\bar{D} + \bar{B}\bar{A} + \bar{B} + \bar{B}\bar{C} + \bar{B}\bar{D}} \\ \cancel{\bar{A} - \bar{A}(\bar{C} + D)} \quad \cancel{\bar{B}(\bar{A} + 0)} \\ (\bar{A} + \bar{B}) \end{array}$$

$$\bar{A}\bar{A} + \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}\bar{D} + \bar{B}\bar{C}\bar{A} + \bar{B}\bar{C}\bar{B} + \bar{B}\bar{C}\bar{B} + \bar{B}\bar{C}$$

A	B	C	D	AB	CD	+
0	0	0	0	0	0	0
0	1	0	0	0	1	1
1	0	0	0	0	0	0
1	1	0	0	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1
1	1	1	1	1	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1
1	1	1	1	1	0	1
1	1	1	1	1	1	1



Basic Logic Function

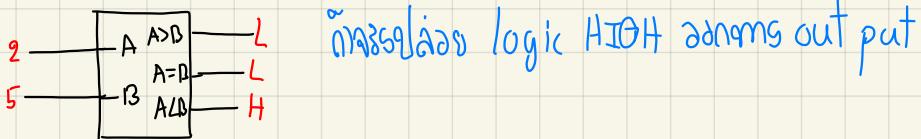
→ มาตราสัมบูรณ์ 2 → ฐาน 10
→ code = binary code

↳ the comparison function, arithmetic function, code conversion function, encoding function, decoding function, data selection function, storage function, counting function

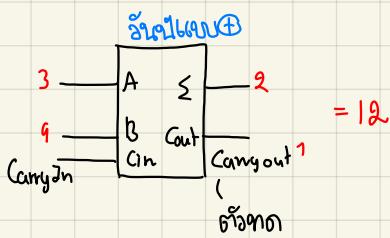
↳ ក្រសួងពិនិត្យ
↳ មនោត remote
↳ ផ្លូវបាយជាពាណិជ្ជកម្ម

ចំណាំលើកដែល
↳ 2 register រាយ

↳ overview comparison function



↳ overview arithmetic function

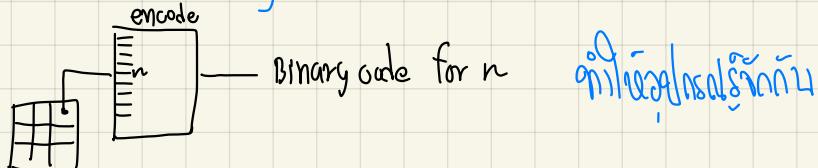


↳ overview code conversion function

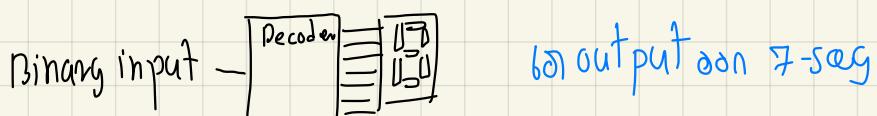
0000
0001
0010
0011
⋮

gate ឲ្យបានទិន្នន័យ

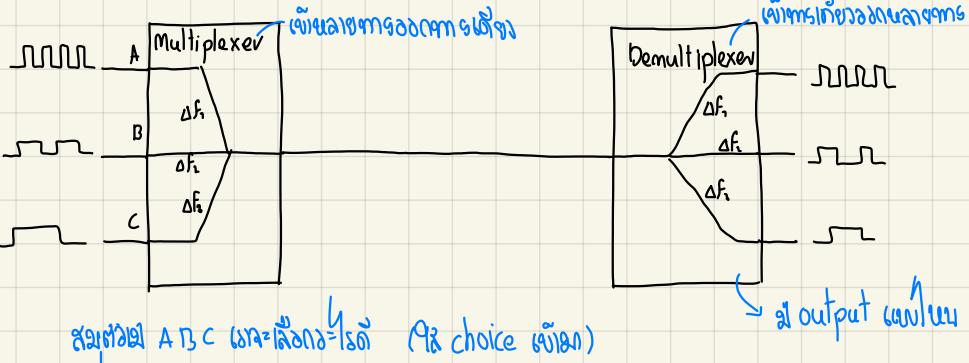
↳ overview encoding function



↳ overview decoding function



↳ overview data selection function



↳ overview storage function

↳ ຂາຍຕົກເລີນຈຳລັງ

↳ ຕິດຂອງ flip-flops, register ຈູລັງ

↳ ສິ່ງເຄີຍໄດ້ຢ່າງ serial, parallel

↳ ດັ່ງນີ້ຈະ

↳ ຂົດຕົກເລີນ

↳ ອົບຕົກເລີນ ram, register

↳ (ຊາຍ) hardware, software ພົມພວມໂຄສະນາ

↳ overview counting function

↳ ການປັບປຸງກາຍ



↳ truth table ເຊື້ອນ

Boolean Algebra & Logic Simplification

↳ ບັນຫາສອນໃຫຍ່ boolean ອະນະເກມນາ (ແກ່ຕົກເລີນໃຫຍ່ລວມທຸລະກຳ (sum-of-products) (SOP))

↳ boolean algebra ອົດດົດຕະນະໃຫຍ່ໂຄສະນາ (digital)

Law and Rule of Boolean algebra

↳ Commutative Laws (ຮຽນສະລັບ)

$$A+B = B+A$$

$$AB = BA$$

↳ Associate Law (ຮຽນປະຕິຫຼາກຂຶ້ນ)

$$A + (B+C) = (A+B)+C$$

$$A(BC) = (AB)C$$

↳ Distribute Law (ຮຽນນັດວຽກ)

$$A(B+C) = AB+AC$$

↳ De Morgan's Theorems

$$\overline{xy} = \overline{x} + \overline{y}$$

$$\text{NAND} \equiv \text{Neg-OR}$$

$$\overline{x+y} = \overline{xy}$$

$$\text{NOR} \equiv \text{Neg-AND}$$

Rule 1. $A+O = A$

2. $A+1 = 1$

3. $AO = O$

4. $A1 = A$

5. $A+A = A$

6. $A+\bar{A} = 1$

7. $A \cdot A = A$

8. $A \cdot \bar{A} = O$

9. $\bar{\bar{A}} = A$

10. $A + AB = A$

11. $A + \bar{A}B = A+B$

12. $(A+B)(A+C) = A+BC$

$$\bar{B} + \bar{A} + AB = \bar{A} + B$$

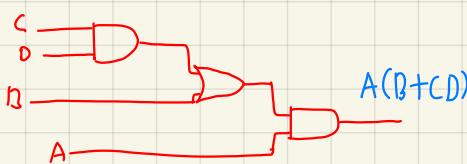
ມີກຳນົດກຳນົດກຳນົດ
ກຳນົດ $\bar{A} \rightarrow A=1$ (1)
ກຳນົດ $A \rightarrow AB=0$ (0)

$$\begin{aligned} & AA + AC + AB + BC \\ & A + AC + AB + BC \\ & A(1+C) + AB + BC \\ & A + AB + BC \\ & A(1+B) + BC \\ & A + BC \end{aligned}$$

$$\begin{aligned} & (A+AB) + (\bar{A}B) \\ & (AA+AB) + (\bar{A}B) \\ & AA + AB + \bar{A}\bar{B} + \bar{A}B \\ & (A+\bar{A})(B+\bar{B}) \\ & 1 \cdot (A+B) \\ & A+B \end{aligned}$$

Boolean Analysis of Logic Circuit

↳ ຂາຍຕົກເລີນ



$$\begin{aligned} A+AB &= A \\ A+\bar{A}B &= A+B \\ \bar{A}+AB &= \bar{A}+B \\ (A+B)(A+C) &= A+BC \end{aligned}$$

$A(B+C)$ ឲ្យបានត្រង់ដោយ? វិធានរបស់យុខ (នៅក្បាន់)

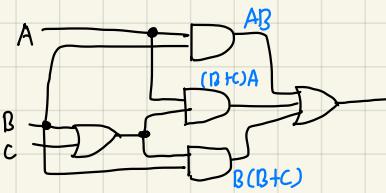
$$A=1 \quad (B+C) = 1$$

!! !!

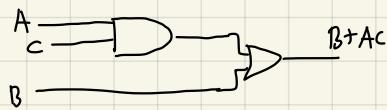
$$\begin{aligned} B+C &= 1+0 \\ B+C &= 0+1 \\ B+C &= 1+1 \end{aligned}$$

Simplification using Boolean Algebra

↳ នីមួយៗនឹងការសារ



$$\begin{aligned} \text{output} &= A\bar{B} + A(B+C) + \bar{B}(B+C) \\ &= A\bar{B} + AB + AC + BB + BC \\ &= A\bar{B} + AC + B + BC \\ &= A\bar{B} + A(C+B(1+C)) \\ &= A\bar{B} + AC + B \\ &= \cancel{B+AB} + AC \\ &= B + AC \end{aligned}$$



ការគណនោ

(propagation time រឿង
ស្ថាបន្ទាត់នូវឯកសារ)

↳ រួមចំណាំទៅលើ Boolean expression

↳ The sum of product form (SOP) \Rightarrow ឯកសារ = 1

↳ ធម្មតាសម្រាក នូវសម្រាកសម្រាក $\text{ex } ABC + BCD + ABD$

↳ ឯកសារមួយនៃការសារ SOP # និង distributive law

↳ ឯកសារមួយនៃការសារ និង ឯកសារមួយនៃការសារ $\text{ex } (A+B)(B+C+D)$ នឹង and or || hand arrangement

↳ Standard SOP

↳ ឯកសារ ឱ្យក្នុង ឯកសារមួយនៃការសារ

នៅនេះ $A\bar{B}C + (\bar{A}\bar{B} + A\bar{B}\bar{C}D)$ និង $\bar{A}\bar{B}(C+\bar{C})$ ជាមួយក្នុង possible តាមរបៀប

$= A\bar{B}\bar{C}(D+\bar{D})$ $\bar{A}\bar{B}(C+\bar{C})$

$\bar{A}\bar{B}CD + A\bar{B}\bar{C}\bar{D}$ $\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

$\bar{A}\bar{B}\bar{C}(D+\bar{D}) + \bar{A}\bar{B}\bar{C}(D+\bar{D})$ $\bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}$

សម្រាកមួយនៃការសារ និង ឯកសារមួយនៃការសារ

តាមរឿង (A+F) (F+G) = F(F+G) = F

និង and or

$$XX = XX$$

↳ The product of sum form (POS) \Rightarrow ឯកសារ = 0

↳ ឯកសារមួយនៃការសារ

↳ ឯកសារ OR ឬ AND

$$\text{ex. } (A+B)(A+\bar{B}+C) \# \text{non standard POS}$$

↳ standard POS

↳ ឯកសារ ឱ្យក្នុង ឯកសារមួយនៃការសារ

$$(A+B)(A+B+C) \# \text{ឯកសារមួយនៃការសារ}$$

$$A+B+C\bar{C}$$

$$(A+B+C)(A+B+\bar{C})$$

$$\begin{aligned} AA + AB + A\bar{C} + AB + B\bar{B} + B\bar{C} + AC + B\bar{C} + C\bar{C} \\ A\bar{A} + A\bar{B} + A\bar{C} + A\bar{B} + B\bar{A} + B\bar{C} + AC + BC \\ A + B + C(A+B) = (A+B)(1+C) = (A+B)(1) \end{aligned}$$

តាមរឿង (A\bar{A}) នឹង ឯកសារ ឬ ឯកសារ
(F\bar{F}) ឯកសារ = ឯកសារ OR

$$X + X + O = XX$$

↳ မြန်း POS ပုံစံ SOP ပုံစံ (standard)

ဒိုက္ခနီး truth table အာ

0	0	0	=	0
0	0	1	=	0
0	1	0	=	0
0	1	1	=	1
1	0	0	=	1
1	0	1	=	0
1	1	0	=	1
1	1	1	=	1

လေယာဉ်တွင် POS ပုံစံ \Rightarrow အပါး output 1

$$\begin{array}{c} 0 \quad 1 \quad 1 \\ / \quad 0 \quad 0 \\ / \quad 1 \quad 0 \\ / \quad 1 \quad 1 \end{array} \left. \begin{array}{l} \\ \\ \end{array} \right\} \text{ဒါ 4 ဂို့} \Rightarrow \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$$

လေယာဉ်တွင် POS \Rightarrow အပါး output 0

$$\begin{array}{c} 0 \quad 0 \quad 0 \\ 0 \quad 0 \quad 1 \\ 0 \quad 1 \quad 0 \\ 1 \quad 0 \quad 1 \end{array} \left. \begin{array}{l} \\ \\ \end{array} \right\} \text{Product} \quad (A+D+C)(A+B+\bar{C})(A+\bar{B}+C)(\bar{A}+B+\bar{C})$$

POS ပုံစံ 1 မှတ် ပုံစံ

↳ The Karnaugh Map (K-Map)

↳ မြန်းဆုံးအတွက် (faster than laws and rule)

↳ မြန်း 3, 4 မိုက် (3 or 4 input)

↳ ABIC

most sig least sig

AB	C	0	1
00			
01			
10			

မြန်းများ 0 မှတ် ပုံစံ

AB	C	0	1
00	$\bar{A}\bar{B}C$	$\bar{A}B\bar{C}$	
01	$\bar{A}B\bar{C}$		$A\bar{B}C$
10		$A\bar{B}C$	$A\bar{B}\bar{C}$

ဒိုက္ခနီး standard

ဒိုက္ခနီးပုံစံများ $\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$

② SOP \rightarrow ဆိုင် 1 | $001 + 010 + 110 + 111$

ဒိုက္ခနီးပုံစံများ non standard form

③ ရွေ့ဆောင်

AB	C	0	1
00		(1)	
01		(1)	
11		(1)	(1)
10			(1)

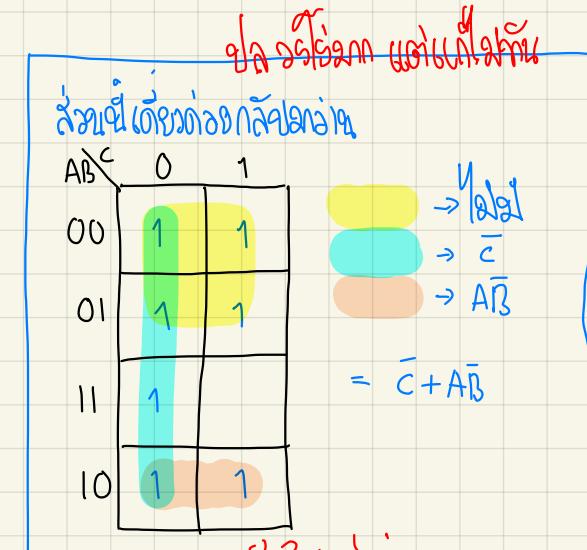
ဒိုက္ခနီးပုံစံ 1 မှတ်

ဒိုက္ခနီးပုံစံများ non-standard form $\bar{A} + A\bar{B} + AB\bar{C}$

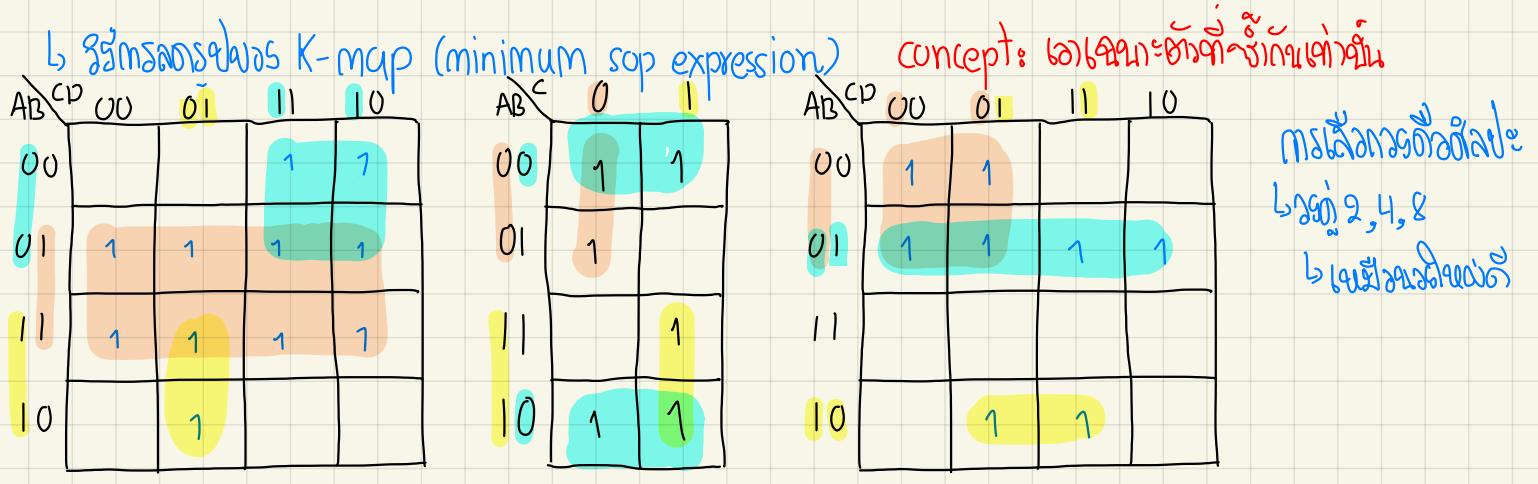
$\bar{A}(\bar{B}C)$	$A\bar{B}(\bar{C})$	$A\bar{B}C$
000	100	110
001	101	
010		
011		

AB	C	0	1
00		1	1
01		1	1
11		1	
10		1	1

ရွေ့ဆောင် ရွေ့ဆောင် ဂျာများပါ၍



= မြန်း non-standard to standard



Concept: តាមទីតាំងដែលមានលេខ 0 និង 1 គឺជាបន្ទាន់ដែលត្រូវការពិនិត្យ។

ការត្រូវការពិនិត្យ
លេខ 2, 4, 8
ឬលម្អិតអាជីវិត

ឧបត្ថម្ភសំនួរ →
ចុចចុចមិនមែនមែន និង C មែន
មានតម្លៃតិច ↓
រួចរាល់ និង A មែន (0)
= $\bar{A}C$

\bar{B}
 $\bar{A}\bar{C}$
 AC

$$= \bar{B} + \bar{A}\bar{C} + AC$$

$\bar{A}\bar{C}$
 $\bar{A}\bar{B}$
 $A\bar{B}C$

$$= \bar{A}\bar{C} + \bar{A}\bar{B} + A\bar{B}C$$

ឧបត្ថម្ភសំនួរ →
ឱ្យមែនតែល
មានតម្លៃតិច ↓
B មែន (1)
= B

ឧបត្ថម្ភសំនួរ →
C 0
មានតម្លៃតិច ↓
A
= $A\bar{C}D$

សមិទ្ធផល $B + \bar{A}\bar{C} + A\bar{C}D$

ទីតាំងទូទៅ truth table

ឬប្រើប្រាស់ K-map ដើម្បី (ទីតាំង 1 ត្រូវពិនិត្យ)

បានតាមទីតាំងដែលបានបញ្ជាក់

បានតាមទីតាំងដែលបានបញ្ជាក់

ឬតាមទីតាំងដែលមិនមែនមែន និង 1, X ដូចមានក្នុង តាមទីតាំងដែលមិនមែន

0	0	1
0	1	1
1	0	X
1	1	X

ទីតាំងដែលមិនមែនមែន SOP

បានតាមទីតាំង SOP ដែលត្រូវ 0

$$(A + \bar{B} + C)(\bar{A} + \bar{B} + C)(\bar{A} + B + C)$$

0 1 0 1 1 0 1 0 0

AB	0	1
00	1	1
01	0	1
11	0	1
10	0	1

Pos

SOP

$$\begin{aligned} &= \bar{B} + C \\ &= \bar{A} + C \\ &\Sigma = (\bar{B} + C)(\bar{A} + C) \\ &= \bar{A}\bar{B} + C \end{aligned}$$

A	B	C	0	1
0	0	0	1	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

ការការពិនិត្យសម្រាប់ SOP និងតាមទីតាំង

↳ ตัวหนังสือ SOP - nonstandard form งาน $(B+C)(A+\bar{B}+\bar{C})$ } 9 ผลิตภัณฑ์ในวงจรต่อกันที่เป็นไปได้

↳ K-map cell numbering (เลขประจำตัวช่อง)

↳ ตัวเลขประจำตัวช่องลักษณะดังนี้

↳ ระบุชุด set ตัวแปรตาม ABCD

$$2^3 \cdot 2^2 \cdot 2^1 \cdot 2^0$$

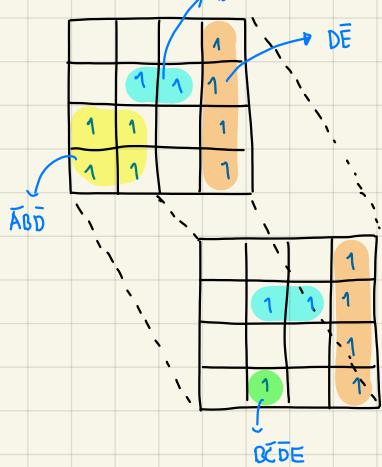
	A	B	C	0	1
00				0	1
01				2	3
11				6	7
10				4	5

ผลิตภัณฑ์ที่ไม่ใช่เลขฐาน 2

↳ การตั้งค่าปัญหาด้วยตัวต่อตัวเป็น 2 แบบ

การตั้งค่า $A=0, A=1$
การตั้งค่าบิทต์ต่อไปนี้

การตั้งค่า 2 = การตั้งค่า + 16



คำแนะนำในการตั้งค่าต่อไปนี้

↳ K-Map \rightarrow (minterm & maxterm)

↳ minterm สำหรับตัวต่อตัวเป็น 1 SOP (1)
maxterm สำหรับตัวต่อตัวเป็น 0 POS (0) } \rightarrow ฟังก์ชัน output

↳ minterm (SOP)

$$\sum m(\text{cellNumbering})$$

$$\hookrightarrow \text{เรื่อง } \sum M(0, 1, 3, 15)$$

↳ เลขประจำตัวช่องที่มี 1 จำนวนเป็น 1

for minterm

↳ maxterm (POS)

$$\prod M(\text{cellNumbering})$$

} 9 ชุดลักษณะของ K-Map cell
Numbering,

โจทย์จะบอกว่าต้องทำอย่างไร K-Map

↳ ดึงหัวเข้าไป แล้วหัวทางขวา

↳ รักษาเข้าไปหัว หัวเดียวเท่านั้น

systems simplification.

→ ନେତ୍ରକାଳୀମଚେଣିପୁଣୀ

- (1) %21mJ (SOP , non-standard , standard)

(0) %21mJ (pos , " " , " ")

truth table (ສະແດງສອດຕິອັນດານີ້ຢາດວຸ)

minterm (1) & maxterm (0)

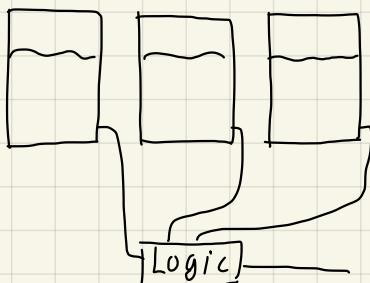
- ↳ ଏକାନ୍ତରିକପ୍ରେସ୍ (1)
- ↳ ଯୁଗମାତ୍ରିକାରୀ ଶବ୍ଦ (0)

→ ແລ້ວເນື້ອໃຈ່າຍກັບ ດີເລີດໄສສະຫະລຸງທີ່ຂ່າຍກຳ ກິດໆໄລຍະຫຼືນ

Combinational Logic Analysis

↳ Logic මාන්‍ය 1 සිංහල පුරුෂ තේරුවක්ද

↳ AND - OR Logic

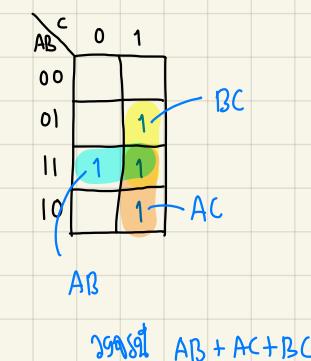


2. 2 1501 → out put oon 1

Median output's sensor

$\{ \text{S}(\text{U}) \} \text{giggle-map } \text{A} \text{B} + \text{A} \text{C} + \text{B} \text{C}$

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

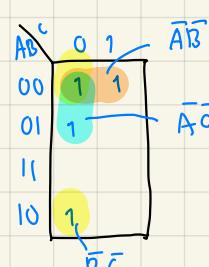


↳ AND-OR Invert Logic

↳ 9^o demorgan → ລອງປັບປຸງ

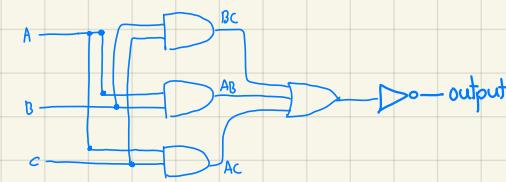
ପ୍ରାଚୀକାରୀ ଓ ପ୍ରଦର୍ଶନକାରୀ

0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	1	0

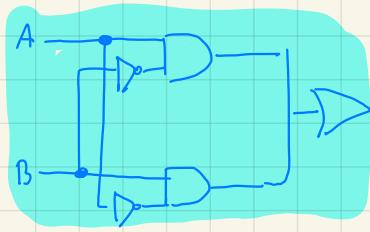


$$= \overline{AB} + \overline{AC} + \overline{BC}$$

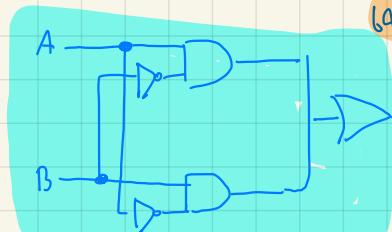
ବ୍ୟାକିନୀରେ



\hookrightarrow XOR & XNOR Logic



$$X = A\bar{B} + \bar{A}B \\ = A \oplus B$$



ເລື່ອມຕົວນັດຍາຕົວ

$$= \overline{AB} + A\overline{B}$$

XOR

ၬ ယခုအမြန်လေ့လာမှုဆိုချိန် မူးဆောင်ရွက်ခဲ့ပါ။ မူးဆောင်ရွက်ခဲ့သော်လည်းကောင်း၊ $x = y$ မှာ $x \oplus y$ မျှတော်းဆောင်ရွက်ခဲ့ပါ။

↳ मध्याह्न ग्रन्थ

ၶ ဆောင်ရွက်ပါတယ်ပြန်လည်မျှမောက်၊ ရှုပ်သတ္တုပို့စ်ဆုံးမျှမောက်

Excel screenshot showing a formula in cell E4: =IF(XOR(C4="Won",D4="Won"),"Yes","No")

	A	B	C	D	E	F
1	สำคัญจะได้รับคะแนน 2 เกมติดแล้ววันนี้ไม่ต้องเล่นเกมที่ 3					
3	No	Name	Game1	Game2	PlayGame3?	
4	1	John	Won	Lost	Yes	
5	2	Jan	Won	Won	No	
6	3	Jack	Lost	Won	Yes	
7	4	Joe	Lost	Lost	No	
8						

ପ୍ରାଚୀନ୍ୟରେ ହେଉଥିଲା

↳ Implementing Combination Logic

↳ ମେନ୍ଟାଲ୍ ହୈପ୍ପିକ୍ସର୍ଜିଙ୍

↳ program Logic gate

↳ given from a truth table to a logic circuit

↳ Qāfiyah SJP, POS

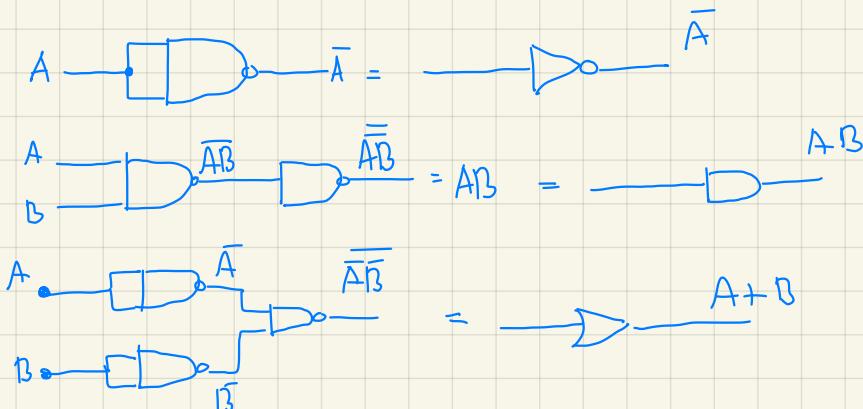
↳ Allows logic circuit to minimize the logic circuit

↳ Quantum logic circuit ንበብ (જાનકારીમાં → ગિર્મસાર) → નો Logic circuit હુએ

b 15

↳ K-Mup

↳ The universal property of NAND and NOR gate



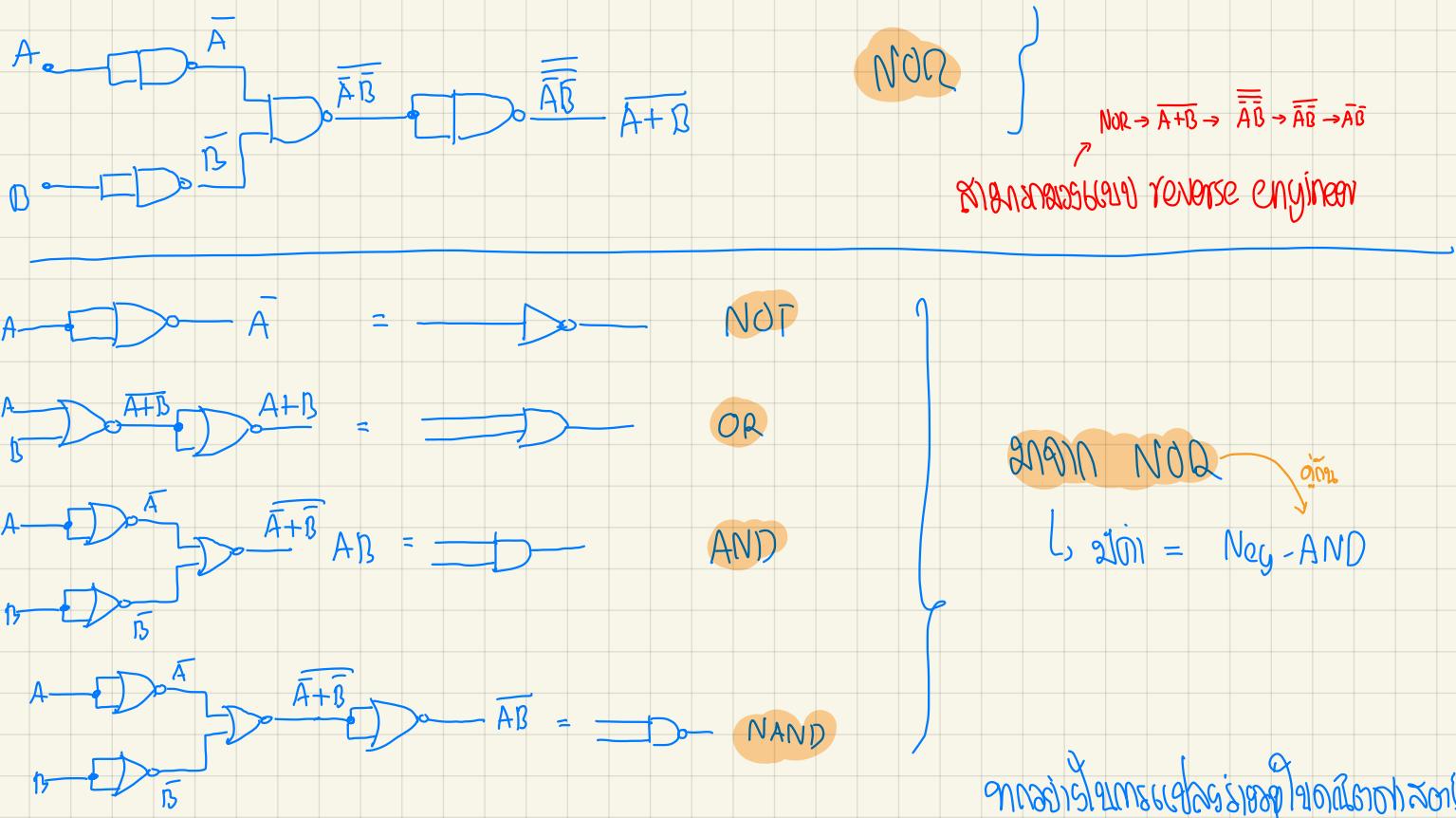
NOT

AND

OR

$f(i) = \text{Neg} - \text{OR}$

ମାନ୍ୟନ୍ ନାଂଡ୍



ນ້າມກຳ NOR

ລົງຈຶນ = Neg-AND

ດູວ່ານີ້ແມ່ນເປົ້າໃຫຍ່ໄດ້

ມັກສະນຸ

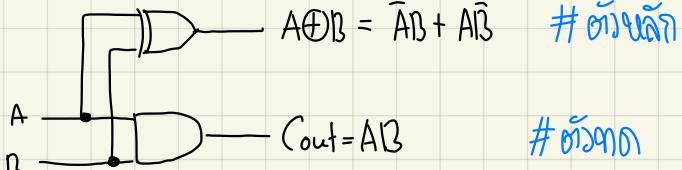
Function of Combinational Logic

ມອບ logic gate ດັກຕົກຕ່າງໆແລ້ວຮັບຜົນໄຟຂອງ fishing ຕິດ ແລະ ປົກປົກ

adder (ດັກຕົກຕ່າງໆ)

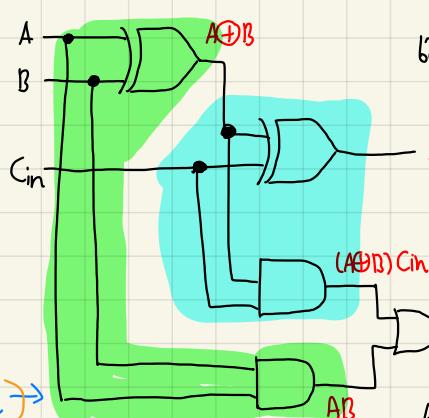
ມີເພື່ອ half-adder \rightarrow ມອບລົບຍົມກາ \rightarrow ອົບເດືອນຈຸດຕົວ (ຄົນ) = ທົດລົບຢືນຢັນການ

$$\begin{array}{l} 0 + 0 = 0 \\ 0 + 1 = 1 \\ 1 + 0 = 1 \\ 1 + 1 = 10 \end{array}$$



full-adder \rightarrow ສິດຕົກຕ່າງໆ \rightarrow ຮັບຈາກຕົກເພີ້ມຂາເຊື່ອງ ໂດຍກຳນົດໃຫຍ່ຕົກຕ່າງໆ (ສິນປົດ)

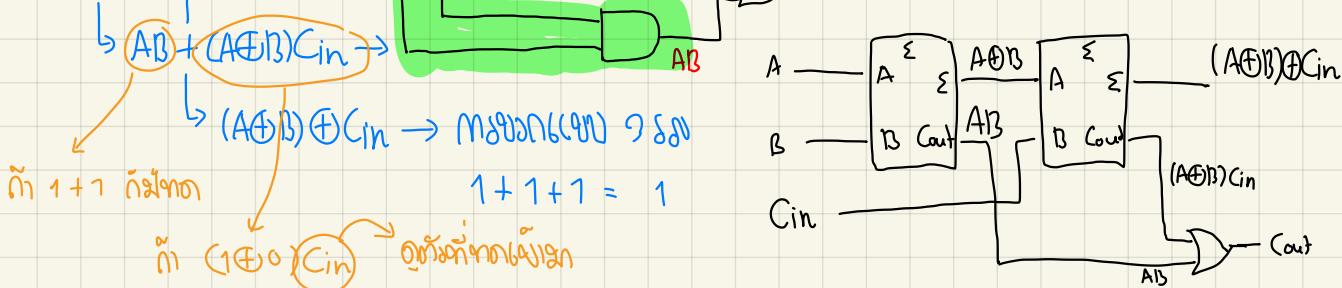
A	B	Cin	Cout	Σ
0	0	0	0	0
0	0	1	0	0
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1



(a) half adder ຂາຍເກີນ

$(A \oplus B) \oplus Cin$

$C_{out} = AB + (A \oplus B)Cin$



ဆាល់ចងក់សម្រាប់ adder និង lempup កែវី

A	B	Cin	Cout	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Add Count

A	B Cin			
	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$\begin{aligned} \text{Cout} &= AC_{in} + DC_{in} + AB \\ &= (A+B)C_{in} + AB \end{aligned}$$

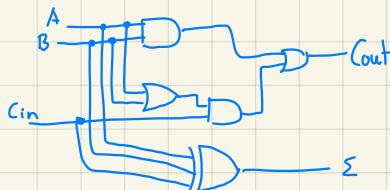
qj05 Σ

A	B Cin			
	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$\bar{A}\bar{B}C_{in} + \bar{A}\bar{B}C_{in} + A\bar{B}C_{in} + \bar{A}B\bar{C}_{in}$$

$$(\bar{A}\bar{B}+AB)C_{in} + (A\bar{B}+\bar{A}B)\bar{C}_{in}$$

$$(A\oplus B)\otimes C_{in}$$



ពីលេខា កែវីដែលបានបញ្ជាក់ 555

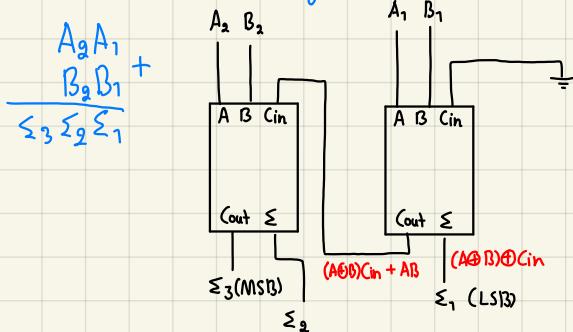
↳ ចំណា full adder នៃលក្ខណៈ IC



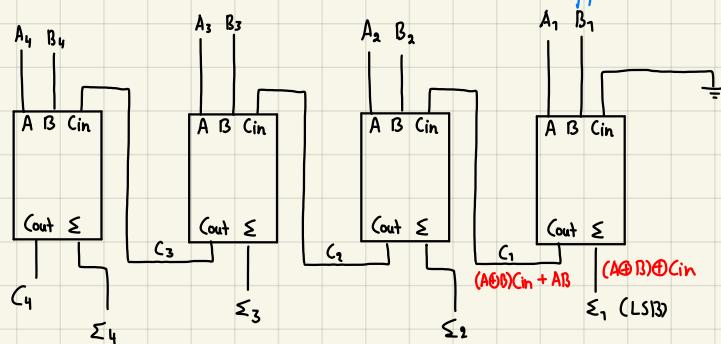
ម៉ោងឯកតាមកំឡុងយុទ្ធឌែលរាយវិធី

(សេដ្ឋកិច្ច)...

↳ Adders - Parallel Binary Adder



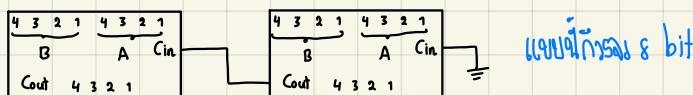
↳ Adders - 4 Bit Parallel Adder ($C_{in} \text{ nipple} \rightarrow \text{សម្រាប់ 4 bit}$)



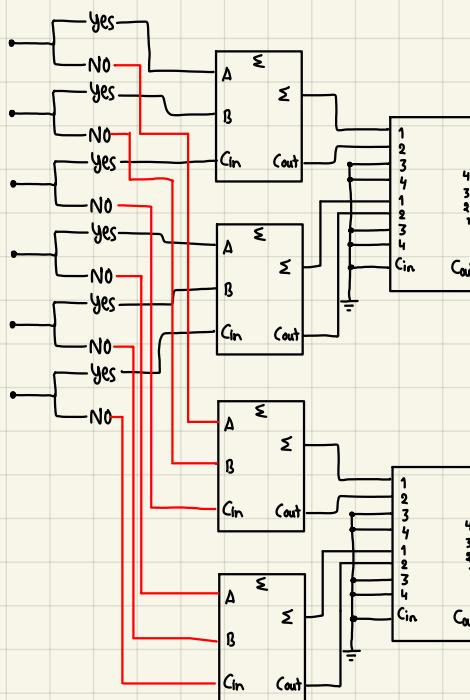
$$\begin{array}{rcl} \text{MSB} & & \text{MLB} \\ \text{ផលិតផល} & A_4 A_3 A_2 A_1 \\ & B_4 B_3 B_2 B_1 \\ & \hline S_4 S_3 S_2 S_1 \end{array}$$

↳ សម្រាប់ការសែនាំការបូក 4 bit ត្រូវបានបញ្ជាក់ថា សម្រាប់ចំណា 4 bit.

↳ Expansion



↳ ចំណាត់ជាន់នៃលក្ខណៈ



Adders - Look Ahead Carry Adders

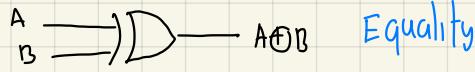
#ຈາກອົດຫຼັງໄດ້ກຳລັງດັບ

ລູກຄະເພິ່ນຕີເທົ່ານັກລ່ວມຍັນ

- ຖືກີ້ນີ້ຂະເທົ່ານັກແກ່ມີຕົວກະທົດຢູ່ນີ້ ດູວັດຫຼັກ (0-0) ຂອບຕົວກະທົດຢູ່ນີ້ (1-1) ດູວັດຫຼັກ (1)
- ມີນັບສິ່ງນັກຮອດຮອກກົດ ວິຊະກຳທີ່ການມູນຍັນ

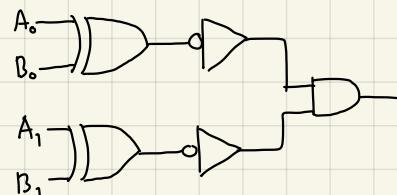
Comparators

- ເປົ້າໂທນັກເທັນ == ອຸດສັດ \oplus ອົບມານ logic $XOR + Invert = XNOR$ #ຕະຫຼອງ



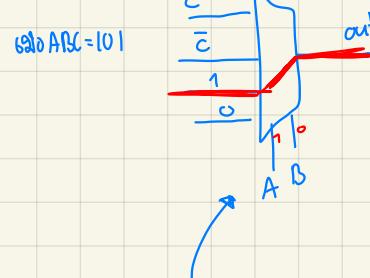
A	B	$A \oplus B$	$\overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

ເພື່ອສົນເກີນໃນ
ເພື່ອສົນເກີນ



- ເປົ້າໂທນັກເທັນເສີ່ງ ລາຍການ ອຸດສັດ ອົບກົດ (Inequality)

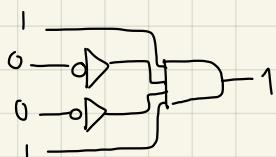
ລູກ IC ດັບປຸງ



Decoders - (The Basic Binary Decoder)

- ຕົວລະດອບສັບ ຈຶ່ງມາຊື່ກົບຊູ່ໄກຕົວຕັ້ງ

- ເຮັດ ຕັ້ງ input ແມ່ນ 1001 ອັນ output ແມ່ນ 1



ກະຊວງມີປະຈຸບັນ ແລ້ວກຳນົດໃຫ້ວັດແມ່ນມີກົດ

ລູກ IC ດັບປຸງໃນຕາມຕົກຕົວ

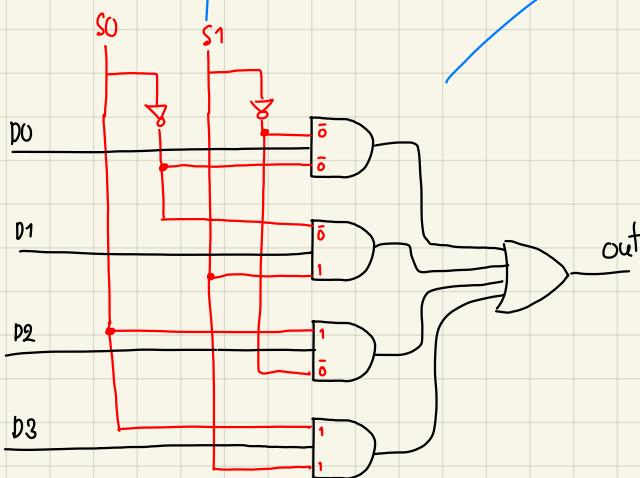
- ແຈ້ວເຕັ້ງໄວ້ໃຫ້ຕົວລະດອບເຫັນວ່າ ດັບ decoder

A	B	C	out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

out = c
out = \bar{c}
out = 1
out = 0

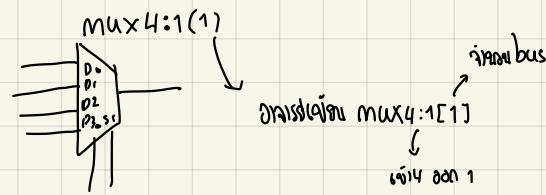
- Multiplexer ອຸດສັດ data selector

- ຕັ້ງຕື່ນວ່າ output ສອນ



ກະຊວງມີປະຈຸບັນ (ມູນຕົກຕົວ)

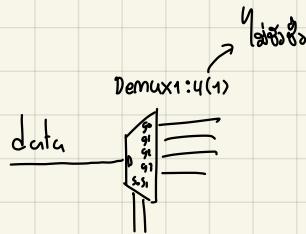
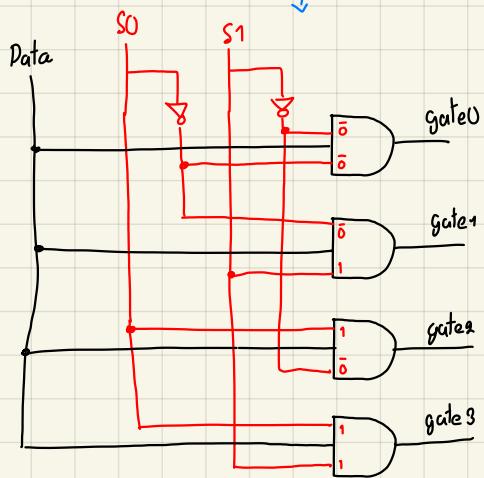
ໄວ້ເຕັ້ງກົດ "multiplexer"



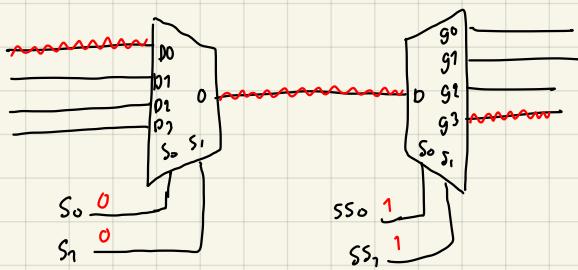
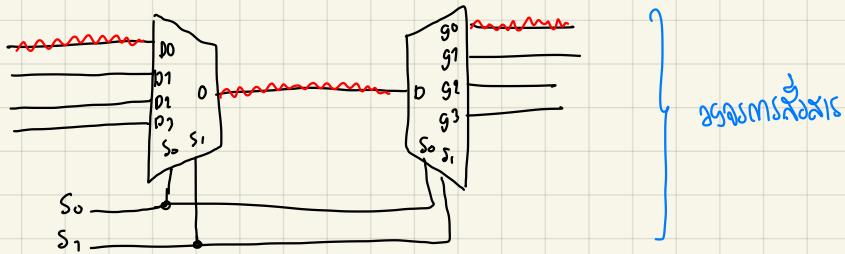
↳ ក្រឡុស demultiplexer

↳ ក្រឡុសដែលបានបង្កើតឡើង

នៅលើសម្រាប់សម្រាប់ចាប់ផ្តើមទិន្នន័យ នៅតី XOR នេះ

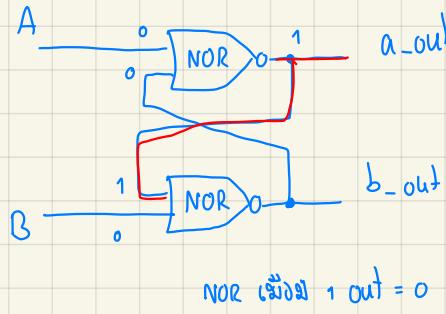


នូវនៅក្នុង mix ក្នុង



Latches, Flip-Flops, and Timers

↳ សម្រេចការណ៍ latch នេះ

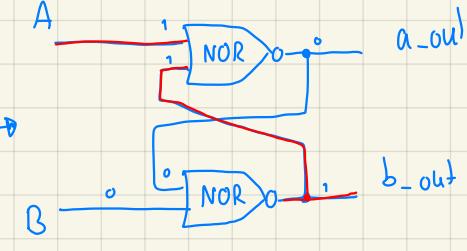
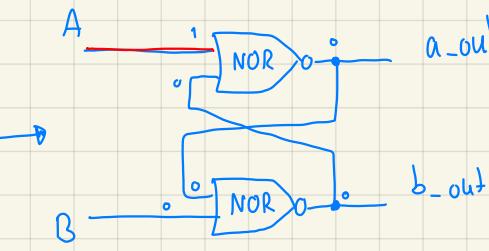
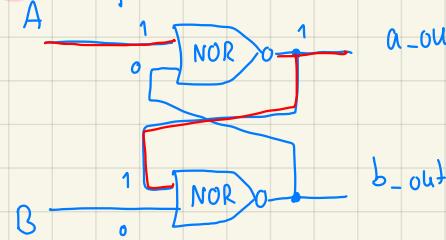


នៅក្នុងគេងតាមលក្ខណៈ latch នេះទេរាងការងារគឺមាន

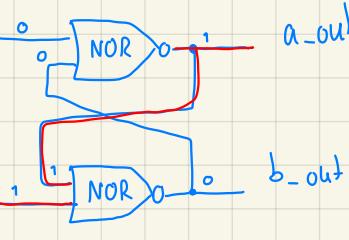
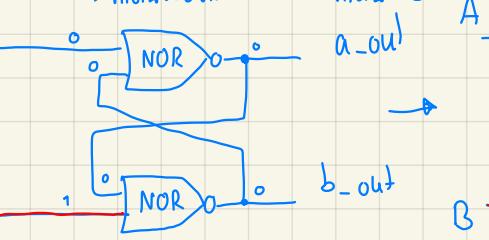
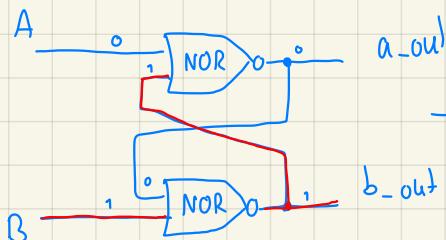
↳ ផ្លូវលក្ខណៈនៃលើបិន 0

↳ ពួកគេនឹងចូលនៅលើលក្ខណៈ a_out ឬ b_out ទាំងមីនាគារណ៍

① ឯកសារអីនូវ Input A ដើម្បីលើកកុង 1



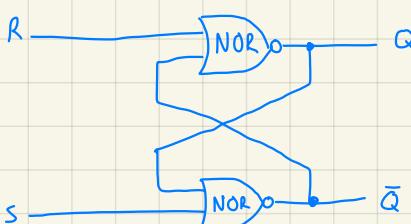
② ឯកសារអីនូវ B = high នាក់កំណត់លើកកុង



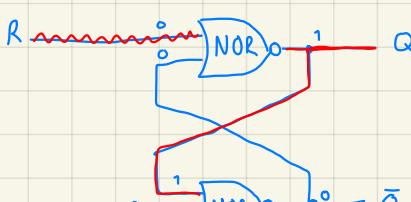
ឯកសារអីនូវ នូវ Input A ដើម្បី output ជាខ្លួន 1 និងលើកកុង b_out } និង ឯកសារអីនូវ នូវ Input B ដើម្បី output ជាខ្លួន 1 និងលើកកុង a_out }

state និងលើកកុងនៃលក្ខណៈ

↳ latch នេះមួយ នៅរឿងកំរើ SR-latch



នៅក្នុង 1, 1 ខ្លួន



(នៅក្នុងខ្លួន)

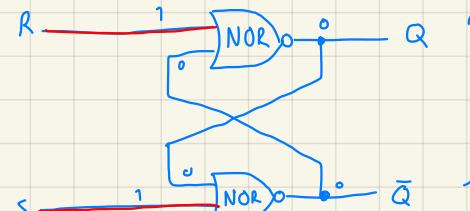
S	R	Q	\bar{Q}	
1	1	0	0	Invalid
1	0	1	0	Latch set
0	1	0	1	Latch reset
0	0	nc	nc	No change

និងលក្ខណៈលើកកុង (NOR)

S	R	Q	\bar{Q}	
1	1	hc	nc	No change.
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
0	0	1	1	Invalid condition

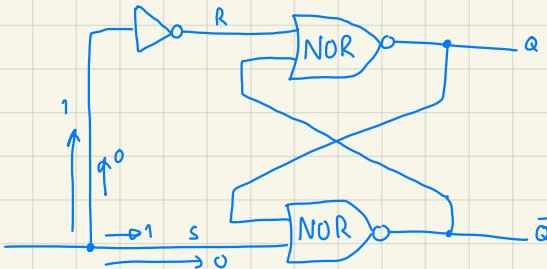
និងលក្ខណៈលើកកុង (NAND)

(Neg-OR)



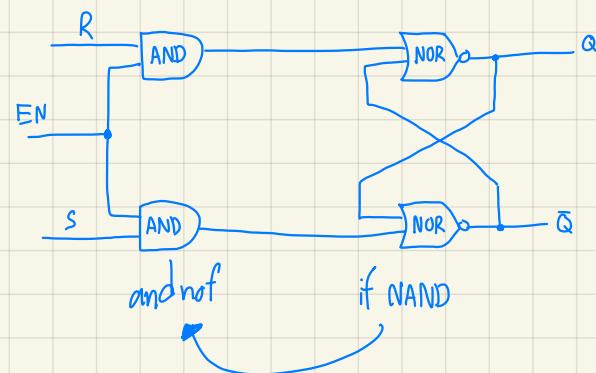
និង invalid state ខ្លួន

ආර්ථික දැල්ච (D-Latch)



ආර්ථික පිළිබඳ මේවා නොවන

ආර්ථික SR - latch with enable



and not

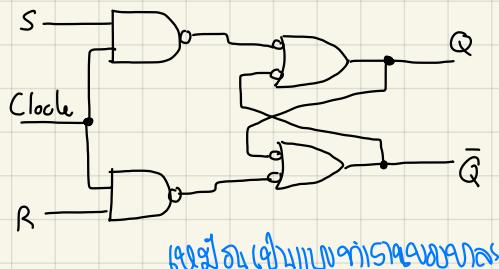
if NAND

enable (ඇඟිටුර්ස්ට්රූ) වූත් මිල්ල

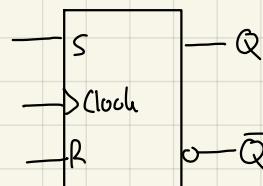
$$\text{NAND} = \text{Neg-OR}$$

0	0	1	1	1	1
0	1	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	0

{ පෙන්වන තාක්ෂණීය output = 1 }



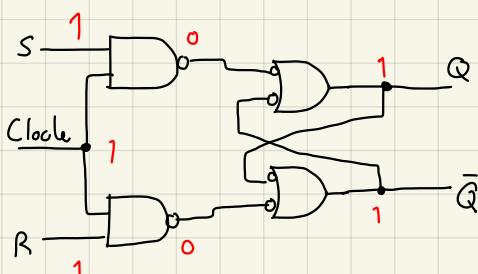
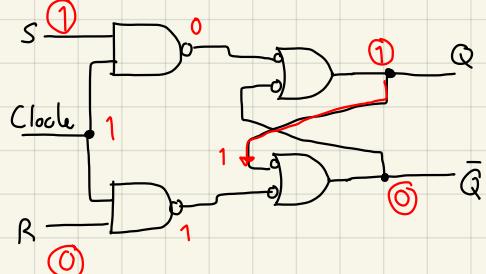
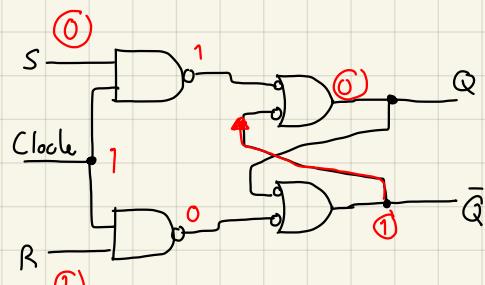
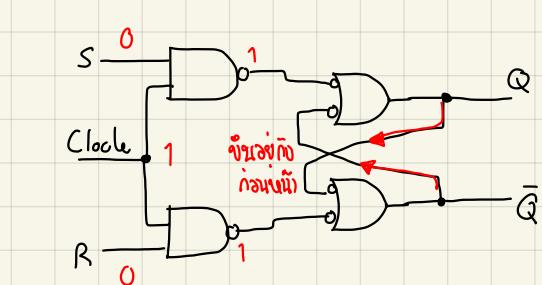
එමුදු පිළිබඳ මේවා නොවන



ආර්ථික පිළිබඳ මේවා

S	R	Clock	Q	\bar{Q}
0	0		1	no change
0	1		1	0
1	0		1	0
1	1		1	1

ආර්ථික පිළිබඳ මේවා, නොවන
ආර්ථික පිළිබඳ මේවා

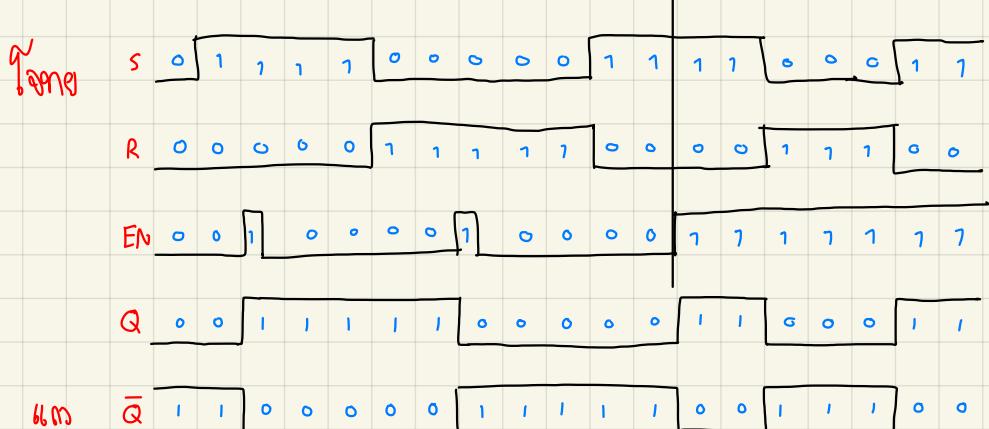


not allow $S=0$ invalid

Clock	S	R	Q	\bar{Q}
0	0	0	0	Latch
0	0	1	0	Latch
0	1	0	0	Latch
0	1	1	0	Latch
1	0	0	0	Latch
1	0	1	0	0
1	1	0	1	0
1	1	1	1	0

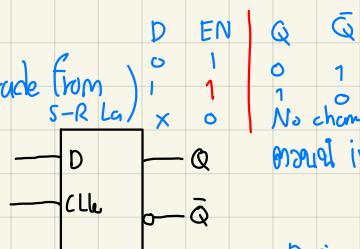
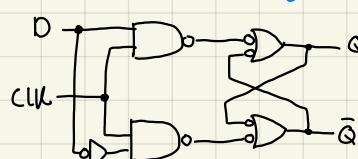
เมื่อ clock เป็น 0 \rightarrow NAND ตัวที่ 1 ผลลัพธ์ $S=1 \quad R=1$ } ทำให้ไม่เกิด no change

เมื่อ clock = 1 \rightarrow ก็จะต้องเปลี่ยนแปลง
3 กรณีดังนี้



↳ D - Latch

↳ (ดึงตัว not gate) upgrade from S-R La



กรณี input แรกเท่ากับ 01 } wrong

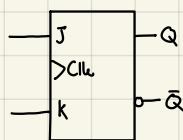
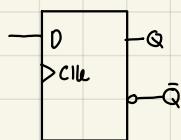
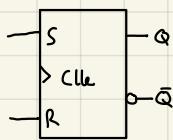
D ต้อง 1 กรณี SET

ต้อง 0 กรณี RESET

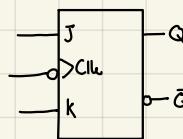
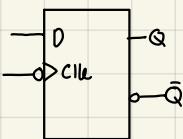
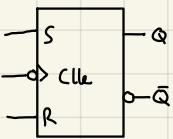
↳ Flip - Flops

↳ ຂົງກາລ ແລະ synchronous bistable devices

↳ ພົມຕົວເປົ້າຕາຫຼາມຂອງພົມຕົວ, ນອບນູກສັດ



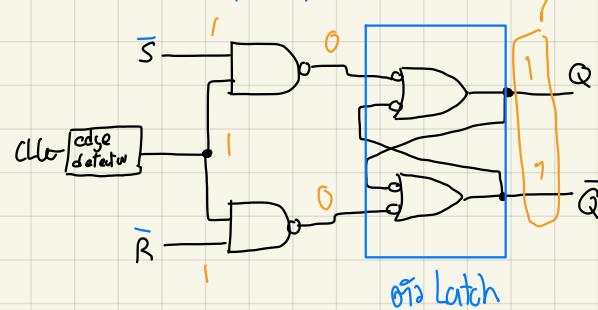
ກຳເຊົາຂອງພົມຕົວ



ກຳເຊົາຂອງພົມຕົວ

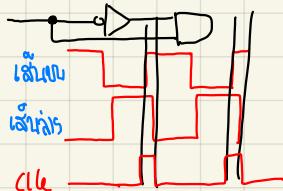
↳ S-R flip flop

ຈົມຍາດັ່ງນີ້ S, R ສໍາເລັດ Q, Q-bar ເລື່ອ 0,1 = 0,1 = Reset



\bar{S}	\bar{R}	clock	Q	\bar{Q}	
0	0	X	nc	nc	nochange
0	1	1	0	1	reset
1	0	1	1	0	set
1	1	1	?	?	Invalid

↳ ເນື່ອໃຈວິທີກຸ່ມ edge detect

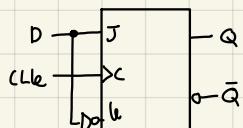


ກຳສົ່ງ \bar{S}, \bar{R} ເຊັ່ນຕີເປົ້າຕາຫຼາມ NAND ແລະ Neg-OR

↳ input ຈົມຍາດັ່ງນີ້ ເບາເລີຍອົງຮູ່ນ ອົງຮູ່ນ

ອົງຮູ່ນ

↳ D - flip flop



D	clock	Q	\bar{Q}
1	1	1	0
0	1	0	1

ເປົ້າຕາຫຼາມ D ແລະ ຖົກເປົາຕາຫຼາມ ທີ່ນີ້ແມ່:

ກົດ J-k flip flop ອົງຮູ່ນຕີກຸ່ມ ອົງຮູ່ນຕີ NAND gate

ກົດ clock

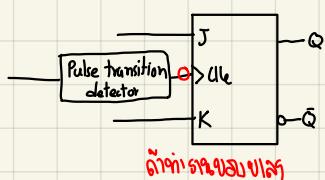
ປົກເປົາຕາຫຼາມ clock

Q

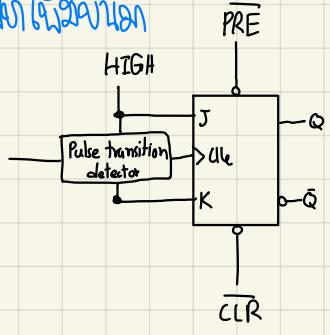
↳ JK flip flop \rightarrow ຕຳຫົວໜ້າສາຍາລັບ ambiguous state

↳ ອູດເຕີຣັກັນ S-R flip flop

↳ ສະບັບໃຫຍ່ focus ທີ່ໄດ້ກາງຊຸມຂອງຈິງນີ້



ຕຳຫົວໜ້າຮັບຂອນປະເທດ



ຕຳຫົວໜ້າຮັບຂອນປະເທດ

J	K	Clk	Q	\bar{Q}
0	0	1	no change	
0	1	1	0	1
1	0	1	1	0
1	1	1	toggle	

JK flip flop \rightarrow ອູດເຕີຣັກັນ SRFF
J, k ມັງ Q, \bar{Q} ແລ້ວ
ຕື່ມັນ 1, 1 ຈະເພີ້ມໃນການ toggle $\begin{cases} 0 \rightarrow 1 \\ 1 \rightarrow 0 \end{cases}$ } ດັວຍກົມສົດຍຸລຸ = ດິນ

J	k	C	$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	Q	\bar{Q}
0	0	0	1	1	no change	
0	1	0	1	1	0	1
1	0	0	1	1	1	0
1	1	0	1	1	toggle	
X	X	X	0	0	invalid	
X	X	X	0	1	1	
X	X	X	1	0	0	
X	X	X	1	1	no change	

ປະເທດຂອນປະເທດ	$\overline{\text{PRE}}$	$\overline{\text{CLR}}$
1	1	ປົກຕົວ
1	0	$Q = 1$
0	1	$Q = 0$
0	0	un used

↳ Potential timing problem in flip-flop circuit

↳ ອູດ output ອະລັດຕົວຕ່າງໆຂອງ input ອະລັດກັນ

↳ propagation delay may cause unpredictable outputs.

↳ ລົງລາຍງານ register ພະນັກ ms shift bit (data transfer)

↳ ms shift bit ມີຄວາມສະດູກເສດຖະກິນ ຈີ່ $l \rightarrow r$, $r \rightarrow l$

↳ parallel transfer require interconnection ຂັ້ນມີໃນ series

↳ more critical when a greater number of bit are being transfer

↳ parallel ແລ້ວຈົກ, ແລ້ວມີລາຍງານ

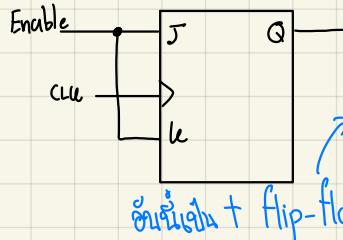
↳ series ຫຼືນໍາຈົກ, ອານຸໄສຢູ່ນັ້ນ

Counter.

0 0
0 1
1 0
1 1

ການຈົດເບຍໃຫ້ສ່ວນ counter → ສັງເກດຂຶ້ນ

clock ຫຼັງຈາກ 0-1-0-1-0-1...



ທີ່ຈະຈົດເປັນ ແລ້ວ
ແຈ້ງປະເມີນ

B	A
0	0
0	1
1	0
1	1

b ເປັນອັນໄສວ່າ A ເປັນ 1 ແລ້ວ ຂີ່ clock

ກຳອຽດ 3 ອົບອະລະ 0 0 0

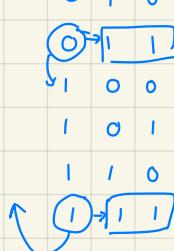
0 0 1

0 1 0

1 0 0

1 0 1

1 1 0



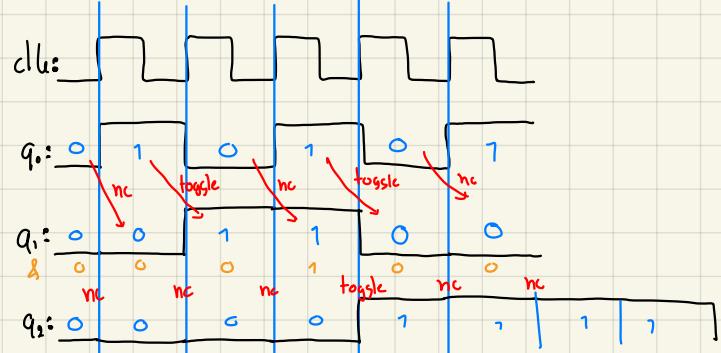
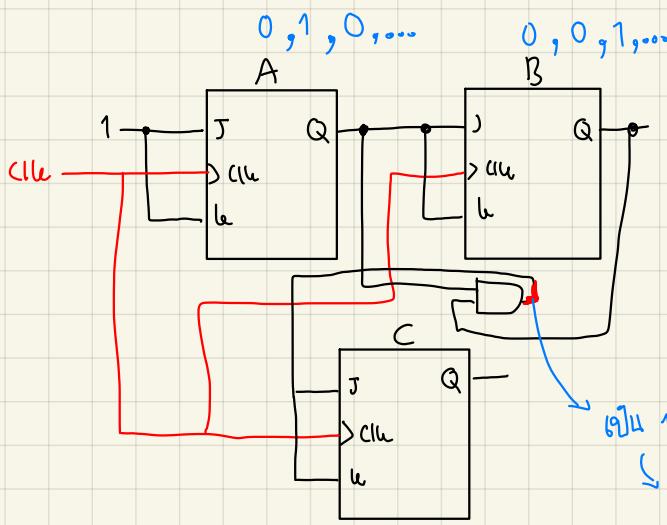
ເຊື່ອຈົດເປັນ a ແລ້ວ b ເປັນ 1 ແລະ ຂີ່ clock

Q3 ເປັນຄົດການເຕືອນໄຫວ

↳ ມອດກາຍໄລຍະ synchronous counter

(1,1) ເຕີ toggle

(0,0) ເຕີ no change.

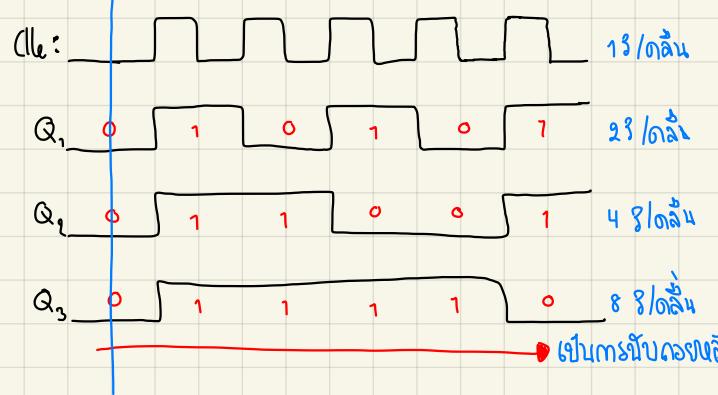
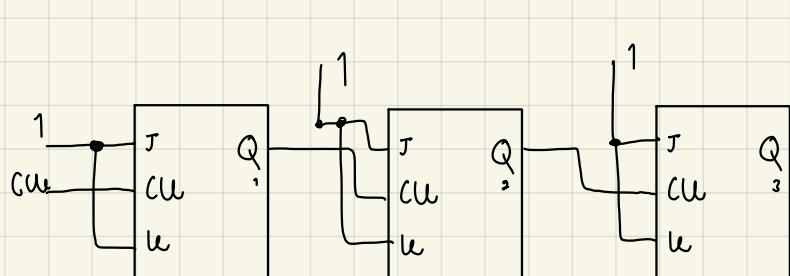


ເຊື່ອ 1 ເຊີບ AB ເປັນ 1
Q3 ເປັນ and ເຕີຂອງຮອງ

0, 0, 0, ...

↳ ມອດກາຍໄລຍະ asynchronous counter

wave form.



13/ຕົ້ນ

23/ຕົ້ນ

48/ຕົ້ນ

88/ຕົ້ນ

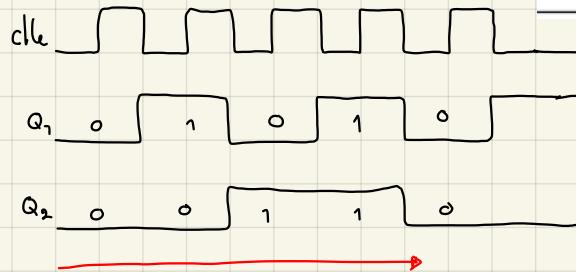
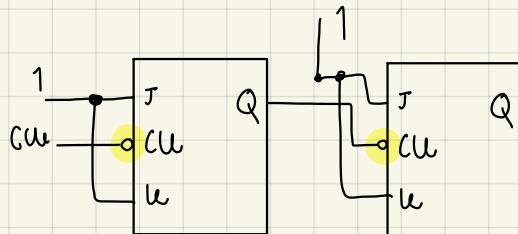
ເປັນກາຍຂັ້ນລອນສັງ

↳ ដែលក្នុងនេះ បានបានឈូមិយោគពី ការបញ្ចូន 2 លើស្ថាន

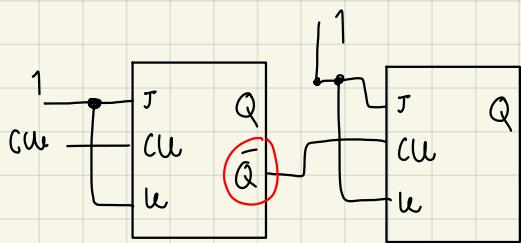
↳ ក្នុងនេះ asynch, syn ស្ថាននូវការបញ្ចូន 2^n , $\text{mod}(2^n)$

↳ តាមរយៈ asynchronous countdown តារាងនេះ countup តុល់?

↳ នឹងមានការបញ្ចូនចុងចាយ

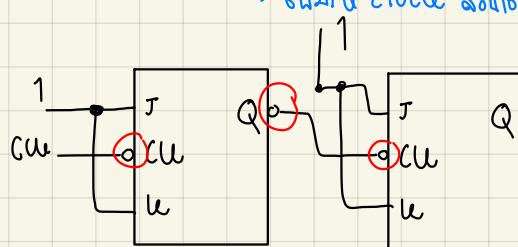


ស្ថាននេះ countup នៅក្នុង



→ នេះជាការបញ្ចូនដូចជា តាមរយៈសម្រាប់បញ្ចូន

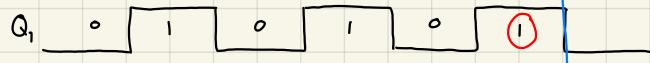
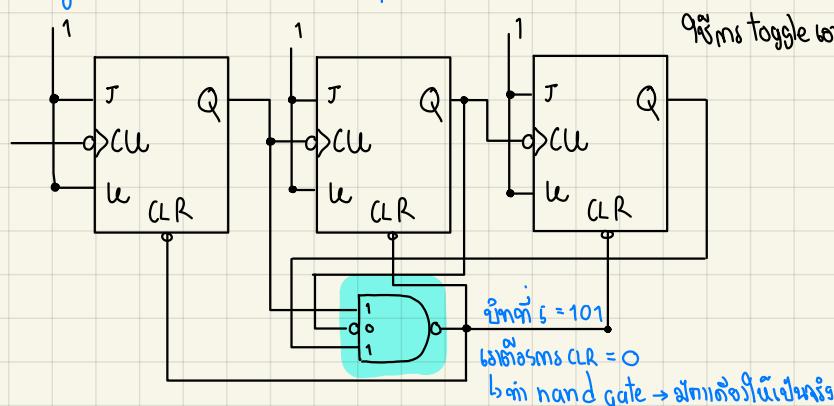
↳ នឹងមិន clock នៅពីរប៉ុណ្ណោះទេ 0 តួនាទារាយ



→ នេះជាការបញ្ចូន count down.

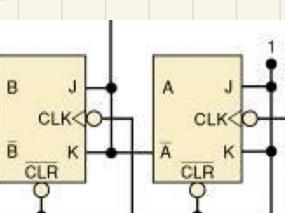
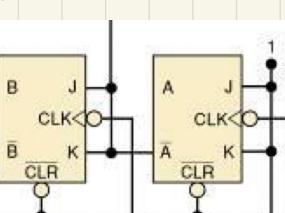
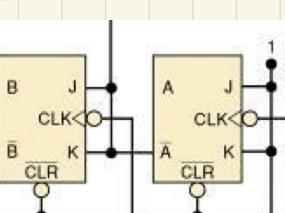
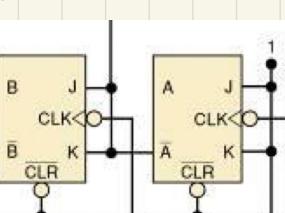
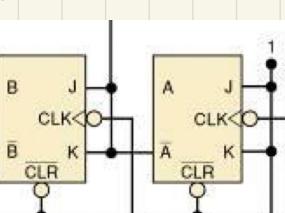
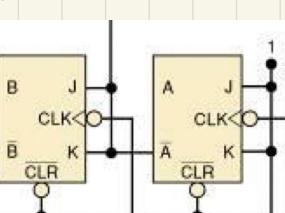
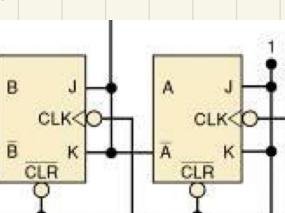
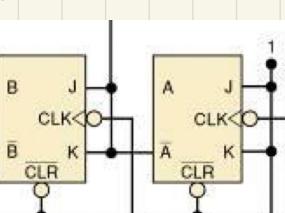
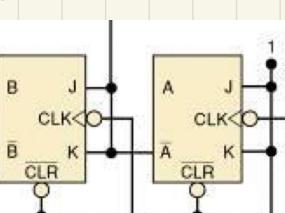
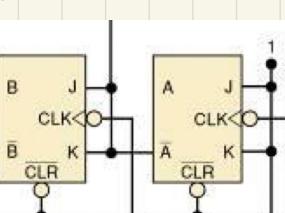
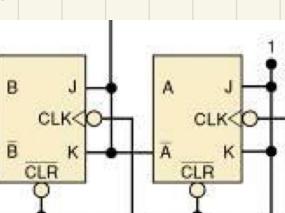
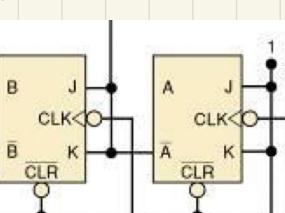
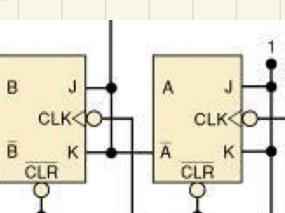
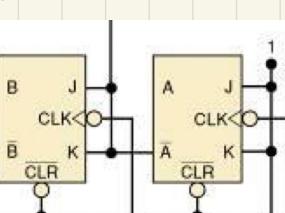
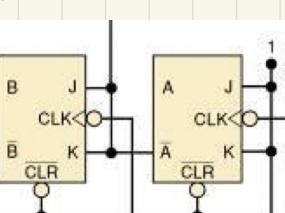
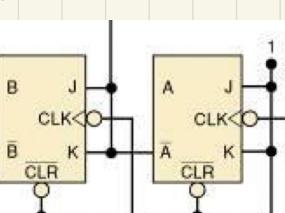
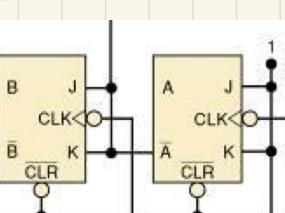
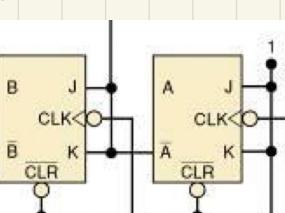
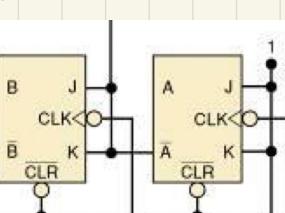
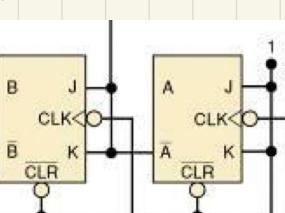
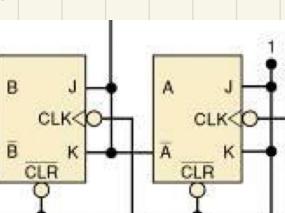
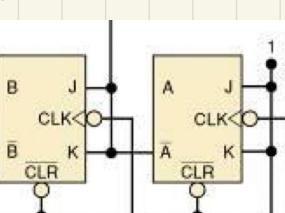
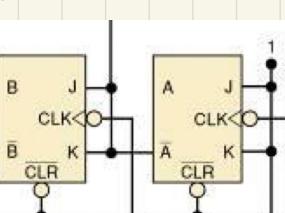
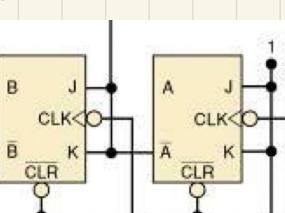
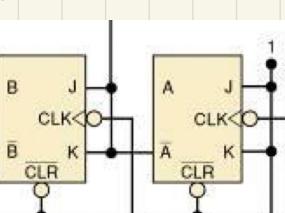
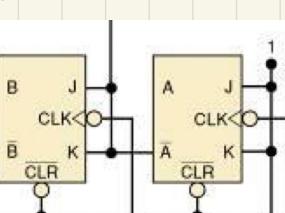
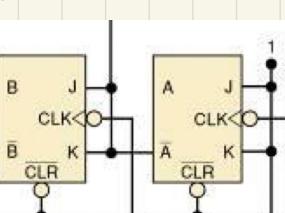
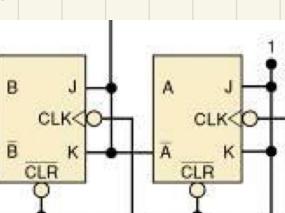
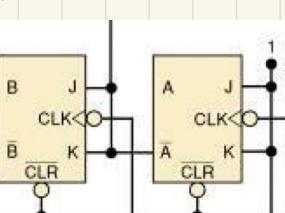
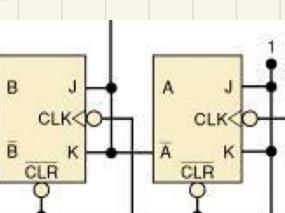
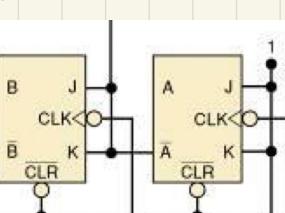
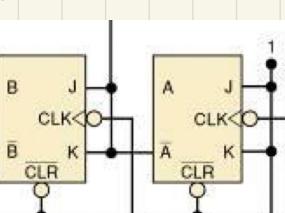
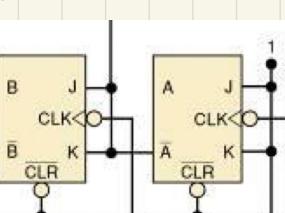
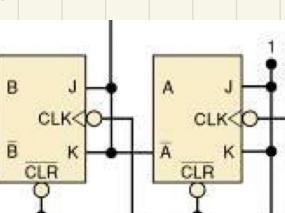
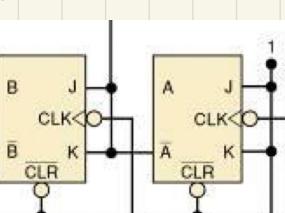
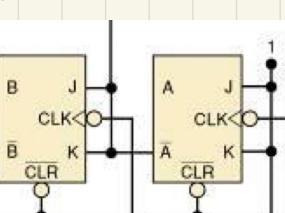
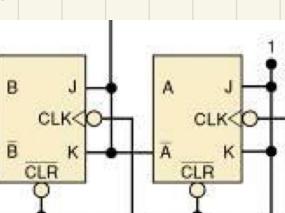
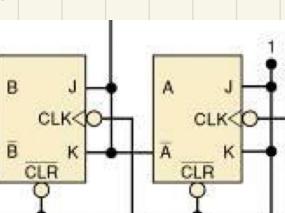
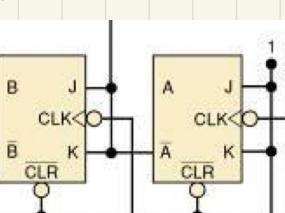
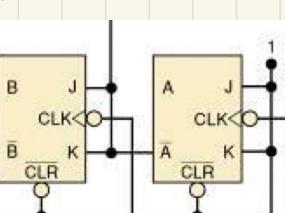
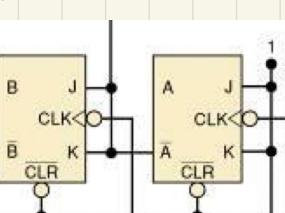
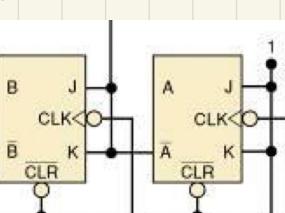
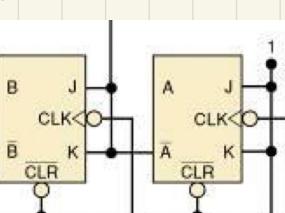
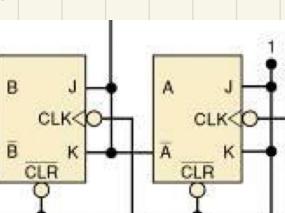
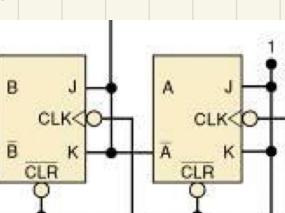
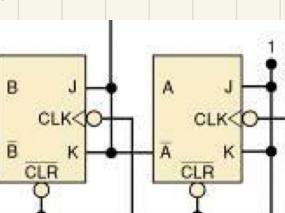
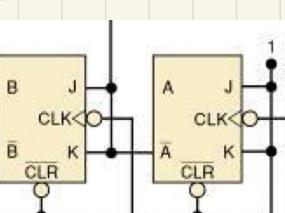
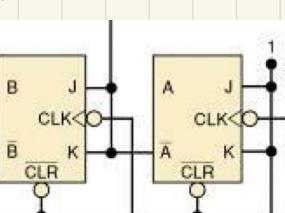
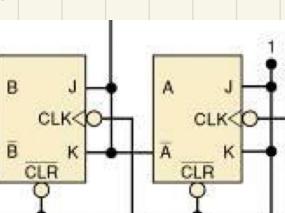
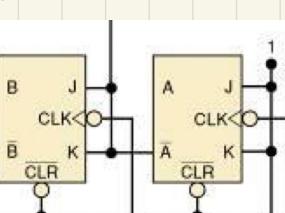
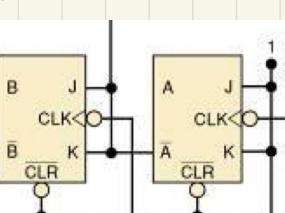
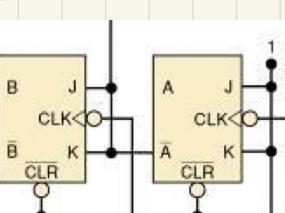
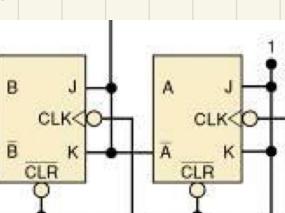
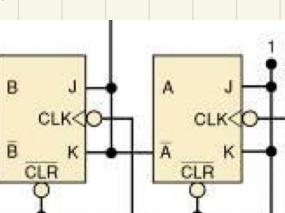
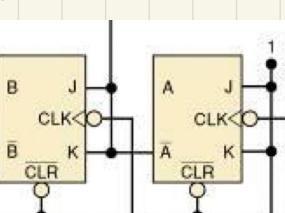
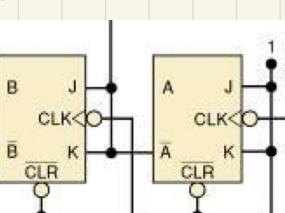
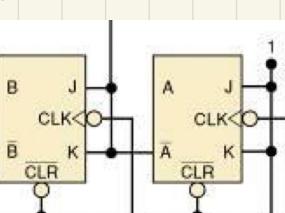
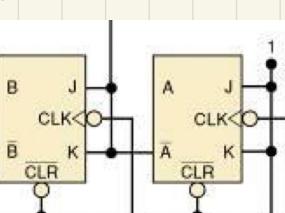
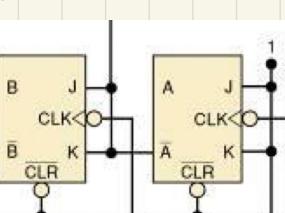
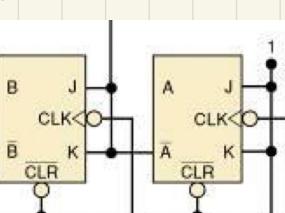
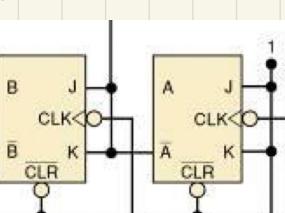
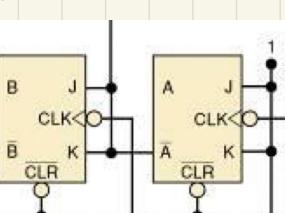
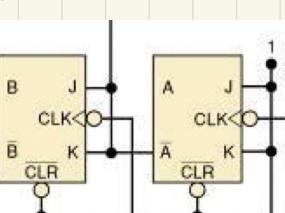
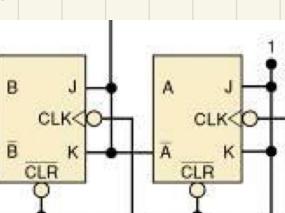
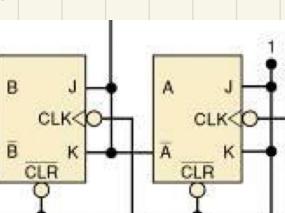
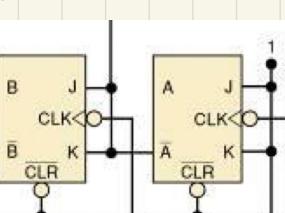
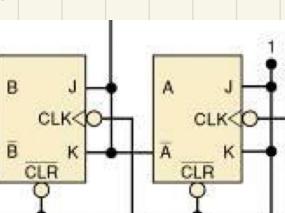
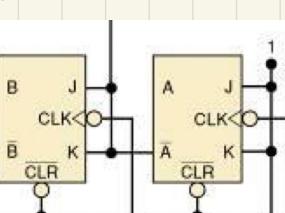
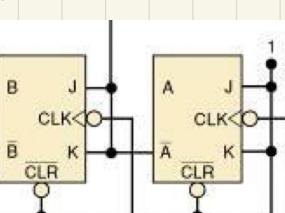
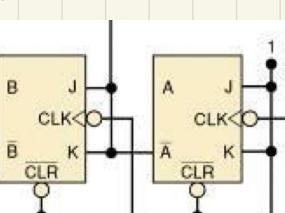
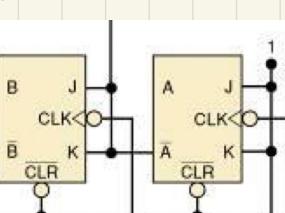
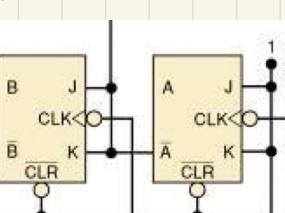
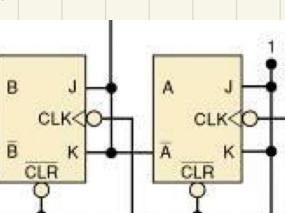
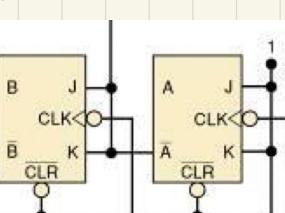
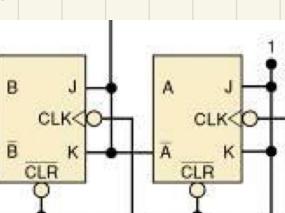
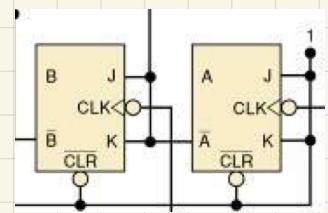
ការសរុបរាល់ mod

↳ asynchronous countup mod(n) → តាមរយៈការសរុប mod(5)



↳ បានស្ថាន synchronous ការបញ្ចូន

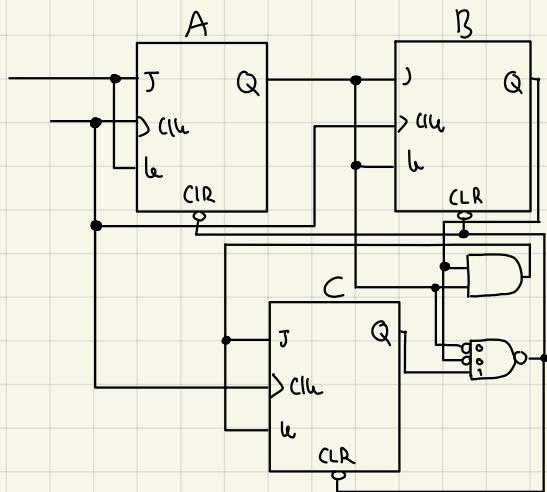
តាមរយៈ synchronous count down



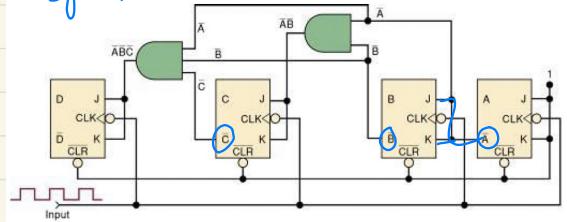
↳ synchronous countup mod(n)

↳ Q_n and gate (Q_n > cuu & Q_n > cuu) \rightarrow នឹងការសម្រាប់ mod (4)

100



↳ synchronous countdown



↳ នូវលទ្ធផលនេះ 0-1-2-3-4-0 ...

និងការបញ្ចូនតុលាការនៃចំណាំ និងការបញ្ចូនតុលាការនៃចំណាំ

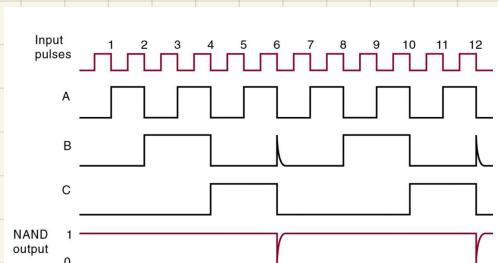
↳ និងការបញ្ចូនតុលាការនៃចំណាំ

↳ និងការបញ្ចូនតុលាការនៃចំណាំ

↳ synchronous countup mod(n)

↳ ការបញ្ចូនតុលាការនៃចំណាំ

បានរាយការណ៍នៅលើ digital
គ្មានការណ៍



synchronous countup mod(n) upgrade.

សម្រាប់ j(k) flip flop

0 0	no change
0 1	0
1 0	1
1 1	toggle

និងសម្រាប់ j(k)

ជាអាមេរិកណ៍

Q _n	Q _{n+1}	j	k		j	k
0	0	0	→ 1	reset	0	X
0	1	1	→ 0	no change	1	X
1	0	1	→ 1	set	X	1
1	0	0	← 1	toggle	X	0
1	1	0	← 0	reset	1	X
1	1	0	← 0	toggle	X	1
		1	← 1	nochange	X	0
				set		

↳ នីមួយៗសម្រាប់ការសម្រាប់ mod(5)

Pre State	Next State	C	B	A
C B A	C B A	j k	j k	j k
0 0 0	0 0 0	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	0 0 0	X 1	0 X	0 X

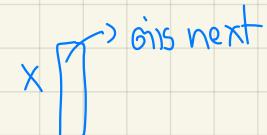
4 ដូចស្រាវជ្រាវ 0

input នៃការសម្រាប់

pre (ភ្លើង) 0 next state ចូលរួម



pre (ភ្លើង) 1



↳mini K-map ०९६

AB\BC		CBA		BA	
		00	01	11	10
J _C	0	0	0	1	0
	1	X	X	X	X

$\text{jos } B$	$\text{J} \setminus \text{B}$	00	01	11	10
J_B	0	0	1	\times	\times
	1	0	\times	\times	\times

WDSA	C	B4	00	01	11	10	\bar{C}
Zt	0	1	X	X	1		
	1	0	X	X	X		

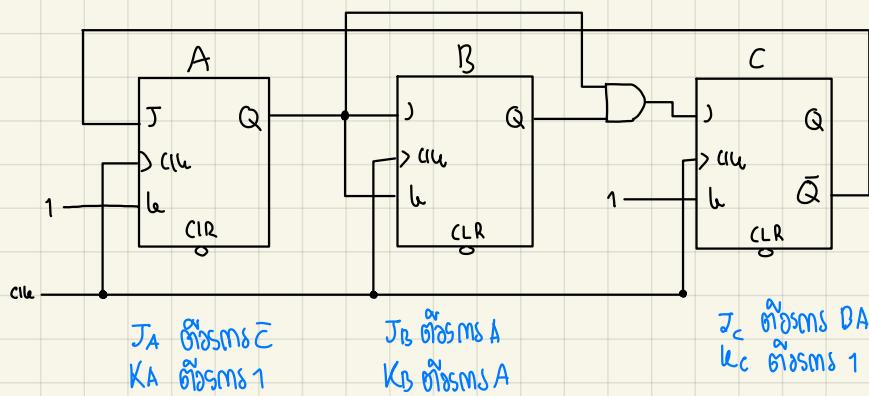
Kc	C	B4	00	01	11	10
0		X	X	X	X	
1		1	X	X	X	

	00	01	11	10
0	X	X	1	0
1	X	X	X	X

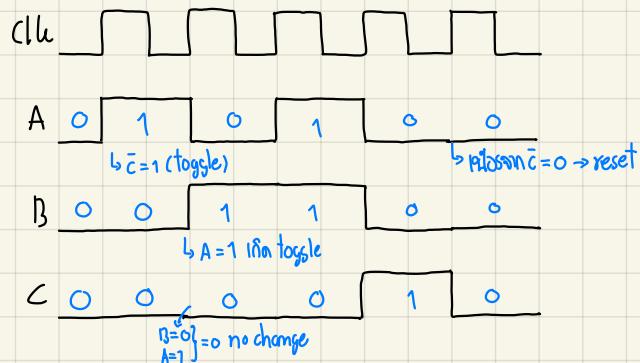
6A	C	BA	00	01	11	10
0		X	1	1	X	X
1		X	X	X	X	X

Pre State	next State			C	B	A					
C	B	A	C	B	A	j	k	j	k	j	k
0 0 0 0 1 1 0 1 1 1	0 0 1 0 1 1 0 0 0 0	0 1 0 1 1 1 0 0 0 0	1 0 0 1 0 1 0 1 0 X	0 X X X 0 X X X X 1	X X 0 X X 0 0 1 X 0	0 1 X X 0 1 X 1 X X	X 1 X 1 0 X 0 X X 0	1 X 1 1 X 1 X 1 X X	1 X 1 1 X 1 X 1 X X	1 X 1 1 X 1 X 1 X X	

↳ input ដែល previous state ទទួលបានការបញ្ចប់ input នៃ flip flop នឹងត្រូវបាន



अवक्षणीय wave from diagram



၃ ဂေါ်ခြားကိစ္စပါန်အတွက်များကိစ္စပါန်အတွက်များ

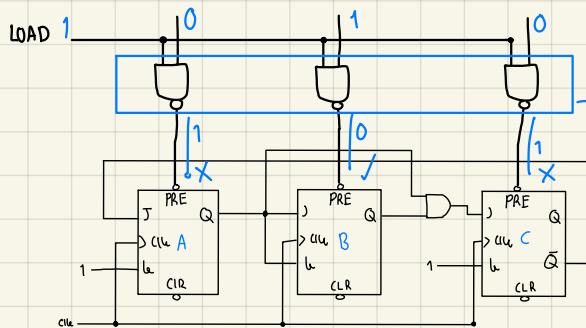
↳ ຖົກ process ເຊີ່ມແລ້ວຈຳ

$\hookrightarrow \text{analog mod } 60 \text{ gibt} =$

↳ $n \bmod 10$ යේ $n \bmod 6$ නිස්සුදුකුරු වේ \rightarrow නැංවා තුළු යොමු යුතු වනු ඇත?

↳ mergescencias (LR que más clearance)

↳ ຕອບຖິ່ນເລີຍໃຫ້ PRE \rightarrow ເຊື້ອ $\overline{\text{PRE}} = 1$, $\overline{\text{CTR}} = 0$ ເພີ້ມໃຈກວ່າ ມີ preset \rightarrow ມີຫຼຸດ Q ສໍາເລັດທີ່ 1.



$\bar{m} \text{ PRE} = 1$, $Q = 1 \rightarrow$ ຕັດສົງ 0 ດັວກເຮົາວິວໆນຳເຢີມ 1

\rightarrow if O output = 1 $\rightarrow \overline{PRE} = O \rightarrow$ q1n1

NAND , Neg -OR

Top-down Design

→ ឧបតម្យរាងនរចងកំពុង → តែង ។ នៅទីនាំរាជការណាត់បាន

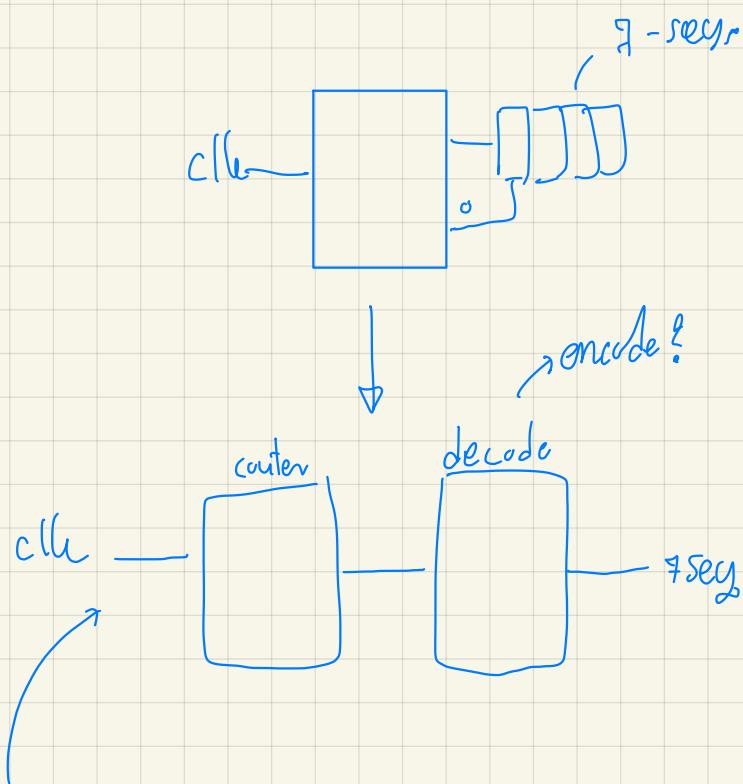
↳ get input នូវលទ្ធផល ដើម្បីសំនើ នឹងចិញ្ញាបាន សម្រួលបានឡើងបីនូវ

↳ ការងារទាមទីនេះបានបាន

↳ output តីវត្ថុ

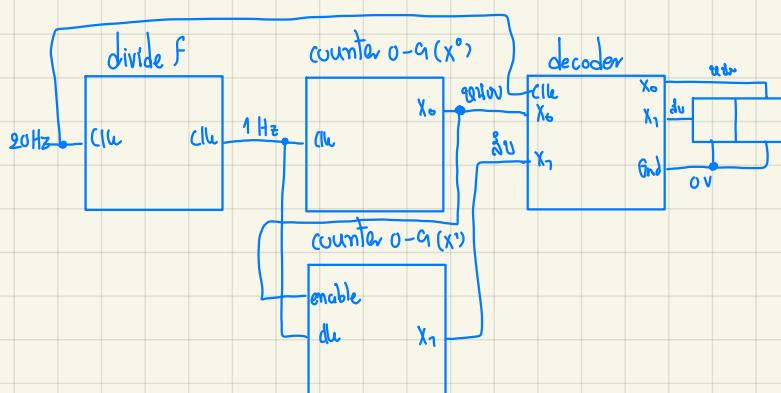
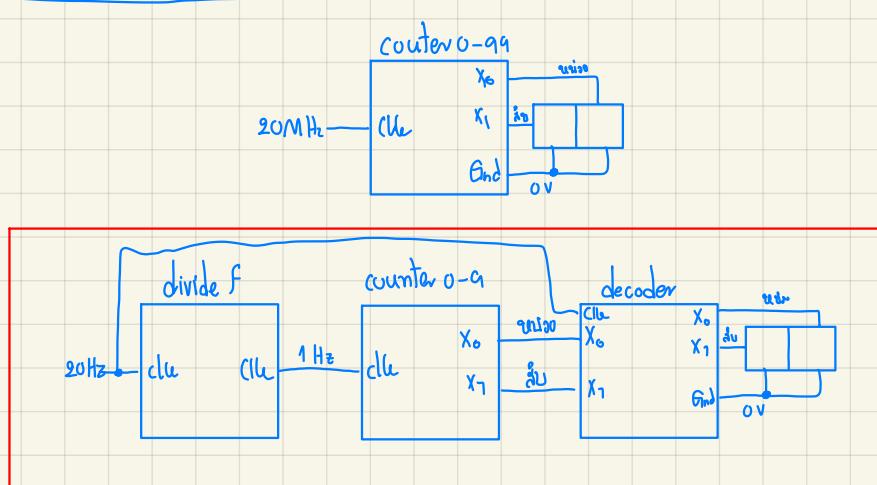
↳ top level design

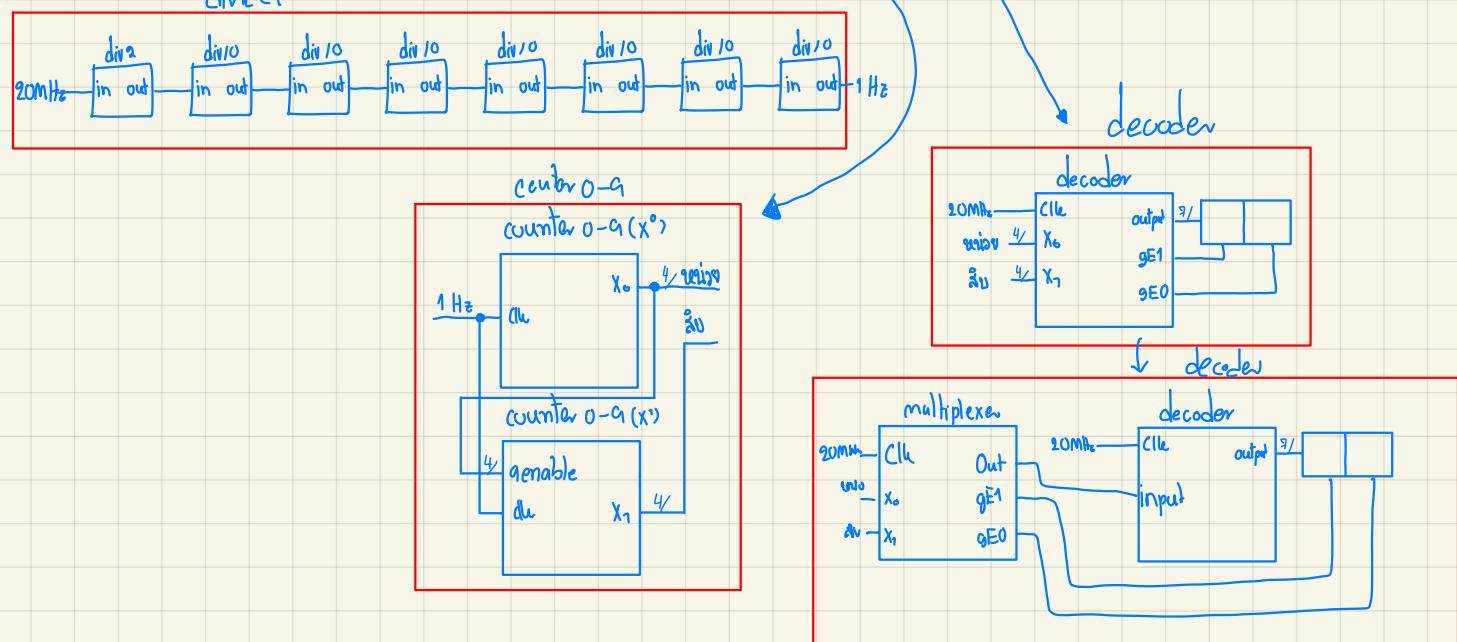
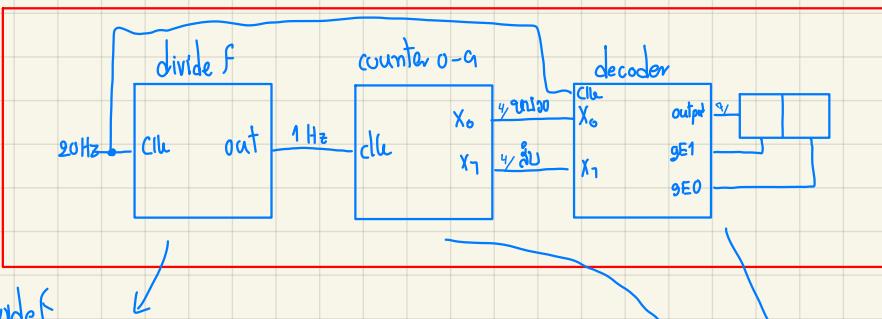
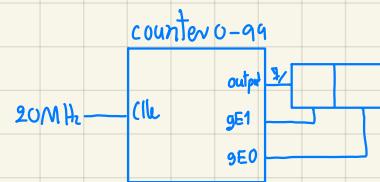
↳ input, output



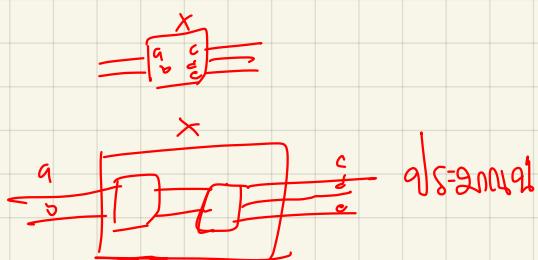
ជាការការងារមាន 3 ការងារទាមទី ការបង្កើតនៃការងារ កំនត់នូវការងាររបស់ខ្លួន

លើសរាក់តាមគន់ ការងារនូវនៅទីនាំរាជការណាត់បាន





9 terms break down into 3 terms involving ∂_{μ} and 6 terms involving ∂_{ν}



Interfacing with analog world

↳ ເນື້ອງໄລຍະໄສ່ເກີດຂຶ້ນຂອງໂຄງລິນ, ລາຍກໍາໃຫຍ່ວ່າ digital to analog converter (DAC)

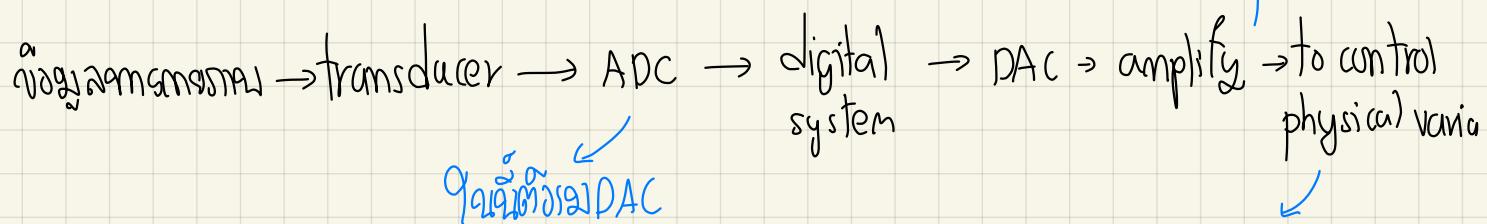
↳ අනුරූප-ඇජ්ඩැස් වියා අනුලෝධ ප්‍රාග්ධන ප්‍රාග්ධනය (ADC)

↳ digital quantities (ເລກທີ່ມີໂຄງການ) set ອຳນັດ

analog quantities $n(\text{aq}) = \infty$ ເຊັ່ນເວັບໄມ້ຮັດວຽກໃກ້

↳ ពីរការងាររបស់ខ្លួន សំណងការទិន្នន័យ analogy ទីផ្សាររាជ (មិន) នៃទីផ្សារ

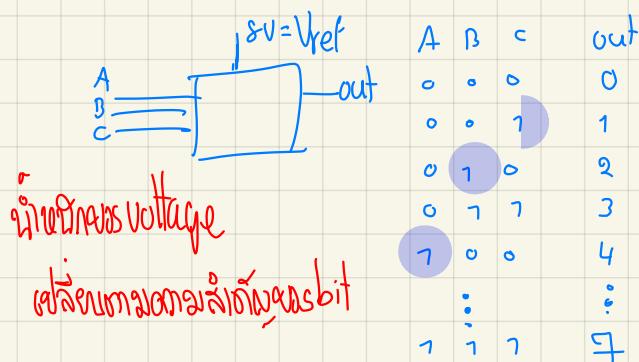
Ե զայտ transducer-ը ուղարկում է առաջացած համապատճենական ազդակը՝ այս ժամանակակից այլ



↳ analog to digital conversion សម្រាប់ការបន្ថែមនូវជុលដំឡើង digital to analog conversion

↳ when DAC Y is connected to output we get digital analog quantities

↳ ເນັດ-ວ່າສູນສຳລັກ ຢາໂຮງດໍາຕຽມຈົດ



(ғілдір) 000, 011, 111

and $g_{\mu\nu}$

2's complement

$$g'(x) = \frac{1}{x} + -\frac{1}{x^2}$$

ຈຳລັງການຕົວອາໄຫາວິທະຍາ analog out = $K \times \text{bit}^{\frac{1}{2}}$ ດີເລີດ ດ້ວຍ DAC

furex : = 1×2^3

ၶ ဂျက်စာမျက်နှာမျက်နှာတွင် (output) လေဆိပ်အောက်မှာ တော်မြေတွင် ပေါ်လေသူများ၏ bit တို့၏

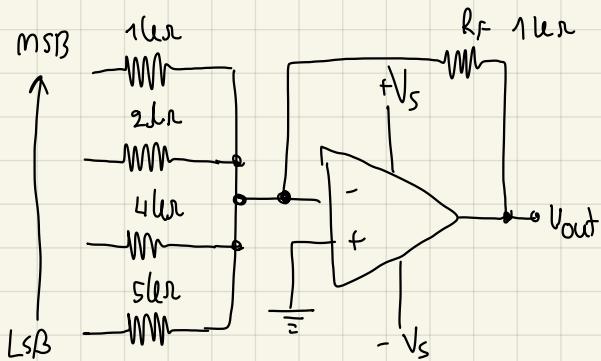
ແລ້ວຮັບໄຫຍ້ກ ລາຍລະອຽດໃນ output ໃຕ່ຈະກາເຊີ້ມຈຳນວຍ bit ອີເມວິເຄີຍເຫຼືອ

↳ ឧបតម្យនៃ analog output នៅក្នុងការបន្ទាន់ទូទៅជា digital input នៅក្នុងការបន្ទាន់

↳ សិរី input រាយការណ៍ 2 និងខាងក្រោម step = 4 , 4 ជាន់លាត់ 16 នៃអាសន្នខ្លួន } ទាក់ទង នូវ សិរី

↳ մասնաւում

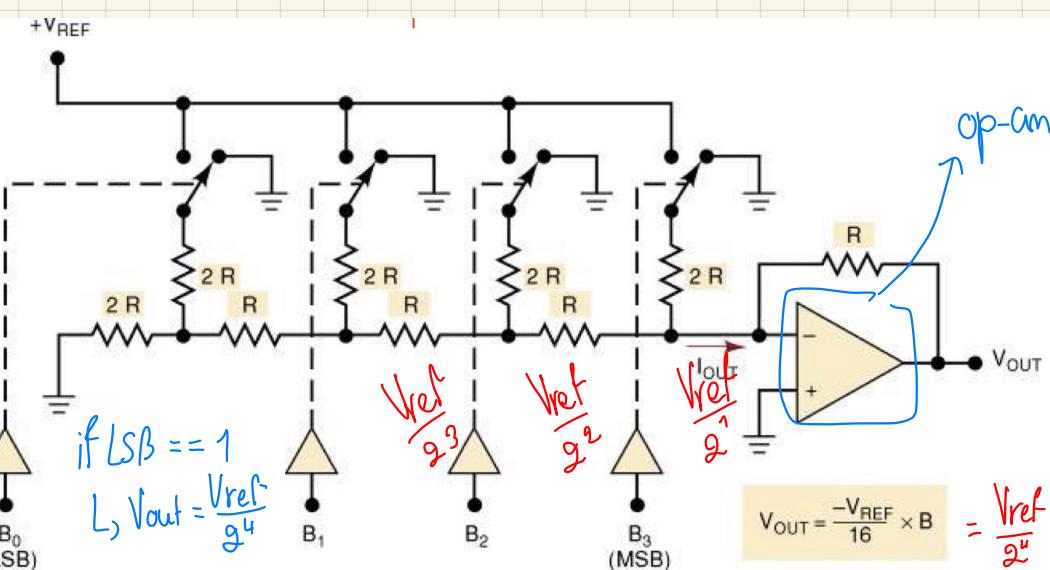
↳ Առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային



Հենց այս տեսքում առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

↳ Եթե առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

↳ այս դեպքում առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

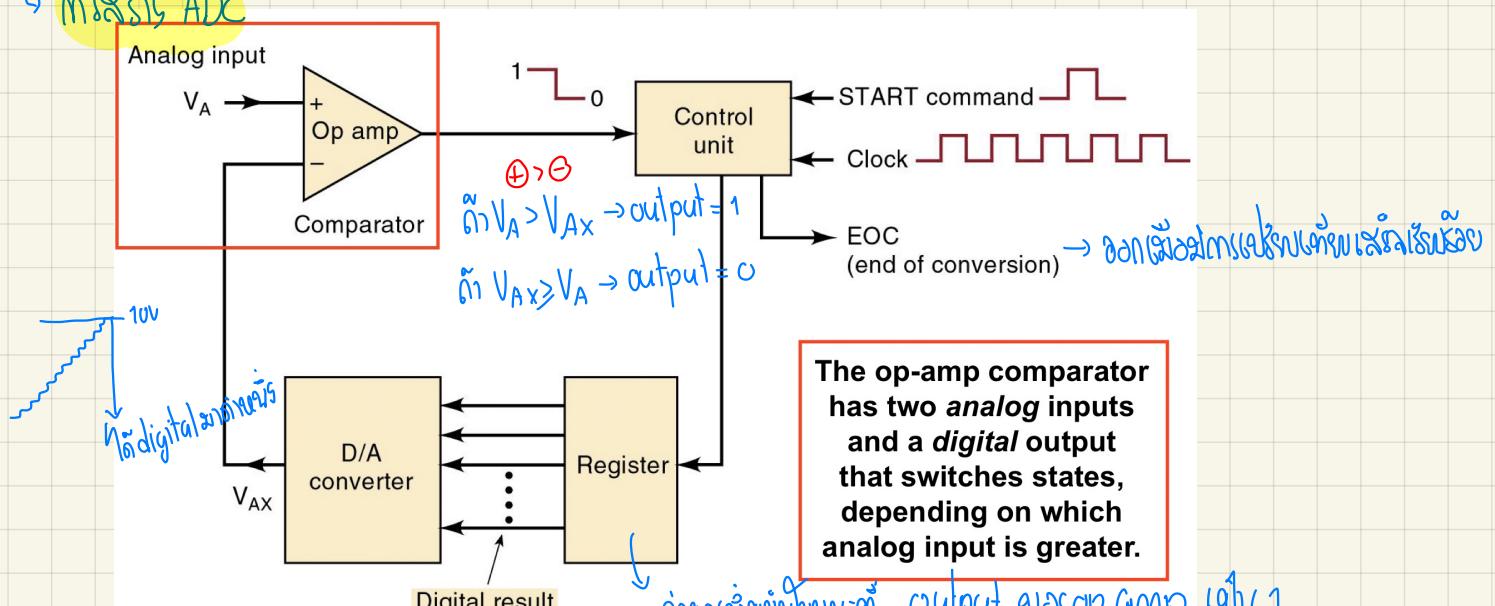


Հենց այս տեսքում առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

$$V_{OUT} = \frac{-V_{REF}}{2^4} + \frac{V_{ref}}{2^3} + \frac{V_{ref}}{2^2} + \frac{V_{ref}}{2^1}$$

↳ 9 զանումներում thevenin, northon գամացցված չեն R, v կամ այլ համար կամ 10v ...

↳ մասնաւում ADC



The op-amp comparator has two analog inputs and a digital output that switches states, depending on which analog input is greater.

↳ առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

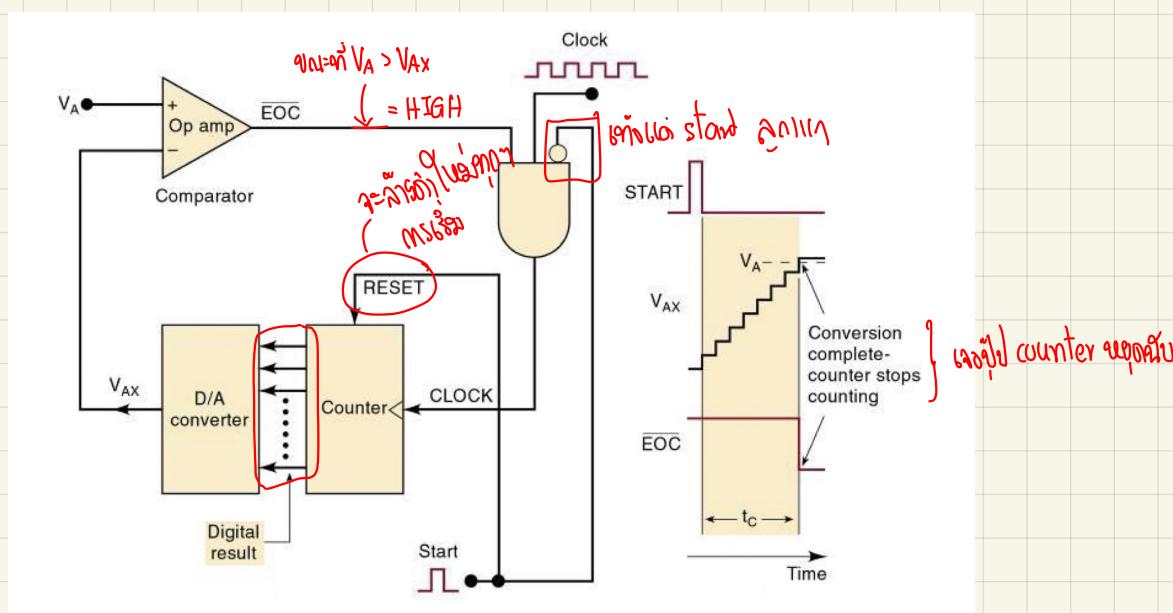
↳ բինար քայլական պատճեն

↳ այս դեպքում առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

Հենց այս տեսքում առաջնային արժեքը կազմությունը է օպ-ամպ սեղմանական լուսային

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↳ ឧបករណីស្ថាបន់ដែលត្រូវបានបង្កើតឡើងដើម្បីបង្កើតការប្រើប្រាស់ ឬការចំណាំស្ថាបន់។

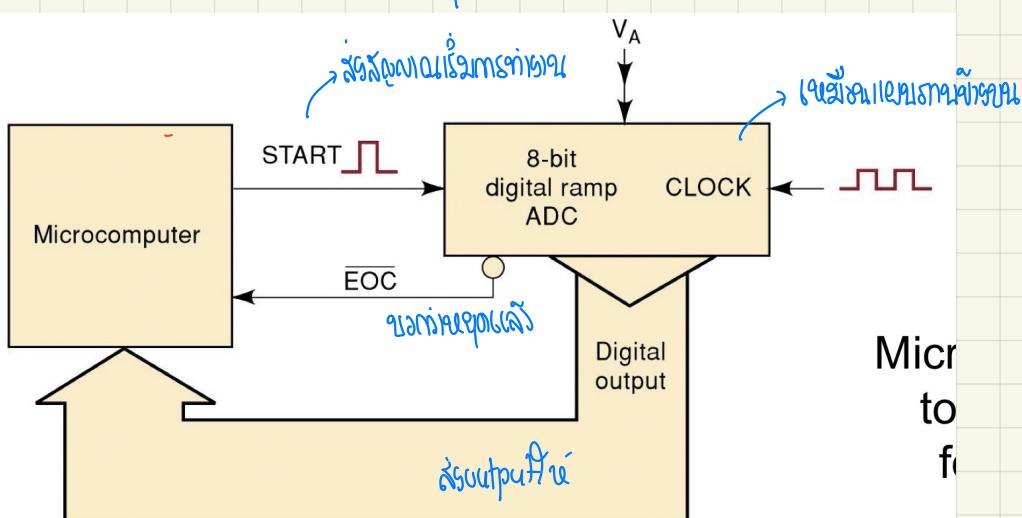


↳ ស្ថាបន់ត្រូវបានបង្កើតឡើង ដើម្បី បានប្រើប្រាស់ ឬការចំណាំស្ថាបន់

10V
9.5V
9V

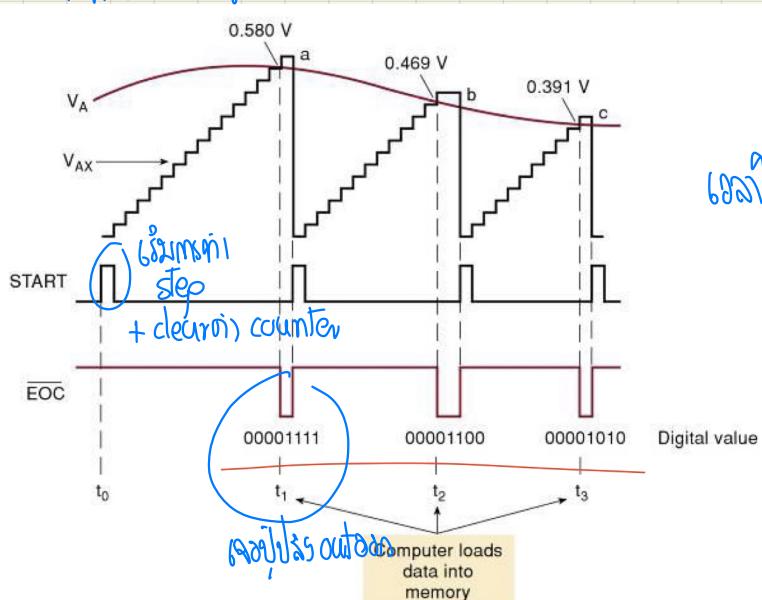
} ពីរបីការបង្កើតឡើង = ផ្ទាល់តម្លៃទិន្នន័យ កំពុងតិចជាមួយ 10 bit
↳ ភាពខ្លួន = គ្រាងការក្នុងការបង្កើតឡើង

នៅថ្មីការ quantization error



Micro
to
fe

នាយករណ៍នៅរបស់ខ្លួន



គ្រប់គ្រងទិន្នន័យ 3 គ្មាន

ការបង្កើតឡើង

សំណងចាត់បិទនា = មិនចូលទៅ



ms reconstruction

យើង wavefrom របស់ខ្លួន

សារការណ៍ C (ដែងទេរសព្វនៃការបង្កើតមេន្តរបាល)

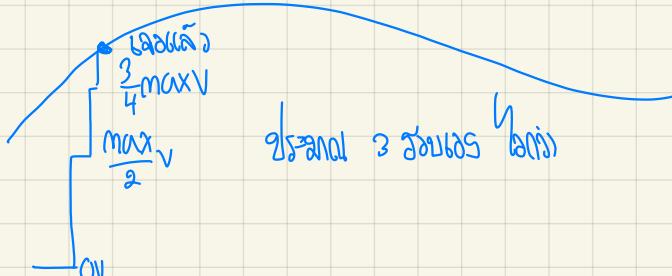
↓ អាជីវិតបាន sampling នៃ data គាំទ្រ → នាយកដោយសាមញ្ញ នៅទីនេះ

↳ បិទអាជីវិតមេន្តរសព្វនៃការបង្កើត / ពីរនាមីតុល linear search

↳ បិទអាជីវិតសព្វនៃការបង្កើត binary search នៅទីនេះ

↳ បិទលេខា

↳ ក្រឡើងក្រក successive - approximation converter



ក្រឡើងក្រក នៅទីនេះ

↓ បិទអាជីវិតមេន្តរសព្វនៃការបង្កើត MSB នូវា

↳ និង algorithm តើម្បី

- ① ស្រួល
- ② clear all bit
- ③ ស្រួលម៉ោង MSB
- ④ កើតឡើង bit មីនីមិន 1
- ⑤ $V_{AX} > V_A$ ឱ្យលើ \rightarrow នាំស្រួល \rightarrow ការស្រួលម៉ោងមីនីមិន 0
- ⑥ ស្រួលម៉ោងបន្ថែមបន្ថែមឡើងឡើង
- ⑦ ឱ្យលើក្រឡើងក្រកនៃ register និងលើ

និង

0 0 0 0

0 0 0 1

0 0 1 0

0 0 1 1

0 1 0 0

0 1 0 1

0 1 1 0

0 1 1 1

0100

1 0 0 0

1 0 0 1

1 0 1 0

1 0 1 1

1 1 0 0

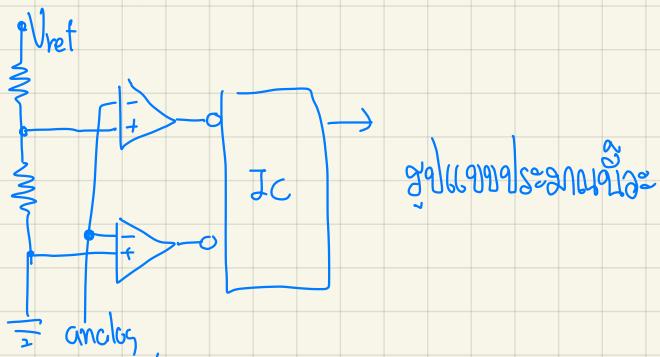
② ឱ្យលើក្រក នៅទីនេះ \rightarrow កើតឡើងក្រក \rightarrow set មីនា # 011

→ ចុចកម្មលើក្រក ④ $V_{AX} > V_A = \text{False} \rightarrow$ ស្រួលម៉ោងមីនីមិន ? \rightarrow ឱ្យលើក្រក នៅទីនេះ \rightarrow នាំស្រួល \rightarrow 010

1000

① ឱ្យលើក្រក $V_{AX} > V_A \rightarrow$ ការស្រួលម៉ោងបន្ថែមឡើងឡើង \rightarrow ការស្រួលម៉ោងបន្ថែម \rightarrow កើតឡើងក្រក

- ↳ The flash converter
- ↳ high speed analog to digital converter (ADC)

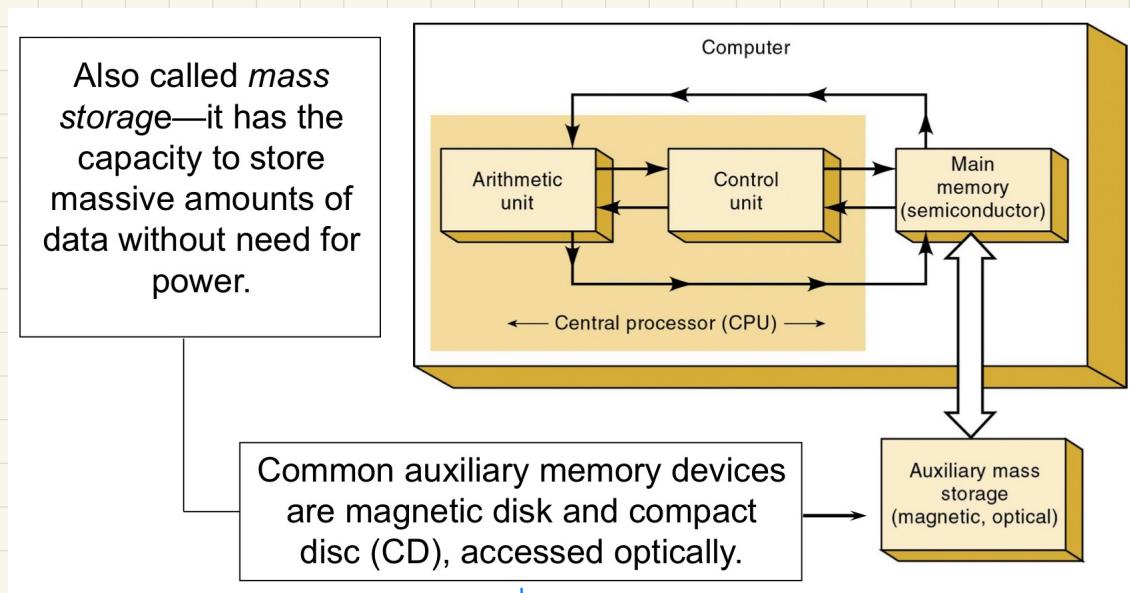


input သိမ်း output ပုံစံနည်းလမ်းအတွက်
ပုံပေါ်အတွက်အမြတ်ဆုံး

- ↳ ရွှေ့ယူလွှာချိန်အတွက်အမြတ်ဆုံး clock
- ↳ မီး၏ input voltage ပြောလုပ်နည်း၏ output အား comparator ပြောလုပ် စိုက်ပိုင် decoder output ဖော်လုပ်လဲ
- ↳ တိုင်းတက်မှတ် delay ပော်ပြန်မှုများ
- ↳ ဒုံး → ဘေးလွှာချိန်၊ ပေါ်လုပ်

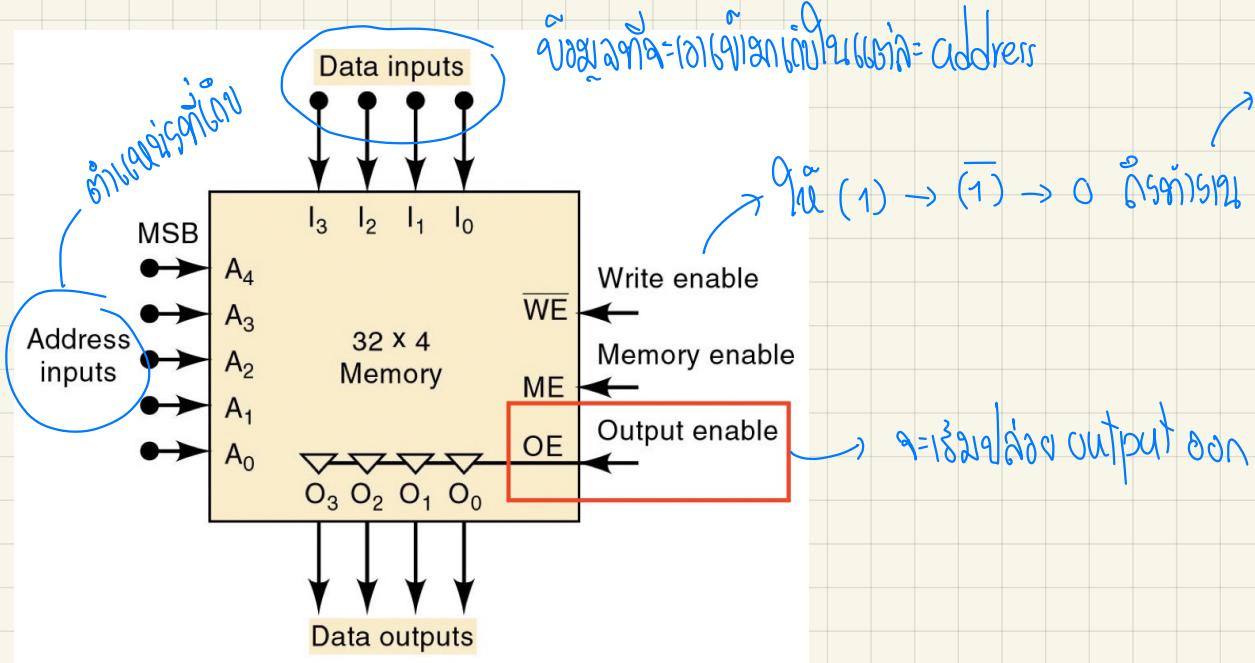
Memory devices

- ↳ memory terminology (ဂုဏ်ပိုင်)
- ↳ အိုအုန္တ (digital) ဆောင်တို့၏ ပေါ်လုပ်များ များ

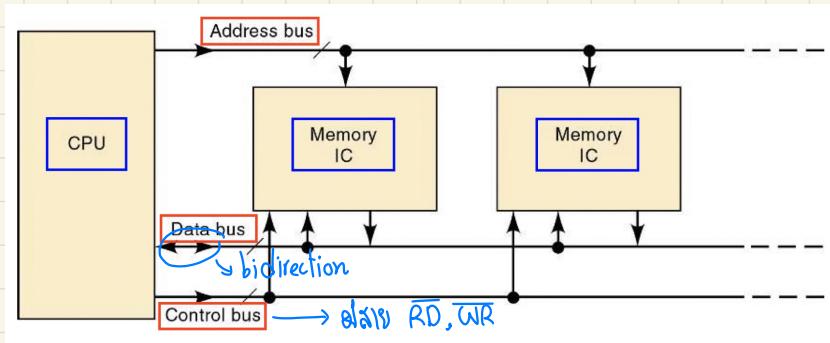


- ↳ memory cell → a device used to store a single bit (0, 1)
- ↳ မှတ်ထုတ်၊ charged capacitor, magnetic tape or disc
- ↳ memory word → a group of bit (cells) in a memory, represents instruction or data
- ↳ capacity → a way specifying how many bits can be stored
 - ↳ another term → density
- ↳ address → a number that identifies the location of a word in memory

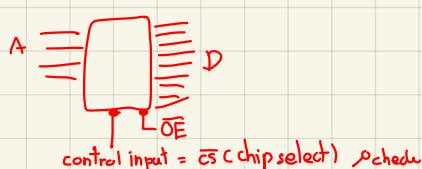
- ↳ read operation (ນຳອັນດີ)
- ↳ write operation (ນຳພົບ)
- ↳ access time
 - ↳ ເລືດທີ່ຈະມີສຳເນົາໃຫຍ້ output
- ↳ Volatile memory
 - ↳ any memory that requires application of electrical power to store information
 - ↳ If there is no power, information will be lost
- ↳ Random Access Memory (RAM)
- ↳ Read Only Memory (ROM)
 - ↳ designed for application with a high ratio read/write operation
- ↳ Sequential Access Memory (SAM)
 - ↳ ມີສຳເນົາດ້ວຍຕົວເລີນກົງ → ອັນ hard disk
- ↳ Read Write Memory (RWM)
 - ↳ ຂໍມານໄສຫຼຸດ & ດ້ວຍມີສຳເນົາໄດ້
- ↳ General memory operation



- ↳ CPU Memory Connections
- ↳ main memory is interfaced to the CPU through : address bus, data bus, control bus
- ↳ These bus allow CPU to read and write data to the memory



- ↳ மெம்பையின் இயங்கல்
 - ↳ சிகிச்சை வழி address bus
 - ↳ address decoder activate the enable input (E)
 - ↳ போடுவதற்கு தகுதி வழி data bus → போடுவதற்கும் போன்று
 - ↳ activate சிகிச்சை வழி control line என்று சொல் (\bar{WR} or R/W)
 - X ↳ Memory IC internally decode the binary address to determine the location selected for the operation.
 - ↳ விடுவதற்கு தகுதி வழி data bus யினால் மெம்பை நிர்ணயித்து
 - ↳ மெம்பையின் இயங்கல்
 - ↳ போடுவதற்கு தகுதி வழி address bus
 - ↳ address decoder activate the memory device's enable input (CE)
 - ↳ சிகிச்சை வழி control ஒரு சிகிச்சை (நீண்ட நிலை, மூன்று நிமிட)
 - ↳ data மெம்பையின் இயங்கல் வழி data bus (போடுவதற்கு சிகிச்சை வழி)
- ↳ read only memories
- ↳ memory which designed to hold data that are permanent or will not change frequently.
- ↳ போடுவதற்கு தகுதி வழி burning the ROM
- ↳ விடுவதற்கு தகுதி வழி nonvolatile → programs are not lost when electrical power is turned off
 - ↳ போடுவதற்கு தகுதி வழி ram → விடுவதற்கு தகுதி வழி address, சிகிச்சை control input



control input = CS (chip select) = select

↳ internal architecture → of 4 part

↳ ① register array

↳ ລົງທຶນລາຍກິດຂອງລະບົບຂອງ ROM

↳ each register contain memory cells equal to word size

② address decoder

↳ one register will be in both row & column selected

③ Output buffer

↳ pass data to an external data output

↳ data → data bus → data buffer → data output

↳ Type of ROM

↳ Mask programmed ROM (MROM)

↳ ຂໍ້ມູນຂອງ ROM

1's complement

↳ ការសែរតាមលក្ខណៈមិនមែន 0 នៅ not gate

Signed Number

ចំណាំសែរ + 0 } នៅលើមាត្រាអនុវត្តន៍ 0 } កំណុំលើតីវា magnitude ដូច ចំណាត់ថ្នាក់ថ្វីនៅក្នុង
ដីលើបច្ចេក 3 លួយ $2^4 = 16$ ពីរ possible

↳ ឲ្យជា signed magnitude នៅលើ 1's complement

+7	0 1 1 1
+6	0 1 1 0
+5	0 1 0 1
+4	0 1 0 0
+3	0 0 1 1
+2	0 0 1 0
+1	0 0 0 1
+0	0 0 0 0
-0	1 0 0 0
-1	1 0 0 1
-2	1 0 1 0
-3	1 0 1 1
-4	1 1 0 0
-5	1 1 0 1
-6	1 1 1 0
-7	1 1 1 1
-8	

ចាប់មើលពី 0 ដល់ -8
ប៉ុន្មានបញ្ជី -8
ប៉ុន្មានបញ្ជី -8

0 1 1 1
0 1 1 0
0 1 0 1
0 1 0 0
0 0 1 1
0 0 1 0
0 0 0 1
0 0 0 0

នៅលើ 2's complement

0 1 1 1
0 1 1 0
0 1 0 1
0 1 0 0
0 0 1 1
0 0 1 0
0 0 0 1
0 0 0 0

-
1 1 1 1
1 1 1 0
1 1 0 1
1 1 0 0
1 0 1 1
1 0 1 0
1 0 0 1
1 0 0 0

ក្រឡាលើ 1's complement

↳ ក្នុង $1 + (-\square) \rightarrow \square$ 1's complement

↳ EAC $\rightarrow \oplus 1$

$$\begin{array}{l} 3 - 7 \quad 0111 \\ 3 + (-7) \quad 1^c \\ 0011 \quad 1000 = -7 \\ \hline \boxed{[0111]} \oplus 1 \\ \boxed{1000} = -4 \end{array}$$

on 2's complement
EAC

$$(1^c) - (3)_2$$

$$\begin{array}{r} 1100 \\ 1101 \\ + 1100 \\ \hline 1101 \end{array}$$

តើខ្លួន EAC \rightarrow នឹងបង់លើលើលើ +

$$\begin{array}{r} 2^4 \\ \times 11 \\ \hline 10 + 10 \\ = 9 \end{array}$$

$$\begin{array}{r} 4 - 7 \\ 0100 \quad 011 \\ 1001 \quad \end{array}$$

$$\begin{array}{r} 0100 \\ 1001 \\ \hline \boxed{1101} \end{array}$$

$$\begin{array}{r} 4 - 7 \\ 0100 \quad 011 \\ 1001 \\ \hline \boxed{101} \end{array}$$

ກອງມີເລກສົດ 10 ເພື່ອມີຜົນໄດ້

$$\begin{array}{r} 4 \\ \times 2 \\ \hline 8 \end{array}$$
$$\begin{array}{r} 0100 \\ \times 0010 \\ \hline 0000 \\ + 0100 \\ \hline 1000 = 8 \end{array}$$

} 16bit Unsigned

ມີຜົນໄດ້

$$\begin{array}{r} 010 \\ \div 10 \\ \hline 10 \\ 10 \\ \hline 00 \\ = 010 = 2 \end{array}$$

BCD ອົບເລກສົດ 10 ເພື່ອມີຜົນໄດ້

15₁₀

$$BCD \rightarrow 0001 \ 0101$$

ມີຜົນ BCD
ຕົວຢ່າງທີ່ມີຜົນ 9 ດັ່ງນີ້

$$\begin{array}{r} 9+1 \\ \hline 1001 \\ 0001 + \\ \hline 1010 \end{array}$$

ມີຜົນ BCD

ມີຜົນລາຍລະອຽດ 16

ALU ບໍ່?

9₁₀ ແລ້ວ
 $\begin{array}{r} 0101 \\ \oplus \\ 0101 \end{array}$ 9₁₀ 2's complement ຂອງ

$$+4 +1 = 5$$

$$\begin{array}{r} 011 \\ \oplus \\ 101 \\ \hline 011 = 3 \rightarrow -3 \end{array}$$

} 16bit 0 ໃຫຍ່າຍັນ 1 ອິນເລີຍ 9₁₀ 2's complement ຂອງ

$$\begin{array}{r} 1111 \\ \ominus \\ 001 \\ \hline 001 = 1 = \ominus 1 \end{array}$$