

# TLV62085 采用 2mm × 2mm VSON 封装的高效 3A 降压转换器

## 1 特性

- DCS-Control™拓扑
- 效率高达 95%
- 17 $\mu$ A 工作静态电流
- 31m $\Omega$  和 23m $\Omega$  功率金属氧化物半导体场效应晶体管 (MOSFET) 开关
- 输入电压范围: 2.5V 至 6.0V
- 可调输出电压: 0.8V 至  $V_{IN}$
- 可在轻载条件下实现高效率的省电模式
- 可实现 100% 占空比, 以确保最低压降
- 自动切断短路保护功能
- 输出放电
- 电源正常输出
- 热关断保护
- 采用 2mm × 2mm 超薄小外形尺寸无引线 (VSON) 封装
- 如需了解改进的特性集, 请参见 [TPS62085](#)
- 借助 [WEBENCH® Power Designer](#) 并使用 [TLV62085](#) 创建定制设计方案

## 2 应用

- 电池供电类应用
- 负载点
- 处理器电源
- 传统硬盘 (HDD)/固态硬盘 (SSD)

## 3 说明

TLV62085 器件是一款高频同步降压转换器, 经优化具有小解决方案尺寸和高效率两大优点。该器件具有 2.5V 至 6.0V 的输入电压范围, 支持常见的电池技术。此器件主要用于宽输出电流范围内的高效降压转换。该转换器在中等程度的负载到高负载时运行于脉宽调制 (PWM) 模式, 并在轻负载时自动进入省电模式运行, 从而在整个负载电流范围内保持高效率。

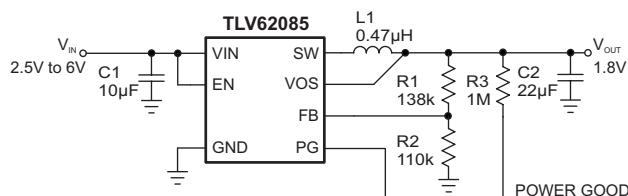
为了满足系统电源轨的需求, 内部补偿电路支持宽范围的外部输出电容值选项, 10 $\mu$ F 到 150 $\mu$ F 甚至更高。加上其 DCS-Control™ 架构, 出色的负载瞬态性能和精确的输出电压调整均可实现。此器件采用 2mm × 2mm VSON 封装。

### 器件信息<sup>(1)</sup>

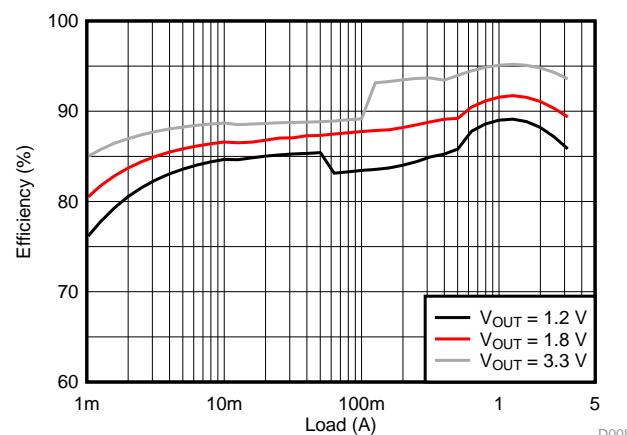
器件型号	封装	封装尺寸 (标称值)
TLV62085	VSON (7)	2.00mm × 2.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



$V_{IN} = 5V$  时的效率



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## 目 录

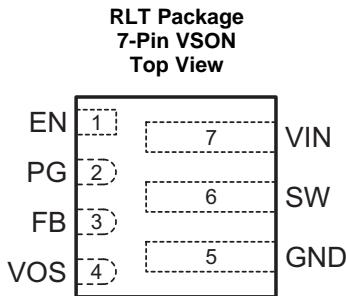
<b>1</b>	特性 .....	1
<b>2</b>	应用 .....	1
<b>3</b>	说明 .....	1
<b>4</b>	修订历史记录 .....	2
<b>5</b>	Pin Configuration and Functions .....	3
<b>6</b>	Specifications .....	4
6.1	Absolute Maximum Ratings .....	4
6.2	ESD Ratings .....	4
6.3	Recommended Operating Conditions .....	4
6.4	Thermal Information .....	4
6.5	Electrical Characteristics .....	5
6.6	Typical Characteristics .....	5
<b>7</b>	Detailed Description .....	6
7.1	Overview .....	6
7.2	Functional Block Diagram .....	6
7.3	Feature Description .....	7
7.4	Device Functional Modes .....	8
<b>8</b>	Application and Implementation .....	9
8.1	Application Information .....	9
8.2	Typical Application .....	9
<b>9</b>	Power Supply Recommendations .....	15
<b>10</b>	Layout .....	15
10.1	Layout Guidelines .....	15
10.2	Layout Example .....	15
10.3	Thermal Considerations .....	15
<b>11</b>	器件和文档支持 .....	16
11.1	开发支持 .....	16
11.2	文档支持 .....	16
11.3	接收文档更新通知 .....	16
11.4	社区资源 .....	16
11.5	商标 .....	16
11.6	静电放电警告 .....	16
11.7	术语表 .....	16
<b>12</b>	机械、封装和可订购信息 .....	17

## 4 修订历史记录

Changes from Revision A (January 2017) to Revision B	Page
• 已添加 图 3 to power save mode section .....	7

Changes from Original (October 2015) to Revision A	Page
• 已添加 WEBENCH™ 信息和超链接至特性、详细设计流程和器件支持部分 .....	1
• Added SW (AC) to the Absolute Maximum Rating table .....	4
• 已添加 表 1, PG Pin Logic .....	8

## 5 Pin Configuration and Functions



### Pin Functions

<b>PIN</b>		<b>I/O</b>	<b>DESCRIPTION</b>
<b>NAME</b>	<b>NO.</b>		
EN	1	IN	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. This pin has a pulldown resistor of typically 400 kΩ when the device is disabled.
FB	3	IN	Feedback pin. Connect a resistor divider to set the output voltage.
GND	5		Ground pin.
PG	2	OUT	Power good open drain output pin. The pullup resistor can not be connected to any voltage higher than 6 V. If unused, leave it floating.
SW	6	PWR	Switch pin of the power stage.
VIN	7	PWR	Input voltage pin.
VOS	4	IN	Output voltage sense pin. This pin must be directly connected to the output capacitor.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage at Pins <sup>(2)</sup>	VIN, FB, VOS, EN, PG	-0.3	7	V
	SW (DC)	-0.3	$V_{IN} + 0.3$	
	SW (AC, less than 100ns) <sup>(3)</sup>	-3	11	
Temperature	Operating Junction, $T_J$	-40	150	°C
	Storage, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) While switching.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	$\pm 500$

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

	MIN	NOM	MAX	UNIT
$V_{IN}$ Input voltage range	2.5		6	V
$V_{OUT}$ Output voltage range	0.8		$V_{IN}$	V
$I_{SINK\_PG}$ Sink current at PG pin			1	mA
$V_{PG}$ Pullup resistor voltage			6	V
$T_J$ Operating junction temperature	-40		125	°C

- (1) Refer to [Application and Implementation](#) for further information.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TLV62085	UNIT
	RLT [VSON]	
	7 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(\text{top})}$ Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	17.1	°C/W
$\Psi_{JT}$ Junction-to-top characterization parameter	2.1	°C/W
$\Psi_{JB}$ Junction-to-board characterization parameter	17.1	°C/W
$R_{\theta JC(\text{bot})}$ Junction-to-case (bottom) thermal resistance	N/A	°C/W

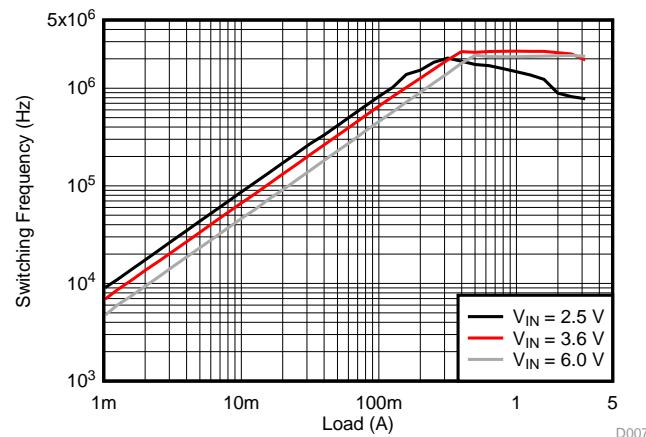
- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$T_J = 25^\circ\text{C}$ , and  $V_{IN} = 3.6\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY</b>							
$I_Q$	Quiescent current into $V_{IN}$	No load, device not switching		17		$\mu\text{A}$	
$I_{SD}$	Shutdown current into $V_{IN}$	$EN = \text{Low}$		0.7		$\mu\text{A}$	
$V_{UVLO}$	Under voltage lock out threshold	$V_{IN}$ falling	2.1	2.2	2.3	$\text{V}$	
	Under voltage lock out hysteresis	$V_{IN}$ rising		200		$\text{mV}$	
$T_{JSD}$	Thermal shutdown threshold	$T_J$ rising		150		$^\circ\text{C}$	
	Thermal shutdown hysteresis	$T_J$ falling		20		$^\circ\text{C}$	
<b>LOGIC INTERFACE EN</b>							
$V_{IH}$	High-level input voltage	$V_{IN} = 2.5\text{ V to }6.0\text{ V}$	1.0			$\text{V}$	
$V_{IL}$	Low-level input voltage	$V_{IN} = 2.5\text{ V to }6.0\text{ V}$		0.4		$\text{V}$	
$I_{EN,LKG}$	Input leakage current into EN pin	$EN = \text{High}$		0.01		$\mu\text{A}$	
$R_{PD}$	Pull-down resistance at EN pin	$EN = \text{Low}$		400		$\text{k}\Omega$	
<b>SOFT START, POWER GOOD</b>							
$t_{SS}$	Soft start time	Time from EN high to 95% of $V_{OUT}$ nominal		0.8		$\text{ms}$	
$V_{PG}$	Power good threshold	$V_{OUT}$ rising, referenced to $V_{OUT}$ nominal	95%				
		$V_{OUT}$ falling, referenced to $V_{OUT}$ nominal	90%				
$V_{PG,OL}$	Low-level output voltage	$I_{sink} = 1\text{ mA}$		0.4		$\text{V}$	
$I_{PG,LKG}$	Input leakage current into PG pin	$V_{PG} = 5.0\text{ V}$		0.01		$\mu\text{A}$	
<b>OUTPUT</b>							
$V_{FB}$	Feedback regulation voltage	$PWM$ mode, $2.5\text{ V} \leq V_{IN} \leq 6\text{ V}$ $T_J = 0^\circ\text{C to }85^\circ\text{C}$	792	800	808	$\text{mV}$	
$I_{FB,LKG}$	Feedback input leakage current	$V_{FB} = 1\text{ V}$		0.01		$\mu\text{A}$	
$R_{DIS}$	Output discharge resistor	$EN = \text{LOW}$ , $V_{OUT} = 1.8\text{ V}$		260		$\Omega$	
<b>POWER SWITCH</b>							
$R_{DS(on)}$	High-side FET on-resistance	$I_{SW} = 500\text{ mA}$		31		$\text{m}\Omega$	
	Low-side FET on-resistance	$I_{SW} = 500\text{ mA}$		23		$\text{m}\Omega$	
$I_{LIM}$	High-side FET switch current limit			3.7	4.6	5.5	$\text{A}$
$f_{SW}$	PWM switching frequency	$I_{OUT} = 1\text{ A}$		2.4		$\text{MHz}$	

## 6.6 Typical Characteristics



$V_{OUT} = 1.2\text{ V}$

图 1. Switching Frequency

## 7 Detailed Description

### 7.1 Overview

The TLV62085 synchronous step-down converter is based on the DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's current consumption to achieve high efficiency over the entire load current range. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. The device offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

### 7.2 Functional Block Diagram

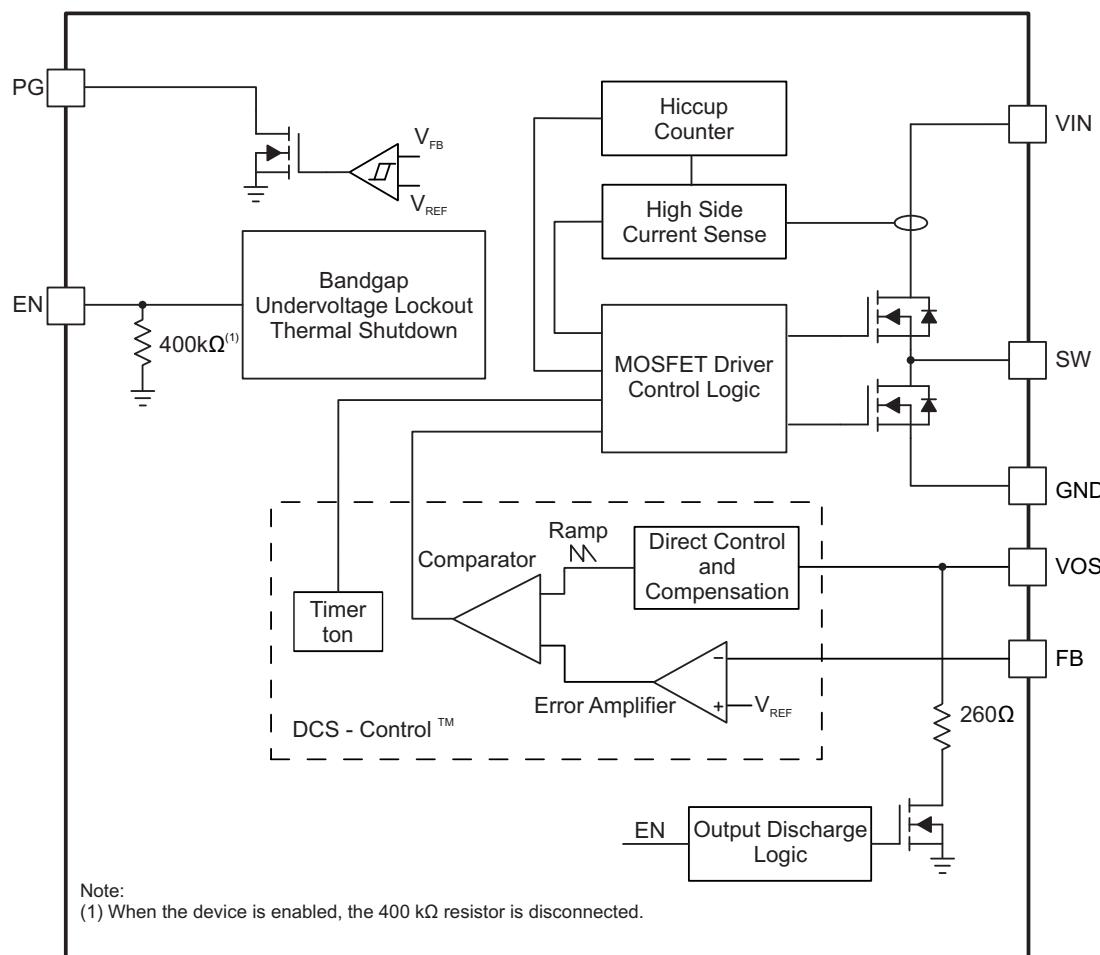


图 2. Functional Block Diagram

## 7.3 Feature Description

### 7.3.1 Power Save Mode

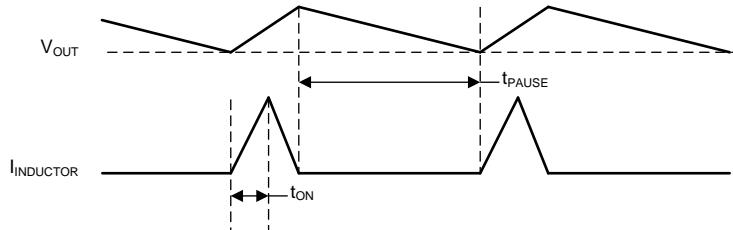
As the load current decreases, the TLV62085 enters Power Save Mode (PSM) operation. During Power Save Mode, the converter operates with reduced switching frequency and with a minimum quiescent current maintaining high efficiency. Power Save Mode occurs when the inductor current becomes discontinuous. Power Save Mode is based on a fixed on-time architecture, as related in [公式 1](#). The switching frequency over the whole load current range is also shown in [图 1](#) for a shown typical application.

$$t_{ON} = 420 \text{ ns} \times \frac{V_{OUT}}{V_{IN}}$$

$$f_{PFM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}}$$
(1)

In PSM, the output voltage rises slightly above the nominal output voltage, as shown in [图 10](#). This effect is minimized by increasing the output capacitor or inductor value.

During PAUSE period in PSM (shown in [图 3](#)), the device does not change the PG pin state nor does it detect an UVLO event, in order to achieve a minimum quiescent current and maintain high efficiency at light loads.



**图 3. Power Save Mode Waveform Diagram**

### 7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L)$$

with

- $V_{IN,MIN}$  = Minimum input voltage to maintain an output voltage
  - $I_{OUT,MAX}$  = Maximum output current
  - $R_{DS(on)}$  = High-side FET ON-resistance
  - $R_L$  = Inductor ohmic resistance (DCR)
- (2)

### 7.3.3 Soft Start

The TLV62085 has an internal soft-start circuitry which monotonically ramps up the output voltage and reaches the nominal output voltage during a soft-start time of typically 0.8 ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to its nominal value.

## Feature Description (接下页)

### 7.3.4 Switch Current Limit and Hiccup Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold  $I_{LIM}$ , the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. When this switch current limits is triggered 32 times, the device stops switching and enables the output discharge. The device then automatically starts a new start-up after a typical delay time of 66  $\mu$ s has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

### 7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than  $V_{UVLO}$  with a hysteresis of 200 mV.

### 7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds  $T_{JSD}$ . When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

## 7.4 Device Functional Modes

### 7.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic HIGH. Accordingly, shutdown mode is forced if the EN pin is pulled LOW with a shutdown current of typically 0.7  $\mu$ A.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 260  $\Omega$  discharges the output through the VOS pin smoothly. The output discharge function also works when thermal shutdown, UVLO, or short-circuit protection are triggered.

An internal pulldown resistor of 400 k $\Omega$  is connected to the EN pin when the EN pin is LOW. The pulldown resistor is disconnected when the EN pin is HIGH.

### 7.4.2 Power Good

The TLV62085 has a power good output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. 表 1 shows the PG pin logic.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	✓	
	EN = High, $V_{FB} \leq V_{PG}$		✓
Shutdown	EN = Low		✓
Thermal Shutdown	$T_J > T_{JSD}$		✓
UVLO	$0.5 \text{ V} < V_{IN} < V_{UVLO}$		✓
Power Supply Removal	$V_{IN} \leq 0.5 \text{ V}$	✓	

## 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TLV62085 is a synchronous step-down converter in which output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using the typical applications as a reference.

### 8.2 Typical Application

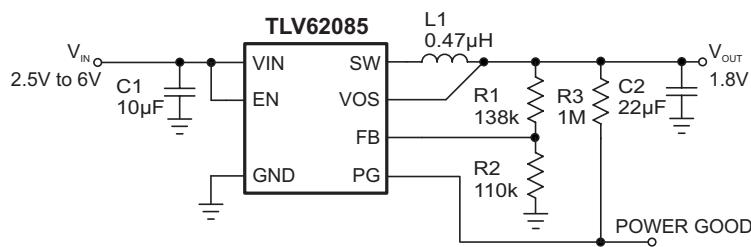


图 4. 1.8-V Output Voltage Application

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 6 V
Output voltage	1.8 V
Output current	≤ 3 A
Output ripple voltage	<30 mV

表 3 lists the components used for the example.

表 3. List of Components<sup>(1)</sup>

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic capacitor, 10 V, X7R, size 0805, GRM21BR71A106ME51L	Murata
C2	22 µF, Ceramic capacitor, 6.3 V, X5R, size 0805, GRM21BR60J226ME39L	Murata
L1	0.47 µH, Power Inductor, size 4 mm × 4 mm × 1.5 mm, XFL4015-471ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0603;	Std
R2	110 kΩ, Chip resistor, 1/16 W, 1%, size 0603;	Std
R3	1 MΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See [Third-Party Products](#) disclaimer.

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Custom Design with WEBENCH® Tools

[Click here](#) to create a custom design using the TLV62085 device with the WEBENCH® Power Designer.

1. Start by entering your  $V_{IN}$ ,  $V_{OUT}$ , and  $I_{OUT}$  requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance
  - Run thermal simulations to understand the thermal performance of your board
  - Export your customized schematic and layout into popular CAD formats
  - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to [公式 3](#):

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8 \text{ V} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

$R2$  must not be higher than  $180 \text{ k}\Omega$  to achieve high efficiency at light load while providing acceptable noise sensitivity.

### 8.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, [表 4](#) outlines possible inductor and capacitor value combinations for most applications.

表 4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [ $\mu\text{H}$ ] <sup>(1)</sup>	NOMINAL C <sub>OUT</sub> [ $\mu\text{F}$ ] <sup>(2)</sup>				
	10	22	47	100	150
0.47		+ <sup>(3)</sup>	+	+	+
1	+	+	+	+	+
2.2					

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and -30%.

(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and -50%.

(3) Typical application configuration. Other '+' mark indicates recommended filter combinations.

### 8.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, [公式 4](#) is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$  = Maximum output current
- $\Delta I_L$  = Inductor current ripple

- $f_{sw}$  = Switching frequency
  - L = Inductor value
- (4)

TI recommends choosing the saturation current for the inductor 20% to 30% higher than the  $I_{L,MAX}$ , out of [公式 4](#). A higher inductor value is also useful to lower ripple current but increases the transient response time as well. The following inductors are recommended to be used in designs.

**表 5. List of Recommended Inductors<sup>(1)</sup>**

INDUCTANCE [ $\mu$ H]	CURRENT RATING [A]	DIMENSIONS L × W × H [mm <sup>3</sup> ]	DC RESISTANCE [mΩ typical]	PART NUMBER
0.47	6.6	4 × 4 × 1.5	7.6	Coilcraft XFL4015-471
0.47	4.7	3.2 × 2.5 × 1.2	21	TOKO DFE322512-R47N
1	5.1	4 × 4 × 2	10.8	Coilcraft XFL4020-102

(1) See [Third-Party Products](#) disclaimer.

### 8.2.2.5 Capacitor Selection

The input capacitor is the low-impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 10  $\mu$ F is sufficient, though a larger value reduces input current ripple.

The architecture of the TLV62085 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended typical output capacitor value is 22  $\mu$ F; this capacitance can vary over a wide range as outline in the output filter selection table. Output capacitors above 150uF may be used with a reduced load current during startup to avoid triggering the short circuit protection.

A feed-forward capacitor is not required for device proper operation.

### 8.2.3 Application Curves

$V_{IN} = 3.6 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted

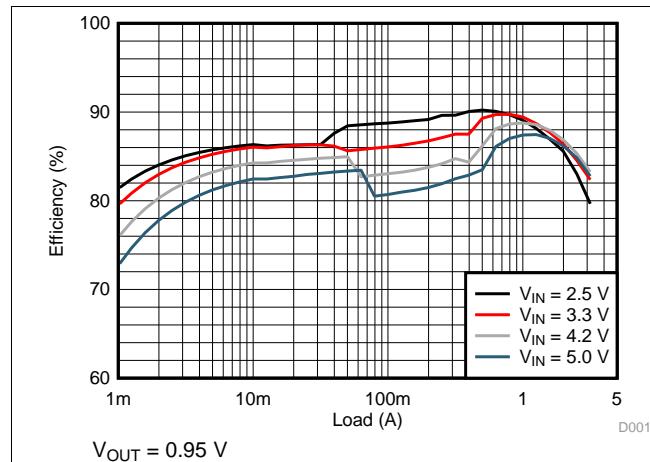


图 5. Efficiency

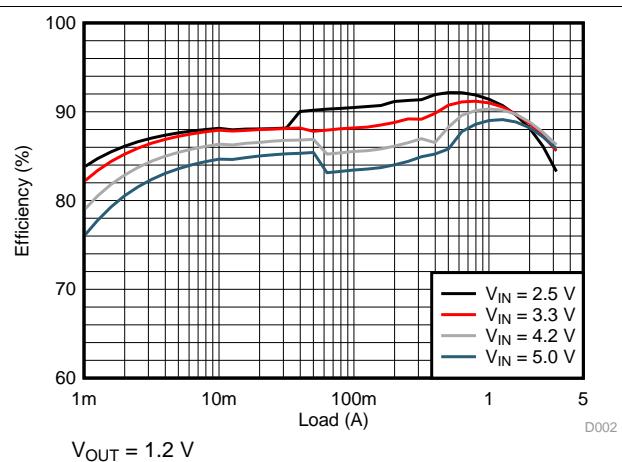


图 6. Efficiency

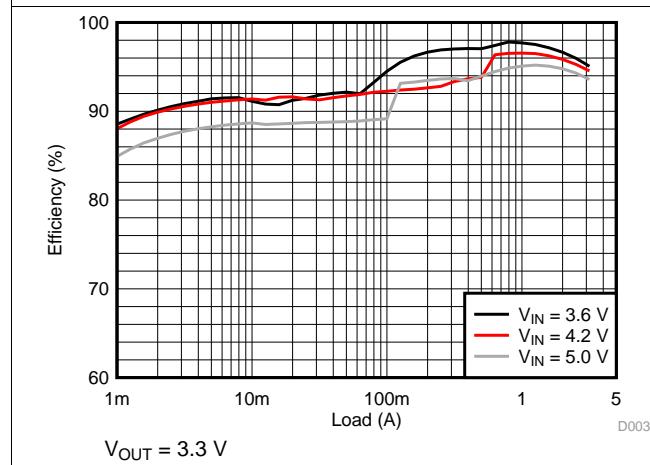


图 7. Efficiency

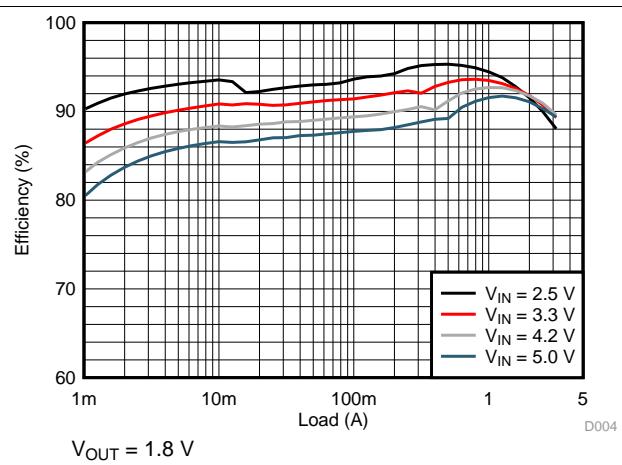


图 8. Efficiency

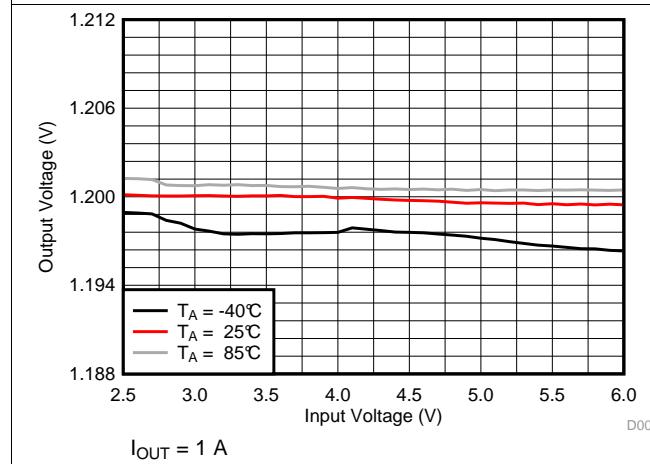


图 9. Line Regulation

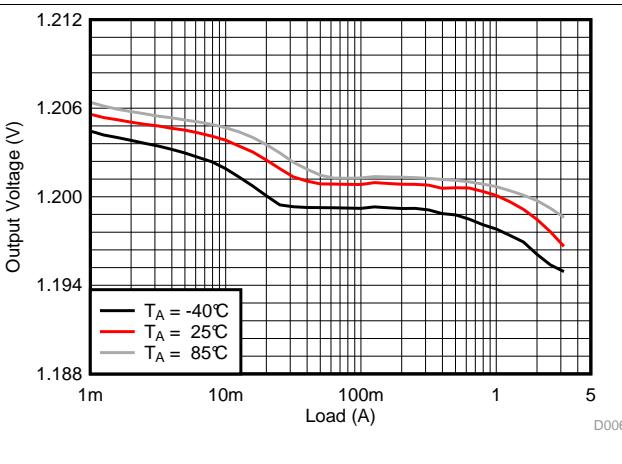
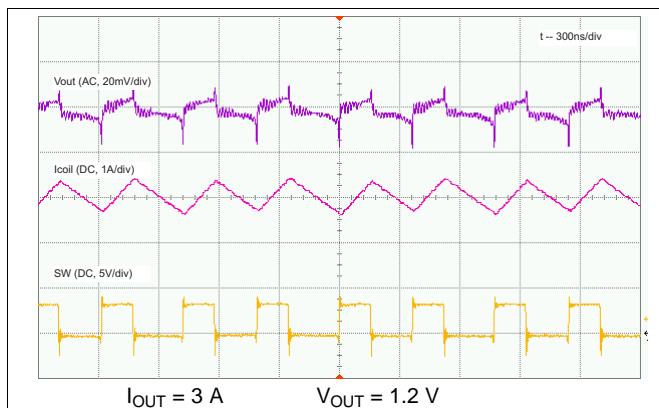
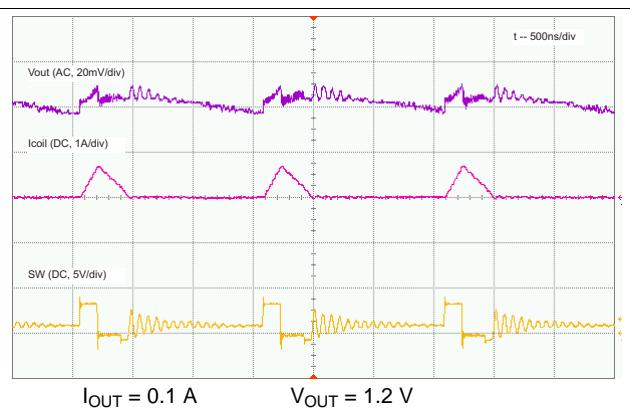
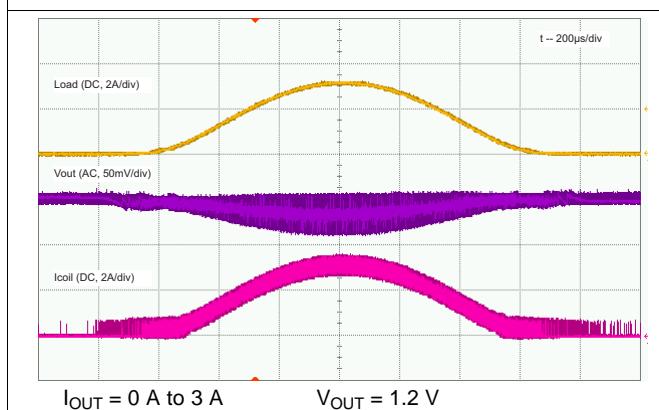
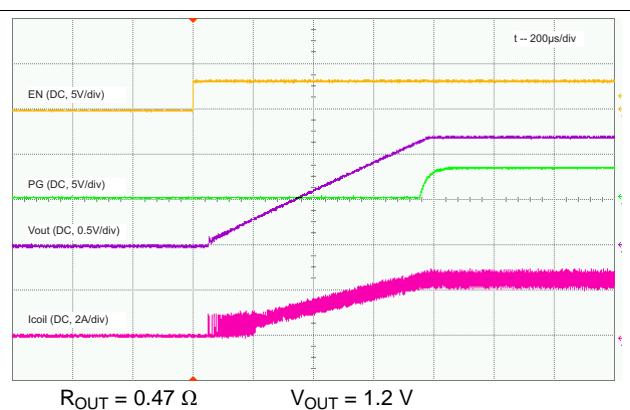
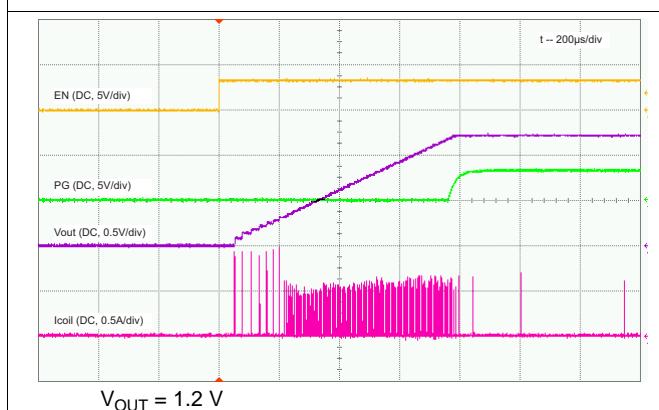
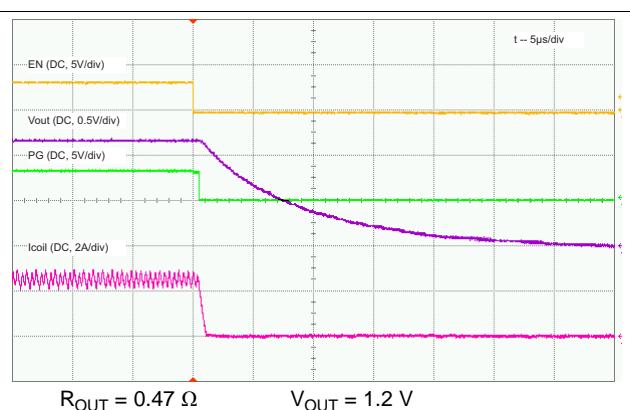
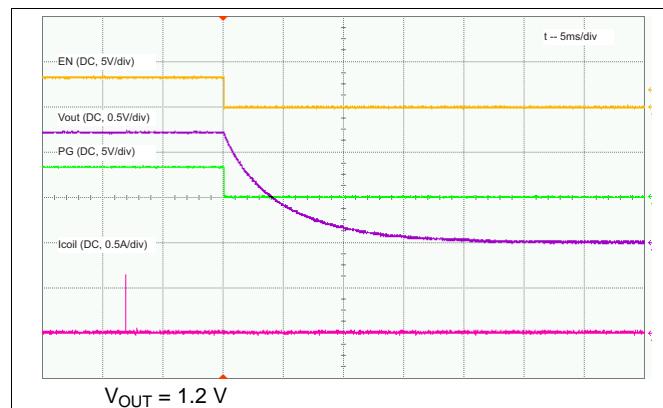
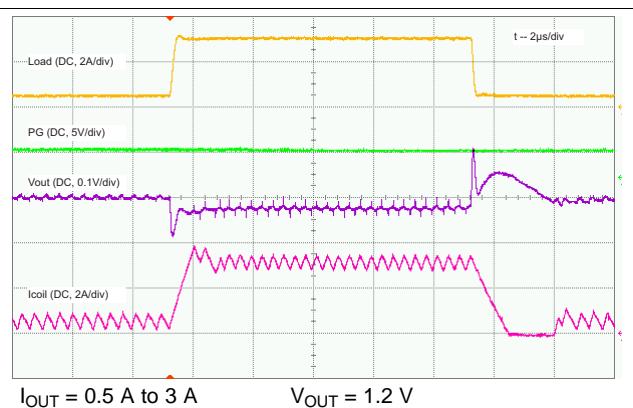
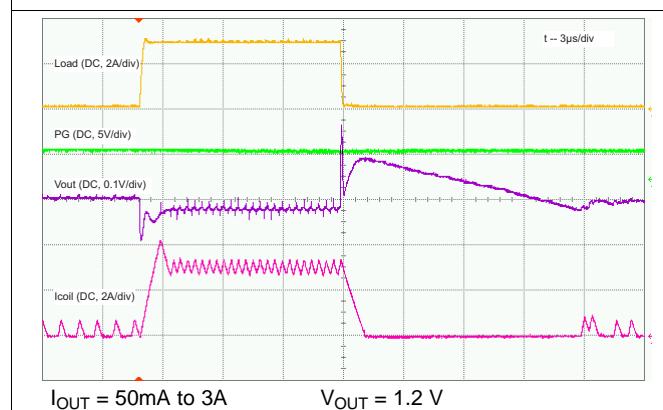
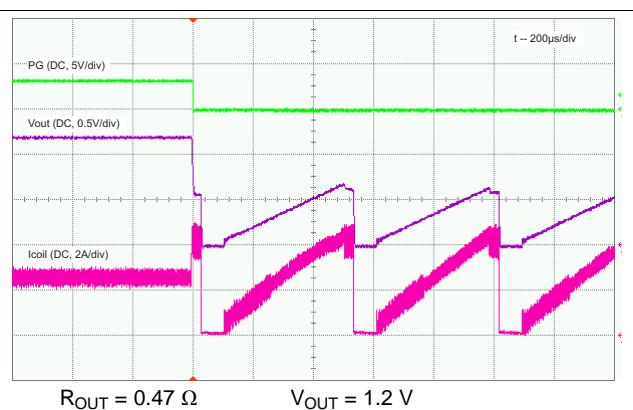
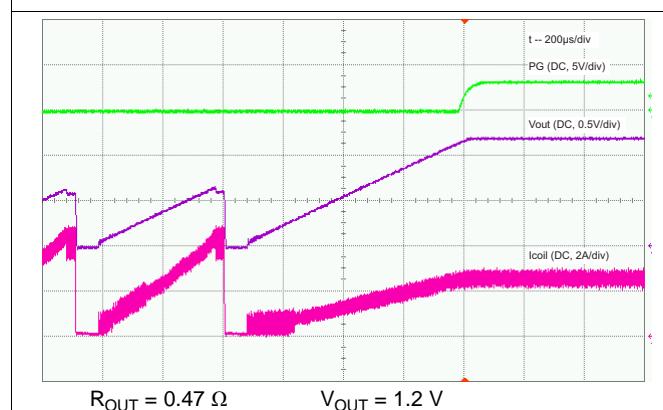
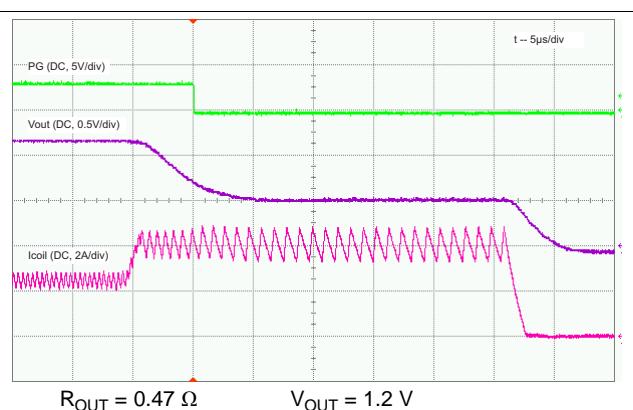


图 10. Load Regulation


**图 11. PWM Operation**

**图 12. PFM Operation**

**图 13. Load Sweep**

**图 14. Start-Up with Load**

**图 15. Start-Up without Load**

**图 16. Shutdown with Load**


**图 17. Shutdown without Load**

**图 18. Load Transient**

**图 19. Load Transient**

**图 20. Output Short-Circuit Protection, Entry**

**图 21. Output Short-Circuit Protection, Recovery**

**图 22. Output Short-Circuit Protection, HICCUP Zoom In**

## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 6 V. Ensure that the input power supply has a sufficient current rating for the application.

## 10 Layout

### 10.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TLV62085 device.

The input and output capacitors and the inductor must be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. The low side of the input and output capacitors must be connected directly to the GND pin to avoid a ground potential shift. The sense traces connected to FB and VOS pins are signal traces. Special care must be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes. See [图 23](#) for the recommended PCB layout.

### 10.2 Layout Example

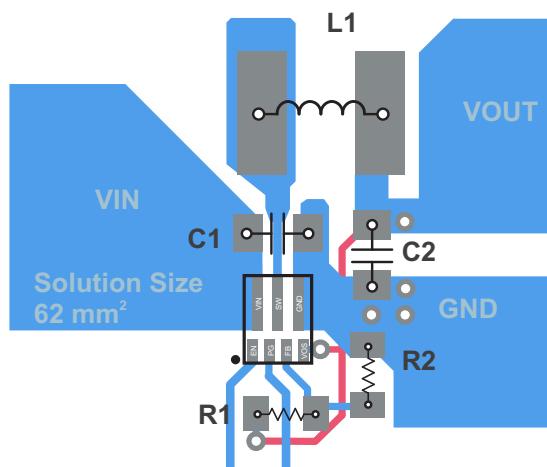


图 23. PCB Layout Recommendation

### 10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the *Thermal Characteristics Application Notes*, [SZZA017](#) and [SPRA953](#).

## 11 器件和文档支持

### 11.1 开发支持

#### 11.1.1 使用 WEBENCH® 工具定制设计方案

请单击此处，借助 WEBENCH® 电源设计器并使用 TPS54360 器件创建定制设计方案。

1. 首先输入您的  $V_{IN}$ 、 $V_{OUT}$  和  $I_{OUT}$  要求。
2. 使用优化器拨盘可优化效率、封装和成本等关键设计参数并将您的设计与德州仪器 (TI) 的其他可行解决方案进行比较。
3. WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。
4. 在多数情况下，您还可以：
  - 运行电气仿真，观察重要波形以及电路性能
  - 运行热性能仿真，了解电路板热性能
  - 将定制原理图和布局方案导出至常用 CAD 格式
  - 打印设计方案的 PDF 报告并与同事共享
5. 有关 WEBENCH 工具的详细信息，请访问 [www.ti.com.cn/WEBENCH](http://www.ti.com.cn/WEBENCH)。

#### 11.1.2 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

### 11.2 文档支持

#### 11.2.1 相关文档

请参阅如下相关文档：

- 《热工特性应用手册》，[SZZA017](#)
- 《热工特性应用手册》，[SPRA953](#)

### 11.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

[TI E2E™ 在线社区](#) **TI 的工程师对工程师 (E2E) 社区**。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

[设计支持](#) **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.5 商标

DCS-Control, WEBENCH, E2E are trademarks of Texas Instruments.  
WEBENCH is a registered trademark of Texas Instruments.

### 11.6 静电放电警告

 这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.7 术语表

[SLYZ022 — TI 术语表](#)。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62085RLTR	ACTIVE	VSON-HR	RLT	7	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Q5	<span style="background-color: red; color: white;">Samples</span>
TLV62085RLTT	ACTIVE	VSON-HR	RLT	7	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Q5	<span style="background-color: red; color: white;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



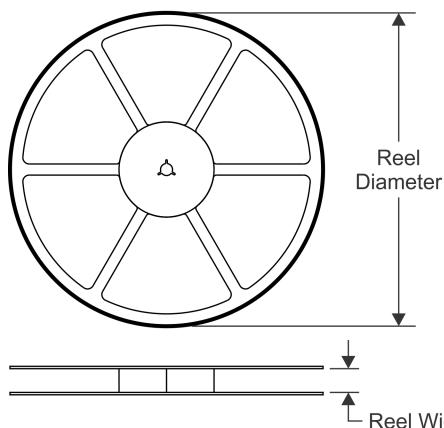
www.ti.com

## PACKAGE OPTION ADDENDUM

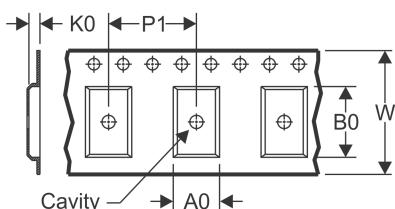
16-Jul-2018

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

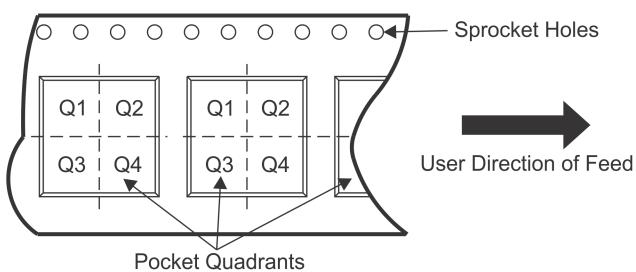


### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

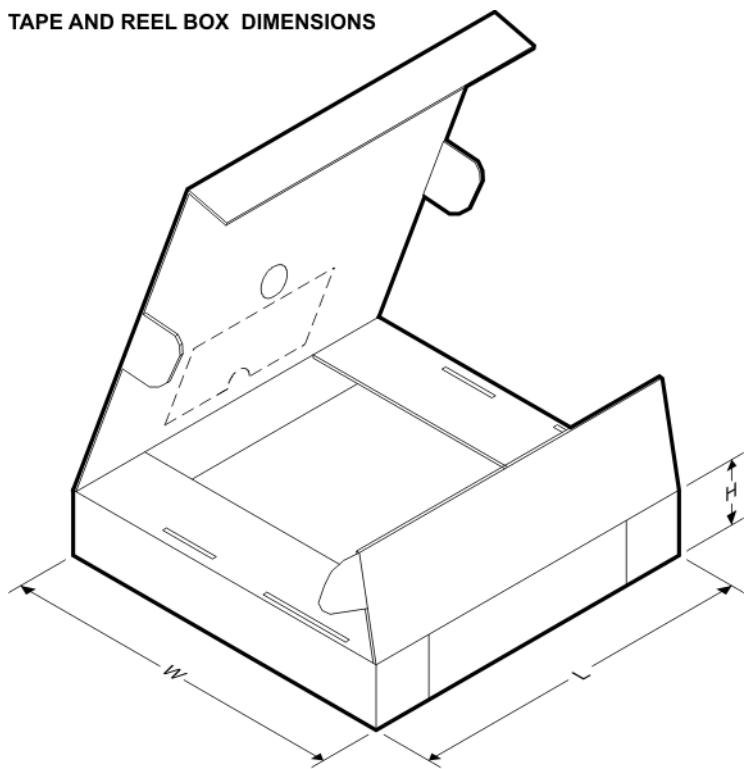
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62085RLTR	VSON-HR	RLT	7	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV62085RLTT	VSON-HR	RLT	7	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



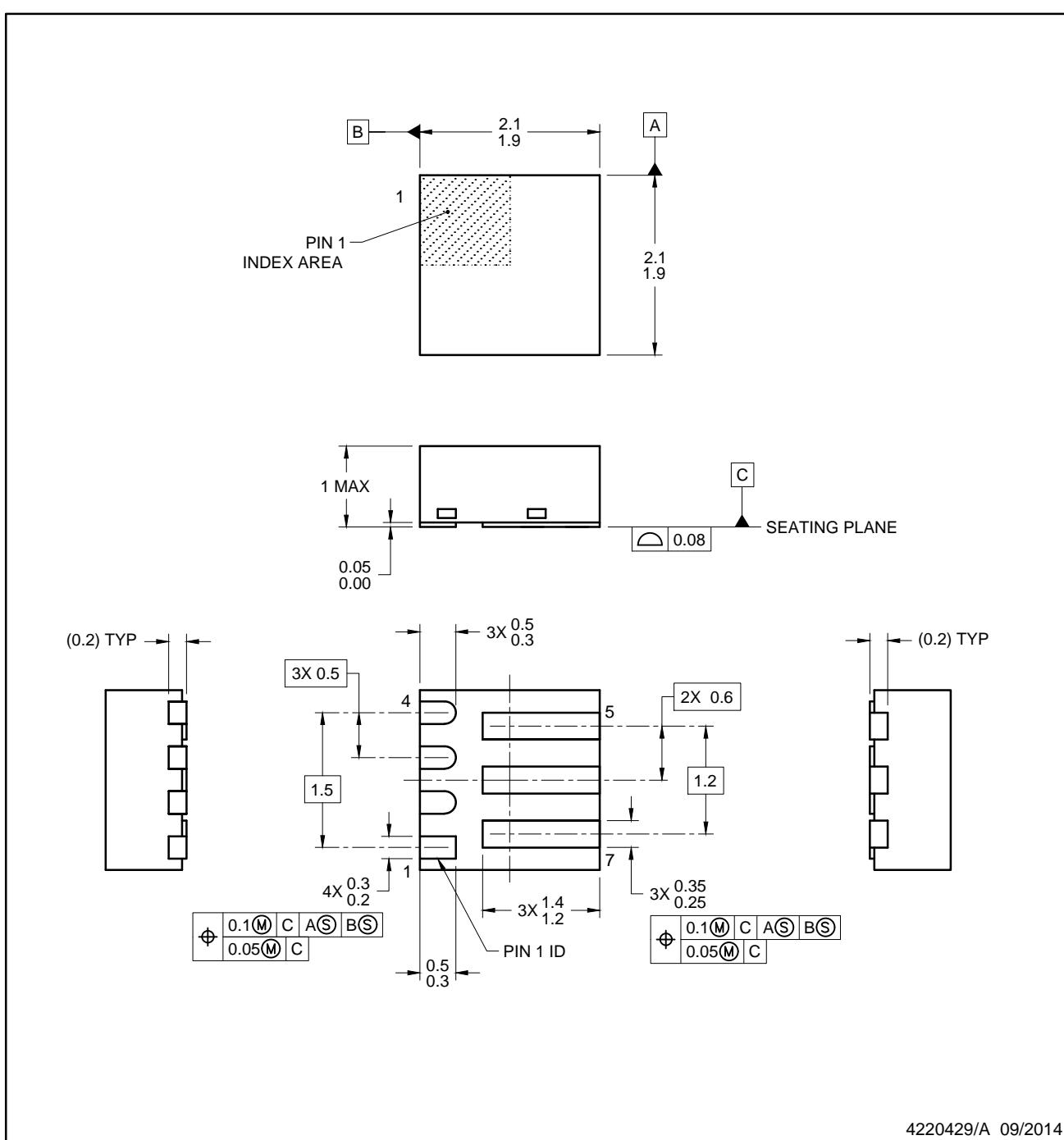
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62085RLTR	VSON-HR	RLT	7	3000	210.0	185.0	35.0
TLV62085RLTT	VSON-HR	RLT	7	250	210.0	185.0	35.0

# PACKAGE OUTLINE

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



### NOTES:

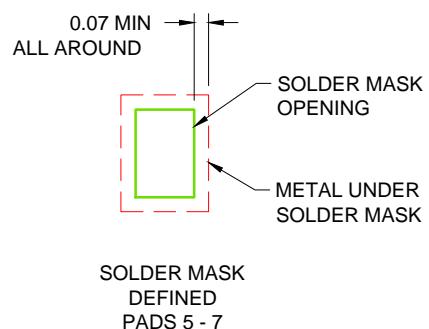
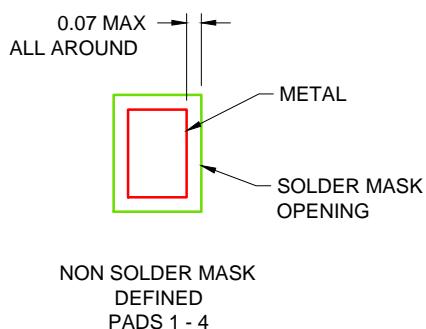
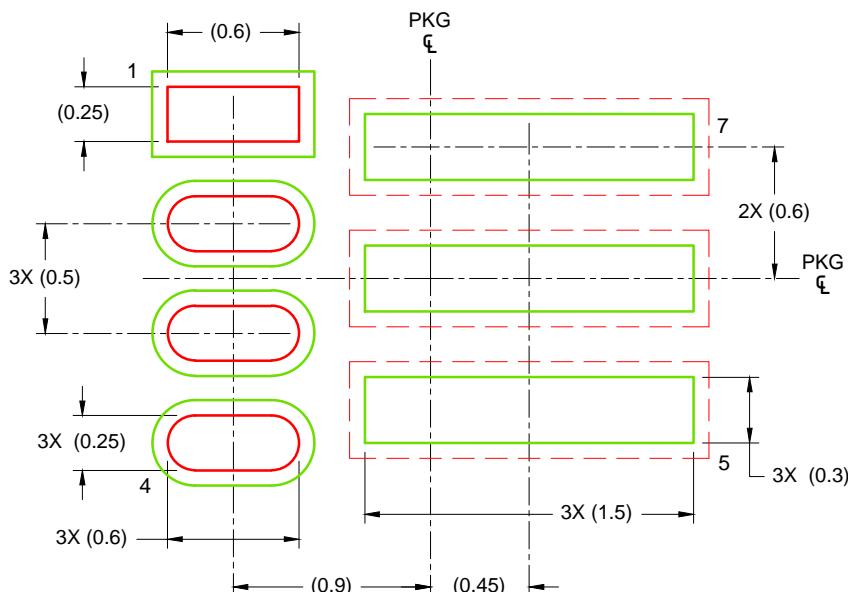
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**RLT0007A**

# EXAMPLE BOARD LAYOUT

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER MASK DETAILS

4220429/A 09/2014

NOTES: (continued)

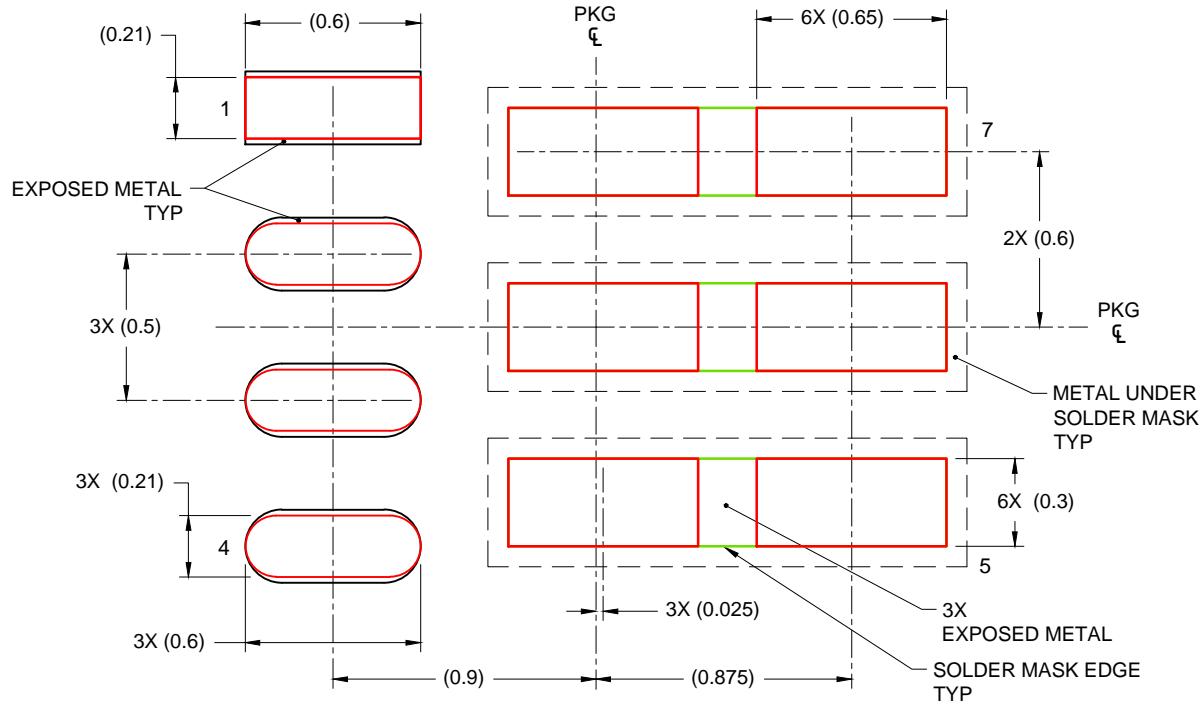
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias should not be placed on soldering pads unless they are plugged or plated shut.

**RLT0007A**

# EXAMPLE STENCIL DESIGN

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

FOR ALL EXPOSED PADS  
85% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 40X

4220429/A 09/2014

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够（1）预见故障的危险后果，（2）监视故障及其后果，以及（3）降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用所用 TI 产品的功能而设计。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会配有任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准而设计。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确规定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2018 德州仪器半导体技术（上海）有限公司