Intel® Pentium® III Processor for the SC242 at 450 MHz to 1.0 GHz

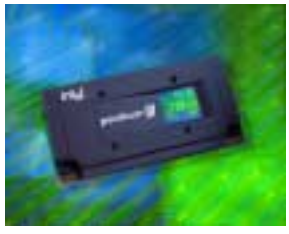
Datasheet

Product Features

- Available in 1.0B GHz, 933, 866, 800EB, 733, 667, 600B, 600EB, 533B, and 533EB MHz speeds support a 133 MHz system bus ('B' denotes support for a 133 MHz system bus where a processor is available at the same specific core frequency in seperate 100 MHz and 133 MHz Front Side Bus versions; 'E' denotes support for Advanced Transfer Cache and Advanced System Buffering)
- Available in 1.0 GHz, 850, 800, 750, 700, 650, 600E, 600, 550E, 550, 500, and 450 MHz speeds support a 100 MHz system bus ('E' denotes support for Advanced Transfer Cache and Advanced System Buffering)
- Available in versions that incorporate 256-KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache with Error Correcting Code (ECC)) or versions that incorporate a discrete, half-speed, 512-KB in-package L2 cache with ECC
- Dual Independent Bus (DIB) architecture increases bandwidth and performance over single-bus processors
- Internet Streaming SIMD Extensions for enhanced video, sound and 3D performance
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Dynamic execution micro architecture
- Power Management capabilities
  —System Management mode
  —Multiple low-power states
- Intel Processor Serial Number
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Single Edge Contact Cartridge (S.E.C.C.) and S.E.C.C.2 packaging technology; the S.E.C. cartridges deliver high performance with improved handling protection and socketability
- Integrated high performance 16 KB instruction and 16-KB data, nonblocking, level one cache
- Enables systems which are scaleable up to two processors
- Error-correcting code for System Bus data

The Intel® Pentium® III processor is designed for high-performance desktops and for workstations and servers. It is binary compatible with previous Intel Architecture processors. The Pentium III processor provides great performance for applications running on advanced operating systems such as Microsoft Windows* 98, Windows NT* and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution, Dual Independent Bus architecture plus Intel® MMX™ technology and Internet Streaming SIMD Extensions—bringing a new level of performance for systems buyers. ThePentium III processor is scaleable to two processors in a multiprocessor system and extends the power of the Intel® Pentium® II processor with performance headroom for business media, communication and internet capabilities. Systems based on Pentium III processors also include the latest features to simplify system management and lower the cost of ownership for large and small business environments. The Pentium III processor offers great performance for today's and tomorrow's applications.

SC242 / SECC2 Package



Document Number: 244452-009
July 2002

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Revision History

Revision	Description	Date
-009	• Removed 1.13 GHz processor frequency. Minor edits for clarity.	July 2002

1.0 Introduction

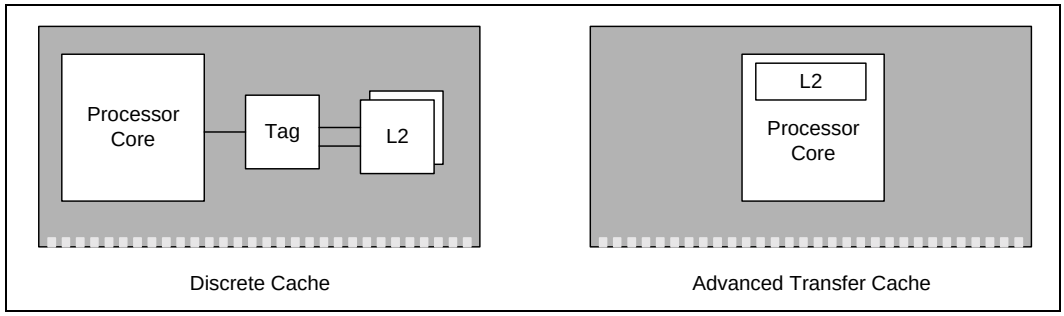
The Intel® Pentium® III processor is the next member of the P6 family, in the Intel® IA-32 processor line. Like the Intel® Pentium® II processor, the Pentium III processor implements the Dynamic Execution microarchitecture - a unique combination of multiple branch prediction, data flow analysis, and speculative execution. This enables these processors to deliver higher performance than the Pentium processor, while maintaining binary compatibility with all previous Intel Architecture processors. The Pentium III processor also executes Intel® MMX™ technology instructions for enhanced media and communication performance just as it's predecessor, the Pentium II processor. The Pentium III processor executes Internet Streaming SIMD Extensions for enhanced floating point and 3-D application performance. In addition, the Pentium III processor extends the concept of processor identification with the addition of a processor serial number. Refer to the *Intel® Processor Serial Number* application note (Document Number 245125) for more detailed information. The Pentium III processor utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Pentium III processor utilizes the same multiprocessing system bus technology as the Pentium II processor. This allows for a higher level of performance for both uni-processor and two-way multiprocessor (2-way MP) systems. See the *Intel® Pentium® III Processor Specification Update* (Document Number 244453) for guidelines on which processors can be mixed in an MP system. Memory is cacheable for 4 GB of addressable memory space, allowing significant headroom for desktop systems.

The Pentium III processor is available with two different second level (L2) cache implementations. The "Discrete" cache version (CPUID=067xh) uses commercially available parts for the L2 cache. The L2 cache is composed of an external (to processor silicon) TagRAM and burst pipelined synchronous static RAM (BSRAM), as seen in Figure 1. The "Advanced Transfer Cache" (CPUID=068xh) does not use commercially available L2 cache parts. Its L2 cache resides entirely within the processor silicon, as seen in Figure 1. Refer to Table 1 to determine the L2 cache implementation for each Pentium III processor.

Pentium III processors are offered in either Single Edge Contact Cartridge (S.E.C.C.) or Single Edge Contact Cartridge 2 (S.E.C.C.2) package technologies. The S.E.C.C. package has the following features: an extended thermal plate, a cover, and a substrate with an edge finger connection. The extended thermal plate allows heatsink attachment or customized thermal solutions. The S.E.C.C.2 package has a cover and a substrate with an edge finger connection. This allows the thermal solutions to be placed directly onto the processor core package. The edge finger connection maintains socketability for system configuration. The edge finger connector is called the 'SC242 connector' in this and other documentation.

Figure 1. Second Level (L2) Cache Implementation



1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. the AGPset components), and other bus agents. The system bus is a multiprocessing interface to processors, memory, and I/O. The term "cache bus" refers to the interface between the processor and the L2 cache components (TagRAM and BSRAMs). The cache bus does NOT connect to the system bus, and is not visible to other agents on the system bus.

1.1.1 S.E.C.C.2 and S.E.C.C. Packaged Processor Terminology

The following terms are used often in this document and are explained here for clarification:

- **Pentium® III processor**—The entire product including internal components, substrate, cover and in S.E.C.C. packaged processors, an extended thermal plate.
- **S.E.C.C.**—The processor package technology called "Single Edge Contact Cartridge."
- **S.E.C.C.2**—The follow-on to S.E.C.C. processor package technology. This differs from its predecessor in that it has no extended thermal plate, thus reducing thermal resistance.
- **Processor substrate**—The FR4 board on which components are mounted inside the S.E.C.C. or S.E.C.C.2 packaged processor (with or without components attached).
- **Processor core**—The processor's execution engine.
- **Extended Thermal Plate**—This S.E.C.C. package feature is the surface used to attach a heatsink or other thermal solution to the processor.
- **Cover**—The plastic casing that covers the backside of the substrate.
- **Latch arms**—An S.E.C.C. package feature which can be used as a means for securing the processor in a retention mechanism.
- **OLGA** - Organic Land Grid Array. This package technology permits attaching the heatsink directly to the die.

Additional terms referred to in this and other related documentation:

- **SC242**—The 242-contact slot connector (previously referred to as Slot 1 connector) that the S.E.C.C. and S.E.C.C.2 plug into, just as the Pentium® Pro processor uses Socket 8.
- **Retention mechanism**—A mechanical piece which holds the S.E.C.C. or S.E.C.C.2 packaged processor in the SC242 connector.
- **Heatsink support**—The support pieces that are mounted on the baseboard to provide added support for heatsinks.
- **Keep-out zone**—The area on or near an S.E.C.C. or S.E.C.C.2 packaged processor substrate that systems designs can not utilize.
- **Keep-in zone**—The area of the center of an S.E.C.C. or S.E.C.C.2 packaged processor substrate that thermal solutions may utilize.

The L2 cache, TagRAM and BSRAM die, are industry designated names.

1.1.2 Processor Naming Convention

A letter(s) is added to certain processors (e.g., 600B MHz) when the core frequency alone may not uniquely identify the processor. Below is a summary what the letter means as well as a table listing all Pentium III processors currently available.

- "B" — 133 MHz System Bus Frequency
- "E" — Processor with "Advanced Transfer Cache" (CPUID=068xh)

Table 1. Processor Identification

Processor	Core Frequency (MHz)	System Bus Frequency (MHz)	L2 Cache Size (Kbytes)	L2 Cache Type	CPUID[1]
450	450	100	512	Discrete	067xh
500	500	100	512	Discrete	067xh
533B	533	133	512	Discrete	067xh
533EB	533	133	256	ATC[2]	068xh
550	550	100	512	Discrete	067xh
550E	550	100	256	ATC[2]	068xh
600	600	100	512	Discrete	067xh
600B	600	133	512	Discrete	067xh
600E	600	100	256	ATC[2]	068xh
600EB	600	133	256	ATC[2]	068xh
650	650	100	256	ATC[2]	068xh
667	667	133	256	ATC[2]	068xh
700	700	100	256	ATC[2]	068xh
733	733	133	256	ATC[2]	068xh
750	750	100	256	ATC[2]	068xh
800	800	100	256	ATC[2]	068xh
800EB	800	133	256	ATC[2]	068xh
850	850	100	256	ATC[2]	068xh
866	866	133	256	ATC[2]	068xh
933	933	133	256	ATC[2]	068xh
1.0 GHz	1000	100	256	ATC[2]	068xh
1.0B GHz	1000	133	256	ATC[2]	068xh

NOTES:
1. Refer to the *Intel® Pentium® III Processor Specification Update* for the exact CPUID for each processor.
2. ATC = Advanced Transfer Cache. ATC is an L2 Cache integrated on the same die as the processor core. With ATC, the interface between the processor core and L2 Cache is 256-bits wide, runs at the same frequency as the processor core and has enhanced buffering.

1.2 Related Documents

The reader of this specification should also be familiar with material and concepts in the documents listed in Table 2. These documents, and a complete list of Pentium III processor reference material, can be found on the Intel Developers' Insight web site located at http://developer.intel.com.

Table 2. Related Documents

Document	Intel Document Number
AP-485, *Intel® Processor Identification and the CPUID Instruction*	241618
AP-585, *Intel®Pentium® II Processor GTL+ Guidelines*	243330
AP-588, *Mechanical and Assembly Technology for S.E.C. Cartridge Processors*	243333
AP-589, *Design for EMI*	243334
AP-826, *Mechanical Assembly and Customer Manufacturing Technology for S.E.P. Packages*	243748
AP-902, *S.E.C.C.2 Heatsink Installation and Removal*	244454
AP-903, *Mechanical Assembly and Customer Manufacturing Technology for Processor in S.E.C.C.2 Packages*	244457
AP-905, *Intel® Pentium® III Processor Thermal Design Guidelines*	245087
AP-906, *100 MHz AGTL+ Layout Guidelines for the Intel® Pentium® III Processor and Intel® 440BX AGPset*	245086
AP-907, *Intel® Pentium® III Processor Power Distribution Guidelines*	245085
Intel® Processor Serial Number	245119
CK97 Clock Synthesizer Design Guidelines	243867
Intel® Architecture Software Developer's Manual	243193
Volume I: Basic Architecture	243190
Volume II: Instruction Set Reference	243191
Volume III: System Programming Guide	243192
P6 Family of Processors Hardware Developer's Manual	244001
Intel® Pentium® II Processor at 350, 400 and 450 MHz datasheet	243657
Intel® Pentium® II Processor Developer's Manual	243502
Pentium® III Processor I/O Buffer Models	Note 1
Intel® Pentium® III Processor Specification Update	244453
SC242 Bus Termination Card Design Guidelines	243409
Slot 1 Connector Specification	243397
VRM 8.4 DC-DC Converter Design Guidelines	245335

NOTES:
1. These models are available in Viewlogic* XTK* model format (formerly known as QUAD format) at the Intel Developer's Website at http://developer.intel.com.

2.0 Electrical Specifications

2.1 Processor System Bus and V_{REF}

Most Pentium III processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

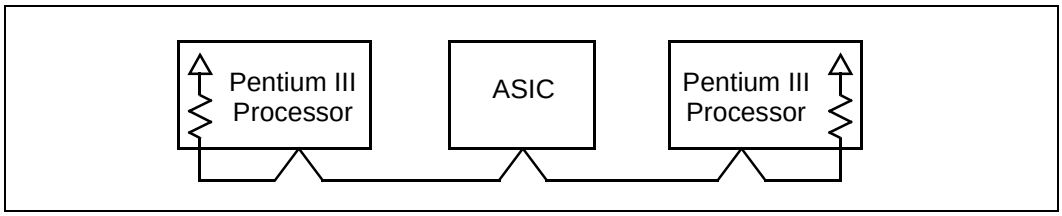
The Pentium Pro processor system bus specification is similar to the GTL specification, but was enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. This specification is different from the GTL specification, and is referred to as GTL+. For more information on GTL+ specifications, see the GTL+ buffer specification in the *Intel® Pentium® II Processor Developer's Manual* (Document Number 243502).

The Pentium III processor varies from the Pentium Pro processor in its output buffer implementation. The buffers that drive the system bus signals on the Pentium III processor are actively driven to VTT for one clock cycle after the low to high transition to improve rise times. These signals should still be considered open-drain and require termination to a supply that provides the high signal level. Because this specification is different from the GTL+ specification, it is referred to as AGTL+ in this and other documentation. AGTL+ logic and GTL+ logic are compatible with each other and may both be used on the same system bus. For more information on AGTL+ routing, see AP-906, *100 MHz AGTL+ Layout Guidelines for the Pentium III® Processor and Intel® 440BX AGPset* (Document Number 245086) or the appropriate platform design guide.

AGTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1, and is generated on the S.E.C.C. and S.E.C.C.2 packages for the processor core. Local V_{REF} copies should be generated on the baseboard for all other devices on the AGTL+ system bus. Termination (usually a resistor at each end of the signal trace) is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor contains termination resistors that provide termination for one end of the Pentium III processor system bus. These specifications assume another resistor at the end of each signal trace to ensure adequate signal quality for the AGTL+ signals; see Table 11 for the bus termination voltage specifications for AGTL+. Refer to the *Intel® Pentium® II Processor Developer's Manual* (Document Number 243502) for the GTL+ bus specification. Solutions exist for single-ended termination as well, though this implementation changes system design. Figure 2 is a schematic representation of AGTL+ bus topology with Pentium III processors.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the Pentium III processor system bus including trace lengths is highly recommended when designing a system with a heavily loaded AGTL+ bus, especially for systems using a single set of termination resistors (i.e., those on the processor substrate). Such designs will not match the solution space allowed for by installation of termination resistors on the baseboard. See Intel's Developer's Website (http://developer.intel.com) to download the *Intel® Pentium® III Processor I/O Buffer Models, Viewlogic* XTK* model format* (formerly known as QUAD format).

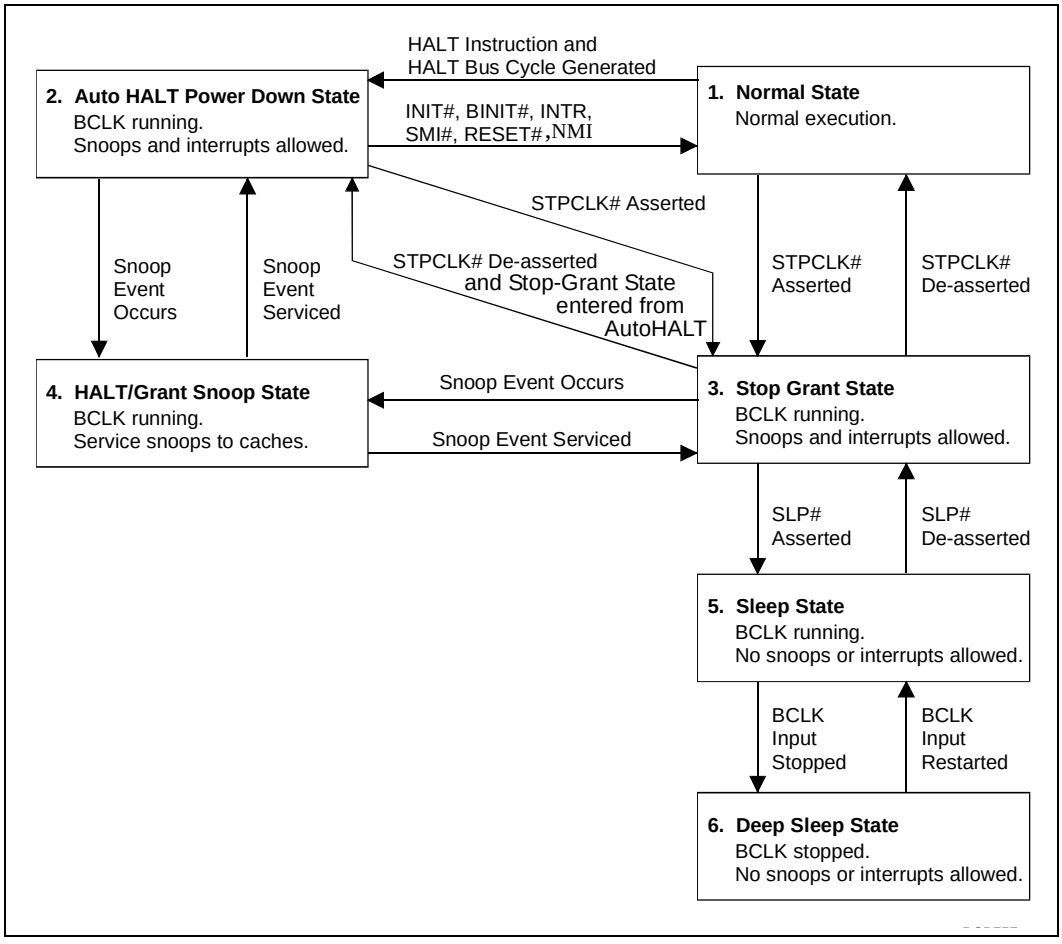
Figure 2. AGTL+ Bus Topology



2.2 Clock Control and Low Power States

Pentium III processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 3 for a visual representation of the Pentium III processor low power states.

Figure 3. Stop Clock State Machine



For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02Ah (Hex), bit 26 must be set to a '1' (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide* (Document Number 243192).

Due to the inability of processors to recognize bus transactions during the Sleep and Deep Sleep states, 2-way MP systems are not allowed to have one processor in Sleep/Deep Sleep state and the other processor in Normal or Stop-Grant state simultaneously.

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* (Document Number 243192) for more information.

FLUSH# will be serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# and FLUSH# will not be serviced during Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.5) will occur with the assertion of the SLP# signal.

While in Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized and serviced upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the Pentium III processor system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the Pentium III processor system bus has been serviced (whether by the processor or another agent on the Pentium III processor system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from the Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input (see Section 2.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BCLK is stopped. It is recommended that the BCLK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BCLK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

The processor provides the clock signal to the L2 cache. During AutoHALT Power Down and Stop-Grant states, the processor will process a system bus snoop. The processor will not stop the clock to the L2 cache during AutoHALT Power Down or Stop-Grant states. Entrance into the Halt/Grant Snoop state will allow the L2 cache to be snooped, similar to the Normal state.

When the processor is in Sleep and Deep Sleep states, it will not respond to interrupts or snoop transactions. During the Sleep state, the clock to the L2 cache is not stopped. During the Deep Sleep state, the clock to the L2 cache is stopped. The clock to the L2 cache will be restarted only after the internal clocking mechanism for the processor is stable (i.e., the processor has re-entered Sleep state).

PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Power and Ground Pins

For clean on-chip power distribution, Pentium III processors have 27 V_{CC} (power) and 30 V_{SS} (ground) inputs. The 27 V_{CC} pins are further divided to provide the different voltage levels to the components. $V_{CC_{CORE}}$ inputs for the processor core and some L2 cache components account for 19 of the V_{CC} pins, while 4 V_{TT} inputs (1.5 V) are used to provide an AGTL+ termination voltage to the processor and 3 $V_{CC_{L2}}/V_{CC_{3.3}}$ inputs (3.3 V) are either used for the off-chip L2 cache TagRAM and BSRAMs (CPUID=067xh) or for the voltage clamp logic (CPUID=068xh). One V_{CC_5} pin is provided for use by test equipment and tools. V_{CC_5}, $V_{CC_{L2}}/V_{CC_{3.3}}$, and $V_{CC_{CORE}}$ must remain electrically separated from each other. On the circuit board, all $V_{CC_{CORE}}$ pins must be connected to a voltage island and all $V_{CC_{L2}}/V_{CC_{3.3}}$ pins must be connected to a separate voltage island (an island is a portion of a power plane that has been divided, or an entire plane). Similarly, all V_{SS} pins must be connected to a system ground plane.

Note: The voltage clamp logic acts as a voltage translator between the processor's 1.5 V tolerant CMOS signals and the 2.5 V CMOS voltage on the motherboard. This logic is only available with Pentium III processors with CPUID=068xh.

2.4 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 8. Failure to do so can result in timing violations or a reduced lifetime of the processor.

2.4.1 Processor VCC_{CORE} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep an interconnect resistance from the regulator (or VRM pins) to the SC242 connector of less than 0.3 mΩ. This can be accomplished by keeping a maximum distance of 1.0 inches between the regulator output and SC242 connector. The recommended VCC_{CORE} interconnect is a 2.0 inch wide by 1.0 inch long (maximum distance between the SC242 connector and the VRM connector) plane segment with a 1-ounce plating. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, is provided on the voltage regulation module (VRM). If using Intel's enabled VRM solutions see developer.intel.com for the specification and a list of qualified vendors. The VCC_{CORE} input should be capable of delivering a recommended minimum $dICC_{CORE}/dt$ (defined in Table 8) while maintaining the required tolerances (also defined in Table 8).

2.4.2 Processor System Bus AGTL+ Decoupling

The Pentium III processor contains high frequency decoupling capacitance on the processor substrate; bulk decoupling must be provided for by the system baseboard for proper AGTL+ bus operation. See AP-906, *100 MHz AGTL+ Layout Guidelines for the Intel® Pentium® III Processor and Intel® 440BX AGPset* (Document Number 245086) or the appropriate platform design guide, AP-907, *Pentium® III Processor Power Distribution Guidelines* (Document Number 245085), and the GTL+ buffer specification in the *Pentium® II Processor Developer's Manual* (Document Number 243502) for more information.

2.5 Processor System Bus Clock and Processor Clocking

The BCLK input directly controls the operating speed of the Pentium III processor system bus interface. All Pentium III processor system bus timing parameters are specified with respect to the rising edge of the BCLK input. See the *P6 Family of Processors Hardware Developer's Manual* (Document Number 244001) for further details.

2.6 Voltage Identification

There are five voltage identification pins on the SC242 connector. These pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor core. The VID pins are needed to cleanly support voltage specification variations on current and future Pentium III processors. VID[4:0] are defined in Table 3. A '1' in this table refers to an open pin and a '0' refers to a short to ground. The power supply must supply the voltage that is requested or disable itself.

To ensure a system is ready for current and future Pentium III processors, the range of values in **bold** in Table 3 should be supported. A smaller range will risk the ability of the system to migrate to a higher performance Pentium III processor and/or maintain compatibility with current Pentium III processors.

Table 3. Voltage Identification Definition

Processor Pins						Notes[1,2]
VID4	VID3	VID2	VID1	VID0	Vcc_{CORE}	
0	1	1	1	1	1.30	
0	1	1	1	0	1.35	
0	1	1	0	1	1.40	
0	1	1	0	0	1.45	
0	1	0	1	1	1.50	
0	1	0	1	0	1.55	
0	1	0	0	1	**1.60**	3
0	1	0	0	0	**1.65**	3
0	0	1	1	1	**1.70**	3
0	0	1	1	0	**1.75**	3
0	0	1	0	1	**1.80**	3
0	0	1	0	0	**1.85**	3
0	0	0	1	1	**1.90**	3
0	0	0	1	0	**1.95**	3
0	0	0	0	1	**2.00**	3
0	0	0	0	0	**2.05**	3
1	1	1	1	1	No Core	
1	1	1	1	0	2.1	
1	1	1	0	1	2.2	
1	1	1	0	0	2.3	
1	1	0	1	1	2.4	
1	1	0	1	0	2.5	
1	1	0	0	1	2.6	
1	1	0	0	0	2.7	
1	0	1	1	1	2.8	
1	0	1	1	0	2.9	
1	0	1	0	1	3.0	
1	0	1	0	0	3.1	
1	0	0	1	1	3.2	
1	0	0	1	0	3.3	
1	0	0	0	1	3.4	
1	0	0	0	0	3.5	

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on baseboard.
3. To ensure a system is ready for the Pentium III processor, the values in **BOLD** in Table 3 should be supported.

Note that the ‘11111’ (all opens) ID can be used to detect the absence of a processor core in a given connector as long as the power supply used does not affect these lines. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

The VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator only if required by the regulator or external logic monitoring the VID[4:0] signals. The power source chosen must be guaranteed to be stable whenever the supply to the

voltage regulator is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. A resistor of greater than or equal to 10 kΩ may be used to connect the VID signals to the converter input.

2.7 Processor System Bus Unused Pins

All RESERVED pins must remain unconnected. Connection of these pins to $V_{CC_{CORE}}$, $V_{CC_{L2}}$/ $V_{CC_{3.3}}$, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium III processors. See Section 5.5 for a pin listing of the processor and the location of each RESERVED pin.

All TESTHI pins must be connected to 2.5 V via 1 kΩ –10 kΩ pull-up resistor.

PICCLK must be driven with a valid clock input and the PICD[1:0] lines must be pulled-up to 2.5 V even when the APIC will not be used. A separate pull-up resistor must be provided for each APIC data line.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused AGTL+ inputs should be left as no connects; AGTL+ termination is provided on the processor. Unused active low CMOS inputs should be connected through a resistor to 2.5 V. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused pins, it is suggested that ~10 kΩ resistors be used for pull-ups (except for PICD[1:0] discussed above), and ~1 kΩ resistors be used as pull-downs.

2.8 Processor System Bus Signal Groups

In order to simplify the following discussion, the Pentium III processor system bus signals have been combined into groups by buffer type. All Pentium III processor system bus outputs are open drain and require a high-level source provided externally by the termination or pull-up resistor. However, the Pentium III processor includes on-cartridge (CPUID=067xh) or on-die (CPUID=068xh) termination.

AGTL+ input signals have differential input buffers, which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

EMI pins may be connected to baseboard ground and/or to chassis ground through zero ohm (0 Ω) resistors. The 0 Ω resistors should be placed in close proximity to the SC242 connector. The path to chassis ground should be short in length and have a low impedance.

The CMOS, Clock, APIC, and TAP inputs can each be driven from ground to 2.5 V. The CMOS, APIC, and TAP outputs are open drain and should be pulled high to 2.5 V. This ensures not only correct operation for current Pentium III processors, but compatibility with future Pentium III processors as well.

The groups and the signals contained within each group are shown in Table 4. Refer to Section 7.0 for a description of these signals.

Table 4. System Bus Signal Groups

Group Name	Signals
AGTL+ Input	BPRI#, BR1#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[1], D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input[5]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD[2], SMI#, SLP#[3], STPCLK#
CMOS Output[5]	FERR#, IERR#, THERMTRIP#[4]
System Bus Clock	BCLK
APIC Clock	PICCLK
APIC I/O[5]	PICD[1:0]
TAP Input[5]	TCK, TDI, TMS, TRST#
TAP Output[5]	TDO
Power/Other[6]	VCC_{CORE}, VCC_{L2}/$VCC_{3.3}$, VCC_5, VID[4:0], V_{TT}, V_{SS}, SLOTOCC#, THERMDP, THERMDN, BSEL[1:0], EMI, TESTHI, Reserved

NOTES:
1. The BR0# pin is the only BREQ# signal that is bidirectional. The internal BREQ# signals are mapped onto BR# pins after the agent ID is determined. See Section 7.0 for more information.
2. See Section 7.0 for information on the PWRGOOD signal.
3. See Section 7.0 for information on the SLP# signal.
4. See Section 7.0 for information on the THERMTRIP# signal.
5. These signals are specified for 2.5 V operation.
6. VCC_{CORE} is the power supply for the processor core.
   VCC_{L2}/$VCC_{3.3}$ is described in Section 2.3.
   VID[4:0] is described in Section 2.6.
   V_{TT} is used to terminate the system bus and generate V_{REF} on the processor substrate.
   V_{SS} is system ground.
   TESTHI should be connected to 2.5 V with a 1 kΩ –10 kΩ resistor.
   VCC_5 is not connected to the Pentium III processor core. This supply is used for the test equipment and tools.
   SLOTOCC# is described in Section 7.0.
   BSEL[1:0] is described in Section 2.8.2 and Section 7.0.
   EMI pins are described in Section 7.0.
   THERMDP, THERMDN are described in Section 7.0.

2.8.1 Asynchronous vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, Clock, APIC, and TAP signals can be applied asynchronously to BCLK.

All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.8.2 System Bus Frequency Select Signal (BSEL0)

The BSEL[1:0] signals (BSEL0 is also known as 100/66#) are used to select the system bus frequency for the Pentium III processor(s). Table 5 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), and frequency synthesizer. All system bus agents must operate at the same core and system bus frequency in a 2-way MP Pentium III processor configuration. In a 2-way MP system design, the BSEL[1:0] signals must be connected to the BSEL[1:0] pins of both processors. The Pentium III processor operates at either a 100 MHz or 133 MHz system bus frequency, but not both. 66 MHz system bus operation is not supported.

For systems that support only a 100 MHz system bus clock, resistors on the processor cartridge will tie the BSEL1 signal to ground (as shown in Figure 4). This signal can either be left as a no connect or tied to ground as shown below. The BSEL0 should be pulled up to 3.3 V with a 220 Ω resistor, and provided as a frequency driver to the clock driver/synthesizer.

On baseboards which support operation at either 100 or 133 MHz, the BSEL[1:0] signals should be pulled up to 3.3 V with a 220 Ω resistor (as shown in Figure 5 and Figure 6) and BSEL1 is provided as a frequency selection signal to the clock driver/synthesizer. The BSEL0 signal can also be incorporated into system shutdown logic on the baseboard (thus forcing the system to shutdown as long as the BSEL0 signal is low). Figure 4 shows this routing example with a 100 MHz Pentium III processor. Figure 5 shows the same routing example with a 133 MHz Pentium III processor.

Table 5. Frequency Select Truth Table for BSEL[1:0]

BSEL1	BSEL0	Frequency
0	0	66 MHz (unsupported)
0	1	100 MHz
1	0	Reserved
1	1	133 MHz

Figure 4. BSEL[1:0] Example for a 100 MHz System Design (100 MHz Processor Installed)

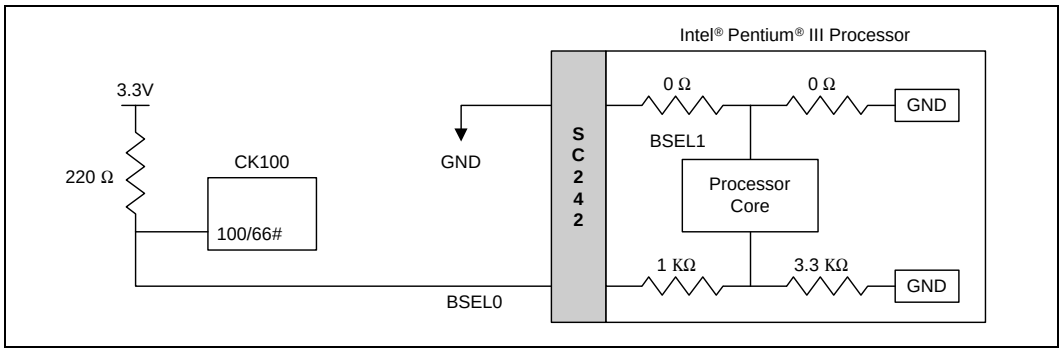


Figure 5. BSEL[1:0] Example for a 100/133 MHz Capable System (100 MHz Processor Installed)

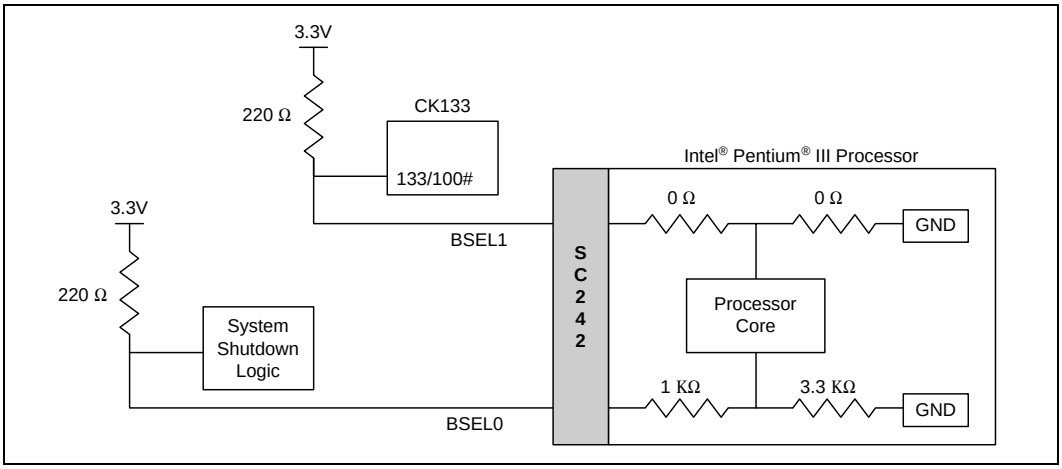
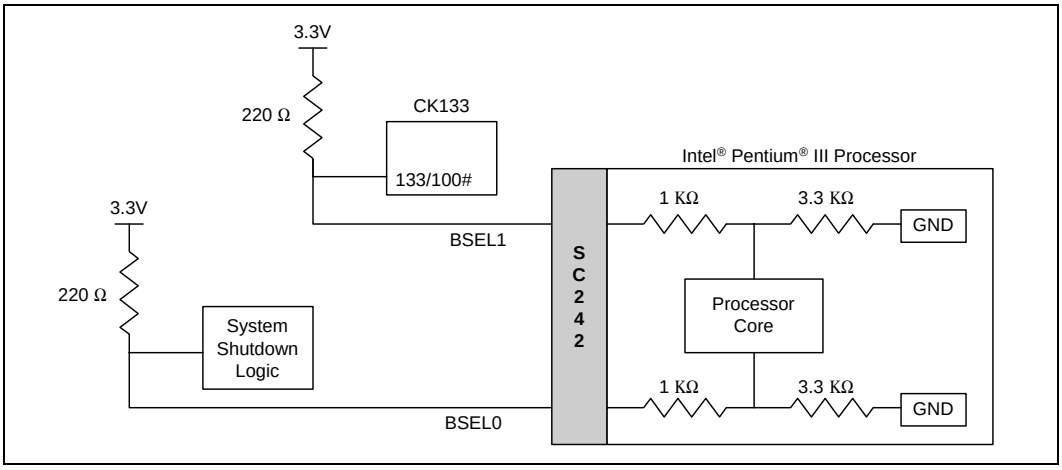


Figure 6. BSEL[1:0] Example for a 100/133 MHz Capable System (133 MHz Processor Installed)



2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium III processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting a 2.5 V input. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

The Debug Port should be placed at the start and end of the TAP chain with the TDI of the first component coming from the Debug Port and the TDO from the last component going to the Debug Port. In a 2-way MP system, be cautious when including an empty SC242 connector in the scan chain. All connectors in the scan chain must have a processor installed to complete the chain or the system must support a method to bypass the empty connectors; SC242 terminator substrates should not connect TDI to TDO in order to avoid placing the TDO pull-up resistors in parallel. See *SC242 Terminator Card Design Guidelines* (Document Number 243409) for more details.

2.10 Maximum Ratings

Table 6 contains Pentium III processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables in Section 2.11 and Section 2.13. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 6. Absolute Maximum Ratings (CPUID=067xh)

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
$V_{CC(All)}$	Any processor supply voltage with respect to V_{SS}	–0.5	Operating voltage + 1.0	V	1, 2
Vin_{AGTL}	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.3	$V_{CC_{CORE}}$ + 0.7	V	
Vin_{CMOS}	CMOS buffer DC input voltage with respect to V_{SS}	–0.3	3.3	V	3
I_{VID}	Max VID pin current		5	mA	
$I_{SLOTOCC}$	Max SLOTOCC# pin current		5	mA	
Mech Max Latch Arms	Mechanical integrity of latch arms		50	Cycles	4, 7
Mech Max Edge Fingers	Mechanical integrity of processor edge fingers		50	Insertions/ Extractions	5, 6

NOTES:
1. Operating voltage is the voltage to which the component is designed to operate. See Table 8.
2. This rating applies to the $V_{CC_{CORE}}$, $V_{CC_{L2}}$/$V_{CC_{3.3}}$, V_{CC_5}, and any input (except as noted below) to the processor.
3. Parameter applies to CMOS, APIC, and TAP bus signal groups only.
4. The mechanical integrity of the latch arms is specified to last a maximum of 50 cycles.
5. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/ extraction cycles.
6. While insertion/extraction cycling above 50 insertions will cause an increase in the contact resistance (above 0.1 Ω) and a degradation in the material integrity of the edge finger gold plating, it is possible to have processor functionality above the specified limit. The actual number of insertions before processor failure will vary based upon system configuration and environmental conditions.
7. This specification only applies to S.E.C.C. packaged processors.

Table 7. Absolute Maximum Ratings (CPUID=068xh)

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
$V_{CC_{CORE}}$ and V_{TT}	Processor core voltage and Termination supply voltage with respect to V_{SS}	-0.5	2.1	V	
$V_{CC_{L2}}/V_{CC_{3.3}}$	$V_{CC_{3.3}}$ with respect to V_{SS}	–0.5	5.0	V	1
$Vin_{1.5}$	1.5 V buffer input voltage	V_{TT} – 2.3	V_{SS} + 2.3	V	2, 3, 5
$Vin_{2.5}$	2.5 V buffer input voltage	–0.7	3.3	V	4
I_{VID}	Max VID pin current		5	mA	
$I_{SLOTOCC}$	Max SLOTOCC# pin current		5	mA	
Mech Max Edge Fingers	Mechanical integrity of processor edge fingers		50	Insertions/ Extractions	6, 7

NOTES:
1. Operating voltage is the voltage to which the component is designed to operate. See Table 7.
2. Input voltage can never be above V_{SS} + 2.3 V.
3. Input voltage can never be below V_{TT} – 2.3 V.
4. Parameter applies to the 2.5 V processor core signals (BCLK, PICCLK, and PWRGOOD).
5. Parameter applies to the 1.5 V processor core signals (all signals except BCLK, PICCLK, and PWRGOOD).
6. The electrical and mechanical integrity of the processor edge fingers are specified to last for 50 insertion/ extraction cycles.
7. While insertion/extraction cycling above 50 insertions will cause an increase in the contact resistance (above 0.1 Ω) and a degradation in the material integrity of the edge finger gold plating, it is possible to have processor functionality above the specified limit. The actual number of insertions before processor failure will vary based upon system configuration and environmental conditions.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the Pentium III processor core pins, edge fingers, and at the SC242 connector pins. See Section 7.0 for the processor edge finger signal definitions and Section 5.0 for the core pin locations and the signal listing.

Most of the signals on the Pentium III processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in Table 9.

To allow connection with other devices, the Clock, CMOS, APIC, and TAP signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in Table 10.

Table 8 through Table 11 list the DC specifications for Pentium III processors. Specifications are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 8. Voltage and Current Specifications (Sheet 1 of 4)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes[1]
		Core Freq	CPUID					
Vcc_{CORE}	Vcc for Processor Core	450 MHz	0672h		2.00		V	2,3,4,5
			0673h		2.00			2,3,4,5
		500 MHz	0672h		2.00			2,3,4,5
			0673h		2.00			2,3,4,5
		533 MHz	0672h		2.00			2,3,4,5
			0673h		2.00			2,3,4,5
		533EB MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		550 MHz	0672h		2.00			2,3,4,5
			0673h		2.00			2,3,4,5
		550E MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		600 MHz	0672h		2.05			2,3,4,5
			0673h		2.05			2,3,4,5
		600B MHz	0672h		2.05			2,3,4,5
			0673h		2.05			2,3,4,5
		600E MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		600EB MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		650 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		667 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		700 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		733 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		750 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		800 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5

Table 8. Voltage and Current Specifications (Sheet 2 of 4)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes[1]
		Core Freq	CPUID					
Vcc_{CORE}	Vcc for Processor Core	800EB MHz	0681h		1.65		V	2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		850 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		866 MHz	0681h		1.65			2,3,4,5
			0683h		1.65			2,3,4,5
			0686h		1.70			2,3,4,5
		933 MHz	0683h		1.70			2,3,4,5
			0686h		1.70			2,3,4,5
		1.0 GHz	0683h		1.70			2,3,4,5
			0686h		1.70			2,3,4,5
		1.0B GHz	0683h		1.70			2,3,4,5
			0686h		1.70			2,3,4,5
Vcc_{L2}/ $Vcc_{3.3}$	Vcc for second level cache or voltage clamp logic			3.135	3.3	3.465	V	3.3 V ±5% [9]
V_{TT}	AGTL+ bus termination voltage			1.365	1.50	1.635	V	1.5 ±9% [6]
Baseboard Tolerance, Static	Processor core voltage static tolerance level at SC242 pins			–0.070 –0.080 –0.050 –0.055		0.070 0.040 0.040 0.040	V	2, 7, 18 2, 7, 19 2, 7, 21 2, 7
Baseboard Tolerance, Transient	Processor core voltage transient tolerance level at SC242 pins			–0.140 –0.080 –0.050 –0.055		0.140 0.050 0.050 0.050	V	2, 7, 18 2, 7, 19 2, 7, 21 2, 7
Vcc_{CORE} Tolerance, Static	Processor core voltage static tolerance level at edge fingers			–0.085 –0.110 –0.065 –0.075		0.085 0.040 0.040 0.040	V	2, 8, 18 2, 8, 19 2, 8, 21 2, 8
Vcc_{CORE} Tolerance, Transient	Processor core voltage transient tolerance level at edge fingers			–0.170 –0.110 –0.065 –0.075		0.170 0.080 0.080 0.080	V	2, 8, 18 2, 8, 19 2, 8, 21 2, 8

Table 8. Voltage and Current Specifications (Sheet 3 of 4)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes[1]
		Core Freq	CPUID					
$I_{CC_{CORE}}$	I_{CC} for processor core	450 MHz 500 MHz 533B MHz 533EB MHz 550 MHz 550E MHz 600 MHz 600B MHz 600E MHz 600EB MHz 650 MHz 667 MHz 700 MHz 733 MHz 750 MHz 800 MHz 800EB MHz 850 MHz 866 MHz 933 MHz 1.0 GHz 1.0B GHz	ALL			14.5 16.1 16.7 10.6 17.0 11.0 17.8 17.8 13.0 13.0 13.0 13.3 14.0 14.6 15.0 16.0 16.0 16.2 16.3 17.7 19.4 19.4	A	2, 3, 10, 11 2, 3, 10, 11 2, 3, 10, 11 2, 3, 20 2, 3, 10, 11 2, 3, 20 2, 3, 10, 11 2, 3, 10, 11 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20 2, 3, 20, 21 2, 3, 20, 21
$I_{CC_{L2}}$	I_{CC} for second level cache	450 MHz 500 MHz 533B MHz 550 MHz 600 MHz 600B MHz				1.08 1.21 1.29 1.33 1.45 1.45	A	2, 9, 10, 18 2, 9, 10, 18 2, 9, 10, 18 2, 9, 10, 18 2, 9, 10, 18 2, 9, 10, 18
I_{VTT}	Termination voltage supply current	ALL				2.7	A	12
$I_{SG_{nt}}$	I_{CC} Stop-Grant for processor core	450 MHz 500 MHz 533B MHz 533EB MHz 550 MHz 550E MHz 600 MHz 600B MHz 600E MHz 600EB MHz 650 MHz 667 MHz 700 MHz 733 MHz 750 MHz 800 MHz 800EB MHz 850 MHz 866 MHz 933 MHz 1.0 GHz 1.0B GHz	ALL			1.20 1.40 1.49 2.50 1.54 2.50 1.68 1.68 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50	A	2, 10, 13 2, 10, 13
$I_{SG_{ntL2}}$	I_{CC} Stop-Grant for second level cache					0.1	A	2, 9, 10, 18

Table 8. Voltage and Current Specifications (Sheet 4 of 4)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes[1]
		Core Freq	CPUID					
I_{SLP}	I_{CC} Sleep for processor core	450 MHz 500 MHz 533B MHz 533EB MHz 550 MHz 550E MHz 600 MHz 600B MHz 600E MHz 600EB MHz 650 MHz 667 MHz 700 MHz 733 MHz 750 MHz 800 MHz 800EB MHz 850 MHz 866 MHz 933 MHz 1.0 GHz 1.0B GHz	ALL			0.80 0.90 1.00 2.50 1.00 2.50 1.00 1.00 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50 2.50	A	2, 10 2, 10
$I_{SL_{PL2}}$	I_{CC} Sleep for second level cache					0.1	A	2, 9, 10, 18
I_{DSLP}	I_{CC} Deep Sleep for processor core					0.50 2.20 3.00	A	2, 10, 18 2, 10, 19 2, 10
$I_{DSL_{PL2}}$	I_{CC} Deep Sleep for second level cache					0.1	A	2, 9, 10, 18
$dICC_{CORE}/dt$	Power supply current slew rate					20	A/µs	2, 14, 15, 16
$dICC_{L2}/dt$	L2 cache power supply current slew rate					1	A/µs	14, 15, 16, 18
$dICC_{VTT}/dt$	Termination current slew rate					8	A/µs	14, 15, See Table 11
V_{CC_5}	5 V supply voltage			4.75	5.00	5.25	V	5 V ±5% [16, 17]
I_{CC_5}	I_{CC} for 5 V supply voltage				1.0		A	17

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. This specification applies to Pentium III processors. For baseboard compatibility information on Pentium II processors, refer to the *Intel® Pentium® II Processor at 350, 400 and 450 MHz* datasheet (Document Number 243657).
3. $V_{CC_{CORE}}$ and $I_{CC_{CORE}}$ supply the processor core.
4. A variable voltage source should exist on all systems in the event that a different voltage is required. See Table 3 for more information.
5. Use the Typical Voltage specification with the Tolerance specifications to provide correct voltage regulation to the processor.
6. V_{TT} must be held to 1.5 V ±9%. It is recommended that V_{TT} be held to 1.5 V ±3% while the Pentium III processor system bus is idle. This is measured at the processor edge fingers across a 20 MHz bandwidth.
7. These are the tolerance requirements, across a 20 MHz bandwidth, at the SC242 connector pin on the bottom side of the baseboard. The requirements at the SC242 connector pins account for voltage drops (and impedance discontinuities) across the connector, processor edge fingers, and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event; see the *VRM 8.4 DC-DC Converter Design Guidelines* (Document Number 245335) for further details.
8. These are the tolerance requirements, across a 20 MHz bandwidth, at the processor edge fingers. The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event.

9. VCC_{L2}/$VCC_{3.3}$ and I_{CCL2}/$I_{CC3.3}$ supply the second level cache (“Discrete” cache type only). Unless otherwise noted, this specification applies to all Pentium III processor cache sizes. Systems should be designed for these specifications, even if a smaller cache size is used.
10. Max ICC measurements are measured at VCC max voltage, maximum temperature, under maximum signal loading conditions. The Max Icc currents specified do not occur simultaneously under the stress measurement condition.
11. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of VCC_{CORE} (VCC_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

$$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times VCC_{CORE\_TYP} / (VCC_{CORE\_TYP} + VCC_{CORE} \text{ Tolerance, Transient})$$

12. The current specified is the current required for a single Pentium III processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
13. The current specified is also for AutoHALT state.
14. Maximum values are specified by design/characterization at nominal VCC_{CORE} and nominal VCC_{L2}/$VCC_{3.3}$.
15. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
16. dI_{CC}/dt specifications are measured and specified at the SC242 connector pins.
17. VCC_5 and ICC_5 are not used by the Pentium III processors. The VCC_5 supply is used for the test equipment and tools.
18. This specification applies to the Pentium III processor with CPUID=067xh.
19. This specification applies to the Pentium III processor with CPUID=068xh.
20. Max I_{CC} measurements are measured at VCC nominal voltage, maximum temperature, under maximum signal loading conditions. The Max Icc currents specified do not occur simultaneously under the stress measurement condition.
21. . This specification applies to the Pentium III processor with CPUID=0683h operating at 1.0 GHz.

Table 9. AGTL+ Signal Groups DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1, 4, 5]
V_{IL}	Input Low Voltage	–0.30 –0.15	0.82 V_{REF} – 0.20	V V	12 13
V_{IH}	Input High Voltage	1.22 V_{REF} + 0.20	V_{TT} V_{TT}	V	2, 3, 12 2, 3, 13
Ron	Buffer On Resistance		16.67	Ω	9
I_L	Leakage Current		±100 ±100	µA µA	6, 7, 8, 12 6, 10, 11, 13

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processor frequencies.
2. V_{IH} and V_{OH} for the Pentium III processor may experience excursions up to 200 mV above V_{TT} for a single system bus clock. However, input signal drivers must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 11.
4. Parameter correlated to measure into a 25 Ω resistor terminated to 1.5 V.
5. I_{OH} for the Pentium III processor may experience excursions of up to a 12 mA for a single bus clock.
6. Leakage current affects input, output, and I/O signals.
7. ($0 \le V_{IN} \le 2.0$ V +5%).
8. ($0 \le V_{OUT} \le 2.0$ V +5%).
9. Refer to the Pentium III I/O Buffer Models for I/V characteristics.
10. ($0 \le V_{IN} \le 1.5$ V +5%).
11. ($0 \le V_{OUT} \le 1.5$ V +5%).
12. This specification applies to the Pentium III processor with CPUID=067xh.
13. This specification applies to the Pentium III processor with CPUID=068xh.

Table 10. Non-AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes [1]
V_{IL}	Input Low Voltage	–0.30 –0.15 –0.30 –0.30 –0.15	0.5 0.7 0.5 0.7 0.7	V V V V V	3, 8 3, 9, 10 2, 9; BCLK only 2, 9; PICCLK only 2, 9; PWRGOOD only
V_{IH}	Input High Voltage	1.7 1.7 2.0	2.625 2.625 2.625	V V V	3, 8 3, 9, 10 2, 9; BCLK, PICCLK, and PWRGOOD only
V_{OL}	Output Low Voltage		0.5	V	3, 4
V_{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain
I_{OL}	Output Low Current	14		mA	3, 11
I_L	Leakage Current		±100	µA	5, 6, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. These values are specified at the processor core pins.
3. These values are specified at the processor edge fingers.
4. Parameter measured at 14 mA (for use with TTL inputs).
5. Leakage current affects input, output and I/O signals.
6. ($0 \le V_{IN} \le 2.5$ V +5%).
7. ($0 \le V_{OUT} \le 2.5$ V +5%).
8. This specification applies to the Pentium III processor with CPUID=067xh.
9. This specification applies to the Pentium III processor with CPUID=068xh.
10. Parameters apply to all non-AGTL+ signals except for BCLK, PICCLK, and PWRGOOD.
11. Specified as the minimum amount of current that the output buffer must be able to sink. However, VOL Max cannot be guaranteed if this specification is exceeded.

2.12 AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to VTT at each end of the signal trace. These termination resistors are placed electrically between the ends of the signal traces and the VTT voltage supply and generally are chosen to approximate the substrate impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}.

Table 11 lists the nominal specification for the AGTL+ termination voltage (VTT). The AGTL+ reference voltage (V_{REF}) is generated on the processor substrate for the processor core, but should be set to 2/3 VTT for other AGTL+ logic using a voltage divider on the baseboard. It is important that the baseboard impedance be specified and held to a ±15% tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on the GTL+ buffer specification, see the *Intel® Pentium® II Processor Developer's Manual* (Document Number 243502) and AP-585, *Intel® Pentium® II Processor GTL+ Guidelines* (Document Number 243330).

Table 11. AGTL+ Bus Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1, 2]
VTT	Bus Termination Voltage	1.365	1.50	1.635	V	3
RTT	Termination Resistor		56		Ω	4
V_{REF}	Bus Reference Voltage	0.95	2/3 VTT	1.05	V	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. Pentium III processors contain AGTL+ termination resistors at the end of each signal trace on the processor substrate. Pentium III processors generate V_{REF} on the processor substrate by using a voltage divider on VTT supplied through the SC 242 connector.
3. VTT must be held to 1.5 V ±9%; $dI_{CC_{VTT}}/dt$ is specified in Table 8. It is recommended that VTT be held to 1.5 V ±3% while the Pentium III processor system bus is idle. This is measured at the processor edge fingers.
4. RTT must be held within a tolerance of ±5%
5. V_{REF} is generated on the processor substrate to be 2/3 VTT ±2% nominally.

2.13 System Bus AC Specifications

The Pentium III processor system bus timings specified in this section are defined at the Pentium III processor core pads. Unless otherwise specified, timings are tested at the processor core during manufacturing. See Section 7.0 for the Pentium III processor edge connector signal definitions. See Section 5.6 for the Pentium III processor closest accessible core pad to substrate via assignment.

Table 12 through Table 18 list the AC specifications associated with the Pentium III processor system bus. These specifications are broken into the following categories: Table 12 through Table 13 contain the system bus clock core frequency and cache bus frequencies, Table 14 contains the AGTL+ specifications, Table 15 contains the CMOS signal group specifications, Table 16 contains timings for the Reset conditions, Table 17 covers APIC bus timing, and Table 18 covers TAP timing.

All Pentium II processor system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium III processor in Viewlogic XTK model format (formerly known as QUAD format) as the *Intel® Pentium® III Processor I/O Buffer Models* on Intel's Developer's Website (http://developer.intel.com.) AGTL+ layout guidelines are also available in AP-906, *100 MHz AGTL+ Layout Guidelines for the Intel® Pentium® III Processor and Intel® 440BX AGPset* (Document Number 245086) or the appropriate platform design guide.

Care should be taken to read all notes associated with a particular timing parameter.

Table 12. System Bus AC Specifications (Clock) at Processor Core Pins

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1, 2, 3]
System Bus Frequency			100.00 133.33	MHz MHz		4, 10 4, 11
T1: BCLK Period	10.0 7.5			ns ns	7 7	4, 5, 10 4, 5, 11
T2: BCLK Period Stability			±250	ps	7	7, 9
T3: BCLK High Time	2.5 1.4			ns ns	7 7	@>2.0 V, 10 @>2.0 V, 11
T4: BCLK Low Time	2.4 1.4			ns ns	7 7	@<0.5 V [6, 10] @<0.5 V [6, 11]
T5: BCLK Rise Time	0.4		1.60	ns	7	(0.5 V–2.0 V) [8, 10, 11]
T6: BCLK Fall Time	0.4		1.60	ns	7	(2.0 V–0.5 V) [8, 10, 11]

1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the Pentium III processor system bus clock. The system bus clock to core clock ratio is fixed for each processor. Individual processors will only operate at their specified system bus frequency, either 100 MHz or 133 MHz. Table 13 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
6. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor core pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
7. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer.
8. Not 100% tested. Specified by design characterization as a clock driver requirement.
9. The average period over a 1uS period of time must be greater than the minimum specified period.
10. This specification applies to the Pentium III processor with a system bus frequency of 100 MHz.
11. This specification applies to the Pentium III processor with a system bus frequency of 133 MHz.

Table 13. Valid System Bus, Core Frequency, and Cache Bus Frequencies

Processor	Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier	L2 Cache (MHz)	Notes[1]
450	450	100	9/2	225	
500	500	100	5	250	
533B	533	133	4	267	
533EB	533	133	4	533	
550	550	100	11/2	275	
550E	550	100	11/2	550	
600	600	100	6	300	
600B	600	133	9/2	300	
600E	600	100	6	600	
600EB	600	133	9/2	600	
650	650	100	13/2	650	
667	666.67	133	5	666.67	
700	700	100	7	700	
733	733	133	11/2	733	
750	750	100	15/2	750	
800	800	100	8	800	
800EB	800	133	6	800	
850	850	100	17/2	850	
866	866	133	13/2	866	
933	933	133	7	933	
1.0 GHz	1000.0	100	10	1000.0	
1.0B GHz	1000.0	133	15/2	1000.0	

NOTE:
1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.

Table 14. System Bus AC Specifications (AGTL+ Signal Group) at the Processor Core Pins

T# Parameter	Min	Max	Unit	Figure	Notes[1, 2, 3]
T7: AGTL+ Output Valid Delay	-0.20 -0.14 -0.10	3.15 2.20 2.70	ns ns ns	8 8 8	4, 10, 13 5, 11, 13 5, 11, 12, 14
T8: AGTL+ Input Setup Time	1.90 1.20 1.20		ns ns ns	9 9 9	6, 7, 8, 11, 13 6, 7, 8, 12, 13 6, 7, 8, 11, 12, 14
T9: AGTL+ Input Hold Time	0.85 0.58 0.80		ns ns ns	9 9 9	9, 11, 13 9, 12, 13 9, 11, 12, 14
T10: RESET# Pulse Width	1.00		ms	11	7, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V at the processor core pins.
4. Valid delay timings for these signals are specified into 25 Ω to 1.5 V and with V_{REF} at 1.0 V.
5. Valid delay timings for these signals are specified into 50 Ω to 1.5 V and with V_{REF} at 1.0 V.
6. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
7. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously. For 2-way MP systems, RESET# should be synchronous.
8. Specification is for a minimum 0.40 V swing.
9. Specification is for a maximum 1.0 V swing.
10. This should be measured after VCC_{CORE}, VCC_{L2}/$VCC_{3.3}$, and BCLK become stable.
11. This specification applies to the Pentium III processor with a system bus frequency of 100 MHz.
12. This specification applies to the Pentium III processor with a system bus frequency of 133 MHz.
13. This specification applies to the Pentium III processor with CPUID=067xh.
14. This specification applies to the Pentium III processor with CPUID=068xh.

Table 15. System Bus AC Specifications (CMOS Signal Group) at the Processor Core Pins

T# Parameter	Min	Max	Unit	Figure	Notes[1, 2, 3, 4]
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	8	Active and Inactive states
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	8, 11	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 0.7 V at the processor core pins. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V.
4. These signals may be driven asynchronously.
5. When driven inactive or after VCC_{CORE}, VCC_{L2}/$VCC_{3.3}$, and BCLK become stable.

Table 16. System Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes[1]
T16: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	10	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	10	After clock that deasserts RESET#

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.

Table 17. System Bus AC Specifications (APIC Clock and APIC I/O) at the Processor Core Pins

T# Parameter	Min	Max	Unit	Figure	Notes[1, 2, 3]
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	7	
T23: PICCLK High Time	12.0		ns	7	
T24: PICCLK Low Time	12.0		ns	7	
T25: PICCLK Rise Time	0.25	3.0	ns	7	
T26: PICCLK Fall Time	0.25	3.0	ns	7	
T27: PICD[1:0] Setup Time	8.0 5.0		ns ns	9 9	4, 7 4, 8
T28: PICD[1:0] Hold Time	2.5		ns	9	4
T29: PICD[1:0] Valid Delay	1.5	10	ns	8	4, 5, 6, 7
T29a: PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	ns	8	4, 5, 6, 8
T29b: PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0	ns	8	4, 5, 6, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor core pins. All APIC I/O signal timings are referenced at 1.25 V (CPUID=067xh) or 0.75 V (CPUID=068xh) at the processor core pins.
4. Referenced to PICCLK rising edge.
5. For open drain signals, valid delay is synonymous with float delay.
6. Valid delay timings for these signals are specified into a 150 Ω load pulled up to 2.5 V +5%.
7. This specification applies to the Pentium III processor with CPUID=067xh.
8. This specification applies to the Pentium III processor with CPUID=068xh.

Table 18. System Bus AC Specifications (TAP Connection) at the Processor Core Pins

T# Parameter	Min	Max	Unit	Figure	Notes[1, 2, 3]
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	7	
T32: TCK High Time	25.0 25.0		ns ns	7 7	@1.7 V [10, 11] @V_{REF} + 0.20 V [10, 12]
T33: TCK Low Time	25.0 25.0		ns ns	7 7	@0.7 V [10, 11] @V_{REF} – 0.20 V [10, 12]
T34: TCK Rise Time		5.0 5.0	ns ns	7 7	(0.7 V–1.7 V) [4, 10, 11] (V_{REF} – 0.20 V) – (V_{REF} + 0.20 V) [10, 12]
T35: TCK Fall Time		5.0 5.0	ns ns	7 7	(1.7 V–0.7 V) [4, 10] (V_{REF} + 0.20 V) – (V_{REF} – 0.20 V) [10, 12]
T36: TRST# Pulse Width	40.0		ns	13	Asynchronous [10]
T37: TDI, TMS Setup Time	5.0		ns	12	5
T38: TDI, TMS Hold Time	14.0		ns	12	5
T39: TDO Valid Delay	1.0	10.0	ns	12	6, 7
T40: TDO Float Delay		25.0	ns	12	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	12	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	12	6, 8, 9, 10

Table 18. System Bus AC Specifications (TAP Connection) at the Processor Core Pins

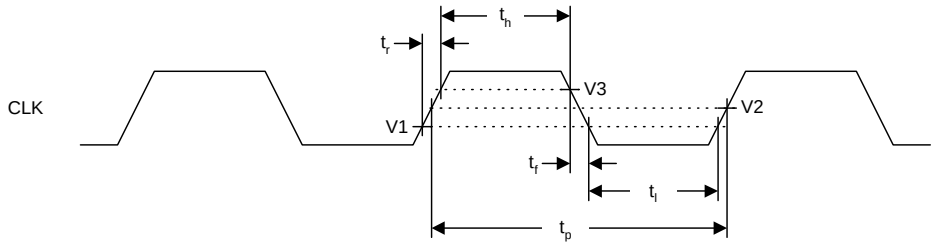
T# Parameter	Min	Max	Unit	Figure	Notes[1, 2, 3]
T43: All Non-Test Inputs Setup Time	5.0		ns	12	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	12	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 1.25 V (CPUID=067xh) or 0.75 V (CPUID=068xh) at the processor core pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 1.25 V (CPUID=067xh) or 0.75 V (CPUID=068xh) at the processor core pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 2.5 V +5%.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.
11. This specification applies to the Pentium III processor with CPUID=067xh.
12. This specification applies to the Pentium III processor with CPUID=068xh.

Note: For Figure 7 through Figure 13, the following apply:

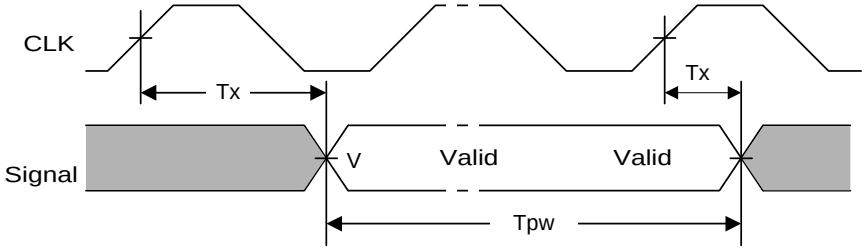
1. Figure 7 through Figure 13 are to be used in conjunction with Table 12 through Table 18.
2. All AC timings for the AGTL+ signals at the processor core pins are referenced to the BCLK rising edge at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.

Figure 7. BCLK, PICCLK, and TCK Generic Clock Waveform



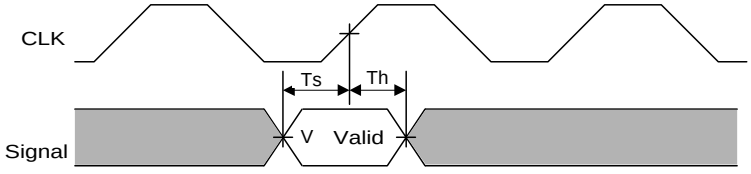
T_r = T5, T25, T34, (Rise Time)
T_f = T6, T26, T35, (Fall Time)
T_h = T3, T23, T32, (High Time)
T_l = T4, T24, T33, (Low Time)
T_p = T1, T22, T31 (BCLK, TCK, PICCLK Period)
V1 = BCLK = 0.5V, PICCLK = 0.7V, and TCK = 0.7V (CPUID 067xh) or V_{REF} - 0.20V (CPUID 068xh)
V2 = BCLK = 1.25V, PICCLK = 1.25V and TCK = 1.25V (CPUID 067xh) or 0.75V (CPUID 068xh)
V3 = BCLK = 2.0V, PICCLK = 1.7V (CPUID 067xh) or 2.0V (CPUID 068xh),
TCK = 1.7V (CPUID 067xh) or V_{REF} - 0.20V (CPUID 068xh)

Figure 8. System Bus Valid Delay Timings



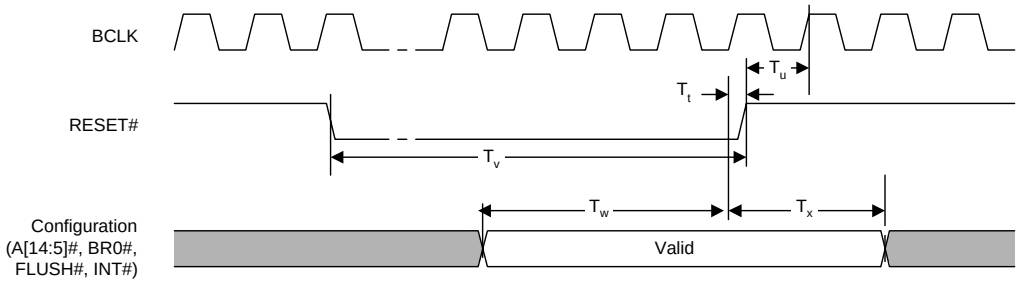
Tx = T7, T29, T29a, T29b (Valid Delay)
Tpw = T14, T15 (Pulse Width)
V = 1.0V for AGTL+ signal group; 1.25V (CPUID 067xh) or 0.75V (CPUID 068xh) for APIC and TAP signal groups

Figure 9. System Bus Setup and Hold Timings



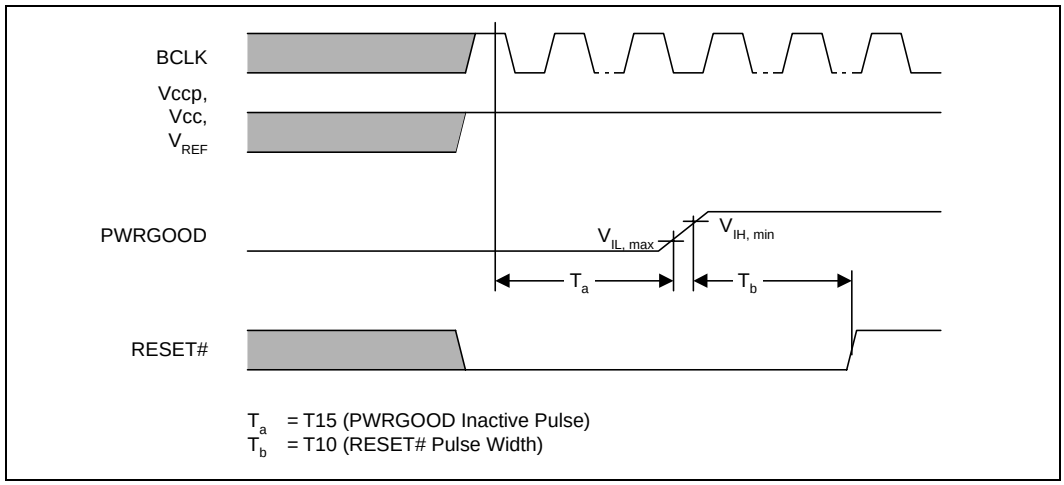
Ts = T8, T27 (Setup Time)
Th = T9, T28 (Hold Time)
V = 1.0V for AGTL+ signal group; 1.25V (CPUID 067xh) or 0.75V (CPUID 068xh) for APIC and TAP signal groups

Figure 10. System Bus Reset and Configuration Timings



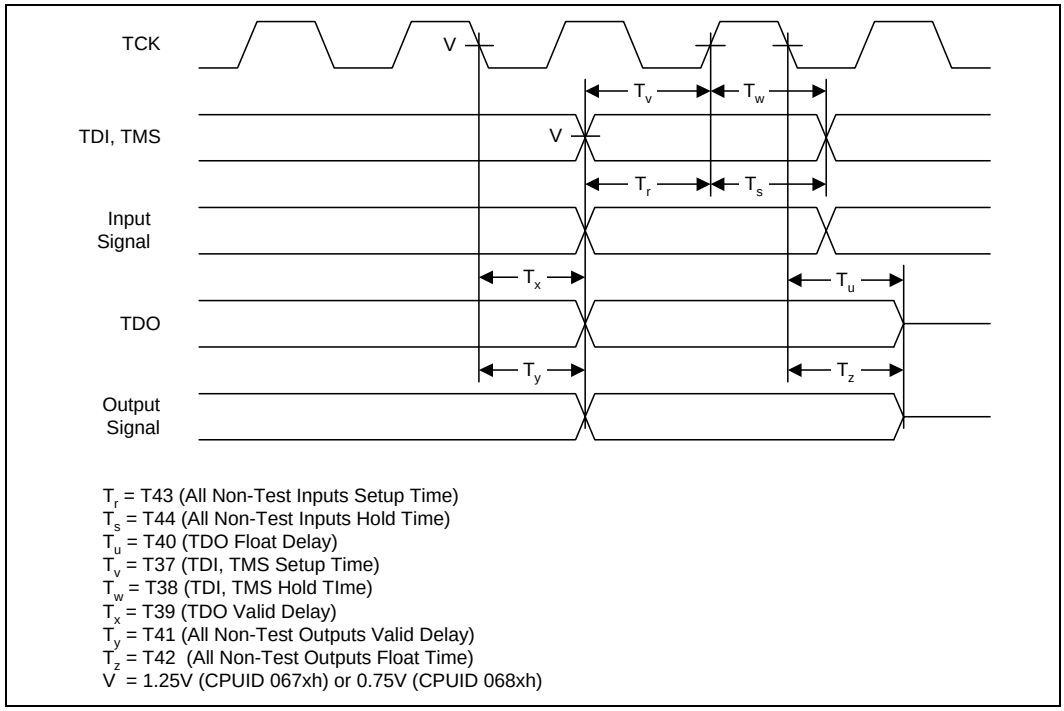
T_t = T9 (AGTL+ Input Hold Time)
T_u = T8 (AGTL+ Input Setup Time)
T_v = T10 (RESET# Pulse Width)
T_w = T16 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time)
T_x = T17 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time)

Figure 11. Power-On Reset and Configuration Timings



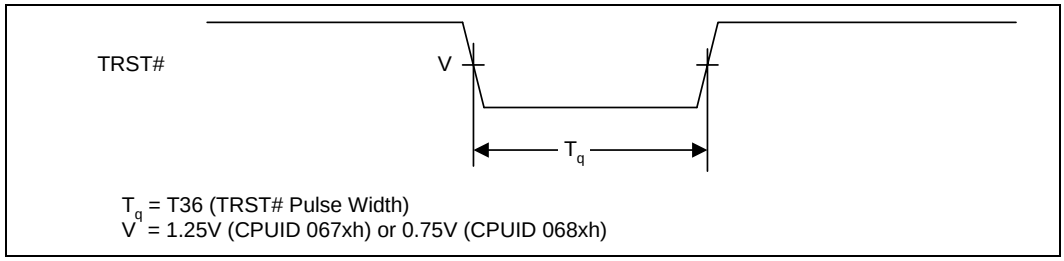
T_a = T15 (PWRGOOD Inactive Pulse)
T_b = T10 (RESET# Pulse Width)

Figure 12. Test Timings (TAP Connection)



T_r = T43 (All Non-Test Inputs Setup Time)
T_s = T44 (All Non-Test Inputs Hold Time)
T_u = T40 (TDO Float Delay)
T_v = T37 (TDI, TMS Setup Time)
T_w = T38 (TDI, TMS Hold TIme)
T_x = T39 (TDO Valid Delay)
T_y = T41 (All Non-Test Outputs Valid Delay)
T_z = T42 (All Non-Test Outputs Float Time)
V = 1.25V (CPUID 067xh) or 0.75V (CPUID 068xh)

Figure 13. Test Reset Timings



T_q = T36 (TRST# Pulse Width)
V = 1.25V (CPUID 067xh) or 0.75V (CPUID 068xh)

3.0 Signal Quality Specifications

Signals driven on the Pentium III processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation and measurement at the processor core; they should not be tested at the edge fingers.

The AGTL+ and non-AGTL+ signal quality specifications listed in this section apply to Pentium III processors with CPUID=068xh. It is recommended that these specifications be used with Pentium III processors with CPUID=067xh, however any deviations from these guidelines must be verified with the specifications listed in the *Intel® Pentium® II Processor Developer's Manual* (Document Number 243502).

3.1 BCLK, PICCLK, and PWRGOOD Signal Quality Specifications and Measurement Guidelines

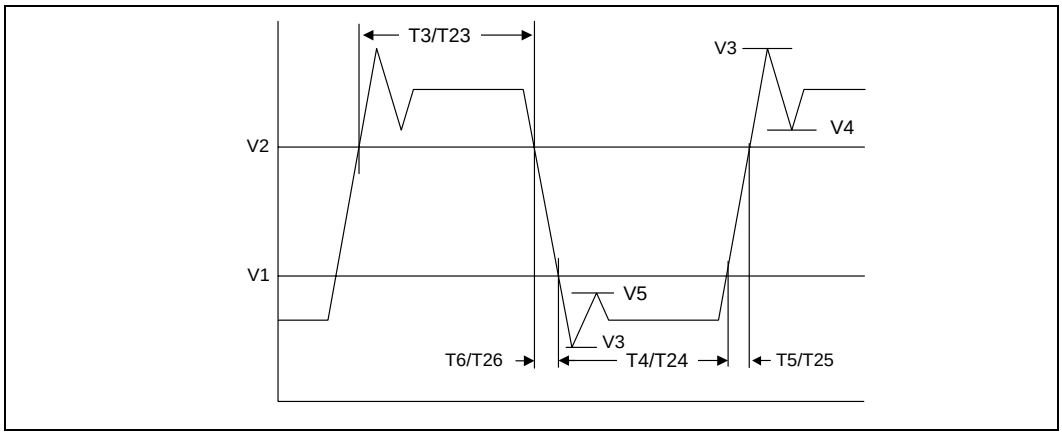
Table 19 describes the signal quality specifications at the processor core for the Pentium III processor system bus clock (BCLK), APIC clock (PICCLK), and PWRGOOD signals. Figure 14 describes the signal quality waveform for the system bus clock at the processor core pins.

Table 19. BCLK, PICCLK, and PWRGOOD Signal Quality Specifications at the Processor Core

V# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
V1: V_{IN} Absolute Voltage Range	–0.7		3.3	V	14	
V2: Rising Edge Ringback	2.0			V	14	2
V3: Falling Edge Ringback			0.5 0.7	V V	14 14	2 3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.
3. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the PICCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 14. BCLK and PICCLK Generic Clock Waveform



3.2 AGTL+ and Non-AGTL+ Overshoot/Undershoot Specifications and Measurement Guidelines

Overshoot/Undershoot is the absolute value of the maximum voltage differential across the input buffer relative termination voltage (VTT). The overshoot/undershoot guideline limits transitions beyond VTT or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot/undershoot events on 1.5 V or 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the Magnitude, the Pulse Duration, and the Activity Factor.

When performing simulations to determine impact of overshoot/undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot/undershoot protection. ESD diodes modeled within the Intel provided *Intel® Pentium® III Processor I/O Buffer Models* do not clamp overshoot/undershoot and will yield correct simulation results. If other I/O buffer models are being used to characterize Pentium III processor performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. The Intel-provided *Pentium® III Processor I/O Buffer Models* also contains I/O capacitance characterization. Therefore, removing the ESD diodes from the I/O buffer model will impact results and may yield excessive overshoot/undershoot.

3.2.1 Overshoot/Undershoot Magnitude

Overshoot/Undershoot Magnitude describes the maximum potential difference between a signal and its voltage reference level, VSS (overshoot) and VTT (undershoot). While overshoot can be measured relative to VSS using one probe (probe to signal - GND lead to VSS), undershoot must be measured relative to VTT. This could be accomplished by simultaneously measuring the VTT plane while measuring the signal undershoot. The true waveform can then be calculated by the oscilloscope itself or by the following oscilloscope date file analysis:

Converted Undershoot Waveform = VTT – Signal_measured

Note: The Converted Undershoot Waveform appears as a positive (overshoot) signal.

Note: Overshoot (rising edge) and undershoot (falling edge) conditions are separate and their impact must be determined independently.

After the conversion, the Undershoot/Overshoot Specifications (Table 20 through Table 22) can be applied to the Converted Undershoot Waveform using the same Magnitude and Pulse Duration Specifications (Table 20 through Table 22) as with an overshoot waveform.

Overshoot/undershoot magnitude levels must observe the Absolute Maximum Specifications (Table 20 through Table 22). These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed Pulse Durations. Provided that the magnitude of the overshoot/undershoot is within the Absolute Maximum Specifications, the impact of the Overshoot/Undershoot Magnitude may be determined based upon the Pulse Duration and Activity Factor.

3.2.2 Overshoot/Undershoot Pulse Duration

Overshoot/Undershoot Pulse duration describes the total time an overshoot/undershoot event exceeds the Overshoot/Undershoot Reference Voltage (V_{OS_REF} = 1.635 V). The total time could encompass several oscillations above the Reference Voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total Pulse Duration.

Note: Oscillations below the Reference Voltage can not be subtracted from the total Overshoot/ Undershoot Pulse Duration.

Note: Multiple Overshoot/Undershoot events occurring within the same clock cycle must be considered together as one event. Using the worst case Overshoot/Undershoot Magnitude, sum together the individual Pulse Durations to determine the total Overshoot/Undershoot Pulse Duration for that total event.

3.2.3 Overshoot/Undershoot Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of an AGTL+ or a CMOS signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs EVERY OTHER clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

The Overshoot/Undershoot Specifications (Table 20 through Table 22) show the Maximum Pulse Duration allowed for a given Overshoot/Undershoot Magnitude at a specific Activity Factor. Each table entry is independent of all others, meaning that the Pulse Duration reflects the existence of overshoot/undershoot events of that Magnitude ONLY. A platform with an overshoot/undershoot that just meets the Pulse Duration for a specific Magnitude where the AF < 1, means that there can be NO other overshoot/undershoot events, even of lesser Magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note: Overshoot (rising edge) and undershoot (falling edge) conditions are separate and their impact must be determined independently.

Note: Activity factor for AGTL+ signals is referenced to BCLK frequency.

Note: Activity factor for CMOS signals is referenced to PICCLK frequency.

3.2.4 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the Pentium III processor is not a simple single value. Instead, many factors are needed to determine what the over/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot (as measured above 1.635 V) and the Activity Factor (AF). To determine the allowed overshoot for a particular overshoot event, you must do the following:

1. Determine the signal group that particular signal falls into. If the signal is an AGTL+ signal operating with a 100 MHz system bus, use Table 20. If the signal is an AGTL+ signal operating with a 133 MHz system bus, use Table 21. If the signal is a CMOS signal, use Table 22.
2. Determine the Magnitude of the overshoot (relative to V_{SS}).
3. Determine the Activity Factor (how often does this overshoot occur?).
4. From the appropriate Specification table, read off the Maximum Pulse Duration (in ns) allowed.
5. Compare the specified Maximum Pulse Duration to the signal being measured. If the Pulse Duration measured is less than the Pulse Duration shown in the table, then the signal meets the specifications.

The above procedure is similar for undershoots after the undershoot waveform has been converted to look like an overshoot. Undershoot events must be analyzed separately from Overshoot events as they are mutually exclusive.

Below is an example showing how the maximum pulse duration is determined for a given waveform and how it relates to a measured value:

Platform Information:

- Signal Group = 133 MHz AGTL+
- Overshoot Magnitude (measured) = 2.3 V
- Pulse Duration (measured) = 1.6 ns
- Activity Factor (measured) = 0.1

Corresponding Maximum Pulse Duration Specification = 1.9 ns

Given the above parameters and using Table 21 (AF = 0.1 column), the maximum allowed pulse duration is 1.9 ns. Since the measured pulse duration is 1.6 ns, this particular overshoot event passes the overshoot specifications, although this doesn't guarantee that the combined overshoot/ undershoot events meet the specifications.

3.2.5 Determining If a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications (Table 20 through Table 22) specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However, most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (magnitude, duration, and AF). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may exceed the specifications. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. Ensure no signal (AGTL+ or 1.5 V non-AGTL+) ever exceeds the 1.635 V

   OR

2. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables. This means that whenever the over/undershoot event occurs, it always over/undershoots to the same level.

   OR

3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications (note: multiple overshoot/undershoot events within one clock cycle must have their pulse durations summed together to determine the total pulse duration). If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table where AF = 1, then the system passes.

Table 20. 100 MHz AGTL+ Signal Group Overshoot/Undershoot Tolerance

Overshoot/Undershoot Magnitude	Maximum Pulse Duration			Unit	Figure	Notes[1, 2, 3, 4, 5]
	AF = 0.01	AF = 0.1	AF = 1			
2.3 V	20	2.53	0.25	ns	15	
2.25 V	20	4.93	0.49	ns	15	
2.2 V	20	9.1	0.91	ns	15	
2.15 V	20	16.6	1.67	ns	15	
2.1 V	20	20	3.0	ns	15	
2.05 V	20	20	5.5	ns	15	
2.0 V	20	20	10	ns	15	

NOTES:
1. BCLK period is 10 ns.
2. These values are specified at the processor core pins.
3. Overshoot/Undershoot Magnitude = 2.3 V is an absolute value and should never be exceeded.
4. Overshoot is measured relative to V_{SS}, while undershoot is measured relative to V_{TT}.
5. Overshoot/Undershoot Pulse Duration is measured relative to 1.635 V.

Table 21. 133 MHz AGTL+ Signal Group Overshoot/Undershoot Tolerance

Overshoot/Undershoot Magnitude	Maximum Pulse Duration			Unit	Figure	Notes[1, 2, 3, 4, 5]
	AF = 0.01	AF = 0.1	AF = 1			
2.3 V	15	1.9	0.19	ns	15	
2.25 V	15	3.7	0.37	ns	15	
2.2 V	15	6.8	0.68	ns	15	
2.15 V	15	12.5	1.25	ns	15	
2.1 V	15	15	2.28	ns	15	
2.05 V	15	15	4.1	ns	15	
2.0 V	15	15	7.5	ns	15	

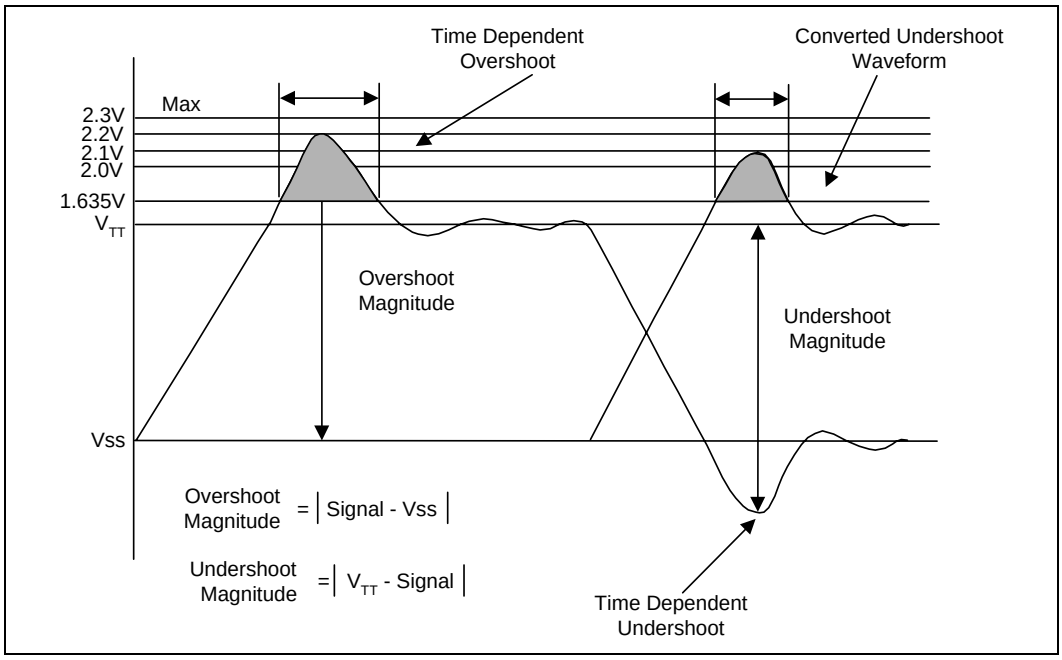
NOTES:
1. BCLK period is 7.5 ns.
2. These values are specified at the processor core pins.
3. Overshoot/Undershoot Magnitude = 2.3 V is an absolute value and should never be exceeded.
4. Overshoot is measured relative to V_{SS}, while undershoot is measured relative to V_{TT}.
5. Overshoot/Undershoot Pulse Duration is measured relative to 1.635 V.

Table 22. 33 MHz Non-AGTL+ Signal Group Overshoot/Undershoot Tolerance

Overshoot/Undershoot Magnitude	Maximum Pulse Duration			Unit	Figure	Notes[1, 2, 3, 4, 5, 6]
	AF = 0.01	AF = 0.1	AF = 1			
2.3 V	60	7.6	0.76	ns	15	
2.25 V	60	14.8	1.48	ns	15	
2.2 V	60	27.2	2.7	ns	15	
2.15 V	60	50	5	ns	15	
2.1 V	60	60	9.1	ns	15	
2.05 V	60	60	16.4	ns	15	
2.0 V	60	60	30	ns	15	

NOTES:
1. PICCLK period is 30 ns.
2. This table applies to all 1.5 V tolerant non-AGTL+ signals. BCLK, PICCLK, and PWRGOOD are the only non-AGTL+ signals that are 2.5 V tolerant at the processor core pins.
3. These values are specified at the processor core pins.
4. Overshoot/Undershoot Magnitude = 2.3 V is an absolute value and should never be exceeded.
5. Overshoot is measured relative to V_{SS}, while undershoot is measured relative to V_{TT}.
6. Overshoot/Undershoot Pulse Duration is measured relative to 1.635 V.

Figure 15. Maximum Acceptable AGTL+ and Non-AGTL+ Overshoot/Undershoot Waveform



3.3 AGTL+ and Non-AGTL+ Ringback Specifications and Measurement Guidelines

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is *the voltage that the signal rings back to after achieving its maximum absolute value.* (See Figure 16 for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for both AGTL+ and non-AGTL+ signals.

When performing simulations to determine the impact of ringback, ESD diodes must be properly characterized. The Intel provided *Pentium III Processor I/O Buffer Models* contain I/O capacitance characterization. Therefore, removing the ESD diodes from the I/O buffer model will impact results and may yield incorrect ringback. If other I/O buffer models are being used to characterize Pentium III processor performance, care must be taken to ensure that ESD models account for the I/O capacitance. See Table 24 for the signal ringback specifications for both AGTL+ and non-AGTL+ signals for simulations at the processor core.

Table 23. Signal Ringback Specifications for Signal Simulation

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes[1]
AGTL+	0 → 1	V_{REF} + 0.200	V	16	
AGTL+	1 → 0	V_{REF} – 0.200	V	16	
Non-AGTL+ Signals	0 → 1	1.7	V	16	2
Non-AGTL+ Signals	1 → 0	0.7	V	16	2
PWRGOOD	0 → 1	2.00	V	16	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies and cache sizes.
2. Non-AGTL+ signals except PWRGOOD.

There are three signal quality parameters defined for both AGTL+ and non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Table 24 for the AGTL+ and non-AGTL+ signal group.

Table 24. AGTL+ and Non-AGTL+ Signal Groups Ringback Tolerance Specifications [1, 2, 3, 4]

T# Parameter	Min	Unit	Figure	Notes
α_α: Overshoot	100	mV	16	4, 8
τ_τ: Minimum Time at High	0.50	ns	16	
ρ_ρ: Amplitude of Ringback	–200	mV	16	5, 6, 7, 8
ϕ_ϕ: Final Settling Voltage	200	mV	16	8
δ_δ: Duration of Squarewave Ringback	N/A	ns	16	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies and cache sizes.
2. These values are specified at the processor core pins.
3. Specifications are for the edge rate of 0.3 – 0.8 $^{V}/_{ns}$. See Figure 16 for the generic waveform.
4. See Table 22 for maximum allowable overshoot.
5. Ringback between V_{REF} + 100 mV and V_{REF} + 200 mV or V_{REF} –200 mV and V_{REF} – 100 mV requires the flight time measurements to be adjusted as described in the AGTL+ Specification (*Intel® Pentium® II Developers Manual*). Ringback below V_{REF} + 100 mV or above V_{REF} – 100 mV is not supported.
6. Intel recommends simulations not exceed a ringback value of V_{REF} ± 200 mV to allow margin for other sources of system noise.
7. A negative value for ρ_ρ indicates that the amplitude of ringback is above V_{REF}. (i.e., f = -100 mV specifies the signal cannot ringback below V_{REF} + 100 mV).
8. ϕ_ϕ and ρ_ρ: are measured relative to V_{REF}. α_α: is measured relative to V_{REF} + 200 mV.

Figure 16. Low to High AGTL+ and Non-AGTL+ Receiver Ringback Tolerance

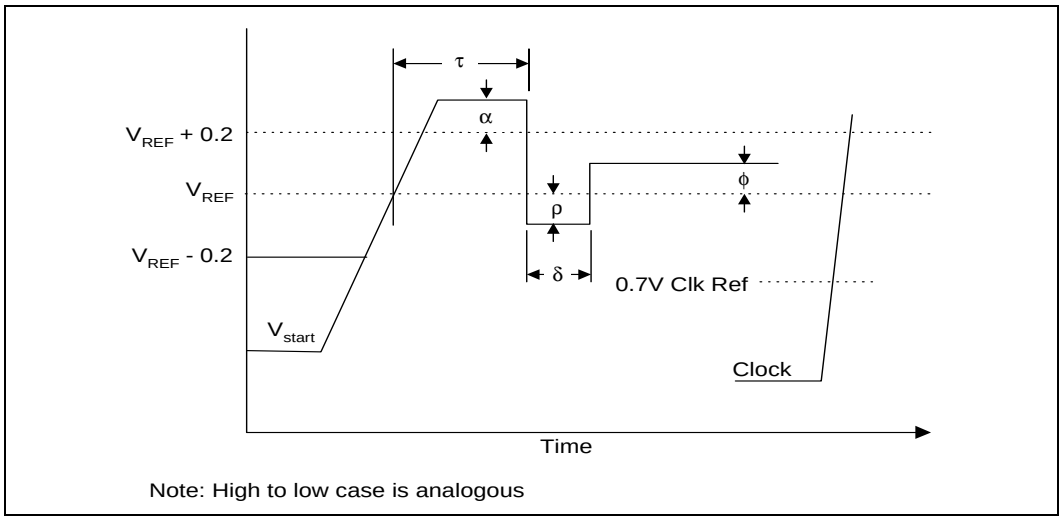
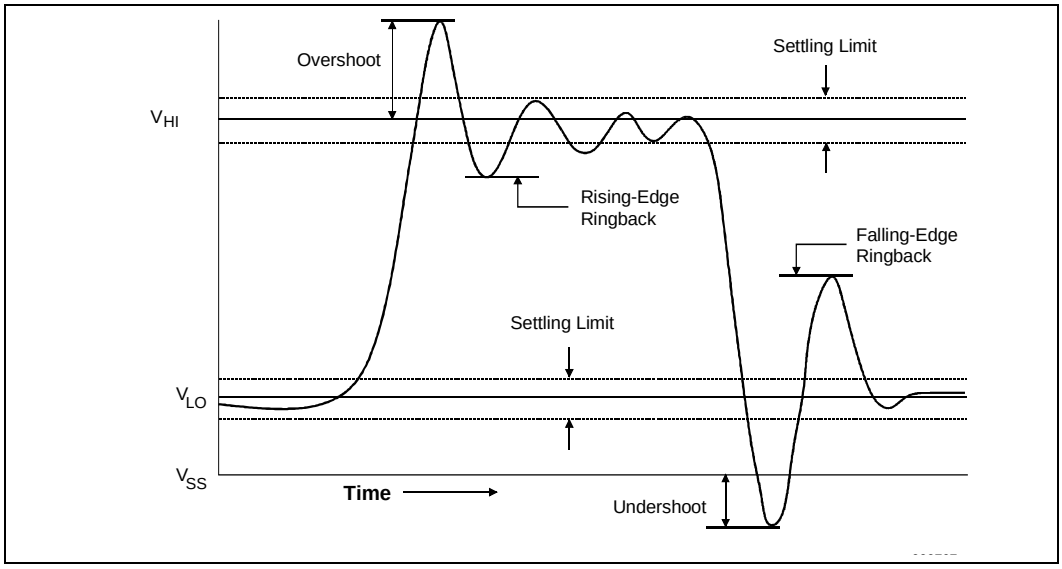


Figure 17. Signal Overshoot/Undershoot, Settling Limit, and Ringback



3.3.1 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10 percent of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

Limited quantities of Pentium III processors utilize S.E.C.C. package technology. This technology uses an extended thermal plate for heatsink attachment. The extended thermal plate interface is intended to provide accessibility for multiple types of thermal solutions. The majority of SC242-based Pentium III processors use S.E.C.C.2 packaging technology. S.E.C.C.2 package technology does not incorporate an extended thermal plate.

This chapter provides needed data for designing a thermal solution. However, for the correct thermal measuring processes, refer to AP-905, *Intel® Pentium® III Processor Thermal Design Guidelines* (Document Number 245087).

Figure 18 provides a 3-dimensional view of an S.E.C.C. package. This figure illustrates the thermal plate location. Figure 19 provides a substrate view of an S.E.C.C.2 package.

Figure 18. S.E.C.Cartridge — 3-Dimensional View

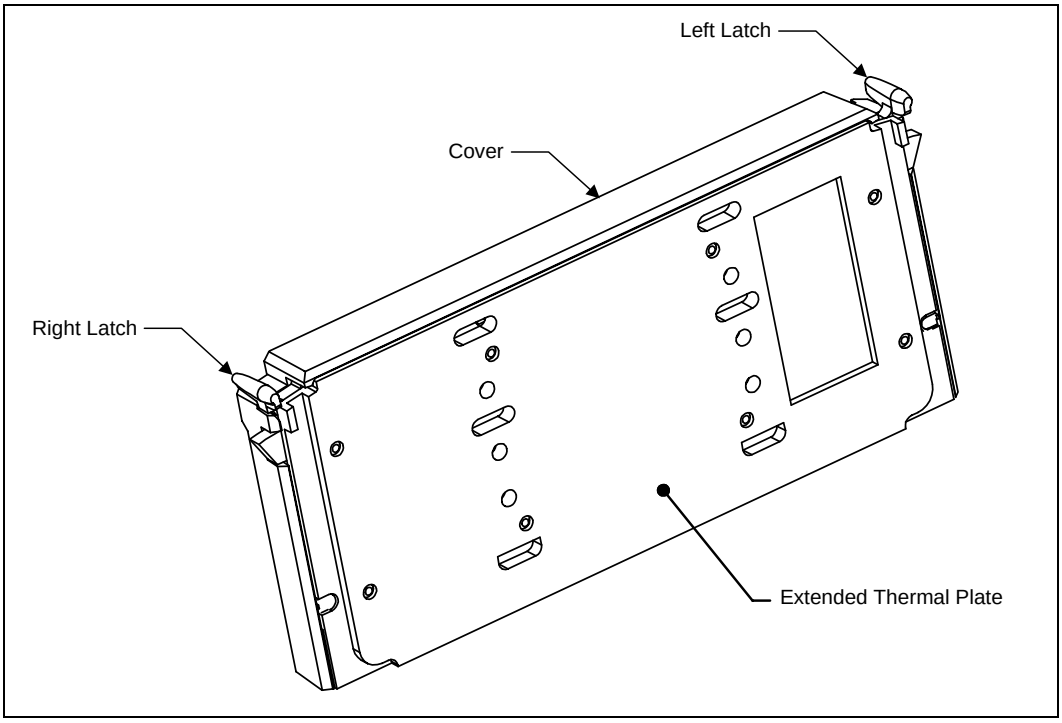
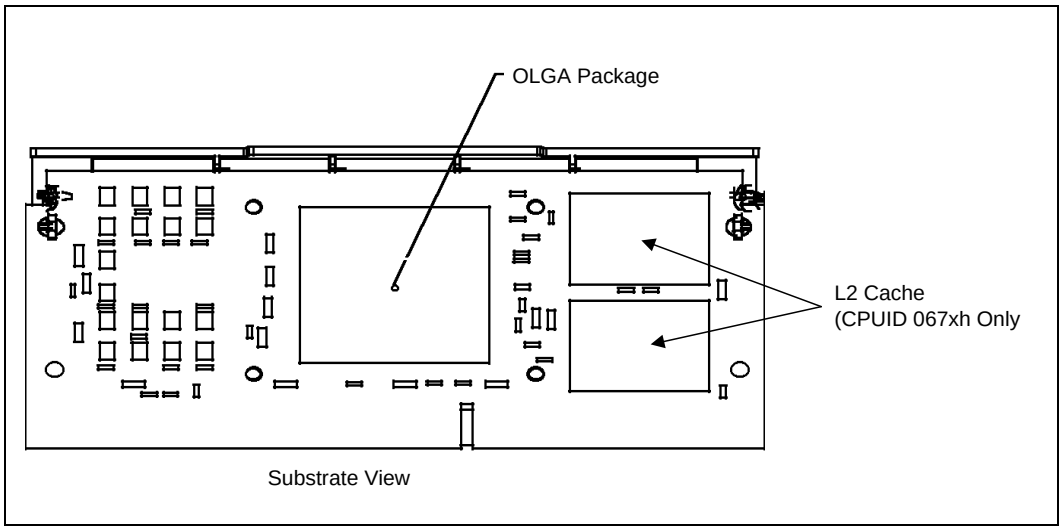


Figure 19. S.E.C.Cartridge 2 — Substrate View



4.1 Thermal Specifications

Table 25 and Table 26 provide the thermal design power dissipation and maximum and minimum temperatures for Pentium III processors with S.E.C.C. and S.E.C.C.2 package technologies respectively. While the processor core dissipates the majority of the thermal power, thermal power dissipated by the L2 cache also impacts the overall processor power specification. This total thermal power is referred to as processor power in the following specifications. Systems should design for the highest possible processor power, even if a processor with a lower thermal dissipation is planned.

Table 25. Thermal Specifications for S.E.C.C. Packaged Processors [1]

Processor Core Frequency (MHz)	L2 Cache Size (KBs)	Processor Power [2] (W)	Extended Thermal Plate Power [3] (W)	Min T_{PLATE} (°C)	Max T_{PLATE} (°C)	Min T_{COVER} (°C)	Max T_{COVER} (°C)
450	512	25.3	25.5	5	70	5	75
500	512	28.0	28.2	5	70	5	75

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor core and nominal $V_{CC_{L2}}/V_{CC_{3.3}}$ for the L2 cache (if applicable).
2. Processor power includes the power dissipated by the processor core, the L2 cache, and the AGTL + bus termination. The maximum power for each of these components does not occur simultaneously.
3. Extended Thermal Plate power is the processor power that is dissipated through the extended thermal plate.

Table 26. Thermal Specifications for S.E.C.C.2 Packaged Processors[1]

Proc. Core Freq. (MHz)	L2 Cache Size (Kbytes)	Thermal Design Power[2] (W)	L2 Cache Power (W)	Power Density[4] (W/cm^2) Up to CPUID 0683h	Power Density[4] (W/cm^2) For CPUID 0686h[6]	Max $T_{JUNCTION}$ (°C)	$T_{JUNCTION}$ Offset[3] (°C)	L2 Cache Min T_{CASE} (°C)	L2 Cache Max T_{CASE} (°C)	Min T_{COVER} (°C)	Max T_{COVER} (°C)
450	512	25.3	1.26	21.6[5]	n/a	90	4.8	5	105	5	75
500	512	28.0	1.33	23.9[5]	n/a	90	4.8	5	105	5	75
533B	512	29.7	1.37	25.4[5]	n/a	90	4.8	5	105	5	75
533EB	256	14.0	N/A	19.3[6]	22.0	82	2.0[7]	N/A	N/A	5	75
550	512	30.8	1.37	26.3[5]	n/a	80	4.8	5	105	5	75
550E	256	14.5	N/A	20.0[6]	22.8	82	2.1[7]	N/A	N/A	5	75
600	512	34.5	1.60	29.5[5]	n/a	85	4.8	5	105	5	75
600B	512	34.5	1.60	29.5[5]	n/a	85	4.8	5	105	5	75
600E	256	15.8	N/A	21.8[6]	24.8	82	2.3[7]	N/A	N/A	5	75
600EB	256	15.8	N/A	21.8[6]	24.8	82	2.3[7]	N/A	N/A	5	75
650	256	17.0	N/A	23.4[6]	26.7	82	2.5[7]	N/A	N/A	5	75
667	256	17.5	N/A	24.1[6]	27.5	82	2.5[7]	N/A	N/A	5	75
700	256	18.3	N/A	25.2[6]	28.7	80	2.7[7]	N/A	N/A	5	75
733	256	19.1	N/A	26.3[6]	30.0	80	2.8[7]	N/A	N/A	5	75
750	256	19.5	N/A	26.9[6]	30.6	80	2.8[7]	N/A	N/A	5	75
800	256	20.8	N/A	28.7[6]	32.6	80	3.0[7]	N/A	N/A	5	75
800EB	256	20.8	N/A	28.7[6]	32.6	80	3.0[7]	N/A	N/A	5	75
850	256	22.5	N/A	31.0[6]	35.2	80	3.3[7]	N/A	N/A	5	75
866	256	22.9	N/A	31.5[6]	35.9	80	3.3[7]	N/A	N/A	5	75
933	256	25.5	N/A	35.1[6]	39.9	75	3.7	N/A	N/A	5	75
1.0 GHz[8]	256	33	N/A	45.5[6]	n/a	60	4.7[7,8]	N/A	N/A	5	75
1.0 GHz	256	26.1	N/A	35.9[6]	40.9	70	3.8[7]	N/A	N/A	5	70
1.0B GHz	256	26.1	N/A	35.9[6]	40.9	70	3.8[7]	N/A	N/A	5	70

NOTES:

1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor core and nominal $V_{CC_{L2}}/V_{CC_{3.3}}$ for the L2 cache (if applicable).
2. Thermal Design Power (TDP) represents the maximum amount of power the thermal solution is required to dissipate. The thermal solution should be designed to dissipate the TDP without exceeding the maximum $T_{JUNCTION}$ specification. TDP does not represent the power delivery and voltage regulation requirements for the processor.
3. $T_{JUNCTIONOFFSET}$ is the worst-case difference between the thermal reading from the on-die thermal diode and the hottest location on the processor's core.
4. Power density is the maximum power the processor die can dissipate (i.e., processor power) divided by the die area over which the power is generated.
5. Power for these processors is generated over the entire processor die (see Figure 41 for processor die dimensions).
6. Power for these processors is generated over the core area (see Figure 20 for processor die and core area dimensions). Thermal solution designs should compensate for this smaller heat flux area (core) and not assume that the power is uniformly distributed across the entire die area (core + cache).
7. $T_{JUNCTION}$ offset values do not include any thermal diode kit measurement error. Diode kit measurement error must be added to the $T_{JUNCTION}$ offset value from the table, as outlined in the *Intel® Pentium® III processor Thermal Metrology for CPUID-068h Family Processors*. Intel has characterized the use of the Analog Devices AD1021 diode measurement kit and found its measurement error to be 1 °C.
8. This specification applies to the Pentium III processor with CPUID=0683h operating at 1.0 GHz.
9. These values are estimates based on preliminary simulation.

Figure 20. Processor Functional Die Layout (CPUID=0686h)

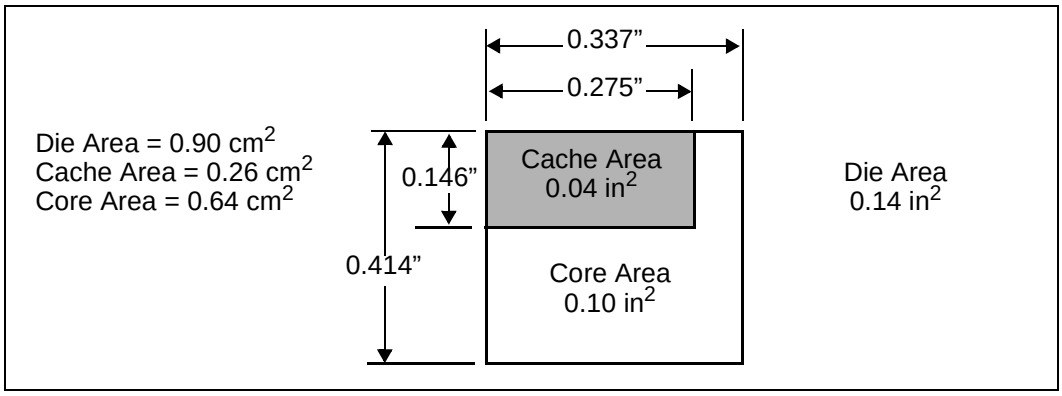
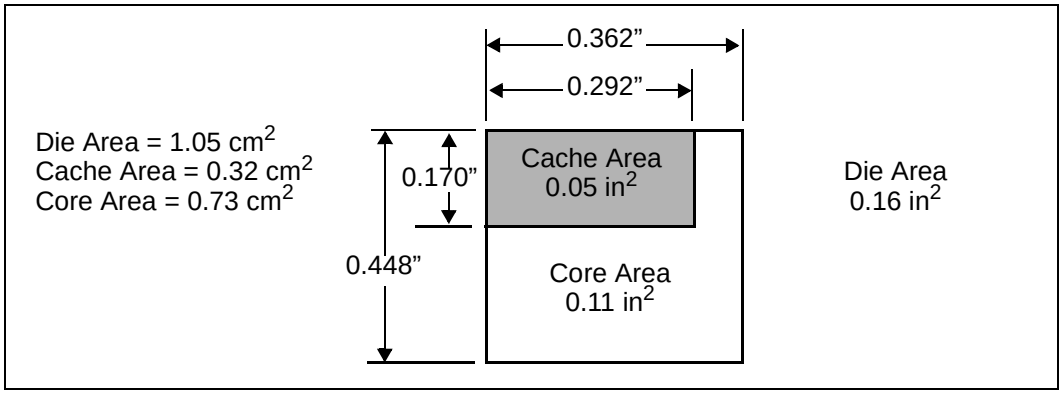


Figure 21. Processor Functional Die Layout (up to CPUID=0683h)



For S.E.C.C. packaged processors, the extended thermal plate is the attach location for all thermal solutions. The maximum and minimum extended thermal plate temperatures are specified in Table 25. For S.E.C.C.2 packaged processors, thermal solutions attach to the processor by connecting through the substrate to the cover. The maximum and minimum temperatures of the pertinent locations are specified in Table 26. A thermal solution should be designed to ensure the temperature of the specified locations never exceeds these temperatures.

The total processor power is a result of heat dissipated by the processor core and L2 cache. The overall system chassis thermal design must comprehend the entire processor power. In S.E.C.C. packaged processors, the extended thermal plate power is a component of this power, and is primarily composed of the processor core and the L2 cache dissipating heat through the extended thermal plate. The heatsink need only be designed to dissipate the extended thermal plate power. See Table 25 for current Pentium III processor S.E.C.C. thermal design specifications.

No extended thermal plate exists for S.E.C.C.2 packaged processors, so thermal solutions have to attach directly to the processor core package. The total processor power dissipated by an S.E.C.C.2 processor is a combination of heat dissipated by both the processor core and L2 cache. Pentium III processors that use a “Discrete” L2 cache have a separate T_{CASE} specification (Table 26) for the surface mounted BSRAM components on the substrate. $T_{JUNCTION}$ encompasses the L2 cache for processors that utilize the “Advanced Transfer Cache”, therefore no separate cache measurement is required.

Specifics on how to measure these specifications are outlined in AP-905, *Intel® Pentium® III Processor Thermal Design Guidelines* (Document Number 245087).

4.1.1 Thermal Diode

The Pentium III processor incorporates an on-die diode that may be used to monitor the die temperature (junction temperature). A thermal sensor located on the baseboard, or a stand-alone measurement kit, may monitor the die temperature of the Pentium III processor for thermal management or instrumentation purposes. Table 27 and Table 28 provide the diode parameter and interface specifications.

Table 27. Thermal Diode Parameters

Symbol	Min	Typ	Max	Unit	Notes[1]
$I_{forward\ bias}$	5		500	µA	
n_ideality	1.0000 1.0057	1.0065 1.0080	1.0173 1.0125		2, 3, 4 2, 3, 5

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. At room temperature with a forward bias of 630 mV.
3. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I=Io(e (Vd*q)/(nkT) – 1).
4. This specification applies to the Pentium III processor with CPUID=067xh.
5. This specification applies to the Pentium III processor with CPUID=068xh.

Table 28. Thermal Diode Interface

Pin Name	SC 242 Connector Signal #	Pin Description
THERMDP	B14	diode anode (p_junction)
THERMDN	B15	diode cathode (n_junction)

5.0 S.E.C.C. and S.E.C.C.2 Mechanical Specifications

Pentium III processors use either S.E.C.C. or S.E.C.C.2 package technology. Both package types contain the processor core, L2 cache, and other passive components. The cartridges connect to the baseboard through an edge connector. Mechanical specifications for the processor are given in this section. See Section 1.1.1 for a complete terminology listing.

5.1 S.E.C.C. Mechanical Specifications

S.E.C.C. package drawings and dimension details are provided in Figure 22 through Figure 31. Figure 22 shows multiple views of the Pentium III processor in an S.E.C.C. package; Figure 23 through Figure 26 show the package dimensions; Figure 27 and Figure 28 show the extended thermal plate dimensions; and Figure 29 and Figure 30 provide details of the processor substrate edge finger contacts. Figure 31 and Table 29 contain processor marking information. See Section 5.2 for S.E.C.C.2 mechanical specifications.

The processor edge connector defined in this document is referred to as the "SC242 connector." See the *Slot 1 Connector Specification* (Document Number 243397) for further details on the SC242 connector.

Note: For Figure 22 through Figure 44, the following apply:

1. Unless otherwise specified, the following drawings are dimensioned in inches.
2. All dimensions provided with tolerances are guaranteed to be met for all normal production product.
3. Figures and drawings labeled as "Reference Dimensions" are provided for informational purposes only. Reference Dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference Dimensions are NOT checked as part of the processor manufacturing. Unless noted as such, dimensions in parentheses without tolerances are Reference Dimensions.
4. Drawings are not to scale.

Figure 22. S.E.C.C. Packaged Processor — Multiple Views

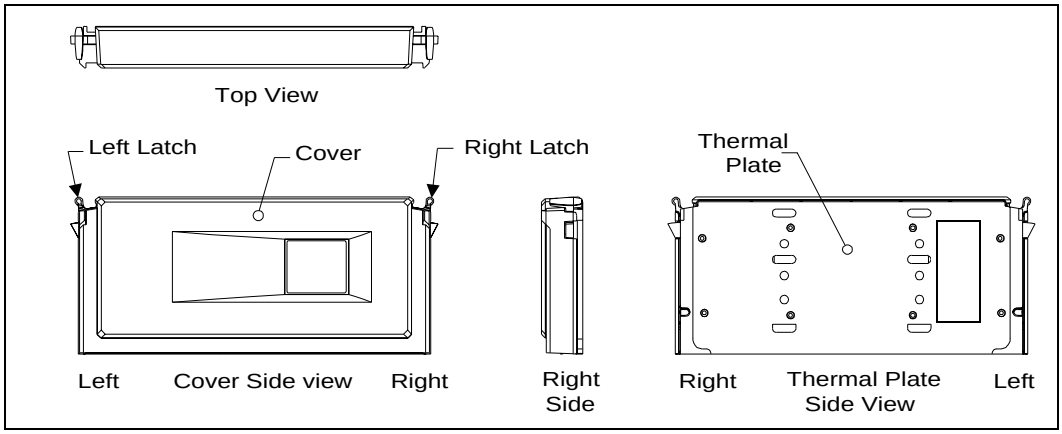


Figure 23. S.E.C.C. Packaged Processor — Extended Thermal Plate Side Dimensions

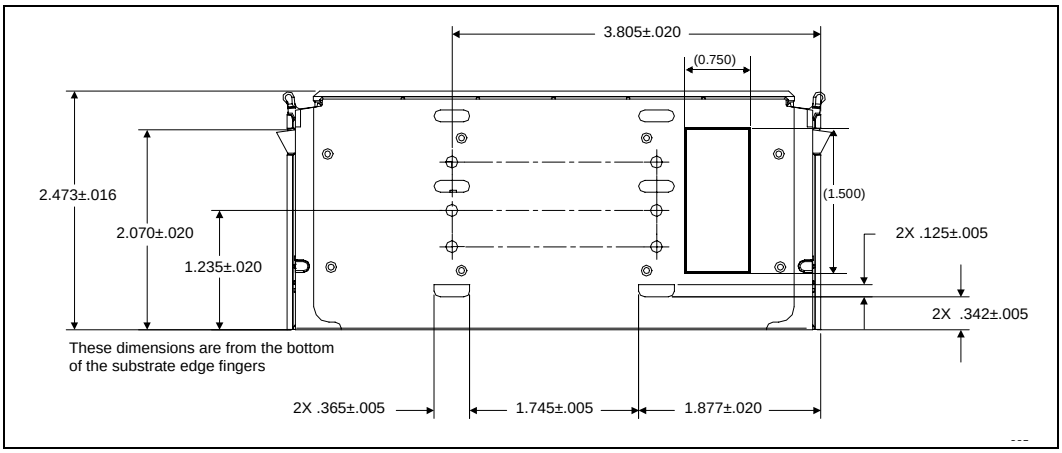


Figure 24. S.E.C.C. Packaged Processor — Bottom View Dimensions

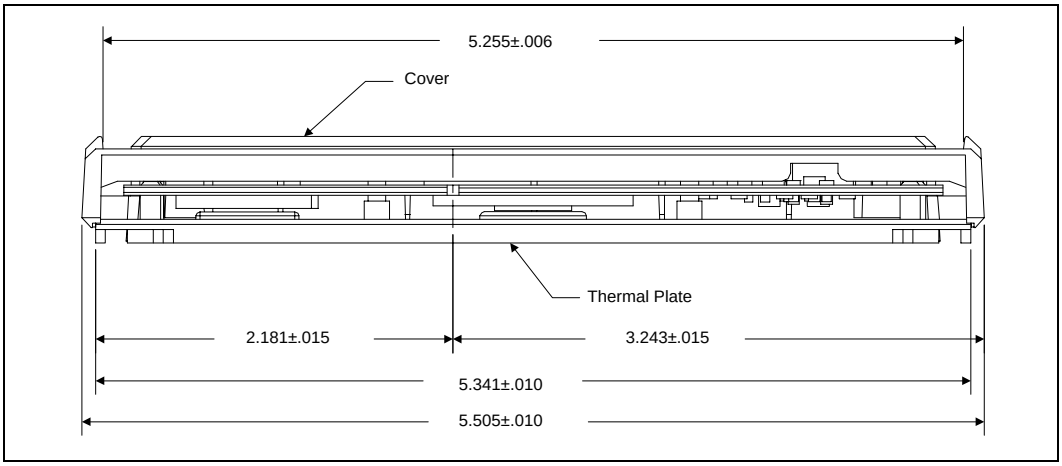


Figure 25. S.E.C.C. Packaged Processor — Latch Arm, Extended Thermal Plate Lug, and Cover Lug Dimensions

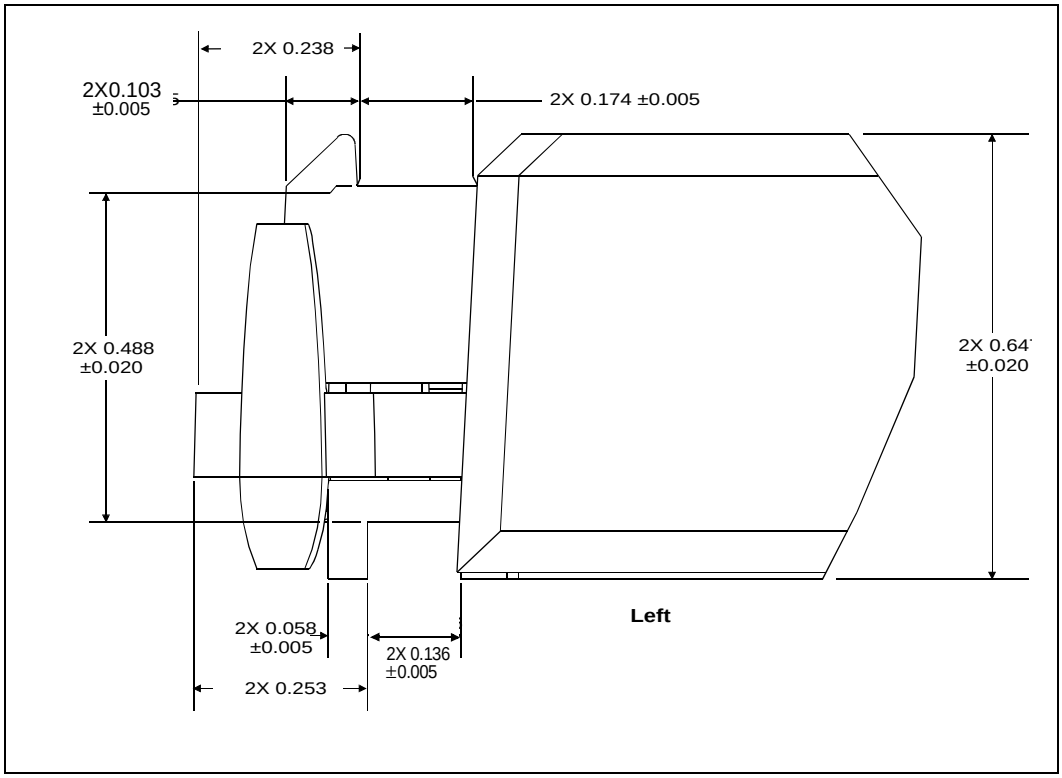


Figure 26. S.E.C.C. Packaged Processor — Latch Arm, Extended Thermal Plate, and Cover Detail Dimensions (Reference Dimensions Only)

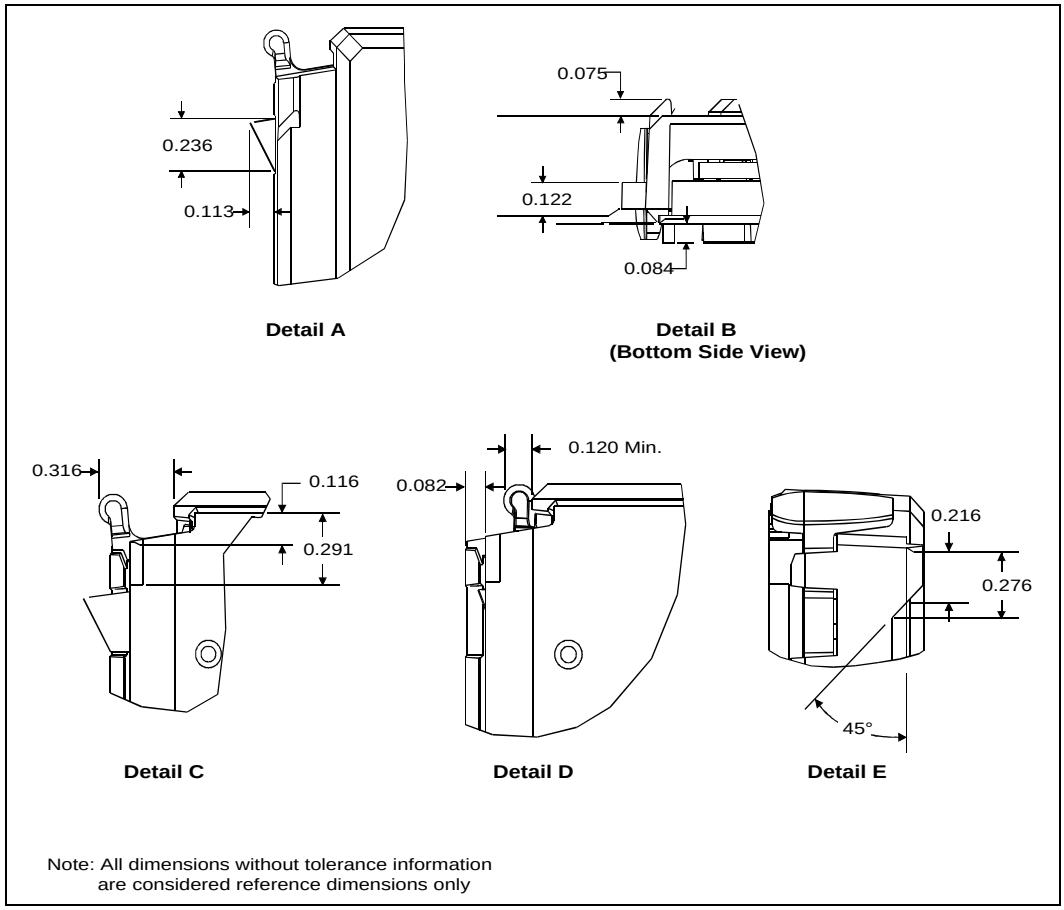


Figure 27. S.E.C.C. Packaged Processor — Extended Thermal Plate Attachment Detail Dimensions

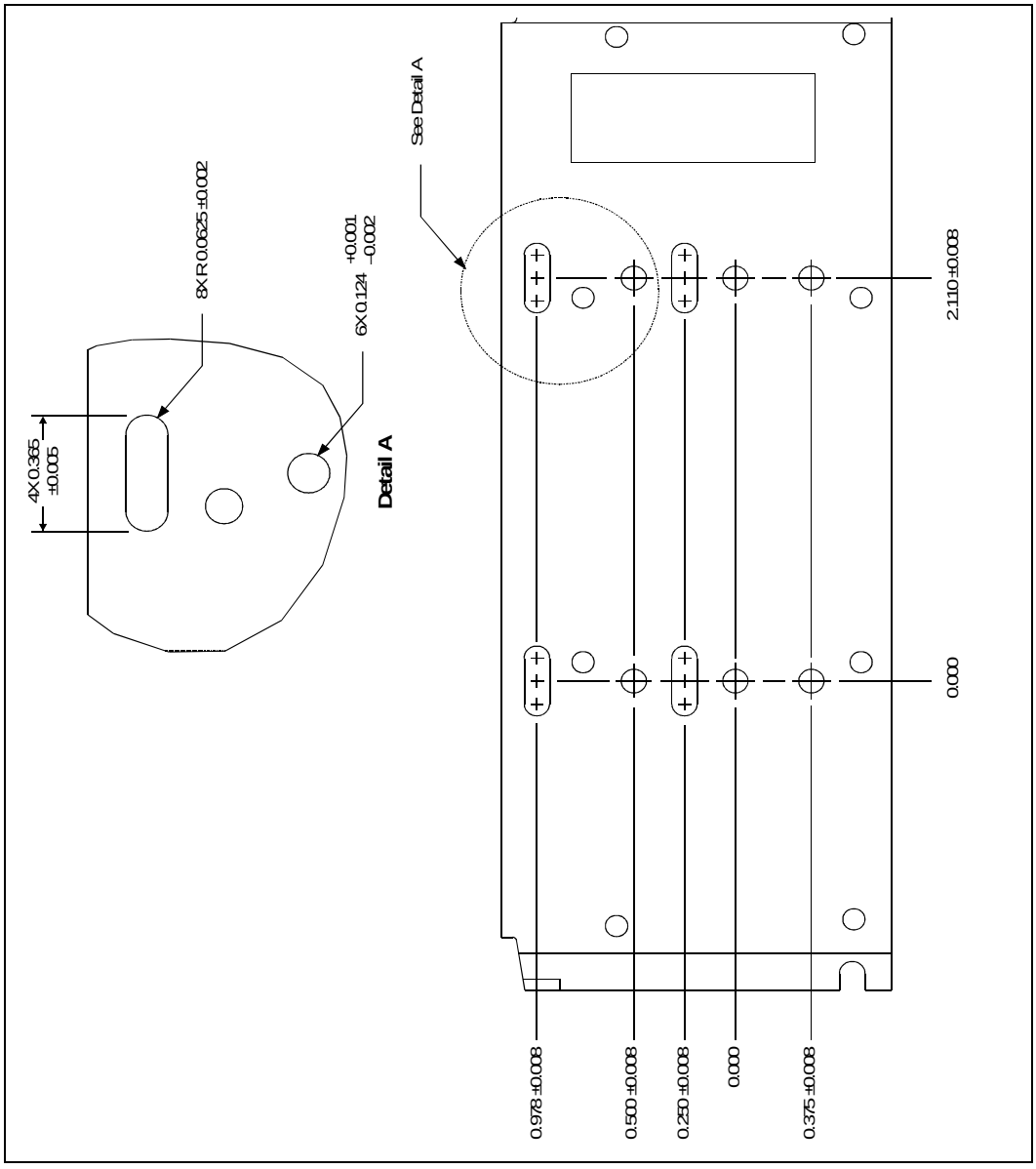


Figure 28. S.E.C.C. Packaged Processor — Extended Thermal Plate Attachment Detail Dimensions, Continued

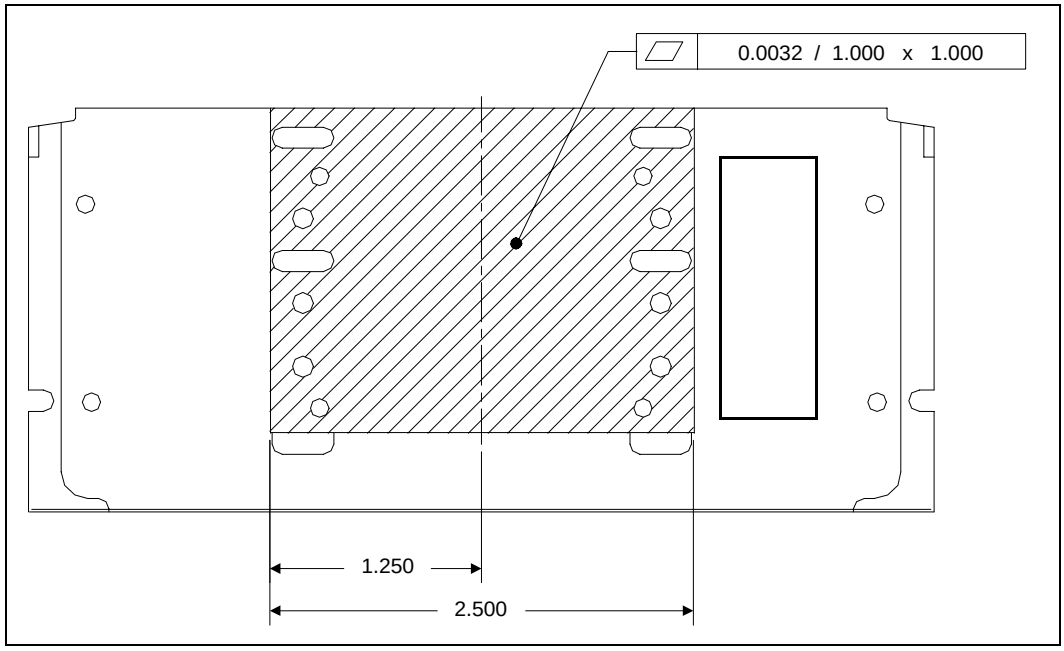


Figure 29. S.E.C.C. Packaged Processor Substrate — Edge Finger Contact Dimensions

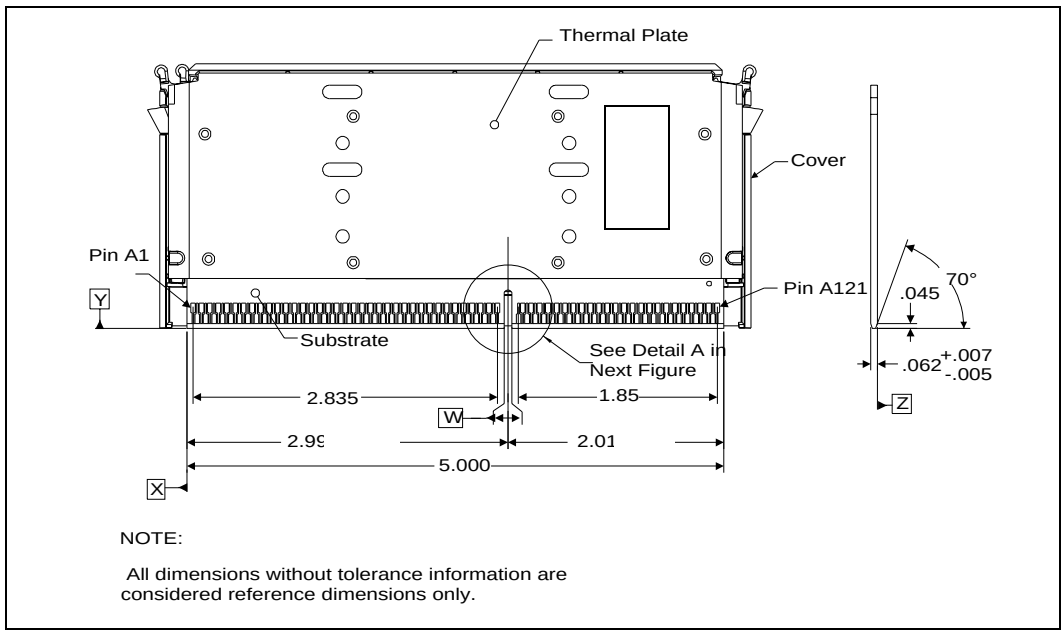


Figure 30. S.E.C.C. Packaged Processor Substrate — Edge Finger Contact Dimensions, Detail A

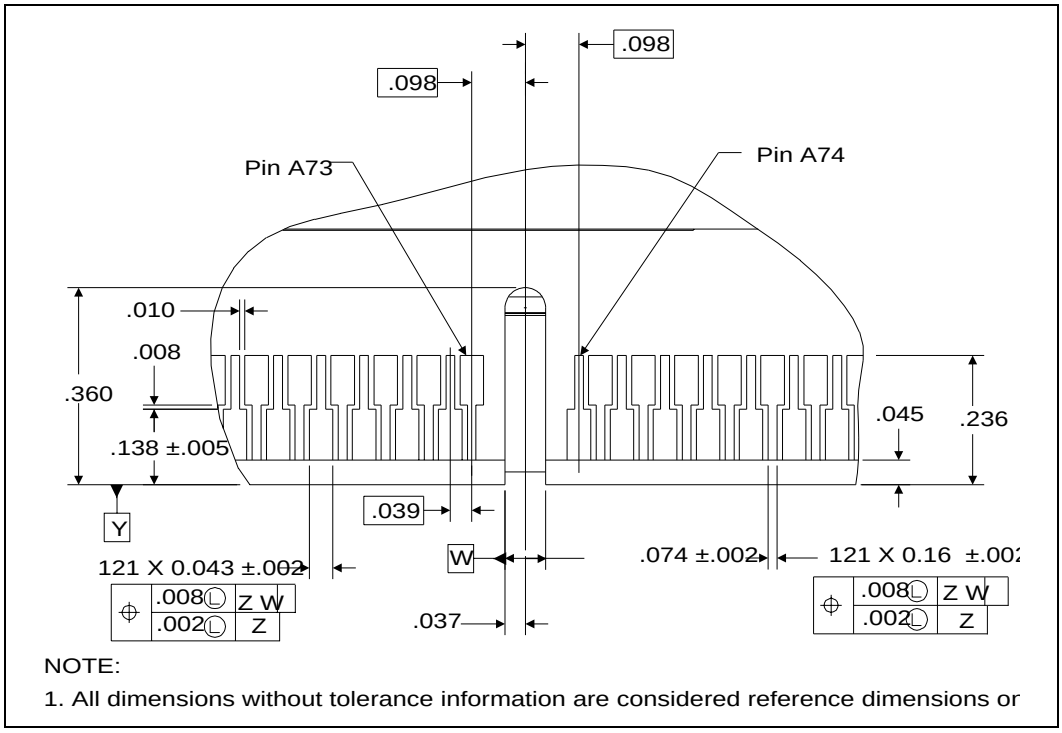


Figure 31. Intel® Pentium® III Processor Markings (S.E.C.C. Packaged Processor)

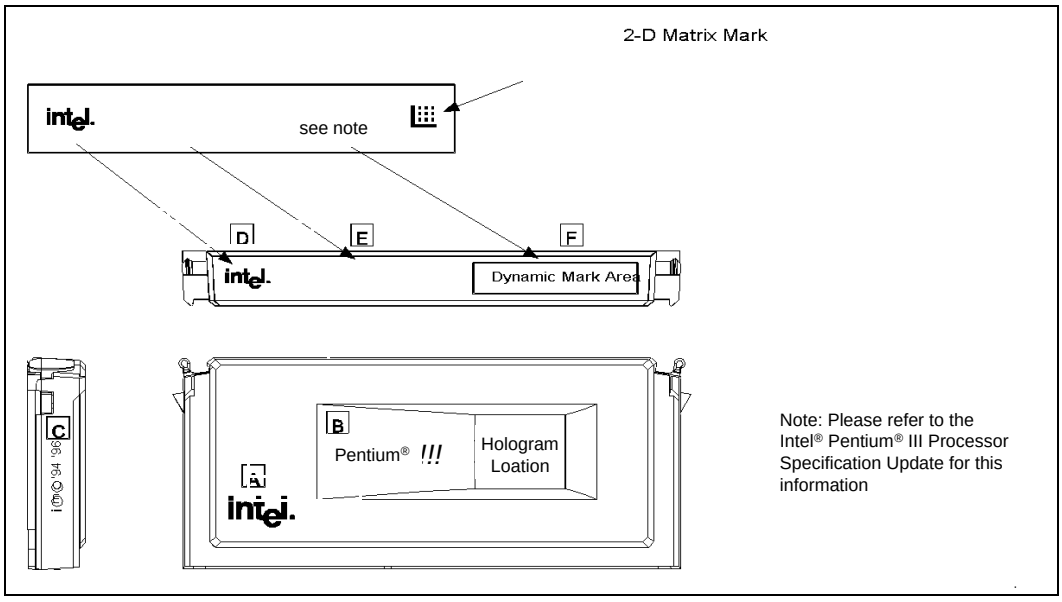


Table 29. Description Table for Processor Markings (S.E.C.C. Packaged Processor)

Code Letter	Description
A	Logo
C	Trademark
D	Logo
E	Product Name
F	Dynamic Mark Area – with 2-D matrix

5.2 S.E.C.C.2 Mechanical Specification

S.E.C.C.2 drawings and dimension details are provided in Figure 32 through Figure 44. Figure 32 shows multiple views of the Pentium III processor in an S.E.C.C.2 package; Figure 33 through Figure 37 show an S.E.C.C.2 package dimensions; Figure 38 and Figure 39 provide dimensions of the processor substrate edge finger contacts; Figure 40 shows the heatsink solution keep-in zone; Figure 42 shows multiple views of an S.E.C.C.2 packaged processor keep-out zone; and Figure 44 and Table 40 contain processor marking information. See Section 5.1 for S.E.C.C. Mechanical Specifications.

Figure 32. S.E.C.C.2 Packaged Processor — Multiple Views

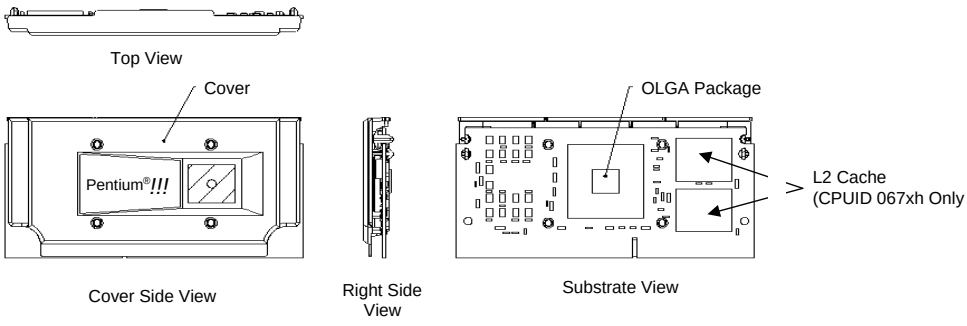


Figure 33. S.E.C.C.2 Packaged Processor Assembly — Primary View

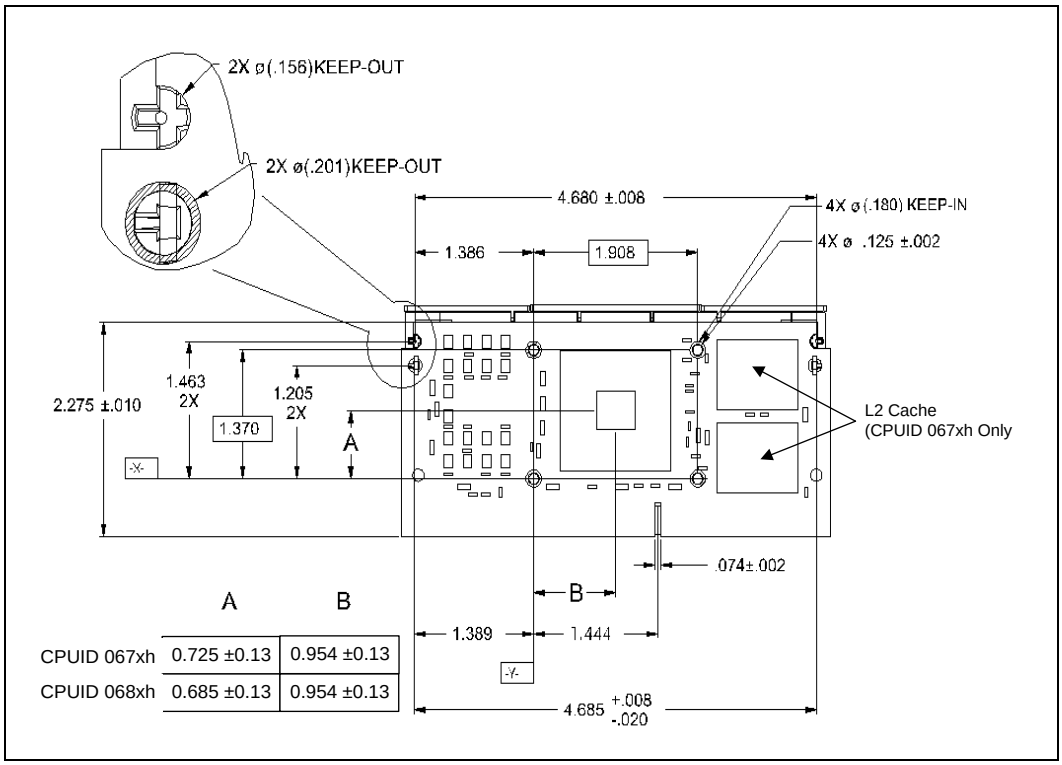


Figure 34. S.E.C.C.2 Packaged Processor Assembly — Cover View with Dimensions

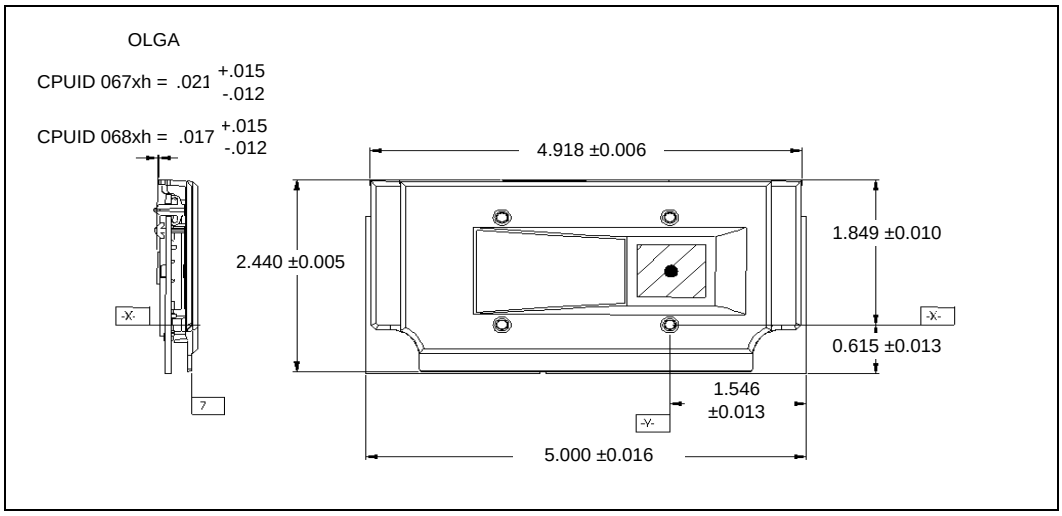


Figure 35. S.E.C.C.2 Packaged Processor Assembly — Heatsink Attach Boss Section

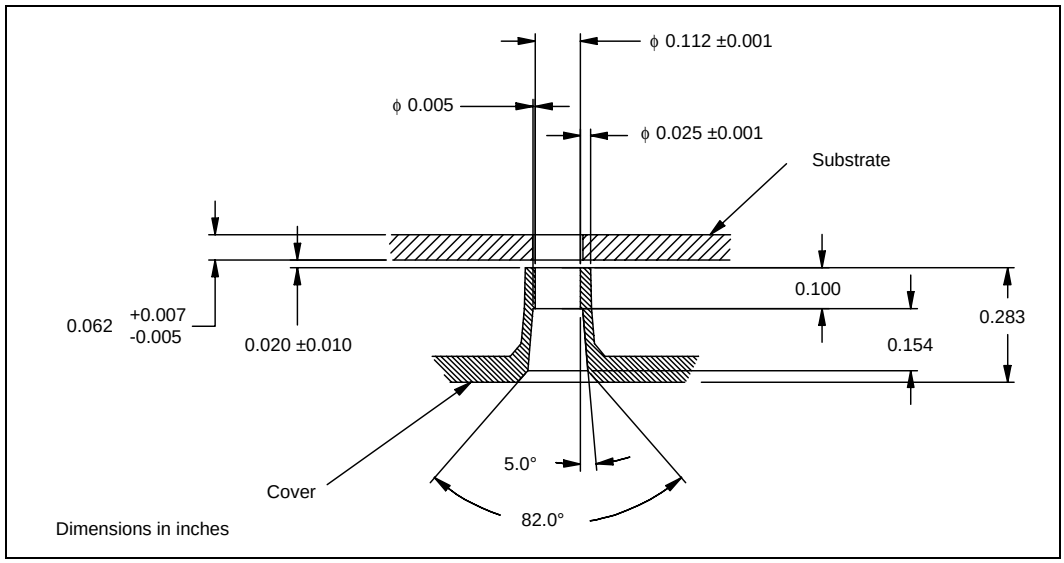


Figure 36. S.E.C.C.2 Packaged Processor Assembly — Side View

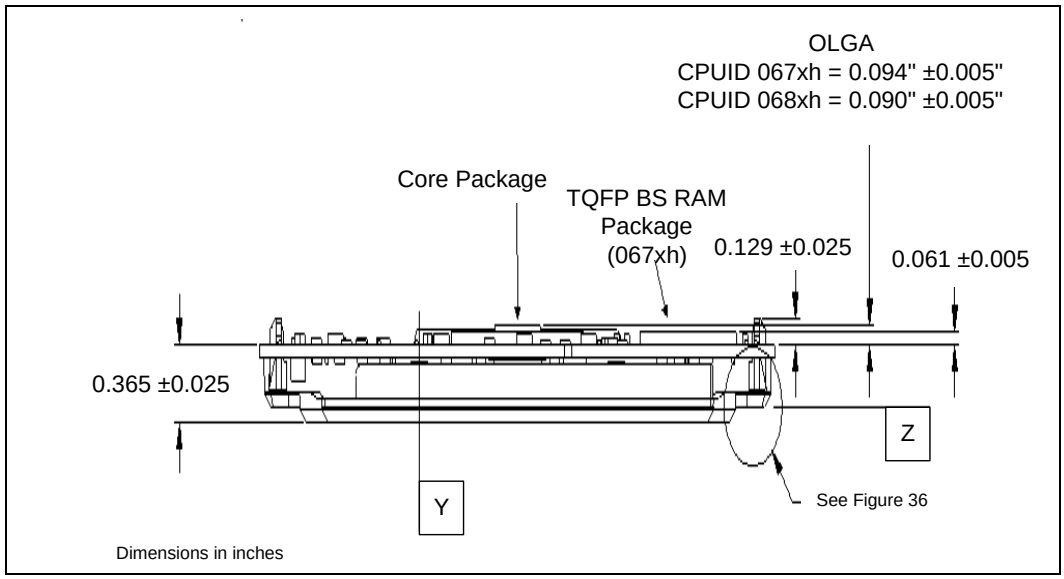


Figure 37. Detail View of Cover in the Vicinity of the Substrate Attach Features

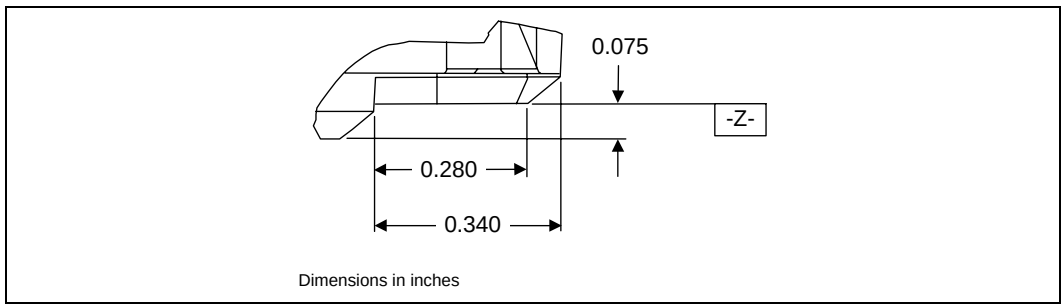


Figure 38. S.E.C.C.2 Packaged Processor Substrate — Edge Finger Contact Dimensions

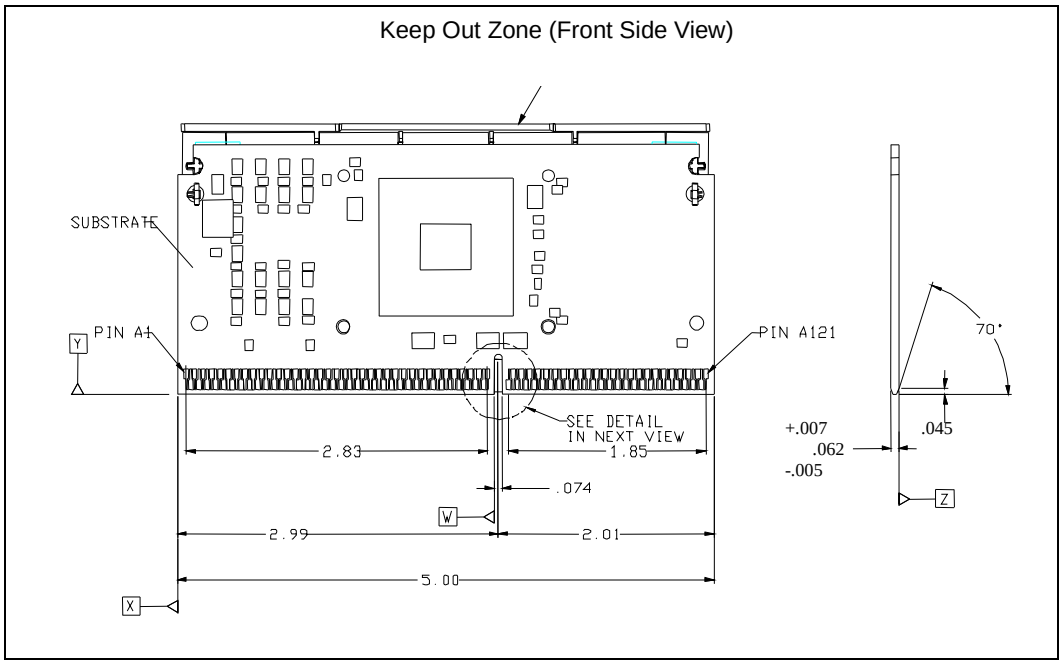


Figure 39. S.E.C.C.2 Packaged Processor Substrate — Edge Finger Contact Dimensions (Detail A)

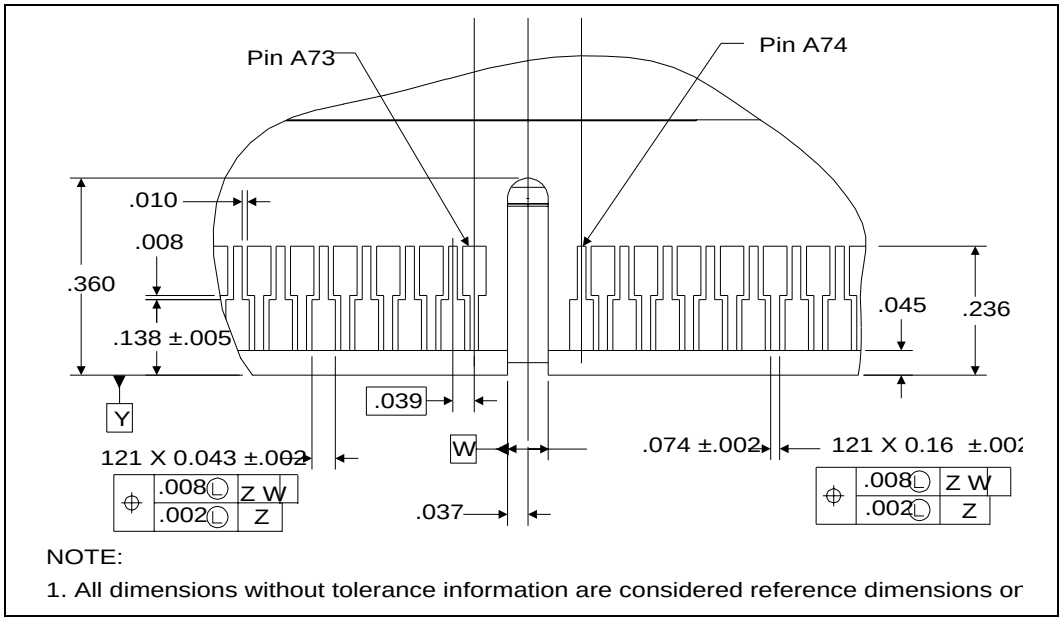


Figure 40. S.E.C.C.2 Packaged Processor Substrate (CPUID=067xh) — Keep-In Zones

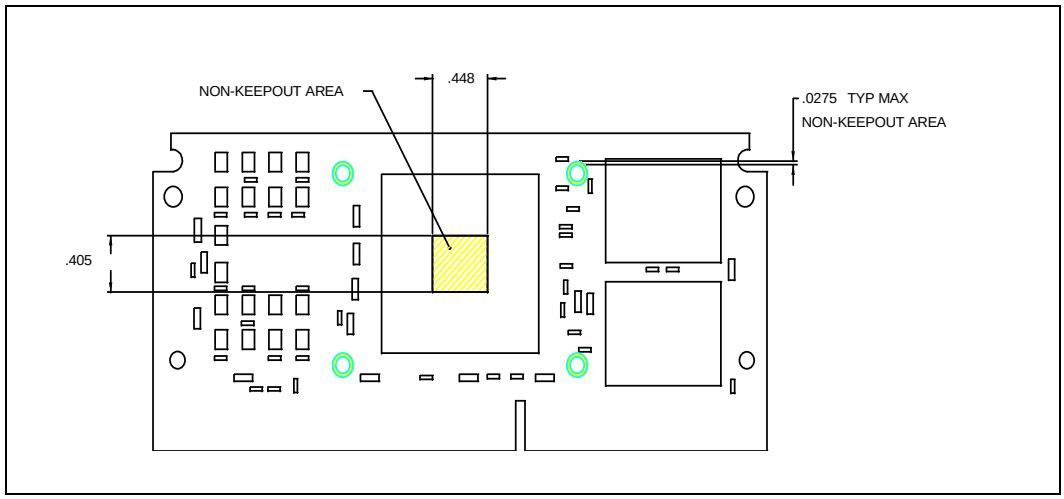


Figure 41. S.E.C.C.2 Packaged Processor Substrate (CPUID=068xh) — Keep-In Zones

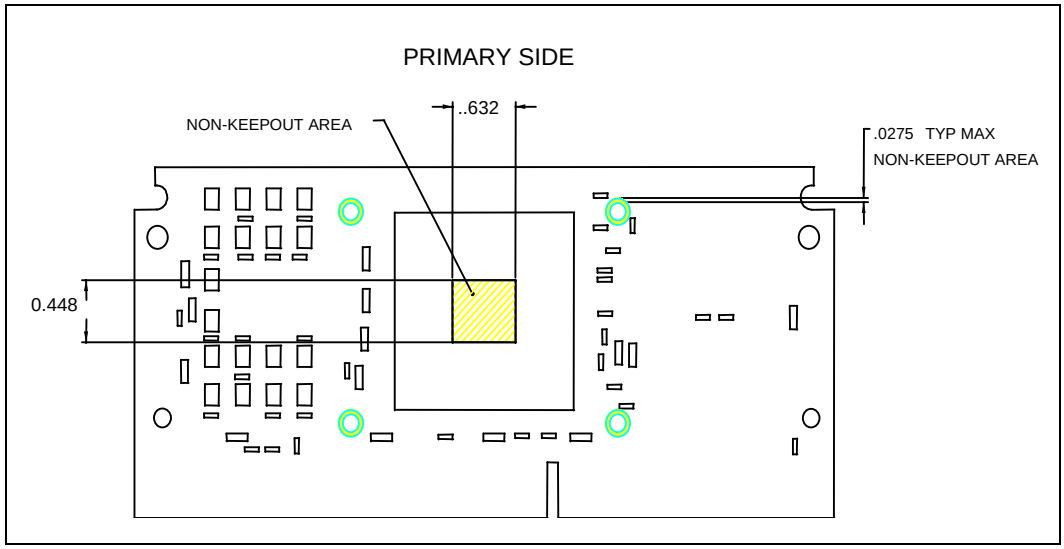


Figure 42. S.E.C.C.2 Packaged Processor Substrate (CPUID=067xh) — Keep-Out Zone

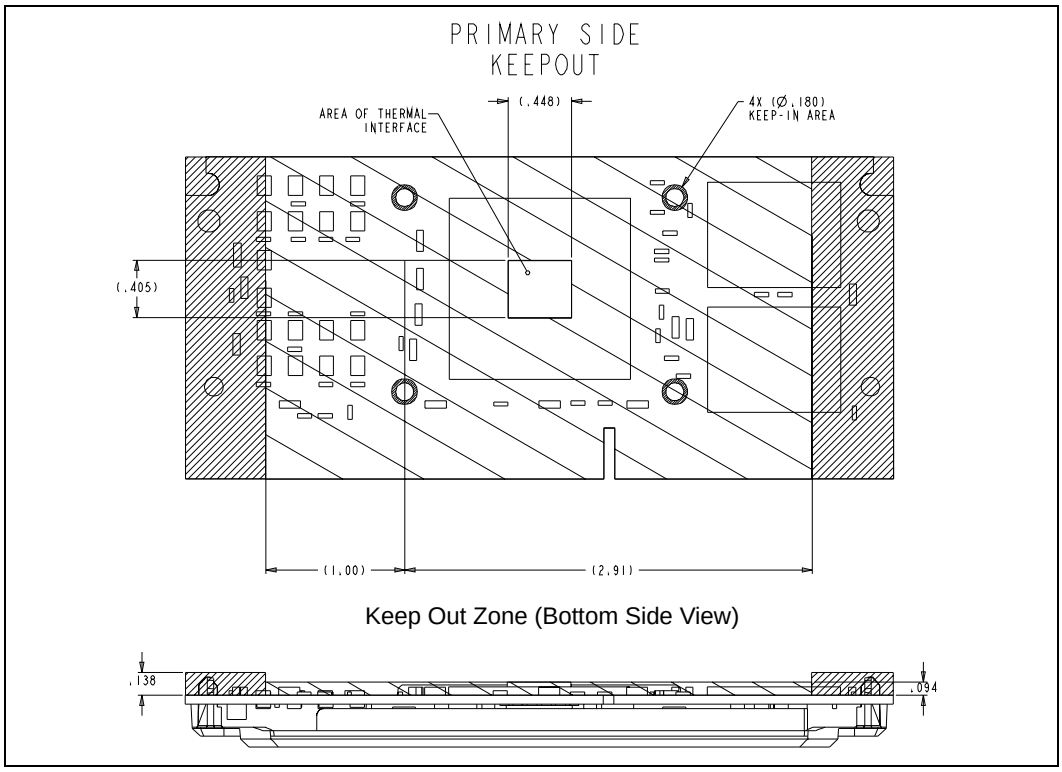


Figure 43. S.E.C.C.2 Packaged Processor Substrate (CPUID=068xh) — Keep-Out Zone

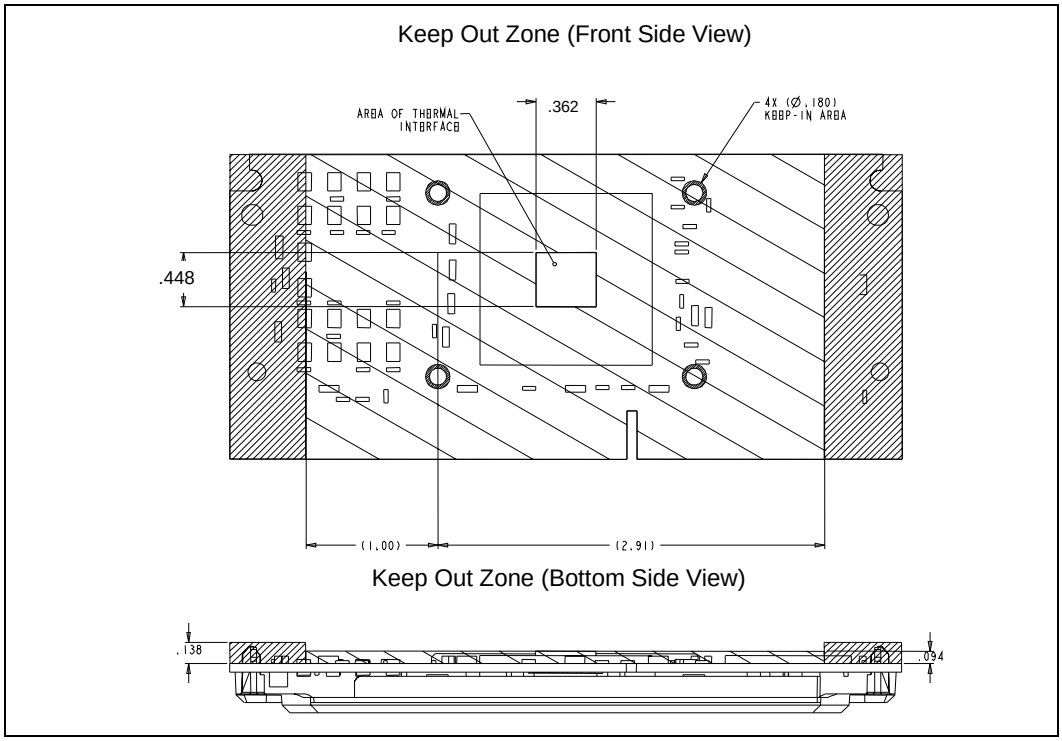


Figure 44. Intel® Pentium® III Processor Markings (S.E.C.C.2 Package)

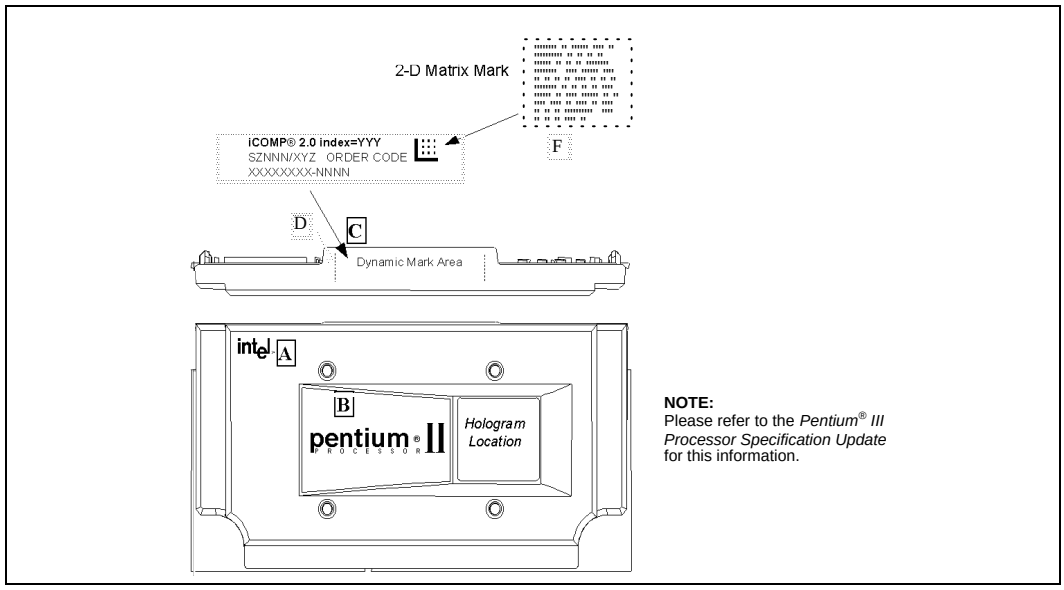


Table 30. Description Table for Processor Markings (S.E.C.C.2 Packaged Processor)

Code Letter	Description
A	Logo
C	Trademark
D	Logo
F	Dynamic Mark Area – with 2-D matrix

5.3 S.E.C.C.2 Structural Mechanical Specification

The intention of the structural specification for S.E.C.C.2 is to ensure that the package will not be exposed to excessive stresses that could adversely affect device reliability. Figure 45 illustrates the deflection specification for deflections away from the heatsink. Figure 46 illustrates the deflection specification in the direction of the heatsink.

The heatsink attach solution must not induce permanent stress into the S.E.C.C.2 substrate with the exception of a uniform load to maintain the heatsink to the processor thermal interface. Figure 47 and Table 31 define the pressure specification.

Figure 45. Substrate Deflection away from Heatsink

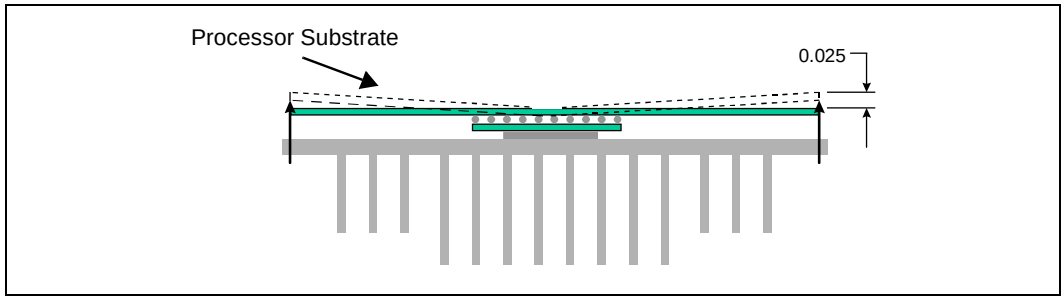


Figure 46. Substrate Deflection toward the Heatsink

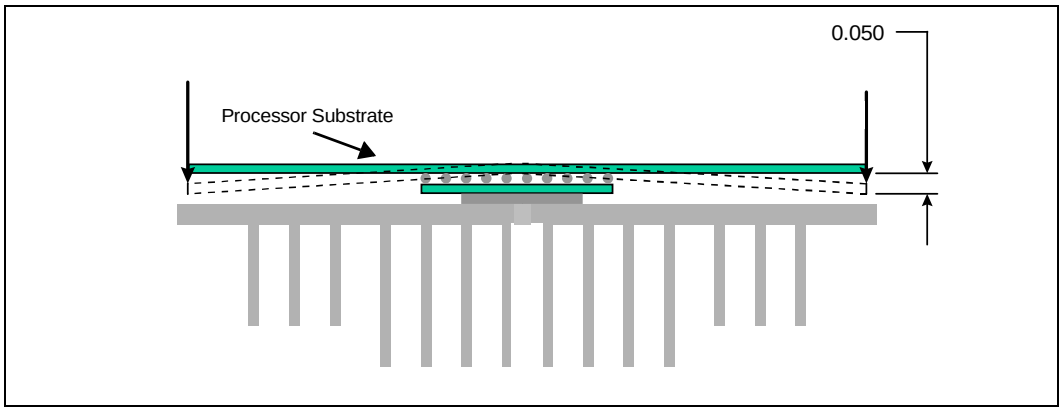


Figure 47. S.E.C.C.2 Packaged Processor Specifications

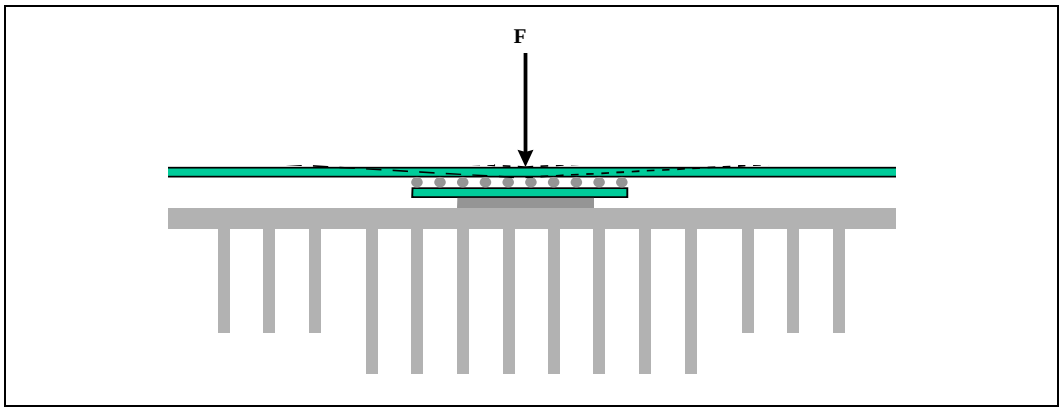


Table 31. S.E.C.C.2 Pressure Specifications

Parameter	Maximum	Unit	Figure	Notes
Static Compressive Force	50	lbf	47	1
Transient Compressive Force	100 75	lbf lbf	47 47	2 3

NOTES:
1. This is the maximum static force that can be applied by the heatsink to maintain the heatsink and processor interface.
2. This specification applies to a uniform load.
3. This specification applies to a nonuniform load.

5.4 Processor Package Materials Information

Both the S.E.C.C. and S.E.C.C.2 processor packages are comprised of multiple pieces to make the complete assembly. This section provides the weight of each piece and the entire package. Table 32 and Table 33 contain piece-part information of the S.E.C.C. and S.E.C.C.2 processor packages, respectively.

Table 32. S.E.C.C. Materials

S.E.C.C. Piece	Piece Material	Maximum Piece Weight (Grams)
Extended Thermal Plate	Aluminum 6063-T6	84.0
Latch Arms	GE Lexan 940-V0, 30% glass filled	Less than 2.0 per latch arm
Cover	GE Lexan 940-V0	24.0
Total Pentium III Processor		112.0

Table 33. S.E.C.C.2 Materials

S.E.C.C.2 Piece	Piece Material	Maximum Piece Weight (Grams)
Cover	GE Lexan 940-V0	18.0
Total Pentium III Processor		54.0

5.5 Intel® Pentium® III Processor Signal Listing

Table 34 and Table 35 provide the processor edge finger signal definitions. The signal locations on the SC242 edge connector are to be used for signal routing, simulation, and component placement on the baseboard.

Table 34 is the Pentium III processor substrate edge finger listing in order by pin number. Table 35 is the Pentium III processor substrate edge connector listing in order by signal name.

Table 34. Signal Listing in Order by Pin Number

Pin #	Pin Name	Signal Group
A1	VTT	Power/Other
A2	GND	Power/Other
A3	VTT	Power/Other
A4	IERR#	CMOS Output
A5	A20M#	CMOS Input
A6	GND	Power/Other
A7	FERR#	CMOS Output
A8	IGNNE#	CMOS Input
A9	TDI	TAP Input
A10	GND	Power/Other
A11	TDO	TAP Output
A12	PWRGOOD	CMOS Input
A13	TESTHI	Power/Other
A14	BSEL1	Power/Other
A15	THERMTRIP#	CMOS Output
A16	Reserved	Power/Other
A17	LINT0/INTR	CMOS Input
A18	GND	Power/Other
A19	PICD0	APIC I/O
A20	PREQ#	CMOS Input
A21	BP3#	AGTL+ I/O
A22	GND	Power/Other
A23	BPM0#	AGTL+ I/O
A24	BINIT#	AGTL+ I/O
A25	DEP0#	AGTL+ I/O
A26	GND	Power/Other
A27	DEP1#	AGTL+ I/O
A28	DEP3#	AGTL+ I/O
A29	DEP5#	AGTL+ I/O
A30	GND	Power/Other
A31	DEP6#	AGTL+ I/O
A32	D61#	AGTL+ I/O
A33	D55#	AGTL+ I/O
A34	GND	Power/Other
A35	D60#	AGTL+ I/O
A36	D53#	AGTL+ I/O
A37	D57#	AGTL+ I/O
A38	GND	Power/Other
A39	D46#	AGTL+ I/O
A40	D49#	AGTL+ I/O
A41	D51#	AGTL+ I/O

Pin #	Pin Name	Signal Group
B1	EMI	Power/Other
B2	FLUSH#	CMOS Input
B3	SMI#	CMOS Input
B4	INIT#	CMOS Input
B5	VTT	Power/Other
B6	STPCLK#	CMOS Input
B7	TCK	TAP Input
B8	SLP#	CMOS Input
B9	VTT	Power/Other
B10	TMS	TAP Input
B11	TRST#	TAP Input
B12	Reserved	Power/Other
B13	VCC_{CORE}	Power/Other
B14	THERMDP	Power/Other
B15	THERMDN	Power/Other
B16	LINT1/NMI	CMOS Input
B17	VCC_{CORE}	Power/Other
B18	PICCLK	APIC Clock
B19	BP2#	AGTL+ I/O
B20	Reserved	Power/Other
B21	BSEL0	Power/Other
B22	PICD1	APIC I/O
B23	PRDY#	AGTL+ Output
B24	BPM1#	AGTL+ I/O
B25	VCC_{CORE}	Power/Other
B26	DEP2#	AGTL+ I/O
B27	DEP4#	AGTL+ I/O
B28	DEP7#	AGTL+ I/O
B29	VCC_{CORE}	Power/Other
B30	D62#	AGTL+ I/O
B31	D58#	AGTL+ I/O
B32	D63#	AGTL+ I/O
B33	VCC_{CORE}	Power/Other
B34	D56#	AGTL+ I/O
B35	D50#	AGTL+ I/O
B36	D54#	AGTL+ I/O
B37	VCC_{CORE}	Power/Other
B38	D59#	AGTL+ I/O
B39	D48#	AGTL+ I/O
B40	D52#	AGTL+ I/O
B41	EMI	Power/Other

Table 34. Signal Listing in Order by Pin Number (Continued)

Pin #	Pin Name	Signal Group
A42	GND	Power/Other
A43	D42#	AGTL+ I/O
A44	D45#	AGTL+ I/O
A45	D39#	AGTL+ I/O
A46	GND	Power/Other
A47	Reserved	Power/Other
A48	D43#	AGTL+I/O
A49	D37#	AGTL+ I/O
A50	GND	Power/Other
A51	D33#	AGTL+ I/O
A52	D35#	AGTL+ I/O
A53	D31#	AGTL+ I/O
A54	GND	Power/Other
A55	D30#	AGTL+ I/O
A56	D27#	AGTL+ I/O
A57	D24#	AGTL+ I/O
A58	GND	Power/Other
A59	D23#	AGTL+ I/O
A60	D21#	AGTL+ I/O
A61	D16#	AGTL+ I/O
A62	GND	Power/Other
A63	D13#	AGTL+ I/O
A64	D11#	AGTL+ I/O
A65	D10#	AGTL+ I/O
A66	GND	Power/Other
A67	D14#	AGTL+ I/O
A68	D9#	AGTL+ I/O
A69	D8#	AGTL+ I/O
A70	GND	Power/Other
A71	D5#	AGTL+ I/O
A72	D3#	AGTL+ I/O
A73	D1#	AGTL+ I/O
A74	GND	Power/Other
A75	BCLK	System Bus
A76	BR0#	AGTL+I/O
A77	BERR#	AGTL+ I/O
A78	GND	Power/Other
A79	A33#	AGTL+ I/O
A80	A34#	AGTL+ I/O
A81	A30#	AGTL+ I/O
A82	GND	Power/Other
A83	A31#	AGTL+ I/O

Pin #	Pin Name	Signal Group
B42	D41#	AGTL+ I/O
B43	D47#	AGTL+ I/O
B44	D44#	AGTL+ I/O
B45	VCC_{CORE}	Power/Other
B46	D36#	AGTL+ I/O
B47	D40#	AGTL+ I/O
B48	D34#	AGTL+ I/O
B49	VCC_{CORE}	Power/Other
B50	D38#	AGTL+ I/O
B51	D32#	AGTL+ I/O
B52	D28#	AGTL+ I/O
B53	VCC_{CORE}	Power/Other
B54	D29#	AGTL+ I/O
B55	D26#	AGTL+ I/O
B56	D25#	AGTL+ I/O
B57	VCC_{CORE}	Power/Other
B58	D22#	AGTL+ I/O
B59	D19#	AGTL+ I/O
B60	D18#	AGTL+ I/O
B61	EMI	Power/Other
B62	D20#	AGTL+ I/O
B63	D17#	AGTL+ I/O
B64	D15#	AGTL+ I/O
B65	VCC_{CORE}	Power/Other
B66	D12#	AGTL+ I/O
B67	D7#	AGTL+ I/O
B68	D6#	AGTL+ I/O
B69	VCC_{CORE}	Power/Other
B70	D4#	AGTL+ I/O
B71	D2#	AGTL+ I/O
B72	D0#	AGTL+ I/O
B73	VCC_{CORE}	Power/Other
B74	RESET#	AGTL+ Input
B75	BR1#	AGTL+ Input
B76	Reserved	Power/Other.
B77	VCC_{CORE}	Power/Other
B78	A35#	AGTL+ I/O
B79	A32#	AGTL+ I/O
B80	A29#	AGTL+ I/O
B81	EMI	Power/Other
B82	A26#	AGTL+ I/O
B83	A24#	AGTL+ I/O

Table 34. Signal Listing in Order by Pin Number (Continued)

Pin #	Pin Name	Signal Group
A84	A27#	AGTL+ I/O
A85	A22#	AGTL+ I/O
A86	GND	Power/Other
A87	A23#	AGTL+ I/O
A88	Reserved	Power/Other
A89	A19#	AGTL+ I/O
A90	GND	Power/Other
A91	A18#	AGTL+ I/O
A92	A16#	AGTL+ I/O
A93	A13#	AGTL+ I/O
A94	GND	Power/Other
A95	A14#	AGTL+ I/O
A96	A10#	AGTL+ I/O
A97	A5#	AGTL+ I/O
A98	GND	Power/Other
A99	A9#	AGTL+ I/O
A100	A4#	AGTL+ I/O
A101	BNR#	AGTL+ I/O
A102	GND	Power/Other
A103	BPRI#	AGTL+ Input
A104	TRDY#	AGTL+ Input
A105	DEFER#	AGTL+ Input
A106	GND	Power/Other
A107	REQ2#	AGTL+ I/O
A108	REQ3#	AGTL+ I/O
A109	HITM#	AGTL+ I/O
A110	GND	Power/Other
A111	DBSY#	AGTL+ I/O
A112	RS1#	AGTL+ Input
A113	Reserved	Power/Other
A114	GND	Power/Other
A115	ADS#	AGTL+ I/O
A116	Reserved	Power/Other
A117	AP0#	AGTL+ I/O
A118	GND	Power/Other
A119	VID2	Power/Other
A120	VID1	Power/Other
A121	VID4	Power/Other

Pin #	Pin Name	Signal Group
B84	A28#	AGTL+ I/O
B85	VCC_{CORE}	Power/Other
B86	A20#	AGTL+ I/O
B87	A21#	AGTL+ I/O
B88	A25#	AGTL+ I/O
B89	VCC_{CORE}	Power/Other
B90	A15#	AGTL+ I/O
B91	A17#	AGTL+ I/O
B92	A11#	AGTL+ I/O
B93	VCC_{CORE}	Power/Other
B94	A12#	AGTL+ I/O
B95	A8#	AGTL+ I/O
B96	A7#	AGTL+ I/O
B97	VCC_{CORE}	Power/Other
B98	A3#	AGTL+ I/O
B99	A6#	AGTL+ I/O
B100	EMI	Power/Other
B101	SLOTOCC#	Power/Other
B102	REQ0#	AGTL+ I/O
B103	REQ1#	AGTL+ I/O
B104	REQ4#	AGTL+ I/O
B105	VCC_{CORE}	Power/Other
B106	LOCK#	AGTL+ I/O
B107	DRDY#	AGTL+ I/O
B108	RS0#	AGTL+ Input
B109	VCC_5	Power/Other
B110	HIT#	AGTL+ I/O
B111	RS2#	AGTL+ Input
B112	Reserved	Power/Other
B113	$VCC_{L2}/VCC_{3.3}$	Power/Other
B114	RP#	AGTL+ I/O
B115	RSP#	AGTL+ Input
B116	AP1#	AGTL+ I/O
B117	$VCC_{L2}/VCC_{3.3}$	Power/Other
B118	AERR#	AGTL+ I/O
B119	VID3	Power/Other
B120	VID0	Power/Other
B121	$VCC_{L2}/VCC_{3.3}$	Power/Other

Table 35. Signal Listing in Order by Signal Name

Pin Name	Pin #	Signal Group
A3#	B98	AGTL+ I/O
A4#	A100	AGTL+ I/O
A5#	A97	AGTL+ I/O
A6#	B99	AGTL+ I/O
A7#	B96	AGTL+ I/O
A8#	B95	AGTL+ I/O
A9#	A99	AGTL+ I/O
A10#	A96	AGTL+ I/O
A11#	B92	AGTL+ I/O
A12#	B94	AGTL+ I/O
A13#	A93	AGTL+ I/O
A14#	A95	AGTL+ I/O
A15#	B90	AGTL+ I/O
A16#	A92	AGTL+ I/O
A17#	B91	AGTL+ I/O
A18#	A91	AGTL+ I/O
A19#	A89	AGTL+ I/O
A20#	B86	AGTL+ I/O
A20M#	A5	CMOS Input
A21#	B87	AGTL+ I/O
A22#	A85	AGTL+ I/O
A23#	A87	AGTL+ I/O
A24#	B83	AGTL+ I/O
A25#	B88	AGTL+ I/O
A26#	B82	AGTL+ I/O
A27#	A84	AGTL+ I/O
A28#	B84	AGTL+ I/O
A29#	B80	AGTL+ I/O
A30#	A81	AGTL+ I/O
A31#	A83	AGTL+ I/O
A32#	B79	AGTL+ I/O
A33#	A79	AGTL+ I/O
A34#	A80	AGTL+ I/O
A35#	B78	AGTL+ I/O
ADS#	A115	AGTL+ I/O
AERR#	B118	AGTL+ I/O
AP0#	A117	AGTL+ I/O
AP1#	B116	AGTL+ I/O
BCLK	A75	System Bus
BERR#	A77	AGTL+ I/O
BINIT#	A24	AGTL+ I/O

Table 35. Signal Listing in Order by Signal Name (Continued)

Pin Name	Pin #	Signal Group
BNR#	A101	AGTL+ I/O
BP2#	B19	AGTL+ I/O
BP3#	A21	AGTL+ I/O
BPM0#	A23	AGTL+ I/O
BPM1#	B24	AGTL+ I/O
BPRI#	A103	AGTL+ Input
BR0#	A76	AGTL+I/O
BR1#	B75	AGTL+ Input
BSEL0	B21	Power/Other
BSEL1	A14	Power/Other
D0#	B72	AGTL+ I/O
D1#	A73	AGTL+ I/O
D2#	B71	AGTL+ I/O
D3#	A72	AGTL+ I/O
D4#	B70	AGTL+ I/O
D5#	A71	AGTL+ I/O
D6#	B68	AGTL+ I/O
D7#	B67	AGTL+ I/O
D8#	A69	AGTL+ I/O
D9#	A68	AGTL+ I/O
D10#	A65	AGTL+ I/O
D11#	A64	AGTL+ I/O
D12#	B66	AGTL+ I/O
D13#	A63	AGTL+ I/O
D14#	A67	AGTL+ I/O
D15#	B64	AGTL+ I/O
D16#	A61	AGTL+ I/O
D17#	B63	AGTL+ I/O
D18#	B60	AGTL+ I/O
D19#	B59	AGTL+ I/O
D20#	B62	AGTL+ I/O
D21#	A60	AGTL+ I/O
D22#	B58	AGTL+ I/O
D23#	A59	AGTL+ I/O
D24#	A57	AGTL+ I/O
D25#	B56	AGTL+ I/O
D26#	B55	AGTL+ I/O
D27#	A56	AGTL+ I/O
D28#	B52	AGTL+ I/O
D29#	B54	AGTL+ I/O
D30#	A55	AGTL+ I/O

Table 35. Signal Listing in Order by Signal Name (Continued)

Pin Name	Pin #	Signal Group
D31#	A53	AGTL+ I/O
D32#	B51	AGTL+ I/O
D33#	A51	AGTL+ I/O
D34#	B48	AGTL+ I/O
D35#	A52	AGTL+ I/O
D36#	B46	AGTL+ I/O
D37#	A49	AGTL+ I/O
D38#	B50	AGTL+ I/O
D39#	A45	AGTL+ I/O
D40#	B47	AGTL+ I/O
D41#	B42	AGTL+ I/O
D42#	A43	AGTL+ I/O
D43#	A48	AGTL+I/O
D44#	B44	AGTL+ I/O
D45#	A44	AGTL+ I/O
D46#	A39	AGTL+ I/O
D47#	B43	AGTL+ I/O
D48#	B39	AGTL+ I/O
D49#	A40	AGTL+ I/O
D50#	B35	AGTL+ I/O
D51#	A41	AGTL+ I/O
D52#	B40	AGTL+ I/O
D53#	A36	AGTL+ I/O
D54#	B36	AGTL+ I/O
D55#	A33	AGTL+ I/O
D56#	B34	AGTL+ I/O
D57#	A37	AGTL+ I/O
D58#	B31	AGTL+ I/O
D59#	B38	AGTL+ I/O
D60#	A35	AGTL+ I/O
D61#	A32	AGTL+ I/O
D62#	B30	AGTL+ I/O
D63#	B32	AGTL+ I/O
DBSY#	A111	AGTL+ I/O
DEFER#	A105	AGTL+ Input
DEP0#	A25	AGTL+ I/O
DEP1#	A27	AGTL+ I/O
DEP2#	B26	AGTL+ I/O
DEP3#	A28	AGTL+ I/O
DEP4#	B27	AGTL+ I/O
DEP5#	A29	AGTL+ I/O

Table 35. Signal Listing in Order by Signal Name (Continued)

Pin Name	Pin #	Signal Group
DEP6#	A31	AGTL+ I/O
DEP7#	B28	AGTL+ I/O
DRDY#	B107	AGTL+ I/O
EMI	B1	Power/Other
EMI	B41	Power/Other
EMI	B61	Power/Other
EMI	B81	Power/Other
EMI	B100	Power/Other
FERR#	A7	CMOS Output
FLUSH#	B2	CMOS Input
GND	A2	Power/Other
GND	A6	Power/Other
GND	A10	Power/Other
GND	A18	Power/Other
GND	A22	Power/Other
GND	A26	Power/Other
GND	A30	Power/Other
GND	A34	Power/Other
GND	A38	Power/Other
GND	A42	Power/Other
GND	A46	Power/Other
GND	A50	Power/Other
GND	A54	Power/Other
GND	A58	Power/Other
GND	A62	Power/Other
GND	A66	Power/Other
GND	A70	Power/Other
GND	A74	Power/Other
GND	A78	Power/Other
GND	A82	Power/Other
GND	A86	Power/Other
GND	A90	Power/Other
GND	A94	Power/Other
GND	A98	Power/Other
GND	A102	Power/Other
GND	A106	Power/Other
GND	A110	Power/Other
GND	A114	Power/Other
GND	A118	Power/Other
HIT#	B110	AGTL+ I/O
HITM#	A109	AGTL+ I/O

Table 35. Signal Listing in Order by Signal Name (Continued)

Pin Name	Pin #	Signal Group
IERR#	A4	CMOS Output
IGNNE#	A8	CMOS Input
INIT#	B4	CMOS Input
LINT0/INTR	A17	CMOS Input
LINT1/NMI	B16	CMOS Input
LOCK#	B106	AGTL+ I/O
PICCLK	B18	APIC Clock
PICD0	A19	APIC I/O
PICD1	B22	APIC I/O
PRDY#	B23	AGTL+ Output
PREQ#	A20	CMOS Input
PWRGOOD	A12	CMOS Input
REQ0#	B102	AGTL+ I/O
REQ1#	B103	AGTL+ I/O
REQ2#	A107	AGTL+ I/O
REQ3#	A108	AGTL+ I/O
REQ4#	B104	AGTL+ I/O
Reserved	A16	Power/Other
Reserved	A47	Power/Other
Reserved	A88	Power/Other
Reserved	A113	Power/Other
Reserved	A116	Power/Other
Reserved	B12	Power/Other
Reserved	B20	Power/Other
Reserved	B76	Power/Other.
Reserved	B112	Power/Other
RESET#	B74	AGTL+ Input
RP#	B114	AGTL+ I/O
RS0#	B108	AGTL+ Input
RS1#	A112	AGTL+ Input
RS2#	B111	AGTL+ Input
RSP#	B115	AGTL+ Input
SLOTOCC#	B101	Power/Other
SLP#	B8	CMOS Input
SMI#	B3	CMOS Input
STPCLK#	B6	CMOS Input
TCK	B7	TAP Input
TDI	A9	TAP Input
TDO	A11	TAP Output
TESTHI	A13	Power/Other
THERMDN	B15	Power/Other

Table 35. Signal Listing in Order by Signal Name (Continued)

Pin Name	Pin #	Signal Group
THERMDP	B14	Power/Other
THERMTRIP#	A15	CMOS Output
TMS	B10	TAP Input
TRDY#	A104	AGTL+ Input
TRST#	B11	TAP Input
V_{CC_5}	B109	Power/Other
$V_{CC_{CORE}}$	B13	Power/Other
$V_{CC_{CORE}}$	B17	Power/Other
$V_{CC_{CORE}}$	B25	Power/Other
$V_{CC_{CORE}}$	B29	Power/Other
$V_{CC_{CORE}}$	B33	Power/Other
$V_{CC_{CORE}}$	B37	Power/Other
$V_{CC_{CORE}}$	B45	Power/Other
$V_{CC_{CORE}}$	B49	Power/Other
$V_{CC_{CORE}}$	B53	Power/Other
$V_{CC_{CORE}}$	B57	Power/Other
$V_{CC_{CORE}}$	B65	Power/Other
$V_{CC_{CORE}}$	B69	Power/Other
$V_{CC_{CORE}}$	B73	Power/Other
$V_{CC_{CORE}}$	B77	Power/Other
$V_{CC_{CORE}}$	B85	Power/Other
$V_{CC_{CORE}}$	B89	Power/Other
$V_{CC_{CORE}}$	B93	Power/Other
$V_{CC_{CORE}}$	B97	Power/Other
$V_{CC_{CORE}}$	B105	Power/Other
$V_{CC_{L2}}$	B113	Power/Other
$V_{CC_{L2}}$	B117	Power/Other
$V_{CC_{L2}}$	B121	Power/Other
VID0	B120	Power/Other
VID1	A120	Power/Other
VID2	A119	Power/Other
VID3	B119	Power/Other
VID4	A121	Power/Other
V_{TT}	A1	Power/Other
V_{TT}	A3	Power/Other
V_{TT}	B5	Power/Other
V_{TT}	B9	Power/Other

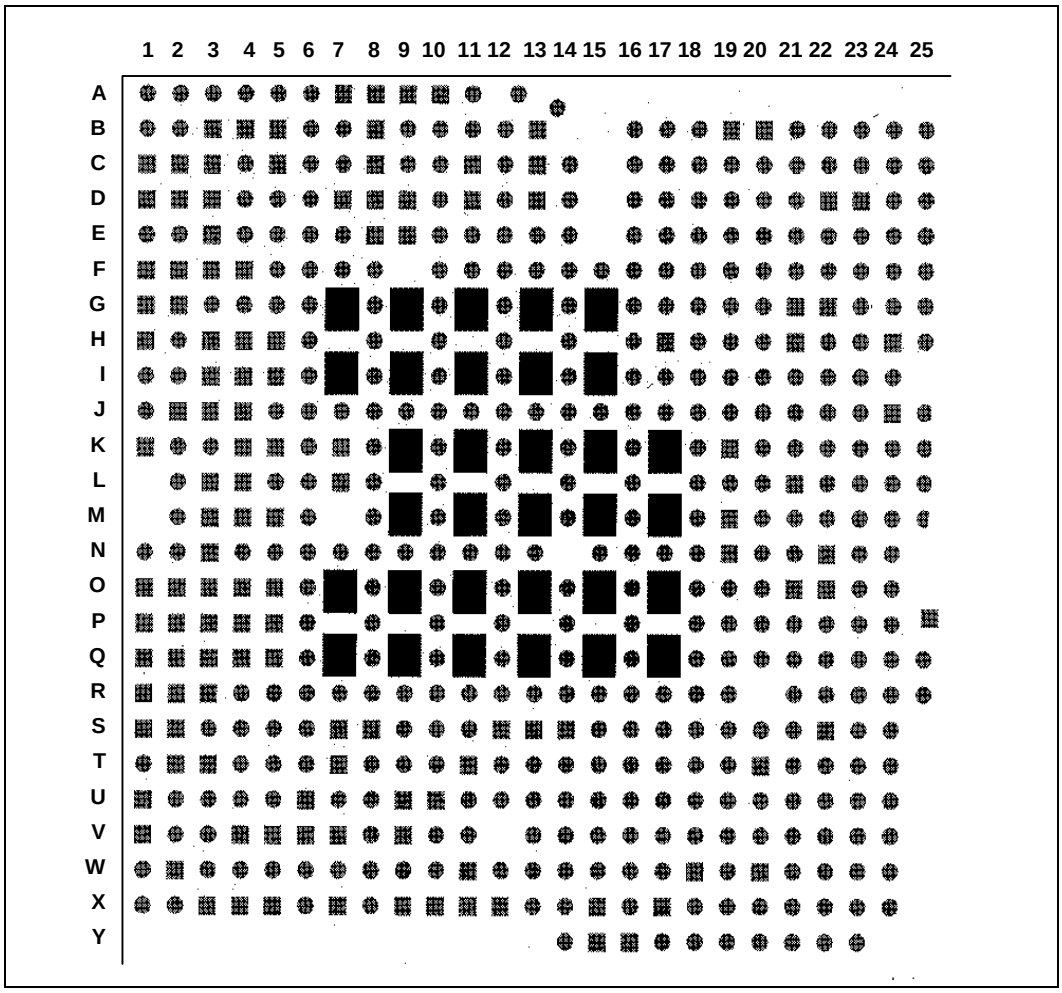
5.6 Intel® Pentium® III Processor Core Pad to Substrate Via Assignments

These test points are the closest locations to the processor core die pad and should be used to validate processor core timings and signal quality on the back of the S.E.C.C. or the S.E.C.C.2 package. See the SECC Disassembly Process Application Note for the instructions on removing the cover of the SECC package.

5.6.1 Processor Core Pad Via Assignments (CPUID=067xh)

Figure 48 shows the via locations on the back of the processor substrate.

Figure 48. Processor Core Pad Via Assignments



5.6.2 Processor Core Signal Assignments (CPUID=067xh)

Table 36 and Table 37 shows the signal to via and the via to signal assignments, respectively.

Table 36. Via Listing in Order by Signal Name

Signal Name	Via Locations
A3#	S18
A4#	W18
A5#	T18
A6#	U18
A7#	Y19
A8#	W19
A9#	V18
A10#	V19
A11#	W20
A12#	X20
A13#	V20
A14#	Y20
A15#	T21
A16#	W21
A17#	V21
A18#	Y21
A19#	W23
A20#	V24
A20M#	P23
A21#	V23
A22#	T22
A23#	U22
A24#	T24
A25#	S20
A26#	S23
A27#	T23
A28#	U23
A29#	R21
A30#	S22
A31#	S21
A32#	R24
A33#	Q20
A34#	R23
A35#	Q21
ADS#	X21
AERR#	X13
AP0#	S16
AP1#	X15

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
BCLK	R6
BERR#	Q23
BINT#	G17
BNR#	S17
BP2#	C16
BP3#	G16
BPM0#	B17
BPM1#	E17
BPRI#	T15
BR0#	V14
BR1#	T16
BSEL0	N23
BSEL1	V2
D0#	M21
D1#	M22
D2#	M19
D3#	M24
D4#	L23
D5#	M20
D6#	L20
D7#	L19
D8#	L22
D9#	L21
D10#	K23
D11#	K20
D12#	K24
D13#	K19
D14#	K25
D15#	K22
D16#	J24
D17#	J25
D18#	J21
D19#	I22
D20#	J23
D21#	J22
D22#	I23
D23#	K21
D24#	J20

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
D25#	I24
D26#	H23
D27#	H22
D28#	H20
D29#	I21
D30#	I19
D31#	H24
D32#	H21
D33#	G24
D34#	E25
D35#	G23
D36#	F23
D37#	F21
D38#	G25
D39#	E24
D40#	D25
D41#	C24
D42#	C23
D43#	G22
D44#	F24
D45#	D23
D46#	D22
D47#	E23
D48#	E22
D49#	B22
D50#	H19
D51#	D21
D52#	D24
D53#	C21
D54#	E21
D55#	B20
D56#	C19
D57#	B21
D58#	E19
D59#	E20
D60#	G19
D61#	F19
D62#	D20

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
D63#	D19
DBSY#	Y14
DEFER#	X17
DEP0#	H17
DEP1#	D18
DEP2#	C18
DEP3#	G18
DEP4#	E18
DEP5#	H18
DEP6#	B19
DEP7#	F18
DRDY#	Y16
FERR#	P25
FLUSH#	O19
HIT#	V13
HITM#	W14
IERR#	Q25
IGNNE#	O21
INIT#	P22
LINT[0]	F15
LINT[1]	E14
LOCK#	V15
PICCLK	B16
PICD[0]	D16
PICD[1]	H16
PRDY#	D17
PREQ#	E16
PWRGOOD	N21
REQ0#	U17
REQ1#	Y17
REQ2#	S15
REQ3#	W15
REQ4#	W16
RESET#	P21
RP#	S14
RS0#	W13
RS1#	S13
RS2#	T13

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
RSP#	V16
SLP#	O22
SMI#	Q24
STPCLK#	P24
TCK	O20
TDI	O23
TDO	N19
THERMTRIP#	M23
THRMDN	N24
THRMDP	M25
TMS	O24
TRDY#	X18
TRST#	N20
$V_{CC_{CORE}}$	A2
$V_{CC_{CORE}}$	A4
$V_{CC_{CORE}}$	B1
$V_{CC_{CORE}}$	B2
$V_{CC_{CORE}}$	B6
$V_{CC_{CORE}}$	B9
$V_{CC_{CORE}}$	B25
$V_{CC_{CORE}}$	C14
$V_{CC_{CORE}}$	D5
$V_{CC_{CORE}}$	E1
$V_{CC_{CORE}}$	E4
$V_{CC_{CORE}}$	E6
$V_{CC_{CORE}}$	E10
$V_{CC_{CORE}}$	E12
$V_{CC_{CORE}}$	F14
$V_{CC_{CORE}}$	G3
$V_{CC_{CORE}}$	G8
$V_{CC_{CORE}}$	G10
$V_{CC_{CORE}}$	G12
$V_{CC_{CORE}}$	G14
$V_{CC_{CORE}}$	H2
$V_{CC_{CORE}}$	H8
$V_{CC_{CORE}}$	H10
$V_{CC_{CORE}}$	H25
$V_{CC_{CORE}}$	I17

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
$V_{CC_{CORE}}$	J1
$V_{CC_{CORE}}$	J5
$V_{CC_{CORE}}$	J8
$V_{CC_{CORE}}$	J10
$V_{CC_{CORE}}$	J12
$V_{CC_{CORE}}$	J14
$V_{CC_{CORE}}$	J16
$V_{CC_{CORE}}$	K2
$V_{CC_{CORE}}$	L8
$V_{CC_{CORE}}$	L10
$V_{CC_{CORE}}$	L12
$V_{CC_{CORE}}$	L14
$V_{CC_{CORE}}$	L16
$V_{CC_{CORE}}$	M2
$V_{CC_{CORE}}$	N2
$V_{CC_{CORE}}$	N4
$V_{CC_{CORE}}$	N6
$V_{CC_{CORE}}$	N8
$V_{CC_{CORE}}$	N10
$V_{CC_{CORE}}$	N12
$V_{CC_{CORE}}$	N16
$V_{CC_{CORE}}$	P8
$V_{CC_{CORE}}$	P10
$V_{CC_{CORE}}$	P12
$V_{CC_{CORE}}$	P14
$V_{CC_{CORE}}$	P16
$V_{CC_{CORE}}$	Q22
$V_{CC_{CORE}}$	R5
$V_{CC_{CORE}}$	R7
$V_{CC_{CORE}}$	R8
$V_{CC_{CORE}}$	R10
$V_{CC_{CORE}}$	R12
$V_{CC_{CORE}}$	R14
$V_{CC_{CORE}}$	R16
$V_{CC_{CORE}}$	R18
$V_{CC_{CORE}}$	S19
$V_{CC_{CORE}}$	S24
$V_{CC_{CORE}}$	T4

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
$V_{CC_{CORE}}$	T5
$V_{CC_{CORE}}$	T9
$V_{CC_{CORE}}$	T12
$V_{CC_{CORE}}$	T19
$V_{CC_{CORE}}$	U2
$V_{CC_{CORE}}$	U14
$V_{CC_{CORE}}$	W1
$V_{CC_{CORE}}$	W6
$V_{CC_{CORE}}$	W9
$V_{CC_{CORE}}$	W24
$V_{CC_{CORE}}$	X2
$V_{CC_{CORE}}$	X14
$V_{CC_{CORE}}$	Y22
$V_{CC_{CORE}}$	Y23
VSS	X24
VSS	U3
VSS	U4
VSS	A1
VSS	A3
VSS	B11
VSS	B24
VSS	C17
VSS	C20
VSS	C22
VSS	C25
VSS	D4
VSS	D6
VSS	F6
VSS	F10
VSS	F17
VSS	F20
VSS	F22
VSS	F25
VSS	G4
VSS	I1
VSS	I2
VSS	I8
VSS	I10

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
VSS	I12
VSS	I14
VSS	I16
VSS	I18
VSS	I20
VSS	J6
VSS	J7
VSS	J9
VSS	J11
VSS	J13
VSS	J15
VSS	J17
VSS	J18
VSS	K6
VSS	K8
VSS	K10
VSS	K12
VSS	K14
VSS	K16
VSS	K18
VSS	L2
VSS	L18
VSS	L25
VSS	M6
VSS	M8
VSS	M10
VSS	M12
VSS	M14
VSS	M16
VSS	M18
VSS	N1
VSS	N18
VSS	O8
VSS	O10
VSS	O12
VSS	O14
VSS	O16
VSS	P18

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
VSS	Q8
VSS	Q10
VSS	Q12
VSS	Q14
VSS	Q16
VSS	Q18
VSS	R4
VSS	R9
VSS	R11
VSS	R13
VSS	R15
VSS	R17
VSS	R19
VSS	R22
VSS	R25
VSS	S3
VSS	S4

Table 36. Via Listing in Order by Signal Name (Continued)

Signal Name	Via Locations
VSS	S5
VSS	U13
VSS	U16
VSS	U19
VSS	U20
VSS	U21
VSS	U24
VSS	V22
VSS	W17
VSS	W22
VSS	X1
VSS	X7
VSS	X16
VSS	X19
VSS	X22
VSS	X23

Table 37. Via Listing in Order by VIA Location

Via Locations	Signal Name
A1	V_{SS}
A2	$V_{CC_{CORE}}$
A3	V_{SS}
A4	$V_{CC_{CORE}}$
B1	$V_{CC_{CORE}}$
B2	$V_{CC_{CORE}}$
B6	$V_{CC_{CORE}}$
B9	$V_{CC_{CORE}}$
B11	V_{SS}
B16	PICCLK
B17	BPM0#
B19	DEP6#
B20	D55#
B21	D57#
B22	D49#
B24	V_{SS}
B25	$V_{CC_{CORE}}$
C14	$V_{CC_{CORE}}$
C16	BP2#
C17	V_{SS}
C18	DEP2#
C19	D56#
C20	V_{SS}
C21	D53#
C22	V_{SS}
C23	D42#
C24	D41#
C25	V_{SS}
D4	V_{SS}
D5	$V_{CC_{CORE}}$
D6	V_{SS}
D16	PICD[0]
D17	PRDY#
D18	DEP1#
D19	D63#
D20	D62#
D21	D51#
D22	D46#

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
D23	D45#
D24	D52#
D25	D40#
E1	$V_{CC_{CORE}}$
E4	$V_{CC_{CORE}}$
E6	$V_{CC_{CORE}}$
E10	$V_{CC_{CORE}}$
E12	$V_{CC_{CORE}}$
E14	LINT[1]
E16	PREQ#
E17	BPM1#
E18	DEP4#
E19	D58#
E20	D59#
E21	D54#
E22	D48#
E23	D47#
E24	D39#
E25	D34#
F6	V_{SS}
F10	V_{SS}
F14	$V_{CC_{CORE}}$
F15	LINT[0]
F17	V_{SS}
F18	DEP7#
F19	D61#
F20	V_{SS}
F21	D37#
F22	V_{SS}
F23	D36#
F24	D44#
F25	V_{SS}
G3	$V_{CC_{CORE}}$
G4	V_{SS}
G8	$V_{CC_{CORE}}$
G10	$V_{CC_{CORE}}$
G12	$V_{CC_{CORE}}$
G14	$V_{CC_{CORE}}$

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
G16	BP3#
G17	BINT#
G18	DEP3#
G19	D60#
G22	D43#
G23	D35#
G24	D33#
G25	D38#
H2	$V_{CC_{CORE}}$
H8	$V_{CC_{CORE}}$
H10	$V_{CC_{CORE}}$
H16	PICD[1]
H17	DEP0#
H18	DEP5#
H19	D50#
H20	D28#
H21	D32#
H22	D27#
H23	D26#
H24	D31#
H25	$V_{CC_{CORE}}$
I1	V_{SS}
I2	V_{SS}
I8	V_{SS}
I10	V_{SS}
I12	V_{SS}
I14	V_{SS}
I16	V_{SS}
I17	$V_{CC_{CORE}}$
I18	V_{SS}
I19	D30#
I20	V_{SS}
I21	D29#
I22	D19#
I23	D22#
I24	D25#
J1	$V_{CC_{CORE}}$
J5	$V_{CC_{CORE}}$

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
J6	V_{SS}
J7	V_{SS}
J8	$V_{CC_{CORE}}$
J9	V_{SS}
J10	$V_{CC_{CORE}}$
J11	V_{SS}
J12	$V_{CC_{CORE}}$
J13	V_{SS}
J14	$V_{CC_{CORE}}$
J15	V_{SS}
J16	$V_{CC_{CORE}}$
J17	V_{SS}
J18	V_{SS}
J20	D24#
J21	D18#
J22	D21#
J23	D20#
J24	D16#
J25	D17#
K2	$V_{CC_{CORE}}$
K6	V_{SS}
K8	V_{SS}
K10	V_{SS}
K12	V_{SS}
K14	V_{SS}
K16	V_{SS}
K18	V_{SS}
K19	D13#
K20	D11#
K21	D23#
K22	D15#
K23	D10#
K24	D12#
K25	D14#
L02	V_{SS}
L08	$V_{CC_{CORE}}$
L10	$V_{CC_{CORE}}$
L12	$V_{CC_{CORE}}$

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
L14	$V_{CC_{CORE}}$
L16	$V_{CC_{CORE}}$
L18	V_{SS}
L19	D7#
L20	D6#
L21	D9#
L22	D8#
L23	D4#
L25	V_{SS}
M2	$V_{CC_{CORE}}$
M6	V_{SS}
M8	V_{SS}
M10	V_{SS}
M12	V_{SS}
M14	V_{SS}
M16	V_{SS}
M18	V_{SS}
M19	D2#
M20	D5#
M21	D0#
M22	D1#
M23	THERMTRIP#
M24	D3#
M25	THRMDP
N1	V_{SS}
N2	$V_{CC_{CORE}}$
N4	$V_{CC_{CORE}}$
N6	$V_{CC_{CORE}}$
N8	$V_{CC_{CORE}}$
N10	$V_{CC_{CORE}}$
N12	$V_{CC_{CORE}}$
N16	$V_{CC_{CORE}}$
N18	V_{SS}
N19	TDO
N20	TRST#
N21	PWRGOOD
N23	BSEL0
N24	THRMDN

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
O8	V_{SS}
O10	V_{SS}
O12	V_{SS}
O14	V_{SS}
O16	V_{SS}
O19	FLUSH#
O20	TCK
O21	IGNNE#
O22	SLP#
O23	TDI
O24	TMS
P8	$V_{CC_{CORE}}$
P10	$V_{CC_{CORE}}$
P12	$V_{CC_{CORE}}$
P14	$V_{CC_{CORE}}$
P16	$V_{CC_{CORE}}$
P18	V_{SS}
P21	RESET#
P22	INIT#
P23	A20M#
P24	STPCLK#
P25	FERR#
Q8	V_{SS}
Q10	V_{SS}
Q12	V_{SS}
Q14	V_{SS}
Q16	V_{SS}
Q18	V_{SS}
Q20	A33#
Q21	A35#
Q22	$V_{CC_{CORE}}$
Q23	BERR#
Q24	SMI#
Q25	IERR#
R4	V_{SS}
R5	$V_{CC_{CORE}}$
R6	BCLK
R7	$V_{CC_{CORE}}$

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
R8	$V_{CC_{CORE}}$
R9	V_{SS}
R10	$V_{CC_{CORE}}$
R11	V_{SS}
R12	$V_{CC_{CORE}}$
R13	V_{SS}
R14	$V_{CC_{CORE}}$
R15	V_{SS}
R16	$V_{CC_{CORE}}$
R17	V_{SS}
R18	$V_{CC_{CORE}}$
R19	V_{SS}
R21	A29#
R22	V_{SS}
R23	A34#
R24	A32#
R25	V_{SS}
S3	V_{SS}
S4	V_{SS}
S5	V_{SS}
S13	RS1#
S14	RP#
S15	REQ2#
S16	AP0#
S17	BNR#
S18	A3#
S19	$V_{CC_{CORE}}$
S20	A25#
S21	A31#
S22	A30#
S23	A26#
S24	$V_{CC_{CORE}}$
T4	$V_{CC_{CORE}}$
T5	$V_{CC_{CORE}}$
T9	$V_{CC_{CORE}}$
T12	$V_{CC_{CORE}}$
T13	RS2#
T15	BPRI#

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
T16	BR1#
T18	A5#
T19	$V_{CC_{CORE}}$
T21	A15#
T22	A22#
T23	A27#
T24	A24#
U02	$V_{CC_{CORE}}$
U03	V_{SS}
U04	V_{SS}
U13	V_{SS}
U14	$V_{CC_{CORE}}$
U16	V_{SS}
U17	REQ0#
U18	A6#
U19	V_{SS}
U20	V_{SS}
U21	V_{SS}
U22	A23#
U23	A28#
U24	V_{SS}
V2	BSEL1
V13	HIT#
V14	BR0#
V15	LOCK#
V16	RSP#
V18	A9#
V19	A10#
V20	A13#
V21	A17#
V22	V_{SS}
V23	A21#
V24	A20#
W1	$V_{CC_{CORE}}$
W6	$V_{CC_{CORE}}$
W9	$V_{CC_{CORE}}$
W13	RS0#
W14	HITM#

Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
W15	REQ3#
W16	REQ4#
W17	V_{SS}
W18	A4#
W19	A8#
W20	A11#
W21	A16#
W22	V_{SS}
W23	A19#
W24	$V_{CC_{CORE}}$
X01	V_{SS}
X02	$V_{CC_{CORE}}$
X07	V_{SS}
X13	AERR#
X14	$V_{CC_{CORE}}$
X15	AP1#
X16	V_{SS}

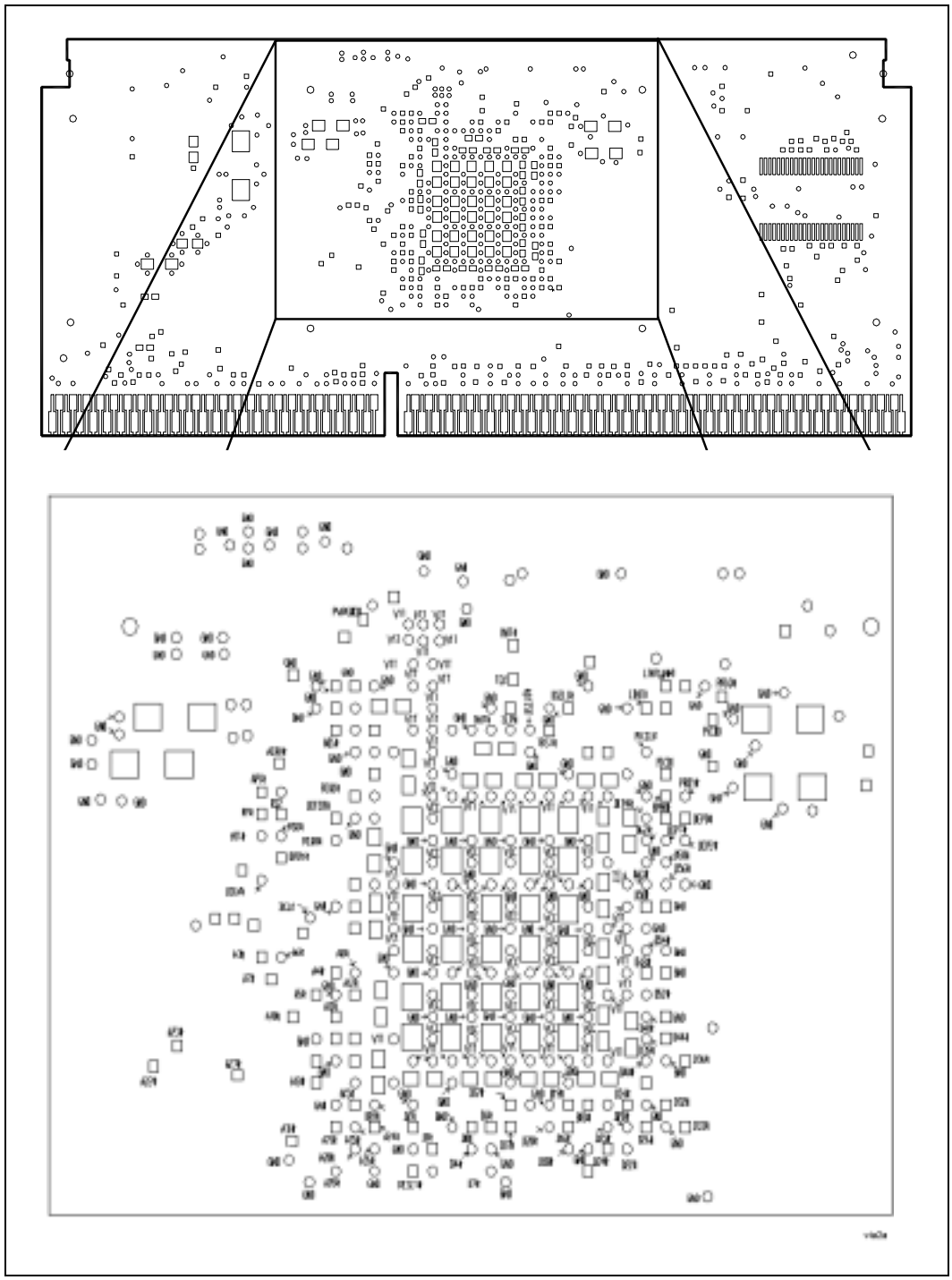
Table 37. Via Listing in Order by VIA Location (Continued)

Via Locations	Signal Name
X17	DEFER#
X18	TRDY#
X19	V_{SS}
X20	A12#
X21	ADS#
X22	V_{SS}
X23	V_{SS}
X24	V_{SS}
Y14	DBSY#
Y16	DRDY#
Y17	REQ1#
Y19	A7#
Y20	A14#
Y21	A18#
Y22	$V_{CC_{CORE}}$
Y23	$V_{CC_{CORE}}$

5.6.3 Processor Core Pad Via Assignments (CPUID=068xh)

Figure 49 shows the via locations on the back of the processor substrate.

Figure 49. Intel® Pentium® III Processor S.E.C.C. 2 Via Map



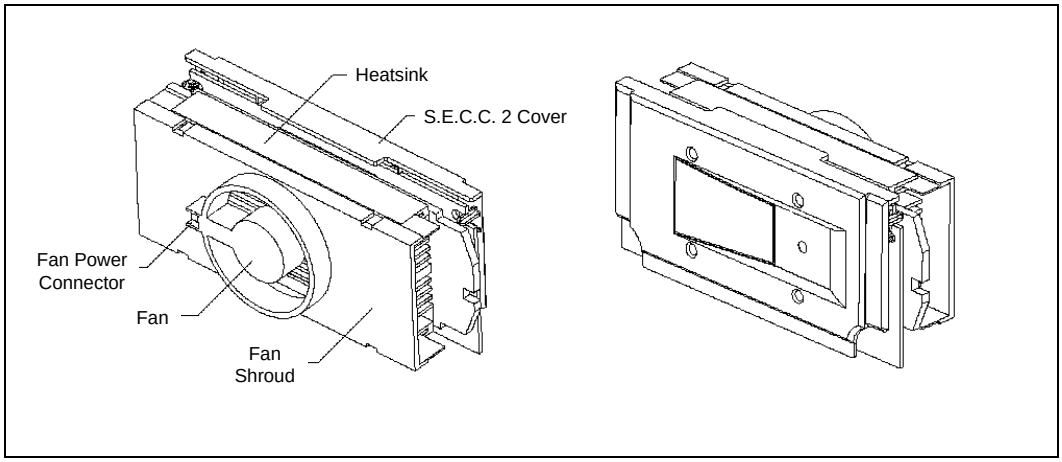
6.0 Boxed Processor Specifications

6.1 Introduction

The Pentium III processor is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from baseboards and components. Boxed Pentium III processors are supplied with an attached fan heatsink. This section documents baseboard and system requirements for the fan heatsink that will be supplied with the boxed Pentium III processor. This section is particularly important for original equipment manufacturer's (OEMs) that manufacture baseboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. Figure 50 shows a mechanical representation of a boxed Pentium III processor in the S.E.C.C.2 package. Boxed Pentium III processors are not available in the S.E.C.C. package.

Note: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

Figure 50. Boxed Intel® Pentium® III Processor in the S.E.C.C.2 Packaging (Fan Power Cable Not Shown)



6.2 Fan Heatsink Mechanical Specifications

This section documents the mechanical specifications of the boxed Pentium III processor fan heatsinks. Baseboard manufacturers and system designers should take into account the spacial requirement for the boxed Pentium III processor in the S.E.C.C.2 package.

6.2.1 Intel® Boxed Processor Fan Heatsink Dimensions

The boxed processor is shipped with an attached fan heatsink. Clearance is required around the fan heatsink to ensure unimpeded air flow for proper cooling. Spacial requirements and dimensions for the boxed processor in S.E.C.C.2 package are shown in Figure 51 (Side View), Figure 52 (Front View), and Figure 53 (Top View). All dimensions are in inches.

Figure 51. Side View Space Requirements for the Intel® Boxed Processor with S.E.C.C.2 Packaging

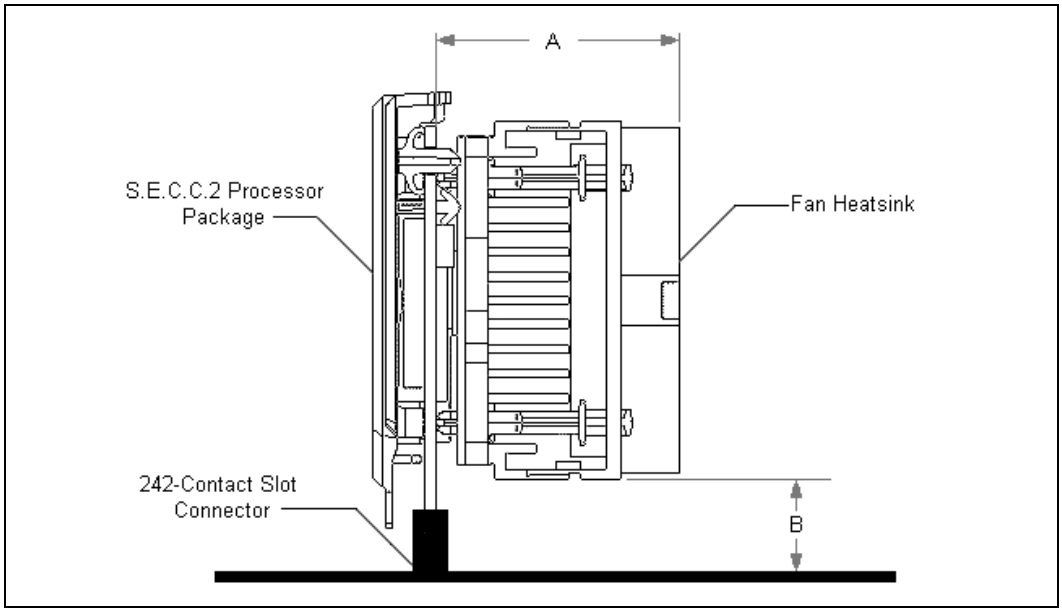


Figure 52. Front View Space Requirements for the Intel® Boxed Processor with S.E.C.C.2 Packaging

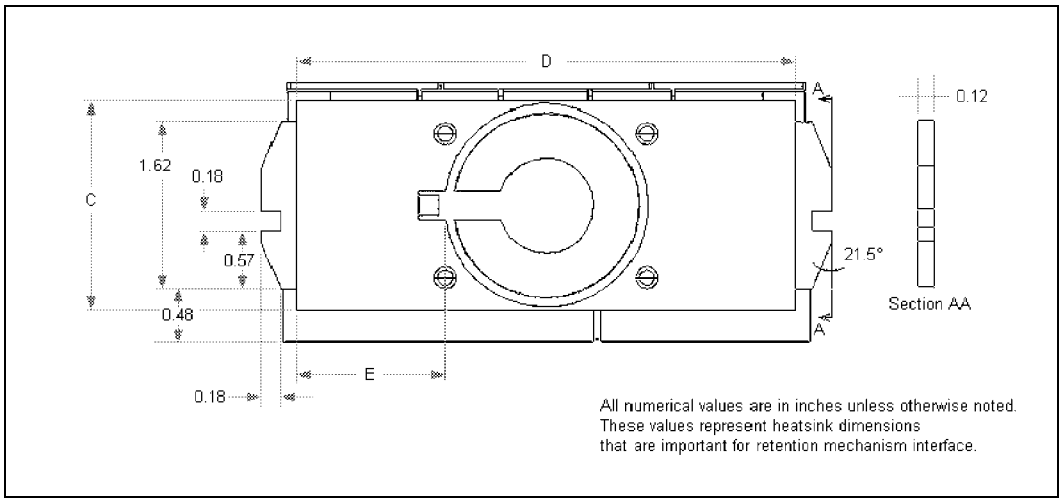


Figure 53. Top View Air Space Requirements for the Intel® Boxed Processor

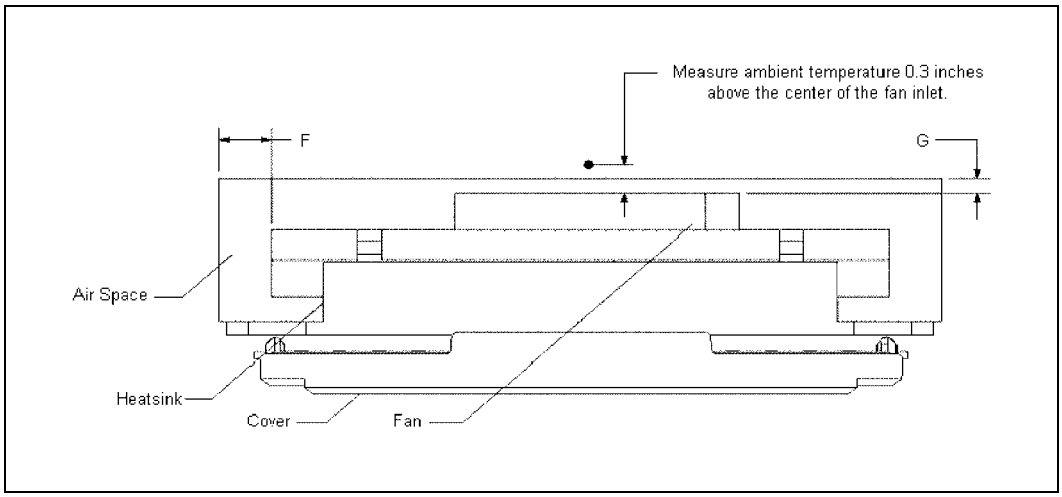


Table 38. Intel® Boxed Processor Fan Heatsink Spatial Dimensions

Fig. Ref. Label	Refers to Figure	Dimensions (Inches)	Min	Typ	Max
A	51	S.E.C.C.2 Fan Heatsink Depth (off processor substrate)			1.48
B	51	S.E.C.C.2 Fan Heatsink Height Above Baseboard	0.4		
C	52	S.E.C.C.2 Fan Heatsink Height			2.2
D	52	S.E.C.C.2 Fan Heatsink Width (plastic shroud only)			4.9
E	52	S.E.C.C.2 Power Cable Connector Location from Edge of Fan Heatsink Shroud	1.4		1.45
F	53	Airflow keep-out zones from end of fan heatsink	0.40		
G	53	Airflow keep-out zones from face of fan heatsink	0.20		

6.2.2 Intel® Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 225 grams. See Section 4.0 and Section 5.0 for details on the processor weight and heatsink requirements.

6.2.3 Intel® Boxed Processor Retention Mechanism

The boxed processor requires processor retention mechanism(s) to secure the processor in the 242-contact slot connector. S.E.C.C.2 processors must use either retention mechanisms described in AP-826, *Mechanical Assembly and Customer Manufacturing Technology for S.E.P. Packages* (Document Number 243748) or Universal Retention Mechanisms that accept S.E.C.C., S.E.P.P. and S.E.C.C.2 packaged processors. The boxed processor will **not** ship with a retention mechanism. Baseboards designed for use by system integrators **must** include retention mechanisms that support the S.E.C.C.2 package and the appropriate installation instructions.

Baseboards designed to accept both Pentium II processors and Pentium III processors have component height restrictions for passive heatsink support designs, as described in AP-588, *Mechanical and Assembly Technology for S.E.C. Cartridge Processors* (Document Number 243333).

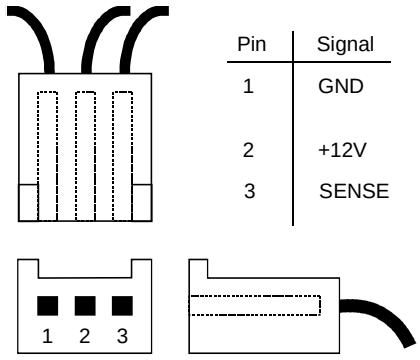
6.3 Fan Heatsink Electrical Requirements

6.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the baseboard. The power cable connector and pinout are shown in Figure 54. Baseboards must provide a matched power header to support the boxed processor. Table 39 contains specifications for the input and output signals at the fan heatsink connector. The cable length will be 7.0 ±0.25 inches. The fan heatsink outputs a SENSE signal, which is an open-collector output, that pulses at a rate of two pulses per fan revolution. A baseboard pull-up resistor (~12 kΩ) provides V_{OH} to match the baseboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the baseboard documentation, or on the baseboard itself. Figure 54 shows the location of the fan power connector relative to the 242-contact slot connector. The baseboard power header should be positioned within 4.75 inches (lateral) of the fan power connector.

Figure 54. Intel® Boxed Processor Fan Heatsink Power Cable Connector Description



Pin	Signal
1	GND
2	+12V
3	SENSE

Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pin pitch, 0.025" square pin width.

Waldom/Molex P/N 22-01-3037 or equivalent.

Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP P/N 640456-3, or equivalent.

Table 39. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	9 V	12 V	13.8 V
I_C: Fan current draw			100 mA
Ics: Fan sense signal current			10 mA
SENSE: SENSE frequency (baseboard should pull this pin up to appropriate Vcc with resistor)		2 pulses per fan revolution	

Figure 55. Recommended Baseboard Power Header Placement Relative to Fan Power Connector and Intel® Pentium® III Processor

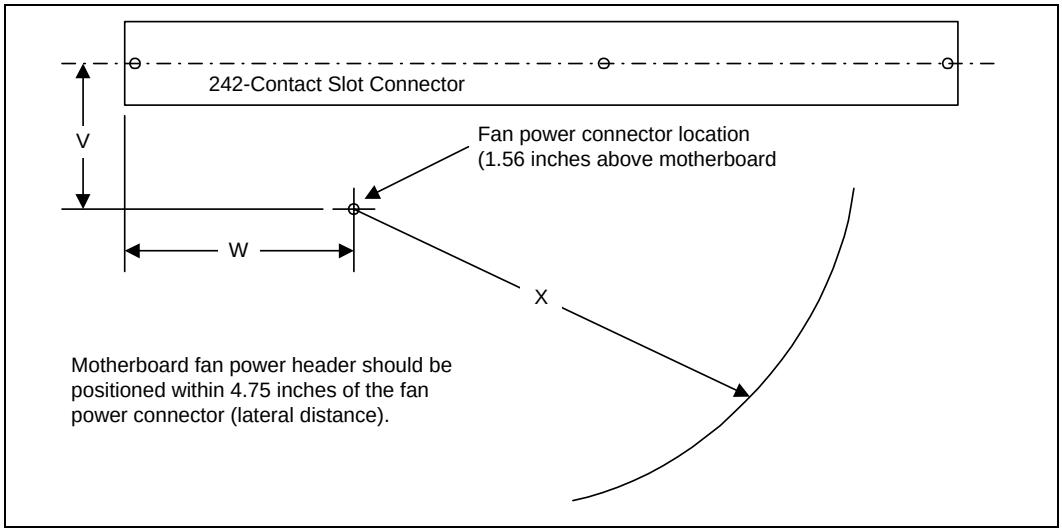


Table 40. Baseboard Fan Power Connector Location

Fig. Ref. Labels	Dimensions (Inches)	Min	Typ	Max
V	Approximate perpendicular distance of the fan power connector from the center of the 242-contact slot connector		1.44	
W	Approximate parallel distance of the fan power connector from the edge of the 242-contact slot connector		1.45	
X	Lateral distance of the baseboard fan power header location from the fan power connector			4.75

6.4 Fan Heatsink Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

6.4.1 Intel® Boxed Processor Cooling Requirements

The boxed processor will be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. Refer to Section 4.0 for processor temperature specifications. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 25 and Table 26) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 53 illustrates an acceptable airspace clearance for the fan heatsink. It is also recommended that the air temperature entering the fan be kept below 45 °C (see Figure 53 for measurement location). Again, meeting the processor's temperature specification is the responsibility of the system integrator. Refer to Section 4.0 for processor temperature specifications.

7.0 Intel® Pentium® III Processor Signal Description

This section provides an alphabetical listing of all Pentium III processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

7.1 Alphabetical Signals Reference

Table 41. Signal Description (Sheet 1 of 7)

Name	Type	Description
A[35:3]#	I/O	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[35:3]# pins to determine their power-on configuration. See the *Intel® Pentium® II Processor Developer's Manual* (Document Number 243502) for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all processor system bus agents.
AERR#	I/O	The AERR# (Address Parity Error) signal is observed and driven by all processor system bus agents, and if used, must connect the appropriate pins on all processor system bus agents. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#, and AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Table 41. Signal Description (Sheet 2 of 7)

Name	Type	Description
BERR#	I/O	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents, and must connect the appropriate pins of all such agents, if used. However, Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted optionally for internal errors along with IERR#. • Asserted optionally by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction.
BINIT#	I/O	The BINIT# (Bus Initialization) signal may be observed and driven by all processor system bus agents, and if used must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after Reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.

Table 41. Signal Description (Sheet 3 of 7)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BR0#
BR1#</td><td>I/O
I</td><td>The BR0# and BR1# (Bus Request) pins drive the BREQ[1:0]# signals in the system. The BREQ[1:0]# signals are interconnected in a rotating manner to individual processor pins. The table below gives the rotating interconnect between the processor and bus signals.

BR0# (I/O) and BR1# Signals Rotating Interconnect
<table><tr><th>Bus Signal</th><th>Agent 0 Pins</th><th>Agent 1 Pins</th></tr><tr><td>BREQ0#</td><td>BR0#</td><td>BR1#</td></tr><tr><td>BREQ1#</td><td>BR1#</td><td>BR0#</td></tr></table>During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[1:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its symmetric agent ID. All agents then configure their pins to match the appropriate bu signal protocol, as shown below.
BR[1:0]# Signal Agent IDs
<table><tr><th>Pin Sampled Active in RESET#</th><th>Agent ID</th></tr><tr><td>BR0#</td><td>0</td></tr><tr><td>BR1#</td><td>1</td></tr></table></td></tr>
<tr><td>BSEL[1:0]</td><td>I/O</td><td>These signals are used to select the system bus frequency. A BSEL[1:0] = 01 will select a 100 MHz system bus and a BSEL[1:0] = 11 will select a 133 MHz system bus frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All system bus agents must operate at the same frequency. The Pentium III processor operates at 100 MHz and 133 MHz system bus frequencies. Individual processors will only operate at their specified system bus frequency. Either 100 MHz or 133 MHz, not both.
On motherboards which support operation at either 66 MHz or 100 MHz, a BSEL[1:0] = x0 will select a 66 MHz system bus frequency.
These signals must be pulled up to 3.3 V with 1 kΩ resistors and provided as frequency selection signal to the clock driver/synthesizer. If the system motherboard is not capable of operating at 133 MHz, it should ground the BSEL1 signal and generate a 100 MHz system bus frequency. See Section 2.8.2 for implementation details.</td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DEP[7:0]#</td><td>I/O</td><td>The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor system bus agents which use them. The DEP[7:0]# signals are enabled or disabled for ECC protection during power on configuration.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
</table>

Table 41. Signal Description (Sheet 4 of 7)

Name	Type	Description
EMI	I	EMI pins should be connected to baseboard ground and/or to chassis ground through zero ohm (0 Ω) resistors. The 0 Ω resistors should be placed in close proximity to the processor connector. The path to chassis ground should be short in length and have a low impedance. These pins are used for EMI management purposes.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, processors write back all data in the Modified state from their internal caches and invalidate all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, each processor samples FLUSH# to determine its power-on configuration. See the *P6 Family of Processors Hardware Developer's Manual* (Document Number 244001) for details.
HIT# HITM#	I/O I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1 or L2) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.

Table 41. Signal Description (Sheet 5 of 7)

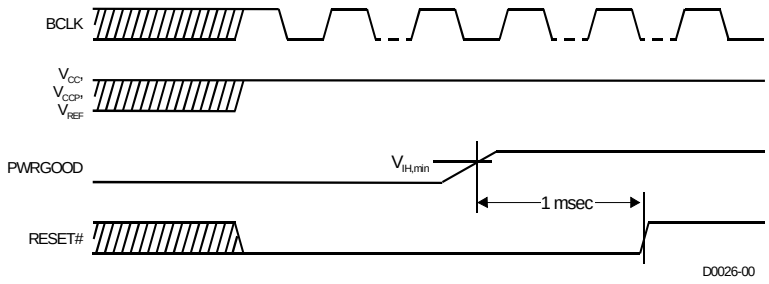
Name	Type	Description
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of all processors and core logic or I/O APIC components on the APIC bus.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The PWRGOOD (Power Good) signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies (V_{CC_CORE}, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state. The figure below illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 15, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. **PWRGOOD Relationship at Power-On** 
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.

Table 41. Signal Description (Sheet 6 of 7)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RESET#</td><td>I</td><td>Asserting the RESET# signal resets all processors to known states and invalidates their L1 and L2 caches without writing back any of their contents. For a Power-on or “warm” reset, RESET# must stay active for at least one millisecond after Vcc_{CORE} and CLK have reached their proper specifications. On observing active RESET#, all processor system bus agents will deassert their outputs within two clocks.
A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the P6 Family of Processors Hardware Developer’s Manual (Document Number 244001) for details.
The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>RP#</td><td>I/O</td><td>The RP# (Request Parity) signal is driven by the request initiator, and provides parity protection on ADS# and REQ[4:0]#. It must connect the appropriate pins of all processor system bus agents.
A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.</td></tr>
<tr><td>RS[2:0]#</td><td>I</td><td>The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>RSP#</td><td>I</td><td>The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect the appropriate pins of all processor system bus agents.
A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.</td></tr>
<tr><td>SLOTOCC#</td><td>O</td><td>The SLOTOCC# signal is defined to allow a system design to detect the presence of a terminator card or processor in a SC242 connector. Combined with the VID combination of VID[4:0]= 11111 (see Section 2.6), a system can determine if a SC242 connector is occupied, and whether a processor core is present. See the table below for states and values for determining the type of cartridge in the SC242 connector.
SC242 Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
Anything other than ‘11111’</td><td>Processor with core in SC242 connector.</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>0
11111</td><td>Terminator cartridge in SC242 connector (i.e., no core present).</td></tr>
<tr><td>SLOTOCC#
VID[4:0]</td><td>1
Any value</td><td>SC242 connector not occupied.</td></tr>
</table></td></tr>
<tr><td>SLP#</td><td>I</td><td>The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.</td></tr>
</table>

Table 41. Signal Description (Sheet 7 of 7)

Name	Type	Description
SMI#	I	The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I	The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	The TCK (Test Clock) signal provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI	I	The TESTHI signal must be connected to a 2.5 V power source through a 1–100 kΩ resistor for proper processor operation.
THERMDN	O	Thermal Diode Cathode. Used to calculate core temperature. See Section 4.1.
THERMDP	I	Thermal Diode Anode. Used to calculate core temperature. See Section 4.1.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all processor system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 Ω pull-down resistor.
VID[4:0]	O	The VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on processors. See Table 3 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.

7.2 Signal Summaries

Table 42 through Table 45 list attributes of the processor output, input, and I/O signals.

Table 42. Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
SLOTOCC#	Low	Asynch	Power/Other
TDO	High	TCK	TAP Output
THERMTRIP#	Low	Asynch	CMOS Output
VID[4:0]	High	Asynch	Power/Other

Table 43. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always[1]
BPRI#	Low	BCLK	AGTL+ Input	Always
BR1#	Low	BCLK	AGTL+ Input	Always
BCLK	High	—	System Bus Clock	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always[1]
IGNNE#	Low	Asynch	CMOS Input	Always[1]
INIT#	Low	Asynch	CMOS Input	Always[1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
RSP#	Low	BCLK	AGTL+ Input	Always
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	TAP Input	
TDI	High	TCK	TAP Input	
TESTHI	High	Asynch	Power/Other	Always
TMS	High	TCK	TAP Input	
TRST#	Low	Asynch	TAP Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:
1. Synchronous assertion with active TDRY# ensures synchronization.

Table 44. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
BSEL[1:0]	High	Asynch	Power/Other	Always
A[35:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
AP[1:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
BR0#	Low	BCLK	AGTL+ I/O	Always
BP[3:2]#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DEP[7:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
RP#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 45. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	AGTL+ I/O	ADS#+3
BERR#	Low	BCLK	AGTL+ I/O	Always
BNR#	Low	BCLK	AGTL+ I/O	Always
BINIT#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always

Pentium® III Processor for the PGA370 Socket at 500 MHz to 1.13 GHz

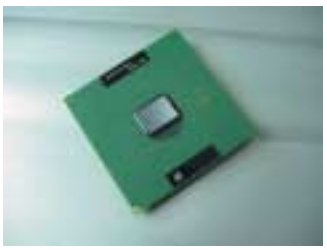
Datasheet *Revision 8*

Product Features

- Available in 1.13 GHz, 1B GHz, 933, 866, 800EB, 733, 667, 600EB, and 533EB MHz for a 133 MHz system bus
- Available in 1.10 GHz, 1 GHz, 900, 850, 800, 750, 700, 650, 600E, 550E, and 500E MHz for a 100 MHz system bus
- System bus frequency at 100 MHz and 133 MHz ("E" denotes support for Advanced Transfer Cache and Advanced system buffering; "B" denotes support for a 133 MHz system bus where both bus frequencies are available for order per each given core frequency; See Table 1 for a summary of features for each line item.)
- Available in versions that incorporate 256-KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache with Error Correcting Code (ECC))
- Dual Independent Bus (DIB) architecture: Separate dedicated external System Bus and dedicated internal high-speed cache bus
- Internet Streaming SIMD Extensions for enhanced video, sound and 3D performance
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Dynamic execution micro architecture
- Intel Processor Serial Number
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Flip Chip Pin Grid Array (FC-PGA/FC-PGA2) packaging technology; FC-PGA/FC-PGA2 processors deliver high performance with improved handling protection and socketability
- Integrated high performance 16-KB instruction and 16-KB data, nonblocking, level one cache
- 256-KB Integrated Full Speed level two cache allows for low latency on read/store operations
- Double Quad Word Wide (256 bit) cache data bus provides extremely high throughput on read/store operations.
- 8-way cache associativity provides improved cache hit rate on reads/store operations.
- Error-correcting code for System Bus data
- Enables systems which are scaleable for up to two processors

The Pentium® III processor is designed for high-performance desktops and for workstations and servers. It is binary compatible with previous Intel Architecture processors. The Pentium III processor provides great performance for applications running on advanced operating systems such as Windows* 98, Windows NT and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution, Dual Independent Bus architecture plus Intel MMX™ technology and Internet Streaming SIMD Extentions— bringing a new level of performance for systems buyers. The Pentium III processor is scaleable to two processors in a multiprocessor system and extends the power of the Pentium® II processor with performance headroom for business media, communication and internet capabilities. Systems based on Pentium III processors also include the latest features to simplify system management and lower the cost of ownership for large and small business environments. The Pentium III processor offers great performance for today's and tomorrow's applications.

FC-PGA370 Package



June 2001

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Tables

1.0 Introduction

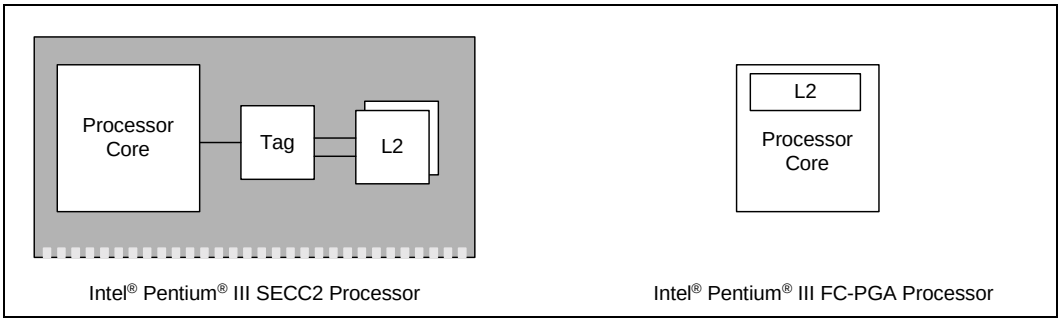
The Intel® Pentium® III processor for the PGA370 socket is the next member of the P6 family, in the Intel IA-32 processor line and hereafter will be referred to as the “Pentium III processor”, or simply “the processor”. The processor uses the same core and offers the same performance as the Pentium III processor for the SC242 connector, but utilizes a package technology called flip-chip pin grid array, or FC-PGA. This package utilizes the same 370-pin zero insertion force socket (PGA370) used by the Intel® Celeron™ processor. Thermal solutions are attached directly to the back of the processor core package without the use of a thermal plate or heat spreader. As core frequencies increase, the need for better power dissipation arises, so an Integrated Heat Spreader (IHS) has been introduced at the higher frequencies near 1B GHz. The package with an IHS is called FC-PGA2.

The Pentium III processor, like its predecessors in the P6 family of processors, implements a Dynamic Execution microarchitecture—a unique combination of multiple branch prediction, data flow analysis, and speculative execution. This enables these processors to deliver higher performance than the Pentium processor, while maintaining binary compatibility with all previous Intel Architecture processors. The processor also executes Intel® MMX™ technology instructions for enhanced media and communication performance just as it’s predecessor, the Pentium III processor. Additionally, Pentium III processor executes Streaming SIMD (single-instruction, multiple data) Extensions for enhanced floating point and 3-D application performance. The concept of processor identification, via CPUID, is extended in the processor family with the addition of a processor serial number. Refer to the *Intel® Processor Serial Number* application note for more detailed information. The processor utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The processor includes an integrated on-die, 256-KB, 8-way set associative level-two (L2) cache. The L2 cache implements the new Advanced Transfer Cache Architecture with a 256-bit wide bus. The processor also includes a 16-KB level one (L1) instruction cache and 16-KB L1 data cache. These cache arrays run at the full speed of the processor core. As with the Pentium III processor for the SC242 connector, the Pentium III processor for the PGA370 socket has a dedicated L2 cache bus, thus maintaining the dual independent bus architecture to deliver high bus bandwidth and performance (see Figure 1). Memory is cacheable for 64 GB of addressable memory space, allowing significant headroom for desktop systems. Refer to the Specification Update document for this processor to determine the cacheability and cache configuration options for a specific processor. The Specification Update document can be requested at your nearest Intel sales office.

The processor utilizes the same multiprocessing system bus technology as the Pentium II processor. This allows for a higher level of performance for both uni-processor and two-way multiprocessor systems. The system bus uses a variant of GTL+ signaling technology called Assisted Gunning Transceiver Logic (AGTL+/AGTL) signaling technology.

Figure 1. Second Level (L2) Cache Implementation



1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. the chipset components), and other bus agents.

1.1.1 Package and Processor Terminology

The following terms are used often in this document and are explained here for clarification:

- **Pentium III processor** - The entire product including all internal components.
- **PGA370 socket** - 370-pin Zero Insertion Force (ZIF) socket which a FC-PGA or PPGA packaged processor plugs into.
- **FC-PGA** - Flip Chip Pin Grid Array. The package technology used on Pentium III processors for the PGA370 socket.
- **FC-PGA2** - Flip Chip Pin Grid Array with an Integrated Heat Spreader (IHS). The package technology used on Pentium III processors for the PGA370 socket for increased power dissipation away from the die. The IHS covers the die and has a very low thermal resistance.
- **Integrated Heat Spreader (IHS)** - The IHS is a metal cover on the die and is an integral part of the CPU. The IHS promotes heat spreading away from the die backside to ease thermal constraints.
- **Advanced Transfer Cache (ATC)** - New L2 cache architecture unique to the 0.18 micron Pentium III processors. ATC consists of microarchitectural improvements that provide a higher data bandwidth interface into the processor core that is completely scaleable with the processor core frequency.
- **Keep-out zone** - The area on or near a FC-PGA packaged processor that system designs can not utilize.
- **Keep-in zone** - The area of a FC-PGA packaged processor that thermal solutions may utilize.
- **OLGA** - Organic Land Grid Array. The package technology for the core used in S.E.C.C. 2 processors that permits attachment of the heatsink directly to the die.
- **PPGA - Plastic Pin Grid Array.** The package technology used for Celeron processors that utilize the PGA370 socket.
- **Processor** - For this document, the term processor is the generic form of the Pentium III processor for the PGA370 socket in the FC-PGA package.
- **Processor core** - The processor's execution engine.
- **S.E.C.C.** - The processor package technology called "Single Edge Contact Cartridge". Used with Intel® Pentium® II processors.
- **S.E.C.C. 2** - The follow-on to S.E.C.C. processor package technology. This differs from its predecessor in that it has no extended thermal plate, thus reducing thermal resistance. Used with Pentium III processors and latest versions of the Pentium II processor.

- **SC242** - The 242-contact slot connector (previously referred to as slot 1 connector) that the S.E.C.C. and S.E.C.C. 2 plug into, just as the Intel® Pentium® Pro processor uses socket 8.

The cache and L2 cache are an industry designated names.

1.1.2 Processor Naming Convention

A letter(s) is added to certain processors (e.g., 600EB MHz) when the core frequency alone may not uniquely identify the processor. Below is a summary of what each letter means as well as a table listing all the available Pentium III processors for the PGA370 socket.

"B" — 133 MHz System Bus Frequency

"E" — Processor with "Advanced Transfer Cache" (CPUID 068xh and greater)

Table 1. Processor Identification

Processor	Core Frequency (MHz)	System Bus Frequency (MHz)	L2 Cache Size (Kbytes)	L2 Cache Type[2]	CPUID[1]
500E	500	100	256	ATC	068xh
533EB	533	133	256	ATC	068xh
550E	550	100	256	ATC	068xh
600E	600	100	256	ATC	068xh
600EB	600	133	256	ATC	068xh
650	650	100	256	ATC	068xh
667	667	133	256	ATC	068xh
700	700	100	256	ATC	068xh
733	733	133	256	ATC	068xh
750	750	100	256	ATC	068xh
800	800	100	256	ATC	068xh
800EB	800	133	256	ATC	068xh
850	850	100	256	ATC	068xh
866	866	133	256	ATC	068xh
900	900	100	256	ATC	068xh
933	933	133	256	ATC	068xh
1 GHz	1000	100	256	ATC	068xh
1B GHz	1000	133	256	ATC	068xh
1.10 GHz	1100	100	256	ATC	068xh
1.13 GHz	1133	133	256	ATC	068xh

NOTES:
1. Refer to the *Pentium® III Processor Specification Update* for the exact CPUID for each processor.
2. ATC = Advanced Transfer Cache. ATC is an L2 Cache integrated on the same die as the processor core. With ATC, the interface between the processor core and L2 Cache is 256-bits wide, runs at the same frequency as the processor core and has enhanced buffering.

1.2 Related Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents [1,2]:

Document	Intel Document Number
AP-485, *Intel® Processor Identification and the CPUID Instruction*	241618
AP-585, *Pentium® II Processor GTL+ Guidelines*	243330
AP-589, *Design for EMI*	243334
AP-905, *Pentium® III Processor Thermal Design Guidelines*	245087
AP-907, *Pentium® III Processor Power Distribution Guidelines*	245085
AP-909, Intel® Processor Serial Number	245125
Intel® Architecture Software Developer's Manual	243193
Volume I: Basic Architecture	243190
Volume II: Instruction Set Reference	243191
Volume III: System Programming Guide	243192
P6 Family of Processors Hardware Developer's Manual	244001
Pentium® II Processor Developer's Manual	243502
Pentium® III Processor Datasheet for SECC2	244452
Pentium® III Processor Datasheet for PGA370	245264
Pentium® III Processor Specification Update	244453
Intel® Celeron™ Processor Datasheet	243658
Intel® Celeron™ Processor Specification Update	243748
370-Pin Socket (PGA370) Design Guidelines	244410
PGA370 Heat Sink Cooling in MicroATX Chassis	245025
Intel® 810E Chipset Platform Design Guide	290675
Intel® 815 B-step Chipset Platform Design Guide[3]	
Intel® 815E Chipset Platform Design Guide	298234
Intel® 820 Chipset Platform Design Guide	290631
Intel® 840 Chipset Platform Design Guide	298021
CK98 Clock Synthesizer/Driver Design Guidelines	245338
Intel® 810E Chipset Clock Synthesizer/Driver Specification [3]	
VRM 8.4 DC-DC Converter Design Guidelines	245335
Pentium III Processor for the PGA370 Socket I/O Buffer Models, XTK/XNS Format* [3]	
Pentium® Pro Processor BIOS Writer's Guide [3]	
Extensions to the Pentium® Pro Processor BIOS Writer's Guide rev. 3.7 [3]	
Pentium® III Thermal/Mechanical Solution Functional Guidelines	245241
Intel®Pentium® III Processor in the FC-PGA2 Package Thermal Design Guide	249660

NOTES:

1. Unless otherwise noted, this reference material can be found on the Intel Developer's Website located at http://developer.intel.com.
2. For a complete listing of Pentium III processor reference material, please refer to the Intel Developer's Website at http://developer.intel.com/design/PentiumIII/.
3. This material is available through an Intel field sales representative.

2.0 Electrical Specifications

2.1 Processor System Bus and V_{REF}

The Pentium III processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

The Pentium Pro processor system bus specification is similar to the GTL specification, but was enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. This specification is different from the GTL specification, and is referred to as GTL+. For more information on GTL+ specifications, see the GTL+ buffer specification in the *Intel® Pentium® II Processor Developer's Manual*.

Current P6 family processors vary from the Pentium Pro processor in their output buffer implementation. The buffers that drive the system bus signals on the Celeron, Pentium II, and Pentium III processors are actively driven to V_{TT} for one clock cycle after the low to high transition to improve rise times. These signals should still be considered open-drain and require termination to a supply that provides the high signal level. Because this specification is different from the standard GTL+ specification, it is referred to as AGTL+, or Assisted GTL+ in this and other documentation. AGTL+ logic and GTL+ logic are compatible with each other and may both be used on the same system bus. For more information on AGTL+ routing, see the appropriate platform design guide.

Note that some Pentium III processors with CPUID 068xh support the AGTL specification in addition to the AGTL+ specification. AGTL logic and AGTL+ logic are not compatible with each other due to differences with the signal switching levels. Processors that do not support the AGTL specification cannot be installed into platforms where the chipset only supports the AGTL signal levels. For more information on AGTL or AGTL+ routing, please refer to the appropriate platform design guide.

Both AGTL and AGTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1, and is supplied by the motherboard to the PGA370 socket for the processor core. Local V_{REF} copies should also be generated on the motherboard for all other devices on the AGTL+ (AGTL) system bus. Termination (usually a resistor at each end of the signal trace) is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor contains on-die termination resistors that provide termination for one end of the bus, except for RESET#. These specifications assume another resistor at the end of each signal trace to ensure adequate signal quality for the AGTL+ (AGTL) signals and provide backwards compatibility for the Celeron processor; see Table 12 for the bus termination voltage specifications for AGTL+. Refer to the *Intel® Pentium® II Processor Developer's Manual* for the AGTL+ bus specification. Solutions exist for single-ended termination as well, though this implementation changes system design and eliminate backwards compatibility for Celeron processors in the PPGA package. Single-ended termination designs must still provide an AGTL+ (AGTL) termination resistor on the motherboard for the RESET# signal. Figure 2 is a schematic representation of the AGTL+ (AGTL) bus topology for the Pentium III processors in the PGA370 socket. Figure 3 is a schematic representation of the AGTL+/AGTL bus topology in a dual-processor configuration with Pentium III processors in the PGA370 socket.

Both AGTL+ and AGTL bus depend on incident wave switching. Therefore, timing calculations for AGTL+ or AGTL signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus including trace lengths is highly recommended when designing a

system with a heavily loaded AGTL+ bus, especially for systems using a single set of termination resistors (i.e., those on the processor die). Such designs will not match the solution space allowed for by installation of termination resistors on the baseboard.

Figure 2. AGTL+/AGTL Bus Topology in a Uniprocessor Configuration

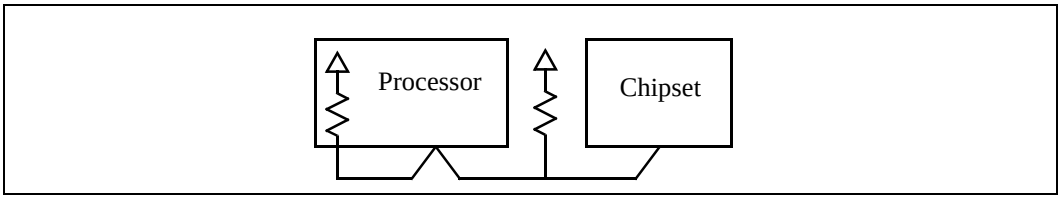
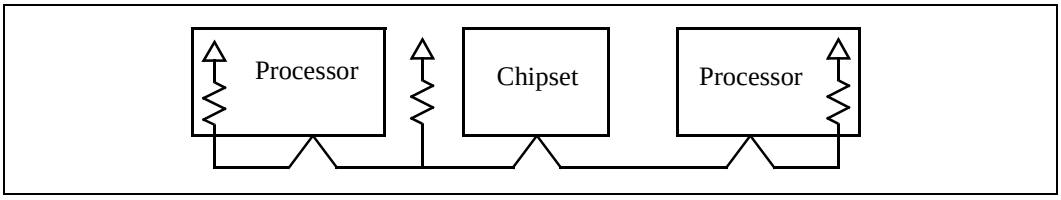


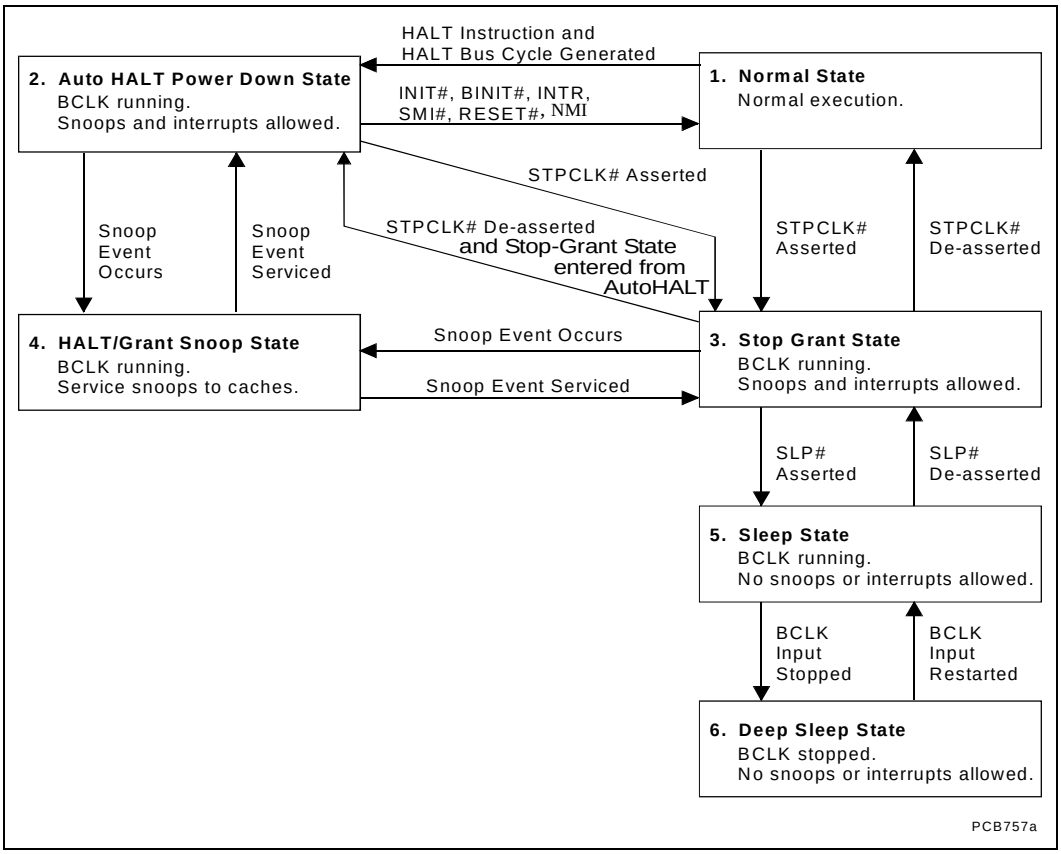
Figure 3. AGTL+/AGTL Bus Topology in a Dual-Processor Configuration



2.2 Clock Control and Low Power States

Processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 4 for a visual representation of the processor low-power states.

Figure 4. Stop Clock State Machine



For the processor to fully realize the low current consumption of the Stop-Grant, Sleep and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a '1' (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide* located on the developer.intel.com website.

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor transitions to the Normal state upon the occurrence of SMI#, INIT#, or LINT[1:0] (NMI, INTR). RESET# causes the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

FLUSH# is serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor returns execution to the HALT state.

2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# and FLUSH# are not serviced during the Stop-Grant state.

RESET# causes the processor to immediately initialize itself, but the processor stays in Stop-Grant state. A transition back to the Normal state occurs with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state occurs when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.5) occurs with the assertion of the SLP# signal.

While in Stop-Grant State, SMI#, INIT#, and LINT[1:0] are latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event is recognized and serviced upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor responds to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor stays in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor returns to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from the Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input (see Section 2.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK[1] input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BCLK is stopped. It is recommended that the BCLK[1] input be held low during the Deep Sleep State. Stopping of the BCLK[1] input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BCLK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

BCLK[2] provides the clock signal for the processor and on die L2 cache. During AutoHALT Power Down and Stop-Grant states, the processor will process a system bus snoop. The processor does not stop the clock to the L2 cache during AutoHALT Power Down or Stop-Grant states. Entrance into the Halt/Grant Snoop state allows the L2 cache to be snooped, similar to the Normal state.

When the processor is in Sleep and Deep Sleep states, it does not respond to interrupts or snoop transactions. During the Sleep state, the internal clock to the L2 cache is not stopped. During the Deep Sleep state, the internal clock to the L2 cache is stopped. The internal clock to the L2 cache is restarted only after the internal clocking mechanism for the processor is stable (i.e., the processor has re-entered Sleep state).

PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.[2]

2.3 Power and Ground Pins

The operating voltage of the Pentium III processor for the PGA370 socket is the same for the core and the L2 cache; $V_{CC_{CORE}}$. There are four pins defined on the package for voltage identification (VID). These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future processors.

For clean on-chip power and voltage reference distribution, the Pentium III processors in the PGA370 socket have 75 $V_{CC_{CORE}}$, 8 V_{REF} (7 for AGTL platforms), 15 V_{TT}, and 77 V_{SS} (ground) inputs. $V_{CC_{CORE}}$ inputs supply the processor core, including the on-die L2 cache. V_{TT} inputs

1. For processors using AGTL level bus with differential clocking, the deep sleep state is entered by stopping BCLK and BCLK# input.
2. For processors using AGTL level bus with differential clocking this would also include the BCLK# signal as well.

(1.5 V/1.25 V) are used to provide an AGTL+/AGTL termination voltage to the processor, and the V_{REF} inputs are used as the AGTL+/AGTL reference voltage for the processor. Note that not all VTT inputs must be connected to the VTT supply. Refer to Section 5.4 for more details.

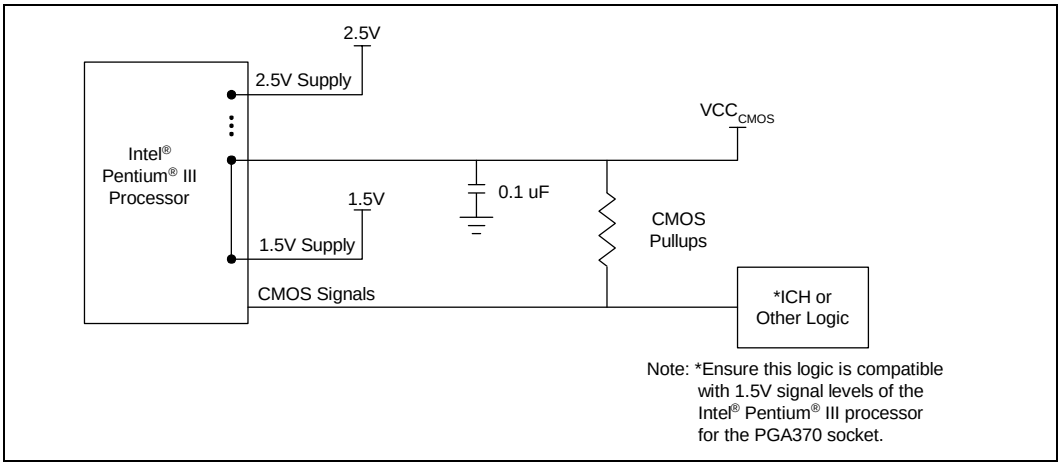
On the motherboard, all VCC_{CORE} pins must be connected to a voltage island (an island is a portion of a power plane that has been divided, or an entire plane). In addition, the motherboard must implement the VTT pins as a voltage island or large trace. Similarly, all GND pins must be connected to a system ground plane.

Three additional power related pins exist on a processors utilizing the PGA370 socket. They are $VCC_{1.5}$, $VCC_{2.5}$ and VCC_{CMOS}.

The VCC_{CMOS} pin provides the CMOS voltage for the pull-up resistors required on the system platform. A 2.5 V source must be provided to the $VCC_{2.5}$ pin and a 1.5 V source must be provided to the $VCC_{1.5}$ pin. The source for $VCC_{1.5}$ must be the same as the one supplying VTT. The processor routes the compatible CMOS voltage source (1.5 V or 2.5 V) through the package and out to the VCC_{CMOS} output pin. Processors based on 0.25 micron technology (e.g., the Celeron processor) utilize 2.5 V CMOS buffers. Processors based on 0.18 micron technology (e.g., the Pentium III processor for the PGA370 socket) utilize 1.5 V CMOS buffers. The signal $VCORE_{DET}$ can be used by hardware on the motherboard to detect which CMOS voltage the processor requires. A $VCORE_{DET}$ connected to VSS within the processor indicates a 1.5 V requirement on VCC_{CMOS}. Refer to Figure 5.

Each power signal must meet the specifications stated in Table 7 on page 28.

Figure 5. Processor VCC_{CMOS} Package Routing



2.3.1 Phase Lock Loop (PLL) Power

It is highly critical that phase lock loop power delivery to the processor meets Intel's requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL. Please refer to the Phase Lock Loop Power section in the **appropriate platform design guide** for the recommended filter specifications.

2.4 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. The fluctuations can cause voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 7. Failure to do so can result in timing violations (in the event of a voltage sag) or a reduced lifetime of the component (in the event of a voltage overshoot). **Unlike SC242 based designs, motherboards utilizing the PGA370 socket must provide high frequency decoupling capacitors on all power planes for the processor.**

2.4.1 Processor VCC_{CORE} and AGTL+ (AGTL) Decoupling

The regulator for the VCC_{CORE} input must be capable of delivering the $dICC_{CORE}/dt$ (defined in Table 7) while maintaining the required tolerances (also defined in Table 7). Failure to meet these specifications can result in timing violations (during VCC_{CORE} sag) or a reduced lifetime of the component (during VCC_{CORE} overshoot).

The processor requires both high frequency and bulk decoupling on the system motherboard for proper AGTL+ (AGTL) bus operation. See the AGTL+ buffer specification in the *Intel® Pentium® II Processor Developer's Manual* for more information. Also, refer to the appropriate platform design guide for recommended capacitor component placement. The minimum recommendation for the processor decoupling is listed below. All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between the VCC_{CORE} and Vss power pins.

1. VCC_{CORE} decoupling - 4.7 µF capacitors in a 1206 package.
2. V_{TT} decoupling - 0.1 µF capacitors in 0603 package.
3. V_{REF} decoupling - 0.1 µF and 0.001 µF capacitors in 0603 package placed near the V_{REF} pins.

For additional decoupling requirements, please refer to the appropriate platform design guide for recommended capacitor component value, quantity and placement.

2.5 Processor System Bus Clock and Processor Clocking

The BCLK input directly controls the operating speed of the system bus interface. All AGTL+/ AGTL system bus timing parameters are specified with respect to the rising edge of the BCLK input.

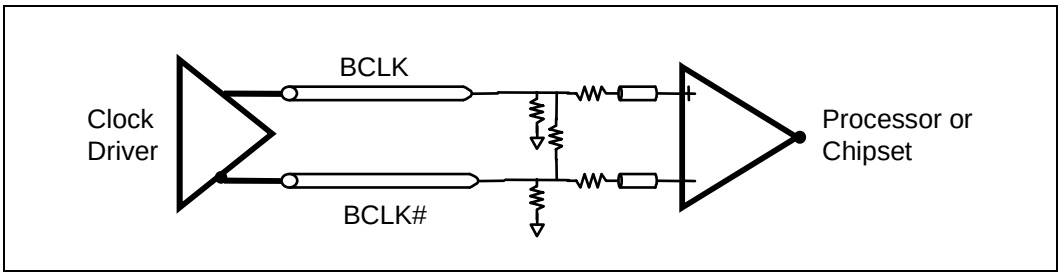
The Coppermine-T processor will implement an auto-detect mechanism that will let the processor use either single-ended or differential signaling for the system bus and processor clocking. The processor checks to see if the signal on pin Y33 is toggling. If this signal is toggling then the processor operates in differential mode. Refer to Figure 6 for a differential clocking example. Resistor values and clock topology are listed in the appropriate platform design guide for a differential implementation.

Note: References to BCLK throughout this document will also imply to its complement signal, BCLK#, in differential implementations and when noted otherwise.

For a differential clock input, all AGTL system bus timing parameters are specified with respect to the crossing point of the rising edge of the BCLK input and the falling edge of the BCLK# input. See the *P6 Family of Processors Hardware Developer's Manual* for further details.

Note: For differential clocking, the reference voltage of the BCLK in the *P6 Family of Processors Hardware Developer's Manual* is re-defined as the crossing point of the BCLK and the BCLK# inputs.

Figure 6. Differential Clocking Example



2.5.1 Mixing Processors of Different Frequencies

In two-way MP (multi-processor) systems, mixing processors of different internal clock frequencies is not supported and has not been validated. Pentium III processors do not support a variable multiplier ratio; therefore, adjusting the ratio setting to a common clock frequency is not valid. However, mixing processors of the same frequency but of different steppings is supported. Details on support for mixed steppings is provided in the *Pentium® III Processor Specification Update*.

Note: Not all Pentium III processors for the PGA370 socket are validated for use in dual processor (DP) systems. Refer to the *Pentium® III Processor Specification Update* to determine which processors are DP capable.

2.6 Voltage Identification

There are four voltage identification pins on the PGA370 socket. These pins can be used to support automatic selection of $V_{CC_{CORE}}$ voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor core. The VID pins are needed to cleanly support voltage specification variations on current and future processors. VID[3:0] are defined in Table 2. A ‘1’ in this table refers to an open pin and a ‘0’ refers to a short to ground. The voltage regulator or VRM must supply the voltage that is requested or disable itself.

To ensure a system is ready for current and future processors, the range of values in **bold** in Table 2 should be supported. A smaller range will risk the ability of the system to migrate to a higher performance processor and/or maintain compatibility with current processors.

Table 2. Voltage Identification Definition [1, 2]

VID3	VID2	VID1	VID0	$V_{CC_{CORE}}$
1	1	1	1	**1.30**
1	1	1	0	**1.35**
1	1	0	1	**1.40**
1	1	0	0	**1.45**
1	0	1	1	**1.50**
1	0	1	0	**1.55**
1	0	0	1	**1.60**[3]
1	0	0	0	**1.65**[3]
0	1	1	1	**1.70**[3]
0	1	1	0	**1.75**[3]
0	1	0	1	**1.80** [3]
0	1	0	0	**1.85** [3]
0	0	1	1	**1.90** [3]
0	0	1	0	**1.95** [3]
0	0	0	1	**2.00** [3]
0	0	0	0	**2.05** [3]
1	1	1	1	**No Core**

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on baseboard.
3. To ensure a system is ready for the Pentium III and Celeron processors, the values in **BOLD** in Table 2 should be supported.

Note that the '1111' (all opens) ID can be used to detect the absence of a processor core in a given socket as long as the power supply used does not affect these lines. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

The VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator only if required by the regulator or external logic monitoring the VID[3:0] signals. The power source chosen must be guaranteed to be stable whenever the supply to the voltage regulator is stable. This will prevent the possibility of the processor supply going above the specified $V_{CC_{CORE}}$ in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. A resistor of greater than or equal to 10 kΩ may be used to connect the VID signals to the converter input. Note that no changes have been made to the physical connector or pin definitions between the Intel-enabled VRM 8.2 and VRM 8.4 specifications.

Note: VRM 8.5 specification uses five VID pin assignments VID[3:0, 25mV] and it is not compatible with VRM 8.4. Some Pentium III processors with CPUID 068xh are capable of supporting both VRM 8.4 and VRM 8.5 specifications. Please refer to the *Pentium III Specification Update* for a listing of processors that support both VRM specifications.

2.7 Processor System Bus Unused Pins

All RESERVED pins must remain unconnected unless specifically noted. Connection of these pins to $V_{CC_{CORE}}$, V_{REF}, V_{SS}, V_{TT}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 5.4 for a pin listing of the processor and the location of each RESERVED pin.

PICCLK must be driven with a valid clock input and the PICD[1:0] signals must be pulled-up to $V_{CC_{CMOS}}$ even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD signal.

For reliable operation, always connect unused inputs or bidirectional signals to their deasserted signal level. The pull-up or pull-down resistor values are system dependent and should be chosen such that the logic high (V_{IH}) and logic low (V_{IL}) requirements are met. See Table 10 and Table 11 for DC specifications of non-AGTL+/AGTL signals.

Unused AGTL+ (or AGTL) inputs must be properly terminated to V_{TT} on PGA370 socket motherboards which support the Celeron and the Pentium III processors. For designs that intend to only support the Pentium III processor, unused AGTL+ inputs will be terminated by the processor's on-die termination resistors and thus do not need to be terminated on the motherboard. However, RESET# must always be terminated on the motherboard as the Pentium III processor for the PGA370 socket does not provide on-die termination of this input.

For unused CMOS inputs, active low signals should be connected through a pull-up resistor to $V_{CC_{CMOS}}$ and meet V_{IH} requirements. Unused active high CMOS inputs should be connected through a pull-down resistor to ground (V_{SS}) and meet V_{IL} requirements. Unused CMOS outputs can be left unconnected. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

2.8 Processor System Bus Signal Groups

To simplify the following discussion, the processor system bus signals have been combined into groups by buffer type. All P6 family processor system bus outputs are open drain and require a high-level source provided termination resistors. However, the Pentium III processor for the PGA370 socket includes on-die termination. **Motherboard designs that also support Celeron processors in the PPGA package will need to provide AGTL+ termination on the system motherboard as well. Platform designs that support dual processor configurations will need to provide AGTL+ termination, via a termination package, in any socket not populated with a processor. Please refer to the *Pentium III Processor Specification Update* for a complete listing of the processors that support the AGTL and AGTL+ specifications. Note that AGTL platforms do not support the Celeron processor in the PPGA package.**

Both AGTL+ and AGTL input signals have differential input buffers which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V while AGTL output signals require termination to 1.25 V. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

The PWRGOOD, BCLK, and PICCLK inputs can each be driven from ground to 2.5 V. Other CMOS inputs (A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SMI, SLP#, and STPCLK#) are only 1.5 V tolerant and must be pulled up to $V_{CC_{CMOS}}$. The CMOS, APIC, and TAP outputs are open drain and must be pulled high to $V_{CC_{CMOS}}$. This ensures correct operation for current Pentium III and Celeron processors.

The groups and the signals contained within each group are shown in Table 3 and Table 4. Refer to Section 7.0 for a description of these signals.

Table 3. System Bus Signal Groups [1]

Group Name	Signals
AGTL+ Input	BPRI#, BR1#[7], DEFER#, RESET# [6],RESET2#, RS[2:0]#, RSP#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[2], D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input[3]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SLP#, SMI#, STPCLK#
CMOS Input[4]	PWRGOOD
CMOS Output[3]	FERR#, IERR#, THERMTRIP#
System Bus Clock[4]	BCLK
APIC Clock[4]	PICCLK
APIC I/O[3]	PICD[1:0]
Power/Other[5]	BSEL[1:0], CLKREF, CPUPRES#, EDGCTRL, PLL[2:1], RESET2#, SLEWCTRL, THERMDN, THERMDP, RTTCTRL[8], $V_{CORE_{DET}}$, VID[3:0], $V_{CC_{1.5}}$, $V_{CC_{2.5}}$, $V_{CC_{CMOS}}$, $V_{CC_{CORE}}$, V_{REF}, V_{SS}, V_{TT}, Reserved

NOTES:
1. See Section 7.0 for information on the these signals.
2. The BR0# pin is the only BREQ# signal that is bidirectional. See Section 7.0 for more information. The internal BREQ# signals are mapped onto the BR[1:0]# pins after the agent ID is determined.
3. These signals are specified for $V_{CC_{CMOS}}$ (1.5 V for the Pentium III processor) operation.
4. These signals are 2.5 V tolerant.
5. $V_{CC_{CORE}}$ is the power supply for the processor core and is described in Section 2.6.
   VID[3:0] is described in Section 2.6.
   V_{TT} is used to terminate the system bus and generate V_{REF} on the motherboard.
   V_{SS} is system ground.
   $V_{CC_{1.5}}$, $V_{CC_{2.5}}$, $V_{CC_{CMOS}}$ are described in Section 2.3.
   BSEL[1:0] is described in Section 2.8.2 and Section 7.0.
   All other signals are described in Section 7.0.
6. RESET# must always be terminated to V_{TT} on the motherboard, on-die termination is not provided for this signal.
7. This signal is not supported by all processors. Refer to the *Pentium® III Processor Specification Update* for a complete listing of processors that support this pin.
8. This signal is used to control the value of the processor on-die termination resistance. Refer to the platform design guide for the recommended pull-down resistor value.

Table 4. System Bus Signal Groups (AGTL)[1] (Sheet 1 of 2)

Group Name	Signals
AGTL Input[9]	BPRI#, BR1#[7], DEFER#, RESET#[6], RSP#, TRDY#, RS[2:0]#
AGTL Output[9]	PRDY#
AGTL I/O[9]	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[2], D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#,
CMOS Input[3]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SLP#, SMI#, STPCLK#
CMOS Input (1.8 V)	PWRGOOD
CMOS Output	FERR#[3], IERR#[3], THERMTRIP#[3], VID[3:0][13], BSEL[1:0][13]

Table 4. System Bus Signal Groups (AGTL)[1] (Sheet 2 of 2)

Group Name	Signals
System Bus Clock[10, 12] (1.25 V/2.5 V)	BCLK, BCLK0#
APIC Clock (2.0 V)	PICCLK[11]
APIC I/O[3]	PICD[1:0]
Power/Other[5]	BSEL[1:0], CLKREF[10], CPUPRES#, EDGCTRL, PLL[2:1], RESET2#, SLEWCTRL, THERMDN, THERMDP, RTTCTRL[8], $VCORE_{DET}$, VID[3:0], $VCC_{1.5}$, $VCC_{2.5}$, VCC_{CMOS}, VCC_{CORE}, V_{REF}, VSS, VTT, Reserved

NOTES:
1. See Section 7.0 for information on the these signals.
2. The BR0# pin is the only BREQ# signal that is bidirectional. See Section 7.0 for more information. The internal BREQ# signals are mapped onto the BR[1:0]# pins after the agent ID is determined.
3. These signals are specified for VCC_{CMOS} (1.5 V for the Pentium III processor) operation.
4. These signals are 2.5 V tolerant.
5. VCC_{CORE} is the power supply for the processor core and is described in Section 2.6.
   VID[3:0] is described in Section 2.6.
   VTT is used to terminate the system bus and generate V_{REF} on the motherboard.
   VSS is system ground.
   $VCC_{1.5}$, $VCC_{2.5}$, VCC_{CMOS} are described in Section 2.3.
   BSEL[1:0] is described in Section 2.8.2 and Section 7.0.
   All other signals are described in Section 7.0.
6. RESET# must always be terminated to VTT on the motherboard, on-die termination is not provided for this signal.
7. This signal is not supported by all processors. Refer to the *Pentium® III Processor Specification Update* for a complete listing of processors that support this pin.
8. This signal is used to control the value of the processor on-die termination resistance. Refer to the platform design guide for the recommended pull-down resistor value.
9. These signals are also classified as AGTL. Refer to the *Pentium® III Processor Specification Update* for a complete listing of processors that support the AGTL and AGTL+ specifications.
10. For differential clock systems, the CLKREF pin becomes BCLK#.
11. For the Coppermine-T differential clock, this signal has been redefined to 2.0 V tolerant.
12. 1.25 V signal for Differential clock application and 2.5 V for Single-ended clock application.
13. This signal is 3.3 V.

2.8.1 Asynchronous vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, Clock, APIC, and TAP signals can be applied asynchronously to BCLK. All APIC signals are synchronous to PICCLK.

2.8.2 System Bus Frequency Select Signals (BSEL[1:0])

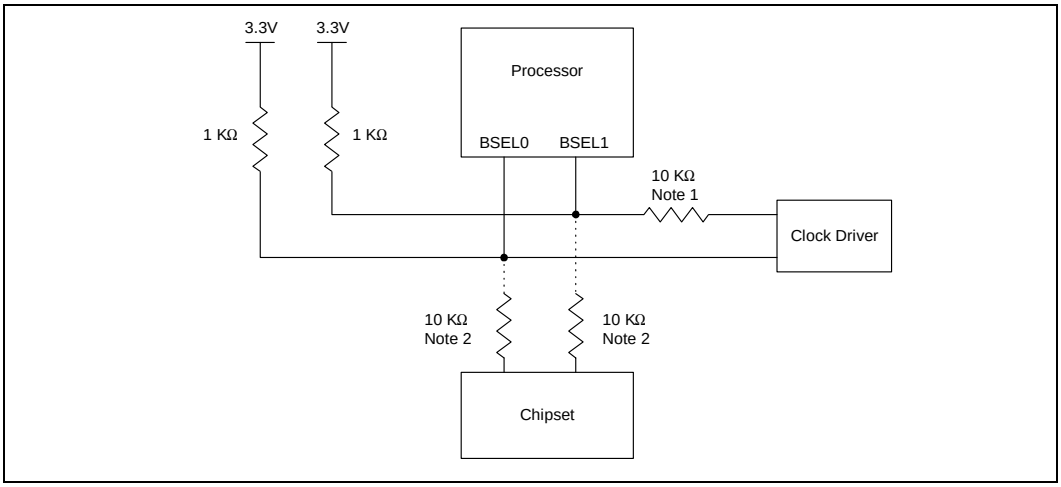
These signals are used to select the system bus frequency for the processor. The BSEL signals are also used by the chipset and system bus clock generator. Table 5 defines the possible combinations of the signals and the frequency associated with each combination. The frequency selection is determined by the processor(s) and driven out to the chipset and clock generator. All system bus agents must operate at the same frequency determined by the processor. **The Pentium lll processor for the PGA370 socket operates at 100 MHz or 133 MHz system bus frequency; 66 MHz system bus operation is not supported**. Individual processors will only operate at their specified front side bus (FSB) frequency, either 100 MHz or 133 MHz, not both. Over or under-clocking the system bus frequency outside the specified rating marked on the package is not recommended.

On motherboards that support operation at either 100 MHz or 133 MHz, the BSEL1 signal must be pulled up to a logic high by a resistor located on the motherboard and provided as a frequency selection signal to the clock driver/synthesizer. This signal can also be incorporated into RESET# logic on the motherboard if only 133 MHz operation is supported (thus forcing the RESET# signal to remain active as long as the BSEL1 signal is low.

The BSEL0 signal will float from the processor and should be pulled up to a logic high by a resistor located on the motherboard. The BSEL0 signal can be incorporated into RESET# logic on the motherboard if 66 MHz operation is unsupported, as demonstrated in Figure 7. Refer to the appropriate clock synthesizer design guidelines and platform design guide for more details on the bus frequency select signals.

In a 2-way MP system design, these BSEL[1:0] signals must connect the pins of both processors.

Figure 7. BSEL[1:0] Example for a 100/133 MHz or 100 MHz Only System Design



NOTES:
1. Some clock drivers may require a series resistor on their BSEL1 input.
2. Some chipsets may connect to the BSEL[1:0] signals and require a series resistor. See the appropriate platform design guide for implementation details.

Table 5. Frequency Select Truth Table for BSEL[1:0]

BSEL1	BSEL0	Frequency
0	0	66 MHz (unsupported)
0	1	100 MHz
1	0	Reserved
1	1	133 MHz

2.9 Maximum Ratings

Table 6 contains processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables in Section 2.10 through Section 2.12. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
Vcc_{CORE} and V_{TT}	Processor core voltage and termination supply voltage with respect to V_{SS}	–0.5	2.1	V	
Vin_{AGTL}	AGTL+ buffer input voltage	V_{TT} - 2.18	2.18	V	1, 2
$Vin_{CMOS}^{1.5}$	CMOS buffer DC input voltage with respect to V_{SS}	V_{TT} - 2.18	2.18	V	1, 2, 3
$Vin_{CMOS}^{2.5}$	CMOS buffer DC input voltage with respect to V_{SS}	-0.58	3.18	V	4
I_{VID}	Max VID pin current	-0.3	5	mA	
$I_{CPUPRES\#}$	Max CPUPRES# pin current		5	mA	

NOTES:
1. Input voltage can never exceed V_{SS} + 2.18 V.
2. Input voltage can never go below V_{TT} - 2.18 V.
3. Parameter applies to CMOS (except BCLK, PICCLK, and PWRGOOD) and APIC bus signal groups only.
4. Parameter applies to CMOS signals BCLK, PICCLK, and PWRGOOD only.

2.10 Processor DC Specifications

The processor DC specifications in this section are defined at the PGA370 socket pins (bottom side of the motherboard). See Section 7.0 for the processor signal descriptions and Section 5.4 for the signal listings.

Most of the signals on the processor system bus are in the AGTL+ (AGTL) signal group. These signals are specified to be terminated to 1.5 V for AGTL+ or 1.25 V for AGTL. The DC specifications for these signals are listed in Table 9 on page 34.

To allow connection with other devices, the clock, CMOS, and APIC signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in Table 11 on page 35.

Table 7 through Table 12 list the DC specifications for the Pentium III processor for the PGA370 socket. Specifications are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 7. Voltage and Current Specifications [1, 2] (Sheet 1 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
$V_{CC_{CORE}}$	V_{CC} for Processor Core	500E MHz	0x681		1.60		V	3,4
			0x683		1.60			3,4
			0x686		n/a			3,4
		533EB MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		n/a			3,4
		550E MHz	0x681		1.60			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
		600E MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4
		600EB MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
		650 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
		667 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
		700 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4
		733 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4
		750 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4

Table 7. Voltage and Current Specifications [1, 2] (Sheet 2 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
$V_{CC_{CORE}}$	V_{CC} for Processor Core	800 MHz	0x681		1.65		V	3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
		800EB MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4
		850 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4
		866 MHz	0x681		1.65			3,4
			0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4
		900 MHz	0x686		1.70			3,4
			0x68A		1.75			3,4
		933 MHz	0x683		1.65			3,4
			0x686		1.70			3,4
			0x68A		1.75			3,4,20
		1 GHz	0x68A		1.75			3,4
		1B GHz	0x686		1.70			3,4
			0x686		1.76			3,4,18,19
			0x68A		1.75			3,4,20
		1.10 GHz	0x68A		1.75			3,4
		1.13 GHz	0x68A		1.75			3,4

Table 7. Voltage and Current Specifications [1, 2] (Sheet 3 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
V_{TT}	Static AGTL+ bus termination voltage			1.455	1.50	1.545	V	1.5 ±3% [5,16]
	Static AGTL bus termination voltage			1.213	1.25	1.288	V	1.25 ±3% [5,16,17]
V_{TT}	Transient AGTL+ bus termination voltage			1.365	1.50	1.635	V	1.5 ±9% [5]
	Transient AGTL bus termination voltage			1.138	1.25	1.363	V	1.25 ±9% [5,17]
$Vcc_{1.5}$	Static AGTL+ bus termination voltage			1.455	1.50	1.545	V	1.5 ±3%
V_{REF}	AGTL+ input reference voltage			-2%	2/3 V_{TT}	+2%	V	±2%, 7
V_{CLKREF}	CLKREF input reference voltage			1.169	1.25	1.331	V	±6.5%, 15
Baseboard $V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at the PGA370 socket pins			–0.080 0.001		0.040 0.100	V	6 18, 19
Baseboard $V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at the PGA370 socket pins			–0.130 –0.110 –0.025		0.080 0.080 0.130	V	6 17 18, 19

Table 7. Voltage and Current Specifications [1, 2] (Sheet 4 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
$I_{CC_{CORE}}$	I_{CC} for processor core	500E MHz	0x683			10.0	A	3, 8, 9
		600E MHz	0x686			12.0		3, 8, 9
			0x68A			12.6		3, 8, 9
		600EB MHz	0x686			12.0		3, 8, 9
		650 MHz	0x686			13.0		3, 8, 9
		667B MHz	0x686			13.3		3, 8, 9
		700 MHz	0x686			14.0		3, 8, 9
			0x68A			14.8		3, 8, 9
		733B MHz	0x686			14.6		3, 8, 9
			0x68A			15.4		3, 8, 9
		750 MHz	0x686			15.0		3, 8, 9
			0x68A			15.7		3, 8, 9
		800 MHz	0x686			16.0		3, 8, 9
		800EB MHz	0x686			16.0		3, 8, 9
			0x68A			16.6		3, 8, 9
		850 MHz	0x686			16.2		3, 8, 9
			0x68A			17.3		3, 8, 9
		866 MHz	0x686			16.3		3, 8, 9
			0x68A			17.6		3, 8, 9
		900 MHz	0x686			17.0		3, 8, 9
			0x68A			18.4		3, 8, 9
		933 MHz	0x686			17.7		3, 8, 9
			0x68A			18.8		3, 8, 9,20
		1 B GHz	0x686			19.4		3, 8, 9
			0x68A			20.2		3, 8, 9, 20
		1 GHz	0x68A			20.2		3, 8, 9
		1.10 GHz	0x68A			22.6		3, 8, 9
		1.13 GHz	0x68A			22.6		3, 8, 9,20

Table 7. Voltage and Current Specifications [1, 2] (Sheet 5 of 5)

Symbol	Parameter	Processor		Min	Typ	Max	Unit	Notes
		Core Freq	CPUID					
$I_{CC_{CMOS}}$	I_{CC} for $V_{CC_{CMOS}}$					250	mA	
I_{CLKREF}	CLKREF voltage supply current					60	µA	
I_{VTT}	Termination voltage supply current					2.7	A	10
I_{SGnt}	I_{CC} Stop-Grant for processor core					6.9	A	8, 11
I_{SLP}	I_{CC} Sleep for processor core					6.9	A	8
I_{DSLP}	I_{CC} Deep Sleep for processor core					6.6	A	8
$dICC_{CORE}/dt$	Power supply current slew rate					240	A/µs	12, 13, 14
dI_{VTT}/dt	Termination current slew rate					8	A/µs	12, 13, See Table 12

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All specifications in this table apply only to the Pentium III processor. For motherboard compatibility with the Celeron processor, see the *Intel® Celeron™ Processor Datasheet*.
3. Vcc_{CORE} and Icc_{CORE} supply the processor core and the on-die L2 cache.
4. Use the "typical voltage" specification with the "tolerance specifications" to provide correct voltage regulation to the processor.
5. V_{TT} and $Vcc_{1.5}$ must be held to 1.5 V ±9% while the AGTL+ bus is active. It is required that V_{TT} and $Vcc_{1.5}$ be held to 1.5 V ±3% while the processor system bus is static (idle condition). The ±3% range is the required design target; ±9% will come from the transient noise added. This is measured at the PGA370 socket pins on the bottom side of the baseboard.
6. **These are the tolerance requirements, across a 20 MHz frequency bandwidth, measured at the processor socket pin on the soldered-side of the motherboard.** $V_{CC_{CORE}}$ must return to within the static voltage specification within 100 µs after a transient event; see the *VRM 8.4 DC-DC Converter Design Guidelines* for further details.
7. V_{REF} should be generated from V_{TT} by a voltage divider of 1% resistors or 1% matched resistors. Refer to the Intel® *Pentium® II Processor Developer's Manual* for more details on V_{REF}.
8. Maximum I_{CC} is measured at V_{CC} typical voltage and under a maximum signal loading conditions.
9. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

$$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times (Vcc_{CORE\_TYP} - Vcc_{CORE\_STATIC\_TOLERANCE}) / Vcc_{CORE\_TYP}$$

10. The current specified is the current required for a single processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
11. The current specified is also for AutoHALT state.
12. Maximum values are specified by design/characterization at nominal Vcc_{CORE}.
13. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
14. dIcc/dt specifications are measured and specified at the PGA370 socket pins.
15. CLKREF must be held to 1.25 V ±6.5%. This tolerance accounts for a ±5% power supply and ±1% resistor divider tolerance. It is recommended that the motherboard generate the CLKREF reference from either the 2.5 V or 3.3 V supply. V_{TT} should not be used due to risk of AGTL+ switching noise coupling to this analog reference.
16. Static voltage regulation includes: DC output initial voltage set point adjust, Output ripple and noise, Output load ranges specified in the tables above.
17. This specification applies to PGA370 processors operating at frequencies of 933 MHz or higher.

18. This specification only applies to 1B GHz S-spec #: SL4WM. This part has a VID request of 1.70 V, however the processor should be supplied 1.76 V at the PGA Vcc pin by the Voltage Regulator Circuit or VRM.
19. This specification applies only to 1B GHz S-spec #: SL4WM. This value is 60 mV offset from the standard specification and more at the Minimum specification. These tolerances are measured from a 1.70 V base, while Vcc supplied is 1.76 V.
20. This processor exists in both FC-PGA and FC-PGA2.

2.10.1 ICC Slew Rate Specifications

This section contains typical current slew rate data for processors covered by this design guideline. Actual slew rate values and wave-shapes may vary slightly depending on the type and size of decoupling capacitors used in a particular implementation.

Figure 8. Slew Rate (23A Load Step)

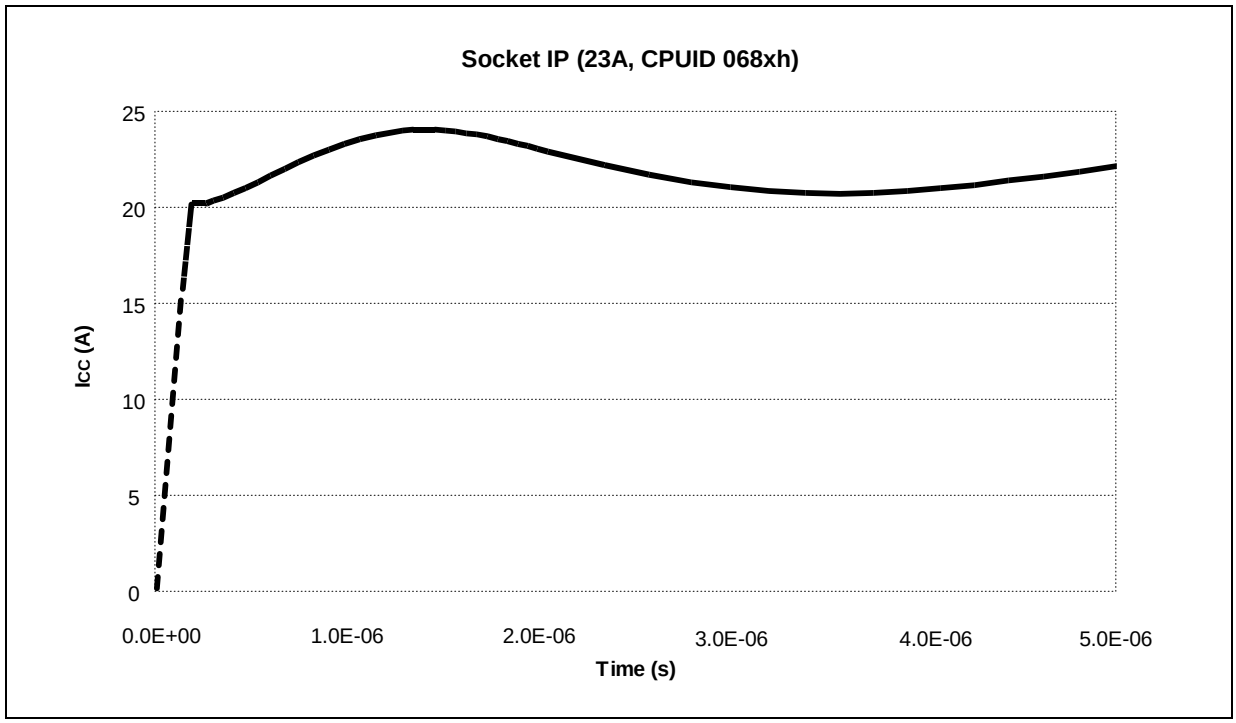


Table 8. PL Slew Rate Data (23A) (Sheet 1 of 2)

Time (µs)	Icc (A)
0.1	9.55
0.15	14.4
0.5	20.85
1	23.04
1.5	23.44
2	23.28
2.5	22.32
3	21.63
3.5	21.45
4	21.63

Table 8. PL Slew Rate Data (23A) (Sheet 2 of 2)

Time (µs)	Icc (A)
4.5	21.88
5	22.01

Table 9. AGTL / AGTL+ Signal Groups DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.150	V_{REF} - 0.200	V	6
V_{IH}	Input High Voltage	V_{REF} + 0.200	V_{TT}	V	2, 3, 6
Ron	Buffer On Resistance		16.67	Ω	5
I_L	Leakage Current for inputs, outputs, and I/O		±100	µA	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. All inputs, outputs, and I/O pins must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 12 on page 36.
4. ($0 \le V_{IN} \le 1.5$ V +3%) and ($0 \le V_{OUT} \le 1.5$ V+3%).
5. Refer to the processor I/O Buffer Models for I/V characteristics.
6. Steady state input voltage must not be above V_{SS} + 1.65 V or below V_{TT} - 1.65 V.

Table 10. Non-AGTL+ Signal Group DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL_{1.5}}$	Input Low Voltage	-0.150	V_{CMOS_REF} - 0.200	V	9
$V_{IL_{2.5}}$	Input Low Voltage	-0.58	0.700	V	5, 8
$V_{IH_{1.5}}$	Input High Voltage	V_{CMOS_REF} + 0.200	1.5	V	6, 9
$V_{IH_{2.5}}$	Input High Voltage	2.000	3.18	V	5, 8
V_{OL}	Output Low Voltage		0.400	V	2
R_{on}			35		2
V_{OH}	Output High Voltage		1.5	V	7, 9, All outputs are open-drain
I_{OL}	Output Low Current	9		mA	
I_{LI}	Input Leakage Current		±100	µA	3, 6
I_{LO}	Output Leakage Current		±100	µA	4, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. Parameter measured at 9 mA (for use with TTL inputs).
3. ($0 \le V_{IN} \le 2.5$ V +5%).
4. ($0 \le V_{OUT} \le 2.5$ V +5%).
5. For BCLK specifications, refer to Table 24 on page 51.
6. ($0 \le V_{IN} \le 1.5$ V +3%).
7. ($0 \le V_{OUT} \le 1.5$ V +3%).
8. Applies to non-AGTL signals except BCLK, PICCLK, and PWRGOOD.
9. Applies to non-AGTL signals **except** BCLK, PICCLK, and PWRGOOD.

Table 11. Non-AGTL Signal Group DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL_{1.5}}$	Input Low Voltage	-0.150	V_{CMOS_REF} - 0.300	V	7, 8
$V_{IL_{2.5}}$	Input Low Voltage	-0.58	0.700	V	4, 6
$V_{IH_{1.5}}$	Input High Voltage	V_{CMOS_REF} + 0.200	1.5	V	5, 7
$V_{IH_{2.5}}$	Input High Voltage	2.000	3.18	V	4, 6
V_{OL}	Output Low Voltage		0.300	V	2
R_{on}			35		2
V_{OH}	Output High Voltage		1.5	V	5, 7, All outputs are open-drain
I_{OL}	Output Low Current	9		mA	
I_{LI}	Input Leakage Current		±100	µA	3, 5
I_{LO}	Output Leakage Current		±100	µA	3, 5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. Parameter measured at 9 mA (for use with TTL inputs).
3. ($0 \le V_{IN} \le 2.5$ V +5%); ($0 \le V_{OUT} \le 2.5$ V +5%).
4. For BCLK specifications, refer to Table 24 on page 51.
5. ($0 \le V_{IN} \le 1.5$ V +3%); ($0 \le V_{OUT} \le 1.5$ V +3%).
6. Applies to non-AGTL+ signals **except** BCLK, PICCLK, and PWRGOOD.
7. Applies to non-AGTL+ signals **except** BCLK, PICCLK, and PWRGOOD.
8. For Coppermine-T differential clocking, the input low voltage is (VCMOS_REF - 0.300)V.

2.11 AGTL / AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to VTT. These termination resistors are placed electrically between the ends of the signal traces and the VTT voltage supply and generally are chosen to approximate the system platform impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Refer to the appropriate platform design guide for more information

Table 12 below lists the nominal specification for the AGTL+ termination voltage (VTT). The AGTL+ reference voltage (V_{REF}) is generated on the system motherboard and should be set to 2/3 VTT for the processor and other AGTL+ logic. It is important that the baseboard impedance be specified and held to a ±15% tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on the AGTL+ buffer specification, see the *Intel® Pentium® II Processor Developer's Manual* and AP-585, *Intel® Pentium® II Processor AGTL+ Guidelines*.

Table 12. Processor AGTL+ Bus Specifications [1, 2]

Symbol	Parameter	Min	Typ	Max	Units	Notes
VTT	Bus Termination Voltage		1.50		V	3
On-die R_{TT}	Termination Resistor	40		130	Ω	4
V_{REF}	Bus Reference Voltage	0.950	2/3 VTT	1.05	V	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. Pentium III processors for the PGA370 socket contain AGTL+ termination resistors on the processor die, except for the RESET# input.
3. VTT and $Vcc_{1.5}$ must be held to 1.5 V ±9%. It is required that VTT and $Vcc_{1.5}$ be held to 1.5 V ±3% while the processor system bus is idle (static condition). This is measured at the PGA370 socket pins on the bottom side of the baseboard.
4. The value of the on-die R_{TT} is determined by the resistor value measured by the RTTCTRL signal pin. See Section 7.0 for more details on the RTTCTRL signal. Refer to the recommendation guidelines for the specific chipset/processor combination.
5. V_{REF} is generated on the motherboard and should be 2/3 VTT ±2% nominally. Insure that there is adequate V_{REF} decoupling on the motherboard.

Table 13. Processor AGTL Bus Specifications [1, 2]

Symbol	Parameter	Min	Typ	Max	Units	Notes
VTT	Bus Termination Voltage	1.14	1.25	1.308	V	3
On-die R_{TT}	Termination Resistor	50[6]	56, 68	115	Ω	4, 7
V_{REF}	Bus Reference Voltage	2/3 VTT - 2%	2/3 VTT	2/3 VTT + 2%	V	5

NOTES:
1. Specifications in this table do not apply to Pentium III processors at all frequencies. Please refer to the *Intel® Pentium® III Processor Specification Update* for a complete listing on the processors that support the AGTL specification.
2. Pentium III processors for the PGA370 socket contain AGTL termination resistors on the processor die, except for the RESET# input.
3. VTT must be held to 1.25 V ±9%. It is required that VTT be held to 1.25 V ±3% while the processor system bus is idle (static condition). This is measured at the PGA370 socket pins on the bottom side of the baseboard.
4. The value of the on-die R_{TT} is determined by the resistor value measured by the RTTCTRL signal pin. The on-die R_{TT} has a resistance tolerance of ±15%. See Section 7.0 for more details on the RTTCTRL signal. Refer to the recommendation guidelines for the specific chipset/processor combination.
5. V_{REF} is generated on the motherboard and should be 2/3 VTT ±2% nominally. Insure that there is adequate V_{REF} decoupling on the motherboard.
6. For the Coppermine-T differential clock platform, the on-die RTT min should be 50 Ω.
7. Coppermine-T UP platforms require a 56Ω resistor and Coppermine-T DP platforms require a 68Ω resistor. Tolerance for the on-die R_{TT} is ±10% for 56Ω and 68Ω resistors and ±15% for 100 Ω resistors

2.12 System Bus AC Specifications

The processor system bus timings specified in this section are defined at the socket pins on the bottom of the motherboard. Unless otherwise specified, timings are tested at the processor pins during manufacturing. Timings at the processor pins are specified by design characterization. See Section 7.0 for the processor signal definitions.

Table 14 through Table 20 list the AC specifications associated with the processor system bus. These specifications are placed into the following categories: Table 14 and Table 15 contain the system bus clock specifications, Table 16 contains the AGTL+/AGTL specifications, Table 17 contains the CMOS signal group specifications, Table 18 contains timings for the reset conditions, Table 19 and covers APIC bus timing, and Table 20 covers power on timing.

All processor system bus AC specifications for the AGTL+/AGTL signal group are relative to the rising edge of the BCLK input. All AGTL+/AGTL timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium III processor in the FC-PGA package in Viewlogic* XTK/XNS* model format (formerly known as QUAD format) and IBIS * 3.1 format as the *Pentium III Processor for the PGA370 Socket I/O Buffer Models* (Electronic Format).

AGTL and AGTL+ layout guidelines are also available in the appropriate platform design guide.

Care should be taken to read all notes associated with a particular timing parameter.

2.12.1 I/O Buffer Model

An electronic copy of the I/O Buffer Model for the AGTL+ and CMOS signals is available at Intel's Developer's Website (http://developer.intel.com). The model is for use in single processor designs and assumes the presence of motherboard R_{TT} values as described in Table 12 on page 36.

Table 14. System Bus AC Specifications (SET Clock)[1, 2]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		100.00 133.33		MHz		4
T1: BCLK Period	10.0 7.5			ns	9	4, 5, 10 4, 5, 11
T2: BCLK Period Stability			±250 ±250	ps		6, 7, 10 6, 7, 11
T3: BCLK High Time	2.5 1.4			ns	9	9, 10 9, 11
T4: BCLK Low Time	2.4 1.4			ns	9	9, 10 9, 11
T5: BCLK Rise Time	0.4		1.6	ns	9	3, 8
T6: BCLK Fall Time	0.4		1.6	ns	9	3, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor pins.

3. Not 100% tested. Specified by design characterization as a clock driver requirement.
4. The internal core clock frequency is derived from the processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Individual processors will only operate at their specified system bus frequency, either 100 MHz or 133 MHz, not both.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation. See the appropriate clock synthesizer/driver specification for details.
6. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25 V at the processor pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
7. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the appropriate clock synthesizer/driver specification for details
8. BCLK Rise time is measure between 0.5 V–2.0 V. BCLK fall time is measured between 2.0 V–0.5 V.
9. BCLK high time is measured as the period of time above 2.0 V. BCLK low time is measured as the period of time below 0.5 V.
10. This specification applies to Pentium III processors operating at a system bus frequency of 100 MHz.
11. This specification applies to Pentium III processors operating at a system bus frequency of 133 MHz

Table 15. System Bus Timing Specifications (Differential Clock)[1, 11, 12]

Parameter	133 MHz		100 MHz		Units	Notes
	Min	Max	Min	Max		
Clock Period—Average	7.5	7.7	10.0	10.2	ns	2, 9, 10
Instantaneous Minimum Clock Period	7.30		9.8		ns	2, 9, 10
CLK Differential Rise Time	175	550	175	467	ps	1, 3
CLK Differential Fall Time	175	550	175	467	ps	1, 3
Waveform Symmetry		325		325	ps	4
Differential Cycle to Cycle Jitter		200		200	ps	1, 5
Differential Duty Cycle	45%	55%	45%	55%		1
Rising Edge Ring Back	0.35		0.35		V	1, 6
Falling Edge Ring Back		–0.35		–0.35	V	1, 6
Cross Point at 1V	0.51	0.76	0.51	0.76	V	7
Input High Voltage	0.92	1.45	0.92	1.45	V	8
Input Low Voltage	–0.2	0.35	–0.2	0.35	V	8

NOTES:
1. Measurement taken from differential waveform, defined as BCLK - BCLK#.
2. Period is defined from one rising 0 V-crossing to the next.
3. Measurement taken from differential waveform, voltage range from -0.35 V to +0.35 V.
4. Measurement taken from common mode waveform, measure rise/fall time from 0.41 V to 0.86 V. Rise/fall time matching is defined as "the instantaneous difference between maximum BCLK rise (fall) and minimum BCLK# fall (rise) time, or minimum BCLK rise (fall) and maximum BCLK# fall (rise) time. "This parameter is designed to guard waveform symmetry.
5. Period difference measured around 0 V-crossings; measurement taken from differential waveform.
6. The rising and falling edge ringback voltage specified is the minimum (rising) or them maximum (falling) voltage, the differential waveform can go after passing Vih_diff (rising) or Vil_diff (falling)
7. Measured in absolute voltage, i.e. single-ended measurement. Includes every cross point for both rise and fall of BCLK.
8. Input high or input low voltage range measured in absolute voltage, i.e. single-ended measurement.
9. The internal Core clock frequency is derived from the processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Individual processors will only operate at their specified system bus frequency 133 MHz. Table 16 shows supported ratios for each processor
10. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 pF to 20 pF. The jitter must be accounted for as a component of BCLK timing skew between devices.
11. AC parameters are measured at the processor pins.
12. BCLK/BCLK# must rise/fall monotonically between Vil and Vih.

Table 16. System Bus AC Specifications (AGTL+ or AGTL Signal Group)[1, 2, 3, 13]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.40	3.25	ns	11	4, 10, 11
T8: AGTL+ Input Setup Time	1.20 0.95		ns ns	12 12	5, 6, 7, 10 5, 6, 7, 11, 12
T9: AGTL+ Input Hold Time	1.00		ns	12	8, 10
T10: RESET# Pulse Width	1.00		ms	13	6, 9, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. These specifications are tested during manufacturing.
3. All timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor pins (for AGTL, the timings are referenced to the rising edge of BCLK and the falling edge of BCLK# at the processor pins). All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00 V (2/3 V_{TT} for AGTL) at the processor pins.
4. Valid delay timings for these signals are specified into 50 Ω to 1.5 V, V_{REF} at 1.0 V ±2% and with 56 Ω on-die R_{TT}. For AGTL platforms, the valid delay timings are specified into 50 Ω to 1.25 V, V_{REF} at 2/3 V_{TT} ±2% and with 56 Ω on-die R_{TT}.
5. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously. For 2-way MP systems, RESET# should be synchronous.
7. Specification is for a minimum 0.40 V swing from V_{REF} - 200 mV to V_{REF} + 200 mV. This assumes an edge rate of 0.3V/ns.
8. Specification is for a maximum 1.0 V (2/3 V_{TT} for AGTL) swing from V_{TT} - 1V to V_{TT}. This assumes an edge rate of 3V/ns.
9. This should be measured after $V_{CC_{CORE}}$, V_{TT}, $V_{CC_{CMOS}}$, and BCLK become stable.
10. This specification applies to the Pentium III processor running at 100 MHz system bus frequency.
11. This specification applies to the Pentium III processor running at 133 MHz system bus frequency.
12. BREQ signals at 133 MHz system bus observe a 1.2 ns minimum setup time.
13. For AGTL, V_{REF} is 2/3 V_{TT} ±3%.

Table 17. System Bus AC Specifications (CMOS Signal Group) [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	11	Active and Inactive states
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	11, 14	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies
2. These specifications are tested during manufacturing.
3. These signals may be driven asynchronously.
4. All CMOS outputs shall be asserted for at least 2 BCLKs.
5. When driven inactive or after VCC_{CORE}, VTT, VCC_{CMOS}, and BCLK become stable.

Table 18. System Bus AC Specifications (Reset Conditions) [1]

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, INIT#) Setup Time	4		BCLKs	13	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, INIT#) Hold Time	2	20	BCLKs	13	After clock that deasserts RESET#

NOTE: 1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.

Table 19. System Bus AC Specifications (APIC Clock and APIC I/O)[1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	9	
T23: PICCLK High Time	10.5		ns	9	@ > 1.7V
T24: PICCLK Low Time	10.5		ns	9	@ < 0.7V
T25: PICCLK Rise Time	0.25	3.0	ns	9	(0.7V - 1.7V)
T26: PICCLK Fall Time	0.25	3.0	ns	9	(1.7V - 0.7V)
T27: PICD[1:0] Setup Time	5.0		ns	12	4
T28: PICD[1:0] Hold Time	2.5		ns	12	4
T29a: PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	ns	10, 11	4, 5, 6
T29b: PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0	ns	10, 11	4, 5, 6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor pins. All APIC I/O signal timings are referenced at 0.75 V at the processor pins.
4. Referenced to PICCLK rising edge.
5. For open drain signals, valid delay is synonymous with float delay.
6. Valid delay timings for these signals are specified into 150 Ω load pulled up to 1.5 V.

Table 20. Platform Power-On Timings[2]

T# Parameter	Min	Max	Unit	Figure	Notes
T45: Valid Time Before VTT_PWRGD	1.0		mS	14	1
T46: Valid Time Before PWRGOOD	2.0		mS	14	1
T47: RESET# Inactive to Valid Outputs	1		BCLK	14	1
T48: RESET# Inactive to Drive Signals	4		BCLK	14	1

NOTES:

1. All signals, during their invalid states, must be guarded against spurious levels from effecting the platform during processor power-up sequence.
2. Configuration Input signals include: A[14:5], BR0#, BR1#, INIT#. For timing of these signals, please refer to Table 17 and Figure 13.

Note: For Figure 9 through Figure 15, the following apply:

1. Figure 9 through Figure 15 are to be used in conjunction with Table 14 through Table 20.
2. All AC timings for the AGTL+ signals at the processor pins are referenced to the BCLK rising edge at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor pins.
3. All AC timings for the APIC I/O signals at the processor pins are referenced to the PICCLK rising edge at 1.25 V. All APIC I/O signal timings are referenced at 0.75 V at the processor pins.
4. All AC timings for the TAP signals at the processor pins are referenced to the TCK rising edge at 0.75 V. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.75 V at the processor pins.

Figure 9. Generic Clock Waveform

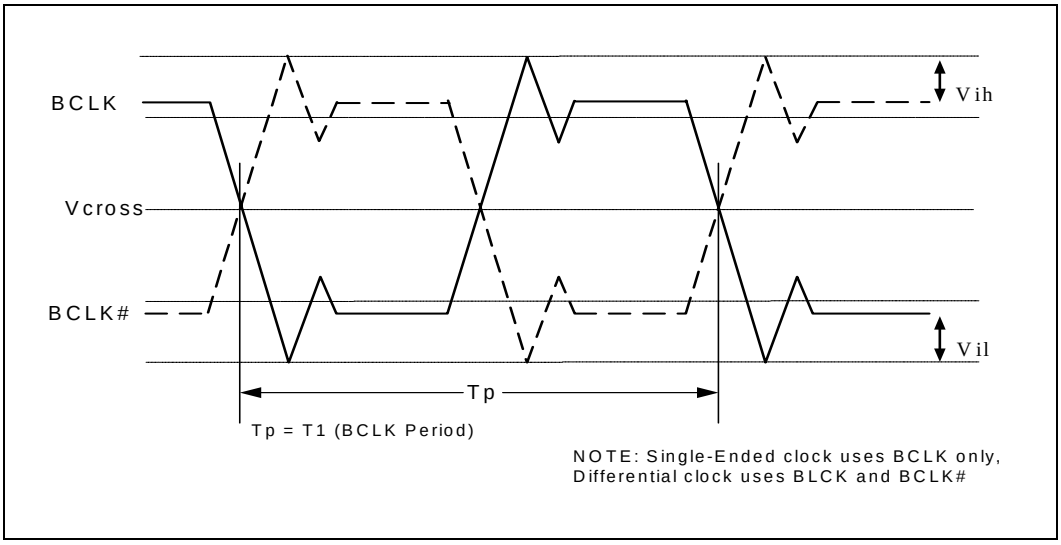
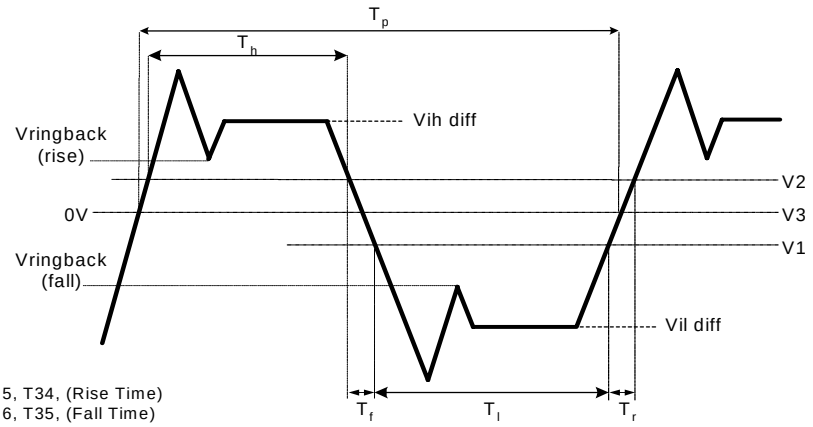
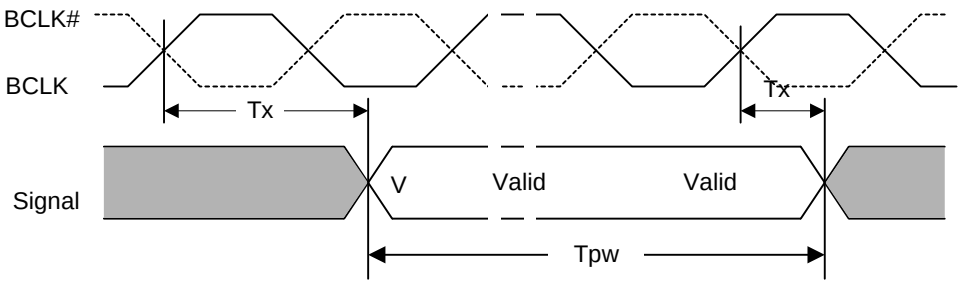


Figure 10. BCLK, PICCLK, and TCK Generic Clock Waveform



T_r = T5, T25, T34, (Rise Time)
T_f = T6, T26, T35, (Fall Time)
T_h = T3, T23, T32, (High Time)
T_l = T4, T24, T33, (Low Time)
T_p = T1, T22, T31 (BCLK, TCK, PICCLK Period)
V1 = BCLK is referenced to 0.30V (Differential Mode), 0.50V (Single-Ended Mode)
TCK is referenced to Vref - 200 mV, PICCLK is referenced to 0.4V.
V2 = BCLK is refernced to 0.9V (Differental Mode), 2.0V (Single-Ended Mode)
TCK is referenced to Vref + 200 mV, PICCLK is refernced to 1.6V
V3 = BCLK and BLCK# crossing point of the rising edge of BLCK and the falling edge of BCLK# (Differential Mode), BCLK i refereced to 1.25V (Single-Ended Mode), PICCLK is reference to 1.0V, TCK is referenced to Vcmosref

Figure 11. System Bus Valid Delay Timings



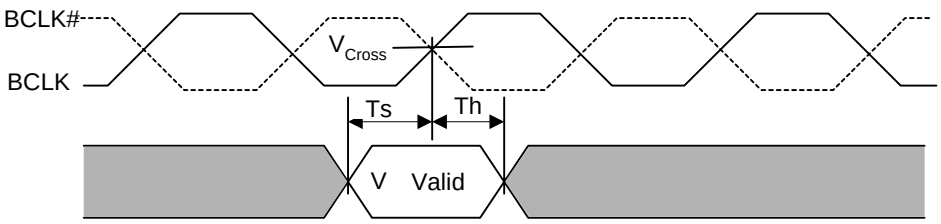
Tx = T7, T11, T29a, T29b (Valid Delay)

Tpw = T14, T15 (Pulse Width)

V = Vref for AGTL signal group; Vcmosref for CMOS, APIC and TAP signal groups

NOTE: Single-Ended clock uses BCLK only, Differential clock uses BCLK and BCLK#

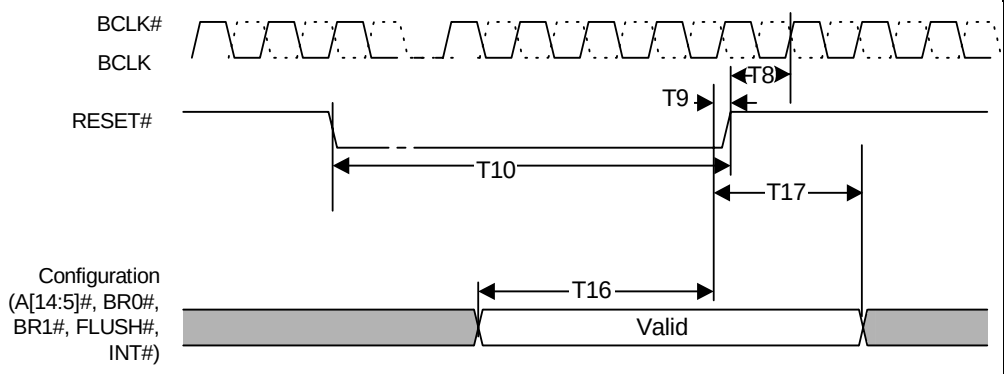
Figure 12. System Bus Setup and Hold Timings



V_{Cross} = Crossing point of BLCK and BCLK#
Ts = T8, T12, T27 (Setup Time)
Th = T9, T13, T28 (Hold Time)
V = Vref for AGTL signal group; 0.75V for APIC and TAP signal groups

NOTE: Single-Ended clock uses BCLK only, Differential clock uses BCLK and BCLK#

Figure 13. System Bus Reset and Configuration Timings



T9 = (AGTL+ Input Hold Time)
T8 = (AGTL+ Input Setup Time)
T10 = (RESET# Pulse Width)
T16 = (Reset Configuration Signals (A[14:5]#, BR0#, BR1#, FLUSH#, INIT#) Setup Time)
T17 = (Reset Configuration Signals (A[14:5]#, BR0#, BR1#, FLUSH#, INIT#) Hold Time)

NOTE: Single-Ended clock uses BCLK only, Differential clock uses BCLK and BCLK#

Figure 14. Platform Power-On Sequence Timings

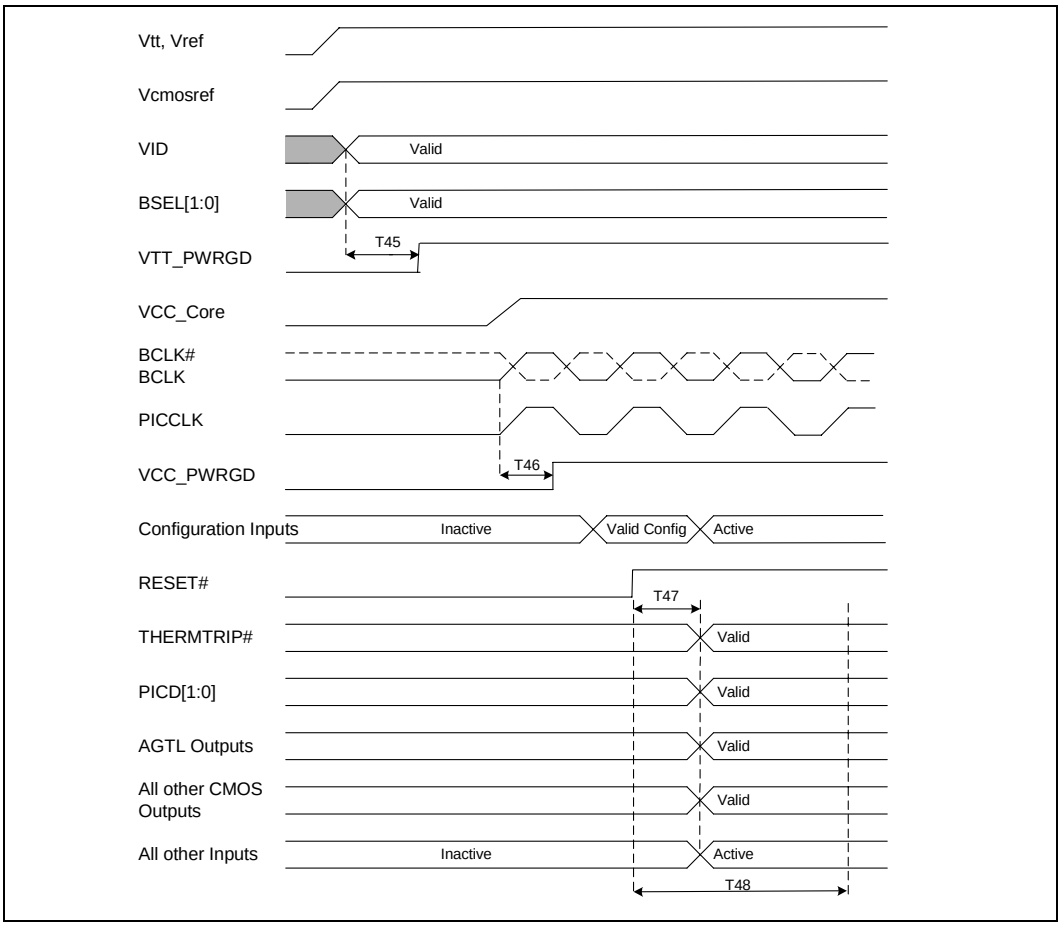
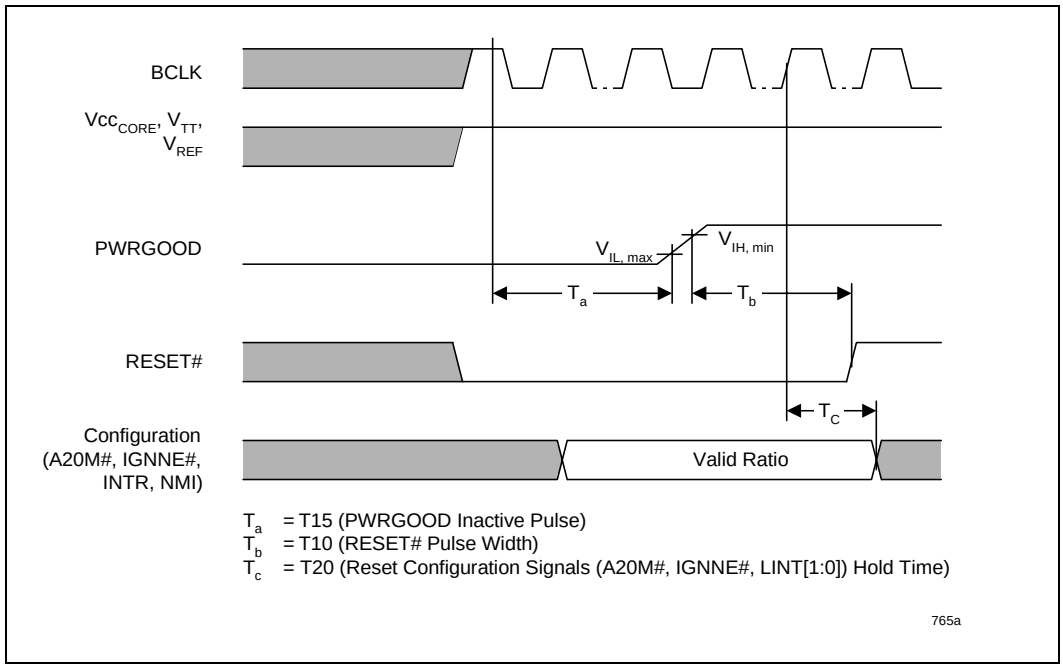


Figure 15. Power-On Reset and Configuration Timings



3.0 Signal Quality Specifications

Signals driven on the processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor pins. Meeting the specifications at the processor pins in Table 21, Table , Table 23, Table , and Table ensures that signal quality effects will not adversely affect processor operation.

3.1 BCLK/BCLK# and PICCLK Signal Quality Specifications and Measurement Guidelines

Table 21 describes the signal quality specifications at the processor pins for the processor system bus clock (BCLK) and APIC clock (PICCLK) signals. Figure 16 describes the signal quality waveform for the system bus clock at the processor pins.

Table 21. BCLK/PICCLK Signal Quality Specifications for Simulation at the Processor Pins [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.500	V	16	
V1: PICCLK V_{IL}			0.700	V	16	
V2: BCLK V_{IH}	2.000			V	16	
V2 PICCLK V_{IH}	2.000			V	16	
V3: V_{IN} Absolute Voltage Range	–0.58		3.18	V	16	
V4: BCLK Rising Edge Ringback	2.000			V	16	2
V4: PICCLK Rising Edge Ringback	2.000			V	16	2
V5: BCLK Falling Edge Ringback			0.500	V	16	2
V5: PICCLK Falling Edge Ringback			0.700	V	16	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processors frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK/PICCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

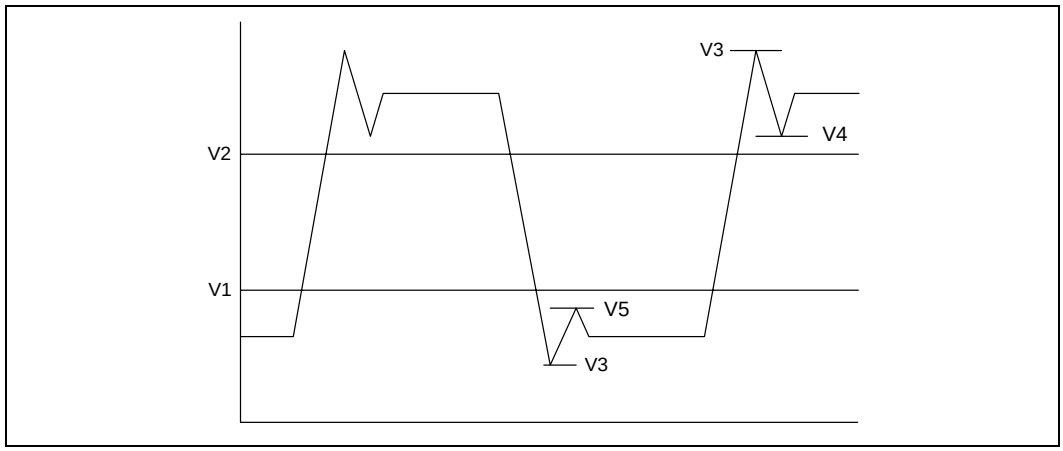
Table 22. BCLK/PICCLK Signal Quality Specifications for Simulation at the Processor Pins in a Differential Clock Platform for AGTL

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: PICCLK V_{IL}			0.40	V	16	
V2 PICCLK V_{IH}	1.60			V	16	
V3: PICCLK Absolute Voltage Range	-0.4		2.4	V	16	
V4: PICCLK Rising Edge Ringback	1.60			V	16	2
V5: PICCLK Falling Edge Ringback			0.40	V	16	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors that support the AGTL specification. Refer to the *Intel® Pentium® III Processor Specification Update* for a complete listing on the processors that support the AGTL specification.

2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK/PICCLK signal can dip back to after passing the VIH (rising) or VIL (falling) voltage limits. This specification is an absolute value.

Figure 16. BCLK, PICCLK Generic Clock Waveform at the Processor Pins



3.2 AGTL+ / AGTL Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in the appropriate platform design guide. Refer to the *Intel® Pentium® II Processor Developer's Manual* (Order Number 243502) for the AGTL+/AGTL buffer specification.

Table 23 provides the AGTL+ signal quality specifications for the processor for use in simulating signal quality at the processor pins.

The Pentium III processor for the PGA370 socket maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 25 through Table 27. Figure 17 shows the AGTL+/AGTL ringback tolerance and Figure 18 shows the overshoot/undershoot waveform.

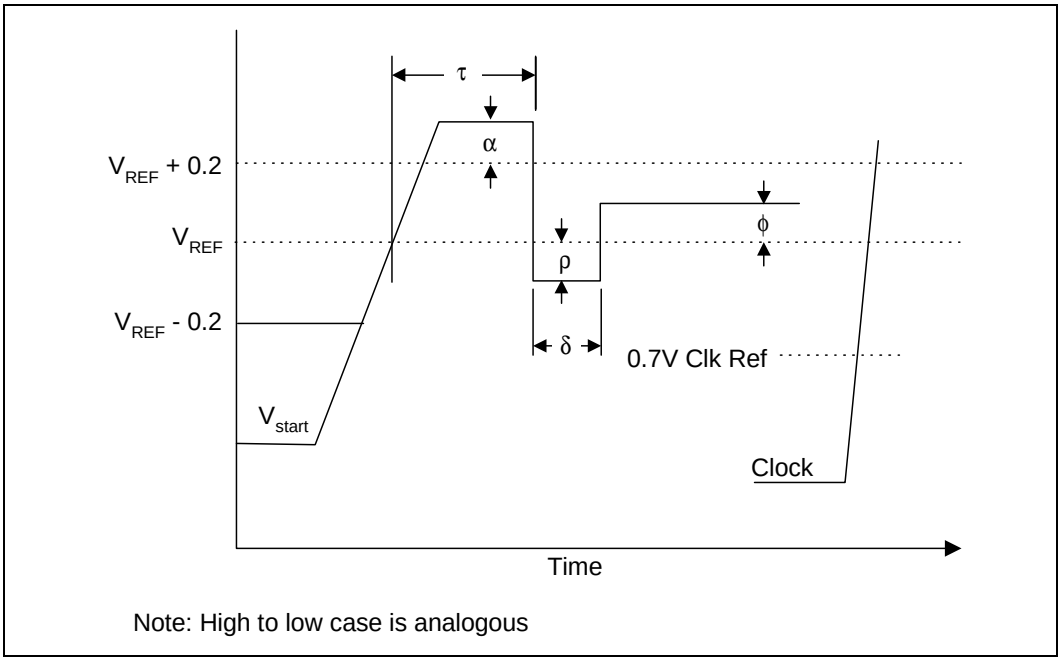
Table 23. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Pins [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	17	4, 8
τ: Minimum Time at High	0.50	ns	17	
ρ: Amplitude of Ringback	±200	mV	17	5, 6, 7, 8
ϕ: Final Settling Voltage	200	mV	17	8
δ: Duration of Squarewave Ringback	N/A	ns	17	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processors frequencies.
2. Specifications are for the edge rate of 0.3 - 0.8V/ns. See Figure 17 for the generic waveform.
3. All values specified by design characterization.
4. Please see Table 25 for maximum allowable overshoot.
5. Ringback between V_{REF} + 100 mV and V_{REF} + 200 mV or V_{REF} - 200 mV and V_{REF} - 100 mVs requires the flight time measurements to be adjusted as described in the Intel AGTL+ Specifications (*Intel®Pentium®II Developers Manual*). Ringback below V_{REF} + 100 mV or above V_{REF} - 100 mV is not supported.

6. Intel recommends simulations not exceed a ringback value of V_{REF} ±200 mV to allow margin for other sources of system noise.
7. A negative value for ρ indicates that the amplitude of ringback is above V_{REF}. (i.e., ϕ = -100 mV specifies the signal cannot ringback below V_{REF} + 100 mV).
8. ϕ and ρ: are measured relative to V_{REF}. α: is measured relative to V_{REF} + 200 mV.

Figure 17. Low to High AGTL+ Receiver Ringback Tolerance



3.3 AGTL+ Signal Quality Specifications and Measurement Guidelines

3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on 1.5 V or 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and overshoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O Buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the Pentium III processor performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O Buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O Buffer model will impact results and may yield excessive overshoot/undershoot.

3.3.2 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level, VSS (overshoot) and VTT (undershoot). While overshoot can be measured relative to VSS using one probe (probe to signal and GND lead to VSS), undershoot must be measured relative to VTT. This could be accomplished by simultaneously measuring the VTT plane while measuring the signal undershoot. Today's oscilloscopes can easily calculate the true undershoot waveform. The true undershoot waveform can also be obtained with the following oscilloscope data file analysis:

Converted Undershoot Waveform = VTT - Signal_measured

Note: The converted undershoot waveform appears as a positive (overshoot) signal.

Note: Overshoot (rising edge) and undershoot (falling edge) conditions are separate and their impact must be determined independently.

After the true waveform conversion, the undershoot/overshoot specifications shown in Table 25 through Table 27 can be applied to the converted undershoot waveform using the same magnitude and pulse duration specifications used with an overshoot waveform.

Overshoot/undershoot magnitude levels must observe the Absolute Maximum Specifications listed in Table 25 through Table 27. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the Absolute Maximum Specifications (2.18V), the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.3.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage (Vos_ref = 1.635 V). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Note: Multiple Overshoot/Undershoot events occurring within the same clock cycle must be considered together as one event. Using the worst case Overshoot/Undershoot Magnitude, sum together the individual Pulse Durations to determine the total Overshoot/Undershoot Pulse Duration for that total event.

3.3.4 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of an AGTL+ or a CMOS signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs EVERY OTHER clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

The specifications provided in Table 25 through Table 27 show the Maximum Pulse Duration allowed for a given Overshoot/Undershoot Magnitude at a specific Activity Factor. Each Table entry is independent of all others, meaning that the Pulse Duration reflects the existence of overshoot/undershoot events of that magnitude **only**. A platform with an overshoot/undershoot that

just meets the pulse duration for a specific magnitude where the AF < 1, means that there can be NO other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note: Activity factor for AGTL+ signals is referenced to BCLK frequency.

Note: Activity factor for CMOS signals is referenced to PICCLK frequency.

3.3.5 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the Pentium III processor for the PGA370 socket is not a simple single value. Instead, many factors are needed to determine what the over/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the junction temperature the processor will be operating at, the width of the overshoot (as measured above 1.635 V) and the Activity Factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group that particular signal falls into. If the signal is an AGTL+ signal operating with a 100 MHz system bus, use Table 25 (100MHz AGTL+ signal group). If the signal is an AGTL+ signal operating with a 133MHz system bus, use Table 26 (133 MHz AGTL+ signal group). If the signal is a CMOS signal, use Table 27 (33 MHz CMOS signal group).
2. Determine the maximum junction temperature (Tj) for the range of processors that the system will support (80^{o}C or 85^{o}C).
3. Determine the Magnitude of the overshoot (relative to V_{SS})
4. Determine the Activity Factor (how often does this overshoot occur?)
5. From the appropriate Specification table, read off the Maximum Pulse Duration (in ns) allowed.
6. Compare the specified Maximum Pulse Duration to the signal being measured. If the Pulse Duration measured is less than the Pulse Duration shown in the table, then the signal meets the specifications.

The above procedure is similar for undershoots after the undershoot waveform has been converted to look like an overshoot. Undershoot events must be analyzed separately from Overshoot events as they are mutually exclusive.

Below is an example showing how the maximum pulse duration is determined for a given waveform.

Table 24. Example Platform Information

Required Information	Maximum Platform Support	Notes
FSB Signal Group	133 MHz AGTL+	
Max Tj	85 °C	
Overshoot Magnitude	2.13V	Measured Value
Activity Factor (AF)	0.1	Measured overshoot occurs on average every 20 clocks

NOTES:
1. Corresponding Maximum Pulse Duration Specification - 2.4 ns
2. Pulse Duration (measured) - 2.0 ns

Given the above parameters, and using Table 26 (85 ^{o}C/AF = 0.1 column) the maximum allowed pulse duration is 2.4 ns. Since the measure pulse duration is 2.0 ns, this particular overshoot event passes the overshoot specifications, although this doesn't guarantee that the combined overshoot/ undershoot events meet the specifications.

3.3.6 Determining if a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below. It is important to meet these guidelines; otherwise, contact your Intel field representative.

1. Insure no signal (CMOS or AGTL+/AGTL) ever exceed the 1.635 V

   OR

2. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables

   OR

3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

The following notes apply to Table 25 through Table 27.

NOTES:
1. Overshoot/Undershoot Magnitude = 2.18 V is an Absolute value and should never be exceeded
2. Overshoot is measured relative to V_{SS}.
3. Undershoot is measured relative to V_{TT}
4. Overshoot/Undershoot Pulse Duration is measured relative to 1.635 V.
5. Ringbacks below V_{TT} can not be subtracted from Overshoots/Undershoots
6. Leser Undershoot does not allocate longer or larger Overshoot
7. OEM's are encouraged to follow Intel provided layout guidelines. Consult the layout guidelines provided in the specific platform design guide.
8. All values specified by design characterization

Table 25. 100 MHz AGTL+ / AGTL Signal Group Overshoot/Undershoot Tolerance at Processor Pins[1,2]

Overshoot/ Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 85 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	20	2.53	0.25	18.6	1.86	0.18
2.13 V	20	4.93	0.49	20	3.2	0.32
2.08 V	20	9.1	0.91	20	6.1	0.6
2.03 V	20	16.6	1.67	20	11.4	1.1
1.98 V	20	20	3.0	20	20	2
1.93 V	20	20	5.5	20	20	6.6
1.88 V	20	20	10	20	20	20

NOTES:
1. BCLK period is 10 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

Table 26. 133 MHz AGTL+/AGTL Signal Group Overshoot/Undershoot Tolerance [1, 2]

Overshoot/Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 85 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	15	1.9	0.19	14	1.4	0.14
2.13 V	15	3.7	0.37	15	2.4	0.24
2.08 V	15	6.8	0.68	15	4.6	0.46
2.03 V	15	12.5	1.25	15	8.6	0.84
1.98 V	15	15	2.28	15	15	1.5
1.93 V	15	15	4.1	15	15	5
1.88 V	15	15	7.5	15	15	15

NOTES:
1. BCLK period is 7.5 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

Table 27. 33 MHz CMOS Signal Group Overshoot/Undershoot Tolerance at Processor Pins[1, 2]

Overshoot/ Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 85 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	60	7.6	0.76	56	5.6	0.56
2.13 V	60	14.8	1.48	60	9.6	0.96
2.08 V	60	27.2	2.7	60	18.4	1.8
2.03 V	60	50	5	60	33	3.3
1.98 V	60	60	9.1	60	60	6
1.93 V	60	60	16.4	60	60	20
1.88 V	60	60	30	60	60	60

NOTES:
1. PICCLK period is 30 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

Figure 18. Maximum Acceptable AGTL+ Overshoot/Undershoot Waveform

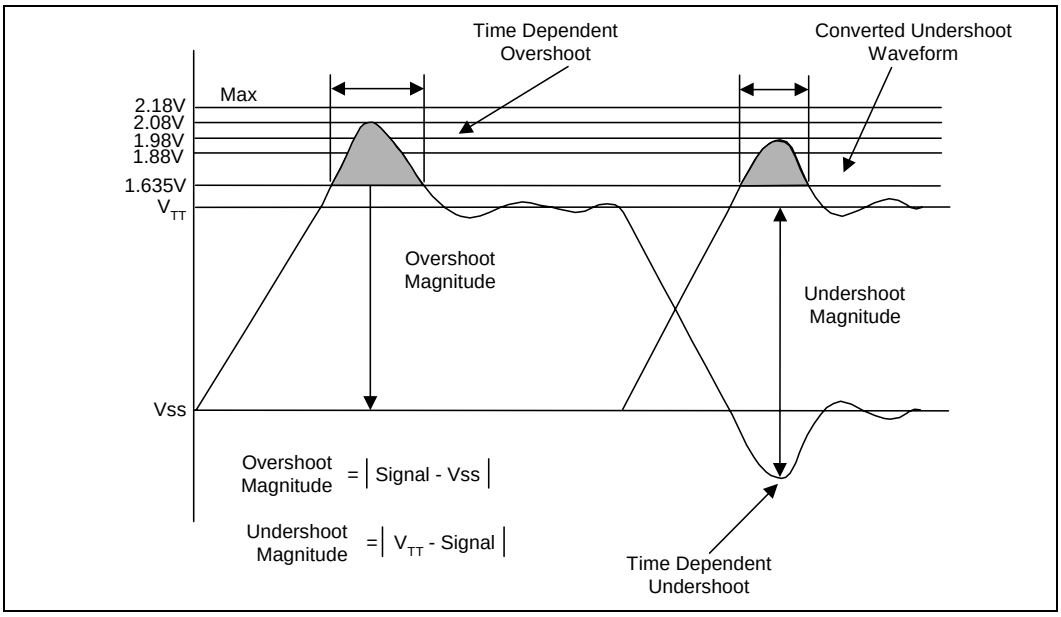
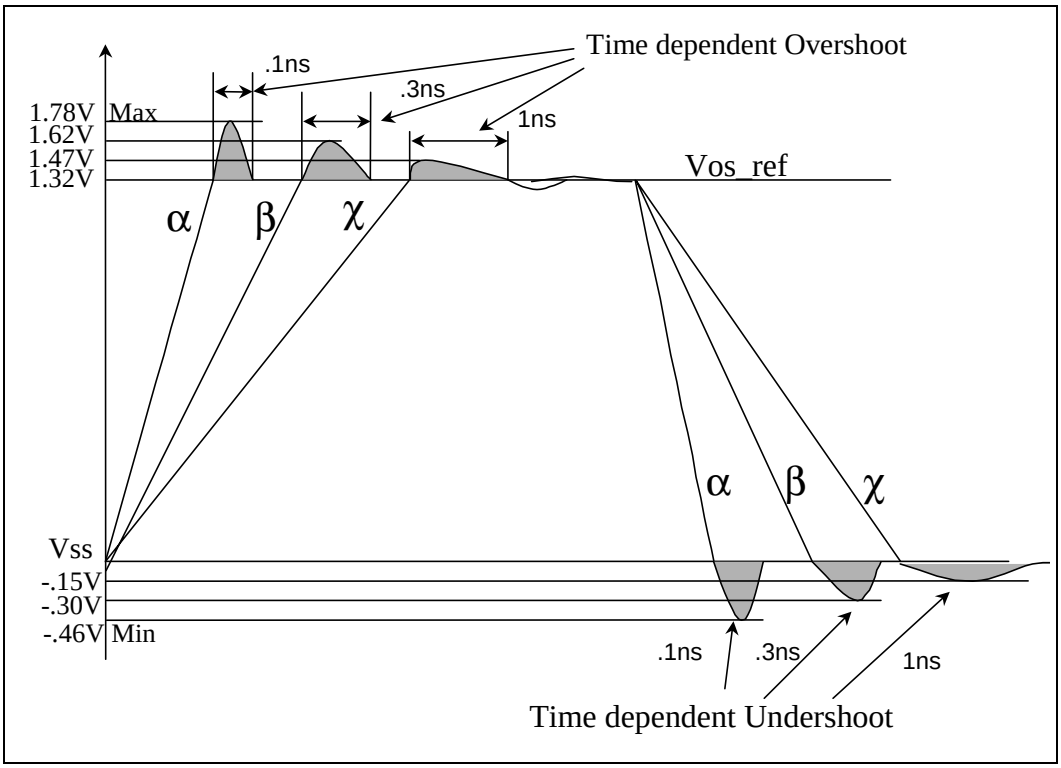


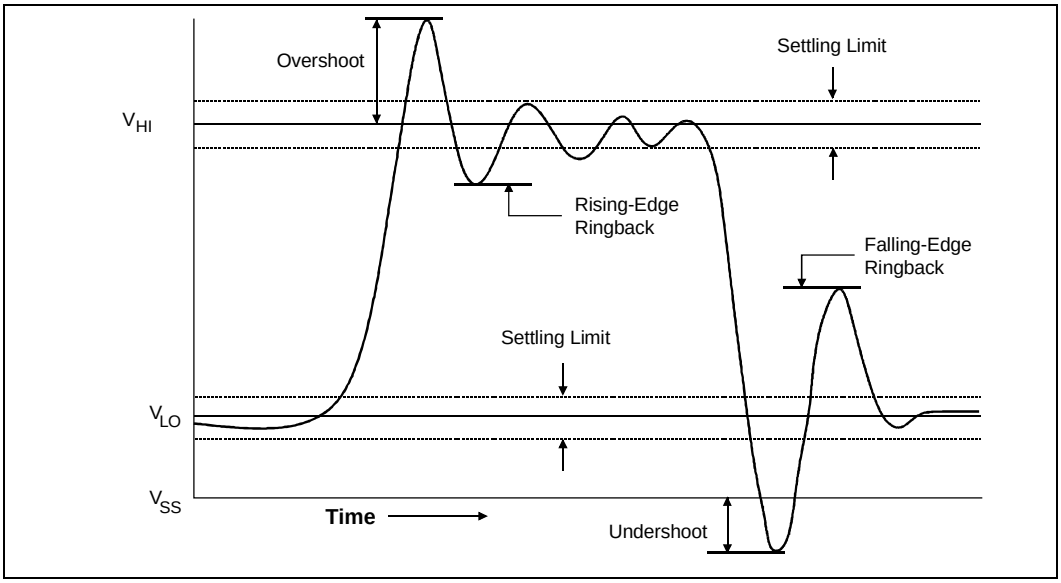
Figure 19. Maximum Acceptable AGTL Overshoot/Undershoot Waveform



3.4 Non-AGTL+ (Non-AGTL) Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 20 for the non-AGTL+ signal group.

Figure 20. Non-AGTL+ (Non-AGTL) Overshoot/Undershoot, Settling Limit, and Ringback [1]



NOTES:
1. V_{HI} = 1.5 V for all non-AGTL+ signals except for BCLK, PICCLK, and PWRGOOD. V_{HI} = 2.5 V for BCLK, PICCLK, and PWRGOOD. BCLK and PICCLK signal quality is detailed in Section 3.1.

3.4.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates (see Figure 20 for non-AGTL+ signals). The processor can be damaged by repeated overshoot events on 1.5 V or 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult. *The overshoot/undershoot guideline is 0.3 V* and assumes the absence of diodes on the input. These guidelines should be verified in simulations *without the on-chip ESD protection diodes present* because the diodes will begin clamping the 1.5 V and 2.5 V tolerant signals beginning at approximately 0.7 V above the appropriate supply and 0.7 V below VSS. If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

Note: The undershoot guideline limits transitions exactly as described for the ATGL+/AGTL signals. See Figure 18.

3.4.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is the voltage that the signal rings back to after achieving its maximum absolute value. See Figure 20 for an illustration of ringback. Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-AGTL+ (non-AGTL) signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table for the signal ringback specifications for non-AGTL+ signals for simulations at the processor pins.

Table 28. Signal Ringback Specifications for Non-AGTL+ Signal Simulations at the Processor Pins[1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals [2]	0 → 1	V_{CMOS_REF} + 0.200	V	20
Non-AGTL+ Signals [2]	1 → 0	V_{CMOS_REF} - 0.200	V	20
PWRGOOD	0 → 1	2.00	V	20

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. Non-AGTL+ signals except PWRGOOD.

Table 29. Signal Ringback Specifications for Non-AGTL Signal Simulations at the Processor Pins [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals [2]	0 → 1	V_{CMOS_REF} + 0.200	V	20
Non-AGTL+ Signals [2]	1 → 0	V_{CMOS_REF} - 0.300	V	20
PWRGOOD	0 → 1	2.00 [3]	V	20

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. Non-AGTL signals except PWRGOOD.
3. For Coppermine-T with differential clocking, this signal is 1.8 V tolerant.

3.4.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10% of the total signal swing (V_{HI}-V_{LO}) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

This chapter provides needed data for designing a thermal solution. However, for the correct thermal measuring processes, refer to AP-905, *Intel® Pentium® III Processor Thermal Design Guidelines* (Document Number 245087). The Pentium III processor uses flip chip pin grid array packaging technology and has a **junction** ($T_{junction}$) or **case** temperature (T_{case}) specified.

4.1 Thermal Specifications

Table 30 provides the thermal design power dissipation and maximum temperatures for the Pentium III processor for the PGA370 socket. Systems should design for the highest possible processor power, even if a processor with a lower thermal dissipation is planned. A thermal solution should be designed to ensure the junction temperature never exceeds these specifications.

Table 30. Intel® Pentium® III Processor Thermal Design Power for the FC-PGA Package[1]

Processor	Processor Core Frequency (MHz)	System Bus Frequency (MHz)	Processor Thermal Design Power [2,3] up to CPUID 0686h (W)	Processor Thermal Design Power [2,3] CPUID 068Ah (W)	Power Density[5] for CPUID 068Ah (W/cm^2)	Maximum $T_{JUNCTION}$[10] (°C)	$T_{JUNCTION}$ Offset for Latest Stepping [4,6] (°C)
500E	500	100	13.2	N/A	N/A	85	1.9
533EB	533	133	14.0	N/A	N/A	85	2.0
550E	550	100	14.5	N/A	N/A	85	2.1
600E	600	100	15.8	19.6	30.5	82	2.6
600EB	600	133	15.8	N/A	N/A	82	2.3
650	650	100	17.0	N/A	N/A	82	2.7
667	667	133	17.5	N/A	N/A	82	2.8
700	700	100	18.3	21.9	34.1	80	2.9
733	733	133	19.1	22.8	35.5	80	3.0
750	750	100	19.5	23.2	36.1	80	3.0
800	800	100	20.8	24.5	38.2	80	3.2
800EB	800	133	20.8	24.5	38.2	80	3.2
850	850	100	22.5	25.7	40.0	80	3.4
866	866	133	22.9	26.1	40.7	80	3.4
900	900	100	23.2	26.7	41.6	77	3.5
933	933	133	24.5	27.5	42.8	77	3.6
1 GHz	1000	100	N/A	29.0	45.2	75[8]	3.8
1B GHz	1000	133	26.1	29.0	45.2	70[9] | 75[8]	3.8
1B GHz[7]	1000	133	29.6	N/A	N/A	70	3.9
1.10 GHz	1100	100	N/A	33.0	51.4	77	4.4

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor pins.

2. Thermal Design Power (TDP) represents the maximum amount of power the thermal solution is required to dissipate. The thermal solution should be designed to dissipate the TDP power without exceeding the maximum Tjunction specification.
3. TDP does not represent the power delivery and voltage regulation requirements for the processor. Refer to Table 6 for voltage regulation and electrical specifications.
4. $T_{junctionoffset}$ is the worst-case difference between the thermal reading from the on-die thermal diode and the hottest location on the processor's core.
5. Power density is the maximum power the processor die can dissipate (i.e., processor power) divided by the die area over which the power is generated. Power for these processors is generated from the core area shown in Figure 21.
6. TJUNCTION offset values do not include any thermal diode kit measurement error. Diode kit measurement error must be added to the TJUNCTION offset value from the table, as outlined in the *Intel® Pentium® III processor Thermal Metrology for CPUID-068h Family Processors* (Order Number: 245301). Intel has characterized the use of the Analog Devices AD1021 diode measurement kit and found its measurement error to be 1 °C.
7. This specification only applies to 1B GHz S-Spec #: SL4WM. This part has a VID request of 1.70 V, however the processor should be supplied 1.76 V at the PGA Vcc pins by the VRM (Voltage Regulator Module) or by the voltage regulator circuit.
8. This specification applies to processors with CPUID 068AH. 1B GHz exists in both FC-PGA and FC-PGA2 packages.
9. This specification applies to processors with CPUID 0686H.
10. Tjunction minimum specification is 0 °C.

Table 31 provides the thermal design power dissipation and maximum temperatures for the Pentium III processor for the FC-PGA2 package. Systems should design for the highest possible processor power, even if a processor with a lower thermal dissipation is planned. A thermal solution should be designed to ensure the case temperature never exceeds these specifications.

Table 31. Intel® Pentium® III Processor for the FC-PGA2 Package Thermal Design Power [1]

Processor	Processor Core Frequency (MHz)	System Bus Frequency (MHz)	Processor Thermal Design Power [2,3] CPUID 068Ah (W)	Maximum T_{case} [4] (°C)	Additional Notes
866	866	133	29.5	70	5
933	933	133	31.5	72	5
1B GHz	1000	133	33.9	69	5
1.13 GHz	1133	133	37.5	72	

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor pins.
2. Thermal Design Power (TDP) represents the maximum amount of power the thermal solution is required to dissipate. The thermal solution should be designed to dissipate the TDP power without exceeding the maximum Tcase specification.
3. TDP does not represent the power delivery and voltage regulation requirements for the processor. Refer to Table 7 for voltage regulation and electrical specifications.
4. $T_{CaseOffset}$ is the worst-case difference between the maximum case temperature and the thermal diode temperature on the processor's core. For more information please refer to the document, *Intel® Pentium® III Processor in the FC-PGA2 Package Thermal Design Guide.*
5. This processor exists in both FC-PGA and FC-PGA2 packages.

4.2 Processor Die Area

Figure 21 is a block diagram of the Pentium III processor die layout and Table 32 contains Pentium III processor die layout measurements. The layout differentiates the processor core from the cache die area. In effect, the thermal design power identified in Table 30 is dissipated entirely from the processor core area. Thermal solution designs should compensate for this smaller heat flux area and not assume that the power is uniformly distributed across the entire die area.

Figure 21. Processor Functional Die Layout for FC-PGA

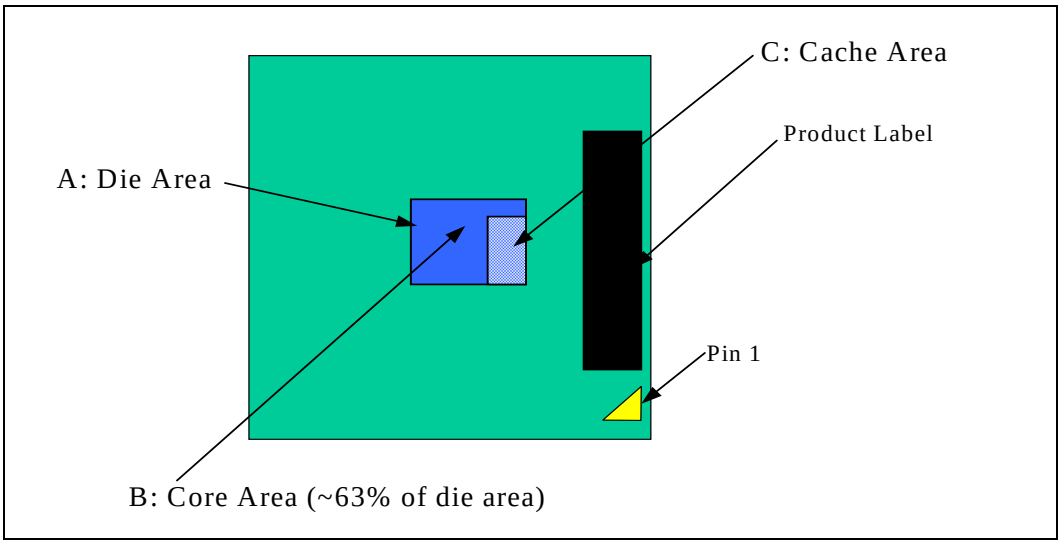


Table 32. Processor Functional Die Layout for FC-PGA

CPUID	A: Die Area (cm^2)	B: Core Area (cm^2)	C: Cache Area (cm^2)
0683H	1.046	0.726	0.320
0686H	0.900	0.642	0.258
068AH	0.947	0.642	0.305

4.3 Thermal Diode

The Pentium III processor for the PGA370 socket incorporates an on-die diode that may be used to monitor the die temperature (junction temperature). A thermal sensor located on the motherboard, or a stand-alone measurement kit, may monitor the die temperature of the processor for thermal management or instrumentation purposes. Table 33 and Table 34 provide the diode parameter and interface specifications. For more information please refer to the document, *Intel® Pentium® III Processor in the FC-PGA2 Package Thermal Design Guide.*

Note: The reading of the thermal sensor connected to the thermal diode will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die at a given point in time, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the $T_{junction}$ temperature can change.

Table 33. Thermal Diode Parameters[1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{fw}	Forward Bias Current	5		300	µA	1
n	Diode Ideality Factor	1.0057	1.0080	1.0125		2, 3, 4

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 100 ° C with a forward bias current of 5 µA–300 µA.
3. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   I_{fw}=Is(e^ ((Vd*q)/(nkT)) - 1), where Is = saturation current, q = electronic charge, Vd = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
4. Not 100% tested. Specified by design characterization.

Table 34. Thermal Diode Interface

Pin Name	PGA370 Socket pin #	Pin Description
THERMDP	AL31	diode anode (p_junction)
THERMDN	AL29	diode cathode (n_junction)

5.0 Mechanical Specifications

The Pentium III processor uses a FC-PGA and FC-PGA2 package technology. Mechanical specifications for the processor are given in this section. FC-PGA2 contains an Integrated Heat Spreader (IHS) to spread out the heat generated from the die. See Section 1.1.1 for a complete terminology listing.

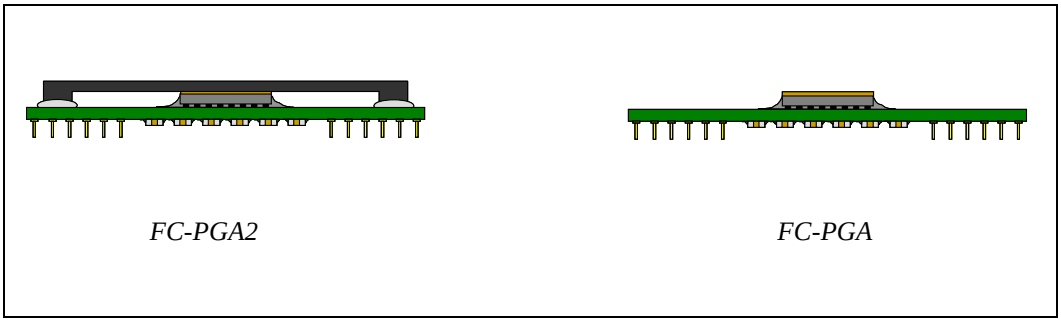
The processor utilizes a PGA370 socket for installation into the motherboard. Details on the socket are available in the *370-Pin Socket (PGA370) Design Guidelines*.

Note: For Figure 23 and Figure 24 the following apply:

1. Unless otherwise specified, the following drawings are dimensioned in inches.
2. All dimensions provided with tolerances are guaranteed to be met for all normal production product.
3. Figures and drawings labeled as “Reference Dimensions” are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are NOT checked as part of the processor manufacturing. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
4. Drawings are not to scale.

The following figure with package dimensions is provided to aid in the design of heatsink and clip solutions as well as demonstrate where pin-side capacitors will be located on the processor. Table 35 includes the measurements for these dimensions in both inches and millimeters.

Figure 22. FC-PGA and FC-PGA2 Package Types



5.1 FC-PGA Mechanical Specifications

The following figure with package dimensions is provided to aid in the design of heatsink and clip solutions as well as demonstrate where pin-side capacitors will be located on the processor. Table 35 includes the measurements for these dimensions in both inches and millimeters.

Figure 23. Package Dimensions

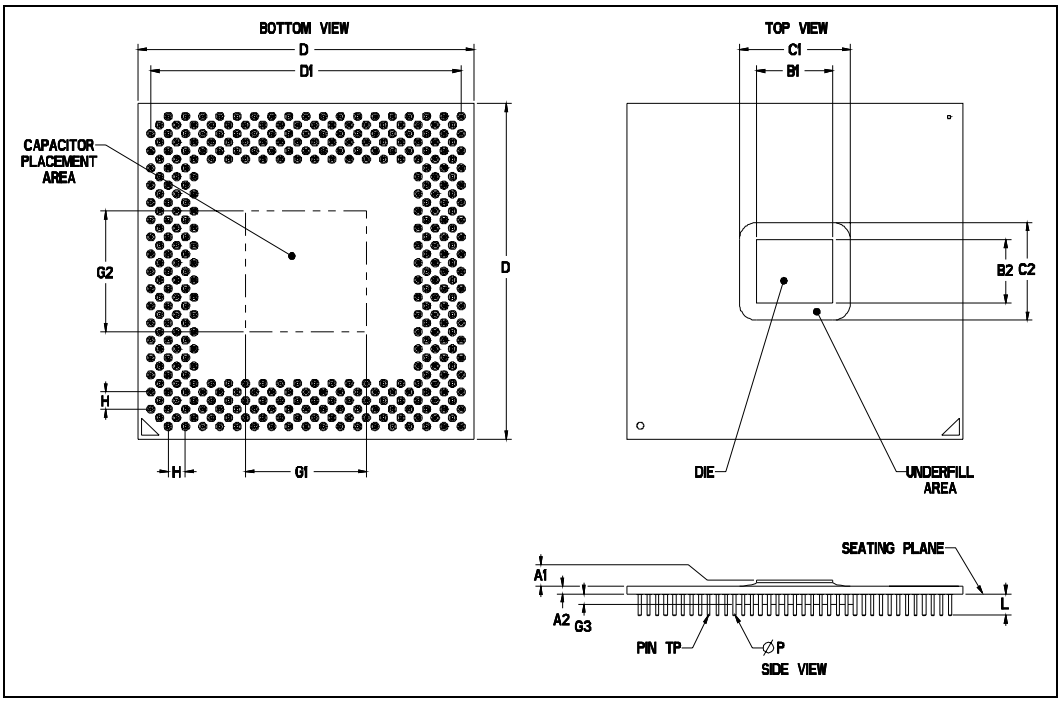


Table 35. Intel® Pentium® III Processor Package Dimensions

Symbol	Millimeters			Inches		
	Minimum	Maximum	Notes	Minimum	Maximum	Notes
A1	0.787	0.889		0.031d	0.035	
A2	1.000	1.200		0.039	0.047	
B1	11.226	11.329		0.442	0.446	
B2	9.296	9.398		0.366	0.370	
C1	23.495 max			0.925 max		
C2	21.590 max			0.850 max		
D	49.428	49.632		1.946	1.954	
D1	45.466	45.974		1.790	1.810	
G1	0.000	17.780		0	0.700	
G2	0.000	17.780		0	0.700	
G3	0.000	0.889		0	0.035	
H	2.540		Nominal	0.100		Nominal
L	3.048	3.302		0.120	0.130	
ΦP	0.431	0.483	Pin Diameter	0.017	0.019	
Pin TP	0.508 Diametric True Position (Pin-to-Pin)			0.020 Diametric True Position (Pin-to-Pin)		

NOTE: Capacitors will be placed on the pin-side of the FC-PGA package in the area defined by G1, G2, and G3. This area is a keepout zone for motherboard designers.

The bare processor die has mechanical load limits that should not be exceeded during heat sink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solution must not induce permanent stress into the processor substrate with the exception of a uniform load to maintain the heatsink to the processor thermal interface. The package dynamic and static loading parameters are listed in Table 36.

For Table 36, the following apply:

1. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.
2. Parameters assume uniformly applied loads.

Table 36. Processor Die Loading Parameters for FC-PGA

Parameter	Dynamic (max)[1]	Static (max)[2]	Unit	Added Notes
Silicon Die Surface	200	50	lbf	3
Silicon Die Edge	100	12	lbf	3

NOTES:
1. This specification applies to a uniform and a non-uniform load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. Please see socket manufacturer's force loading specification also to ensure compliance.

5.1.1 FC-PGA2 Mechanical Specifications

The following figure is provided to aid in the design of heatsink and clip solutions. Also, it is used to demonstrate where pin-side capacitors will be located on the processor. Table 31 includes the measurements for these dimensions in both inches and millimeters.

Figure 24. Package Dimensions for FC-PGA2

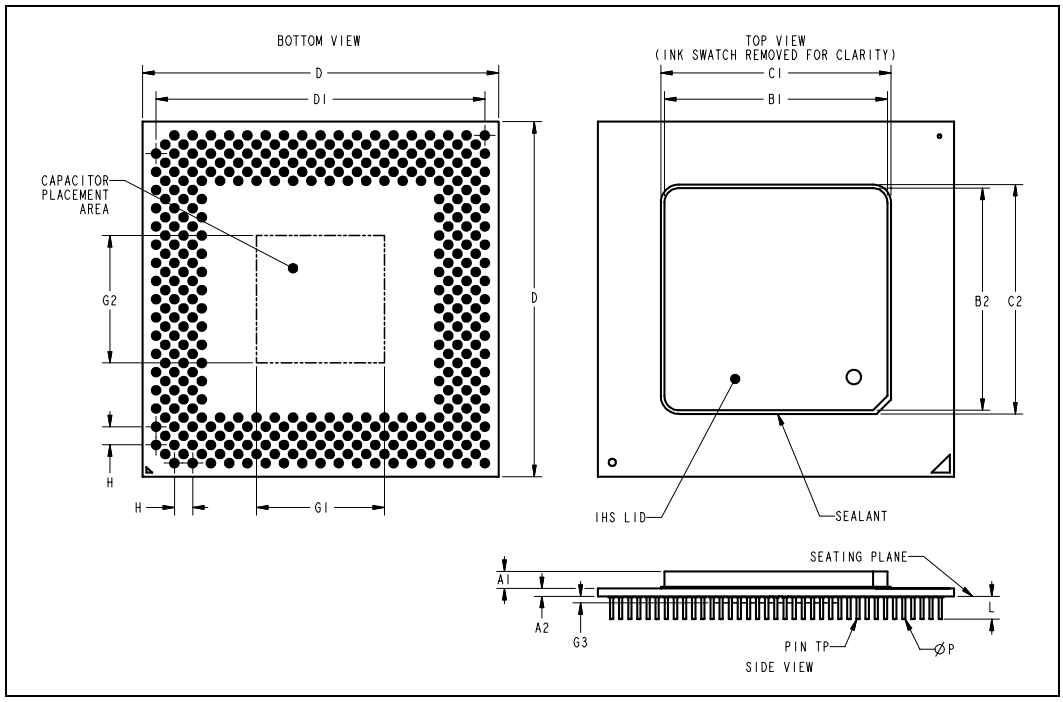


Table 37. Package Dimensions for Intel® Pentium® III Processor FC-PGA2 Package

Symbol	Millimeters			Inches		
	Minimum	Maximum	Notes	Minimum	Maximum	Notes
A1	2.266	2.690		0.089	0.106	
A2	0.980	1.180		0.038	0.047	
B1	30.800	31.200		1.212	1.229	
B2	30.800	31.200		1.212	1.229	
C1	33.000 max			1.299 max		
C2	33.000 max			1.299 max		
D	49.428	49.632		1.946	1.954	
D1	45.466	45.974		1.790	1.810	
G1	0.000	17.780		0.000	0.700	
G2	0.000	17.780		0.000	0.700	
G3	0.000	0.889		0.000	0.035	
H	2.540		Nominal	0.100		Nominal
L	3.048	3.302		0.120	0.130	
ΦP	0.431	0.483		0.017	0.019	

Table 37. Package Dimensions for Intel® Pentium® III Processor FC-PGA2 Package

Symbol	Millimeters			Inches		
	Minimum	Maximum	Notes	Minimum	Maximum	Notes
Pin TP	0.508 Diametric True Position (Pin-to-Pin)			0.020 Diametric True Position (Pin-to-Pin)		

NOTE: Capacitors will be placed on the pin-side of the FC-PGA package in the area defined by G1, G2, and G3. This area is a keepout zone for motherboard designers.

For Table 38, the following apply:

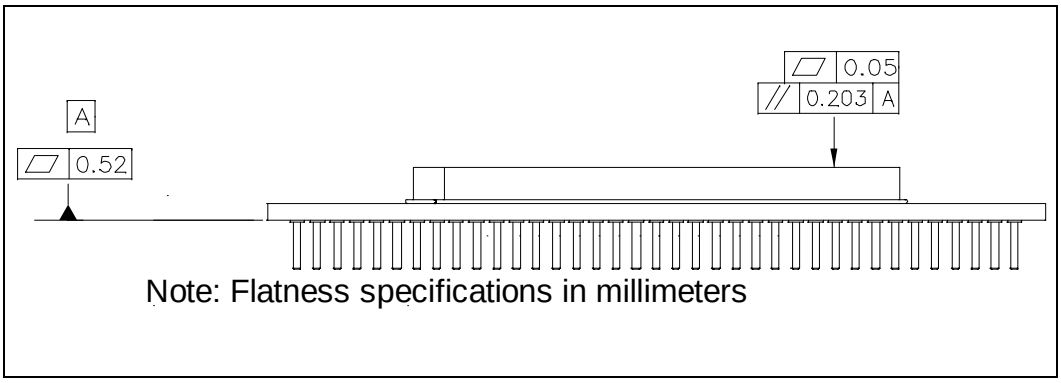
1. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.
2. Parameters assume uniformly applied loads

Table 38. Processor Case Loading Parameters for FC-PGA2

Parameter	Transient (max)[1, 4]	Dynamic (max)[2, 4]	Static (max)[3, 4]	Unit
IHS Surface	200	200	100	lbf
IHS Edge	125	N/A	N/A	lbf
IHS Corner	75	N/A	N/A	lbf

NOTES:
1. Transient loading refers to a one time short duration loading, such as during heatsink installation.
2. Dynamic loading refers to a shock load.
3. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
4. Please see socket manufacturer's force loading specification also to ensure compliance. Maximum static loading listed here does not account for the maximum reaction forces on the socket tabs or pins. Designs must ensure that the socket can withstand this force.

Figure 25. FC-PGA2 Flatness Specification



5.2 Processor Markings

The following figure exemplifies the processor top-side markings and it is provided to aid in the identification of an Pentium III processor for the PGA370 socket. Table 35 and Table 37 list the measurements for the package dimensions.

Figure 26. Top Side Processor Markings for FC-PGA (up to CPUID 0x686H)

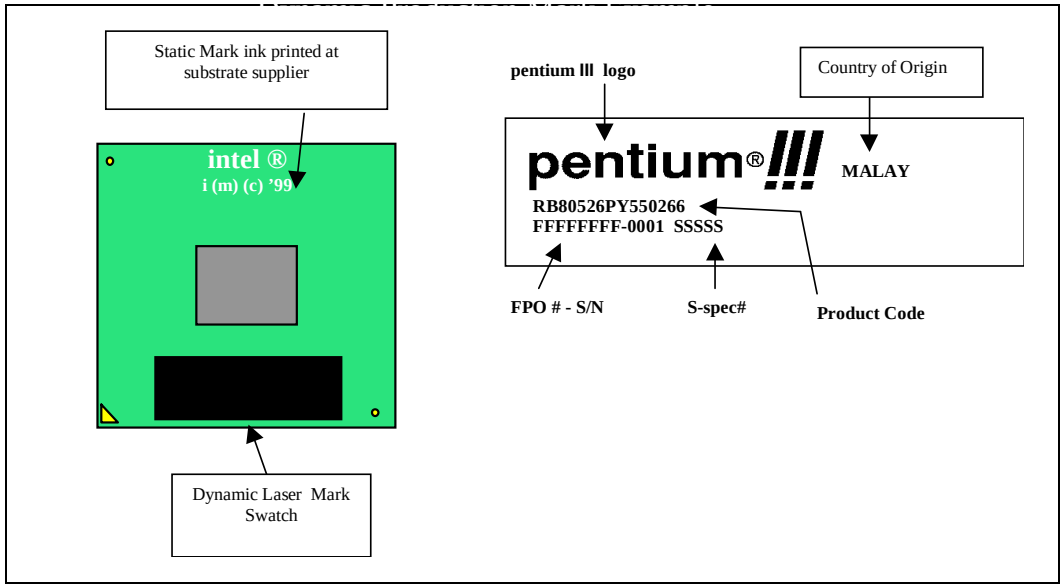
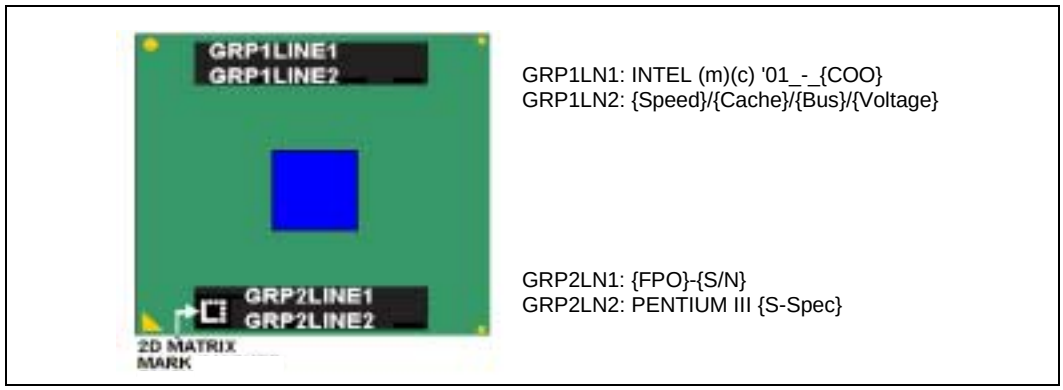


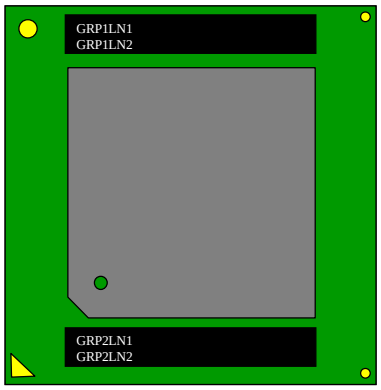
Figure 27. Top Side Processor Markings for FC-PGA (for CPUID 0x68AH))



5.2.1 Processor Markings for FC-PGA2

The following figure exemplifies the processor top-side markings and it is provided to aid in the identification of an Pentium III processor for the FC-PGA2 socket. Table 37 lists the measurements for the package dimensions. (Note: this package label will also have a 2D matrix mark.)

Figure 28. Top Side Processor Markings for FC-PGA2

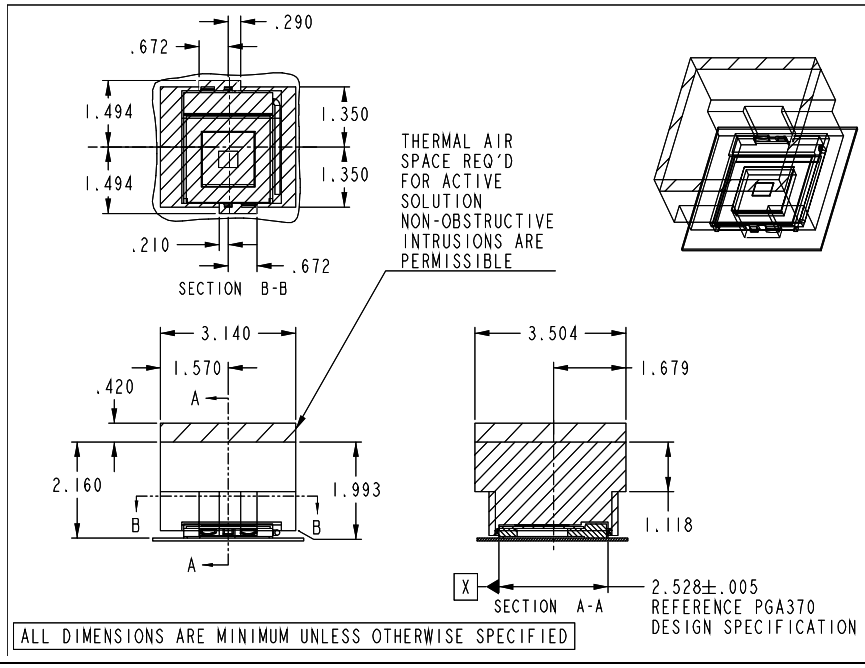


GRP1LN1: INTEL (m)(c) '01_-_{Country of Origin}
GRP1LN2: {Core freq}/{Cache}/{Bus Freq}/{Voltage}

GRP2LN1: {FPO}-{S/N}
GRP2LN2: PENTIUM III {S-Spec}

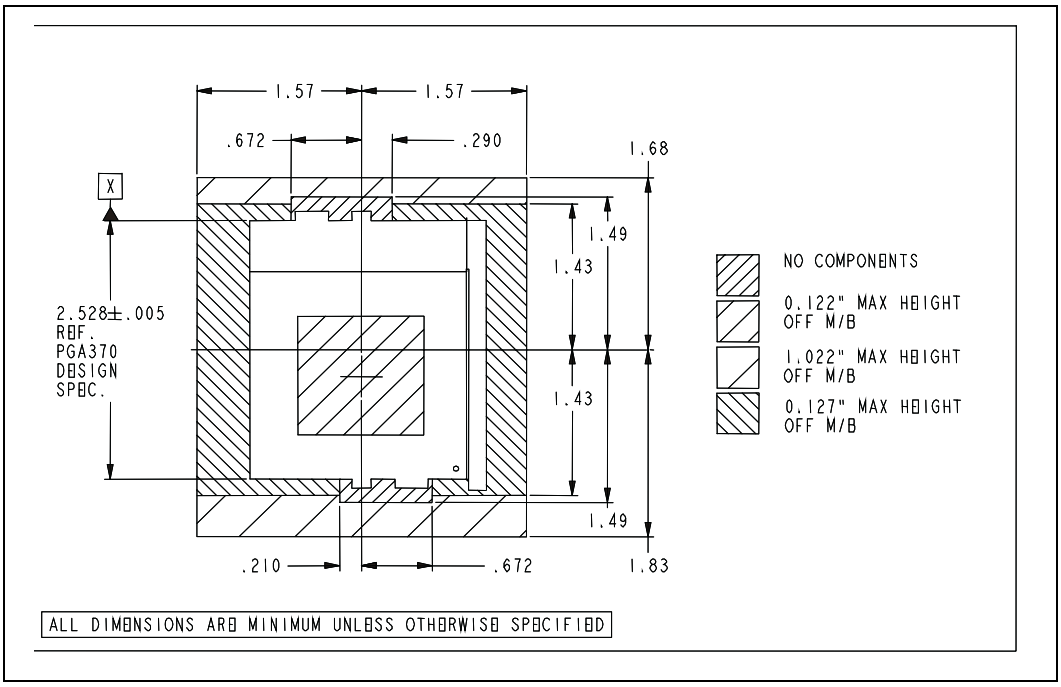
5.3 Recommended Mechanical Keep-Out Zones

Figure 29. Volumetric Keep-Out for FC-PGA and FC-PGA2 [1, 2]



NOTES:
1. This drawing applies to FC-PGA2 package. The only differences from the FC-PGA package Keep-Out drawing are as follows: height 2.160” was changed from 2.100” and height 1.118” was changed from 1.058”.
2. Refer to the Pentium III Thermal/Mechanical Solution Functional Guidelines (see section 1.2 for reference order number) for the latest information.

Figure 30. Component Keep-Out



5.4 Processor Signal Listing

Table 39 and Table 40 provide the processor pin definitions. The signal locations on the PGA370 socket are to be used for signal routing, simulation, and component placement on the baseboard. Figure 31 provides a pin-side view of the Pentium III processor pinout.

Figure 31. Intel® Pentium® III Processor Pinout

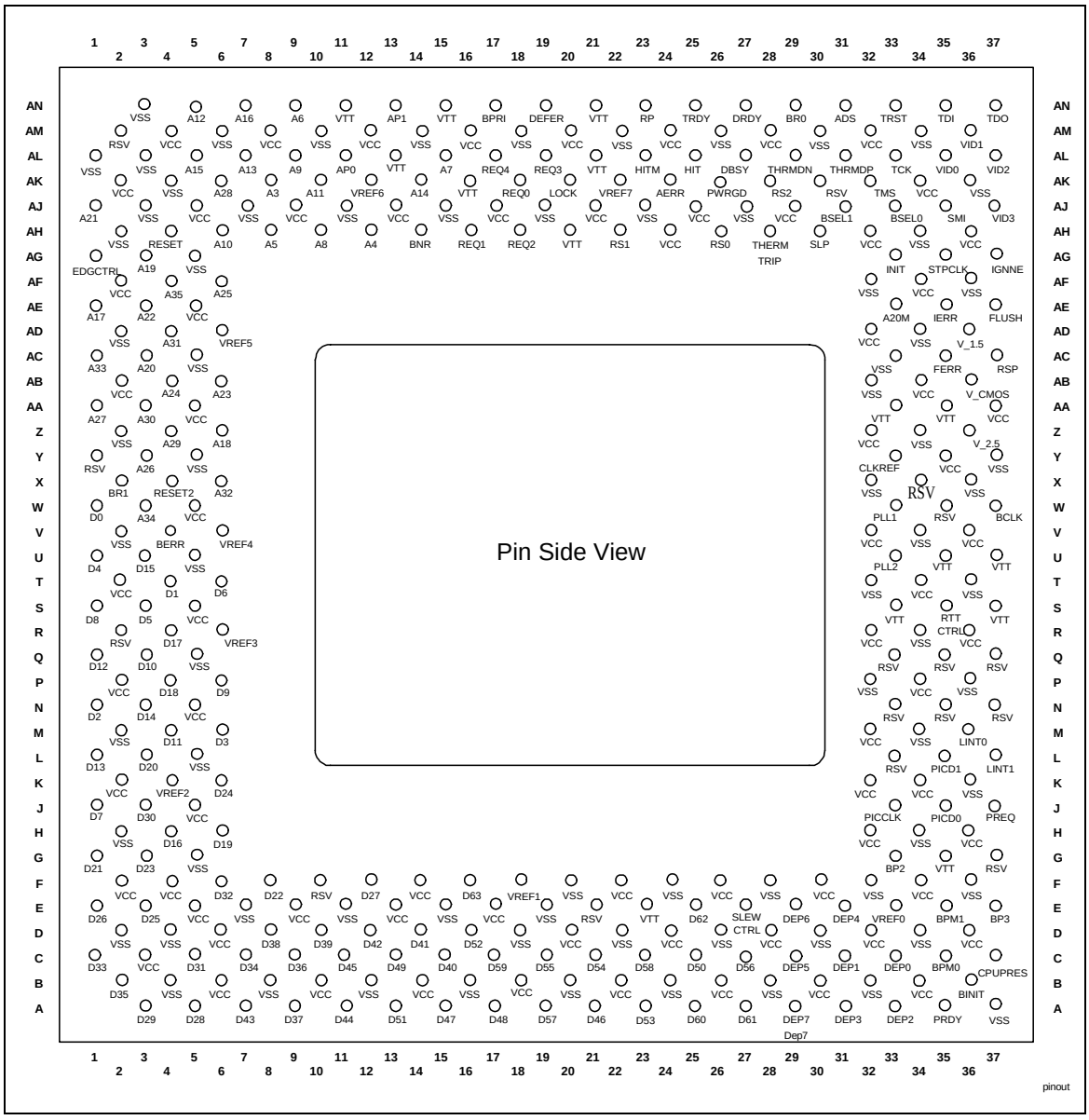


Table 39. Signal Listing in Order by Signal Name

Pin No.	Pin Name	Signal Group
AK8	A3#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AN9	A6#	AGTL+ I/O
AL15	A7#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AL9	A9#	AGTL+ I/O
AH6	A10#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AN5	A12#	AGTL+ I/O
AL7	A13#	AGTL+ I/O
AK14	A14#	AGTL+ I/O
AL5	A15#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AE1	A17#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
AG3	A19#	AGTL+ I/O
AC3	A20#	AGTL+ I/O
AE33	A20M#	CMOS Input
AJ1	A21#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB4	A24#	AGTL+ I/O
AF6	A25#	AGTL+ I/O
Y3	A26#	AGTL+ I/O
AA1	A27#	AGTL+ I/O
AK6	A28#	AGTL+ I/O
Z4	A29#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AD4	A31#	AGTL+ I/O
X6	A32#	AGTL+ I/O
AC1	A33#	AGTL+ I/O
W3	A34#	AGTL+ I/O
AF4	A35#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AK24	AERR#	AGTL+ I/O
AL11	AP0#	AGTL+ I/O
AN13	AP1#	AGTL+ I/O
W37	BCLK	System Bus Clock
V4	BERR#	AGTL+ I/O

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
B36	BINIT#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
G33	BP2#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
C35	BPM0#	AGTL+ I/O
E35	BPM1#	AGTL+ I/O
AN17	BPRI#	AGTL+ Input
AN29	BR0#	AGTL+ I/O
X2	BR1#[8]	AGTL+ Input
AJ33	BSEL0	Power/Other
AJ31	BSEL1	Power/Other
Y33	CLKREF [7]	Power/Other
C37	CPUPRES#	Power/Other
W1	D0#	AGTL+ I/O
T4	D1#	AGTL+ I/O
N1	D2#	AGTL+ I/O
M6	D3#	AGTL+ I/O
U1	D4#	AGTL+ I/O
S3	D5#	AGTL+ I/O
T6	D6#	AGTL+ I/O
J1	D7#	AGTL+ I/O
S1	D8#	AGTL+ I/O
P6	D9#	AGTL+ I/O
Q3	D10#	AGTL+ I/O
M4	D11#	AGTL+ I/O
Q1	D12#	AGTL+ I/O
L1	D13#	AGTL+ I/O
N3	D14#	AGTL+ I/O
U3	D15#	AGTL+ I/O
H4	D16#	AGTL+ I/O
R4	D17#	AGTL+ I/O
P4	D18#	AGTL+ I/O
H6	D19#	AGTL+ I/O
L3	D20#	AGTL+ I/O
G1	D21#	AGTL+ I/O
F8	D22#	AGTL+ I/O
G3	D23#	AGTL+ I/O
K6	D24#	AGTL+ I/O
E3	D25#	AGTL+ I/O
E1	D26#	AGTL+ I/O

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
F12	D27#	AGTL+ I/O
A5	D28#	AGTL+ I/O
A3	D29#	AGTL+ I/O
J3	D30#	AGTL+ I/O
C5	D31#	AGTL+ I/O
F6	D32#	AGTL+ I/O
C1	D33#	AGTL+ I/O
C7	D34#	AGTL+ I/O
B2	D35#	AGTL+ I/O
C9	D36#	AGTL+ I/O
A9	D37#	AGTL+ I/O
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
C15	D40#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D12	D42#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A11	D44#	AGTL+ I/O
C11	D45#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
C13	D49#	AGTL+ I/O
C25	D50#	AGTL+ I/O
A13	D51#	AGTL+ I/O
D16	D52#	AGTL+ I/O
A23	D53#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C27	D56#	AGTL+ I/O
A19	D57#	AGTL+ I/O
C23	D58#	AGTL+ I/O
C17	D59#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
E25	D62#	AGTL+ I/O
F16	D63#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AN19	DEFER#	AGTL+ Input
C33	DEP0#	AGTL+ I/O

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
C31	DEP1#	AGTL+ I/O
A33	DEP2#	AGTL+ I/O
A31	DEP3#	AGTL+ I/O
E31	DEP4#	AGTL+ I/O
C29	DEP5#	AGTL+ I/O
E29	DEP6#	AGTL+ I/O
A29	DEP7#	AGTL+ I/O
AN27	DRDY#	AGTL+ I/O
AG1	EDGCTRL [5]	Power/Other
AC35	FERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AM22	GND	Power/Other
AM26	GND	Power/Other
AM30	GND	Power/Other
AM34	GND	Power/Other
AM6	GND	Power/Other
AN3	GND	Power/Other
B12	GND	Power/Other
B16	GND	Power/Other
B20	GND	Power/Other
B24	GND	Power/Other
B28	GND	Power/Other
B32	GND	Power/Other
B4	GND	Power/Other
B8	GND	Power/Other
D18	GND	Power/Other
D2	GND	Power/Other
D22	GND	Power/Other
D26	GND	Power/Other
D30	GND	Power/Other
D34	GND	Power/Other
D4	GND	Power/Other
E11	GND	Power/Other
E15	GND	Power/Other
E19	GND	Power/Other
E7	GND	Power/Other
F20	GND	Power/Other
F24	GND	Power/Other
F28	GND	Power/Other
F32	GND	Power/Other

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
F36	GND	Power/Other
G5	GND	Power/Other
H2	GND	Power/Other
H34	GND	Power/Other
K36	GND	Power/Other
L5	GND	Power/Other
M2	GND	Power/Other
M34	GND	Power/Other
P32	GND	Power/Other
P36	GND	Power/Other
A37	GND	Power/Other
AB32	GND	Power/Other
AC33	GND	Power/Other
AC5	GND	Power/Other
AD2	GND	Power/Other
AD34	GND	Power/Other
AF32	GND	Power/Other
AF36	GND	Power/Other
AG5	GND	Power/Other
AH2	GND	Power/Other
AH34	GND	Power/Other
AJ11	GND	Power/Other
AJ15	GND	Power/Other
AJ19	GND	Power/Other
AJ23	GND	Power/Other
AJ27	GND	Power/Other
AJ3	GND	Power/Other
AJ7	GND	Power/Other
AK36	GND	Power/Other
AK4	GND	Power/Other
AL1	GND	Power/Other
AL3	GND	Power/Other
AM10	GND	Power/Other
AM14	GND	Power/Other
AM18	GND	Power/Other
Q5	GND	Power/Other
R34	GND	Power/Other
T32	GND	Power/Other
T36	GND	Power/Other
U5	GND	Power/Other

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
V2	GND	Power/Other
V34	GND	Power/Other
X32	GND	Power/Other
X36	GND	Power/Other
Y37	GND	Power/Other
Y5	GND	Power/Other
Z2	GND	Power/Other
Z34	GND	Power/Other
AL25	HIT#	AGTL+ I/O
AL23	HITM#	AGTL+ I/O
AE35	IERR#	CMOS Output
AG37	IGNNE#	CMOS Input
AG33	INIT#	CMOS Input
M36	LINT0/INTR	CMOS Input
L37	LINT1/NMI	CMOS Input
AK20	LOCK#	AGTL+ I/O
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
L35	PICD1	APIC I/O
W33	PLL1	Power/Other
U33	PLL2	Power/Other
A35	PRDY#	AGTL+ Output
J37	PREQ#	CMOS Input
AK26	PWRGOOD	CMOS Input
AK18	REQ0#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
G37	Reserved	Reserved for future use
L33	Reserved	Reserved for future use
N33	Reserved	Reserved for future use
N35	Reserved	Reserved for future use
N37	Reserved	Reserved for future use
Q33	Reserved	Reserved for future use
Q35	Reserved	Reserved for future use
Q37	Reserved	Reserved for future use
R2	Reserved	Reserved for future use
W35	Reserved	Reserved for future use
Y1	Reserved	Reserved for future use

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
AK30	Reserved	Reserved for future use
AM2 [6]	Reserved	Reserved for future use
F10	Reserved	Reserved for future use
X34	Reserved	Reserved for future use
E21	Reserved[11]	Reserved for future use
X2	BR1#[8]	AGTL+ Input
AH4	RESET# [2]	AGTL+ Input
X4	RESET2# [2]	AGTL+ I/O
AN23	RP#	AGTL+ I/O
AH26	RS0#	AGTL + Input
AH22	RS1#	AGTL+ Input
AK28	RS2#	AGTL+ Input
AC37	RSP#	AGTL+ Input
S35	RTTCTRL	Power/Other
E27	SLEWCTRL	Power/Other
AH30	SLP#	CMOS Input
AJ35	SMI#	CMOS Input
AG35	STPCLK#	CMOS Input
AL33	TCK	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AH28	THERMTRIP#	CMOS Output
AK32	TMS	TAP Input
AN25	TRDY#	AGTL+ Input
AN33	TRST#	TAP Input
AD36	$V_{CC1.5}$ [3]	Power/Other
Z36	$V_{CC2.5}$ [1]	Power/Other
AB36	V_{CCCMOS}	Power/Other
AA37	V_{CCCORE}	Power/Other
AA5	V_{CCCORE}	Power/Other
AB2	V_{CCCORE}	Power/Other
AB34	V_{CCCORE}	Power/Other
AD32	V_{CCCORE}	Power/Other
AE5	V_{CCCORE}	Power/Other
E5	V_{CCCORE}	Power/Other
E9	V_{CCCORE}	Power/Other
F14	V_{CCCORE}	Power/Other
F2	V_{CCCORE}	Power/Other

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
F22	V_{CCCORE}	Power/Other
F26	V_{CCCORE}	Power/Other
F30	V_{CCCORE}	Power/Other
F34	V_{CCCORE}	Power/Other
F4	V_{CCCORE}	Power/Other
H32	V_{CCCORE}	Power/Other
H36	V_{CCCORE}	Power/Other
J5	V_{CCCORE}	Power/Other
K2	V_{CCCORE}	Power/Other
K32	V_{CCCORE}	Power/Other
K34	V_{CCCORE}	Power/Other
M32	V_{CCCORE}	Power/Other
N5	V_{CCCORE}	Power/Other
P2	V_{CCCORE}	Power/Other
P34	V_{CCCORE}	Power/Other
R32	V_{CCCORE}	Power/Other
R36	V_{CCCORE}	Power/Other
S5	V_{CCCORE}	Power/Other
T2	V_{CCCORE}	Power/Other
T34	V_{CCCORE}	Power/Other
V32	V_{CCCORE}	Power/Other
V36	V_{CCCORE}	Power/Other
W5	V_{CCCORE}	Power/Other
Y35	V_{CCCORE}	Power/Other
Z32	V_{CCCORE}	Power/Other
AF2	V_{CCCORE}	Power/Other
AF34	V_{CCCORE}	Power/Other
AH24	V_{CCCORE}	Power/Other
AH32	V_{CCCORE}	Power/Other
AH36	V_{CCCORE}	Power/Other
AJ13	V_{CCCORE}	Power/Other
AJ17	V_{CCCORE}	Power/Other
AJ21	V_{CCCORE}	Power/Other
AJ25	V_{CCCORE}	Power/Other
AJ29	V_{CCCORE}	Power/Other
AJ5	V_{CCCORE}	Power/Other
AK2	V_{CCCORE}	Power/Other
AK34	V_{CCCORE}	Power/Other
AM12	V_{CCCORE}	Power/Other
AM16	V_{CCCORE}	Power/Other

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
AM20	$V_{CC_{CORE}}$	Power/Other
AM24	$V_{CC_{CORE}}$	Power/Other
AM28	$V_{CC_{CORE}}$	Power/Other
AM32	$V_{CC_{CORE}}$	Power/Other
AM4	$V_{CC_{CORE}}$	Power/Other
AM8	$V_{CC_{CORE}}$	Power/Other
B10	$V_{CC_{CORE}}$	Power/Other
B14	$V_{CC_{CORE}}$	Power/Other
B18	$V_{CC_{CORE}}$	Power/Other
B22	$V_{CC_{CORE}}$	Power/Other
B26	$V_{CC_{CORE}}$	Power/Other
B30	$V_{CC_{CORE}}$	Power/Other
B34	$V_{CC_{CORE}}$	Power/Other
B6	$V_{CC_{CORE}}$	Power/Other
C3	$V_{CC_{CORE}}$	Power/Other
D20	$V_{CC_{CORE}}$	Power/Other
D24	$V_{CC_{CORE}}$	Power/Other
D28	$V_{CC_{CORE}}$	Power/Other
D32	$V_{CC_{CORE}}$	Power/Other
D36	$V_{CC_{CORE}}$	Power/Other
D6	$V_{CC_{CORE}}$	Power/Other
E13	$V_{CC_{CORE}}$	Power/Other
E17	$V_{CC_{CORE}}$	Power/Other
AJ9	$V_{CC_{CORE}}$	Power/Other
AL35	VID0	Power/Other
AM36	VID1	Power/Other

Table 39. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
AL37	VID2	Power/Other
AJ37	VID3	Power/Other
E33	$V_{REF}0$	Power/Other
F18	$V_{REF}1$	Power/Other
K4	$V_{REF}2$	Power/Other
R6	$V_{REF}3$	Power/Other
V6	$V_{REF}4$	Power/Other
AD6	$V_{REF}5$	Power/Other
AK12	$V_{REF}6$	Power/Other
AK22	$V_{REF}7$	Power/Other
AH20	V_{TT}	Power/Other
AK16	V_{TT}	Power/Other
AL13	V_{TT}	Power/Other
AL21	V_{TT}	Power/Other
AN11	V_{TT}	Power/Other
AN15	V_{TT}	Power/Other
G35	V_{TT}	Power/Other
AA33	V_{TT} [4]	Power/Other
AA35	V_{TT} [4]	Power/Other
AN21	V_{TT} [4]	Power/Other
E23	V_{TT} [4]	Power/Other
S33	V_{TT} [4]	Power/Other
S37	V_{TT} [4]	Power/Other
U35	V_{TT} [4]	Power/Other
U37	V_{TT} [4]	Power/Other

Table 40. Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
A3	D29#	AGTL+ I/O
A5	D28#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A9	D37#	AGTL+ I/O
A11	D44#	AGTL+ I/O
A13	D51#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
A19	D57#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A23	D53#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
A29	DEP7#	AGTL+ I/O
A31	DEP3#	AGTL+ I/O
A33	DEP2#	AGTL+ I/O
A35	PRDY#	AGTL+ Output
A37	GND	Power/Other
AA1	A27#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AA5	$V_{CC_{CORE}}$	Power/Other
AA33	V_{TT} [4]	Power/Other
AA35	V_{TT} [4]	Power/Other
AA37	$V_{CC_{CORE}}$	Power/Other
AB2	$V_{CC_{CORE}}$	Power/Other
AB4	A24#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB32	GND	Power/Other
AB34	$V_{CC_{CORE}}$	Power/Other
AB36	$V_{CC_{CMOS}}$	Power/Other
AC1	A33#	AGTL+ I/O
AC3	A20#	AGTL+ I/O
AC5	GND	Power/Other
AC33	GND	Power/Other
AC35	FERR#	CMOS Output
AC37	RSP#	AGTL+ Input
AD2	GND	Power/Other
AD4	A31#	AGTL+ I/O
AD6	V_{REF}5	Power/Other
AD32	$V_{CC_{CORE}}$	Power/Other

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AD34	GND	Power/Other
AD36	$V_{CC_{1.5}}$ [3]	Power/Other
AE1	A17#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AE5	$V_{CC_{CORE}}$	Power/Other
AE33	A20M#	CMOS Input
AE35	IERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AF2	$V_{CC_{CORE}}$	Power/Other
AF4	A35#	AGTL+ I/O
AF6	A25#	AGTL+ I/O
AF32	GND	Power/Other
AF34	$V_{CC_{CORE}}$	Power/Other
AF36	GND	Power/Other
AG1	EDGCTRL [5]	Power/Other
AG3	A19#	AGTL+ I/O
AG5	GND	Power/Other
AG33	INIT#	CMOS Input
AG35	STPCLK#	CMOS Input
AG37	IGNNE#	CMOS Input
AH2	GND	Power/Other
AH4	RESET# [2]	AGTL+ Input
AH6	A10#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AH20	V_{TT}	Power/Other
AH22	RS1#	AGTL+ Input
AH24	$V_{CC_{CORE}}$	Power/Other
AH26	RS0#	AGTL + Input
AH28	THERMTRIP#	CMOS Output
AH30	SLP#	CMOS Input
AH32	$V_{CC_{CORE}}$	Power/Other
AH34	GND	Power/Other
AH36	$V_{CC_{CORE}}$	Power/Other
AJ1	A21#	AGTL+ I/O
AJ3	GND	Power/Other

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AJ5	$V_{CC_{CORE}}$	Power/Other
AJ7	GND	Power/Other
AJ9	$V_{CC_{CORE}}$	Power/Other
AJ11	GND	Power/Other
AJ13	$V_{CC_{CORE}}$	Power/Other
AJ15	GND	Power/Other
AJ17	$V_{CC_{CORE}}$	Power/Other
AJ19	GND	Power/Other
AJ21	$V_{CC_{CORE}}$	Power/Other
AJ23	GND	Power/Other
AJ25	$V_{CC_{CORE}}$	Power/Other
AJ27	GND	Power/Other
AJ29	$V_{CC_{CORE}}$	Power/Other
AJ31	BSEL1	Power/Other
AJ33	BSEL0	Power/Other
AJ35	SMI#	CMOS Input
AJ37	VID3	Power/Other
AK2	$V_{CC_{CORE}}$	Power/Other
AK4	GND	Power/Other
AK6	A28#	AGTL+ I/O
AK8	A3#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AK12	V_{REF}6	Power/Other
AK14	A14#	AGTL+ I/O
AK16	V_{TT}	Power/Other
AK18	REQ0#	AGTL+ I/O
AK20	LOCK#	AGTL+ I/O
AK22	V_{REF}7	Power/Other
AK24	AERR#	AGTL+ I/O
AK26	PWRGOOD	CMOS Input
AK28	RS2#	AGTL+ Input
AK30	Reserved	Reserved for future use
AK32	TMS	TAP Input
AK34	$V_{CC_{CORE}}$	Power/Other
AK36	GND	Power/Other
AL1	GND	Power/Other
AL3	GND	Power/Other
AL5	A15#	AGTL+ I/O
AL7	A13#	AGTL+ I/O
AL9	A9#	AGTL+ I/O

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AL11	AP0#	AGTL+ I/O
AL13	V_{TT}	Power/Other
AL15	A7#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL21	V_{TT}	Power/Other
AL23	HITM#	AGTL+ I/O
AL25	HIT#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AL33	TCK	TAP Input
AL35	VID0	Power/Other
AL37	VID2	Power/Other
AM2 [6]	Reserved	Reserved for future use
AM4	$V_{CC_{CORE}}$	Power/Other
AM6	GND	Power/Other
AM8	$V_{CC_{CORE}}$	Power/Other
AM10	GND	Power/Other
AM12	$V_{CC_{CORE}}$	Power/Other
AM14	GND	Power/Other
AM16	$V_{CC_{CORE}}$	Power/Other
AM18	GND	Power/Other
AM20	$V_{CC_{CORE}}$	Power/Other
AM22	GND	Power/Other
AM24	$V_{CC_{CORE}}$	Power/Other
AM26	GND	Power/Other
AM28	$V_{CC_{CORE}}$	Power/Other
AM30	GND	Power/Other
AM32	$V_{CC_{CORE}}$	Power/Other
AM34	GND	Power/Other
AM36	VID1	Power/Other
AN3	GND	Power/Other
AN5	A12#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AN9	A6#	AGTL+ I/O
AN11	V_{TT}	Power/Other
AN13	AP1#	AGTL+ I/O
AN15	V_{TT}	Power/Other
AN17	BPRI#	AGTL+ Input

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AN19	DEFER#	AGTL+ Input
AN21	V_{TT} [4]	Power/Other
AN23	RP#	AGTL+ I/O
AN25	TRDY#	AGTL+ Input
AN27	DRDY#	AGTL+ I/O
AN29	BR0#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AN33	TRST#	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
B2	D35#	AGTL+ I/O
B4	GND	Power/Other
B6	$V_{CC_{CORE}}$	Power/Other
B8	GND	Power/Other
B10	$V_{CC_{CORE}}$	Power/Other
B12	GND	Power/Other
B14	$V_{CC_{CORE}}$	Power/Other
B16	GND	Power/Other
B18	$V_{CC_{CORE}}$	Power/Other
B20	GND	Power/Other
B22	$V_{CC_{CORE}}$	Power/Other
B24	GND	Power/Other
B26	$V_{CC_{CORE}}$	Power/Other
B28	GND	Power/Other
B30	$V_{CC_{CORE}}$	Power/Other
B32	GND	Power/Other
B34	$V_{CC_{CORE}}$	Power/Other
B36	BINIT#	AGTL+ I/O
C1	D33#	AGTL+ I/O
C3	$V_{CC_{CORE}}$	Power/Other
C5	D31#	AGTL+ I/O
C7	D34#	AGTL+ I/O
C9	D36#	AGTL+ I/O
C11	D45#	AGTL+ I/O
C13	D49#	AGTL+ I/O
C15	D40#	AGTL+ I/O
C17	D59#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C23	D58#	AGTL+ I/O

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
C25	D50#	AGTL+ I/O
C27	D56#	AGTL+ I/O
C29	DEP5#	AGTL+ I/O
C31	DEP1#	AGTL+ I/O
C33	DEP0#	AGTL+ I/O
C35	BPM0#	AGTL+ I/O
C37	CPUPRES#	Power/Other
D2	GND	Power/Other
D4	GND	Power/Other
D6	$V_{CC_{CORE}}$	Power/Other
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
D12	D42#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D16	D52#	AGTL+ I/O
D18	GND	Power/Other
D20	$V_{CC_{CORE}}$	Power/Other
D22	GND	Power/Other
D24	$V_{CC_{CORE}}$	Power/Other
D26	GND	Power/Other
D28	$V_{CC_{CORE}}$	Power/Other
D30	GND	Power/Other
D32	$V_{CC_{CORE}}$	Power/Other
D34	GND	Power/Other
D36	$V_{CC_{CORE}}$	Power/Other
E1	D26#	AGTL+ I/O
E3	D25#	AGTL+ I/O
E5	$V_{CC_{CORE}}$	Power/Other
E7	GND	Power/Other
E9	$V_{CC_{CORE}}$	Power/Other
E11	GND	Power/Other
E13	$V_{CC_{CORE}}$	Power/Other
E15	GND	Power/Other
E17	$V_{CC_{CORE}}$	Power/Other
E19	GND	Power/Other
E21	Reserved[11]	Reserved for future use
E23	V_{TT} [4]	Power/Other
E25	D62#	AGTL+ I/O
E27	SLEWCTRL	Power/Other
E29	DEP6#	AGTL+ I/O

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
E31	DEP4#	AGTL+ I/O
E33	$V_{REF}0$	Power/Other
E35	BPM1#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
F2	$V_{CC_{CORE}}$	Power/Other
F4	$V_{CC_{CORE}}$	Power/Other
F6	D32#	AGTL+ I/O
F8	D22#	AGTL+ I/O
F10	Reserved	Reserved for future use
F12	D27#	AGTL+ I/O
F14	$V_{CC_{CORE}}$	Power/Other
F16	D63#	AGTL+ I/O
F18	$V_{REF}1$	Power/Other
F20	GND	Power/Other
F22	$V_{CC_{CORE}}$	Power/Other
F24	GND	Power/Other
F26	$V_{CC_{CORE}}$	Power/Other
F28	GND	Power/Other
F30	$V_{CC_{CORE}}$	Power/Other
F32	GND	Power/Other
F34	$V_{CC_{CORE}}$	Power/Other
F36	GND	Power/Other
G1	D21#	AGTL+ I/O
G3	D23#	AGTL+ I/O
G5	GND	Power/Other
G33	BP2#	AGTL+ I/O
G35	V_{TT}	Power/Other
G37	Reserved	Reserved for future use
H2	GND	Power/Other
H4	D16#	AGTL+ I/O
H6	D19#	AGTL+ I/O
H32	$V_{CC_{CORE}}$	Power/Other
H34	GND	Power/Other
H36	$V_{CC_{CORE}}$	Power/Other
J1	D7#	AGTL+ I/O
J3	D30#	AGTL+ I/O
J5	$V_{CC_{CORE}}$	Power/Other
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
J37	PREQ#	CMOS Input

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
K2	$V_{CC_{CORE}}$	Power/Other
K4	$V_{REF}2$	Power/Other
K6	D24#	AGTL+ I/O
K32	$V_{CC_{CORE}}$	Power/Other
K34	$V_{CC_{CORE}}$	Power/Other
K36	GND	Power/Other
L1	D13#	AGTL+ I/O
L3	D20#	AGTL+ I/O
L5	GND	Power/Other
L33	Reserved	Reserved for future use
L35	PICD1	APIC I/O
L37	LINT1/NMI	CMOS Input
M2	GND	Power/Other
M4	D11#	AGTL+ I/O
M6	D3#	AGTL+ I/O
M32	$V_{CC_{CORE}}$	Power/Other
M34	GND	Power/Other
M36	LINT0/INTR	CMOS Input
N1	D2#	AGTL+ I/O
N3	D14#	AGTL+ I/O
N5	$V_{CC_{CORE}}$	Power/Other
N33	Reserved	Reserved for future use
N35	Reserved	Reserved for future use
N37	Reserved	Reserved for future use
P2	$V_{CC_{CORE}}$	Power/Other
P4	D18#	AGTL+ I/O
P6	D9#	AGTL+ I/O
P32	GND	Power/Other
P34	$V_{CC_{CORE}}$	Power/Other
P36	GND	Power/Other
Q1	D12#	AGTL+ I/O
Q3	D10#	AGTL+ I/O
Q5	GND	Power/Other
Q33	Reserved	Reserved for future use
Q35	Reserved	Reserved for future use
Q37	Reserved	Reserved for future use
R2	Reserved	Reserved for future use
R4	D17#	AGTL+ I/O
R6	$V_{REF}3$	Power/Other
R32	$V_{CC_{CORE}}$	Power/Other

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
R34	GND	Power/Other
R36	$V_{CC_{CORE}}$	Power/Other
S1	D8#	AGTL+ I/O
S3	D5#	AGTL+ I/O
S5	$V_{CC_{CORE}}$	Power/Other
S33	V_{TT} [4]	Power/Other
S35	RTTCTRL	Power/Other
S37	V_{TT} [4]	Power/Other
T2	$V_{CC_{CORE}}$	Power/Other
T4	D1#	AGTL+ I/O
T6	D6#	AGTL+ I/O
T32	GND	Power/Other
T34	$V_{CC_{CORE}}$	Power/Other
T36	GND	Power/Other
U1	D4#	AGTL+ I/O
U3	D15#	AGTL+ I/O
U5	GND	Power/Other
U33	PLL2	Power/Other
U35	V_{TT} [4]	Power/Other
U37	V_{TT} [4]	Power/Other
V2	GND	Power/Other
V4	BERR#	AGTL+ I/O
V6	V_{REF}4	Power/Other
V32	$V_{CC_{CORE}}$	Power/Other
V34	GND	Power/Other

Table 40. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
V36	$V_{CC_{CORE}}$	Power/Other
W1	D0#	AGTL+ I/O
W3	A34#	AGTL+ I/O
W5	$V_{CC_{CORE}}$	Power/Other
W33	PLL1	Power/Other
W35	Reserved	Reserved for future use
W37	BCLK	System Bus Clock
X2	BR1#[8]	AGTL+ input
X4	RESET2# [2]	AGTL+ I/O
X6	A32#	AGTL+ I/O
X32	GND	Power/Other
X34	Reserved	Reserved for future use
X36	GND	Power/Other
Y1	Reserved	Reserved for future use
Y3	A26#	AGTL+ I/O
Y5	GND	Power/Other
Y33	CLKREF [7]	Power/Other
Y35	$V_{CC_{CORE}}$	Power/Other
Y37	GND	Power/Other
Z2	GND	Power/Other
Z4	A29#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
Z32	$V_{CC_{CORE}}$	Power/Other
Z34	GND	Power/Other
Z36	$V_{CC_{2.5}}$ [1]	Power/Other

NOTES: See next page for notes.

NOTES:

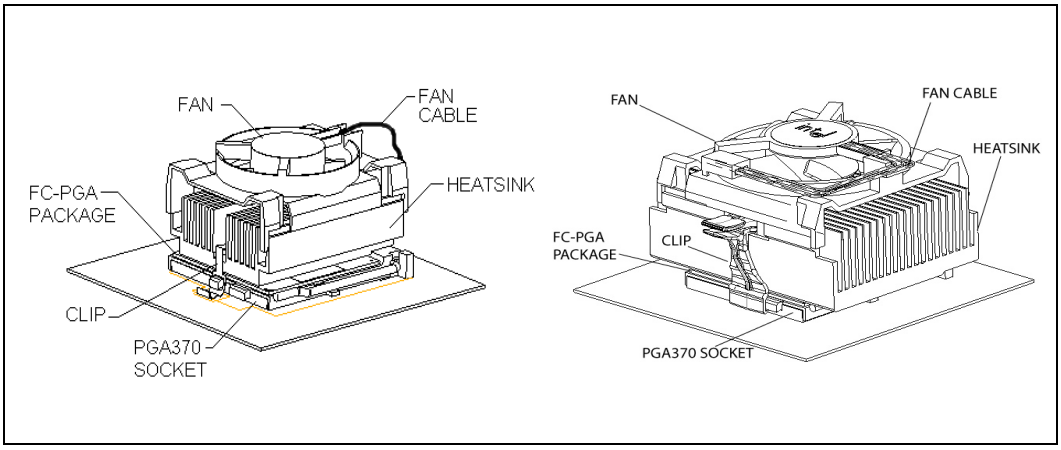
1. These pins are required for backwards compatibility with other Intel processors. They are not used by the Pentium III processor. Refer to the appropriate platform design guide and Section 7.1 for implementation details.
2. RESET# signal must be connected to pins AH4 and X4 for backwards compatibility. Refer to the appropriate platform design guide and Section 7.1 for implementation details. If backwards compatibility is not required, then RESET2# (X4) should be connected to GND.
3. $VCC_{1.5}V$ must be supplied by the same voltage source supplying the V_{TT} pins.
4. These V_{TT} pins must be left unconnected (N/C) for backwards compatibility with Celeron processors (CPUID 066xh). For designs which do not support the Celeron processors (CPUID 066xh), and for compatibility with future processors, these V_{TT} pins should be connected to the V_{TT} plane. Refer to the appropriate platform design guide and Section 7.1 for implementation details. For dual processor designs, these pins must be connected to V_{TT}.
5. This pin is required for backwards compatibility. If backwards compatibility is not required, this pin may be left connected to VCC_{CORE}. Refer to the appropriate platform design guide for implementation details.
6. Previously, PGA370 designs defined this pin as a GND. It is now reserved and must be left unconnected (N/C).
7. Previously, PGA370 socket designs defined this pin as a GND. It is now CLKREF.
8. For Uniprocessor designs, this pin is not used and it is defined as RESERVED. Refer to the *Pentium® III processor Specification Update* for a complete listing of processors that support DP operation.
9. Future low voltage AGTL PGA370 designs will redefine this pin as V_{TT}. Refer to the appropriate platform design guide for connectivity and to the *Pentium® III processor Specification Update* for a complete listing of processors that support the new pinout definition.
10. Future low voltage AGTL PGA370 designs define these pins as GND. Refer to the appropriate platform design guide for connectivity and to the *Pentium® III processor Specification Update* for a complete listing of processors that support the new pinout definition.
11. Future low voltage AGTL PGA370 designs define this pin as RESERVED and must be left unconnected. Refer to the appropriate platform design guide for connectivity.
12. Future low voltage AGTL PGA370 designs will redefine these pins. Refer to the appropriate platform design guide for connectivity and to the *Pentium® III processor Specification Update* for a complete listing of processors that support the new pinout definition.
13. On AGTL and differential clock platforms, this pin is defined as BCLK#.

6.0 Boxed Processor Specifications

The Pentium III processor for the PGA370 socket is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed Pentium III processor for the PGA370 socket will be supplied with an unattached fan heatsink. This section documents motherboard and system requirements for the fan heatsink that will be supplied with the boxed Pentium III processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all heatsinks. It is the system designer's responsibility to consider their proprietary solution when designing to the required keep-out zone on their system platform and chassis. Refer to the *Intel® Pentium® III Processor Thermal/ Mechanical Functional Specifications* for further guidance. Contact your local Intel Sales Representative for this document.

Figure 32. Conceptual Boxed Intel® Pentium® III Processor for the PGA370 Socket



6.1 Mechanical Specifications for the Boxed Intel® Pentium® III Processor

6.1.1 Boxed Processor Thermal Cooling Solution Dimensions

This section documents the mechanical specifications of the boxed Pentium III processor fan heatsink in the FC-PGA package. The boxed processor in the FC-PGA package ships with an un-attached fan heatsink. Figure 32 shows a mechanical representation of the boxed Pentium III processor for the PGA370 socket in the Flip Chip Pin Grid Array (FC-PGA) package.

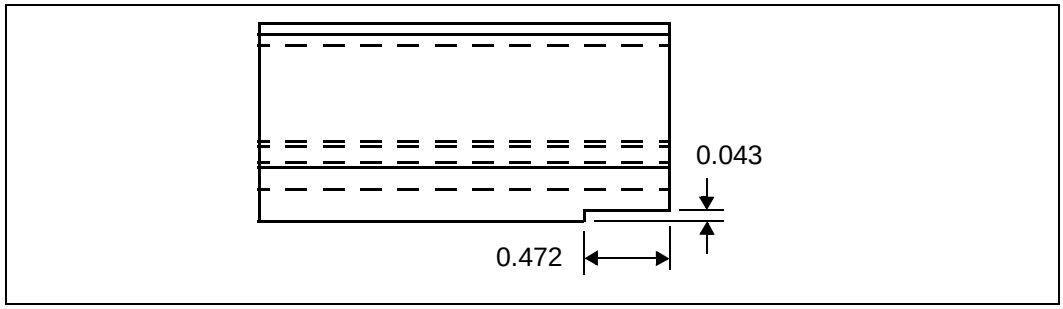
Section 5.3 of this document also shows the recommended mechanical keepout zones for the boxed processor fan heatsink assembly. Figure 30 and Figure 31 show the **required** keepout dimensions for the boxed processor thermal solution. The cooling fin orientation on the heatsink relative to the PGA-370 socket is subject to change. Contact your local Intel Sales Representative for documentation specific to the boxed fan heatsink orientation relative to the PGA-370 socket. Also, contact your Intel representative for specific fan heatsink dimensions.

The fan heatsink is designed to allow visibility of the FC-PGA processor markings located on top of the package. The FC-PGA processor markings are visible after installation of the fan heatsink due to notched sides of the heatsink base (see Figure 34). The boxed processor fan heatsink is also asymmetrical in that the mechanical step feature (see Figure 33) must sit over the socket's cam. The step allows the heatsink to securely interface with the processor in order to meet thermal requirements.

Note: The heatsink airflow keepout zones found in Figure 35 refer specifically to the boxed processor's active fan heatsink. This does not reflect the worst-case dimensions that may exist with other third party passive or active fan heatsinks.

The Pentium III processor is manufactured in two different packages: FC-PGA and FC-PGA2. For specifications on these two packages please see Section 5.0 of this document. Not all frequencies of Pentium III processors are offered in both packages. The thermal solutions for these two packages are incompatible. Therefore, the thermal solution shipped with each boxed Pentium III processor should only be used with the accompanied processor.

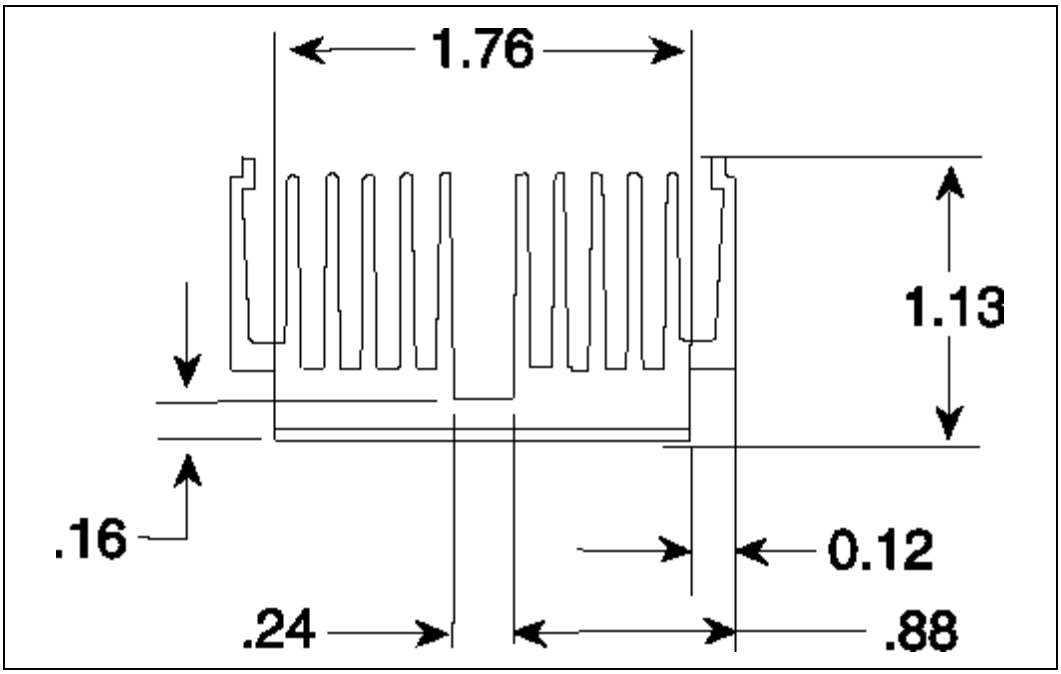
Figure 33. Dimensions of Mechanical Step Feature in Heatsink Base



6.1.2 Boxed Processor Heatsink Weight

The boxed processor thermal cooling solution will not weigh more than 180 grams.

Figure 34. Dimensions of Notches in Heatsink Base



6.1.3 Boxed Processor Thermal Cooling Solution Clip

The boxed processor thermal solution requires installation by a system integrator to secure the thermal cooling solution to the processor after it is installed in the 370-pin socket ZIF socket. Motherboards designed for use by system integrators should take care to consider the implications of clip installation and potential scraping of the motherboard PCB underneath the 370-pin socket attach tabs. Motherboard components should not be placed too close to the 370-pin socket attach tabs in a way that interferes with the installation of the boxed processor thermal cooling solution (see Section 5.3 for specification).

6.2 Thermal Specifications

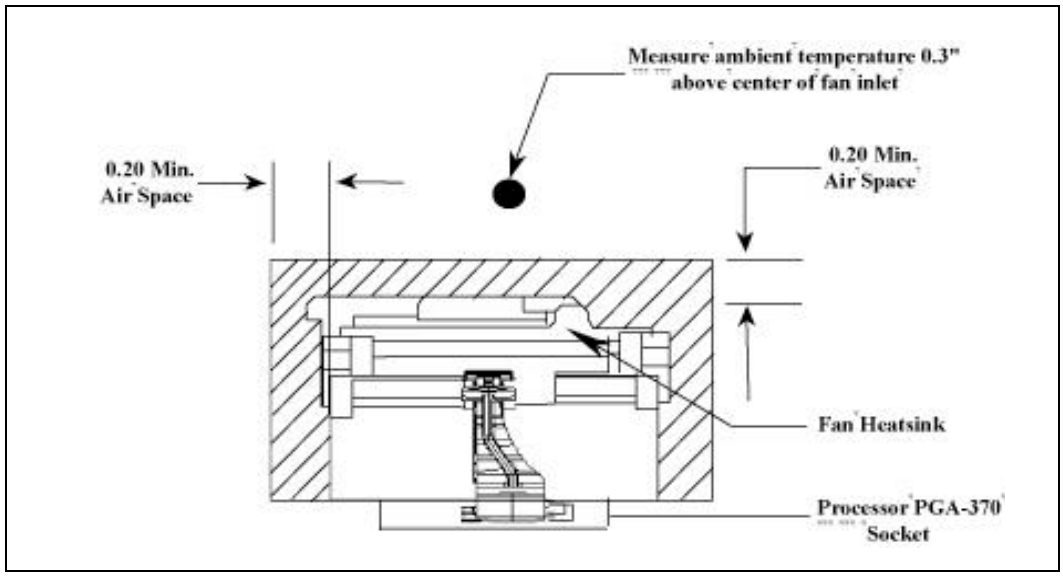
This section describes the cooling requirements of the thermal cooling solution utilized by the boxed processor.

6.2.1 Boxed Processor Cooling Requirements

The boxed processor is directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Section 4.0 of this document. The boxed processor fan heatsink is able to keep the processor core within the specifications (see Table 33 and Table 34) in chassis that provide good thermal management.

For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 35 illustrates an acceptable airspace clearance for the fan heatsink. It is also recommended that the air temperature entering the fan be kept below 45 ^{o} C. Meeting the processor's temperature specification is the responsibility of the system integrator. The processor temperature specification is found in Section 4.0 of this document.

Figure 35. Thermal Airspace Requirement for all Boxed Intel® Pentium® III Processor Fan Heatsinks in the PGA370 Socket



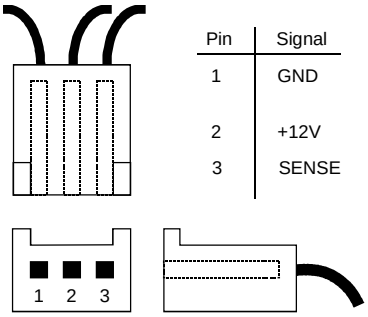
6.3 Electrical Requirements for the Boxed Intel® Pentium® III Processor

6.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable is attached to the fan and will draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 36. Motherboards must provide a matched power header to support the boxed processor. Table 41 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE (open-collector output) signal that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides VOH to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 37 shows the recommended location of the fan power connector relative to the PGA370 socket. The motherboard power header should be positioned within 4.00 inches (lateral) from the center of the PGA370 socket.

Figure 36. Boxed Processor Fan Heatsink Power Cable Connector Description



Pin	Signal
1	GND
2	+12V
3	SENSE

Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pin pitch, 0.025" square pin width.

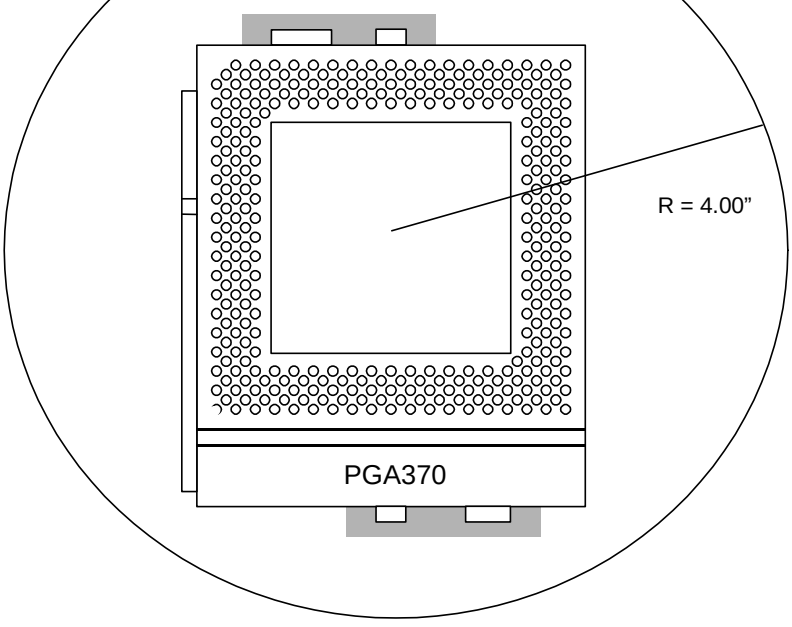
Waldom/Molex P/N 22-01-3037 or equivalent.

Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP P/N 640456-3, or equivalent.

Table 41. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	10.8 V	12 V	13.2 V
IC: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate V_{CC} with resistor)		2 pulses per fan revolution	

Figure 37. Motherboard Power Header Placement Relative to the Boxed Intel® Pentium® III Processor



7.0 Processor Signal Description

This section provides an alphabetical listing of all the Pentium III processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

7.1 Alphabetical Signals Reference

Table 42. Signal Description (Sheet 1 of 8)

Name	Type	Description
A[35:3]#	I/O	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[35:3]# pins to determine their power-on configuration. See the *Intel® Pentium® II Processor Developer's Manual* for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all processor system bus agents.
AERR#	I/O	The AERR# (Address Parity Error) signal is observed and driven by all processor system bus agents, and if used, must connect the appropriate pins on all processor system bus agents. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#, and AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all processor system bus agents.
BCLK/BCLK#	I	The BCLK (Bus Clock) signal determines the bus frequency. All processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Table 42. Signal Description (Sheet 2 of 8)

Name	Type	Description
BERR#	I/O	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents, and must connect the appropriate pins of all such agents, if used. However, Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted optionally for internal errors along with IERR#. • Asserted optionally by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction.
BINIT#	I/O	The BINIT# (Bus Initialization) signal may be observed and driven by all processor system bus agents, and if used must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after Reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.

Table 42. Signal Description (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BR0#
BR1#</td><td>I/O
I</td><td>The BR0# and BR1# (Bus Request) pins drive the BREQ[1:0]# signals in the system. The BREQ[1:0]# signals are interconnected in a rotating manner to individual processor pins. The table below gives the rotating interconnect between the processor and bus signals.

BR0# (I/O) and BR1# Signals Rotating Interconnect
<table><tr><th>Bus Signal</th><th>Agent 0 Pins</th><th>Agent 1 Pins</th></tr><tr><td>BREQ0#</td><td>BR0#</td><td>BR1#</td></tr><tr><td>BREQ1#</td><td>BR1#</td><td>BR0#</td></tr></table>During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[1:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its symmetric agent ID. All agents then configure their pins to match the appropriate bus signal protocol, as shown below.
BR[1:0]# Signal Agent IDs
<table><tr><th>Pin Sampled Active in RESET#</th><th>Agent ID</th></tr><tr><td>BR0#</td><td>0</td></tr><tr><td>BR1#</td><td>3</td></tr></table></td></tr>
<tr><td>BSEL[1:0]</td><td>I/O</td><td>These signals are used to select the system bus frequency. A BSEL[1:0] = “01” selects a 100 MHz system bus frequency and a BSEL[1:0] = “11” selects a 133 MHz system bus frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All system bus agents must operate at the same frequency. The Pentium III processor for the PGA370 socket operates at 100 MHz and 133 MHz system bus frequencies. Individual processors will only operate at their specified front side bus (FSB) frequency. Either 100 MHz or 133 MHz, not both.
On motherboards which support operation at either 66 MHz or 100 MHz, a BSEL[1:0] = “x0” will select a 66 Mhz system bus frequency. 66 MHz operation is not support by the Pentium III processor for the PGA370 socket; therefore, BSEL0 is ignored.
These signals must be pulled up to 2.5 V or 3.3V with 1 KΩ resistors and provided as a frequency selection signal to the clock driver/synthesizer. If the system motherboard is not capable of operating at 133 MHz, it should ground the BSEL1 signal and generate a 100 MHz system bus frequency. See Section 2.8.2 for implementation examples.</td></tr>
<tr><td>CLKREF</td><td>I</td><td>The CLKREF input is a filtered 1.25 V supply voltage for the processor PLL. A voltage divider and decoupling solution is provided by the motherboard. See the design guide for implementation details.</td></tr>
</table>

Table 42. Signal Description (Sheet 4 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>CPUPRES#</td><td>O</td><td>The CPUPRES# signal is defined to allow a system design to detect the presence of a terminator device or processor in a PGA370 socket. Combined with the VID combination of VID[3:0]= 1111 (see Section 2.6), a system can determine if a socket is occupied, and whether a processor core is present. See the table below for states and values for determining the presence of a device.

PGA370 Socket Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
Anything other than ‘1111’</td><td>Processor core installed in the PGA370 socket.</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
1111</td><td>Terminator device installed in the PGA370 socket (i.e., no core present).</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>1
Any value</td><td>PGA370 socket not occupied.</td></tr>
</table></td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DEP[7:0]#</td><td>I/O</td><td>The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor system bus agents which use them. The DEP[7:0]# signals are enabled or disabled for ECC protection during power on configuration.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>EDGCTRL</td><td>O</td><td>The EDGCTRL input adjusts the edge rate of AGTL+ output buffers for previous processors and should be pulled up to $V_{CC_{CORE}}$ with a 51 Ω ±5% resistor. See the platform design guide for implementation details. This signal is not used by the Pentium III processor.</td></tr>
<tr><td>FERR#</td><td>O</td><td>The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel387™ coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.</td></tr>
</table>

Table 42. Signal Description (Sheet 5 of 8)

Name	Type	Description
FLUSH#	I	When the FLUSH# input signal is asserted, processors write back all data in the Modified state from their internal caches and invalidate all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, each processor samples FLUSH# to determine its power-on configuration. See the *P6 Family of Processors Hardware Developer's Manual* for details.
HIT# HITM#	I/O I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1 or L2) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.

Table 42. Signal Description (Sheet 6 of 8)

Name	Type	Description
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of all processors and core logic or I/O APIC components on the APIC bus.
PLL1, PLL2	I	All Pentium III processors have an internal analog PLL clock generator that requires a quiet power supply. PLL1 and PLL2 are inputs to this PLL and must be connected to $V_{CC_{CORE}}$ through a low pass filter that minimizes jitter. See the platform design guide for implementation details.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The PWRGOOD (Power Good) signal is processor input. The processor requires this signal to be a clean indication that the clocks and power supplies ($V_{CC_{CORE}}$, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The figure below illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 19, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their L1 and L2 caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after $V_{CC_{CORE}}$ and CLK have reached their proper specifications. On observing active RESET#, all processor system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the *P6 Family of Processors Hardware Developer's Manual* for details. The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.
RESET2#	I	The RESET2# pin is provided for compatibility with other Intel Architecture processors. The Pentium III processor does not use the RESET2# pin. Refer to the platform design guide for the proper connections of this signal.
RP#	I/O	The RP# (Request Parity) signal is driven by the request initiator, and provides parity protection on ADS# and REQ[4:0]#. It must connect the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.

Table 42. Signal Description (Sheet 7 of 8)

Name	Type	Description
RSP#	I	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
RTTCTRL	I	The RTTCTRL input signal provides AGTL+ termination control. The Pentium III processor samples this input to sense the presence of motherboard AGTL+ termination. See the platform design guide for implementation details.
SLEWCTRL	I	The SLEWCTRL input signal provides AGTL+ slew rate control. The Pentium III processor samples this input to determine the slew rate for AGTL+ signals when it is the driving agent. See the platform design guide for implementation details.
SLP#	I	The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.
SMI#	I	The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I	The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and latch interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units, services pending interrupts while in the Stop-Grant state, and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
THERMDN	O	Thermal Diode Cathode. Used to calculate core (junction) temperature. See Section 4.3.
THERMDP	I	Thermal Diode Anode. Used to calculate core (junction) temperature. See Section 4.3.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped. The system designer should not act upon THERMTRIP# until after RESET# input is de-asserted since, until this time, the THERMTRIP# output is indeterminate.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all processor system bus agents.

Table 42. Signal Description (Sheet 8 of 8)

Name	Type	Description
VID[3:0]	O	The VID[3:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on processors. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
$VCORE_{DET}$	O	The $VCORE_{DET}$ pin indicate the type of processor core present. This pin will float for 2.0 V VCC_{CORE} based processor and will be shorted to V_{SS} for the Pentium III processor.
$VCC_{1.5}$	I	The $VCC_{1.5}$ V input pin provides the termination voltage for CMOS signals interfacing to the processor. The Pentium III processor reroutes the 1.5 V input to the VCC_{CMOS} output via the package. The supply for $VCC_{1.5}$ V must be the same one used to supply V_{TT}.
$VCC_{2.5}$	I	The $VCC_{2.5}$ V input pin provides the termination voltage for CMOS signals interfacing to processors which require 2.5 V termination on the CMOS signals. This signal is not used by the Pentium III processor.
VCC_{CMOS}	O	The VccCMOS pin provides the CMOS voltage for use by the platform and is used for terminating CMOS signals that interface to the processor.
V_{REF}	I	The V_{REF} input pins supply the AGTL+ reference voltage, which is typically 2/3 of V_{TT}. V_{REF} is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1.

7.2 Signal Summaries

Table 43 through Table 46 list attributes of the processor output, input, and I/O signals.

Table 43. Output Signals

Name	Active Level	Clock	Signal Group
CPUPRES#	Low	Asynch	Power/Other
EDGCTRL	N/A	Asynch	Power/Other
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
THERMTRIP#	Low	Asynch	CMOS Output
$VCORE_{DET}$	N/A	Asynch	Power/Other
VID[3:0]	N/A	Asynch	Power/Other

Table 44. Input Signals (Sheet 1 of 2)

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always[1]
BCLK	High	—	System Bus Clock	Always
BPRI#	Low	BCLK	AGTL+ Input	Always
BR1#	Low	BCLK	AGTL+ Input	Always

Table 44. Input Signals (Sheet 2 of 2)

Name	Active Level	Clock	Signal Group	Qualified
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always[1]
IGNNE#	Low	Asynch	CMOS Input	Always[1]
INIT#	Low	Asynch	CMOS Input	Always[1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
RSP#	Low	BCLK	AGTL+ Input	Always
RTTCTRL	N/A	Asynch	Power/Other	
SLEWCTRL	N/A	Asynch	Power/Other	
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:
1. Synchronous assertion with active TDRY# ensures synchronization.

Table 45. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
AP[1:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
BP[3:2]#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
BR0#	Low	BCLK	AGTL+ I/O	Always
BSEL[1:0]	High	Asynch	Power/Other	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DEP[7:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
RP#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 46. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	AGTL+ I/O	ADS#+3
BERR#	Low	BCLK	AGTL+ I/O	Always
BINIT#	Low	BCLK	AGTL+ I/O	Always
BNR#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always