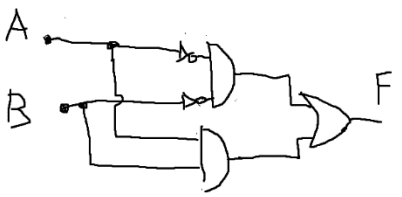
Answer all the questions.

1. Draw the logic gates represented by the Karnaugh Map below. Show your working.

[4]

CD \ AB	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	1	1
10	0	0	1	1



2. An electronics engineer needs a circuit with the following logic.

$(A \wedge B) \vee (\neg A \wedge B) \vee (\neg C \wedge \neg D)$

Complete and use the Karnaugh map below to simplify the expression above.

CD \ AB	00	01	11	10
00				
01				
11				
10				

CD \ AB	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

Simplified expression:

$F = B + \overline{C}\,\overline{D}$

[4]

3(a). Draw an XOR gate.

[1]

(b). Explain the difference in the function of OR and XOR gates.

= OR can be seen as AND/OR connector. One or bot choices can be true or choen. XOR, on the other hand, could be described as real OR . Only one of both choices can be true (or chosen)

[2]

4. A NAND gate and its truth table are shown in Fig. 10.1.

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

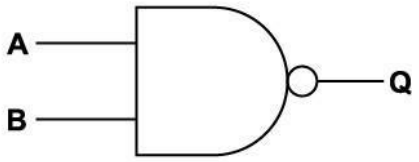
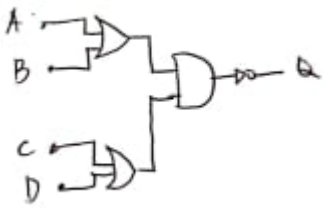


Fig. 10.1

Draw a set of gates equivalent to a NAND gate, but built only of AND, OR and NOT gates.



[2]

END OF QUESTION PAPER