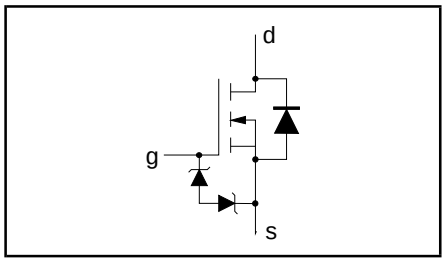
TrenchMOS™ transistor Logic level FET

PHB11N06LT, PHD11N06LT

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 55 V

I_D = 11 A

$R_{DS(ON)} \leq 150\ m\Omega$ (V_{GS} = 5 V)

$R_{DS(ON)} \leq 130\ m\Omega$ (V_{GS} = 10 V)

GENERAL DESCRIPTION

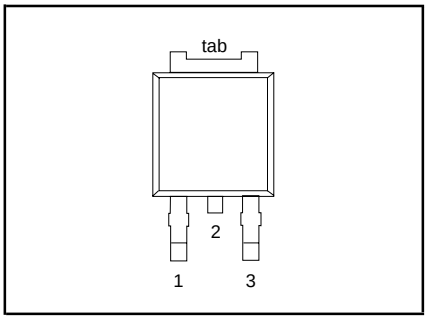
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using '**trench**' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHB11N06LT is supplied in the SOT404 surface mounting package.
The PHD11N06LT is supplied in the SOT428 surface mounting package.

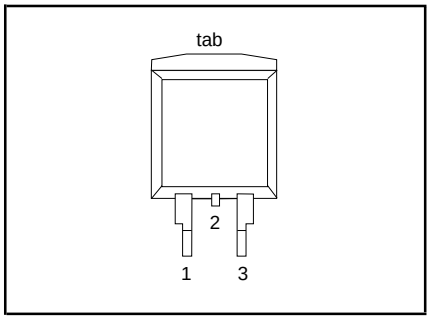
PINNING

PIN	DESCRIPTION
1	gate
2	drain [1]
3	source
tab	drain

SOT428



SOT404



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 ˚C	-	11	A
		T_{mb} = 100 ˚C	-	7.6	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	44	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	36	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	˚C

1 It is not possible to make contact to pin 2 of the SOT404 or SOT428 package

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	4.17	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT78 package, in free air	60	-	K/W
		SOT428 and SOT404 package, pcb mounted, minimum footprint	50	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5.5 A	-	100	130	mΩ
		V_{GS} = 5 V; I_D = 5.5 A	-	120	150	mΩ
		T_j = 175˚C	-	250	315	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5.5 A	4	10	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 11 A; V_{DD} = 44 V; V_{GS} = 5 V	-	6.1	-	nC
Q_{gs}	Gate-source charge		-	1.3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	3.2	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 5 A;	-	6	16	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	23	35	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	18	30	ns
t_f	Turn-off fall time		-	18	30	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	250	330	pF
C_{oss}	Output capacitance		-	34	50	pF
C_{rss}	Feedback capacitance		-	35	50	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	11	A
I_{SM}	Pulsed source current (body diode)		-	-	44	A
V_{SD}	Diode forward voltage	I_F = 11 A; V_{GS} = 0 V	-	0.95	1.2	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	34	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	57	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D \leq 10$ A; $V_{DD} \leq 25$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	10	mJ

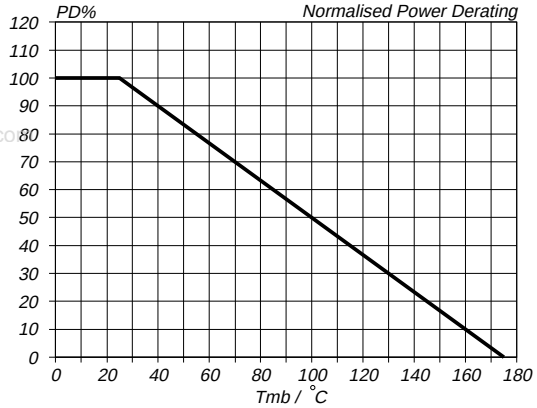


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ °C}$ = f(T_{mb})

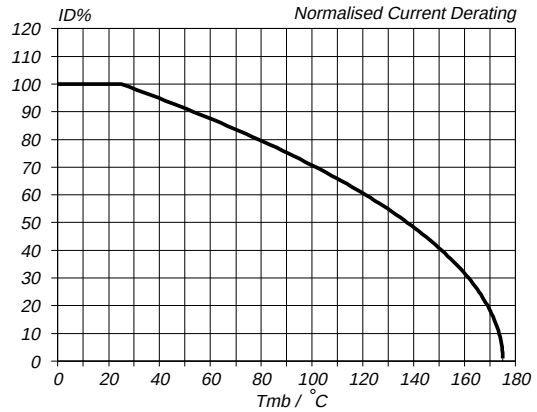


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ °C}$ = f(T_{mb}); conditions: V_{GS} ≥ 5 V

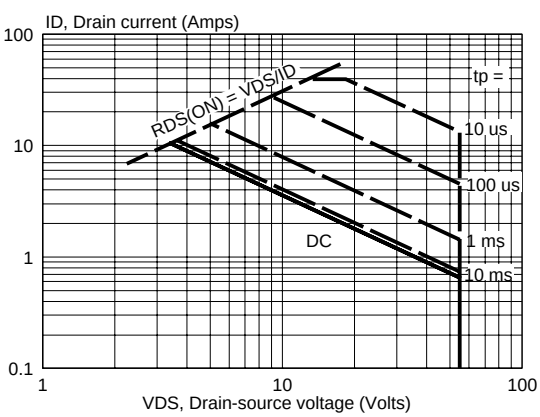


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

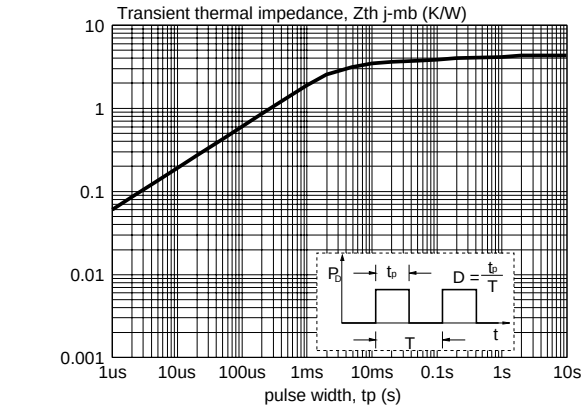


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

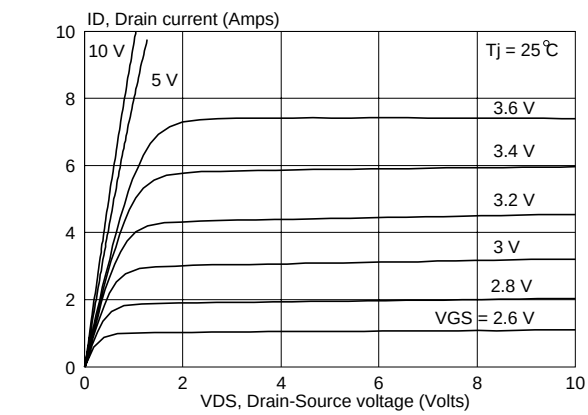


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

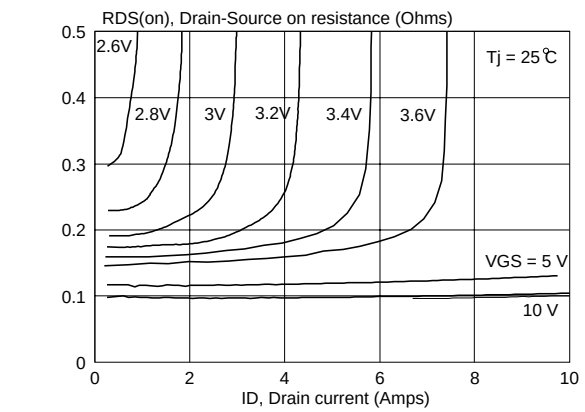


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

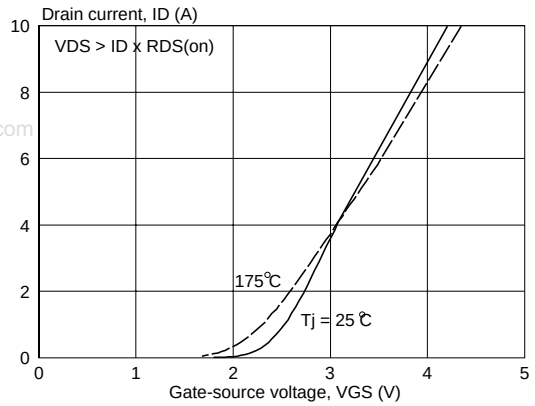


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

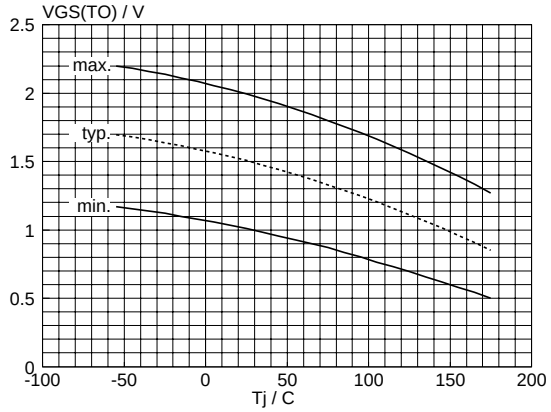


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

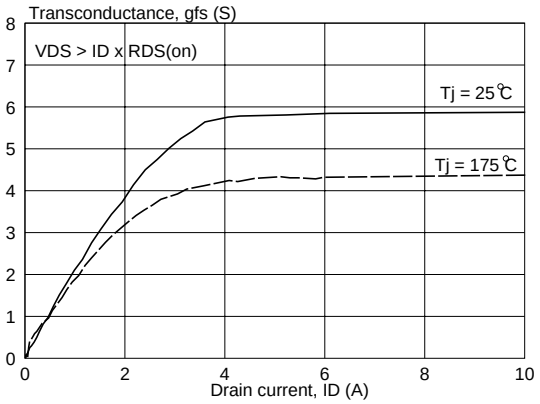


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

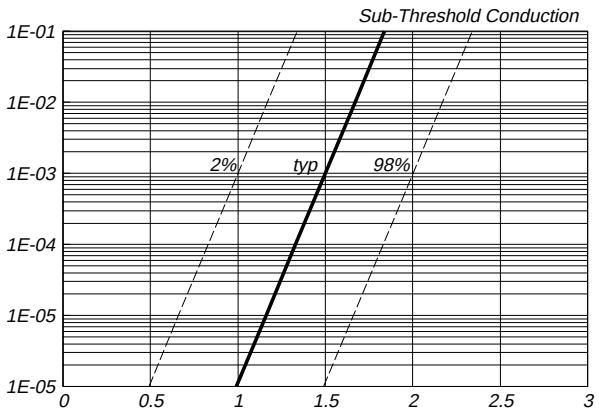


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

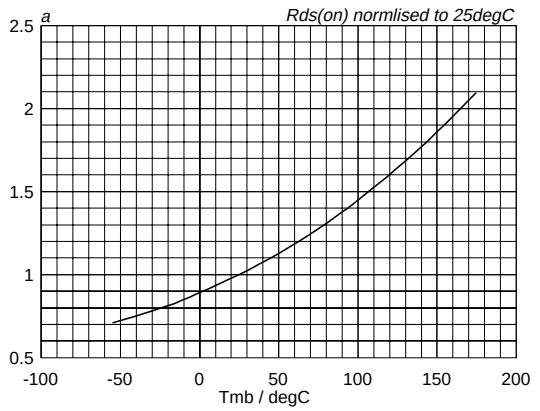


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 5 V

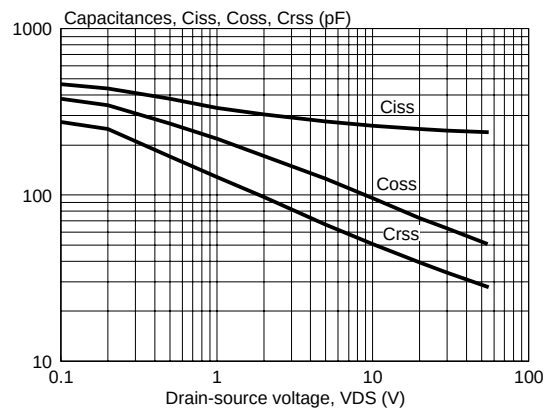


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

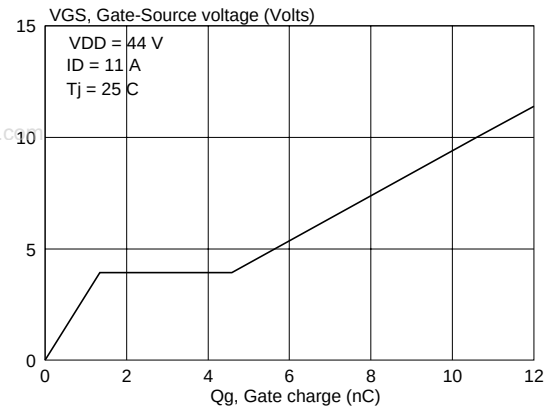


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

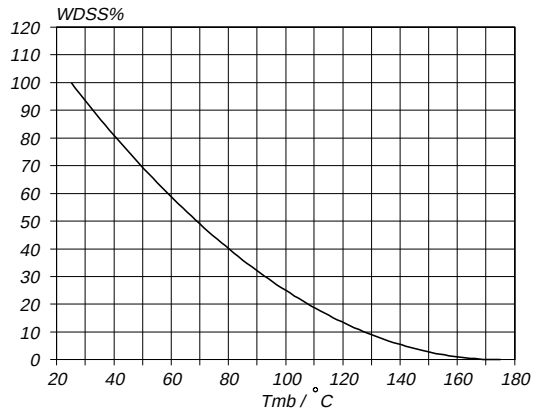


Fig.15. Normalised avalanche energy rating. $W_{DSS}\% = f(T_{mb})$

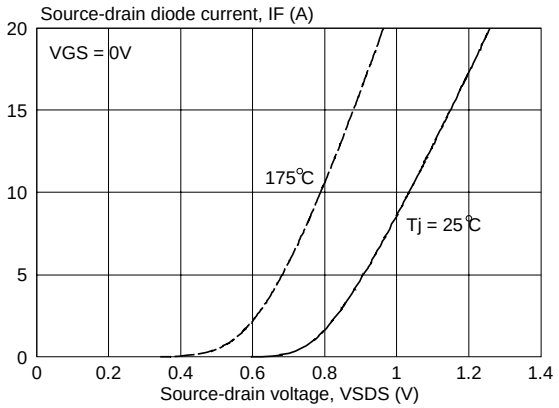


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

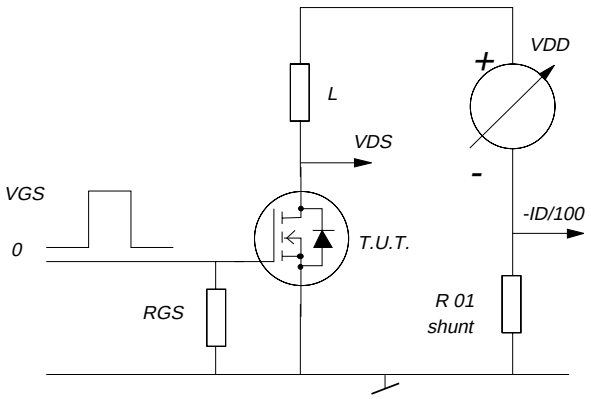


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

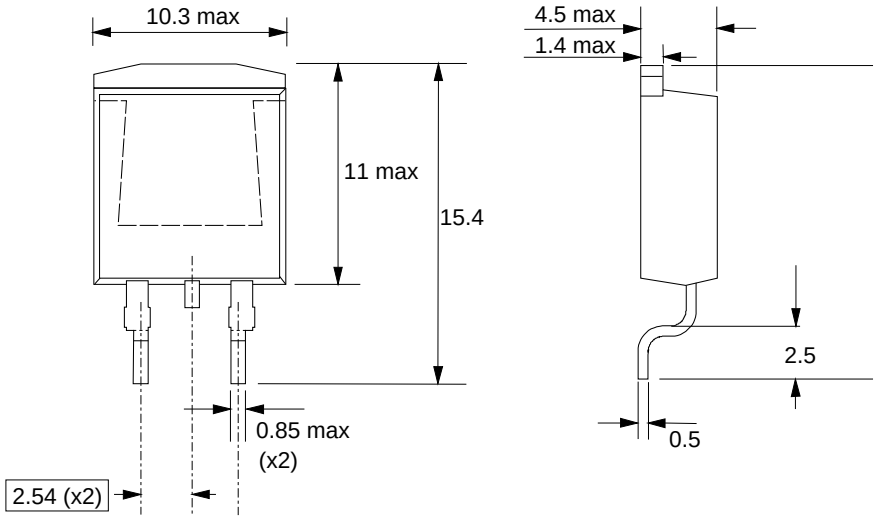


Fig.17. SOT404 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

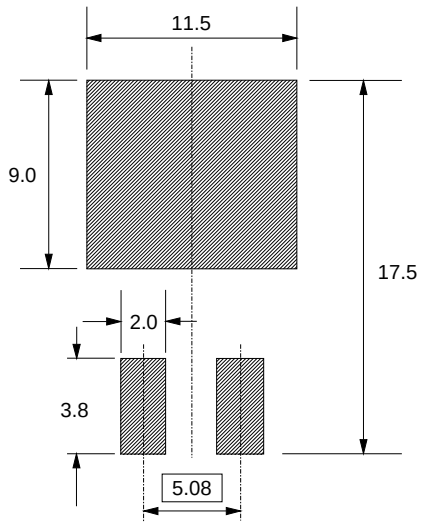


Fig.18. SOT404 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

MECHANICAL DATA

Dimensions in mm : Net Mass: 1.4 g

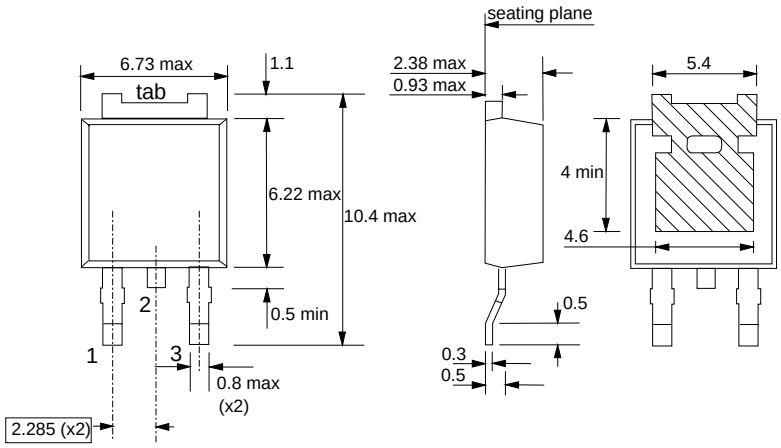


Fig.19. SOT428 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

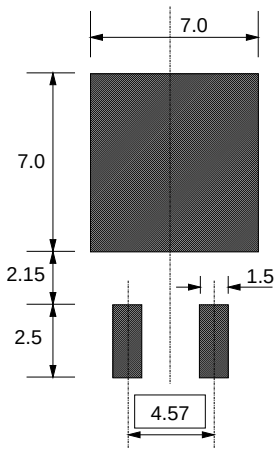


Fig.20. SOT428 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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