Logic Design 2DI4
Lab #1

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.
Submitted by **[Jamin Xu, xu826, 400557470]**

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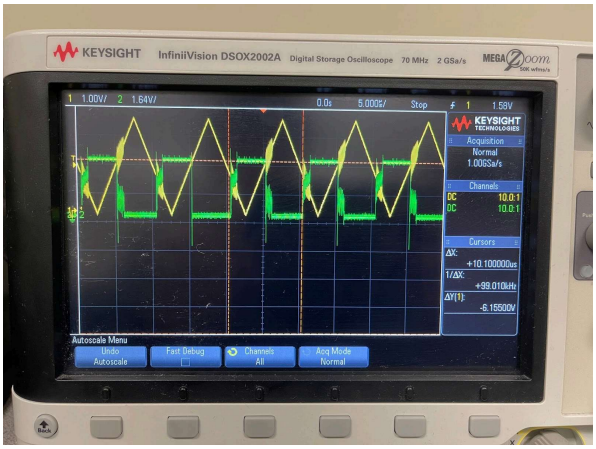
Submitted by **[Kyle Rebello, rebellok, 400590059]**

2. Experiment

Section 4.1

1. Display the function generator's 100kHz triangular wave on channel 1 of the oscilloscope.

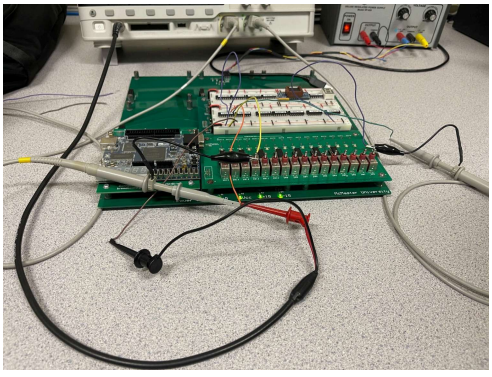
2. Display the output of the NAND gate on channel 2 of the oscilloscope.



3. Using the automatic measuring functions of the digital oscilloscope, state at what input voltage level the output of the NAND changes? Specifically, does the automatic measuring function match the HIGH-SPEED CMOS levels for LO and HI

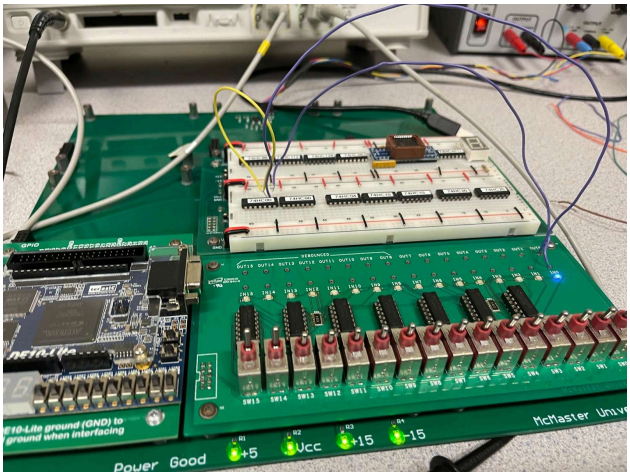
Input Voltage - 1.80V

The output of the NAND changes at 1.8V. We found this by using the cursors to measure the voltage the instant the square waveform changes from low to high. The measuring function does not match the HIGH-SPEED CMOS levels for LO and HI, as there was a delay between the time that the input would change from low to high versus when the output would change from low to high.



Section 4.2

Circuit 1: Not Function



4.

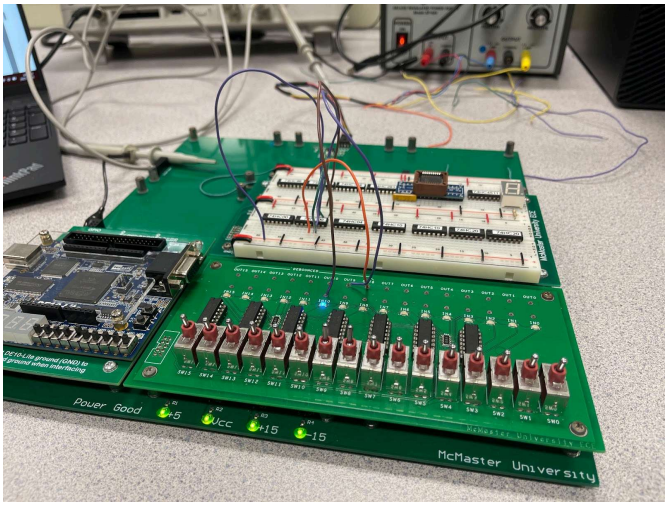
a) Figure 2

$F_1 = (x \cdot x)' = x'$

x	F_1
1	0
0	1

∴ Not function

Circuit 2: And function



b) Figure 3

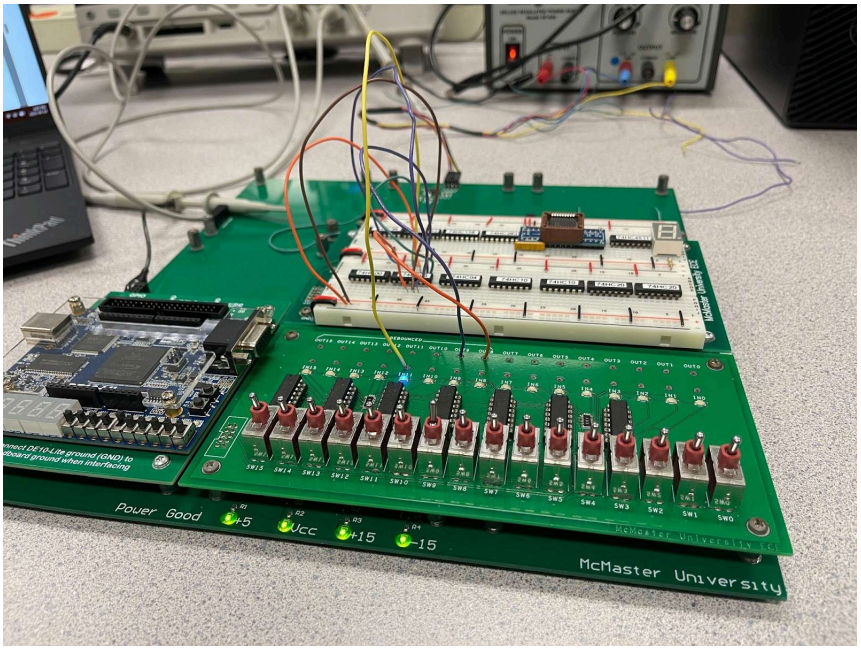
$A = (xy)'$ ← First Nand

$F_2 = (A \cdot 1)' = ((xy)')' = xy$ ← Second Nand

∴ And Function

X	Y	F_2
0	0	0
0	1	0
1	0	0
1	1	1

Circuit 3: Or Function



c) Figure 4

$(x \cdot 1)' = x'$ Top Nand

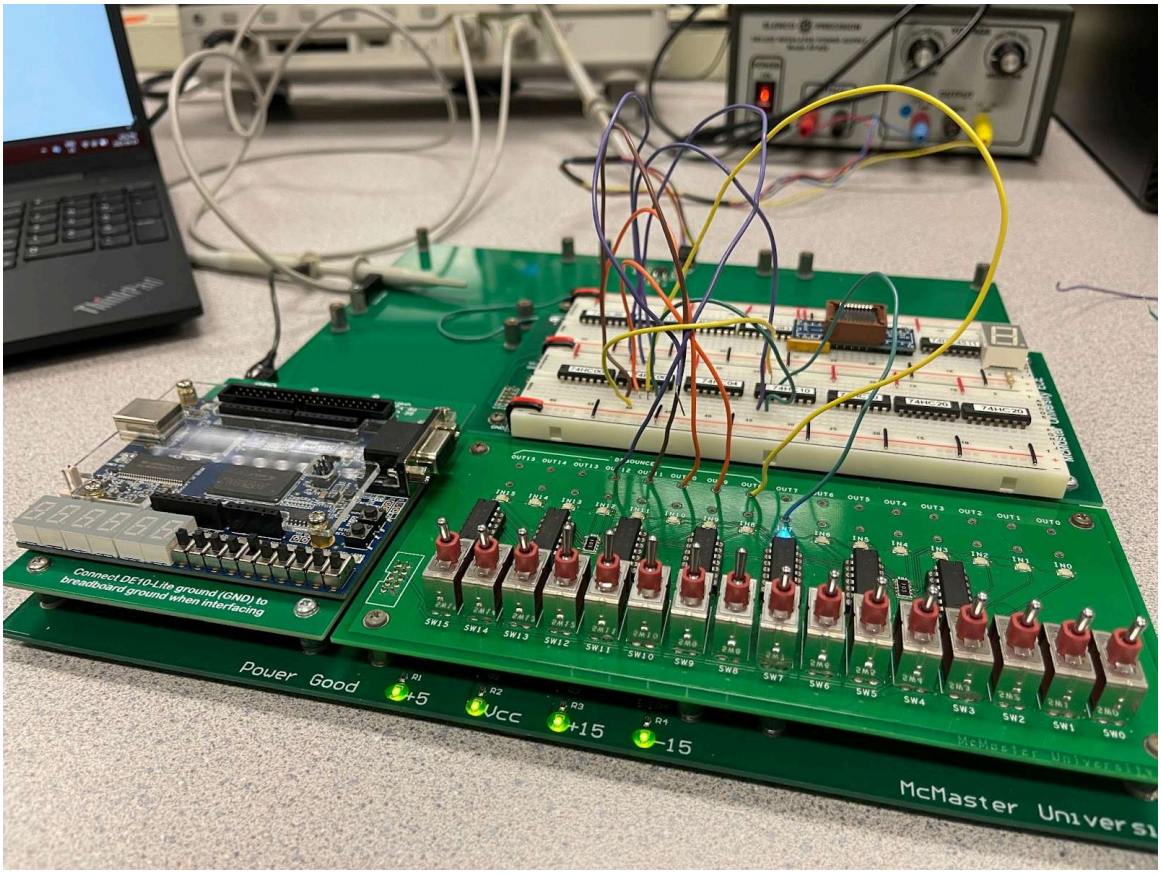
$(y \cdot 1)' = y'$ bottom Nand

$\therefore$ OR function

$F_3 = (x'y')' = x + y$ ← Final Nand

x	y	F_3
0	0	0
0	1	1
1	0	1
1	1	1

Circuit 4: Or of 3 Ands Function


Connect DE10-Lite ground (GND) to breadboard ground when interfacing
Power Good
+5
Vcc
+15
-15
McMaster Universi

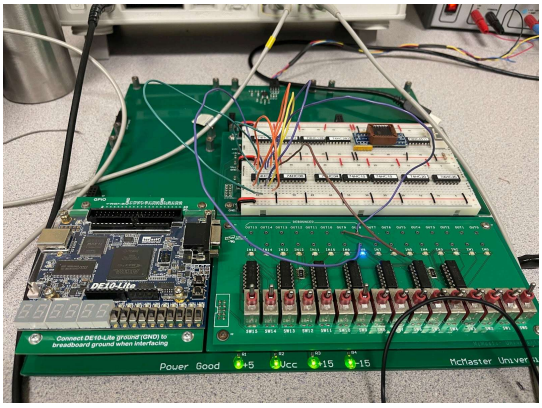
d) Figure 5

Nand1, Nand2, Nand3 = $(wv)'$, $(wx)'$, $(yz)'$

$F_4 = (N1 \cdot N2 \cdot N3)' = (wv) + (wx) + (yz)$ ∴ OR of 3 Ands function

wv	wx	yz	F_4
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Circuit 5: XOR Function



e) Figure 6

$N_{and1} = (xy)' = x' + y'$

$F_5 = ((x \cdot N1)' \cdot (y \cdot N1)')'$ ($N2$, $N3$, N_4)

$= (xN1) + (yN1)$

$= N1(x+y)$

$= (x'+y')(x+y)$

$= xy' + x'y$

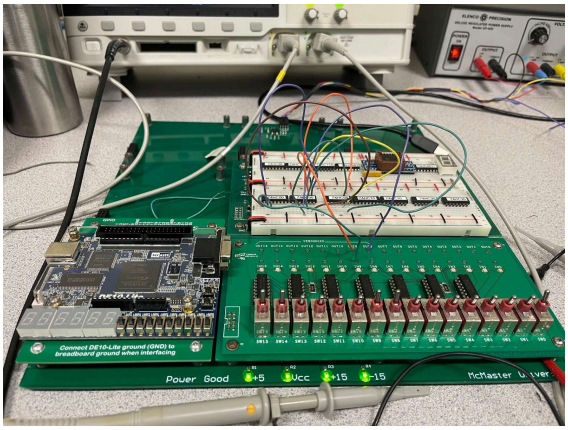
$= x \oplus y$

∴ XOR function

X	y	F_6
0	0	0
0	1	1
1	0	1
1	1	0

Milestone 2: TA checked Circuit 5.

Section 4.3



4.3

5.

Nand1, Nand2 = $(x \cdot y')'$, $(x' \cdot y)'$

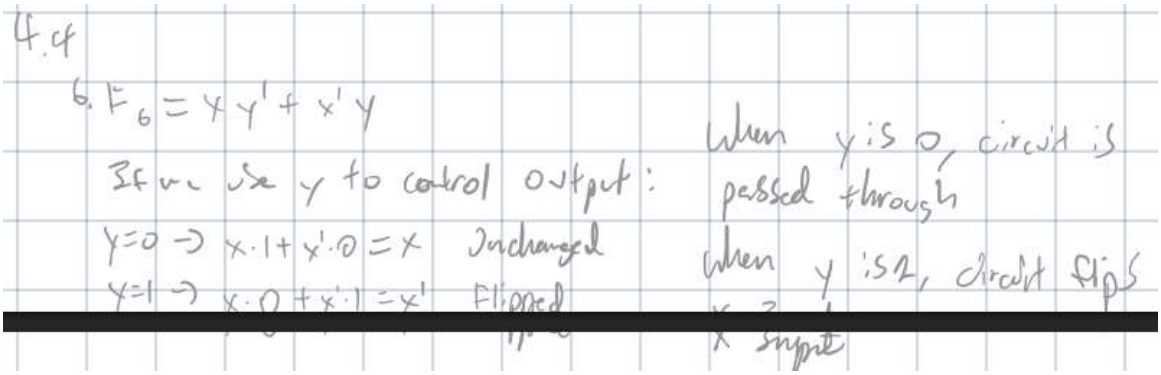
Nand3 = $((x \cdot y')' \cdot (x' \cdot y)')'$

$F_7 = (xy) + (xy') = x \oplus y$ XOR function

X	y	F_6
0	0	0
0	1	1
1	0	1
1	1	0

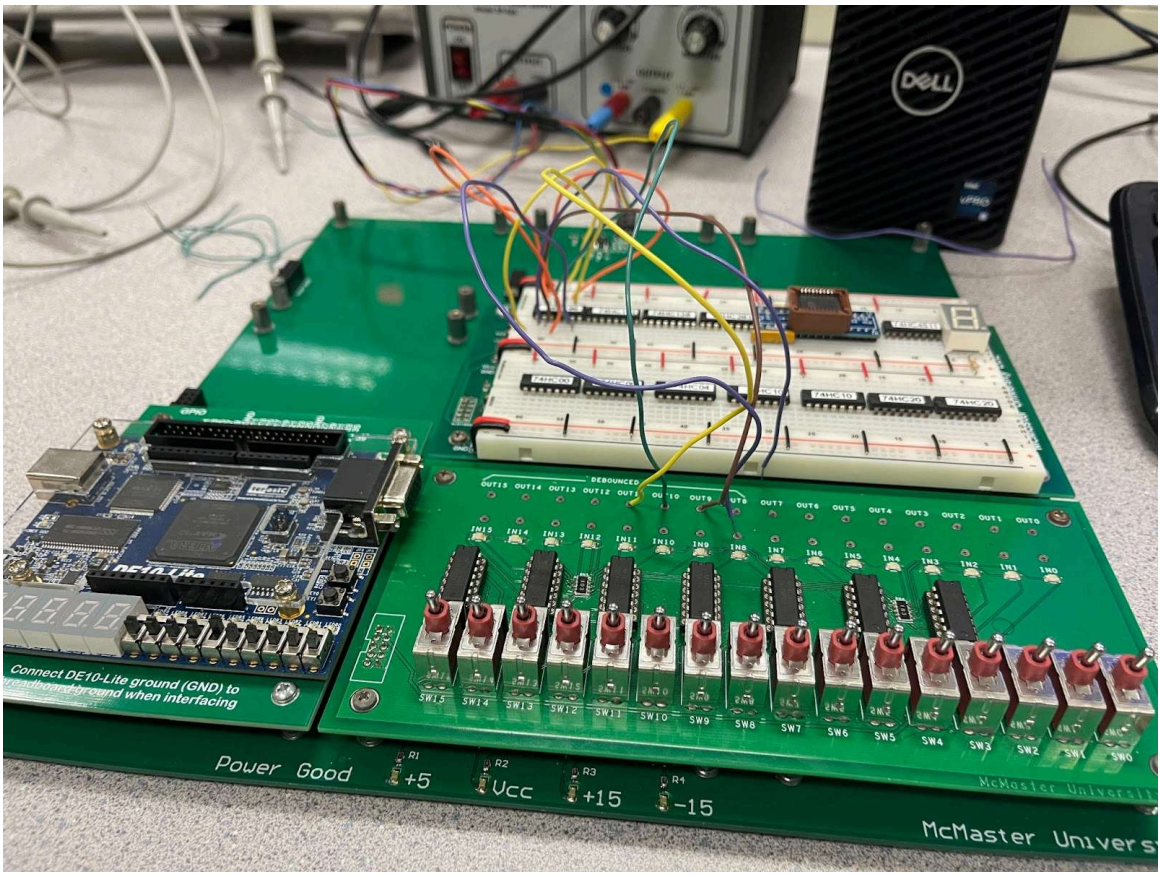
Milestone 3: TA checked Circuit 6.

Section 4.4



When y is o, circuit is passed through
When y is 1, circuit flips x input

Section 4.5

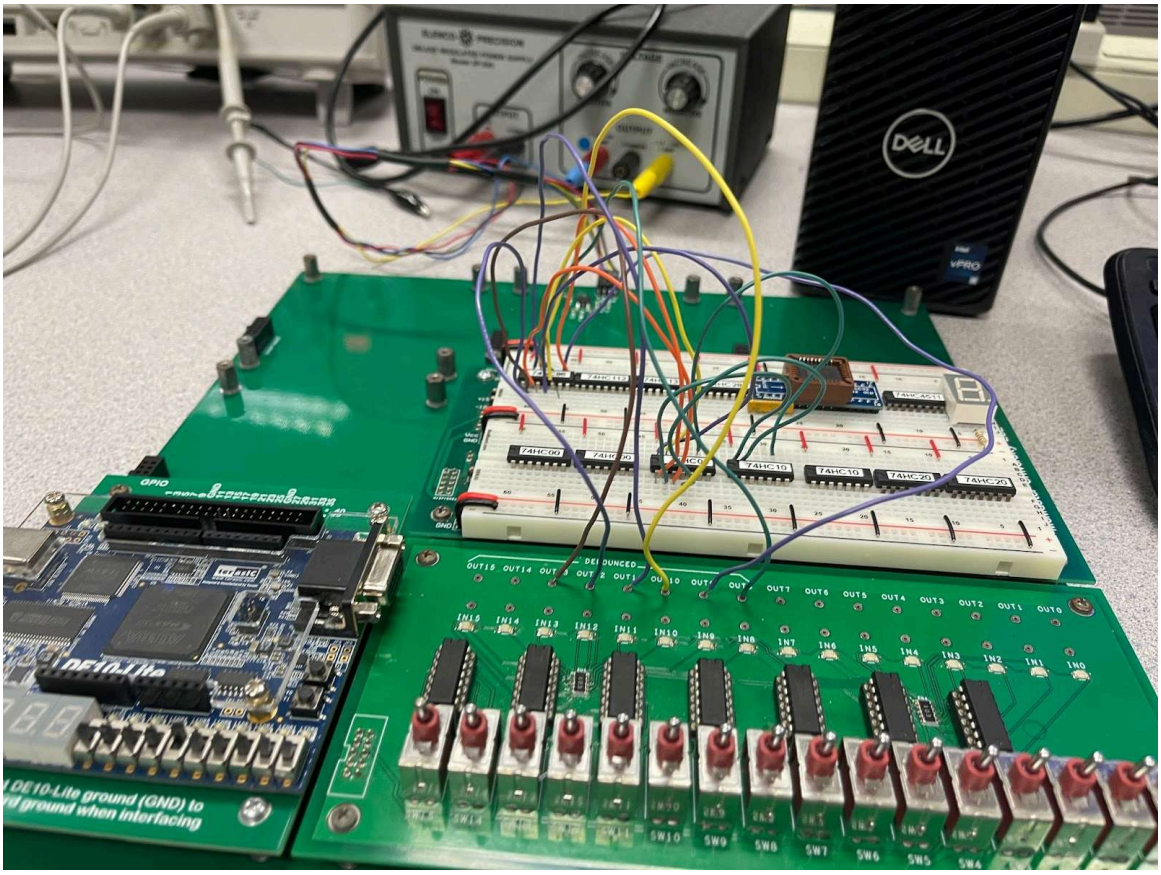


4.5

7.

# of 1	F_{parity}
0	0
1	1
2	0
3	1
4	0

Section 4.6


DELL
74HC00
74HC10
74HC20
DE10-Lite
SW9
SW8
SW7
SW6
SW5
SW4

4.6

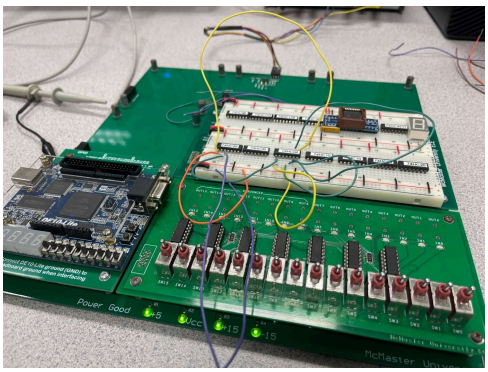
8.

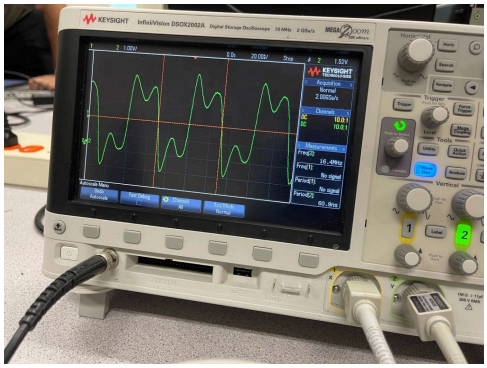
abc	xyz	ax	by	cz	output
000	000	1	1	1	1
001	001	1	1	1	1
101	101	1	1	1	1
101	100	1	1	0	0
011	111	0	1	0	0

Section 4.7

a) Measure and clearly state the time for 1/2 of one cycle of this circuit using the automatic measurement functions of the oscilloscope.

The time for ½ of the period = 30.45 / 4ns(Shows the time per inverter) = 7.6125ns





(b) How does this measured time compare to parameters tPLH and tPHL from the sn74HC00 data sheet? State tPLH and tPHL.

Our measured time per inverter was 7.6125ns, which is pretty close to the reported typical value of 9ns. The Tpd represents the higher of the two values of tPLH and tPHL. This means that our measured time is pretty accurate.

Milestone 4: TA checked measurements.

Section 5.0

Referring back to the Gate Delay Measurement using the pulse Fdelay (see Section 4.7), sketch and explain the output you would expect to see if the NAND in the original circuit were replaced with a NOR gate (you are not required to actually modify the circuit.