CompEng 2DI4
Digital Logic Design
Laboratory 2:
Combinational
Logic

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The manual was prepared to assist in meeting requirements
in the Digital Logic Design undergraduate laboratory.

General Lab Information

Laboratory exercises may offer bonus mark(s) for extra and/or advanced work by the student. The bonus mark(s) will only apply to lab reports that make a clear attempt to meet all non-bonus criteria (including pre-lab). For example, by not attempting to answer a question from the Laboratory Prelab section, the bonus mark(s) will not be considered in evaluation of the exercise. It should also be noted, although the bonuses may make it possible to achieve greater than 100% in the laboratory component of CompEng 2DI4, the maximum grade assigned to the laboratory component will not be greater than 100%.

Labs run every other week of the course. You are required to check Avenue daily to confirm the schedule and receive corrections and/or clarifications to the lab exercises. Pre-labs are due at the beginning of the lab. Laboratory report and code/HDL are due during the student's assigned section. The student is advised that a submission after the laboratory session ends is considered late, no exceptions.

It should be stressed that due to high course enrolment, students shall not be admitted to other laboratory sessions than those assigned. Please enter and exit the lab punctually and pay close attention to the time limits your TAs give you for submitting your lab exercises. Failure to have your lab execution checked because the lab time expired may result in a 0 for the lab – TAs are instructed to not accept/review work that is late. Failure to exit the lab punctually may result in being assigned an automatic zero for the entire lab exercise.

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1.0 Objective

To introduce fundamental concepts of combinational logic and circuit design.

2.0 Pre-Laboratory Preparation [30 marks total]

1. Define the term multiplexer and provide an example of where one would be used in a digital system. [2 marks]
2. Define the term encoder and provide an example of where one would be used in a digital system (not a software system/application). [2 marks]
3. Define the term decoder and provide an example of where one would be used in a digital system (not a software system/application). [2 marks]
4. Define the term binary coded decimal and provide an example of where one would be used in a digital system. [2 marks]
5. Minimize the following Boolean function and draw the circuit diagram (use logic gate symbols) using only NAND gates (HINT: DeMorgan's Theorem is required here).

$$F(a,b,c,d) = \Sigma(0,2,5,7,8,10,13,15)$$

a) Complete the correct K-map of function $F(a,b,c,d)$. [4 marks]
b) Write $F(a,b,c,d)$ in standard form (terms must be correctly ordered in increasing value).[4 marks]
c) Write the minimized Boolean $F(a,b,c,d)$ function using K-map reduction techniques.[4 marks]
d) Write the minimized Boolean $F(a,b,c,d)$ function using ONLY NAND gates. Show how you verified the minimized circuit. [4 marks]
e) Using logic symbols draw the minimized Boolean $F(a,b,c,d)$ function using ONLY NAND gates. [6 marks]

3.0 Integrated Circuits

The following integrated circuits are to be used in this laboratory:

Table 1: Integrated Circuits for Lab 2

Identification	Description
sn74HC00	2-input NAND
sn74HC10	3-input NAND
sn74HC20	4-input NAND
cd74HC4511	BCD-to-7-segment encoder
sn74HC86	2-input XOR
cd74HC283	4-bit binary adder

Obtain the data sheets for each of the above HIGH-SPEED CMOS devices. Familiarize yourself with their logical and electrical characteristics and bring a copy to your lab session.

4.0   Experiment

Read the following experiment and study the circuits as shown.

REQUIRED: Pre-filling your report with the necessary truth tables, tables, circuit diagrams, etc. and structuring your report such that you only need record experimental observations will allow you to focus on the experiment(s). Failing to do this will result in an incomplete lab.

REQUIRED: ENSURE YOUR MILESTONES ARE VISUALLY CHECKED AND RECORDED BY A TA.

4.1   The Karnaugh-Map for Boolean Minimization

1.   Minimize and implement the following function using only NAND gates (note if you design calls for inverter(s) you may use inverter IC to simplify your implementation if you can explain how a NAND can become an inverter):

<mark>Milestone 1: TA to check 1</mark>

$$F(a,b,c,d) = \Sigma(0,2,5,7,8,10,13,15)$$

4.2   The Multiplexer (MUX)

<mark>Milestone 2: TA to check 2</mark>

2.   A MUX is a combination circuit that selects binary information from one of several inputs and logically directs that input to the output channel(s). Complete the following circuit to implement a 4:1 MUX. The input are data lines D_0 to D_3. The select lines are S_0 and S_1 (hint: given two select variables, how many items can you uniquely select?). Output is Y. Build the circuit and verify the function table.

Table 2: 4:1 MUX Function Table

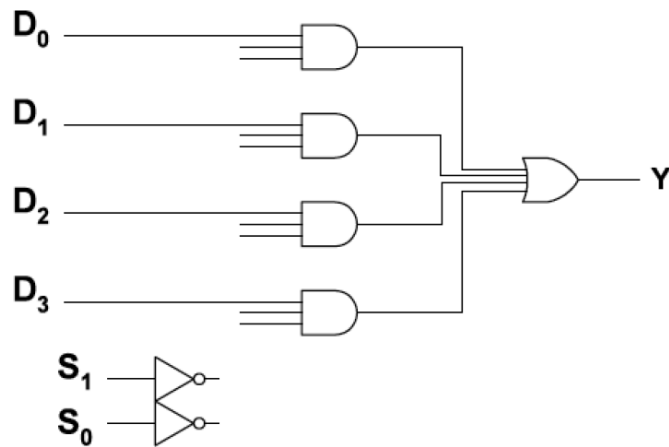| S_1	S_2	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

Figure 1: 4:1 MUX

4.3   Half Adder

3. The fundamental circuit for computation is the half adder. Figure 2 illustrates the half-adder combinational logic circuit. The output S is the sum of inputs A and B, where C_{out} represents a carry out. Build this circuit and verify the truth table. Use switches for inputs and LEDs for output(s).
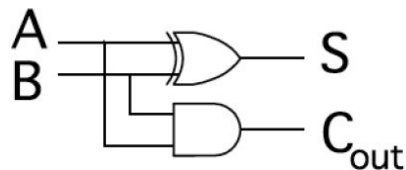

Figure 2: The half-adder

4.4   Full Adder

4. The full adder is a combination of two half-adders to produce a combinational logic circuit with a sum output (S), and a carry output (C_{out}) from inputs A, B, and C_{in}. Figure 3 illustrates the full-adder combinational logic circuit. This arrangement permits fast parallel organization for the addition of n-bit numbers. This circuit is the basis for many arithmetic functions, such as, subtraction, multiplication, and division. Build this circuit and verify the truth table. Use switches for inputs and LEDs for output(s).
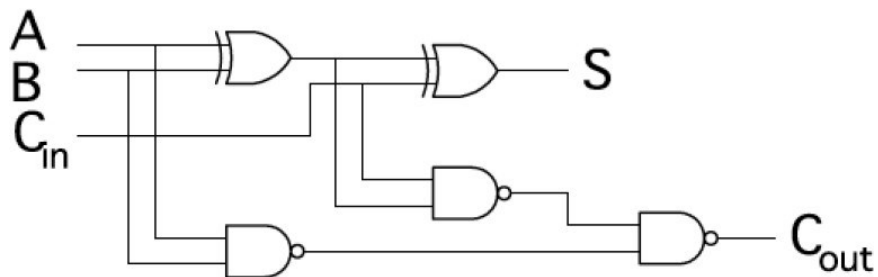

Figure 3: The full-adder

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4.5   n-bit Adder using cd74HC283

5. An *n*-bit adder can be constructed by connecting the carry-out *n* full adders. The input carry to the first full address in the serial chain is C_0 and the output from the final full adder is C_n. Because of the serial carry configuration, this arrangement is often referred to as a ripple carry adder and as a result it has the undesirable characteristic that add time is proportional to *n*. A better approach is to form the sum and carry out in a parallel arrangement, such as the arrangement of the cd74HC283. The cd74HC283 is a 4-bit parallel adder with internal carry look-ahead. Review the data sheet for this IC and note the internal configuration of gates.

    Verify the operation of the cd74HC283 by wiring the IC and completing the table below. Use switches for inputs and LEDs for output(s). Clearly record the output as unsigned and as signed 2's complement.

C0	A	B	Σ	Decimal Equivalent if Σ is unsigned	Decimal Equivalent if Σ is 2's comp	C4
0	0000	0000				
0	0000	0011				
0	0011	0000				
1	0011	0000				
0	0111	1000				
1	0111	1000				
0	1000	1000				
0	0011	1111				
0	0111	1111				
0	1001	1111				
0	1111	1111				
1	1111	1111				

Figure 4: Function table for the cd74HC283

4.6   Addition and Subtraction using cd74HC283

6. A parallel adder may be used to add or subtract 4-bit numbers. Given the following arrangement, when S=0 the output is A+B. When S=1, the output is A-B. Construct and verify this circuit. Explain the operation (hint: what are S and the XORs doing?).

    Note that this adder/subtractor may be used to take the 2's complement of an input B by setting A=0000 and S=1. Verify this for several test cases. This feature will be used in a following circuit so do not disconnect this circuit.
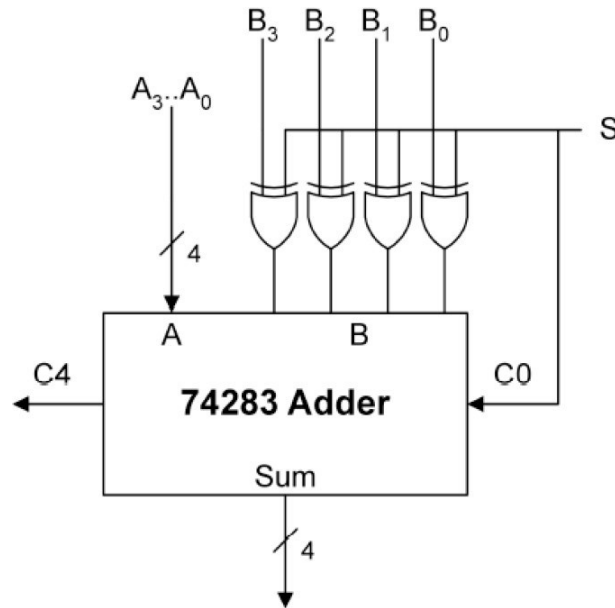
==Milestone 3: TA to check 6==

Figure 5: Addition and Subtraction with the cd74HC283

4.7   Binary Code Decimal and the 7-Segment Display Encoder

7. The seven-segment display is an easy and very common way to display decimal from binary codes. Each segment of the display is lit by pulling the input to the display LO. The cd74HC4511 BCD to 7-segment encoder will drive the display (part number: 157142V12703) with the correct current-limiting requirements. NEVER CONNECT THE DISPLAY INPUTS TO GROUND OR +5V – YOU WILL DESTROY THE DEVICE. Connect the circuit as shown below and leave this circuit connected for use in a following circuit. However, before proceeding you should connect the 4 BCD inputs to 4 sequential toggle switches and verify you understand the device operation.
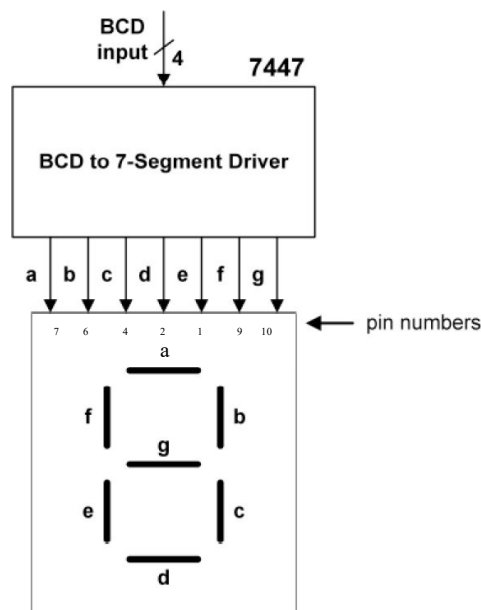

Figure 6: BCD to 7-Segment Display

4.8   BCD, 7-Segment Display, and the 2's Complement

8. Connect the output of the adder/subtractor circuit from Section 4.6 to the input of the cd74HC4511 BCD to 7-segment encoder circuit from Section 4.7.

<mark>Milestone 4: TA to check 8</mark>

4.9   (Bonus) Display the Correct Negative BCD

After completing Milestones 1 to 4, design a combinational logic circuit to correctly display a negative BCD number after cd74HC283 subtraction. To denote a negative, turn on a decimal point on the seven-segment display. You will have to explain your design.

<mark>Bonus Milestone: TA to check bonus design and implementation</mark>

5.0   Submission Requirements

Please ensure you complete the following items prior leaving the laboratory:

1. At the beginning of each lab you are to have your Pre-Lab submitted no later than 2:45pm.
2. Your lab report has a cover page clearly indicating the lab title, date, each member's name, and student number.
3. Cover page must also contain the following statement: As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is our own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.
4. Each experiment milestone has been checked by a TA.
5. One report uploaded per 2-member team. Please ensuring both team members have a copy for future reference.

6.0   TA Grading Table

Component	Weight	Grade
Pre-lab	30	
Milestone 1	10	
Milestone 2	10	
Milestone 3	15	
Milestone 4	15	
Bonus Milestone	10	
Experiment Observations and Report	20	
Total	**100**	
Deductions		
Final Score		