Logic Design 2DI4
Lab #3

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Jamin Xu, xu826, 400557470]**

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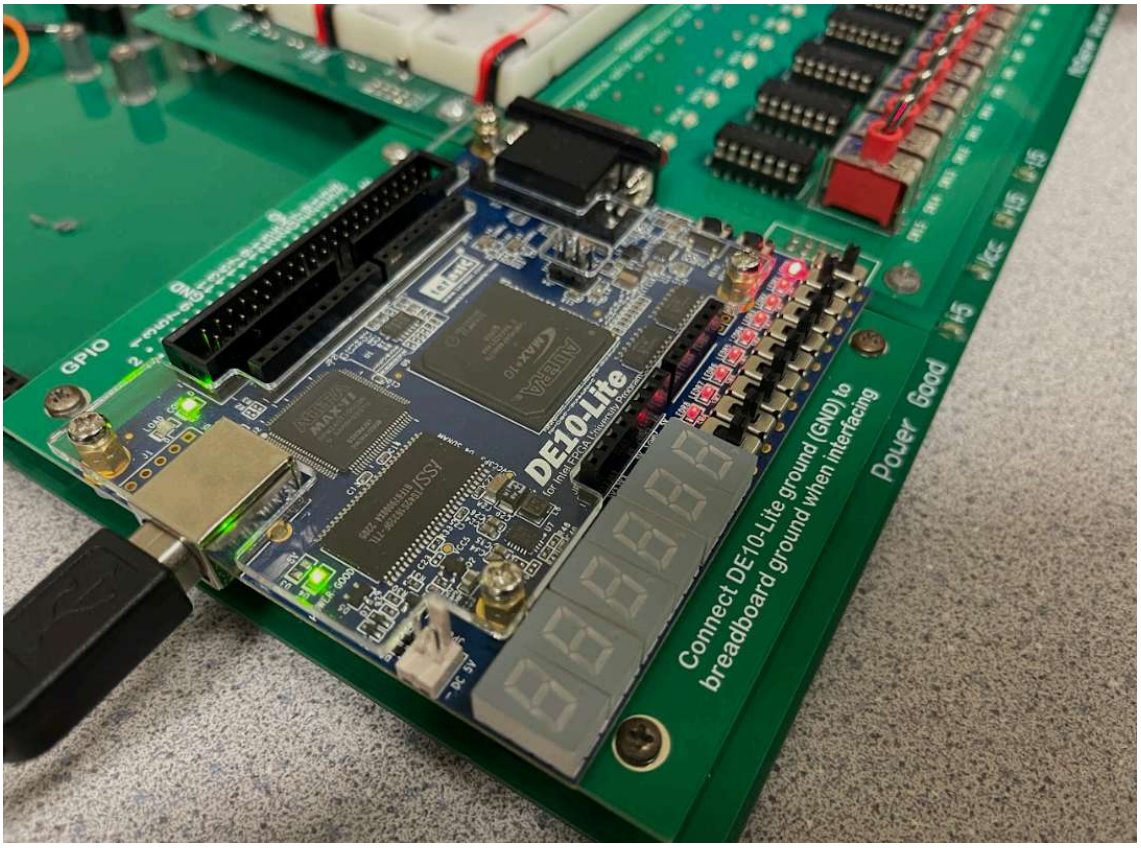
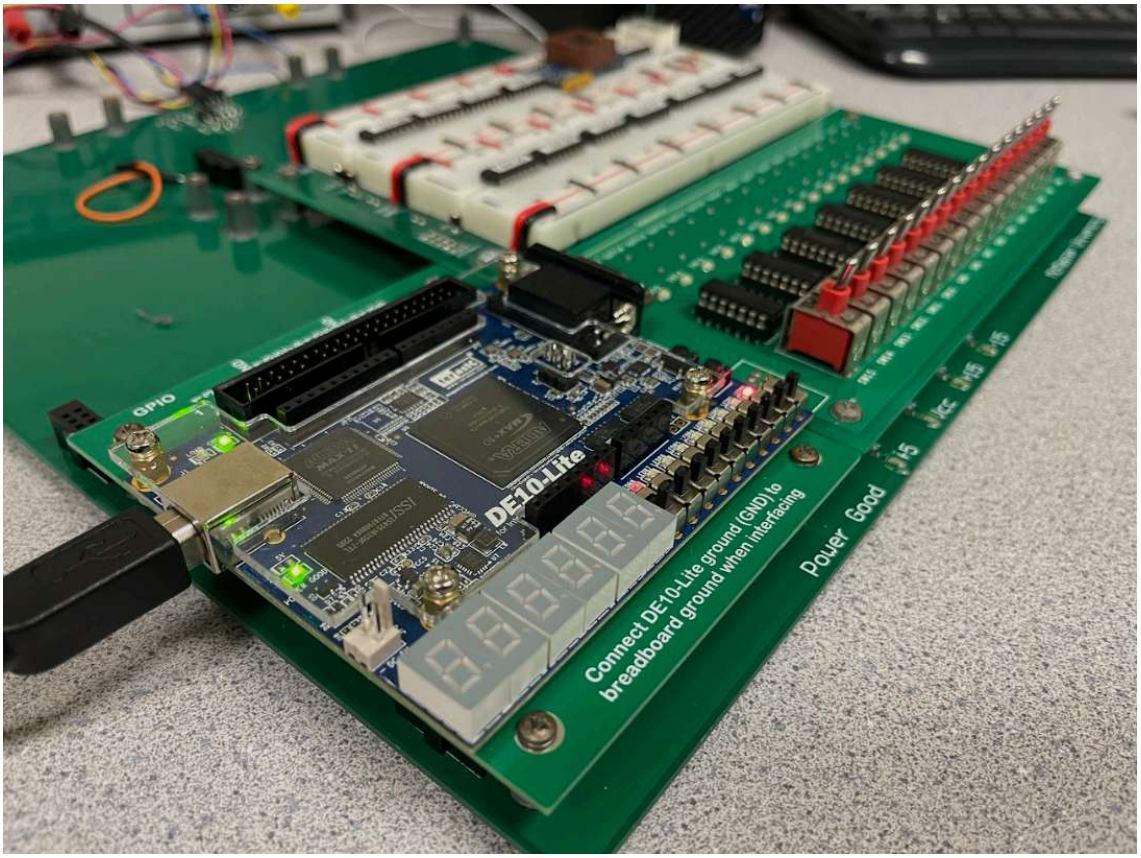
4.1

```
1  // Team: [Jamin Xu] ([400557470]), [Kyle Rebello] ([400590059])
2
3  module prelab1 (x1, x2, f);
4      input x1, x2;
5      output f;
6
7      assign f = (x1 & ~x2) | (~x1 & x2);
8
9  endmodule
```



4.2

```
1   // Milestone 2: 3-to-8 Line Decoder (Dataflow Model)
2   // Team: [Jamin Xu] ([400557470]), [Kyle Rebello] ([400590059])
3
4   module milestone2 (
5       input  x, y, z,    // 3 inputs
6       output D0, D1, D2, D3, D4, D5, D6, D7 // 8 outputs
7   );
8
9       // Create internal wires for the inverted signals (from the NOT gates)
10      wire x_n, y_n, z_n;
11
12      assign x_n = ~x;
13      assign y_n = ~y;
14      assign z_n = ~z;
15
16      assign D0 = x_n & y_n & z_n;  // D0 = x'y'z'
17      assign D1 = x_n & y_n & z;    // D1 = x'y'z
18      assign D2 = x_n & y & z_n;    // D2 = x'yz'
19      assign D3 = x_n & y & z;     // D3 = x'yz
20      assign D4 = x & y_n & z_n;    // D4 = xy'z'
21      assign D5 = x & y_n & z;     // D5 = xy'z
22      assign D6 = x & y & z_n;     // D6 = xyz'
23      assign D7 = x & y & z;      // D7 = xyz
24
25  endmodule
```



4.3

```
// Team: [Jamin Xu] ([400557470]), [Kyle Rebello] ([400590059])

module milestone3 (
    input  in1, in0,    // 2-bit binary input

    // 7-segment outputs (active-high)
    output a, b, c, d, e, f, g
);

    // Minimized equations from Pre-Lab Q3 K-Maps
    assign a = ~((~in0) | (in1));          // a = in0' + in1
    assign b = ~(1'b1);                    // b = 1
    assign c = ~((~in1) | (in0));          // c = in1' + in0
    assign d = ~((~in0) | (in1));          // d = in0 + in1'
    assign e = ~(~in0);                   // e = in0'
    assign f = ~((~in1) & (~in0));         // f = in1' & in0'
    assign g = ~(in1);                    // g = in1

endmodule
```