CompEng 2DI4
Digital Logic Design
Laboratory 1:
Logic Gates

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The manual was prepared to assist in meeting requirements
in the Digital Logic Design undergraduate laboratory.

General Lab Information

Laboratory exercises may offer bonus mark(s) for extra and/or advanced work by the student. The bonus mark(s) will only apply to lab reports that make a clear attempt to meet all non-bonus criteria (including pre-lab). For example, by not attempting to answer a question from the Laboratory Prelab section, the bonus mark(s) will not be considered in evaluation of the exercise. It should also be noted, although the bonuses may make it possible to achieve greater than 100% in the laboratory component of CompEng 2DI4, the maximum grade assigned to the laboratory component will not be greater than 100%.

Labs run every other week of the course. You are required to check Avenue daily to confirm the schedule and receive corrections and/or clarifications to the lab exercises. Pre-labs are due at the beginning of the lab. Laboratory report and code/HDL are due during the student's assigned section. The student is advised that a submission after the laboratory session ends is considered late, no exceptions.

It should be stressed that due to high course enrolment, students shall not be admitted to other laboratory sessions than those assigned. Please enter and exit the lab punctually and pay close attention to the time limits your TAs give you for submitting your lab exercises. Failure to have your lab execution checked because the lab time expired may result in a 0 for the lab – TAs are instructed to not accept/review work that is late. Failure to exit the lab punctually may result in being assigned an automatic zero for the entire lab exercise.

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1.0 Objective

To introduce fundamental concepts of digital logic gates and laboratory techniques.

2.0 Pre-Laboratory Preparation [25 marks total]

The prelab is to be prepared as a short report, submitted as a pair (same two students that work together in lab), and uploaded to Avenue not later than 15 minutes after the start of your assigned lab session. For example, if your lab session is scheduled to begin at 2:30pm, then your prelab report is due before 2:45pm on that day. Be prepared to show your TA the completed pre-lab.

Successful completion of each lab will require students to come prepared. To be prepared you should:

a. Review the lab exercise and complete the full pre-lab independently or with your lab partner,
b. Complete a draft skeleton lab report document that will allow you to focus on the lab problem and not the report format (e.g., pre-populate headings, make tables for data entry, make a list of questions to ask the TA, etc.). You should use the lab cover sheet available on Avenue for your draft lab report.

The Prelab Report for Lab 1 should contain answers to the following questions:

1. Find a lab partner for Lab 1. It is recommended to work with the same lab partner for the whole term, but this is not required. In the Prelab report, write the name of your lab Partner for Lab 1. [1 mark]

   Note: Both students are responsible for all content in the lab and the report – this means the TA will ask either student about the lab and if a student cannot answer then they cannot be awarded the grades.

2. Review all the following resources:
   a. What is a breadboard?
   b. How to Use a Breadboard
   c. What is an Integrated Circuit?
   d. Introduction to the Signal Generator and Oscilloscope (you may need to be logged-in to macvideo.ca)

   For each of parts a, b, c, d in #2, write at least one sentence to describe what new information you learned from each resource. If you did not learn anything new, write a sentence to explain where you previously learned this information. [1 mark each, 4 marks total for parts a-d]

3. Complete the ECE lab safety quiz (on Avenue). [0 marks, but must be complete be allowed into Lab 1]

4. From Lab 3 onwards you will be using Quartus software for your hardware description language (HDL) designs. On Avenue you will find a section under Labs called "Quartus Related." In this section you will find a document called **Quartus Installation Instructions.** Do the following:

   a. Download the correct Questa software **to your laptop (the lab computers are already configured)**
   b. Obtain and install Questa License (watch the video, create an account, sign in, sign up for no-cost license, enter your computer info). When registering, use your mcmaster email and your local address.
   c. Download the free license.

In your Prelab report, attest that you have completed #4. [2 marks]
Prior to Lab 3, configure and test the Questa License.

5. For each of the following logic operations define the i) truth table, ii) logic gate symbol for drawing circuit schematics (not the mathematical logic symbol), and iii) integrated circuit name/identification (hint: how do you identify the integrated circuit – find the 2-input data sheet) for the following logic operators [18]:
   (a) AND
   (b) OR
   (c) NAND
   (d) NOR
   (e) XNOR
   (f) XOR

3.0 Integrated Circuits

The following integrated circuits are to be used in this laboratory:

Table 1: Integrated Circuits for Lab 1

Identification	Description
sn74HC00	2-input NAND
sn74HC04	1-input inverter
sn74HC10	3-input NAND
sn74HC86	2-input XOR

Obtain the data sheets for each of the above HIGH-SPEED CMOS devices. Familiarize yourself with their logical and electrical characteristics and bring a copy to your lab session.

4.0 Experiment

Read the following experiment and study the circuits as shown. **Pre-filling your report with the necessary truth tables and structuring your report such that you only need to record experimental output will allow you to focus on the experiment(s).**

ENSURE YOUR MILESTONES ARE VISUALLY CHECKED AND RECORDED BY A TA.

COMPLETED LAB REPORT MUST BE UPLOADED TO AVENUE BY 5:30 pm.
LATE LABS WILL NOT BE ACCEPTED.

4.1 TTL vs HC Levels

For input to a TTL gate, voltages from 0 to 0.8 V are taken to mean a logical LO (or False). Input voltages between 2.0 and 5.0 V (assumes 5.0V supply) are considered logical HI (or True). Voltages between 0.8V and 2.0V are indeterminate and are avoided. These ranges are slightly different for TTL outputs to allow some noise margin. Integrated circuits (ICs) are implemented using specific chip technology and chips designated with "LS" conform to TTL voltages.

For input to a CMOS gate, voltages from 0 to 0.9 are taken to mean a logical LO (or False). Input voltages between 3.15 and 5.0 V (assumes 5.0V supply) are considered logical HI (or True). Voltages between 0.9V

and 3.15V are indeterminate and are avoided. These ranges are slightly different for HIGH-SPEED CMOS outputs to allow some noise margin. Integrated circuits (ICs) are implemented using specific chip technology and chips designated with "HC" conform to CMOS voltages.

A large amount of information exists using TTL logic, but care should be taken to note that TTL/LS and CMOS/HC have different logic levels and should be considered incompatible (see HCT family for TTL compatible CMOS). 2DI4 uses CMOS/HC devices and any reference to LS in the lab manual should be brought to the instructor's attention as this is a typographical error.

Using a function generator, set the output of the function generator to a 100kHz triangular wave (carefully verifying that it is 3.3V peak-to-peak with 1.65V DC offset using the oscilloscope). Apply this triangular waveform from the function generator to the NAND gate input as shown below.

1. Display the function generator's 100kHz triangular wave on channel 1 of the oscilloscope.
2. Display the output of the NAND gate on channel 2 of the oscilloscope.
3. Using the automatic measuring functions of the digital oscilloscope, state at what input voltage level the output of the NAND changes? Specifically, does the automatic measuring function match the HIGH-SPEED CMOS levels for LO and HI?

Milestone 1: TA to check 3. [10 marks]

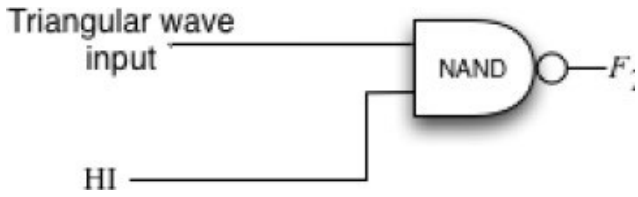

Figure 1: Logic Test Circuit

4.2 Building Circuits, Expressions, and Truth Tables

4. Connect each of the following circuits and experimentally verify each circuit truth table. For inputs use switches and for output connect light emitting diodes (LEDs). For each circuit i) state the logical function, and ii) draw the truth table.

Milestone 2: TA to check 4e. [10 marks]

(a)

Figure 2: Logic Circuit 1

(b)

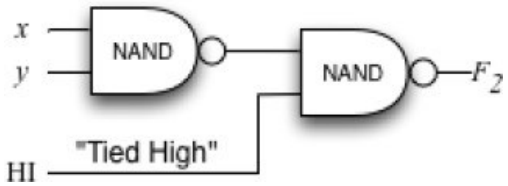

Figure 3: Logic Circuit 2

(c)

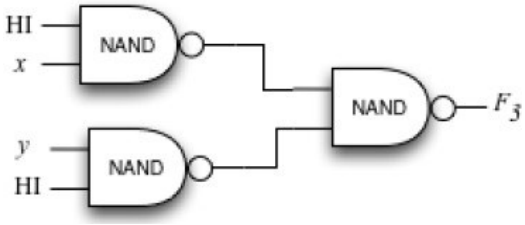

Figure 4: Logic Circuit 3

(d)

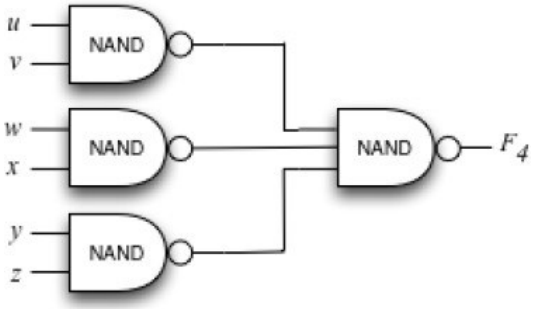

Figure 5: Logic Circuit 4

(e)

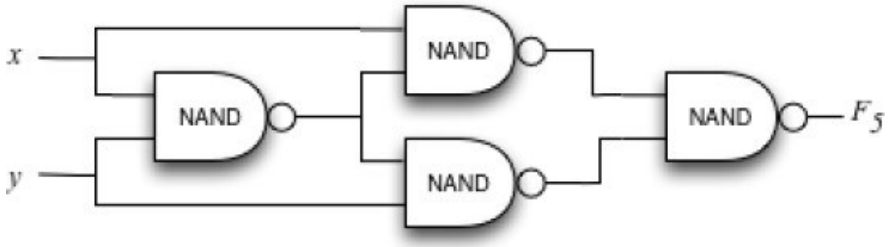

Figure 6: Logic Circuit 5

4.3 Logical Equivalence

5. Build the following circuit and experimentally verify the truth table. Is this logically equivalent to a logical operator that you have seen before? If so, which one?

Milestone 3: TA to check 5 – answer equivalence question. [10 marks]

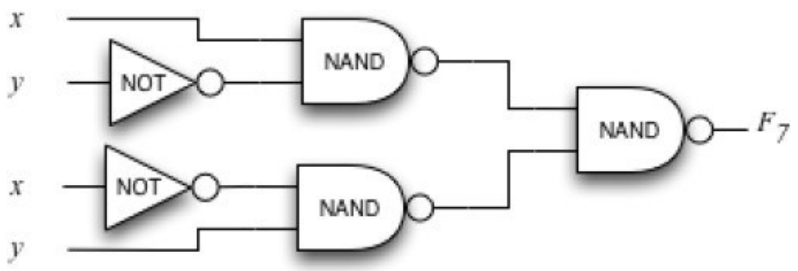

Figure 7: Logic Circuit 6

4.4 Enable/Disable Inverter

6. The output of the 2-input XOR gate is HI when its inputs are different and LO otherwise. Verify the truth table for the XOR gate and explain how it could also be considered to be a "controllable inverter".

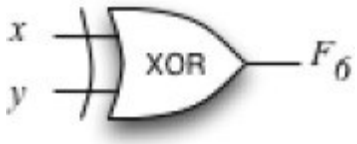

Figure 8: Logic Circuit 7

4.5 Parity Generator

7. Parity bits are commonly used to detect errors in serial communications and memory access. A binary number is said to have odd parity if the number of 1's contained in it is odd; it has even parity when the number of 1's is even. This may be detected using an XOR gate circuit such as the one shown. Build the following circuit to verify that the output F_{Parity} is HI when the parity of the input word wxyz is odd and LO otherwise. Draw the corresponding truth table.

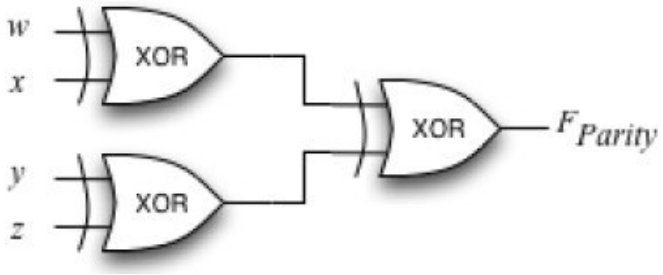

Figure 9: Logic Circuit 8

4.6 Equality Detection

8. The equality of two bits can be indicated with the XNOR (sometimes called a "coincidence gate"). Verify this by examining the truth table of the XNOR. For testing the equality of multi-bit numbers, corresponding bits from each number may be compared using an XNOR gate, and the results of each of these AND'ed together. Build a circuit to implement the following logic and verify that its output $F_{equality}$ is HI only when 3-bit inputs abc and xyz are equal.

   Note: this idea is readily extended to produce a circuit that compares the magnitude of input numbers. For

example the 74HC85 takes two 4-bit inputs A and B, and produces three outputs that indicate A = B, A > B or A < B.

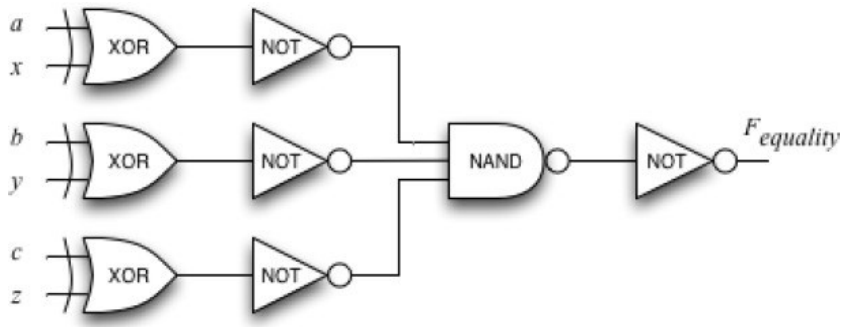

Figure 10: Logic Circuit 9

4.7 Gate Delay

Gate propagation delays can be used to the designer's advantage to generate a short pulse; however, when this is done inadvertently, it is called a "glitch" and can be the source of frustrating problems.

Oscillator

9. Connect a series of 4 inverters plus a NAND gate (as shown below) and display the output $F_{oscillator}$ on the oscilloscope. An odd number of inversions back-to-back will produce an oscillator with a period equal to twice the delay of the inverter chain.

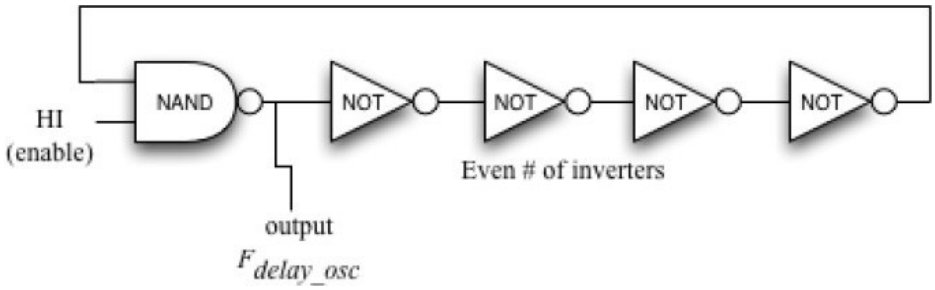

Figure 11: Logic Circuit 10

Milestone 4: TA to check 9b. [15 marks]

(a) Measure and clearly state the time for 1/2 of one cycle of this circuit using the automatic measurement functions of the oscilloscope.
(b) How does this measured time compare to parameters t_{PLH} and t_{PHL} from the sn74HC00 data sheet? State t_{PLH} and t_{PHL}.

5.0 Discussion [10 marks total]

Referring back to the Gate Delay Measurement using the pulse F_{delay} (see Section 4.7), sketch and explain the output you would expect to see if the NAND in the original circuit were replaced with a NOR gate (you are not required to actually modify the circuit).

6.0 Summary of Milestones

The TA must visually verify and record your completion of:
1. 3
2. 4e
3. 5
4. 9b

7.0 Note Regarding Pre-Lab/Lab Format

Please note the following:

1. Milestones must be checked off by TA.
2. Milestone results/observations must be recorded in lab report as proof of work and reference for students. (e.g., photo of oscilloscope waveform, photo of circuit, etc.)
3. Complete lab report must be uploaded to Avenue by 5:30 pm. No late labs will be accepted. Upload what you have by 5:30pm.
4. Students must exit laboratory no later than 5:30pm. No exceptions.
5. All files should be submitted in PDF format.

8.0 Submission Requirements

Please ensure you complete the following items prior leaving the laboratory:

1. At the beginning of each lab you are to have your Pre-Lab checked for completion by a TA.
2. Your lab report has a cover page clearly indicating the lab title, date, each member's name, and student number.
3. Cover page must also contain the following statement: As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is our own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario.
4. Each experiment milestone has been checked by a TA.
5. One member has uploaded the lab report to Avenue (ensuring both have a copy for future reference).

9.0 TA Grading Table

Component	Weight	Grade
Pre-lab	25	
Milestone 1	10	
Milestone 2	10	
Milestone 3	10	
Milestone 4	15	
Discussion	10	
Report	20	
Total	**100**	
Deductions		
Final Score		