Low-Power SRAM Using Hierarchical Bit Line and Local Sense Amplifiers

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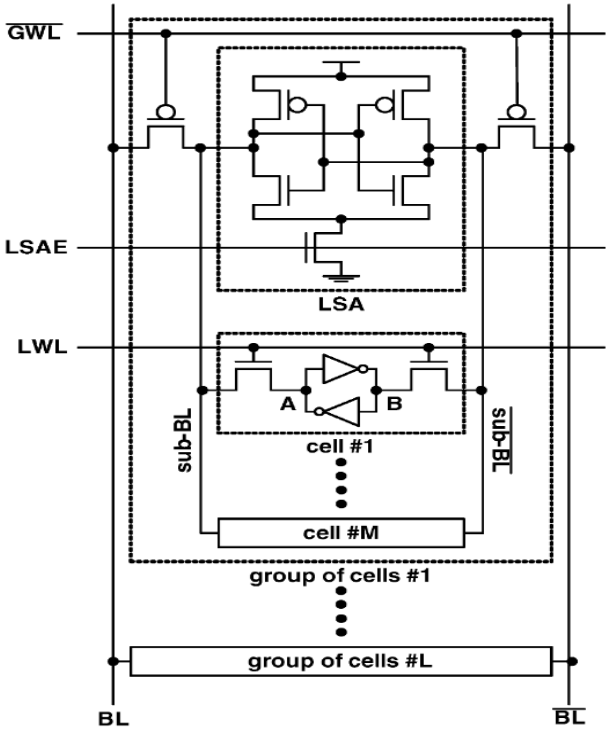
Introduction

Why do we need HBLSA-SRAM?

- Reducing capacitance of bitlines
- Reducing write swing voltage of bit lines
- Reducing the power consumption
- No noise margin degradation
- No extra logic in each local row decoder



Cited from(B.-D. Y. a. L.-S. Kim, "A low-power SRAM using hierarchical bit line and local sense amplifiers)

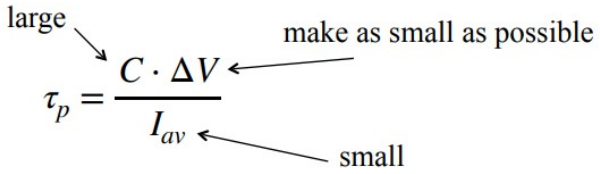
How does HBLSA-SRAM work?

Static Random Access Memory (SRAM):

- Read the signal from voltage change of sub_bitlines (subBL, subBL_bar)

Local Sense Amplifier (LSA):

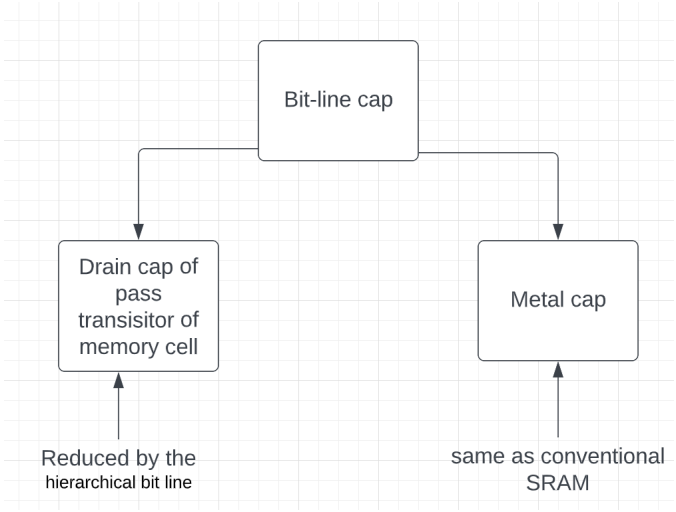
- Precharged Bitline, differential small change of voltage from bitlines
- Amplifier the low swing signal to the full swing signal



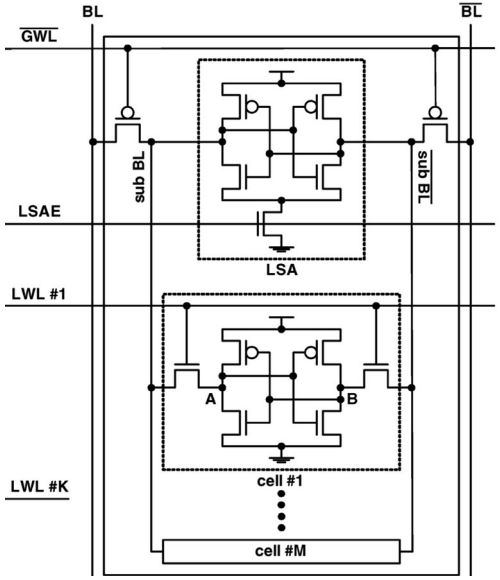
HBLSA-SRAM Structure

ARCHITECTURE:

- BL (Bitlines): Sense amplified signal from LSA
- GWL (Global Write lines): Control “Access” to the bit for LSA
- LWL (Local Write lines): Control “Access” to the bit for SRAM
- Sub BL (sub bitlines): Used for “Write” and “Read”
- LSAE (Local sense amplifier enable)： Enable the LSA



Schematic



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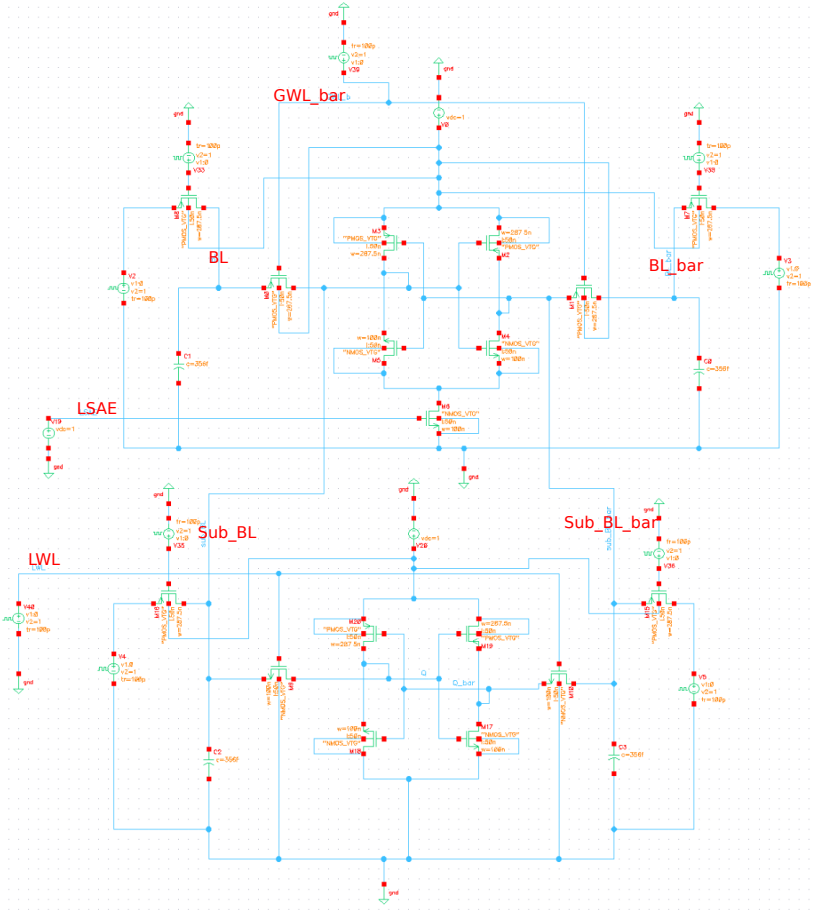
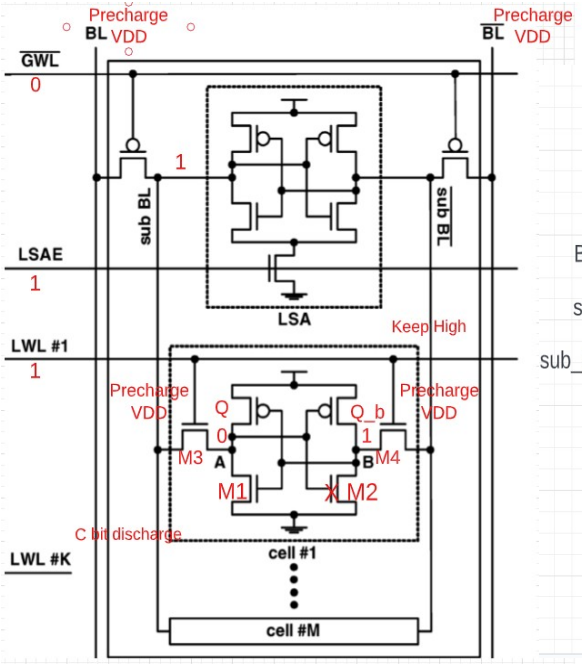


Read simulation

- In read operation, all bit-lines are pre-charged to Vdd and then word-line (WL) is selected to turn on the access transistor.
- After the selected sub-bit line is disconnected from the bit line, the local sense amplifier amplifies the low swing signal to the full swing signal.
- The swing voltage of sub bit line in memory cell is generated by LWL

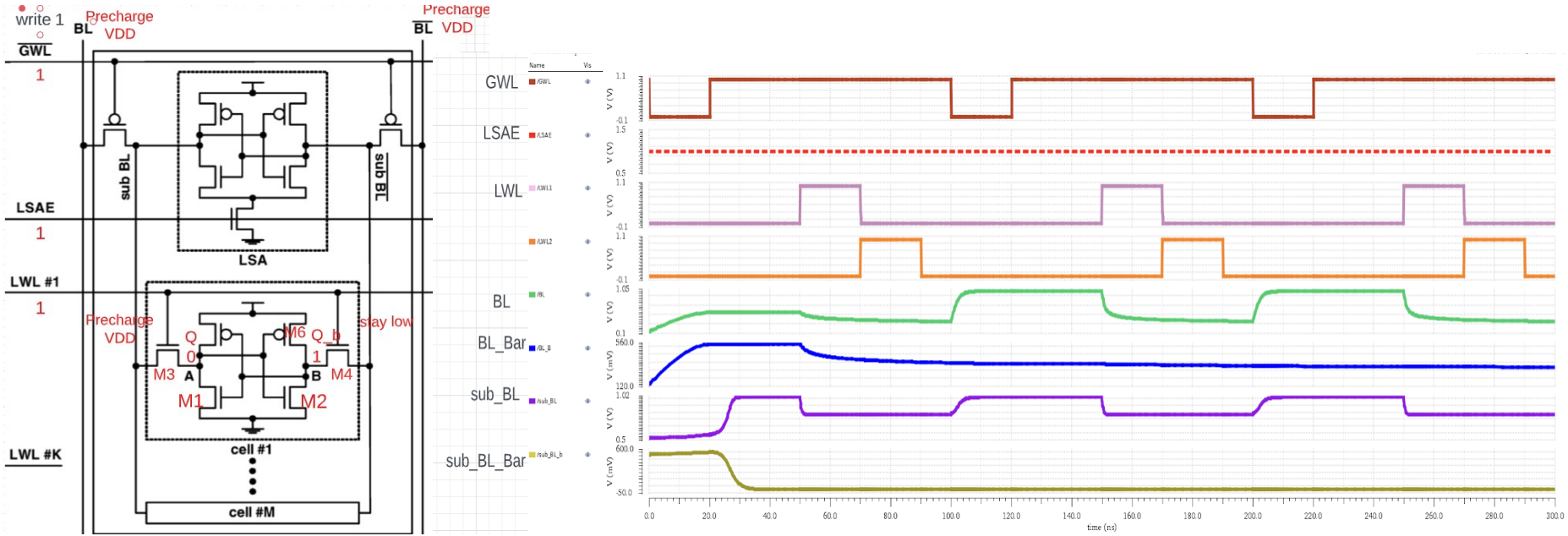
Read simulation



Write simulation

- Same as SRAM cell reading operation, the two bit-lines are pre-charged to VDD in a write operation. The address decoder enables the word line (WL) to turn on the access transistor.
- To write data in memory cells, the full swing signal is used only in the low capacitive sub-bit line whereas the low swing signal is used in the high capacitive bit line.

Write simulation



Simulation Challenge

· Guess the author's intended voltage input

· Trying to match simulation waveform in paper

· Using different technology node and PDK

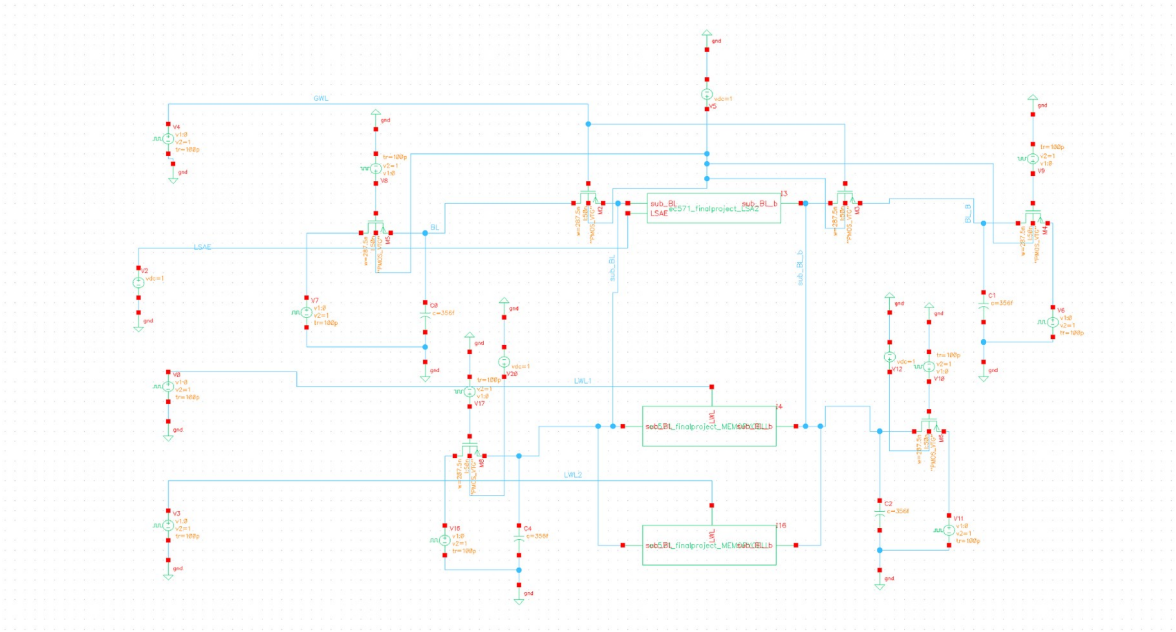
Comparison with CV_SRAM

Power Consumption for 6T SRAM = 4.337 uW

Power Consumption for HBLSA-SRAM = 2.433 uW

Reduction of Power Consumption = (4.337-2.433)/4.337 = 43.9%

HBLSA_SRAM with extra memory



Power Consumption

- Huge reduction in VBL change
- Added SBL only has small V change

$$
\begin{aligned}
P_{\mathrm{BL}} &= f \times C_{\mathrm{BL}} \times \mathrm{V}_{\mathrm{BL}} \times \mathrm{V}_{\mathrm{DD}} \\
P_{\mathrm{SBL}} &= f \times C_{\mathrm{SBL}} \times \mathrm{V}_{\mathrm{DD}}^2 \\
P_{\mathrm{HBL}} &= P_{\mathrm{BL}} + P_{\mathrm{SBL}} \\
&= f \times (C_{\mathrm{BL}} \times V_{\mathrm{BL}} + C_{\mathrm{SBL}} \times V_{\mathrm{DD}}) \times V_{\mathrm{DD}}
\end{aligned}
$$

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Question?