Review of A Low-Power SRAM Using Hierarchical Bit Line and Local Sense Amplifier

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I. Abstract

This paper proposes a low power SRAM using hierarchical bit line and local sense amplifiers (HBLSA-SRAM). It reduces both capacitance and write swing voltage of bit lines by using the hierarchical bit line composed of a bit line and sub-bit lines with local sense amplifiers. The HBLSA-SRAM reduces the swing voltage of bit lines for both read and write. In this article, the schematics and simulation of the HBLSA will be demonstrate. According to the result, this structure saves 44% power consumption compared to the conventional SRAM.

II. Background

The motivation behind low power SRAMs comes from high demands on portable electronic products, with the majority of them being battery powered. Lower power consumption gives more runtime per full charge. Another factor that pushes the demand for the low power SRAMs is the increased use of cache in processors to achieve higher performance.

Similar low power SRAM designs previously came up from others, which all reduce write operation power consumption by limiting voltage swing on the bit lines, all have the drawback of requiring extra logics in each row decoder along with dc-dc voltage converters for pre-charging/discharging the bit lines. These additions happen at the cost of performance drop, error margin degradations, and big chip area increases.

HBLSA-SRAM was then proposed to avoid error margin degradations of those low power SRAM designs. It also came with slight improvement in chip area usage by using one sense amplifier for multiple memory cells instead of per-memory-cell sense amplifier.

Main idea of this circuit is to use a hierarchical bit line and low charge amplifier to save power consumption. When the low swing voltage is applied to the low charge amplifier, the sub-bit line is selected by the global word line that can pass full swing voltage to the memory cell. Compared to other technologies applied for saving power consumption of the SRAM, HBLSA-SRAM does not need extra transistors on the memory cell and extra logic in each row decoder.

The advantage of this structure is the power consumption, the reduction of the bit line capacitance and no noise margin degradation. Such that, instead of charging the BL from 1 V to 2V, BL_bar from 1 V to 0 V. We can charge BL from 1 V to 1.1 V and BL_bar from 1 V to 0.9 V. LSA can differential this small voltage change, and write the signal properly. Also, the bit line cap is composed of drain cap of the pass transistors and the metal cap of the bit lines. The drain cap is significantly reduced by the hierarchical bit line. This would dramatically increase the write speed and reduce the power consumption.

III. Schematics

The HBLSA system is mainly composed with two parts. The local sense amplifier (LSA) and static random-access memory (SRAM). Compared to the conventional SRAM memory cell, the low charge amplifier has been added on the top of schematics, it connects to the memory cell with two sub-bit lines. There is a local sense amplifier enable line used in the bottom of the low charge amplifier. There are

two-word lines in the circuit, global word line and local word line.

In the low charge amplifier, two p-mos pass transistors are used in the connected to the global word line (GWL). In the memory cell, two n-mos pass transistors are used to connect to local word line (LWL).

LSA

Local Sense Amplifier (LSAs) local sense amplifiers (LSAs) are used to save the write power in bit lines. The local sense amplifier amplifies the low swing signals to the full swing signals in the sub-bit lines before the local word line is enabled to write data in the memory cell [1].

6T SRAM

Memory Cell Read the signal from voltage change of Bitlines (BL, BL_bar). The conventional 6T SRAM cell uses two cross coupled inverters and two access transistors as shown in Figure 1. These access transistors connect the cell to the outside world. The inverters are the storage element and reinforce the data bit within the cell as long as the power is supplied (VDD) [2].

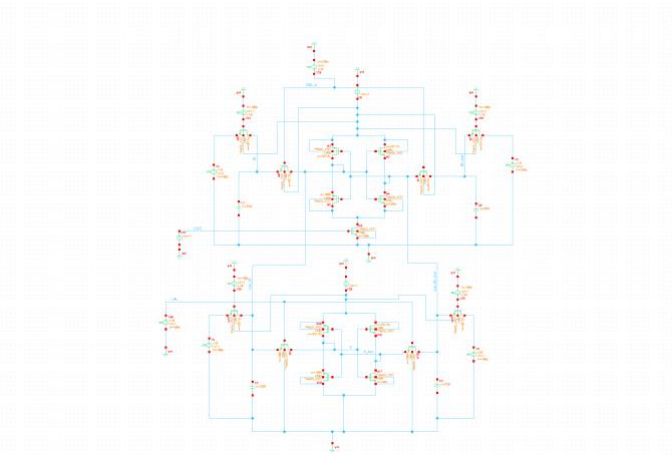

*Figure 3. Circuit Schematics of Memory Cell, Local Sense Amplifier (*HBLSA-SRAM*)*

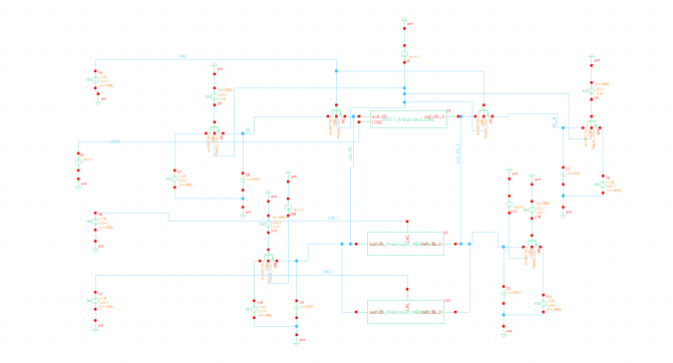

*Figure 4. Circuit Schematics of Memory Cell, Local Sense Amplifier (*HBLSA-SRAM*)*

IV. Simulation

In the simulation, we simulate the read and write process of HBLSA-SRAM. Compared to the conventional SRAM, we need to explore how the hierarchical bit works with global word lines and local word lines from top to bottom in the circuit. The local sense amplifier enable (LSAE) signals are set to Vdd in both operations.

Read

In the reading section, HBLSA-SRAM uses the regular word line to reduce the swing voltage. In this circuit, the bit lines and sub bit line which is connected to the bit line are selected by GWL. Then they are pre charged to Vdd by a bit line pre-charged signal. One side of the bit line and the sub-bit line are lowered to Vdd - VBL. The swing voltage is generated by the pulsed LWL signal. The low swing voltage works on a local sense amplifier. After getting the LSAE (local sense amplifier enable) signal, the low swing voltage will be amplified to full swing signal in the memory cell.

In the read cycle, one PMOS pass transistor which is connected to the GWL and two NMOS pass transistors in the memory cell make bit line discharge.

In the memory cell, we save 0 in Q and 1 in Q_bar. M1 is on and M2 is off [Figure 5]. When LWL is triggered, M3 and M4 are on. There is current from M3 to M1 because M1 is connected to GND. The capacitance on the sub-bit line is discharged. The voltage difference between sub-bit line and sub-bit line bar triggers a local sense amplifier response that leads to low voltage output. The value will be saved in the data buffer. After finishing reading, the sub-bit line will be charged back to Vdd.

From the Figure 6, we keep the GWL at low while LWL is high. Because it is read simulation, we do not need GWL keep high when we read data. One side of sub bit line keep high, it has swing voltage with LWL. The other side of sub bit line is generally discharged to because the capacitance of bit is discharged. In the paper, both side of bit line and sub bit line have same swing voltage. I think maybe we use different voltage, then the leakage current is different.

Write

In the writing section shown in Figure.7, We keep LSAE at Vdd. The bit line and sub-bit line which is connected to the bit line are pre-charged to Vdd when they are selected by GWL. After LWL is triggered, the other side of the bit line and sub-bit line are lower to Vdd - VBL. The VBL is the swing voltage. It is generated by the bit line write driver via pulsed bit line write enable signal. After the global word line is disabled, the sub-bit line is disconnected from the bit line. The local sense amplifier enable (LSAE) signal amplifies the low swing voltage to full swing voltage.

In the write cycle, one PMOS pass transistor which is connected to the GWL and two NMOS pass transistors in the memory cell make bit line discharge. This process is the same as the process in the read cycle.

Local sense amplifier (LSA) writes the data in the memory cell with full swing voltage. From the Figure 5 diagram, we set Q to 0 and Q bar to 1. When we write the value, one side sub-bit line keeps at Vdd, the other side of the sub-bit line will be low voltage. When we want to write '1', the conductivity of M4 needs to be bigger than the conductivity of M6. Then the voltage of M2 is lowered to thread voltage. Finally, M1 is closed because M5 and M3 pull up. The leakage of M2 helps M4 make Q bar to the low voltage. The unit will be flipped.

In the Figure 7, we need to keep GWL at high while the LWL is high. For writing, both lines are used at same time. One side of bit line and sub bit line is triggered by the LWL. One side of bit line and sub bit line keeps low for writing input. The simulation is closed to the paper displays.

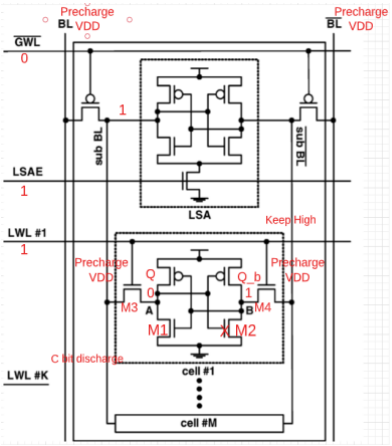

Figure 5. HBLSA Simulation Flowchart

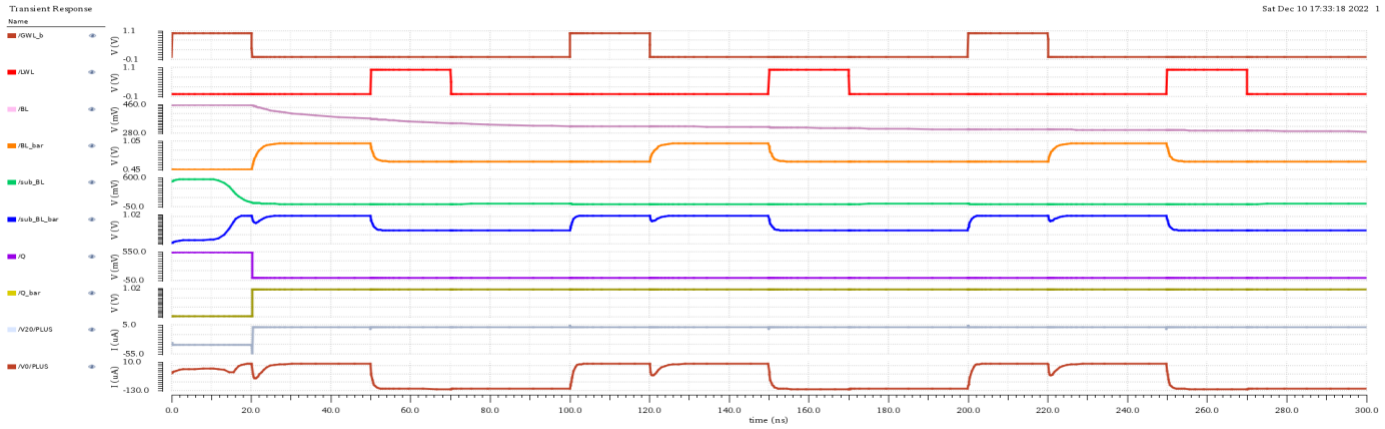

Figure 6. HBLSA Read Simulation

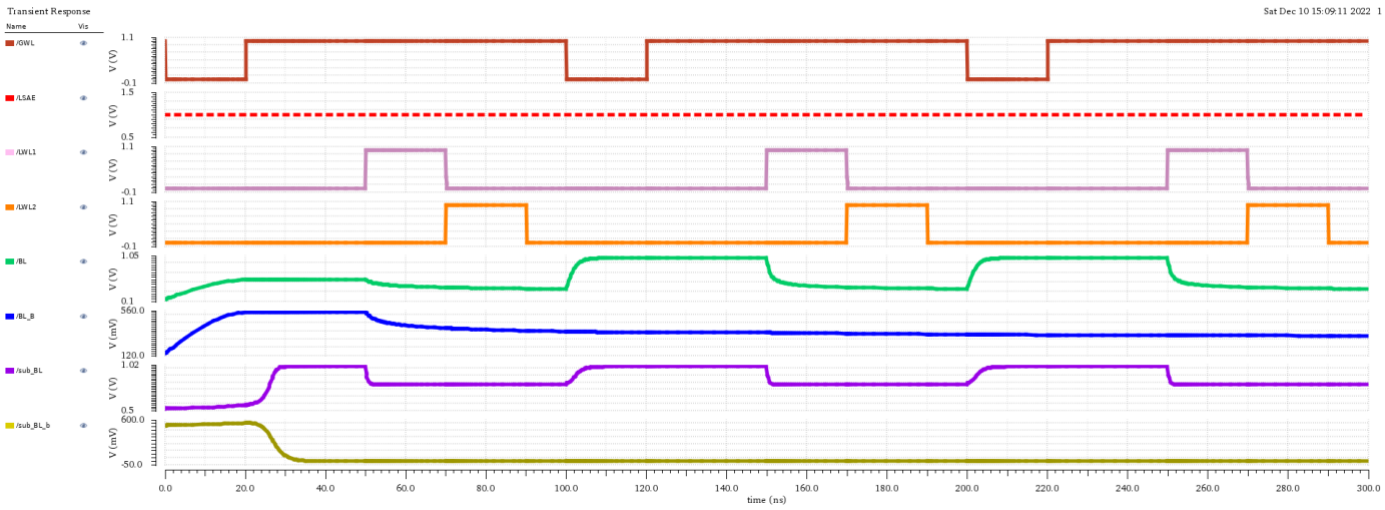

Figure 7. HBLSA Write Simulation

V. Results & Discussion

We see a reduction in the voltage swing on the bit line of around 40%, which suggests that we are going in the right direction. However, the voltage swings on the sub-bit lines are less than a full VDD, which might suggest some problems. The simulation waveform we obtained differs from the waveform on the authors' paper. The reason behind this can be that we are not driving the local sense amplifier and memory units by drivers or decoders, but VPulse sources instead. Another possible reason which might explain the waveform differences is that we might have different PMOS and NMOS sizing from the sizing that the authors of the paper are using. This can lead to different beta values of the cross-coupled inverters, and thus different voltage swings on sub-bit lines and bit lines. The third possible reason which might explain the waveform difference is that we might be using a different technology node and PDK from what the author of the paper is using. Different technology nodes and PDKs might have different PMOS and NMOS strengths, so even if our sizing is the same, the simulation waveforms can be different.

One disadvantage of the HBLSA-SRAM is the need for extra logic to control more than one LWL other

than just the GWL, which also increases the power consumption that is not measured in our result. Another disadvantage is the added complexity, which will make the consideration of MOS speed difference due to process variations more complicated.

VI. Conclusion

To conclude, HBLSA-SRAM reduces power consumption by introducing a sub-bit line and a sense amplifier for multiple memory cells. It is a step forward from Mai's, Mizuno's, and Kanda's design in terms of chip area usage and noise margin.

VII. References

[1] B.-D. Y. a. L.-S. Kim, "A low-power SRAM using hierarchical bit line and local sense amplifiers," *IEEE Journal of Solid-State Circuits,* vol. 40, pp. 1366-1376, June 2005.

[2] A. Bhaskar, "Design and analysis of low power SRAM cells," in *2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*, 2017, pp. 1-5.