Fan Yang

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EDUCATION

Aug 2012 to May 2014 University of Southern California, Los Angeles

- Master of Science, Electrical Engineering
- Main Coursework: MOS VLSI Design, VLSI System Design, Solid State Processing and Integrated Circuits Laboratory, Computer Systems Organization, Computer Systems Architecture, Diagnosis and Design of Reliable Digital Systems, Analysis of Algorithms

Sep 2008 to Jun 2012 Henan University of Technology, China

- Bachelor of Engineering, Electrical Engineering and Automation

SKILLS

Language: Verilog, System Verilog, Perl, Python, C/C++

Tools: Modelsim, Cadence Virtuoso, Cadence NCSim, NCVerilog, Synopsys DC, TetraMax, Xilinx ISE13.2, FPGA, Cadence SOC Encounter, Synopsys PrimeTime, Protel

PROJECT EXPERIENCE

• ASIC Verification using System Verilog (System Verilog) Dec 2013

Verifying simple DUT with constraint random coverage and different assertions (immediate and concurrent). Implement a simple FSM by using more Object Oriented Programming including classes and objects. Extending class has been added to override the original function.

• DDR2 SDRAM Memory Controller Design (Verilog, Cadence Encounter) Oct 2013 to Nov 2013

Implement a 512Mb DDR2 SDRAM controller in Verilog HDL and simulate the design with Denali's DDR2 model using Cadence NC-Verilog. Automatic place and route has been performed by Cadence Encounter after synthesizing. Timing analysis and debugging have also been implemented.

• Diagnosis and test system for Combinational Circuit (C Programming) Nov 2013 to Dec 2013

Design and implement a testing program for the combinational circuit with two ATPG algorithms: D-algorithm and PODEM, two fault simulators: parallel and deductive, and one preprocessor. The program is based on C programming and realizes the functions such as: test vectors creativity and their corresponding outputs as well as fault location.

• Classical General Purpose Microprocessor Design (Virtuoso, Perl) May 2013

Implement a 16bit multi-cycle microprocessor in gate level. Instruction fetch and decode is done by a control signal vector file via Perl-scripting. A 1024-bit 6T SRAM has been designed as main memory. My design uses dynamic logic circuit with domino structure. And releases power*delay*area optimization with clock gating.

• DFT , BIST Realization and Fault Table Generation (NCVerilog, TetraMax) Oct 2013

Synthesizing the RTL to include scan cells. Then use TetraMax ATPG automatically generates high quality manufacturing test patterns for SA-faults. For BIST, the design has two modes: normal and test with LFSR counter.

• Simulation-based Verification using Python Scripting (Python) Oct 2013

Implement a python scripting in order to automate the simulation process, perform result checking and generate a testing report automatically.

• FPGA Prototyping and Code Coverage lab (Verilog, Xilinx) Nov 2013

Debugging the FPGA design with given constraints. Rising the code coverage to 100% with Modelsim. Optimization the design to meet the timing and power constraints. Implement the Viterbi Decoder with Viterbi algorithm, using the FPGA simulator to verify the functionality.

• Single-Clock and Double-Clock FIFO Design(Verilog) Sep 2013

Design and implement a circular single-clock FIFO in 4-value system by using three methods: fill-counter, almost full/almost empty and (n+1) bit pointer. For double-clock FIFO design, double synchronization and gray code have been used to solve the metastability and racing problem. The designs with min clock have been synthesized via Synopsys DC.

• TCAM Design (Verilog) Oct 2013

Design a general-purpose ternary content-addressable memory (TCAM) with 3-value system. A LRU is used to keep the history of each memory location and determines the victim when the memory is full. The design has the min-clock period.

• JTAG (Verilog) Nov 2013

Implement an on-chip JTAG interface to test a design, and familiar with the IEEE testing standard 1149.1(JTAG).