Lab 4:Pipeline CPU

Due: 2018/06/04 11:59pm

1. Goal:

Modifying the CPU designed in CPU lab3 and implementing a simple version pipelined CPU.

2. HW requirement:

a. Please use Modelsim as simulation platform.

b. **Group member same as Lab1**. Just hand in one assignment for one group. Please attach your student IDs as comments in each of .v source code.

c. Pipe_Reg.v, Reg_File.v, Instruction_Memory.v, Data_Memory.v and Pipe_CPU_1.v are supplied.

d. Must use the supplied Reg_File.v

e. In the top module, please change N to the value which is total lengths of input signal (include data and control) of pipeline register.

Pipe_Reg #(.size(N)) ID_EX

(google: verilog + parameter / parameterized modules / 參數式模組)

3. Requirement description:

a. Code (80%):

Instruction set (80%): ADD, ADDI, SUB, AND, OR, SLT, SLTI, LW, SW, BEQ, and MULT.

- Mult rd, rs, rt; // rd=rs*rt

0	Rs	Rt	Rd	0	24

b. Bonus (20%):

Answer the question and describe what you do and why it works in the report.

c. Testbench:

Please use the tested pattern CO_P4_test_1.txt to test basic instruction.

CO_P4_test_1.txt

Begin:

addi $1, $0, 3; // a = 3

```
addi    $2, $0, 4;      // b = 4
addi    $3, $0, 1;      // c = 1
sw      $1, 4($0);      // A[1] = 3
add     $4, $1, $1;     // $4 = 2a
or      $6, $1, $2;     // e = a | b
and     $7, $1, $3;     // f = a & c
sub     $5, $4, $2;     // d = 2a - b
slt     $8, $1, $2;     // g = a < b
beq     $s1, $2, begin
lw      $10, 4($0);     // i = A[1]
```

c. Report (20%):

The context must include:

1. Source code and the note
2. Your architecture
3. Hardware module analysis
4. Problems you met and solutions
5. Division of this work (if you are the two member team)
6. Summary

4. Bonus:

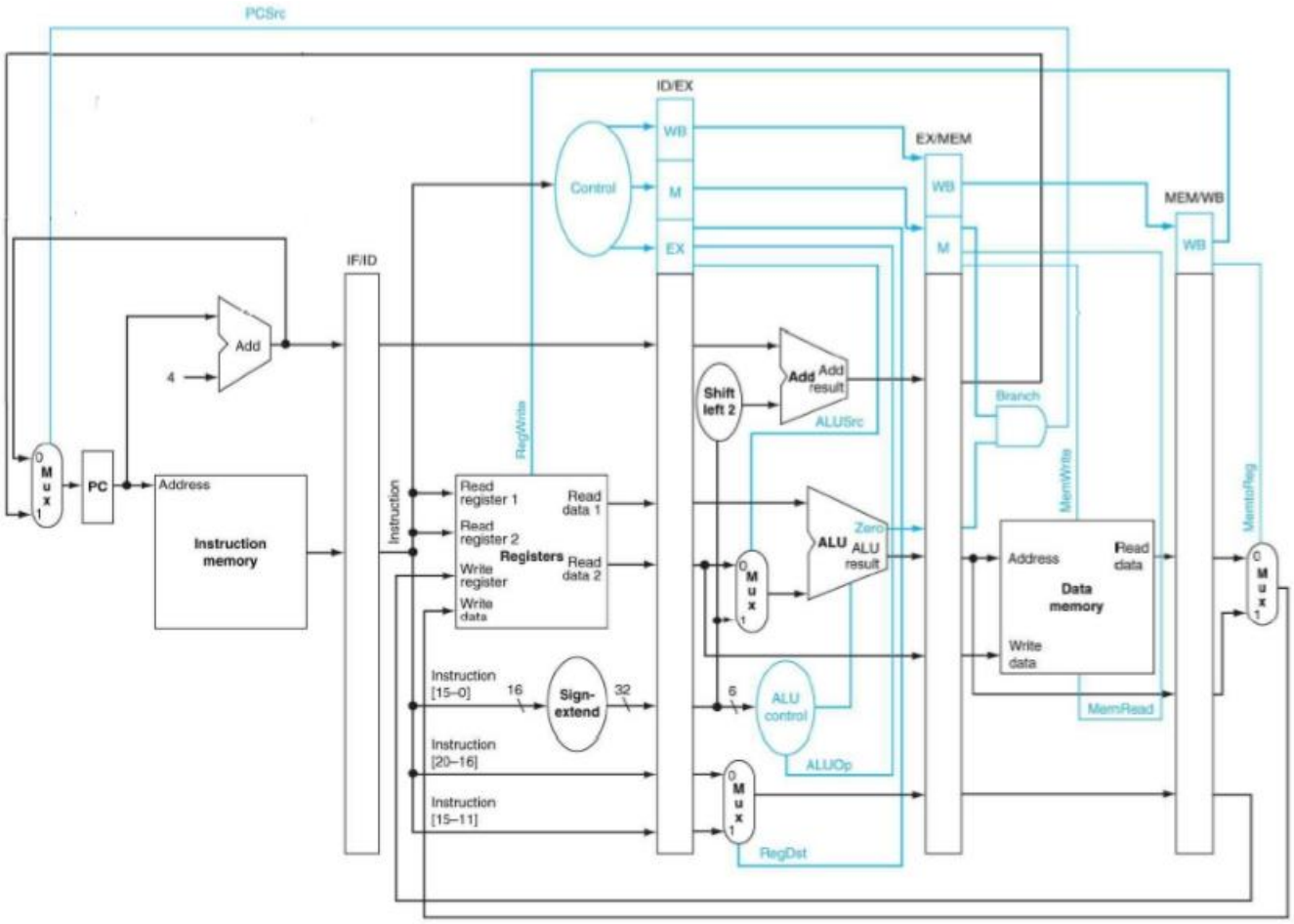
Consider CO_P4_test_2.txt, try to solve the data hazard in I1 / I2, I5 / I6, and I8 / I9 data dependency. Just modify the machine code of the testbench and test on your pipeline CPU. (Write down the machine code in the report.)

CO_P4_test_2.txt

```
I1:  addi   $1, $0, 16
I2:  addi   $2, $1, 4
I3:  addi   $3, $0, 8
I4:  sw     $1, 4($0)
I5:  lw     $4, 4($0)
I6:  sub    $5, $4, $3
I7:  add    $6, $3, $1
I8:  addi   $7, $1, 10
I9:  and    $8, $7, $3
I10: addi   $9, $0, 100
```

Hint: You may (1) insert NOP, (2) reorder instructions, (3) other ideas

5. Architecture:



6. Grade

a. Total score: 120% COPY WILL GET 0!

b. Basic score: 80%

c. Bonus score: 20%

d. Report: 20%

e. Delay: Late submission: Score*0.8 before 6/11. After 6/11,you will get 0 point.

f. Put .v source files and report into a compressed file.The compressed file you upload on E3 must have the form of "student ID.zip " , otherwise deduct 20points.

7. Hand in your Assignment

Please upload the assignment to the E3.

Only hand in one assignment for one group.

Put all of .v source files and report into same compressed file in zip format. (Use your student ID to be the name of your compressed file and must have the form of “student ID.zip”. (Ex. 0216310_0216077.zip or 0216310.zip)

8. Q&A

If you have any question, just send email to TAs.