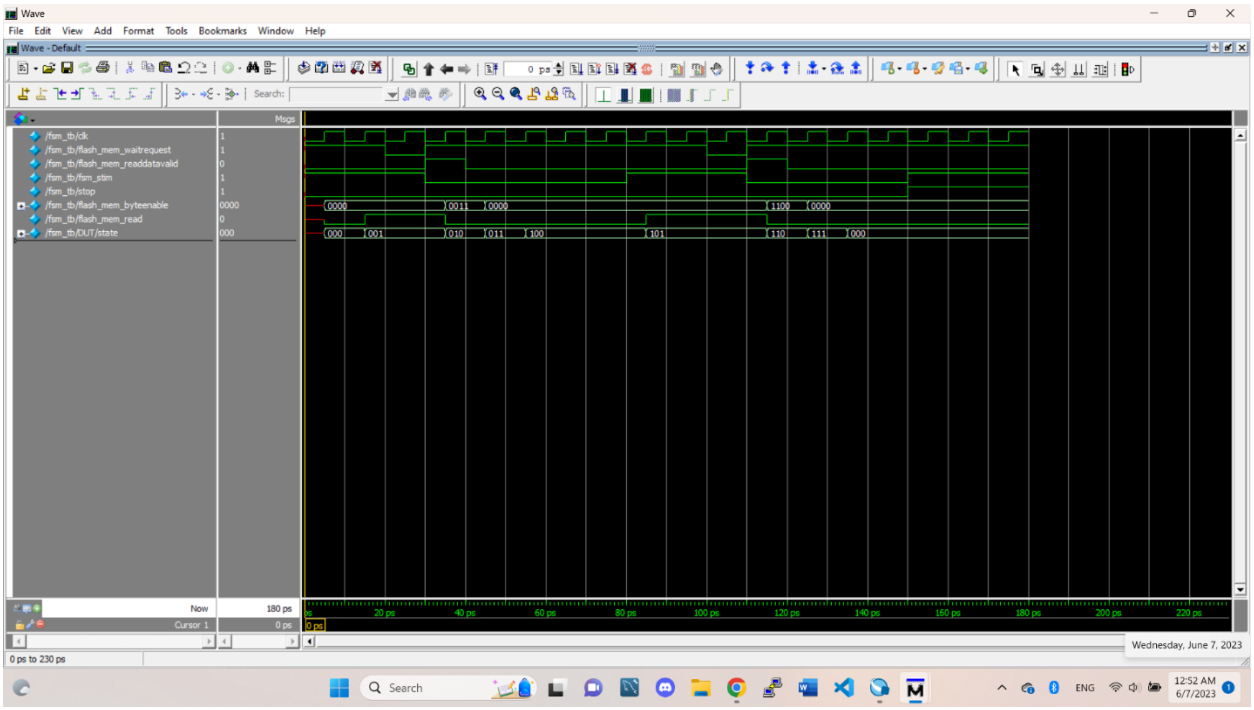
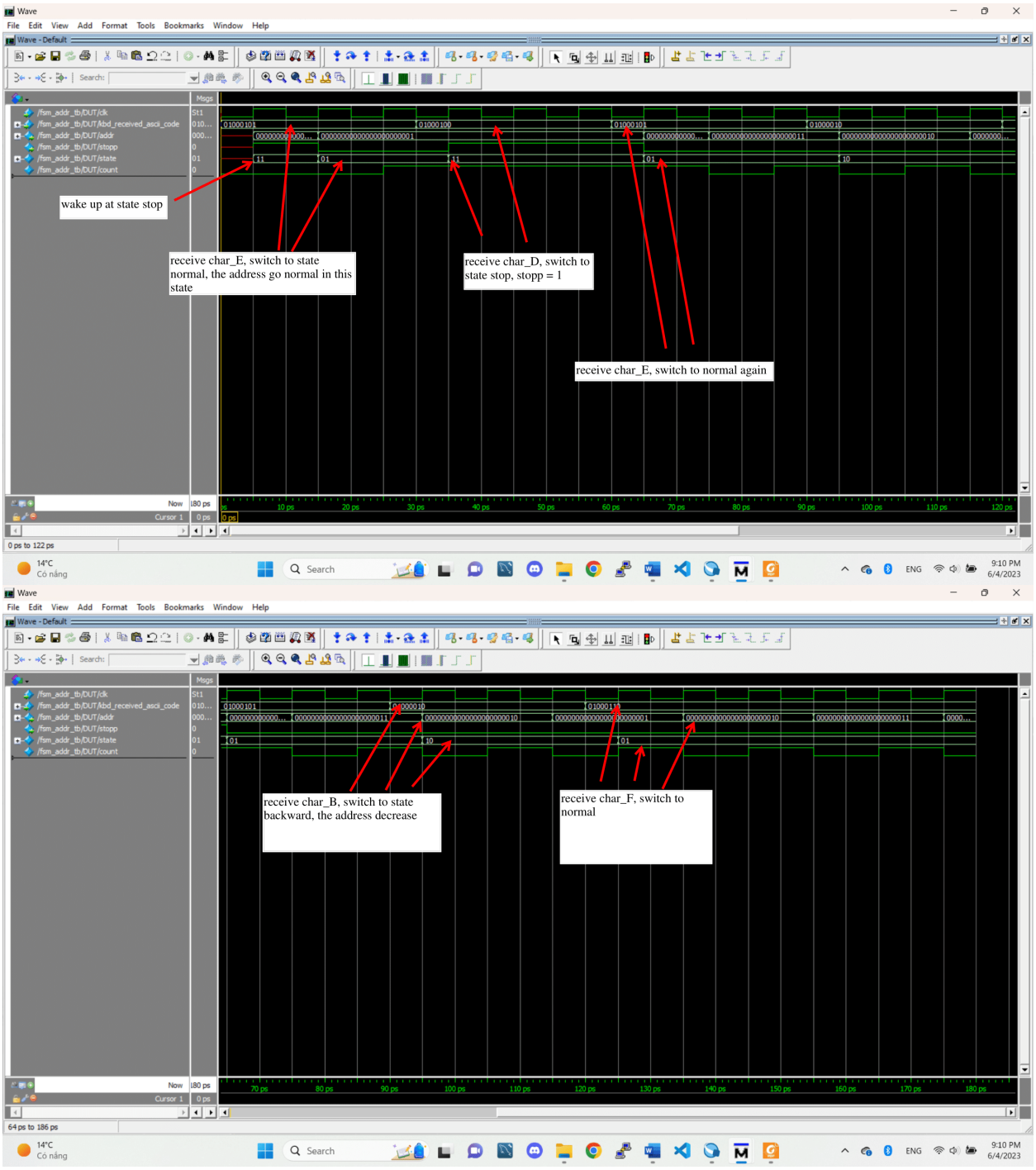
Xuan Tung Luu - 30236798 - README

1. My SOF file is located at xuan_tung_luu_30236798_Lab_2/rtl/simple_ipod_solution.sof
2. Everything works.
3. I have 2 FSM. The first one is to control the signals such as flash_mem_waitrequest, flash_mem_readdatavalid, flash_mem_byteenable, flash_mem_read to interact with the flash. This first module is called fsm. The other FSM controls the address, also sending signal to the first one if the music needs to stop. This second module is called fsm_addr.

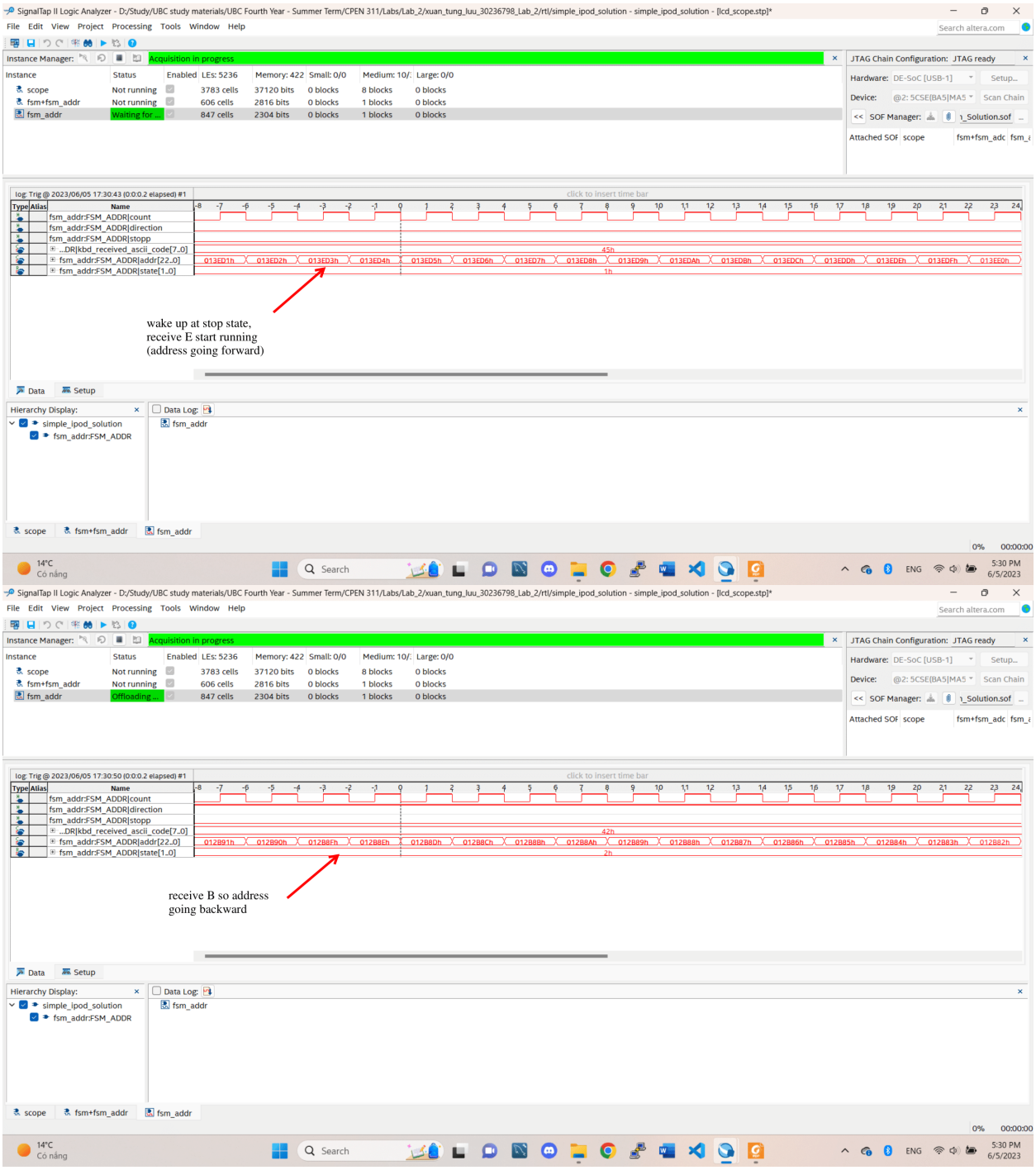


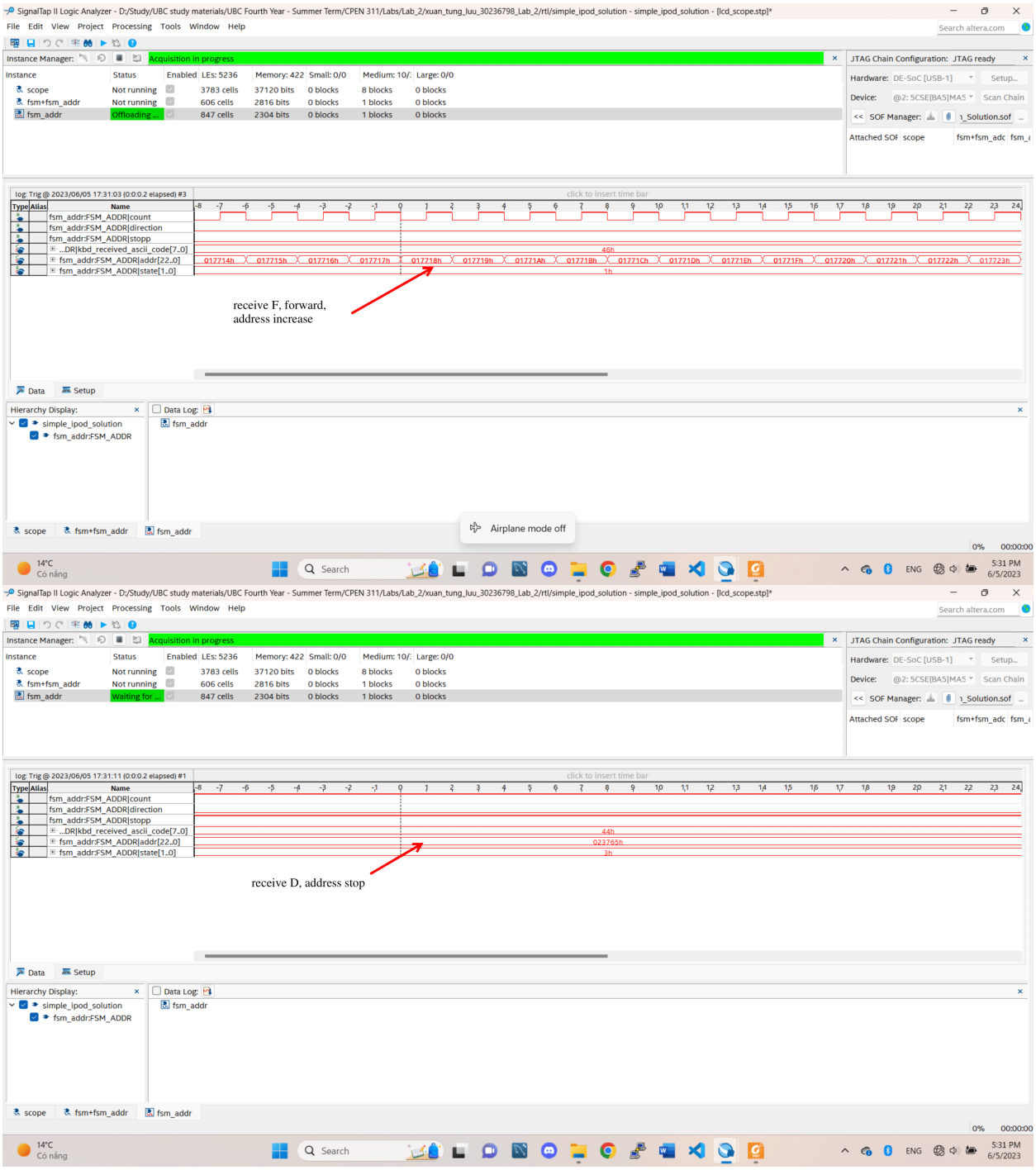
FSM for control signals with FLASH



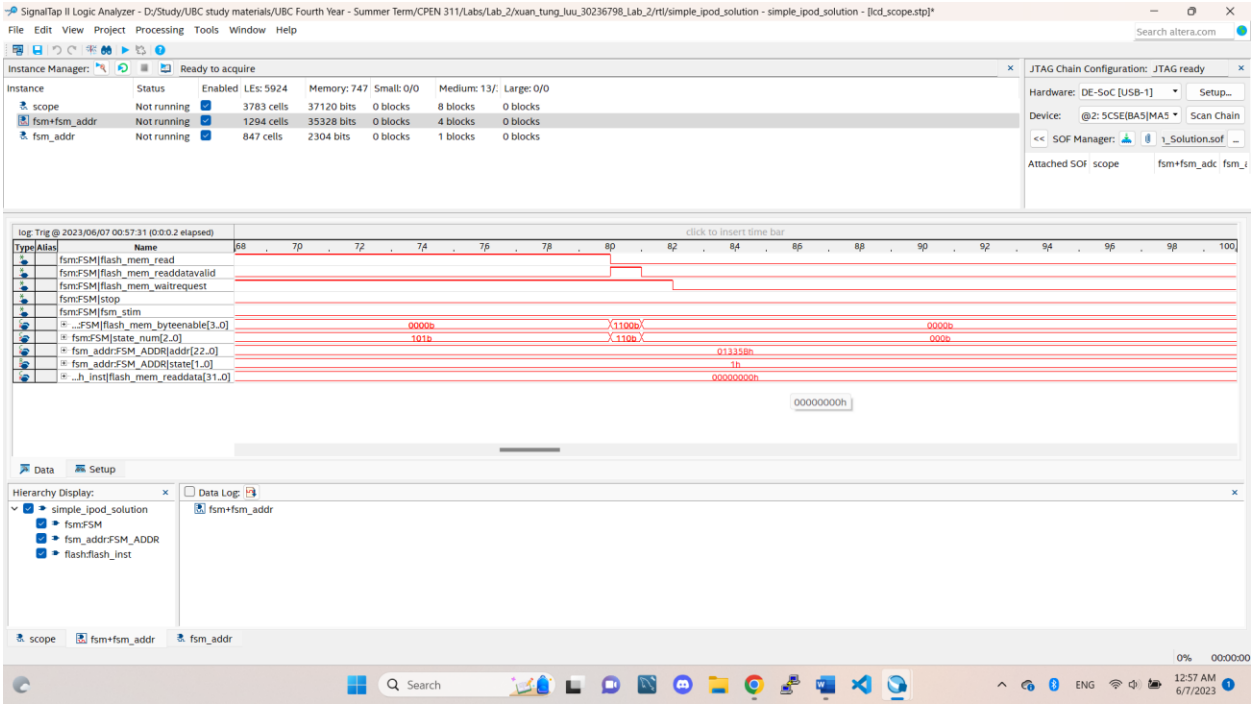
2 pictures of FSM controlling the address

4.Signal tap


SignalTap II Logic Analyzer - D:/Study/UBC study materials/UBC Fourth Year - Summer Term/CPEN 311/Labs/Lab_2/xuan_tung_luu_30236798_Lab_2/rtl/simple_ipod_solution - simple_ipod_solution - [lcd_scope.stp]*
File Edit View Project Processing Tools Window Help
Search altera.com
Instance Manager: Acquisition in progress
Instance Status Enabled LEs: 5236 Memory: 422 Small: 0/0 Medium: 10/. Large: 0/0
scope Not running 3783 cells 37120 bits 0 blocks 8 blocks 0 blocks
fsm+fsm_addr Not running 606 cells 2816 bits 0 blocks 1 blocks 0 blocks
fsm_addr Waiting for ... 847 cells 2304 bits 0 blocks 1 blocks 0 blocks
JTAG Chain Configuration: JTAG ready
Hardware: DE-SoC [USB-1] Setup...
Device: @2: 5CSE(BA5|MA5 Scan Chain
SOF Manager: _Solution.sof
Attached SOF scope fsm+fsm_adc fsm_
log: Trig @ 2023/06/05 17:30:43 (0:0:0.2 elapsed) #1
click to insert time bar
Type Alias Name
fsm_addr:FSM_ADDR|count
fsm_addr:FSM_ADDR|direction
fsm_addr:FSM_ADDR|stopp
..DR|kbd_received_ascii_code[7..0]
fsm_addr:FSM_ADDR|addr[22..0]
fsm_addr:FSM_ADDR|state[1..0]
45h
013ED1h 013ED2h 013ED3h 013ED4h 013ED5h 013ED6h 013ED7h 013ED8h 013ED9h 013EDAh 013EDBh 013EDCh 013EDDh 013EDEh 013EDFh 013EE0h
1h
wake up at stop state,
receive E start running
(address going forward)
Data Setup
Hierarchy Display:
simple_ipod_solution
fsm_addr:FSM_ADDR
Data Log:
fsm_addr
scope fsm+fsm_addr fsm_addr
0% 00:00:00
14°C Có nắng
Search
ENG 5:30 PM 6/5/2023
SignalTap II Logic Analyzer - D:/Study/UBC study materials/UBC Fourth Year - Summer Term/CPEN 311/Labs/Lab_2/xuan_tung_luu_30236798_Lab_2/rtl/simple_ipod_solution - simple_ipod_solution - [lcd_scope.stp]*
File Edit View Project Processing Tools Window Help
Search altera.com
Instance Manager: Acquisition in progress
Instance Status Enabled LEs: 5236 Memory: 422 Small: 0/0 Medium: 10/. Large: 0/0
scope Not running 3783 cells 37120 bits 0 blocks 8 blocks 0 blocks
fsm+fsm_addr Not running 606 cells 2816 bits 0 blocks 1 blocks 0 blocks
fsm_addr Offloading ... 847 cells 2304 bits 0 blocks 1 blocks 0 blocks
JTAG Chain Configuration: JTAG ready
Hardware: DE-SoC [USB-1] Setup...
Device: @2: 5CSE(BA5|MA5 Scan Chain
SOF Manager: _Solution.sof
Attached SOF scope fsm+fsm_adc fsm_
log: Trig @ 2023/06/05 17:30:50 (0:0:0.2 elapsed) #1
click to insert time bar
Type Alias Name
fsm_addr:FSM_ADDR|count
fsm_addr:FSM_ADDR|direction
fsm_addr:FSM_ADDR|stopp
..DR|kbd_received_ascii_code[7..0]
fsm_addr:FSM_ADDR|addr[22..0]
fsm_addr:FSM_ADDR|state[1..0]
42h
012B91h 012B90h 012B8Fh 012B8Eh 012B8Dh 012B8Ch 012B8Bh 012B8Ah 012B89h 012B88h 012B87h 012B86h 012B85h 012B84h 012B83h 012B82h
2h
receive B so address
going backward
Data Setup
Hierarchy Display:
simple_ipod_solution
fsm_addr:FSM_ADDR
Data Log:
fsm_addr
scope fsm+fsm_addr fsm_addr
0% 00:00:00
14°C Có nắng
Search
ENG 5:30 PM 6/5/2023



FSM for controlling address



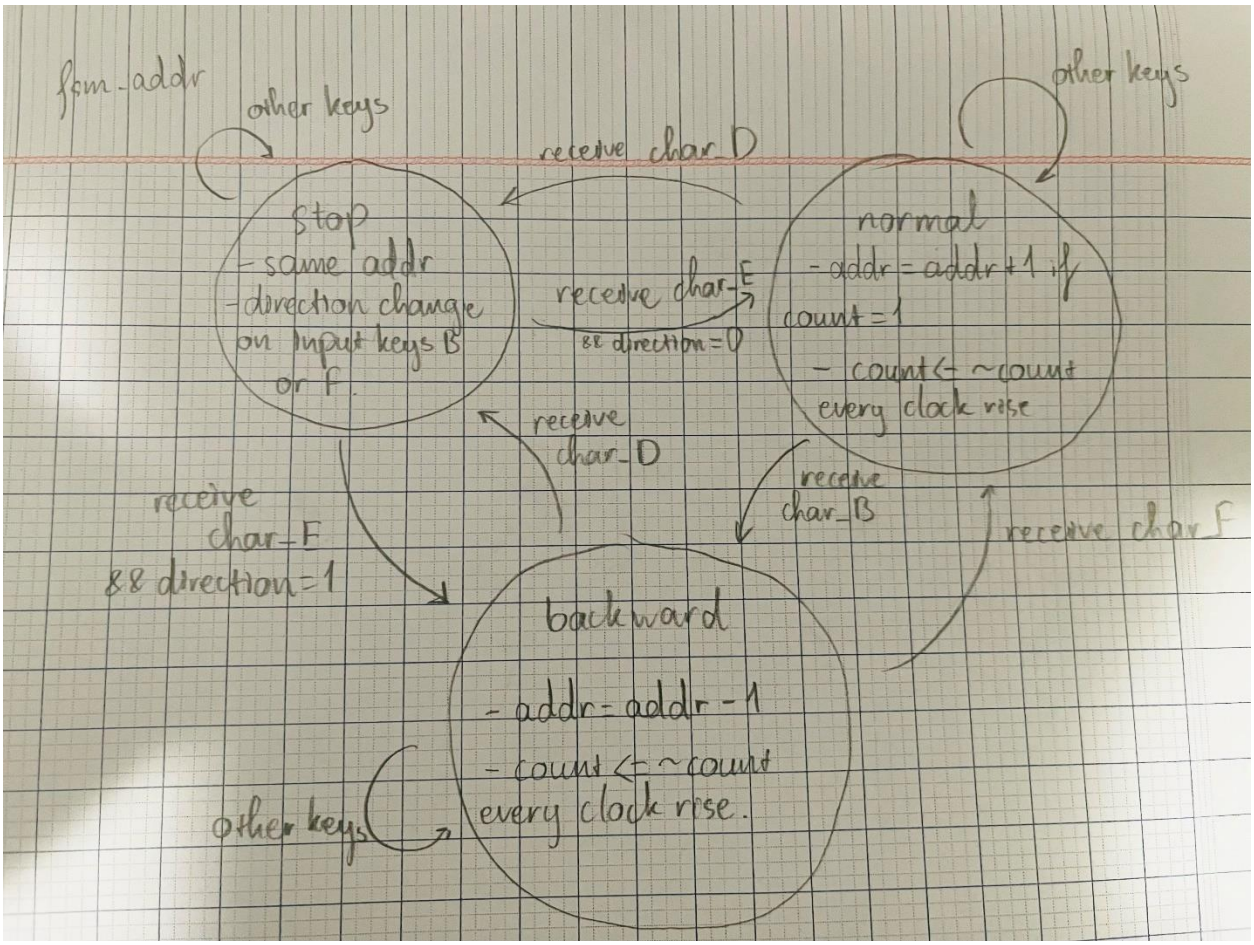
FSM for signals with FLASH

5. I use modelsim to run the simulation. There is a wave.do file in the same folder as the project.

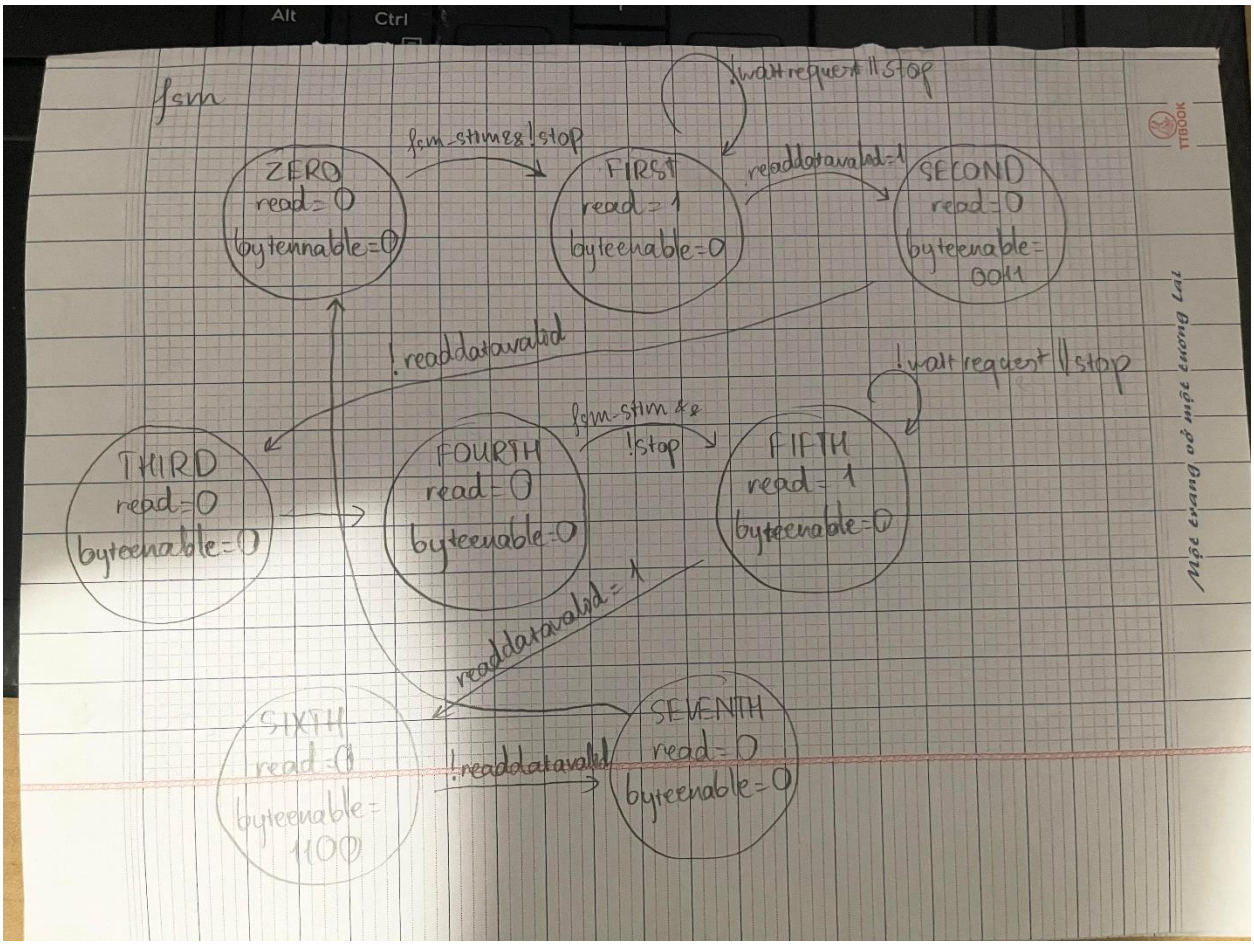
The modelsim project for the first FSM (fsm) is located at:
xuan_tung_luu_30236798_Lab_2/sim/fsm/fsm.mpf

The modelsim project for the second FSM (fsm_addr) is located at:
xuan_tung_luu_30236798_Lab_2/sim/fsm_addr/fsm_addr.mpf

6. State diagram



State diagram for fsm_addr (control address)



State diagram for fsm (for control signals to FLASH)