## DSAR IRAM Package Alpha Release 107\_4\_2

## 1 General

This IRAM package includes the following main features: Custom Classification (CC), Independent-Mode (IM), Host-Commands (HC) and Deep Sleep Auto Response (DSAR). For DSAR the following features are supported: ARP, ICMP, ND and SNMP. For more information see FMan-Controller RM chapter.

## 2 Availability

The package is currently available for the following devices.

Table 1. Package Availability by Device

Device	Version Number	Compiler Version	Loader file name (.h .bin)
T1040 rev 1.0	107_4_2	_	t1040_r1.0.h
T1040 rev 1.1			t1040_r1.1.h
			fsl_fman_ucode_t1040_r1.0 _107_4_2.bin
			fsl_fman_ucode_t1040_r1.1 _107_4_2.bin
T1024 rev 1.0	107_4_2	_	t1024_r1.0.h
			fsl_fman_ucode_t1024_r1.0 _107_4_2.bin



Document Number: DSAR\_107\_4\_2

## **3 Revision History**

Table 2. Revision History for Alpha Release 107.4.2

Release Date: June 24, 2014		
New Features	None.	
New Features (Not in spec)	None.	
Spec Un-Supported Features	The following IP Acceleration features are not supported in this package:  IP fragmentation,  IP reassembly,  Header Manipulation,  Frame Replication.  Please note that CC STD (statistics table descriptor) is supported.	
Bug Fixes/CCB	Following Errata were fixed:  DSAR6 SNMP: Varbind with length field span between 256 bytes blocks cause varbind interpreted incorrectly.  DSAR7 SNMP: SNMP: If the community string is larger than the remaining byte length next to the community string, community mismatch may occur even the string matches.  DSAR8 SNMP: Community mismatch may occur if the community string is located across 256 bytes boundary of the frame.  DSAR9 SNMP: Incorrect interpretation on length field if the length is 2-bytes (i.e. 256~65535) and located across 256 bytes boundary of the SNMP frame.	
Known Issues	None.	
Restrictions	None.	

Table 3. Revision History for Alpha Release 107.4.1

Release Date: May 13, 2014		
New Features	None.	
New Features (Not in spec)	None.	
Table continues on the next page		

Table 3. Revision History for Alpha Release 107.4.1 (continued)

Spec Un-Supported	The following IP Acceleration features are not supported in this package:
Features	IP fragmentation,
	IP reassembly,
	Header Manipulation,
	Frame Replication.
	Please note that CC STD (statistics table descriptor) is supported.
Bug Fixes/CCB	Following Errata were fixed:
	DSAR1:SNMP: Intermittent incorrect UDP checksum on response packet.
	DSAR2:SNMP: The beginning of the frame is corrupted for the NOSUCHNAME response
	DSAR3:SNMP: The UDP checksum of the NOSUCHNAME response is not correct if response frame size exceed 256 bytes.
	DSAR4:SNMP: The Active Mode Hardware Parser NIA is not invoked for the case of set-request message is received.
	DSAR5:VLAN tagged frames are not matched correctly in the IP address tables. Frames with VLAN tags are considered mismatch in the IP/VLAN matching.
Known Issues	None.
Restrictions	None.

Table 4. Revision History for Alpha Release 107.4.0

Release Date: March 30, 2014				
New Features	Deep Sleep Auto-Response: ARP, ICMP, ND and SNMP. Also provide AR Pass filter.			
New Features for B4860/T4240	See above.			
New Features (Not in spec)	None.			
Spec Un-Supported Features	The following IP Acceleration features are not supported in this package:  IP fragmentation,  IP reassembly,  Header Manipulation,  Frame Replication.  Please note that CC STD (statistics table descriptor) is supported.			
Bug Fixes/CCB	None.			
Known Issues	None.			
Table continues on the next page				

Table 4. Revision History for Alpha Release 107.4.0 (continued)

Restrictions
--------------

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFIRE, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorlQ, QorlQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, AMBA, ARM Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and µVision are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. ARM7, ARM9, ARM11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

> DSAR\_107\_4\_2 Rev. 1 10 Feb 2017

