



TCAD

Tutorial and Examples

Volume I

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TCAD
Tutorial and Examples Manual
Volume I

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Intended Audience

The information in this manual is based on the following assumptions:

- The reader is familiar with the basic terminology of semiconductor processing and semiconductor device operation,
and
- The reader understands the basic operations of the computer hardware and operation systems being used.

Introduction

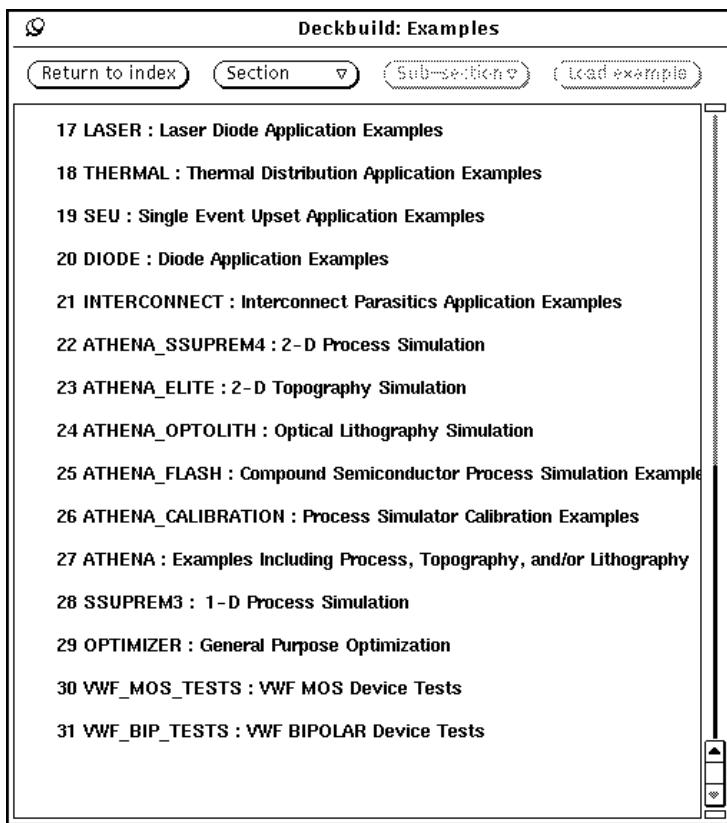
This manual is intended as an additional guide to the use of Silvaco's process and device simulators. It contains descriptions of all the standard examples that demonstrate the use of SSUPREM3, ATHENA, ATLAS, and the VWF INTERACTIVE TOOLS manuals. Users should consult the relevant "User's Manual" for a full description of the models and syntax of each program.

Included on your distribution media are more than five hundred (500) Standard Examples that demonstrate the way that the simulators are used to model many different technologies. The examples are instructional and it is strongly recommended that new users apply these examples as a starting point for creating their own simulations. One of the first things you should learn is how to access, load, and run these examples.

Accessing the Examples

The examples are accessed from the menu system in DECKBUILD. To select and load an example:

1. Start DECKBUILD as described in the VWF INTERACTIVE TOOLS MANUAL.
2. Pull down the **MainControl** menu using the right hand mouse button. There are options on this menu for **MainControl**, **Optimizer**, **Examples**, **Help**, etc.
3. Select **Examples**. An index will appear in a **DeckBuild: Examples** window (see below). The examples are divided by technology or technology group. The most common technologies are clear (e.g., MOS, BJT) while others are grouped with similar devices (e.g., IGBT and LDMOS are under POWER, and solar cell and photodiode are under OPTOELECTRONICS).



The Examples Index in DeckBuild

4. Choose the technology you are interested in by double-clicking the left mouse button over that item in the examples index.
5. A list of examples for that technology will appear. These examples typically illustrate different devices, applications, or types of simulation.
6. Choose a particular example by double-clicking the left mouse button over that item in the list.
7. A text description of the example will appear in the window. This online text is the same as in this manual. It describes the important physical mechanisms in the simulation, as well as giving details of the simulator syntax used. You should read this information before proceeding.
8. Press the **Load Example** button. The **Input Command** file for the example will be copied into your current working directory, together with any associated files. A copy of the command file will be loaded into DECKBUILD. (Note that the **Load Example** button remains faded until Step 6 is performed correctly.)
9. To run the example, press the **Run** button in the middle frame of the DECKBUILD application window.
10. Alternatively, most examples are supplied with results that can be copied into the current working directory, along with the input file. To view the results, select (highlight) the name of the **Results File** and select the DECKBUILD menu option, **Tools-Plot**. Details on the use of TONYPLOT can be found in the VWF INTERACTIVE TOOLS manual.

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1.1. MOS1: MOS Application Examples

1.1.1. mos1ex01.in: NMOS: Id/Vgs and Threshold Voltage Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating an Id/Vgs curve and extracting threshold voltage and other SPICE parameters. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- auto-interface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=0.1V
- parameter extraction for Vt, linear gain (beta) and mobility rolloff (theta)

The process simulation in SSUPREM4 follows a standard LDD MOS process. The process steps are simplified and default models are used to give a fast runtime. The polysilicon gate is formed by a simple geometrical etch. Before this point the simulation is essentially one dimensional and hence is run in ATHENA's 1D mode. After the poly etch, the structure converts to 2D.

The grid used in this example is defined quite tightly. However, the statement, `init...spac.mult=3`, relaxes the mesh in X and Y directions by a factor of three. A more typical mesh for MOS simulation can be obtained by setting `spac.mult=1`.

Using DECKBUILD's auto-interface the process simulation structure will be passed into ATLAS automatically. This auto-interface therefore allows global optimization from process simulation to device simulation to spice model parameter extraction.

The `extract` statement at the end of the file is used to calculate the oxide thickness at that point. The value returned here may be used as an optimization target for calibration. Refer to the INTERACTIVE TOOLS OF THE VIRTUAL WAFER FAB manual for instruction in the use of the OPTIMIZER. This value will be appended to a file in the current working directory called `results.final`. When using the VWF automation tools, `extract` values are logged to the worksheet for RSM modeling. Significant use of `extract` statements is strongly recommended, especially at points where in-line Fab measurements are taken.

Electrodes are defined at the end of the process simulation. Metal is deposited and patterned. Electrode statements are then used to define the metal regions plus the polysilicon as electrodes for use in ATLAS..

In ATLAS the first task is to define the models and material parameters for the simulation. The `contact` statement is used to define the workfunction of the gate electrodes. The `interface` statement defines the fixed charge at the silicon/oxide interface. For simple MOS simulation the parameters `CVT` and `SRH` define the recommended models. `CVT` sets a general purpose mobility model including concentration, temperature, parallel field and transverse field dependence. For more complete MOS simulations of short channel lengths energy balance simulation might be used.

The statement`{begin} solve init` is used to solve the thermal equilibrium case. After this the voltages can be ramped. It is recommended to use small steps at first when ramping voltages. Once two non-zero biases have been obtained the program uses a projection as initial guesses to further bias points. The projection method allows larger voltage steps to be taken. The syntax **method trap** enables ATLAS to cut user-defined voltage steps in half if convergence is not obtained. This is a highly recommended option and is turned on by default.

The unique feature of this example is the IV data simulated and the extraction syntax used. The model, interface and contact statements in ATLAS are also as in the previous example.

The sequence of solve statements is set to ramp the gate bias with the drain voltage at 0.1V. Solutions are obtained at 0.25V intervals up to 3.0V. All terminal characteristics are saved to the file mos1ex02_1.log as specified in the log statement.

The extract statements at the end of the file are used to measure the threshold voltage and other SPICE parameters. The results from the extract statements are printed in the run-time output, saved to a file called results.final and optionally used in the optimizer or VWF AUTOMATION TOOLS. The syntax used in these statements is freely composed of operators such as maximum value (max) and simulation results such as drain current (i.“drain”). The name parameter specifies only a user-defined label. The routines are not hard-coded to these names. Thus the first extraction statement reads:

```
Extract the value called nvt found by taking the x intercept of the
maximum slope to the curve of drain voltage vs. drain current and
subtracting half the drain voltage.
```

This is just one possible definition of threshold voltage. Current search methods are also possible and is described under the DIBL example later in this section. The VWF INTERACTIVE TOOLS manual has details of the extract syntax.

The second extract statement measures the gain (or Beta). This is defined as the value of the steepest slope to the Id/Vgs curve divided by the drain voltage. The final extraction is for the SPICE level 3 mobility roll-off parameter (or Theta). This syntax shows the use of the syntax: \$“nvt” and \$“nbeta”. This tells DECKBUILD to substitute the previously extracted values of threshold and beta into this places in the equation.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

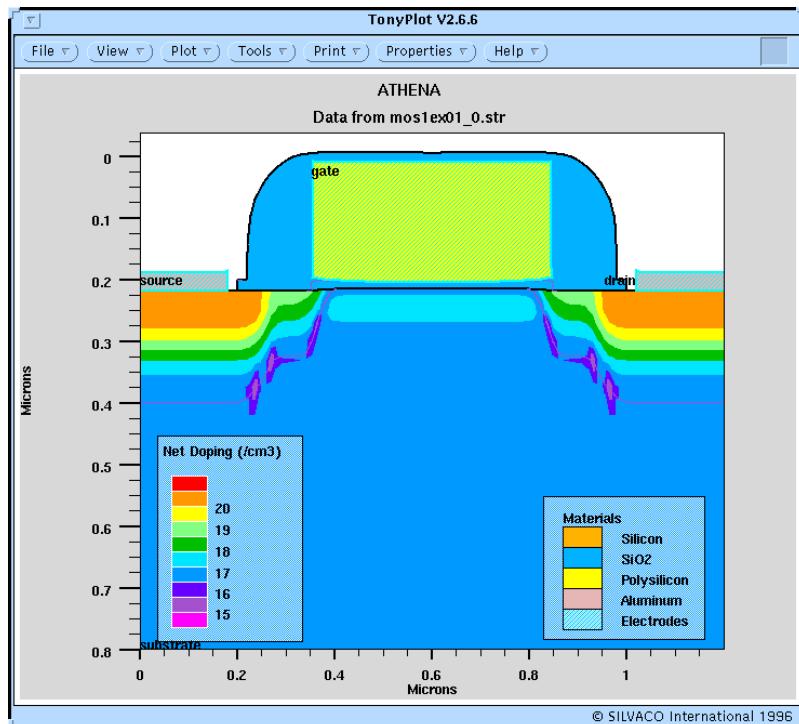


Figure 1.1: Geometry and Doping of 0.6um n-channel MOSFET

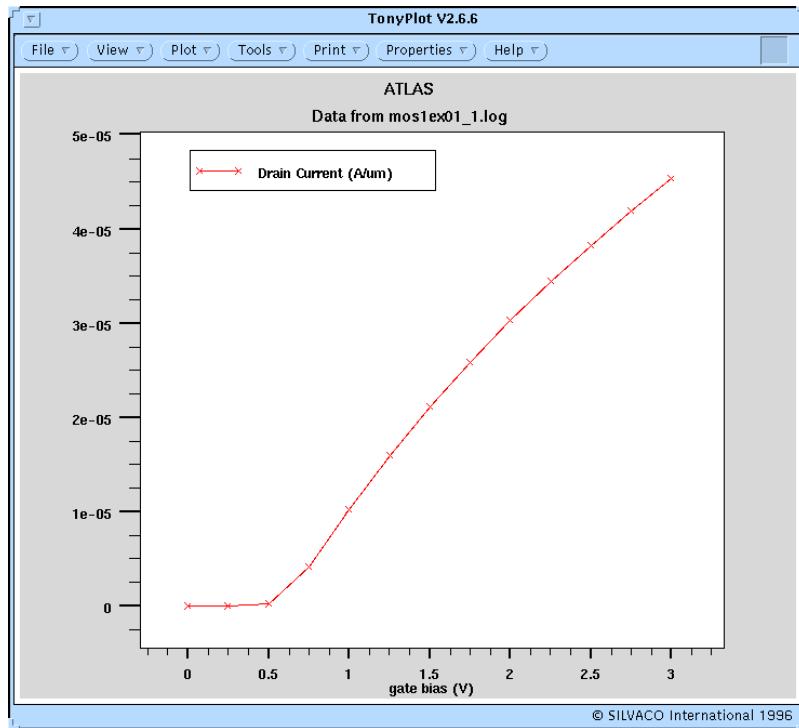


Figure 1.2: NMOS Id/Vgs curve for extracting threshold voltage and linear gain

Input File mos1/mos1ex01.in:

```

1 go athena
2
3 #
4 line x loc=0.0 spac=0.1
5 line x loc=0.2 spac=0.006
6 line x loc=0.4 spac=0.006
7 line x loc=0.6 spac=0.01
8 #
9 line y loc=0.0 spac=0.002
10 line y loc=0.2 spac=0.005
11 line y loc=0.5 spac=0.05
12 line y loc=0.8 spac=0.15
13 #
14 init orientation=100 c.phos=1e14 space.mul=2
15
16 #pwell formation including masking off of the nwell
17 #
18 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
19 #
20 etch oxide thick=0.02
21 #

```

```
22 #P-well Implant
23 #
24 implant boron dose=8e12 energy=100 pears
25
26 #
27 diffus temp=950 time=100 weto2 hcl=3
28 #
29 #N-well implant not shown -
30 #
31 # welldrive starts here
32 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
33 #
34 diffus time=220 temp=1200 nitro press=1
35 #
36 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
37 #
38 etch oxide all
39 #
40 #sacrificial "cleaning" oxide
41 diffus time=20 temp=1000 dryo2 press=1 hcl=3
42 #
43 etch oxide all
44 #
45 #gate oxide grown here:-
46 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
47 #
48 # Extract a design parameter
49 extract name="gateox" thickness oxide mat.occno=1 x.val=0.05
50
51 #
52 #vt adjust implant
53 implant boron dose=9.5e11 energy=10 pearson
54
55 #
56 depo poly thick=0.2 divi=10
57 #
58 #from now on the situation is 2-D
59 #
60 etch poly left p1.x=0.35
61 #
62 method fermi compress
63 diffuse time=3 temp=900 weto2 press=1.0
64 #
```

```
65 implant phosphor dose=3.0e13 energy=20 persion
66 #
67 depo oxide thick=0.120 divisions=8
68 #
69 etch oxide dry thick=0.120
70 #
71 implant arsenic dose=5.0e15 energy=50 persion
72 #
73 method fermi compress
74 diffuse time=1 temp=900 nitro press=1.0
75 #
76
77 # pattern s/d contact metal
78 etch oxide left p1.x=0.2
79 deposit alumin thick=0.03 divi=2
80 etch alumin right p1.x=0.18
81
82 # Extract design parameters
83
84 # extract final S/D Xj
85 extract name="nxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
86
87 # extract the N++ regions sheet resistance
88 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1
     x.val=0.05 region.occno=1
89
90 # extract the sheet rho under the spacer, of the LDD region
91 extract name="ldd sheet rho" sheet.res material="Silicon" \
92 mat.occno=1 x.val=0.3 region.occno=1
93
94 # extract the surface conc under the channel.
95 extract name="chan surf conc" surf.conc impurity="Net Doping" \
96 material="Silicon" mat.occno=1 x.val=0.45
97
98 # extract a curve of conductance versus bias.
99 extract start material="Polysilicon" mat.occno=1 \
100 bias=0.0 bias.step=0.2 bias.stop=2 x.val=0.45
101 extract done name="sheet cond v bias" \
102 curve(bias,ldn.conduct material="Silicon" mat.occno=1 region.occno=1) \
103 outfile="extract.dat"
104
105 # extract the long chan Vt
106 extract name="nlodvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
```

```
107
108
109 structure mirror right
110
111 electrode name=gate x=0.5 y=0.1
112 electrode name=source x=0.1
113 electrode name=drain x=1.1
114 electrode name=substrate backside
115
116 structure outfile=moslex01_0.str
117
118 # plot the structure
119 tonyplot moslex01_0.str -set moslex01_0.set
120
121 ##### Vt Test : Returns Vt, Beta and Theta #####
122 go atlas
123
124 # set material models
125 models cvt srh print
126
127 contact name=gate n.poly
128 interface qf=3e10
129
130 method gummel newton
131 solve init
132
133 # Bias the drain
134 solve vdrain=0.1
135
136 # Ramp the gate
137 log outf=moslex01_1.log master
138 solve vgate=0 vstep=0.25 vfinal=3.0 name=gate
139 save outf=moslex01_1.str
140
141 # plot results
142 tonyplot moslex01_1.log -set moslex01_1_log.set
143
144 # extract device parameters
145 extract name="nvt" (xintercept(maxs-
    lope(curve(abs(v."gate"),abs(i."drain")))) \ 
146 - abs(ave(v."drain"))/2.0)
147 extract name="nbeta" slope(maxs-
    lope(curve(abs(v."gate"),abs(i."drain")))) \
148 * (1.0/abs(ave(v."drain")))
```

```

149 extract name="ntheta" ((max(abs(v."drain")) * $nbeta")/
    max(abs(i."drain"))) \
150 - (1.0 / (max(abs(v."gate")) - ($"nvt")))
151
152 quit
153

```

1.1.2. mos1ex02.in: NMOS: Family of Id/Vds Curves

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example demonstrating the simulation of a family of Id/Vds curves. The maximum drive current and saturation slope are extracted. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- Id/Vds curve generation with Vgs=1.1, 2.2 and 3.3V
- IV Curve parameter extraction for Idmax and saturation slope

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

A more advanced sequence of solve statements is used for this example. Three Id/Vds curves are required at different gate voltages. The first part of the solve sequence sets up the initial point of the three curves. For each of the three gate voltages a solution with Vds=0.0 is simulated and the results saved to a solution file.

Then each of these three solution files are loaded in turn into ATLAS. A log file is opened and the ramp of Vds is set. When a file is loaded, the voltages in ATLAS are reset to the values in the file.

At the end of the simulation, extract is used to measure the peak current and the saturation slope. From the shape of the Id/Vds curves, the saturation slope is clearly the minimum value of the gradient along the curve. Finally, the three Id/Vds curves are overlaid in TonyPlot.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

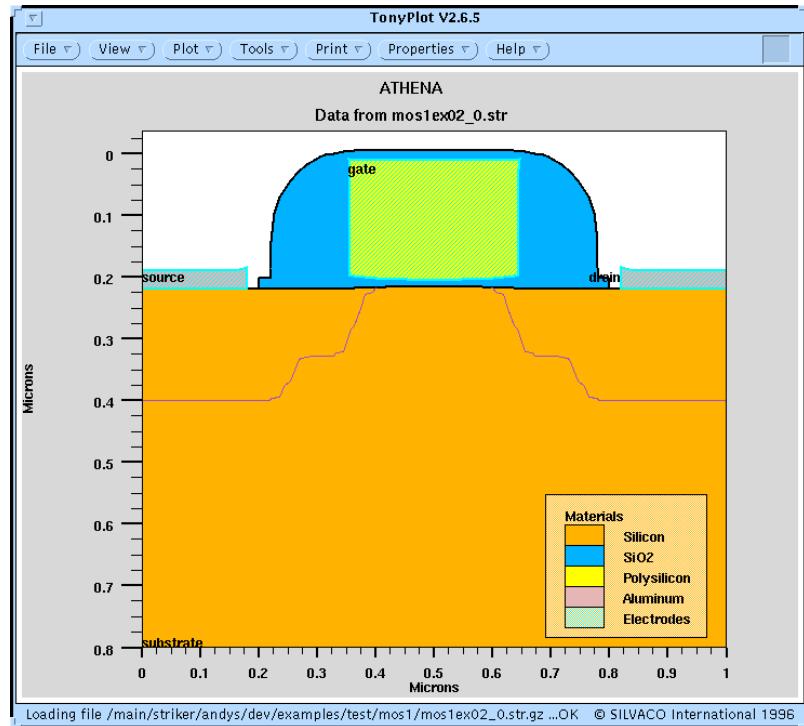


Figure 1.3: Junctions and materials in NMOSFET simulated in ATHENA

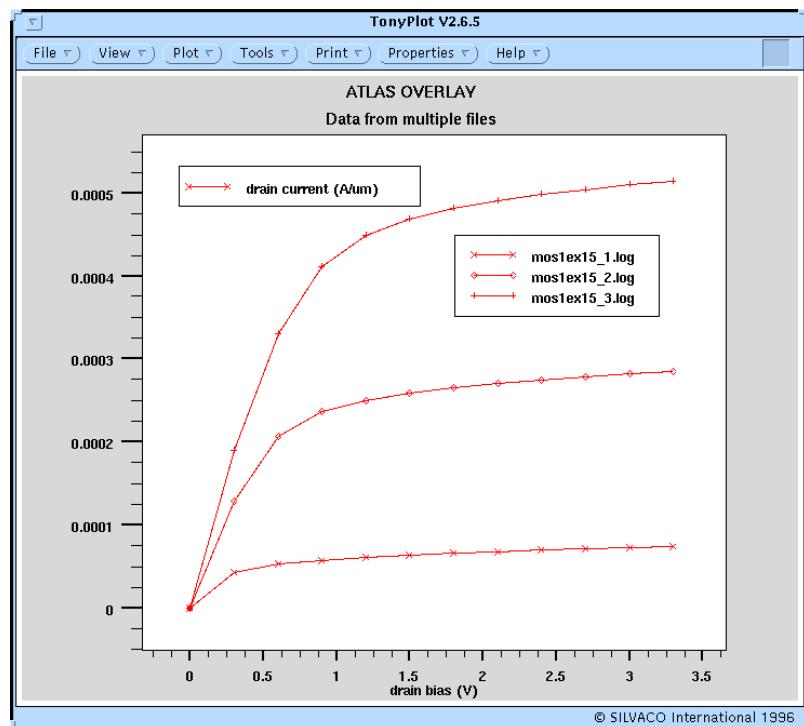


Figure 1.4: Family of ID/VDS curves from an n-channel MOSFET

Input File mos1/mos1ex02.in:

1 go athena

```
2  #
3  line x loc=0 spac=0.1
4  line x loc=0.2 spac=0.006
5  line x loc=0.4 spac=0.006
6  line x loc=0.5 spac=0.01
7  #
8  line y loc=0.00 spac=0.002
9  line y loc=0.2 spac=0.005
10 line y loc=0.5 spac=0.05
11 line y loc=0.8 spac=0.15
12 #
13 init orientation=100 c.phos=1e14 space.mul=3
14 #
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=8e12 energy=100 pears
24 #
25 #
26 diffus temp=950 time=100 weto2 hcl=3
27 #
28 #N-well implant not shown -
29 #
30 # welldrive starts here
31 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
32 #
33 diffus time=220 temp=1200 nitro press=1
34 #
35 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
36 #
37 etch oxide all
38 #
39 #sacrificial "cleaning" oxide
40 diffus time=20 temp=1000 dryo2 press=1 hcl=3
41 #
42 etch oxide all
43 #
44 #gate oxide grown here:-
```

```
45 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
46 #
47 #
48
49
50 #
51 #vt adjust implant
52 implant boron dose=9.5e11 energy=10 pearson
53
54 #
55 depo poly thick=0.2 divi=10
56 #
57 #from now on the situation is 2-D
58 #
59 etch poly left p1.x=0.35
60 #
61 method fermi compress
62 diffuse time=3 temp=900 weto2 press=1.0
63 #
64 implant phosphor dose=3.0e13 energy=20 pearson
65 #
66 depo oxide thick=0.120 divisions=8
67 #
68 etch oxide dry thick=0.120
69 #
70 implant arsenic dose=5.0e15 energy=50 pearson
71 #
72 method fermi compress
73 diffuse time=1 temp=900 nitro press=1.0
74 #
75
76 #
77 etch oxide left p1.x=0.2
78 deposit alumin thick=0.03 divi=2
79 etch alumin right p1.x=0.18
80
81
82 # Extract a design parameter.....
83 extract name="gateox" thickness oxide mat.occno=1 x.val=0.49
84 # Extract another design parameters...
85 # extract final S/D Xj...
86 extract name="nxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
87 # extract the long chan Vt...
```

```
88 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
89 # extract a curve of conductance versus bias....
90 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
91 extract done name="sheet cond v bias" curve(bias,ldn.conduct materi-
    al="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
92 # extract the N++ regions sheet resistance...
93 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.05 region.occno=1
94 # extract the sheet rho under the spacer, of the LDD region...
95 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.3 region.occno=1
96 # extract the surface conc under the channel....
97 extract name="chan surf conc" surf.conc impurity="Net Doping" materi-
    al="Silicon" mat.occno=1 x.val=0.45
98
99 structure mirror right
100
101 electrode name=gate x=0.5 y=0.1
102 electrode name=source x=0.1
103 electrode name=drain x=0.9
104 electrode name=substrate backside
105
106 structure outfile=moslex02_0.str
107
108 # plot the structure
109 tonyplot -st moslex02_0.str -set moslex02_0.set
110
111
112 go atlas2
113
114 # define the Gate workfunction
115 contact name=gate n.poly
116
117 # Define the Gate Qss
118 interface qf=3e10
119
120 # Use the cvt mobility model for MOS
121 models cvt srh
122
123 # set gate biases with Vds=0.0
124 solve init
125 solve vgate=1.1 outf=solve_tmp1
126 solve vgate=2.2 outf=solve_tmp2
```

```
127 solve vgate=3.3 outf=solve_tmp3
128
129 #load in temporary files and ramp Vds
130 load infile=solve_tmp1
131 log outf=moslex02_1.log
132 solve name=drain vdrain=0 vfinal=3.3 vstep=0.3
133
134 load infile=solve_tmp2
135 log outf=moslex02_2.log
136 solve name=drain vdrain=0 vfinal=3.3 vstep=0.3
137
138 load infile=solve_tmp3
139 log outf=moslex02_3.log
140 solve name=drain vdrain=0 vfinal=3.3 vstep=0.3
141
142 # extract max current and saturation slope
143 extract name="nidsmax" max(i."drain")
144 extract name="sat_slope" slope(minslope(curve(v."drain",i."drain")))
145
146 tonyplot -overlay -st moslex02_1.log moslex02_2.log moslex02_3.log -set
    moslex02_1.set
147
148 quit
149
150
```

1.1.3. moslex03.in: NMOS: Sub-Threshold Slope Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating an Id/Vgs curve and extracting sub-threshold slope. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=0.1
- parameter extraction for Sub-Threshold Slope

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

In ATLAS the same sequence of statements is used as in the first example in this section. The only difference is that the gate voltage is ramped from zero to 1.0V only in 0.1V steps.

The EXTRACT statement used in this example measures the sub-threshold slope of the MOSFET. The syntax uses the operators log10(), slope() and curve() to specify the reciprocal of the steepest slope

to the curve of V_{gs} vs. $\log(I_d)$. Note that the operator $\log10()$ is needed here. The operator $\log()$ specifies the function for natural logarithm.

To load and run this example, select **Load example button** while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

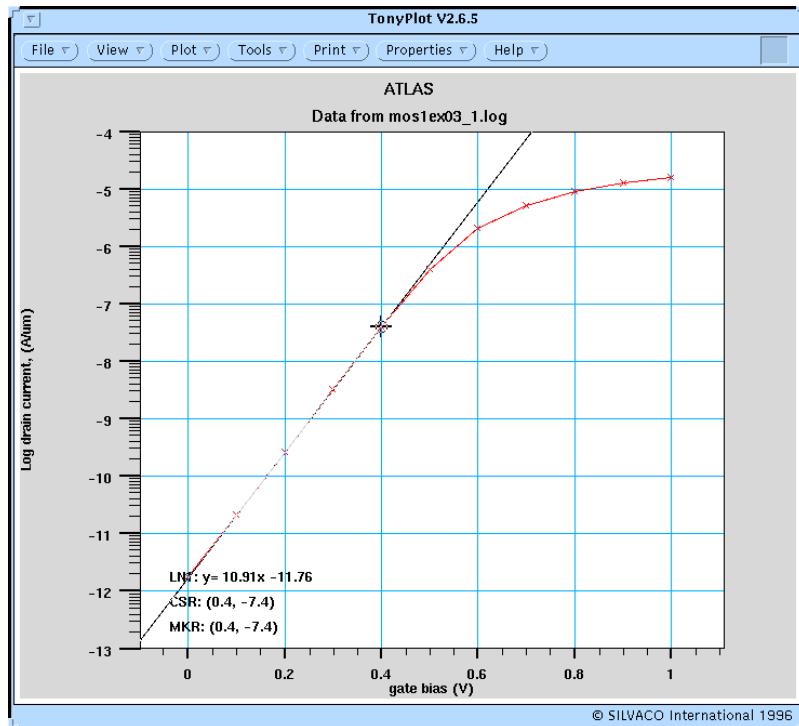


Figure 1.5: Sub-threshold swing extraction from a $\log(I_d)$ vs V_{gs} plot. The 4145 emulator feature of TonyPlot is used to get the slope

Input File mos1/mos1ex03.in :

```

1  go athena
2  #
3  line x loc=0 spac=0.1
4  line x loc=0.2 spac=0.006
5  line x loc=0.4 spac=0.006
6  line x loc=0.5 spac=0.01
7  #
8  line y loc=0.00 spac=0.002
9  line y loc=0.2 spac=0.005
10 line y loc=0.5 spac=0.05
11 line y loc=0.8 spac=0.15
12 #
13 init orientation=100 c.phos=1e14 space.mul=3
14
15 #pwell formation including masking off of the nwell
16 #

```

```
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=8e12 energy=100 pears
24 #
25 #
26 diffus temp=950 time=100 weto2 hcl=3
27 #
28 #N-well implant not shown -
29 #
30 # welldrive starts here
31 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
32 #
33 diffus time=220 temp=1200 nitro press=1
34 #
35 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
36 #
37 etch oxide all
38 #
39 #sacrificial "cleaning" oxide
40 diffus time=20 temp=1000 dryo2 press=1 hcl=3
41 #
42 etch oxide all
43 #
44 #gate oxide grown here:-
45 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
46 #
47 #
48
49
50 #
51 #vt adjust implant
52 implant boron dose=9.5e11 energy=10 pearson
53
54 #
55 depo poly thick=0.2 divi=10
56 #
57 #from now on the situation is 2-D
58 #
59 etch poly left p1.x=0.35
```

```
60 #
61 method fermi compress
62 diffuse time=3 temp=900 weto2 press=1.0
63 #
64 implant phosphor dose=3.0e13 energy=20 pearson
65 #
66 depo oxide thick=0.120 divisions=8
67 #
68 etch oxide dry thick=0.120
69 #
70 implant arsenic dose=5.0e15 energy=50 pearson
71 #
72 method fermi compress
73 diffuse time=1 temp=900 nitro press=1.0
74 #
75
76 #
77 etch oxide left p1.x=0.2
78 deposit alumin thick=0.03 divi=2
79 etch alumin right p1.x=0.18
80
81
82 # Extract a design parameter.....
83 extract name="gateox" thickness oxide mat.occno=1 x.val=0.49
84 # Extract another design parameters...
85 # extract final S/D Xj...
86 extract name="nxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
87 # extract the long chan Vt...
88 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
89 # extract a curve of conductance versus bias....
90 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
91 extract done name="sheet cond v bias" curve(bias,ldn.conduct material="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
92 # extract the N++ regions sheet resistance...
93 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1 x.val=0.05 region.occno=1
94 # extract the sheet rho under the spacer, of the LDD region...
95 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occno=1 x.val=0.3 region.occno=1
96 # extract the surface conc under the channel....
97 extract name="chan surf conc" surf.conc impurity="Net Doping" material="Silicon" mat.occno=1 x.val=0.45
98
```

```
99 structure mirror right
100
101 electrode name=gate x=0.5 y=0.1
102 electrode name=source x=0.1
103 electrode name=drain x=0.9
104 electrode name=substrate backside
105
106 structure outfile=moslex03_0.str
107
108 # plot the structure
109 tonyplot moslex03_0.str -set moslex03_0.set
110
111
112
113 ##### SubVt Test : Returns NSubVt Parameter #####
114 go atlas
115
116
117 # set material models
118 models cvt srh print
119 contact name=gate n.poly
120 interface qf=3e10
121
122
123 # get initial solution
124
125 solve init
126
127 method newton trap
128 solve prev
129
130
131 # Bias the drain a bit...
132 solve vdrain=0.025 vstep=0.025 vfinal=0.1 name=drain
133 # Ramp the gate to a volt...
134 log outf=moslex03_1.log master
135 solve vgate=0 vstep=0.1 vfinal=1.0 name=gate
136
137
138 # extract the device parameter SubVt...
139 extract init inf="moslex03_1.log"
140 extract name="nsubvt" 1.0/slope(maxs-
    lope(curve(abs(v."gate"),log10(abs(i."drain")))))
```

```
141 tonyplot mos1ex03_1.log -set mos1ex03_1_log.set
142
143 quit
```

1.1.4. mos1ex04.in: NMOS: DIBL Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating two Id/Vgs curves at different drain biases and extracting the drain-induced barrier lowering (DIBL) parameter. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=0.1V
- ramp of drain voltage
- simple Id/Vgs curve generation with Vds=3.0V
- parameter extraction for the DIBL parameter

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

In ATLAS the models, interface and contact statements are also the same as the first example. The extraction of the first Id/Vgs curve is very similar to the previous threshold voltage extraction example.

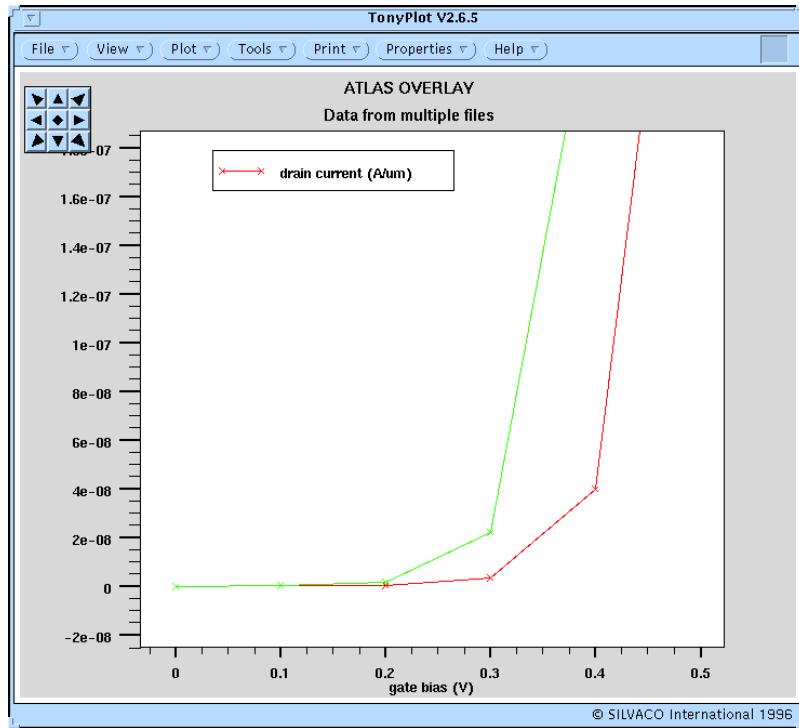
One difference is the use of the syntax, `compl=1.1e-7 cname=drain`. This sets a compliance limit on the drain current. Although the `Solve` statement calls for a ramp in gate voltage from zero to 1.5V, once the trigger current specified by `compl` is exceeded on the electrode specified by `cname` then the gate voltage ramp will step and ATLAS will execute the next line of syntax. Compliances are more commonly used in breakdown simulations but can be used in this way to stop voltage ramps once the area of interest is passed.

All results from the first Id/Vgs curve are saved to the file specified by the first log statement. In ATLAS the only way to stop the IV points being saved is either to specify another LOG statement or exit the simulator. That is why the statement `log outf=dummy.log` is needed. This stops the output from the drain voltage ramp being saved to the Id/Vgs logfile.

The second `solve init` statement resets all applied voltages to zero. Then the drain is ramped to 3.0V and the gate ramp with compliance is repeated.

After each gate ramp, the threshold voltage was extracted using a different syntax than the NMOS threshold voltage example described earlier in this section. In this example the threshold is determined by looking for the voltage where the drain current reaches a user-defined value. The syntax, `x.val from curve (x,y) where y.val=<number>` is used. At large drain biases this method is preferred for threshold extraction over the steepest slope approach. The search value of 0.1uA/um of current is typical for channel lengths around 1um. These thresholds are stored as values `nvt1` and `nvt2` in DECKBUILD. The final `extract` statement is used to obtain the DIBL parameter. It is the difference in threshold voltage divided by the difference in the drain bias.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

Figure 1.6: Drain voltage dependence of V_t for a NMOSFET**Input File mos1/mos1ex04.in :**

```

1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.2 spac=0.006
5 line x loc=0.4 spac=0.006
6 line x loc=0.5 spac=0.01
7 #
8 line y loc=0.00 spac=0.002
9 line y loc=0.2 spac=0.005
10 line y loc=0.5 spac=0.05
11 line y loc=0.8 spac=0.15
12 #
13 init orientation=100 c.phos=1e14 space.mul=3
14
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant

```

```
22 #
23 implant boron dose=8e12 energy=100 pears
24 #
25 #
26 diffus temp=950 time=100 weto2 hcl=3
27 #
28 #N-well implant not shown -
29 #
30 # welldrive starts here
31 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
32 #
33 diffus time=220 temp=1200 nitro press=1
34 #
35 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
36 #
37 etch oxide all
38 #
39 #sacrificial "cleaning" oxide
40 diffus time=20 temp=1000 dryo2 press=1 hcl=3
41 #
42 etch oxide all
43 #
44 #gate oxide grown here:-
45 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
46 #
47 #
48
49
50 #
51 #vt adjust implant
52 implant boron dose=9.5e11 energy=10 pearson
53
54 #
55 depo poly thick=0.2 divi=10
56 #
57 #from now on the situation is 2-D
58 #
59 etch poly left p1.x=0.35
60 #
61 method fermi compress
62 diffuse time=3 temp=900 weto2 press=1.0
63 #
64 implant phosphor dose=3.0e13 energy=20 pearson
```

```
65 #
66 depo oxide thick=0.120 divisions=8
67 #
68 etch oxide dry thick=0.120
69 #
70 implant arsenic dose=5.0e15 energy=50 pearson
71 #
72 method fermi compress
73 diffuse time=1 temp=900 nitro press=1.0
74 #
75
76 #
77 etch oxide left p1.x=0.2
78 deposit alumin thick=0.03 divi=2
79 etch alumin right p1.x=0.18
80
81
82 # Extract a design parameter.....
83 extract name="gateox" thickness oxide mat.occcno=1 x.val=0.49
84 # Extract another design parameters...
85 # extract final S/D Xj...
86 extract name="nxj" xj silicon mat.occcno=1 x.val=0.1 junc.occcno=1
87 # extract the long chan Vt...
88 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
89 # extract a curve of conductance versus bias....
90 extract start material="Polysilicon" mat.occcno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
91 extract done name="sheet cond v bias" curve(bias,ldn.conduct materi-
    al="Silicon" mat.occcno=1 region.occcno=1) outfile="extract.dat"
92 # extract the N++ regions sheet resistance...
93 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.05 region.occcno=1
94 # extract the sheet rho under the spacer, of the LDD region...
95 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.3 region.occcno=1
96 # extract the surface conc under the channel....
97 extract name="chan surf conc" surf.conc impurity="Net Doping" materi-
    al="Silicon" mat.occcno=1 x.val=0.45
98
99 structure mirror right
100
101 electrode name=gate x=0.5 y=0.1
102 electrode name=source x=0.1
103 electrode name=drain x=0.9
```

```
104 electrode name=substrate backside
105
106 structure outfile=moslex04_0.str
107
108 # plot the structure
109 tonyplot moslex04_0.str -set moslex04_0.set
110
111
112
113
114 ##### DIBL Test : Returns DIBL Parameter #####
115 go atlas
116
117
118 # set material models
119 models cvt srh print
120 contact name=gate n.poly
121 interface qf=3e10
122
123
124 # get initial solution
125
126 solve init
127
128 method newton trap
129 solve prev
130
131
132 # Bias the drain a bit...
133 solve vdrain=0.025 vstep=0.025 vfinal=0.1 name=drain
134 # Ramp the gate
135 log outf=moslex04_1.log master
136 solve vgate=0 vstep=0.1 vdrain=0.1 vfinal=1.5 name=gate compl=1.1e-7
      cname=drain
137
138
139 # extract device parameters
140 extract init inf="moslex04_1.log"
141 extract name="nvt1" x.val from curve(abs(v."gate"),abs(i."drain")) where
      y.val=0.1e-6
142
143
144
145 # now open a dummy log file...
```

```
146 log off
147
148 # Now start again and ramp the drain to 3 volts...
149 solve init
150 # Bias the drain to 3 volts.....slowly at first....
151 solve vdrain=0.025 vstep=0.025 vfinal=0.1 name=drain
152 solve vdrain=0.25 vstep=0.25 vfinal=3 name=drain
153
154 # Ramp the gate again with another opened logfile...
155 log outf=moslex04_2.log master
156 solve vgate=0 vstep=0.1 vdrain=3 vfinal=1.5 name=gate compl=1.1e-7
      cname=drain
157
158
159 # extract the next device parameter with the drain now at 3 volts....
160 extract init inf="moslex04_2.log"
161 extract name="nvt2" x.val from curve(abs(v."gate"),abs(i."drain")) where
      y.val=0.1e-6
162
163
164
165 # Calculate a DIBL parameter....in V/V
166 extract name="ndibl" ($"nvt1"-$"nvt2")/(3.0-0.1)
167
168 tonyplot -overlay moslex04_1.log moslex04_2.log -set moslex04_log.set
169
170
171 quit
```

1.1.5. moslex05.in: NMOS: Body Effect Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating two Id/Vgs curves at different substrate biases and extracting the body effect(gamma) parameter. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vbs=0.0V
- ramp of drain voltage
- simple Id/Vgs curve generation with Vbs=-1.0V
- parameter extraction for body effect

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

In ATLAS the whole example is very similar in syntax to the DIBL parameter extraction example described previously in this section. The difference is that instead of different drain biases different substrate biases are used,

Two threshold voltages are measured using the extract syntax described in the DIBL extraction example. The body effect parameter is derived from the threshold voltages using the standard formula assuming 0.6V for phi.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

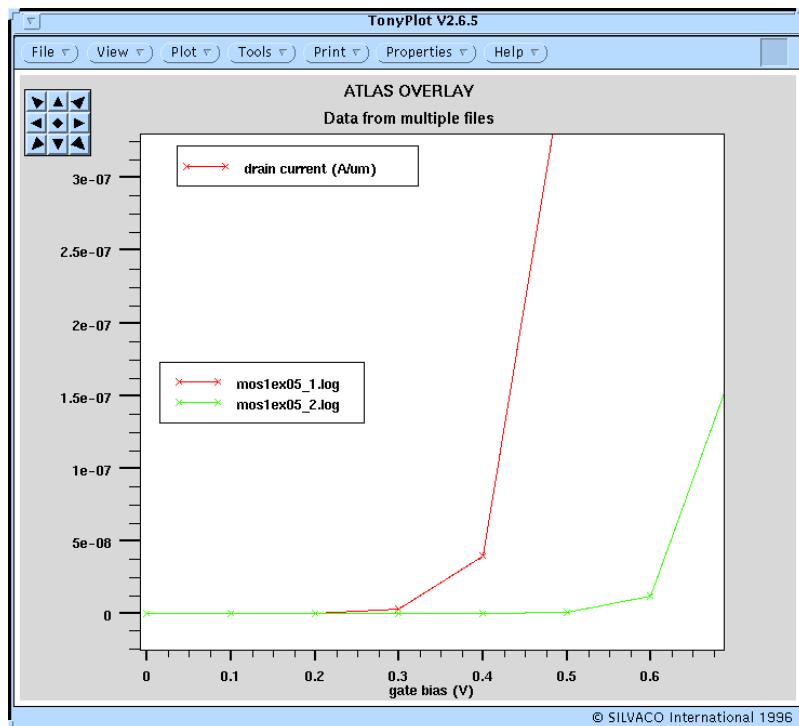


Figure 1.7: Body effect showing bulk voltage dependence of V_t for an NMOSFET

Input File mos1/mos1ex05.in :

```

1 ##### Gamma Test for an NMOS transistor #####
2
3 go athena
4
5 #
6 line x loc=0 spac=0.1
7 line x loc=0.2 spac=0.006
8 line x loc=0.4 spac=0.006
9 line x loc=0.5 spac=0.01
10 #
11 line y loc=0.00 spac=0.002
12 line y loc=0.2 spac=0.005
13 line y loc=0.5 spac=0.05

```

```
14 line y loc=0.8 spac=0.15
15 #
16 init orientation=100 c.phos=1e14 space.mul=3
17
18 #pwell formation including masking off of the nwell
19 #
20 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
21 #
22 etch oxide thick=0.02
23 #
24 #P-well Implant
25 #
26 implant boron dose=8e12 energy=100 pears
27
28 #
29 diffus temp=950 time=100 weto2 hcl=3
30 #
31 #N-well implant not shown -
32 #
33 # welldrive starts here
34 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
35 #
36 diffus time=220 temp=1200 nitro press=1
37 #
38 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
39 #
40 etch oxide all
41 #
42 #sacrificial "cleaning" oxide
43 diffus time=20 temp=1000 dryo2 press=1 hcl=3
44 #
45 etch oxide all
46 #
47 #gate oxide grown here:-
48 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
49 #
50 #
51
52
53 #
54 #vt adjust implant
55 implant boron dose=9.5e11 energy=10 pearson
56
```

```
57 #
58 depo poly thick=0.2 divi=10
59 #
60 #from now on the situation is 2-D
61 #
62 etch poly left p1.x=0.35
63 #
64 method fermi compress
65 diffuse time=3 temp=900 weto2 press=1.0
66 #
67 implant phosphor dose=3.0e13 energy=20 pearson
68 #
69 depo oxide thick=0.120 divisions=8
70 #
71 etch oxide dry thick=0.120
72 #
73 implant arsenic dose=5.0e15 energy=50 pearson
74 #
75 method fermi compress
76 diffuse time=1 temp=900 nitro press=1.0
77 #
78
79 #
80 etch oxide left p1.x=0.2
81 deposit alumin thick=0.03 divi=2
82 etch alumin right p1.x=0.18
83
84
85 # Extract a design parameter.....
86 extract name="gateox" thickness oxide mat.occcno=1 x.val=0.49
87 # Extract another design parameters...
88 # extract final S/D Xj...
89 extract name="nxj" xj silicon mat.occcno=1 x.val=0.1 junc.occcno=1
90 # extract the long chan Vt...
91 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
92 # extract a curve of conductance versus bias....
93 extract start material="Polysilicon" mat.occcno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
94 extract done name="sheet cond v bias" curve(bias,ldn.conduct materi-
    al="Silicon" mat.occcno=1 region.occcno=1) outfile="extract.dat"
95 # extract the N++ regions sheet resistance...
96 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.05 region.occcno=1
97 # extract the sheet rho under the spacer, of the LDD region...
```

```
98 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occno=1
      x.val=0.3 region.occno=1
99 # extract the surface conc under the channel....
100 extract name="chan surf conc" surf.conc impurity="Net Doping" materi-
      al="Silicon" mat.occno=1 x.val=0.45
101
102 structure mirror right
103
104 electrode name=gate x=0.5 y=0.1
105 electrode name=source x=0.1
106 electrode name=drain x=0.9
107 electrode name=substrate backside
108
109 structure outfile=moslex05_0.str
110
111 # plot the structure
112 tonyplot moslex05_0.str -set moslex05_0.set
113
114
115
116 ##### Body Effect Test : Returns N-channel Gamma #####
117 go atlas
118
119
120 # set material models
121 models cvt srh print
122
123 # Define the worksunction and the Qss....
124 contact name=gate n.poly
125 interface qf=3e10
126
127
128 # get initial solution
129 solve init
130 method newton
131 solve prev
132
133
134 # Bias the drain a bit...
135 solve vdrain=0.025 vstep=0.025 vfinal=0.1 name=drain
136 # Ramp the gate
137 log outf=moslex05_1.log master
138 solve vgate=0 vstep=0.1 vdrain=0.1 vfinal=2 name=gate \
139 compl=1.0e-7 cname=drain
```

```

140
141
142 # extract device parameters
143 extract init inf="moslex05_1.log"
144 extract name="nvt1" x.val from curve(abs(v."gate"),abs(i."drain")) where
      y.val=0.1e-6
145
146
147
148 # now open a dummy log file...
149 log off
150
151 # Now start again but with a substrate back-bias of a volt....
152 solve init
153 # Bias the substrate to -1 volt....
154 solve vdrain=0.05 vstep=0.05 vfinal=0.1 name=drain
155 solve vdrain=0.1 vsubstrate=-0.25 vstep=-0.25 vfinal=-1 name=substrate
156
157 # Ramp the gate again with another opened logfile...
158 log outf=moslex05_2.log master
159 solve vgate=0 vstep=0.1 vdrain=0.1 vsubstrate=-1 \
160 vfinal=2 name=gate compl=1.0e-7 cname=drain
161
162
163 extract init inf="moslex05_2.log"
164 extract name="nvt2" x.val from curve(abs(v."gate"),abs(i."drain")) where
      y.val=0.1e-6
165
166
167
168 # Calculate the parameter Gamma .... with phi = 0.6 eV....
169 extract name="ngamma" ($"nvt2"-$"nvt1")/((sqrt(1+0.6))-sqrt(0.6))
170
171 tonyplot -overlay moslex05_1.log moslex05_2.log -set moslex05_log.set
172
173 quit

```

1.1.6. moslex06.in: NMOS: Substrate and Gate Current Extraction

Requires: SSUPREM4/DEVEDIT/SPISCES

MOS ATHENA/DEVEDIT/ATLAS interface example simulating substrate and gate current versus gate bias using energy balance and impact ionization models. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)

- autointerface between ATHENA and DEVEDIT
- remeshing using DEVEDIT
- auto interface between DEVEDIT and ATLAS
- solution for a Vgs ramp with Vds=3.3V
- parameter extraction for maximum gate and substrate currents

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

The grid requirements for ATLAS simulation of impact ionization effects are more stringent than for the low electric field cases described earlier. DEVEDIT is used to remesh the ATHENA structure before proceeding to ATLAS. DEVEDIT has two modes. The graphical mode allows users to draw and interactively edit regions and impurities. The batch mode used here executes structure and mesh commands similar to these. The syntax used by DEVEDIT is described in the DEVEDIT manual. It can be constructed from the DECKBUILD Command menu or most commonly mesh edits made during a graphical session can be saved as a ‘command file’ from the **save** menu is DEVEDIT.

The **imp.refine** commands specify regrids on impurities. Here a regrid on net doping is done. The **constr.mesh** command defines the base mesh. The **refine** commands specify mesh refinements inside boxes specified by the coordinates in each statement.

The ATLAS simulation contains similar syntax to the simple examples described earlier in this section. The solution of the energy balance equations for electrons is specified by the parameter, **hcte.el**. The parameter, **hei**, specifies the hot carrier injection model, which gives the gate current. The equivalent **hcte.ho** and **hhii** exist for holes, but is not required in NMOS simulation.

The impact ionization model is selected on the **impact** statement. The parameter, **lrel.el**, sets the relaxation time for electrons in this model. Although the **hei** model is directly responsible for the gate current. There is no ‘special’ model required to simulate substrate current. Running this sweep of gate voltage with a high drain bias and including impact ionization and energy balance supplies all the necessary physics. The substrate current can simply be plotted from the log file in a similar manner to drain current. No special extraction of substrate current is needed.

The **extract** statements used in this run extract the peak value and position of the substrate and gate currents. The value of the peak current is measured first. Then this result is used in a current search to find the gate voltage where this current is measured.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

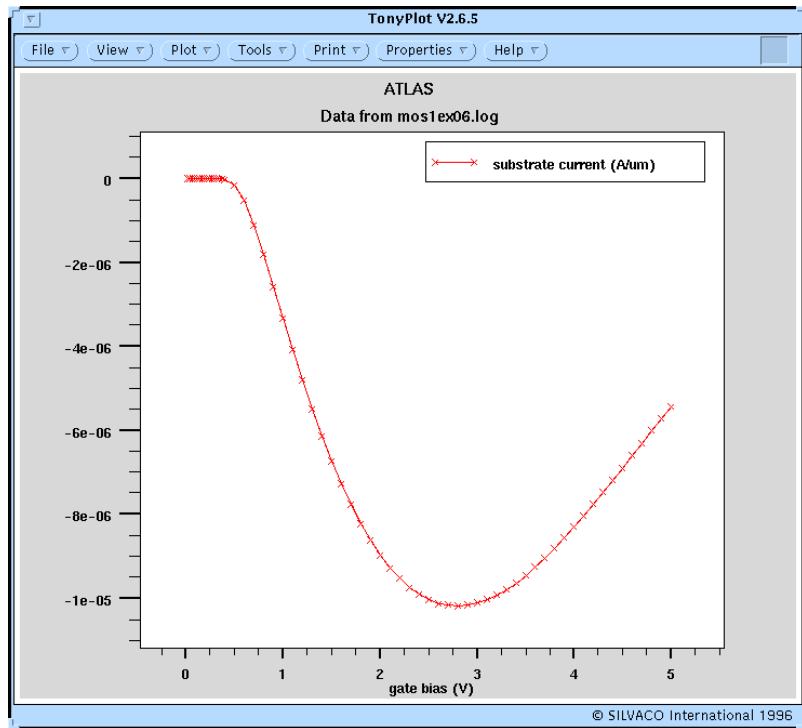


Figure 1.8: NMOS substrate current curve using energy balance models

Input File mos1/mos1ex06.in :

```

1
2 go athena
3
4 #
5 line x loc=0 spac=0.1
6 line x loc=0.2 spac=0.01
7 line x loc=0.5 spac=0.01
8 #
9 line y loc=0.00 spac=0.01
10 line y loc=0.2 spac=0.01
11 line y loc=0.5 spac=0.05
12 line y loc=0.8 spac=0.15
13 #
14 init orientation=100 c.phos=1e14 space.mul=3
15
16 #pwell formation including masking off of the nwell
17 #
18 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
19 #
20 etch oxide thick=0.02
21 #

```

```
22 #P-well Implant
23 #
24 implant boron dose=8e12 energy=100 pears
25 #
26 diffus temp=950 time=100 weto2 hcl=3
27 #
28 #N-well implant not shown -
29 #
30 # welldrive starts here
31 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
32 #
33 diffus time=220 temp=1200 nitro press=1
34 #
35 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
36 #
37 etch oxide all
38 #
39 #sacrificial "cleaning" oxide
40 diffus time=20 temp=1000 dryo2 press=1 hcl=3
41 #
42 etch oxide all
43 #
44 #gate oxide grown here:-
45 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
46 #
47 #
48 #
49 #
50 #vt adjust implant
51 implant boron dose=9.5e11 energy=10 pearson
52 #
53 depo poly thick=0.2 divi=10
54 #
55 #from now on the situation is 2-D
56 #
57 etch poly left p1.x=0.35
58 #
59 method fermi compress
60 diffuse time=3 temp=900 weto2 press=1.0
61 #
62 implant phosphor dose=3.0e13 energy=20 pearson
63 #
64 depo oxide thick=0.120 divisions=8
```

```
65 #
66 etch oxide dry thick=0.120
67 #
68 implant arsenic dose=5.0e15 energy=50 persion
69 #
70 method fermi compress
71 diffuse time=1 temp=900 nitro press=1.0
72 #
73
74 #
75 etch oxide left pl.x=0.2
76 deposit alumin thick=0.03 divi=2
77 etch alumin right pl.x=0.18
78
79 # Extract a design parameter.....
80 extract name="gateox" thickness oxide mat.occcno=1 x.val=0.49
81 # Extract another design parameters...
82 # extract final S/D Xj...
83 extract name="nxj" xj silicon mat.occcno=1 x.val=0.1 junc.occcno=1
84 # extract the long chan Vt...
85 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
86 # extract a curve of conductance versus bias....
87 extract start material="Polysilicon" mat.occcno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
88 extract done name="sheet cond v bias" curve(bias,ldn.conduct materi-
    al="Silicon" mat.occcno=1 region.occcno=1) outfile="extract.dat"
89 # extract the N++ regions sheet resistance...
90 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.05 region.occcno=1
91 # extract the sheet rho under the spacer, of the LDD region...
92 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.3 region.occcno=1
93 # extract the surface conc under the channel....
94 extract name="chan surf conc" surf.conc impurity="Net Doping" materi-
    al="Silicon" mat.occcno=1 x.val=0.45
95
96 structure mirror right
97
98 electrode name=gate x=0.5 y=0.1
99 electrode name=source x=0.1
100 electrode name=drain x=0.9
101 electrode name=substrate backside
102
103 go DevEdit
```

```
104
105
106 # Set Meshing Parameters
107 #
108 base.mesh height=1000000 width=1000000
109 #
110 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.points when=automatic
111 #
112 imp.refine imp="NetDoping" sensitivity=1
113 imp.refine min.spacing=0.02
114 #
115 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
116 max.width=1 min.height=0.0001 min.width=0.0001
117 #
118 # Perform mesh operations
119 #
120 Mesh Mode=MeshBuild
121 refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
122 refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
123 refine mode=both x1=0.65 y1=0.26 x2=0.82 y2=0.34
124 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
125 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
126 refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
127
128 structure outf=moslex06_0.str
129 tonyplot moslex06_0.str -set moslex06_0.set
130
131 go atlas
132
133 models cvt srh print hcte.el hei nearflg
134
135 impact selb length.rel lrel.el=0.02
136 contact name=gate n.poly
137 interface qf=3e10
138
139 material taun0=1e-7 taup0=1e-7
140 material taurel.el=0.2e-12 taumob.el=0.2e-12
141
142
143 solve init
144
145 method gummel block newton trap temp.tol=1.e-4
```

```

146
147 solve vdrain=0.1 vstep=0.1 vfinal=3.3 name=drain
148
149 log outf=moslex06.log master
150
151 method newton trap temp.tol=1.e-4
152 solve vgate=0.025 vstep=0.025 vfinal=0.4 name=gate
153 solve vgate=0.5 vstep=0.1 vfinal=5 name=gate
154
155
156 tonyplot moslex06.log -set moslex06_log.set
157
158 # Extract Substrate current peak value parameter....
159 extract init inf="moslex06.log"
160 extract name="nmax_isub_vd3.3" max(curve(abs(v."gate"),abs(i."substrate")))
161
162 # Extract gate voltage at the peak substrate current point....
163 extract init inf="moslex06.log"
164 extract name="nVgate_at_isubmax_vd3.3" x.val from
      curve(abs(v."gate"),abs(i."substrate")) where y.val=$"nmax_isub_vd3.3"
165
166 # Extract Gate current peak value parameter....
167 extract init inf="moslex06.log"
168 extract name="nmax_igate_vd3.3"
      (max(curve(abs(v."gate"),abs(i."gate"))))
169
170
171 # Extract gate voltage at the peak gate current point....
172 extract init inf="moslex06.log"
173 extract name="nVgate_at_isubmax_vd3.3" x.val from
      curve(abs(v."gate"),abs(i."gate")) where y.val=$"nmax_igate_vd3.3"
174
175
176 quit
177
178

```

1.1.7. moslex07.in: NMOS: Breakdown Voltage Extraction

Requires: SSUPREM4/DEVEDIT/SPISCES

ATHENA/DEVEDIT/ATLAS interface example simulating the breakdown voltage of an NMOS transistor. This example demonstrates:

- process simulation of a MOS transistor in ATHENA

- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and DEVEDIT
- remeshing using DEVEDIT
- autointerface between DEVEDIT and ATLAS
- solution for a Vds ramp with Vgs=0.0V to get breakdown

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

The grid requirements for ATLAS simulation of impact ionization effects are more stringent than for the low electric field cases described earlier. DEVEDIT is used to remesh the ATHENA structure before proceeding to ATLAS. The remeshing commands are described in the previous example in this section.

The ATLAS simulation contains similar syntax to the simpler examples described earlier in this section. The models, contact and interface parameters are the same, except that the concentration dependent SRH model is used. This provides a more accurate simulation of the pre-breakdown leakage current. The Selberherr impact ionization model is also selected.

On the method statement two parameters are chosen to restrict the use of the current convergence criteria used in ATLAS. Since the pre-breakdown leakage current is very low it is necessary to tighten the tolerances on current convergence. The parameter setting, `method climit=1e-4`, is also recommended in cases where the mesh is not as tight as the one used here.

The sequence of SOLVE statements shows a ramp in drain voltage. At first small steps are taken, but the main simulation is done in 0.5V steps. A compliance limit of 5.0e-8A/um is set on the drain. Compliance limits are useful in breakdown simulations to stop the simulation once the breakdown point is reached.

The value used here might seem rather low compared to typical values used in measurements. This is simply an issue of CPU time. Running the simulation up into microamp or milliamp ranges is possible, however the extra information gained is usually not worth the CPU time spent. Once the voltage exceeds the breakdown voltage no solutions will be possible. ATLAS will cut the voltage step and try again. It does this four times resulting in a minimum step of $(0.5)^4$ or 0.0625V. This is sufficient to resolve most breakdown voltages. It is possible for users to ramp using smaller voltage steps, to use current boundary conditions or curve tracing to further trace the IV curve to higher values of current. However usually this is not needed. Much extra CPU time might be required and yet the value of breakdown voltage remains the same to within the accuracy expected by simulation. Examples demonstrating snapback and curve tracing are included in other sections.

The `extract` syntax used to measure the breakdown voltage is of the current search type. This is preferred over the simple `max (v.“drain”)` syntax that could be used as it gives more consistent results.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

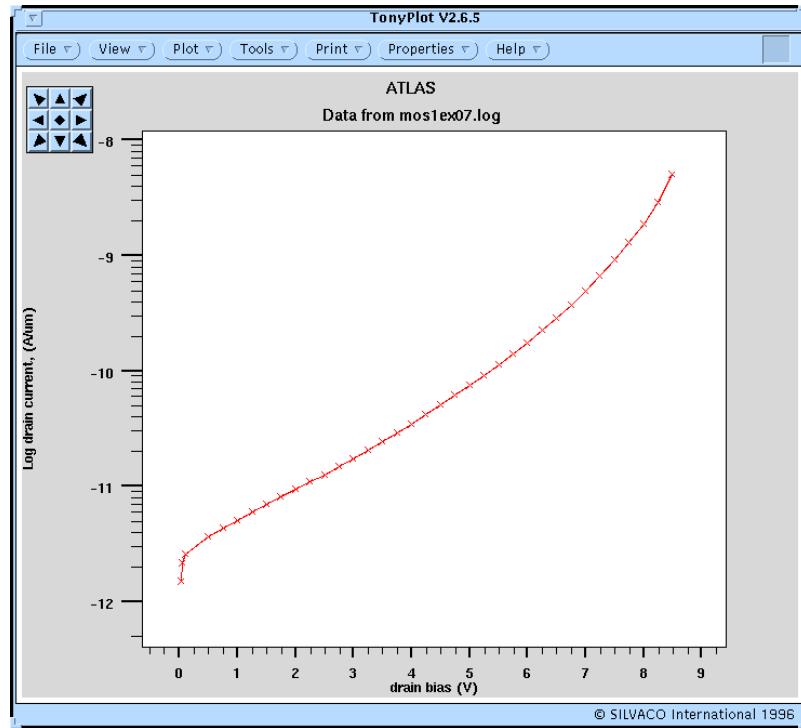


Figure 1.9: NMOS breakdown simulation. Slope of curve indicates a punchthrough effect as well as an avalanche effect

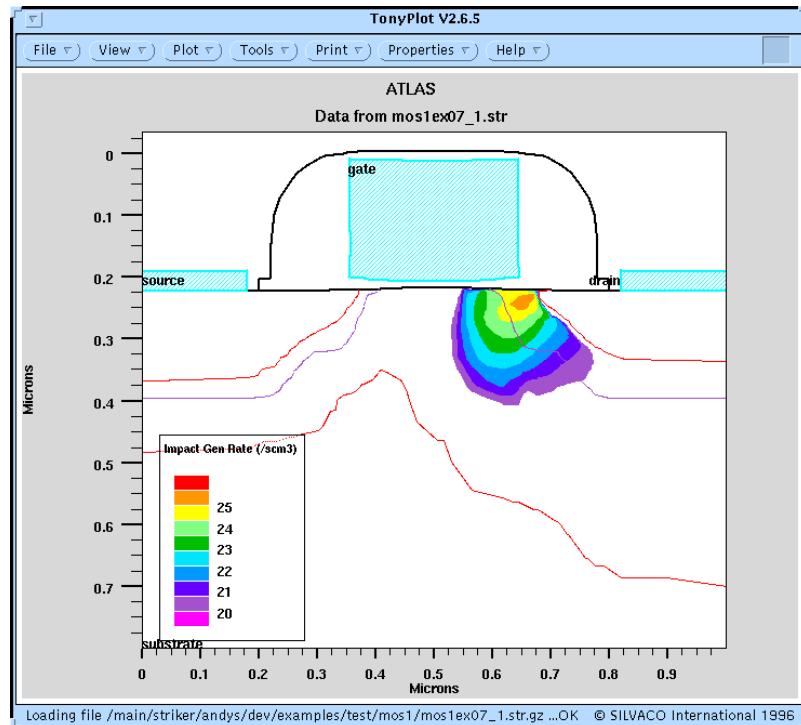


Figure 1.10: Contours of impact ionization in the MOSFET at the BV point

Input File mos1/mos1ex07.in:

1 go athena

```
2
3  #
4  line x loc=0 spac=0.1
5  line x loc=0.2 spac=0.01
6  line x loc=0.5 spac=0.01
7  #
8  line y loc=0.00 spac=0.01
9  line y loc=0.2 spac=0.01
10 line y loc=0.5 spac=0.05
11 line y loc=0.8 spac=0.15
12 #
13 init orientation=100 c.phos=1e14 space.mul=3
14 #
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=8e12 energy=100 pears
24 #
25 diffus temp=950 time=100 weto2 hcl=3
26 #
27 #N-well implant not shown -
28 #
29 # welldrive starts here
30 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
31 #
32 diffus time=220 temp=1200 nitro press=1
33 #
34 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
35 #
36 etch oxide all
37 #
38 #sacrificial "cleaning" oxide
39 diffus time=20 temp=1000 dryo2 press=1 hcl=3
40 #
41 etch oxide all
42 #
43 #gate oxide grown here:-
44 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
```

```
45 #
46 #
47
48 #
49 #vt adjust implant
50 implant boron dose=9.5e11 energy=10 pearson
51 #
52 depo poly thick=0.2 divi=10
53 #
54 #from now on the situation is 2-D
55 #
56 etch poly left p1.x=0.35
57 #
58 method fermi compress
59 diffuse time=3 temp=900 weto2 press=1.0
60 #
61 implant phosphor dose=3.0e13 energy=20 pearson
62 #
63 depo oxide thick=0.120 divisions=8
64 #
65 etch oxide dry thick=0.120
66 #
67 implant arsenic dose=5.0e15 energy=50 pearson
68 #
69 method fermi compress
70 diffuse time=1 temp=900 nitro press=1.0
71 #
72
73 #
74 etch oxide left p1.x=0.2
75 deposit alumin thick=0.03 divi=2
76 etch alumin right p1.x=0.18
77
78 # Extract a design parameter.....
79 extract name="gateox" thickness oxide mat.occno=1 x.val=0.49
80 # Extract another design parameters...
81 # extract final S/D Xj...
82 extract name="nxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
83 # extract the long chan Vt...
84 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
85 # extract a curve of conductance versus bias....
86 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
```

```
87 extract done name="sheet cond v bias" curve(bias,ldn.conduct material-
     al="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
88 # extract the N++ regions sheet resistance...
89 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1
     x.val=0.05 region.occno=1
90 # extract the sheet rho under the spacer, of the LDD region...
91 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occno=1
     x.val=0.3 region.occno=1
92 # extract the surface conc under the channel....
93 extract name="chan surf conc" surf.conc impurity="Net Doping" material-
     al="Silicon" mat.occno=1 x.val=0.45
94
95 structure mirror right
96
97 electrode name=gate x=0.5 y=0.1
98 electrode name=source x=0.1
99 electrode name=drain x=0.9
100 electrode name=substrate backside
101
102
103
104
105 go DevEdit
106
107
108 # Set Meshing Parameters
109 #
110 base.mesh height=1000000 width=1000000
111 #
112 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
     line.straightening=1 align.points when=automatic
113 #
114 imp.refine imp="NetDoping" sensitivity=1
115 imp.refine min.spacing=0.02
116 #
117 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
118 max.width=1 min.height=0.0001 min.width=0.0001
119 #
120 # Perform mesh operations
121 #
122 Mesh Mode=MeshBuild
123 refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
124 refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
125 refine mode=both x1=0.65 y1=0.26 x2=0.82 y2=0.34
```

```
126 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
127 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
128 refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
129 structure outf=moslex07_0.str
130
131 tonyplot moslex07_0.str -set moslex07_0.set
132
133
134 go atlas
135
136 # Set workfunction for poly gate and interface charge
137 contact name=gate n.polysilicon
138 interf qf=3E10
139
140 # Set models
141 models print cvt consrh
142
143 impact selb
144
145
146 method newton trap climit=1e-4
147
148 # open log file
149 log outf=moslex07.log
150
151 solve vdrain=0.025
152 solve vdrain=0.05
153 solve vdrain=0.1
154 solve vdrain=0.5
155
156 solve vstep=0.25 vfinal=12 name=dRAIN compl=5e-9 cname=dRAIN
157 save outf=moslex07_1.str
158
159
160 # Extract the design parameter, Vbd
161 extract name="NVbd" x.val from curve(abs(v."drain"),abs(i."drain")) where
    y.val=1e-9
162
163 tonyplot moslex07.log -set moslex07_log.set
164 tonyplot moslex07_1.str -set moslex07_1.set
165
166 quit
```

1.1.8. mos1ex08.in: PMOS: Id/Vgs and Threshold Voltage Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating an Id/Vgs curve and extracting threshold voltage and other SPICE parameters. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- auto interface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=-0.1V
- IV Curve parameter extraction for Vt, Beta and Theta

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

The unique feature of this example is the IV data simulated and the extraction syntax used. The model, interface and contact statements in ATLAS are also as in the previous example.

The sequence of Solve statements is set to ramp the gate bias with the drain voltage at -0.1V. Solutions are obtained at -0.25V intervals up to -3.0V. All terminal characteristics are saved to the file mos1ex02_1.log as specified in the Log statement.

The extract statement at the end of the file are used to measure the threshold voltage and other SPICE parameters. The results from the extract statements are printed in the run-time output, saved to a file called results.final and optionally used in the optimizer or VWF automation tools. The syntax used in these statements is freely composed of operators such as maximum value (max) and simulation results such as drain current (i.“drain”). One operator of particular use in PMOS device extraction is abs(). This takes the absolute value of a variable and can be used to convert make all PMOS and NMOS extractions equivalent.

The name parameter specified only a user-defined label. The routines are not hard-coded to these names. Thus the first extraction statement reads: extract the value called pvt found by taking the x intercept of the maximum slope to the curve of drain voltage vs. drain current and subtracting half the drain voltage. This just one definition of threshold voltage. Current search methods are also possible and is described under the DIBL example later in this section. The VWF INTERACTIVE TOOLS manual has details of the extract syntax.

The second extract statement measures the gain (or Beta). This is defined as the value of the steepest slope to the Id/Vgs curve divided by the drain voltage. The final extraction is for the SPICE level 3 mobility roll-off parameter (or Theta). This syntax shows the use of the syntax, \$"pvt" and \$"pbeta". This tells DECKBUILD to substitute the previously extracted values of threshold and beta into these places in the equation.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

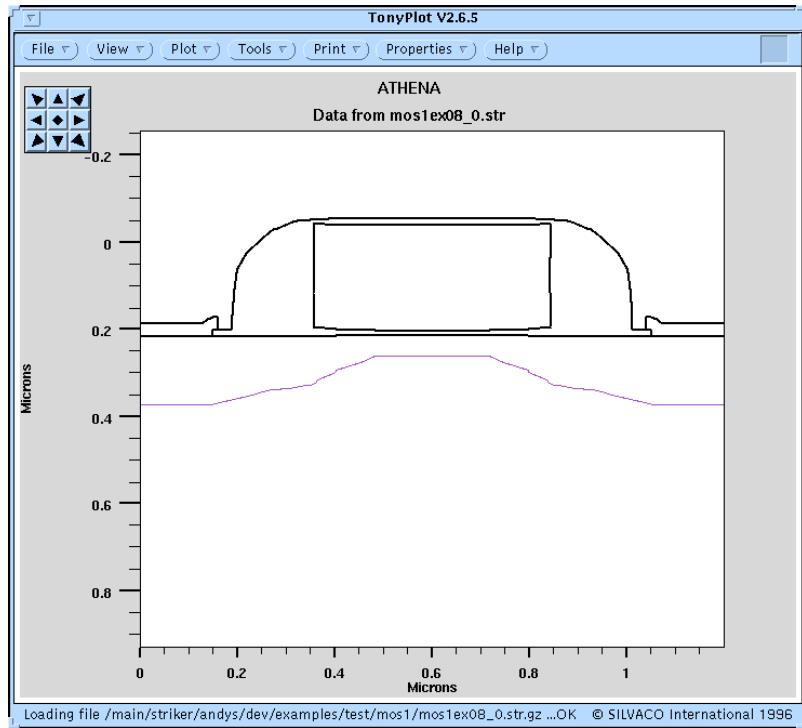


Figure 1.11: Junction and Material boundaries for a P-channel MOSFET. This device has a buried channel due to p-implant under the gate.

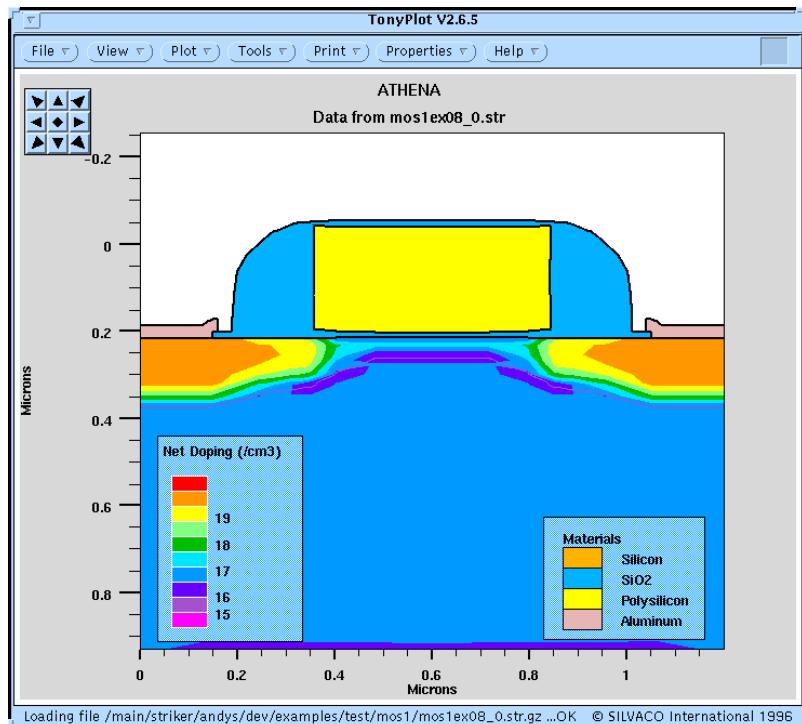


Figure 1.12: Contours of doping in the PMOS transistor

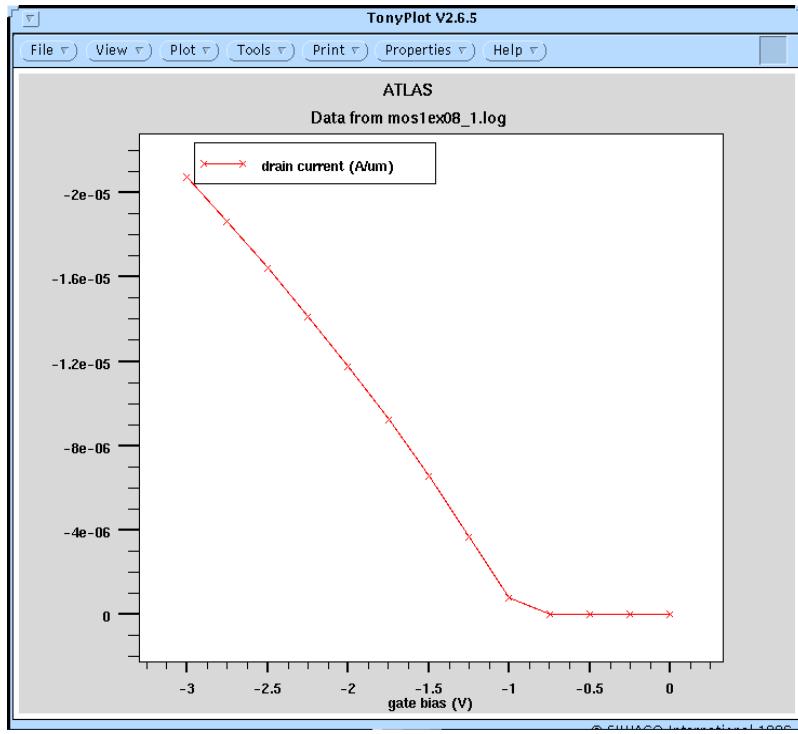


Figure 1.13: PMOS Id/Vgs curve for extracting threshold voltage and linear gain

Input File mos1/mos1ex08.in:

```

1 go athena
2 #
3 # Set up a mesh suitable for a single MOSFET device....
4 line x loc=0 spac=0.1
5 line x loc=0.35 spac=0.02
6 line x loc=0.6 spac=0.1
7 #
8 line y loc=0.00 spac=0.005
9 line y loc=0.3 spac=0.015
10 line y loc=0.5 spac=0.02
11 line y loc=2 spac=0.2
12 line y loc=5 spac=1
13 #
14 # Start off by defining silicon with 1e14 phos doping...
15 # Decrease the following space.mult parameter for a denser
16 # mesh and more accuracy...
17 init orientation=100 c.phos=1e14 space.mult=2
18 #
19 #pwell formation including masking off of the nwell
20 #
21 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3

```

```
22 #
23 etch oxide thick=0.02
24 #
25 #N-well Implant
26 implant amorphous phos dose=9e12 energy=100 pears
27 #
28 diffus temp=950 time=100 weto2 hcl=3
29 #
30 #N-well implant amorphous not shown -
31 #
32 # welldrive
33 diffus time=220 temp=1200 nitro press=1
34 #
35 etch oxide all
36 #
37 #sacrificial "cleaning" oxide
38 diffus time=20 temp=1000 dryo2 press=1 hcl=3
39 #
40 etch oxide all
41 #
42 #gate oxide grown here:-
43 set partial_press=1.0
44 diffus time=10 temp=800 nitrogen hcl=3
45 diffus time=2 temp=900 dryo2 press=$partial_press
46 diffus time=13 temp=900 dryo2 press=$partial_press hcl=3
47 diffus time=10 temp=900 nitrogen hcl=3
48 diffus time=10 temp=800 t.final=800 nit hcl=3
49 #
50 # Extract a design parameter.....
51 extract name="gateox" thickness oxide mat.occno=1 x.val=0.005
52 #
53 #vt adjust implant amorphous
54 implant amorphous bf2 dose=1.20e12 energy=25 pearson
55 #
56 depo poly thick=0.250 div=3
57 #
58 etch poly left p1.x=0.35
59 #
60 # Relax the mesh below the 0.5um plane, for speed....
61 relax y.min=0.5
62 #
63 method fermi compress
64 diffuse time=5 temp=900 weto2 press=0.8
```

```
65 #
66 # PLDD implant amorphous
67 implant amorphous bf2 dose=2.0e14 energy=50 pearson
68 #
69 # This is a good way of defining the spacer.....define a variable
70 # first with the 'set' command....
71 set spacer=0.15
72 depo oxide thick=$"spacer" divisions=5
73 etch oxide dry thick=$"spacer"+0.005
74 #
75 # P++ Implant
76 implant amorphous bf2 dose=1.50e15 energy=60 pearson
77 #
78 #
79 # Final anneal.
80 method fermi compress
81 diffuse time=5 temp=900 nitro press=1.0
82 #
83
84
85
86
87 # Extract other design parameters...
88 # extract final S/D Xj...
89 extract name="pxj" xj silicon mat.occcno=1 x.val=0.1 junc.occcno=1
90 # extract the long chan Vt...
91 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
92 # extract a curve of conductance versus bias....
93 extract start material="Polysilicon" mat.occcno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
94 extract done name="sheet cond v bias" curve(bias,ldn.conduct material=
    "Silicon" mat.occcno=1 region.occcno=1) outfile="extract.dat"
95 # extract the P++ regions sheet resistance...
96 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.05 region.occcno=1
97 # extract the sheet rho under the spacer, of the LDD region...
98 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occcno=1
    x.val=0.3 region.occcno=1
99 # extract the surface conc under the channel....
100 extract name="pchan surf conc" surf.conc impurity="Net Doping" material=
    "Silicon" mat.occcno=1 x.val=0.45
101 # Etch contact cuts and place the aluminium where electrodes are re-
    quired.....
102 etch oxide left p1.x=0.15
103 deposit alumin thick=0.03 div=2
```

```
104 etch alumini right p1.x=0.16
105
106
107 # mirror the structure.....
108 structure mirror right
109
110
111
112 # Name the electrodes...
113 electrode name=gate x=0.5
114 electrode name=source x=0
115 electrode name=drain x=1.1
116 electrode name=substrate backside
117
118
119 # output the structure
120 structure outfile=moslex08_0.str
121
122 # plot it
123 tonyplot moslex08_0.str -set moslex08_0.set
124
125
126 ##### PVt Test : Returns PVt, PBeta and PTheta #####
127 go atlas
128
129 # set material models
130 models cvt srh print
131 contact name=gate n.poly
132 interface qf=3e10
133
134 # get initial solution
135 solve init
136
137
138 method newton trap
139 solve prev
140
141 # Bias the drain a bit...
142 solve vdrain=-0.1 name=drain
143
144 # Ramp the gate
145 log outf=moslex08_1.log master
146 solve vgate=0 vstep=-0.25 vfinal=-3.0 vdrain=-0.1 name=gate
```

```
147 save outf=moslex08_1.str
148
149 # extract device parameters.....
150 extract init inf="moslex08_1.log"
151 extract name="pvt" (xintercept(maxs-
    lope(curve(abs(v."gate"),abs(i."drain")))) - abs(ave(v."drain")))/2.0)
152
153
154 extract init inf="moslex08_1.log"
155 extract name="pbeta" ((slope(maxs-
    lope(curve(abs(v."gate"),abs(i."drain")))) * (1.0/
    abs(ave(v."drain")))))
156
157 extract init inf="moslex08_1.log"
158 extract name="ptheta" ((max(abs(v."drain")) * $"pbeta")/
    max(abs(i."drain")) - (1.0 / (max(abs(v."gate")) - ($"pvt"))))
159
160
161
162 # plot results
163 tonyplot moslex08_1.log -set moslex08_1_log.set
164
165 quit
```

1.1.9. moslex09.in: PMOS: Family of Id/Vds Curves

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example demonstrating the simulation of a family of Id/Vds curves. The maximum drive current and saturation slope are extracted. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- Id/Vds curve generation with Vgs=-1.1, -2.2 and -3.3V
- IV Curve parameter extraction for Idmax and saturation slope

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first PMOS example in this section.

A more advanced sequence of solve statements is used for this example. Three Id/Vds curves are required at different gate voltages. The first part of the solve sequence sets up the initial point of the three curves. For each of the three gate voltages a solution with Vds=0.0 is simulated and the results saved to a solution file.

Each of these three solution files is then loaded in turn into ATLAS. A log file is opened and the ramp of Vds is set. When a file is loaded the voltages in ATLAS are reset to the values in the file.

At the end of the simulation, extract is used to measure the peak current and the saturation slope. From the shape of the Id/Vds curves, the saturation slope is clearly the minimum value of the gra-

dient along the curve as long as the absolute values of current and voltage are taken. Finally, the three Id/Vds curves are overlaid in TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

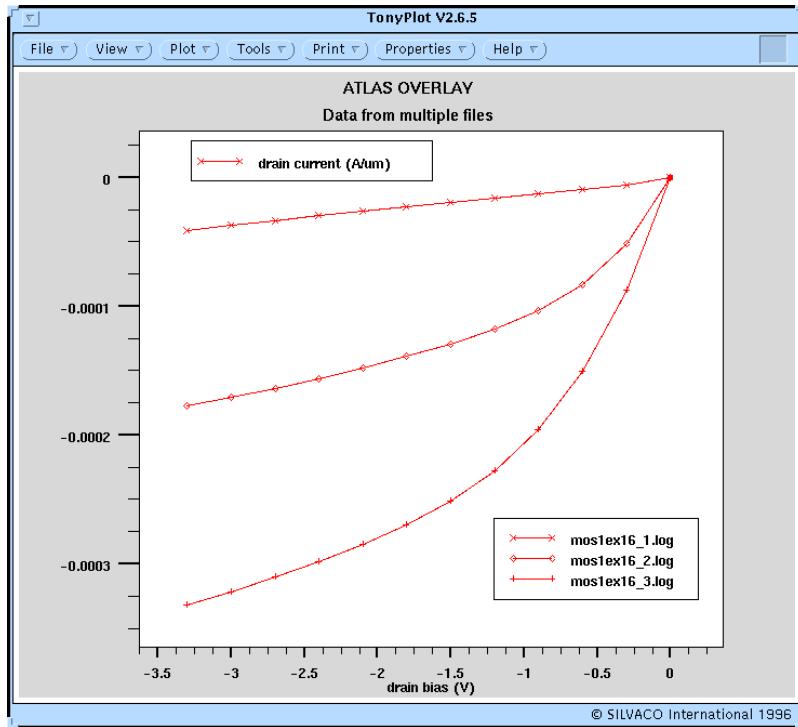


Figure 1.14: Family of ID/VDS curves from a p-channel MOSFET

Input File mos1/mos1ex09.in:

```

1  # This is a simple Input File representing a Process flow and a device
2  # test. All lines beginning with a '#' sign
3
4
5  may be treated as directive
6  # comments.....
7
8  # Start the Athena Process simulator running...
9  go athena
10 #
11 # Set up a mesh suitable for a single MOSFET device....
12 line x loc=0 spac=0.1
13 line x loc=0.35 spac=0.02
14 line x loc=0.5 spac=0.1
15 #
16 line y loc=0.00 spac=0.005
17 line y loc=0.3 spac=0.015

```

```
18 line y loc=0.5 spac=0.02
19 line y loc=2 spac=0.2
20 line y loc=5 spac=1
21 #
22 # Start off by defining silicon with 1e14 phos doping...
23 # Decrease the following space.mult parameter for a denser
24 # mesh and more accuracy...
25 init orientation=100 c.phos=1e14 space.mult=2
26 #
27 #pwell formation including masking off of the nwell
28 #
29 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
30 #
31 etch oxide thick=0.02
32 #
33 #N-well Implant
34 implant amorphous phos dose=1.0e13 energy=100 pears
35 #
36 diffus temp=950 time=100 weto2 hcl=3
37 #
38 #N-well implant amorphous not shown -
39 #
40 # welldrive
41 diffus time=220 temp=1200 nitro press=1
42 #
43 etch oxide all
44 #
45 #sacrificial "cleaning" oxide
46 diffus time=20 temp=1000 dryo2 press=1 hcl=3
47 #
48 etch oxide all
49 #
50 #gate oxide grown here:-
51 set partial_press=1.0
52 diffus time=10 temp=800 nitrogen hcl=3
53 diffus time=2 temp=900 dryo2 press=$partial_press
54 diffus time=13 temp=900 dryo2 press=$partial_press hcl=3
55 diffus time=10 temp=900 nitrogen hcl=3
56 diffus time=10 temp=800 t.final=800 nit hcl=3
57 #
58 # Extract a design parameter.....
59 extract name="gateox" thickness oxide mat.ocno=1 x.val=0.005
60 #
```

```
61 #vt adjust implant amorphous
62 implant amorphous bf2 dose=1.10e12 energy=25 pearson
63 #
64 depo poly thick=0.250 div=3
65 #
66 etch poly left p1.x=0.35
67 #
68 # Relax the mesh below the 0.5um plane, for speed....
69 relax y.min=0.5
70 #
71 method fermi compress
72 diffuse time=5 temp=900 weto2 press=0.8
73 #
74 # PLDD implant amorphous
75 implant amorphous bf2 dose=1.0e14 energy=50 pearson
76 #
77 # This is a good way of defining the spacer.....define a variable
78 # first with the 'set' command....
79 set spacer=0.15
80 depo oxide thick="$spacer" divisions=5
81 etch oxide dry thick="$spacer"+0.005
82 #
83 # P++ Implant
84 implant amorphous bf2 dose=1.0e15 energy=60 pearson
85 #
86 #
87 # Final anneal.
88 method fermi compress
89 diffuse time=5 temp=900 nitro press=1.0
90 #
91
92
93
94
95 # Extract other design parameters...
96 # extract final S/D Xj...
97 extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
98 # extract the long chan Vt...
99 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
100 # extract a curve of conductance versus bias....
101 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
102 extract done name="sheet cond v bias" curve(bias,ldn.conduct materi-
    al="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
```

```
103 # extract the P++ regions sheet resistance...
104 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occno=1
      x.val=0.05 region.occno=1
105 # extract the sheet rho under the spacer, of the LDD region...
106 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occno=1
      x.val=0.3 region.occno=1
107 # extract the surface conc under the channel....
108 extract name="pchan surf conc" surf.conc impurity="Net Doping" material="Silicon" mat.occno=1 x.val=0.45
109 # Etch contact cuts and place the aluminium where electrodes are required.....
110 etch oxide left p1.x=0.15
111 deposit alumin thick=0.03 div=2
112 etch alumin right p1.x=0.16
113
114
115 # mirror the structure....
116 structure mirror right
117
118
119
120 # Name the electrodes...
121 electrode name=gate x=0.5
122 electrode name=source x=0
123 electrode name=drain x=0.9
124 electrode name=substrate backside
125
126
127 # output the structure
128 structure outfile=moslex09_0.str
129
130 # plot it
131 tonyplot moslex09_0.str -set moslex09_0.set
132
133
134
135 go atlas2
136
137 # define the Gate workfunction
138 contact name=gate n.poly
139
140 # Define the Gate Qss
141 interface qf=3e10
142
```

```

143 # Use the cvt mobility model for MOS
144 models cvt srh
145
146 # set gate biases with Vds=0.0
147 solve init
148 solve vgate=-1.1 outf=solve_tmp1
149 solve vgate=-2.2 outf=solve_tmp2
150 solve vgate=-3.3 outf=solve_tmp3
151
152 #load in temporary files and ramp Vds
153 load infile=solve_tmp1
154 log outf=moslex09_1.log
155 solve name=drain vdrain=0 vfinal=-3.3 vstep=-0.3
156
157 load infile=solve_tmp2
158 log outf=moslex09_2.log
159 solve name=drain vdrain=0 vfinal=-3.3 vstep=-0.3
160
161 load infile=solve_tmp3
162 log outf=moslex09_3.log
163 solve name=drain vdrain=0 vfinal=-3.3 vstep=-0.3
164
165 # extract max current and saturation slope
166 extract name="pidsmmax" max(abs(i."drain"))
167 extract name="p_sat_slope" slope(mins-
    lope(curve(abs(v."drain"),abs(i."drain")))))
168
169 tonyplot -overlay moslex09_1.log moslex09_2.log moslex09_3.log -set
    moslex09_1.set
170
171 quit

```

1.1.10. moslex10.in: PMOS: Sub-Threshold Slope Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating an Id/Vgs curve and extracting sub-threshold slope. No advanced features are used in this example so as to demonstrate simple functionality. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=-0.1V
- parameter extraction for Sub-Threshold Slope

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

In ATLAS the same sequence of statements is used as in the first example in this section. The only difference is that the gate voltage is ramped from zero to -1.0V only in -0.1V steps.

The extract statement used in this example measures the sub-threshold slope of the MOSFET. The syntax uses the operators log10(), slope() and curve() to specify the reciprocal of the steepest slope to the curve of V_{gs} vs. $\log(I_d)$. Note that the operator log10() is needed here. The operator log() specifies the function for natural logarithm. It is obviously necessary to take the absolute value of I_d before the log10() operator is used.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

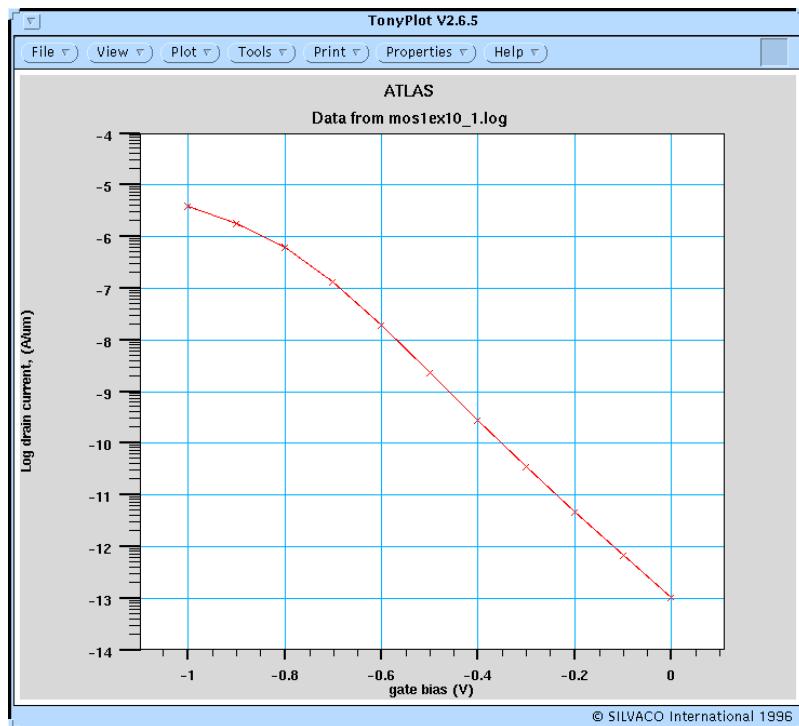


Figure 1.15: Sub-threshold swing extraction from a $\log(I_d)$ vs V_{gs} plot for PMOS

Input File mos1/mos1ex10.in :

```

1  # This is a simple Input File representing a Process flow and a device
2  # text. All lines begining with a '#' sign may be treated as directive
3  # comments.....
4
5  # Start the Athena Process simulator running...
6  go athena
7  #
8  # Set up a mesh suitable for a single MOSFET device....
9  line x loc=0 spac=0.1
10 line x loc=0.35 spac=0.02

```

```
11 line x loc=0.5 spac=0.1
12 #
13 line y loc=0.00 spac=0.005
14 line y loc=0.3 spac=0.015
15 line y loc=0.5 spac=0.02
16 line y loc=2 spac=0.2
17 line y loc=5 spac=1
18 #
19 # Start off by defining silicon with 1e14 phos doping...
20 # Decrease the following space.mult parameter for a denser
21 # mesh and more accuracy...
22 init orientation=100 c.phos=1e14 space.mult=2
23 #
24 #pwell formation including masking off of the nwell
25 #
26 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
27 #
28 etch oxide thick=0.02
29 #
30 #N-well Implant
31 implant amorphous phos dose=9e12 energy=100 pears
32 #
33 diffus temp=950 time=100 weto2 hcl=3
34 #
35 #N-well implant amorphous not shown -
36 #
37 # welldrive
38 diffus time=220 temp=1200 nitro press=1
39 #
40 etch oxide all
41 #
42 #sacrificial "cleaning" oxide
43 diffus time=20 temp=1000 dryo2 press=1 hcl=3
44 #
45 etch oxide all
46 #
47 #gate oxide grown here:-
48 set partial_press=1.0
49 diffus time=10 temp=800 nitrogen hcl=3
50 diffus time=2 temp=900 dryo2 press=$partial_press
51 diffus time=11 temp=900 dryo2 press=$partial_press hcl=3
52 diffus time=10 temp=900 nitrogen hcl=3
53 diffus time=10 temp=800 t.final=800 nit hcl=3
```

```
54 #
55 # Extract a design parameter.....
56 extract name="gateox" thickness oxide mat.occno=1 x.val=0.005
57 #
58 #vt adjust implant amorphous
59 implant amorphous bf2 dose=1.20e12 energy=25 pearson
60 #
61 depo poly thick=0.250 div=3
62 #
63 etch poly left p1.x=0.35
64 #
65 # Relax the mesh below the 0.5um plane, for speed....
66 relax y.min=0.5
67 #
68 method fermi compress
69 diffuse time=5 temp=900 weto2 press=0.8
70 #
71 # PLDD implant amorphous
72 implant amorphous bf2 dose=2.0e14 energy=50 pearson
73 #
74 # This is a good way of defining the spacer.....define a variable
75 # first with the 'set' command....
76 set spacer=0.15
77 depo oxide thick=$"spacer" divisions=5
78 etch oxide dry thick=$"spacer"+0.005
79 #
80 # P++ Implant
81 implant amorphous bf2 dose=1.50e15 energy=60 pearson
82 #
83 #
84 # Final anneal.
85 method fermi compress
86 diffuse time=5 temp=900 nitro press=1.0
87 #
88
89
90
91
92 # Extract other design parameters...
93 # extract final S/D Xj...
94 extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
95 # extract the long chan Vt...
96 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
```

```
97 # extract a curve of conductance versus bias....
98 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
99 extract done name="sheet cond v bias" curve(bias,ldn.conduct materi-
    al="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
100 # extract the P++ regions sheet resistance...
101 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.05 region.occno=1
102 # extract the sheet rho under the spacer, of the LDD region...
103 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.3 region.occno=1
104 # extract the surface conc under the channel....
105 extract name="pchan surf conc" surf.conc impurity="Net Doping" materi-
    al="Silicon" mat.occno=1 x.val=0.45
106 # Etch contact cuts and place the aluminium where electrodes are re-
    quired.....
107 etch oxide left p1.x=0.15
108 deposit alumin thick=0.03 div=2
109 etch alumin right p1.x=0.16
110
111
112 # mirror the structure....
113 structure mirror right
114
115
116
117 # Name the electrodes...
118 electrode name=gate x=0.5
119 electrode name=source x=0
120 electrode name=drain x=0.9
121 electrode name=substrate backside
122
123
124 # output the structure
125 structure outfile=moslex10_0.str
126
127 # plot it
128 tonyplot moslex10_0.str -set moslex10_0.set
129
130
131
132 ##### SubVt Test : Returns PSubVt Parameter #####
133 go atlas
134
135
```

```
136 # set material models
137 models cvt srh print
138 contact name=gate n.poly
139 interface qf=1e10
140
141
142 # get initial solution
143
144 solve init
145
146 method newton trap
147 solve prev
148
149
150 # Bias the drain a bit...
151 solve vdrain=-0.025 vstep=-0.025 vfinal=-0.1 name=drain
152 # Ramp the gate to a volt...
153 log outf=moslex10_1.log master
154 solve vgate=0 vstep=-0.1 vfinal=-1.0 name=gate
155
156
157 # extract the device parameter SubVt...
158 extract init inf="moslex10_1.log"
159 extract name="psubvt" 1.0/slope(maxs-
    lope(curve(abs(v."gate"),log10(abs(i."drain")))))
160
161 tonyplot moslex10_1.log -set moslex10_1_log.set
162
163 quit
```

1.1.11. moslex11.in: PMOS: DIBL Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating two Id/Vgs curves at different drain biases and extracting the drain-induced barrier lowering (DIBL) parameter. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vds=-0.1V
- ramp of drain voltage
- simple Id/Vgs curve generation with Vds=-3.0V
- parameter extraction for the DIBL parameter

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

In ATLAS the models, interface and contact statements are also the same as the first example. The extraction of the first Id/Vgs curve is very similar to the previous threshold voltage extraction example.

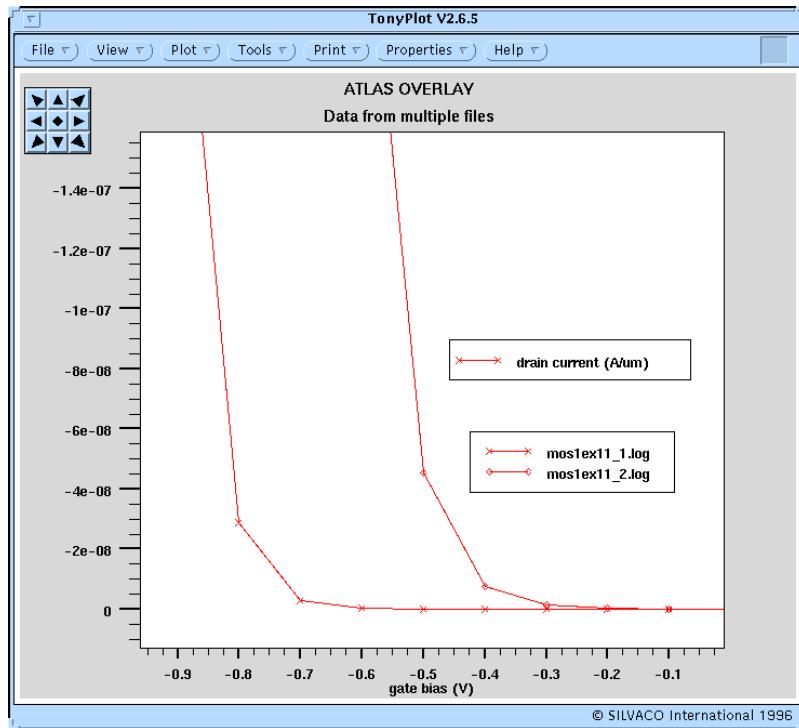
One difference is the use of the syntax, `compl=1.1e-7 cname=drain`. This sets a compliance limit on the drain current. Although the Solve statement calls for a ramp in gate voltage from zero to -1.5V, once the trigger current specified by `compl` is exceeded on the electrode specified by `cname` then the gate voltage ramp will step and ATLAS will execute the next line of syntax. Note that the compliance value does not need to be signed. A current more negative than -1.1e-7 will also trigger the compliance limit. Compliances are more commonly used in breakdown simulations but can be used in this way to stop voltage ramps once the area of interest is passed.

All results from the first Id/Vgs curve are saved to the file specified by the first log statement. In ATLAS the only way to stop the IV points being saved is either to specify another LOG statement or exit the simulator. That is why the statement, `log outf=dummy.log`, is needed. This stops the output from the drain voltage ramp being saved to the Id/Vgs log file.

The second `solve init` statement resets all applied voltages to zero. Then the drain is ramped to -3.0V and the gate ramp with compliance is repeated.

After each gate ramp, the threshold voltage was extracted using a different syntax than the PMOS threshold voltage example described earlier in this section. In this example, the threshold is determined by looking for the voltage where the drain current reaches a user-defined value. The syntax, `x.val from curve (x,y) where y.val=<number>` is used. At large drain biases this method is preferred for threshold extraction over the steepest slope approach. The search value of 0.1uA/um of current is typical for channel lengths around 1um. These thresholds are stored as values `pvt1` and `pvt2` in DECKBUILD. The final extract statement is used to obtain the DIBL parameter. It is the difference in threshold voltage divided by the difference in the drain bias.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

Figure 1.16: Drain voltage dependence of V_t for a PMOSFET**Input File mos1/mos1ex11.in:**

```

1  # This is a simple Input File representing a Process flow and a device
2  # text. All lines beginning with a '#' sign may be treated as directive
3  # comments.....
4
5  # Start the Athena Process simulator running...
6 go athena
7 #
8 # Set up a mesh suitable for a single MOSFET device....
9 line x loc=0 spac=0.1
10 line x loc=0.35 spac=0.02
11 line x loc=0.5 spac=0.1
12 #
13 line y loc=0.00 spac=0.005
14 line y loc=0.3 spac=0.015
15 line y loc=0.5 spac=0.02
16 line y loc=2 spac=0.2
17 line y loc=5 spac=1
18 #
19 # Start off by defining silicon with 1e14 phos doping...
20 # Decrease the following space.mult parameter for a denser
21 # mesh and more accuracy...

```

```
22 init orientation=100 c.phos=1e14 space.mult=2
23 #
24 #pwell formation including masking off of the nwell
25 #
26 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
27 #
28 etch oxide thick=0.02
29 #
30 #N-well Implant
31 implant amorphous phos dose=1e13 energy=100 pears
32 #
33 diffus temp=950 time=100 weto2 hcl=3
34 #
35 #N-well implant amorphous not shown -
36 #
37 # welldrive
38 diffus time=220 temp=1200 nitro press=1
39 #
40 etch oxide all
41 #
42 #sacrificial "cleaning" oxide
43 diffus time=20 temp=1000 dryo2 press=1 hcl=3
44 #
45 etch oxide all
46 #
47 #gate oxide grown here:-
48 set partial_press=1.0
49 diffus time=10 temp=800 nitrogen hcl=3
50 diffus time=2 temp=900 dryo2 press=$partial_press
51 diffus time=11 temp=900 dryo2 press=$partial_press hcl=3
52 diffus time=10 temp=900 nitrogen hcl=3
53 diffus time=10 temp=800 t.final=800 nit hcl=3
54 #
55 # Extract a design parameter.....
56 extract name="gateox" thickness oxide mat.occno=1 x.val=0.005
57 #
58 #vt adjust implant amorphous
59 implant amorphous bf2 dose=1.10e12 energy=25 pearson
60 #
61 depo poly thick=0.250 div=3
62 #
63 etch poly left p1.x=0.35
64 #
```

```
65 # Relax the mesh below the 0.5um plane, for speed....
66 relax y.min=0.5
67 #
68 method fermi compress
69 diffuse time=5 temp=900 weto2 press=0.8
70 #
71 # PLDD implant amorphous
72 implant amorphous bf2 dose=5e13 energy=40 pearson
73 #
74 # This is a good way of defining the spacer.....define a variable
75 # first with the 'set' command....
76 set spacer=0.15
77 depo oxide thick="$spacer" divisions=5
78 etch oxide dry thick="$spacer"+0.005
79 #
80 # P++ Implant
81 implant amorphous bf2 dose=1.50e15 energy=45 pearson
82 #
83 #
84 # Final anneal.
85 method fermi compress
86 diffuse time=5 temp=900 nitro press=1.0
87 #
88
89
90
91
92 # Extract other design parameters...
93 # extract final S/D Xj...
94 extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
95 # extract the long chan Vt...
96 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
97 # extract a curve of conductance versus bias....
98 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
99 extract done name="sheet cond v bias" curve(bias,ldn.conduct material="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
100 # extract the P++ regions sheet resistance...
101 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.05 region.occno=1
102 # extract the sheet rho under the spacer, of the LDD region...
103 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.3 region.occno=1
104 # extract the surface conc under the channel....
```

```
105 extract name="pchan surf conc" surf.conc impurity="Net Doping" materi-
    al="Silicon" mat.occcno=1 x.val=0.45
106 # Etch contact cuts and place the aluminium where electrodes are re-
    quired.....
107 etch oxide left p1.x=0.15
108 deposit alumin thick=0.03 div=2
109 etch alumin right p1.x=0.16
110
111
112 # mirror the structure.....
113 structure mirror right
114
115
116
117 # Name the electrodes...
118 electrode name=gate x=0.5
119 electrode name=source x=0
120 electrode name=drain x=0.9
121 electrode name=substrate backside
122
123
124 # output the structure
125 structure outfile=moslex11_0.str
126
127 # plot it
128 tonyplot moslex11_0.str -set moslex11_0.set
129
130
131 ##### P-channel DIBL Test : Returns Vt with 0.1 and 3 volts Vd
    #####
132 ##### and a DIBL Parameter
    #####
133
134
135 go atlas
136
137
138 # set material models
139 models cvt srh print
140 contact name=gate n.poly
141 interface qf=3e10
142
143
144 # get initial solution
```

```
145
146 solve init
147
148 method newton trap maxtraps=8 autonr itlimit=30
149 solve prev
150
151
152 # Bias the drain a bit...
153 solve vdrain=-0.025 vstep=-0.025 vfinal=-0.1 name=drain
154 # Ramp the gate
155 log outf=moslex11_1.log master
156 solve vgate=0 vstep=-0.1 vdrain=-0.1 vfinal=-1.5 \
157 name=gate compl=1.1e-7 cname=drain
158
159
160 # extract device parameters
161 extract init inf="moslex11_1.log"
162 extract name="pvt1" x.val from curve(abs(v."gate"),abs(i."drain")) where
    y.val=0.1e-6
163
164
165
166 # now open a dummy log file...
167 log off
168
169 # Now start again and ramp the drain to 3 volts...
170 solve init
171 # Bias the drain to 3 volts.....slowly at first....
172 solve vdrain=-0.025 vstep=-0.025 vfinal=-0.1 name=drain
173 solve vdrain=-0.25 vstep=-0.25 vfinal=-3 name=drain
174
175 # Ramp the gate again with another opened logfile...
176 log outf=moslex11_2.log master
177 solve vgate=0 vstep=-0.1 vdrain=-3 vfinal=-1.5 name=gate \
178 compl=1.1e-7 cname=drain
179
180
181 # extract the next device parameter wuth the drain now at 3 volts....
182 extract init inf="moslex11_2.log"
183 extract name="pvt2" x.val from curve(abs(v."gate"),abs(i."drain")) where
    y.val=0.1e-6
184
185
186
```

```
187 # Calculate a DIBL parameter....in V/V
188 extract name="pdibl" ("$pvt1"-">$pvt2")/(3.0-0.1)
189
190 tonyplot -overlay moslex11_1.log moslex11_2.log -set moslex11_log.set
191
192 quit
```

1.1.12. moslex12.in: PMOS: Body Effect Extraction

Requires: SSUPREM4/SPISCES

Basic MOS ATHENA to ATLAS interface example simulating two Id/Vgs curves at different substrate biases and extracting the body effect (gamma) parameter. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and ATLAS
- simple Id/Vgs curve generation with Vbs=0.0V
- ramp of drain voltage
- simple Id/Vgs curve generation with Vbs=1.0V
- parameter extraction for body effect

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

In ATLAS the whole example is very similar in syntax to the DIBL parameter extraction example described previously in this section. The difference is that instead of different drain biases different substrate biases are used,

Two threshold voltages are measured using the extract syntax described in the DIBL extraction example. The body effect parameter is derived from the threshold voltages using the standard formula assuming 0.6V for phi.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

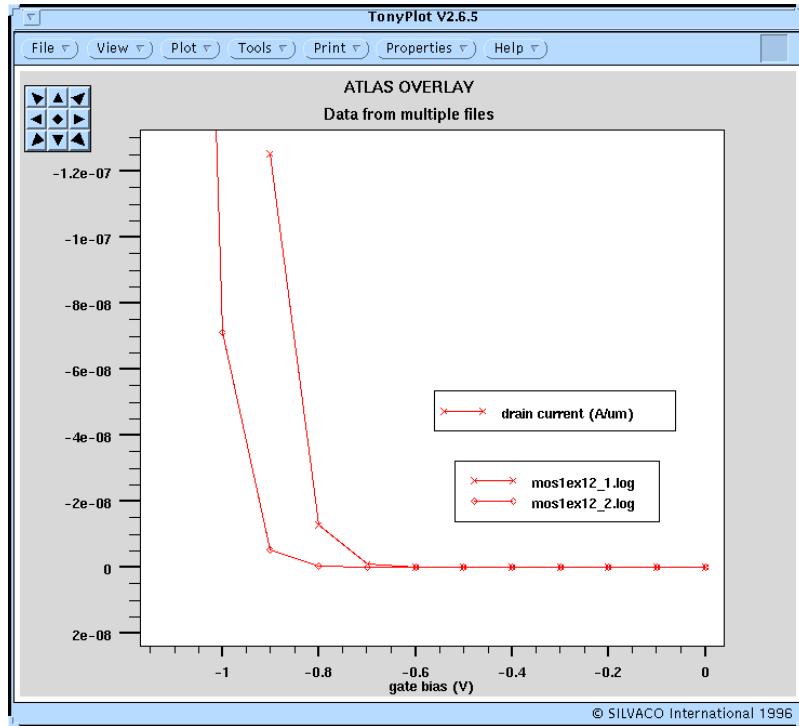


Figure 1.17: Body effect showing bulk voltage dependence of V_t for a PMOSFET

Input File mos1/mos1ex12.in:

```

1  # This is a simple Input File representing a Process flow and a device
2  # text. All lines begining with a '#' sign may be treated as directive
3  # comments.....
4
5  # Start the Athena Process simulator running...
6  go athena
7  #
8  # Set up a mesh suitable for a single MOSFET device....
9  line x loc=0 spac=0.1
10 line x loc=0.35 spac=0.02
11 line x loc=0.5 spac=0.1
12 #
13 line y loc=0.00 spac=0.005
14 line y loc=0.3 spac=0.015
15 line y loc=0.5 spac=0.02
16 line y loc=2 spac=0.2
17 line y loc=5 spac=1
18 #
19 # Start off by defining silicon with 1e14 phos doping...
20 # Decrease the following space.mult parameter for a denser
21 # mesh and more accuracy...

```

```
22 init orientation=100 c.phos=1e14 space.mult=2
23 #
24 #pwell formation including masking off of the nwell
25 #
26 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
27 #
28 etch oxide thick=0.02
29 #
30 #N-well Implant
31 implant amorphous phos dose=1e13 energy=100 pears
32 #
33 diffus temp=950 time=100 weto2 hcl=3
34 #
35 #N-well implant amorphous not shown -
36 #
37 # welldrive
38 diffus time=220 temp=1200 nitro press=1
39 #
40 etch oxide all
41 #
42 #sacrificial "cleaning" oxide
43 diffus time=20 temp=1000 dryo2 press=1 hcl=3
44 #
45 etch oxide all
46 #
47 #gate oxide grown here:-
48 set partial_press=1.0
49 diffus time=10 temp=800 nitrogen hcl=3
50 diffus time=2 temp=900 dryo2 press=$partial_press
51 diffus time=11 temp=900 dryo2 press=$partial_press hcl=3
52 diffus time=10 temp=900 nitrogen hcl=3
53 diffus time=10 temp=800 t.final=800 nit hcl=3
54 #
55 # Extract a design parameter.....
56 extract name="gateox" thickness oxide mat.occno=1 x.val=0.005
57 #
58 #vt adjust implant amorphous
59 implant amorphous bf2 dose=1.0e12 energy=25 pearson
60 #
61 depo poly thick=0.250 div=3
62 #
63 etch poly left p1.x=0.35
64 #
```

```
65 # Relax the mesh below the 0.5um plane, for speed....
66 relax y.min=0.5
67 #
68 method fermi compress
69 diffuse time=5 temp=900 weto2 press=0.8
70 #
71 # PLDD implant amorphous
72 implant amorphous bf2 dose=5e13 energy=40 pearson
73 #
74 # This is a good way of defining the spacer.....define a variable
75 # first with the 'set' command....
76 set spacer=0.15
77 depo oxide thick=$"spacer" divisions=5
78 etch oxide dry thick=$"spacer"+0.005
79 #
80 # P++ Implant
81 implant amorphous bf2 dose=1.50e15 energy=45 pearson
82 #
83 # Final anneal.
84 method fermi compress
85 diffuse time=5 temp=900 nitro press=1.0
86 #
87
88
89
90
91 # Extract other design parameters...
92 # extract final S/D Xj...
93 extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
94 # extract the long chan Vt...
95 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
96 # extract a curve of conductance versus bias....
97 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
98 extract done name="sheet cond v bias" curve(bias,ldn.conduct material="Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
99 # extract the P++ regions sheet resistance...
100 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.05 region.occno=1
101 # extract the sheet rho under the spacer, of the LDD region...
102 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.3 region.occno=1
103 # extract the surface conc under the channel....
```

```
104 extract name="pchan surf conc" surf.conc impurity="Net Doping" materi-
    al="Silicon" mat.occcno=1 x.val=0.45
105 # Etch contact cuts and place the aluminium where electrodes are re-
    quired.....
106 etch oxide left p1.x=0.15
107 deposit alumin thick=0.03 div=2
108 etch alumin right p1.x=0.16
109
110
111 # mirror the structure.....
112 structure mirror right
113
114
115
116 # Name the electrodes...
117 electrode name=gate x=0.5
118 electrode name=source x=0
119 electrode name=drain x=0.9
120 electrode name=substrate backside
121
122
123 # output the structure
124 structure outfile=moslex12_0.str
125
126 # plot it
127 tonyplot moslex12_0.str -set moslex12_0.set
128
129
130 ##### Body Effect Test : Returns P-channel Gamma #####
131 go atlas
132
133
134 # set material models
135 models cvt srh print
136
137 # Define the worksunction and the Qss....
138 contact name=gate n.poly
139 interface qf=3e10
140
141
142 # get initial solution
143 solve init
144 method newton
145 solve prev
```

```
146
147
148 # Bias the drain a bit...
149 solve vdrain=-0.025 vstep=-0.025 vfinal=-0.1 name=drain
150 # Ramp the gate
151 log outf=moslex12_1.log master
152 solve vgate=0 vstep=-0.1 vdrain=-0.1 vfinal=-2 name=gate \
153         compl=1.0e-7 cname=drain
154
155
156 # extract device parameters
157 extract init inf="moslex12_1.log"
158 extract name="pvt1" x.val from curve(abs(v."gate"),abs(i."drain")) where
    y.val=0.1e-6
159
160
161
162 # now open a dummy log file...
163 log off
164
165 # Now start again but with a substrate back-bias of a volt....
166 solve init
167 # Bias the substrate to 1 volt.....
168 solve vdrain=-0.05 vstep=-0.05 vfinal=-0.1 name=drain
169 solve vdrain=-0.1 vsubstrate=0.25 vstep=0.25 vfinal=1 name=substrate
170
171 # Ramp the gate again with another opened logfile...
172 log outf=moslex12_2.log master
173 solve vgate=0 vstep=-0.1 vdrain=-0.1 vsubstrate=1 \
174         vfinal=-2 name=gate compl=1.0e-7 cname=drain
175
176
177 # extract the next device parameter....
178 extract init inf="moslex12_2.log"
179 extract name="pvt2" x.val from curve(abs(v."gate"),abs(i."drain")) where
    y.val=0.1e-6
180
181
182
183 # Calculate the parameter Gamma .... with phi = 0.6 eV....
184 extract name="pgamma" ($"pvt2"-$"pvt1")/((sqrt(1+0.6))-sqrt(0.6))
185
186 tonyplot -overlay moslex12_1.log moslex12_2.log -set moslex12_log.set
```

187**188 quit**

1.1.13. mos1ex13.in: PMOS: Substrate and Gate Current Extraction

Requires: SSUPREM4/DEVEDIT/SPISCES

MOS ATHENA/DEVEDIT/ATLAS interface example simulating substrate and gate current versus gate bias using energy balance and impact ionization models. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and DEVEDIT
- remeshing using DEVEDIT
- autointerface between DEVEDIT and ATLAS
- solution for a V_{gs} ramp with V_{ds}=-3.3V
- parameter extraction for maximum gate and substrate currents

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

The grid requirements for ATLAS simulation of impact ionization effects are more stringent than for the low electric field cases described earlier. DEVEDIT is used to remesh the ATHENA structure before proceeding to ATLAS. DEVEDIT has two modes. The graphical mode allows users to draw and interactively edit regions and impurities. The batch mode used here executes structure and mesh commands similar to these. The syntax used by DevEdit is described in the DEVEDIT manual. It can be constructed from the DeckBuild command menu or most commonly mesh edits made during a graphical session can be saved as a ‘command file’ from the **Save** menu in DEVEDIT.

The `imp.refine` commands specify regrids on impurities. Here, a regrid on net doping is done. The `constr.mesh` command defines the base mesh. The `refine` commands specify mesh refinements inside boxes specified by the coordinates in each statement.

The ATLAS simulation contains similar syntax to the simple examples described earlier in this section. The solution of the energy balance equations for holes is specified by the parameter, `hcte.ho`. The parameter, `hh`, specifies the hot carrier injection model, which gives the gate current. The equivalent `hcte.el` and `hei` exist for holes but are not required in PMOS simulation.

The impact ionization model is selected on the `impact` statement. The parameter, `lrel.ho`, sets the relaxation time for holes in this model. Although the `hei` model is directly responsible for the gate current. There is no ‘special’ model required to simulate substrate current. Running this sweep of gate voltage with a high drain bias and including impact ionization and energy balance supplies all the necessary physics. The substrate current can simply be plotted from the log file in a similar manner to drain current. No special extraction of substrate current is needed.

The `extract` statements used in this run extract the peak value and position of the substrate and gate currents. The value of the peak current is measured first. Then this result is used in a current search to find the gate voltage where this current is measured.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

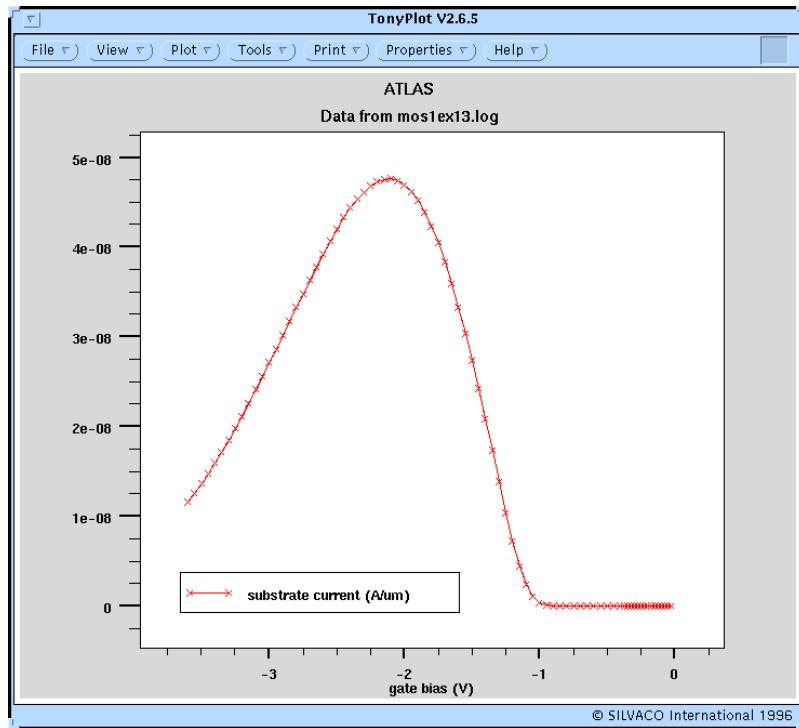


Figure 1.18: NMOS substrate current curve using energy balance models

Input File mos1/mos1ex13.in:

```

1  # This is a simple Input File representing a Process flow and a device
2  # test. All lines begining with a '#' sign may be treated as directive
3  # comments.....  

4  

5  

6  # Start the Athena Process simulator running...
7  go athena
8  #
9  # Set up a mesh suitable for a single MOSFET device....  

10 line x loc=0 spac=0.01
11 line x loc=0.25 spac=0.01
12 line x loc=0.5 spac=0.1
13 #
14 line y loc=0.00 spac=0.005
15 line y loc=0.3 spac=0.015
16 line y loc=0.5 spac=0.02
17 line y loc=2 spac=0.2
18 line y loc=5 spac=1
19 #
20 # Start off by defining silicon with 1e14 phos doping...
21 # Decrease the folowing space.mult parameter for a denser

```

```
22 # mesh and more accuracy...
23 init orientation=100 c.phos=1e14 space.mult=2
24 #
25 #pwell formation including masking off of the nwell
26 #
27 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
28 #
29 etch oxide thick=0.02
30 #
31 #N-well Implant
32 implant amorphous phos dose=2.9e13 energy=100 pears
33 #
34 diffus temp=950 time=100 weto2 hcl=3
35 #
36 #N-well implant amorphous not shown -
37 #
38 # welldrive
39 diffus time=220 temp=1200 nitro press=1
40 #
41 etch oxide all
42 #
43 #sacrificial "cleaning" oxide
44 diffus time=20 temp=1000 dryo2 press=1 hcl=3
45 #
46 etch oxide all
47 #
48 #gate oxide grown here:-
49 set partial_press=1.0
50 diffus time=10 temp=800 nitrogen hcl=3
51 diffus time=2 temp=900 dryo2 press=$partial_press
52 diffus time=13 temp=900 dryo2 press=$partial_press hcl=3
53 diffus time=10 temp=900 nitrogen hcl=3
54 diffus time=10 temp=800 t.final=800 nit hcl=3
55 #
56 #vt adjust implant amorphous
57 implant amorphous bf2 dose=2.30e12 energy=25 pearson
58 #
59 depo poly thick=0.250 div=3
60 #
61 etch poly left p1.x=0.25
62 #
63 # Relax the mesh below the 0.5um plane, for speed....
64 relax y.min=0.5
```

```
65 #
66 method fermi compress
67 diffuse time=5 temp=900 weto2 press=0.8
68 #
69 # PLDD implant amorphous
70 implant amorphous bf2 dose=2.0e14 energy=50 pearson
71 #
72 # This is a good way of defining the spacer.....define a variable
73 # first with the 'set' command....
74 set spacer=0.15
75 depo oxide thick="$spacer" divisions=5
76 etch oxide dry thick="$spacer"+0.005
77 #
78 # P++ Implant
79 implant amorphous bf2 dose=1.50e15 energy=60 pearson
80 #
81 #
82 # Final anneal.
83 method fermi compress
84 diffuse time=5 temp=900 nitro press=1.0
85 #
86
87
88
89
90 # Extract other design parameters...
91 # extract final S/D Xj...
92 extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
93 # extract the long chan Vt...
94 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
95 # extract a curve of conductance versus bias....
96 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
    bias.stop=2 x.val=0.45
97 extract done name="sheet cond v bias" curve(bias,ldn.conduct material=
    "Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
98 # extract the P++ regions sheet resistance...
99 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.05 region.occno=1
100 # extract the sheet rho under the spacer, of the LDD region...
101 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occno=1
    x.val=0.3 region.occno=1
102 # extract the surface conc under the channel....
103 extract name="pchan surf conc" surf.conc impurity="Net Doping" material=
    "Silicon" mat.occno=1 x.val=0.45
```

```
104 # Etch contact cuts and place the aluminium where electrodes are re-
     quired.....
105 etch oxide left p1.x=0.15
106 deposit alumin thick=0.03 div=2
107 etch alumin right p1.x=0.16
108
109
110 # mirror the structure.....
111 structure mirror right
112
113
114
115 # Name the electrodes...
116 electrode name=gate x=0.5
117 electrode name=source x=0
118 electrode name=drain x=0.9
119 electrode name=substrate backside
120
121
122
123 go DevEdit
124
125 # Set Meshing Parameters
126 #
127 base.mesh height=1000000 width=1000000
128 #
129 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
     line.straightening=1 align.points when=automatic
130 #
131 imp.refine imp="NetDoping" sensitivity=1
132 imp.refine min.spacing=0.02
133 #
134 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
135 max.width=1 min.height=0.0001 min.width=0.0001
136 #
137 # Perform mesh operations
138 #
139 Mesh Mode=MeshBuild
140 refine mode=both x1=0.32 y1=0.22 x2=0.67 y2=0.28
141 refine mode=both x1=0.4 y1=0.22 x2=0.60 y2=0.26
142 refine mode=both x1=0.74 y1=0.32 x2=1.0 y2=0.48
143
144
145 # output the structure
```

```
146 structure outfile=moslex13_0.str
147
148 # plot it
149 tonyplot moslex13_0.str -set moslex13_0.set
150
151
152
153
154
155 go atlas
156
157
158 # add workfunction and interface charge
159 contact name=gate n.polysilicon
160 interf qf=1E10
161
162 # select MOS models
163 models cvt consrh hcte.ho hhi nearflg
164
165 impact selb length.rel lrel.ho=0.025
166
167 material taurel.ho=0.25e-12 taumob.ho=0.25e-12
168
169 options verbose
170 solve init
171
172 method gummel block newton trap temp.tol=1.e-4
173
174 solve
175 solve vdrain=-0.05
176 solve vdrain=-0.1
177 solve vdrain=-0.2 vstep=-0.2 vfinal=-3.6 name=drain
178
179
180 log outf=moslex13.log master
181
182
183 solve vgate=-0.025 vstep=-0.025 vfinal=-0.4 name=gate
184
185 method newton trap temp.tol=1.e-4
186
187 solve vgate=-0.45 vstep=-0.05 vfinal=-3.6 name=gate
188
```

```

189
190 tonyplot moslex13.log -set moslex13_log.set
191
192 # Extract Substrate current peak value parameter....
193 extract init inf="moslex13.log"
194 extract name="pmax_isub_vd3.6" max(curve(abs(v."gate"),abs(i."substrate")))
195
196 #Extract gate voltage at the peak substrate current
197 extract init inf="moslex13.log"
198 extract name="pVgate_at_isubmax_vd3.6" x.val from
      curve(abs(v."gate"),abs(i."substrate")) where y.val=$"pmax_isub_vd3.6"
199
200
201 # Extract Gate current peak value parameter....
202 extract init inf="moslex13.log"
203 extract name="pmax_igate_vd3.6"
      (max(curve(abs(v."gate"),abs(i."gate"))))
204
205
206 # Extract gate voltage at the peak gate current point....
207 extract init inf="moslex13.log"
208 extract name="pVgate_at_igate_vd3.6" x.val from
      curve(abs(v."gate"),abs(i."gate")) where y.val=$"pmax_igate_vd3.6"
209
210 quit

```

1.1.14. moslex14.in: PMOS: Breakdown Voltage Extraction

Requires: SSUPREM4/DEVEDIT/SPISCES

ATHENA/DEVEDIT/ATLAS interface example simulating the breakdown voltage of an PMOS transistor. This example demonstrates:

- process simulation of a MOS transistor in ATHENA
- process parameter extraction (eg. oxide thicknesses)
- autointerface between ATHENA and DEVEDIT
- remeshing using DEVEDIT
- autointerface between DEVEDIT and ATLAS
- solution for a Vds ramp with Vgs=0.0V to get breakdown

The process simulation, process parameter extraction and electrode definition for this example are exactly as described in the first example in this section.

The grid requirements for ATLAS simulation of impact ionization effects are more stringent than for the low electric field cases described earlier. DEVEDIT is used to remesh the ATHENA structure before proceeding to ATLAS. The remeshing commands are described in the previous example in this section.

The ATLAS simulation contains similar syntax to the simpler examples described earlier in this section. The models, contact and interface parameters are the same, except that the concentration dependent SRH model is used. This provides a more accurate simulation of the pre-breakdown leakage current. The Selberherr impact ionization model is also selected.

On the method statement two parameters are chosen to restrict the use of the current convergence criteria used in ATLAS. Since the pre-breakdown leakage current is very low it is necessary to tighten the tolerances on current convergence. The parameter setting, `method climit=1e-4`, is also recommended in cases where the mesh is not as tight as the one used here.

The sequence of solve statements shows a ramp in drain voltage. At first small steps are taken, but the main simulation is done in 0.5V steps. A compliance limit of 5.0e-8A/um is set on the drain. Compliance limits are useful in breakdown simulations to stop the simulation once the breakdown point is reached.

The value used here might seem rather low compared to typical values used in measurements. This is simply an issue of CPU time. Running the simulation up into microamp or milliamp ranges is possible, however the extra information gained is usually not worth the CPU time spent. Once the voltage exceeds the breakdown voltage no solutions will be possible. ATLAS will cut the voltage step and try again. It does this four times resulting in a minimum step of $(0.5)^4$ or 0.0625V. This is sufficient to resolve most breakdown voltages. It is possible for users to ramp using smaller voltage steps, to use current boundary conditions or curve tracing to further trace the IV curve to higher values of current. Usually, this is not needed. Much extra CPU time might be required and yet the value of breakdown voltage remains the same to within the accuracy expected by simulation. Examples demonstrating snapback and curve tracing are included in other sections.

The `extract` syntax used to measure the breakdown voltage is of the current search type. This is preferred over the simple `max(v. "drain")` syntax that could be used as it gives more consistent results.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

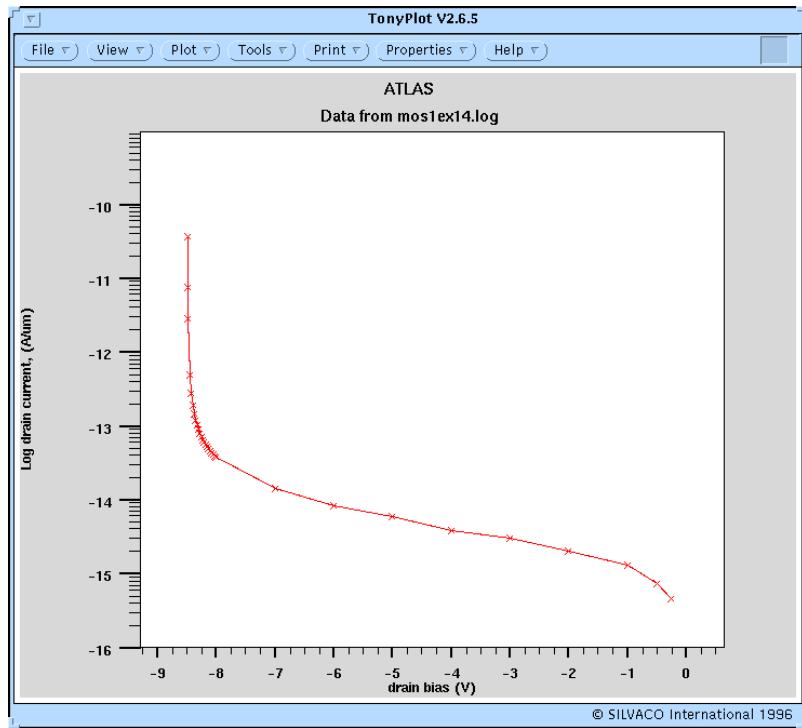


Figure 1.19: PMOS breakdown simulation. The clear breakdown point on the curve indicates a primarily avalanche breakdown.

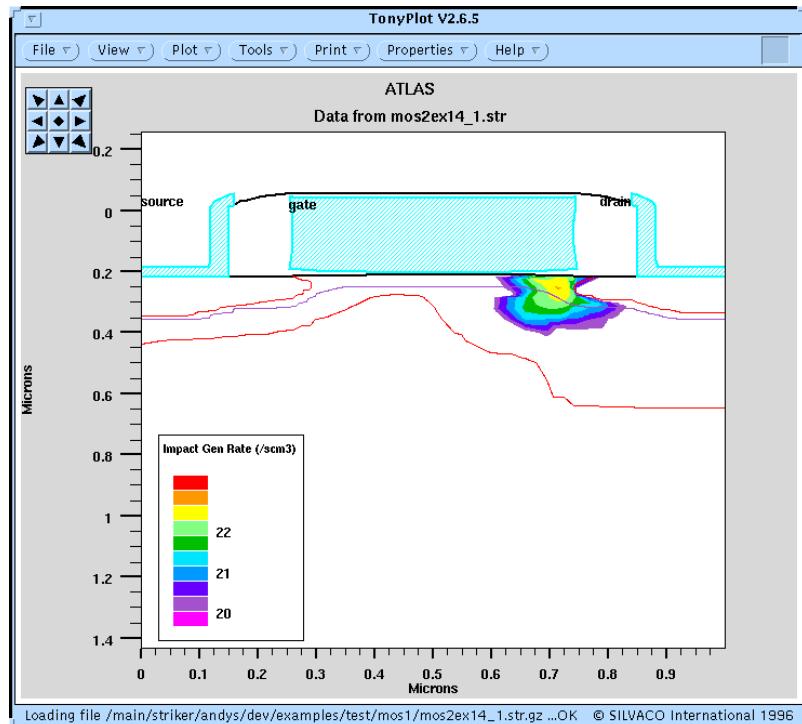


Figure 1.20: Contours of impact ionization in the POSFET at the BV point. The depletion edges around the junctions are also shown.

Input File mos1/mos1ex14.in:

```
1 go athena
2 # This is a simple Input File representing a Process flow and a device
3 # test. All lines begining with a '#' sign may be treated as directive
4 # comments.....
5
6 # Start the Athena Process simulator running...
7 #
8 # Set up a mesh suitable for a single MOSFET device....
9 line x loc=0 spac=0.01
10 line x loc=0.25 spac=0.01
11 line x loc=0.5 spac=0.1
12 #
13 line y loc=0.00 spac=0.005
14 line y loc=0.3 spac=0.015
15 line y loc=0.5 spac=0.02
16 line y loc=2 spac=0.2
17 line y loc=5 spac=1
18 #
19 # Start off by defining silicon with 1e14 phos doping...
20 # Decrease the following space.mult parameter for a denser
21 # mesh and more accuracy...
22 init orientation=100 c.phos=1e14 space.mult=2
23 #
24 #pwell formation including masking off of the nwell
25 #
26 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
27 #
28 etch oxide thick=0.02
29 #
30 #N-well Implant
31 implant amorphous phos dose=2.9e13 energy=100 pears
32 #
33 diffus temp=950 time=100 weto2 hcl=3
34 #
35 #N-well implant amorphous not shown -
36 #
37 # welldrive
38 diffus time=220 temp=1200 nitro press=1
39 #
40 etch oxide all
41 #
42 #sacrificial "cleaning" oxide
```

```
43 diffus time=20 temp=1000 dryo2 press=1 hcl=3
44 #
45 etch oxide all
46 #
47 #gate oxide grown here:-
48 set partial_press=1.0
49 diffus time=10 temp=800 nitrogen hcl=3
50 diffus time=2 temp=900 dryo2 press=$partial_press
51 diffus time=13 temp=900 dryo2 press=$partial_press hcl=3
52 diffus time=10 temp=900 nitrogen hcl=3
53 diffus time=10 temp=800 t.final=800 nit hcl=3
54 #
55 #vt adjust implant amorphous
56 implant amorphous bf2 dose=2.30e12 energy=25 pearson
57 #
58 depo poly thick=0.250 div=3
59 #
60 etch poly left p1.x=0.25
61 #
62 # Relax the mesh below the 0.5um plane, for speed....
63 relax y.min=0.5
64 #
65 method fermi compress
66 diffuse time=5 temp=900 weto2 press=0.8
67 #
68 # PLDD implant amorphous
69 implant amorphous bf2 dose=2.0e14 energy=50 pearson
70 #
71 # This is a good way of defining the spacer.....define a variable
72 # first with the 'set' command....
73 set spacer=0.15
74 depo oxide thick="$spacer" divisions=5
75 etch oxide dry thick="$spacer"+0.005
76 #
77 # P++ Implant
78 implant amorphous bf2 dose=1.50e15 energy=60 pearson
79 #
80 #
81 # Final anneal.
82 method fermi compress
83 diffuse time=5 temp=900 nitro press=1.0
84 #
85
```

```
86
87
88
89 # Extract other design parameters...
90 # extract final S/D Xj...
91 extract name="pxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
92 # extract the long chan Vt...
93 extract name="pldvt" ldvt ptype vb=0.0 qss=1e10 x.val=0.49
94 # extract a curve of conductance versus bias....
95 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
     bias.stop=2 x.val=0.45
96 extract done name="sheet cond v bias" curve(bias,ldn.conduct material-
     "Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
97 # extract the P++ regions sheet resistance...
98 extract name="p++ sheet rho" sheet.res material="Silicon" mat.occno=1
     x.val=0.05 region.occno=1
99 # extract the sheet rho under the spacer, of the LDD region...
100 extract name="pldd sheet rho" sheet.res material="Silicon" mat.occno=1
      x.val=0.3 region.occno=1
101 # extract the surface conc under the channel....
102 extract name="pchan surf conc" surf.conc impurity="Net Doping" material-
     "Silicon" mat.occno=1 x.val=0.45
103 # Etch contact cuts and place the aluminium where electrodes are re-
     quired.....
104 etch oxide left p1.x=0.15
105 deposit alumin thick=0.03 div=2
106 etch alumin right p1.x=0.16
107
108
109 # mirror the structure....
110 structure mirror right
111
112
113
114 # Name the electrodes...
115 electrode name=gate x=0.5
116 electrode name=source x=0
117 electrode name=drain x=0.9
118 electrode name=substrate backside
119
120
121
122 go DevEdit
123
124
```

```
125
126 # Set Meshing Parameters
127 #
128 base.mesh height=1000000 width=1000000
129 #
130 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.points when=automatic
131 #
132 imp.refine imp="NetDoping" sensitivity=1
133 imp.refine min.spacing=0.02
134 #
135 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
136 max.width=1 min.height=0.0001 min.width=0.0001
137 #
138 # Perform mesh operations
139 #
140 Mesh Mode=MeshBuild
141 refine mode=both x1=0.32 y1=0.22 x2=0.67 y2=0.28
142 refine mode=both x1=0.4 y1=0.22 x2=0.60 y2=0.25
143 refine mode=both x1=0.74 y1=0.32 x2=1.0 y2=0.48
144
145
146
147
148
149 # output the structure
150 structure outfile=moslex14_0.str
151
152 # plot it
153 tonyplot moslex14_0.str -set moslex14_0.set
154
155
156
157
158
159 ##### P-channel Vbd Extraction test #####
160
161
162 go atlas
163
164 # add workfunction and interface charge
165 contact name=gate n.polysilicon
166 interf qf=1E10
```

```
167
168 # select MOS models
169 models cvt consrh print
170 impact selb
171
172 solve init
173
174 method newton trap ir.tol=1.e-25 ix.tol=1.e-25 climit=1e-4
175 solve
176 solve vdrain=-0.05
177 solve vdrain=-0.1
178
179 # Open log file to store the IV points in....
180 log      outf=moslex14.log
181
182 solve vdrain=-0.25
183 solve vdrain=-0.5
184
185 solve vdrain=-1 vstep=-1 vfinal=-8 name=drain
186 solve vdrain=-8.025 vstep=-0.025 vfinal=-15 name=drain compl=1e-11
      cname=drain
187 save outf=mos2ex14_1.str
188
189 # Extract the design parameter, Vbd
190 extract init inf="moslex14.log"
191 extract name="PVbd" x.val from curve(abs(v."drain"),abs(i."drain")) where
      y.val=1e-11
192
193 tonyplot moslex14.log -set moslex14_log.set
194
195 quit
```

1.1.15. moslex15.in: NMOS: Gate Length Scaling

Requires: SSUPREM4/SPISCES

ATHENA/ATLAS interface example similar to the first example in this section demonstrating the setting of gate length through parameter substitution.

In this example an NMOS transistors length is defined with a `set` statement around the poly etch stage in the simulation. The `set` statement defines a variable used in a subsequent `stretch` statement to define the half length of the transistor.

Importantly the variable, `$cd`, is also used to place the name of the drain electrode in the subsequent `electrode` statement. Thus, a user does not have too much difficulty in defining the drains' position.

Note the use of the `right` statement in the `stretch` command. This makes sure that the coordinate system of the stretched device remains unchanged from the original making sure that the left hand side of the structure is in the same place as before. Both `right/left` flags are available.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

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2.1. MOS2: Advanced MOS Application Examples

2.1.1. mos2ex01.in: Circuit Analysis of NMOS Inverters

Requires: SPICES/MIXEDMODE

This example uses the MIXEDMODE module in ATLAS to simulate the circuit performance of two NMOS inverters in series. The first inverter is simulated using ATLAS, the second inverter using SPICE level 1 models. This simulation shows how to:

- create an NMOS structure using ATLAS syntax
- calculate the initial DC state in circuit mode
- simulate the DC transfer curve of the inverters
- simulate the transient switching curve of the inverters

The input file consists of four separate runs, each, starting with the statement, `go atlas`. The first one uses the ATLAS syntax to construct an NMOS transistor. The mesh, regions and electrodes are specified as coordinates in the syntax. It is compulsory to use electrode names (and not just numbers) when the structure is used in MIXEDMODE. The doping distribution for the device is constructed from several Gaussian and uniform analytical functions. The final structure is saved for later use.

The second run calculates the initial operating point of the circuit. The syntax for this run is split into two parts. The first is a SPICE-like circuit description and control cards. This part is bounded by `.begin` and `.end`. The second is device parameter syntax. The circuit netlist is written using standard SPICE syntax. This example has two inverters composed on an NMOS transistor and resistor connected in series feeding into a capacitor.

The two NMOS transistors are defined in different ways. The first NMOS transistor labeled `an` is to be simulated in ATLAS. The syntax specifies the structure file name from the previous run and also connects up the circuit nodes to electrode names. The other NMOS transistor labeled `mn` is simulated using SPICE level 1 model labeled `simple`.

After the `.end` statement the device parameter syntax is given. This sets the models, material and contact parameters for the ATLAS device.

The second run solves a single DC operating point as the initial guess to the third run. The third run uses the command `.dc` to set a DC ramp of the input voltage '`vin`' from zero to 5.0V in 0.25V steps. The currents and voltages for each node are stored in the file specified in the `.log` statement.

The final run uses the `.tran` statement combined with a time dependent definition of '`vin`' using the `PULSE` parameter to set up a switching transient. The `PULSE` syntax specifies that the pulse of '`vin`' has a peak value of 5.0V a rise and fall time of 50ps and a time at peak value of 1ns. On the `.tran` statement, `1ps` specifies the initial timestep only. All other timesteps are automatically calculated by ATLAS. This differs from the `.tran` card in standalone SPICE programs. The maximum simulation time is set to 3ns.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

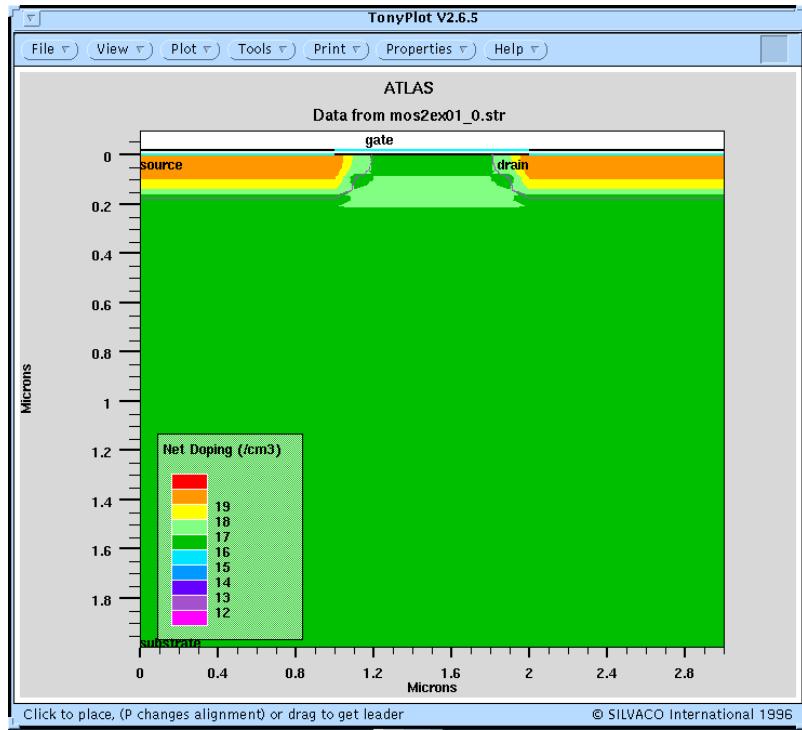


Figure 2.1: Doping and Geometry on an NMOSFET defined using ATLAS syntax

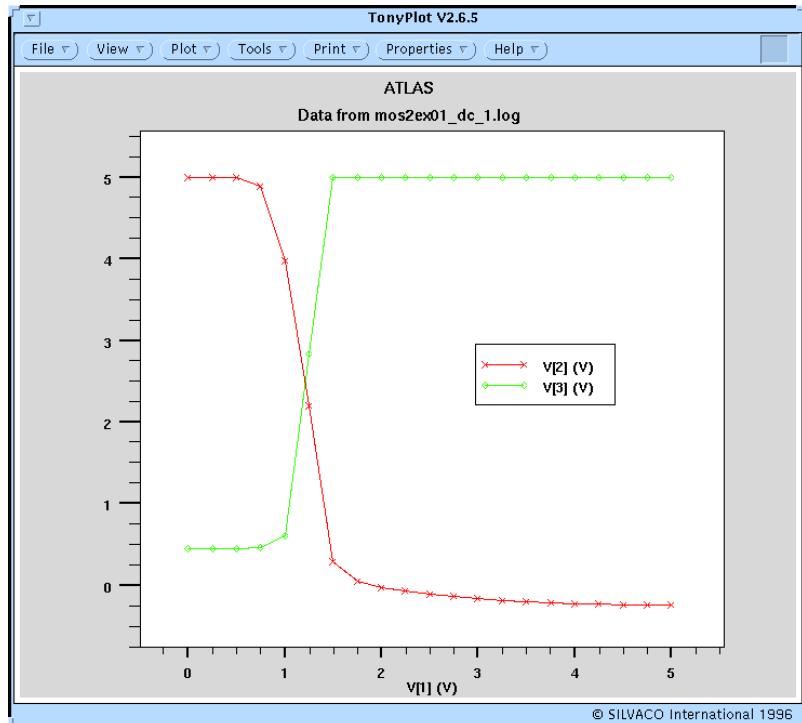


Figure 2.2: DC Output Voltages from first stage (o) and second stage (x) inverters in a chain using MIXEDMODE simulation

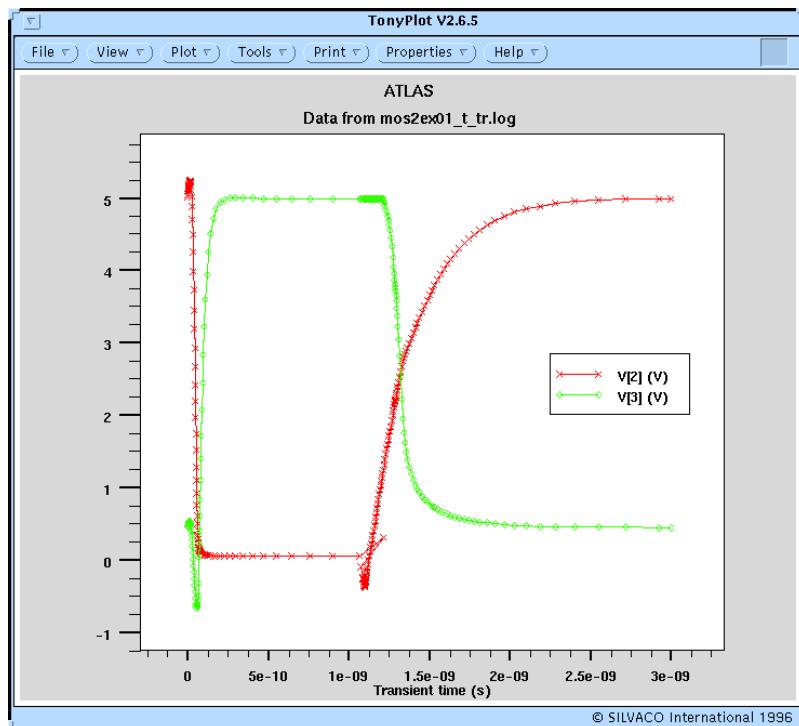


Figure 2.3: Output Voltages from first stage (o) and second stage (x) inverters during a transient switching simulation in MIXEDMODE

Input File mos2/mos2ex01.in:

```

1 go atlas
2
3 #      SILVACO International
4
5 #      N-MOSFET structure
6 #
7 #
8 #      For MIXEDMODE master.out should be specified
9 #
10
11 mesh      outf=mos2ex01_0.str master.out
12 #
13 x.m      l=0.0  spacing=0.1
14 x.m      l=3.0  spacing=0.1
15 #
16 y.m      l=-0.02 spacing=0.01
17 y.m      l=0.0   spacing=0.01
18 y.m      l=0.7   spacing=0.06
19 y.m      l=2.0   spacing=0.2
20 #
21 #      Regions

```

```
22 #
23 region num=1 y.min=0 silicon
24 region num=2 y.max=0 oxide
25 #
26 #   Electrodes. For MIXEDMODE names must be specified
27 #
28 elec num=1 x.min=1 length=1.0 name=gate
29 elec num=2 left length=1.0 y.min=0 y.max=0 name=source
30 elec num=3 right length=1.0 y.min=0 y.max=0 name=drain
31 elec num=4 substrate name=substrate
32 #
33 #   Doping profiles
34 #
35 doping uniform conc=1e16 p.type
36 doping gauss conc=1e17 p.type char=0.2 peak=0.15
37 doping gauss conc=1e20 n.type junc=0.17 x.right=1.0 ratio=0.7
38 doping gauss conc=1e20 n.type junc=0.17 x.left=2.0 ratio=0.7
39
40 tonyplot mos2ex01_0.str -set mos2ex01_0.set
41 #
42
43 go atlas
44 .begin
45 #
46 #   NMOS inverters - DC point simulation
47 #   SILVACO International
48 #
49 #   Circuit description
50 #
51 vin 1 0 0
52 an 2=drain 1=gate 0=source 0=substrate infile=mos2ex01_0.str width=15.
53 mn 3 2 0 0 simple L=2.0u W=5u
54 r1 2 4 10k
55 r2 3 4 10k
56 vcc 4 0 5.
57 c1 3 0 3ff
58 #
59 #   End of circuit description
60 #
61 .model simple nmos ( tox=0.02e-6 vt0=0.9 )
62 #
63 .numeric vchange=1.
64 .options print m2ln noshift
```

```
65 #
66 .save outfile=nmos
67 .end
68 #
69 # Define physical models for ATLAS device
70 #
71 contact device=an name=gate n.poly
72 model device=an reg=1 conmob fldmob bgn
73
74 go atlas
75 .begin
76 #
77 #      NMOS inverters - DC curve simulation
78
79 #
80 #      Circuit description
81 #
82 vin 1 0 0
83 an 2=drain 1=gate 0=source 0=substrate infile=mos2ex01_0.str width=15.
84 mn 3 2 0 0 simple L=2.0u W=5u
85 r1 2 4 10k
86 r2 3 4 10k
87 vcc 4 0 5.
88 c1 3 0 3ff
89 #
90 #      End of circuit description
91 #
92 .model simple nmos ( tox=0.02e-6 vt0=0.9 )
93 #
94 .options print fulln noshift
95 #
96 .load infile=nmos
97 .log outfile=mos2ex01
98 .dc vin 0. 5. 0.25
99 #
100 .end
101 #
102 # Define physical models for ATLAS device
103 #
104 contact device=an name=gate n.poly
105 model device=an reg=1 conmob fldmob bgn
106
107 go atlas
```

```
108
109 tonyplot mos2ex01_dc_1.log -set mos2ex01_dc_1.set
110
111 go atlas
112 .begin
113 #
114 #      NMOS inverters - transient simulation
115 #
116 #      Circuit description
117 #
118 vin 1 0 0. PULSE 0 5 0 50ps 50ps 1000ps 10
119 an 2=drain 1=gate 0=source 0=substrate infile=mos2ex01_0.str width=15.
120 mn 3 2 0 0 simple L=2.0u W=5u
121 r1 2 4 10k
122 r2 3 4 10k
123 vcc 4 0 5.
124 c1 3 0 3ff
125 #
126 #      End of circuit description
127 #
128 .model simple nmos ( tox=.02e-6 vt0=0.9 )
129 #
130 .numeric lte=0.05
131 .options print noshift
132 #
133 .load infile=nmos
134 .log outfile=mos2ex01_t
135 #
136 .tran 1ps 3ns
137 #
138 .end
139 #
140 #      ATLAS device models and parameters
141 #
142 contact device=an name=gate n.poly
143 model device=an reg=1 conmob fldmob bgn
144
145 go atlas
146 tonyplot mos2ex01_t_tr.log -set mos2ex01_tr.set
147 quit
```

2.1.2. mos2ex02.in: Hot Electron Reliability

Requires: SPISCES/C-INTERPRETER

This is a demonstration of the hot carrier reliability feature of ATLAS. A PMOS transistor is stressed at high voltages and a threshold voltage shift observed. The simulation shows:

- formation of PMOS transistor using ATLAS syntax
- Id/Vgs test
- high voltage stress for 1000 seconds
- Id/Vgs tests of devices at various stress times.

The example file consists of five separate ATLAS runs each starting with the statement, `go atlas`. The first run uses the ATLAS syntax to construct the geometry, mesh and doping of a PMOS transistor. The doping is specified using Gaussian functions. The mesh file saved by this run is loaded into the next run.

The second ATLAS run sets commands to perform an Id/Vgs simulation to observe the threshold voltage and gain. A more complete description of extracting PMOS threshold can be found in the MOS examples section.

The device degradation modeling is done in the third run. First the structure is loaded and the correct workfunction and interface fixed charge are set. On the `models` statement the standard mobility and recombination models are specified. In addition the parameters, `hei`, `devdeg.e` are set. The `hei` parameter turns on the hot electron injection model for gate current. The `devdeg.e` parameter sees that the gate current is used to calculate device degradation. The degradation parameter is used to specify the interface state density and the electron trapping cross section, `sigmae`. The density of interface states as a function of position is defined here using a C-Interpreter routine. The external file `mos2ex02_devdeg.nta` is used in this example. This file will be copied to your current working directory if you press 'Load example'. This file contains a C language description of the density of acceptor-like traps at the oxide/silicon interface. Use of the C-Interpreter allows complete flexibility in specifying the position of the traps.

The stressing conditions are $V_{ds} = -6.0V$ and $V_{gs} = -1.5V$. The device is biased to these voltages in DC mode. Then ATLAS is switched to a transient solution. Since the time of this transient is very long compared with the transit time of carriers a faster transient solution method can be selected using `method quasistatic`.

The transient simulation is set to run for 1000s. At various intervals, data is saved to solution files whose prefix is set to `mosex02.str`. The statement, `output devdeg`, is required to save the interface trap occupancy to these solution files. These files will be the initial starting points of the subsequent Id/Vgs runs.

The fourth and fifth runs are just repetitions of the second one. They perform the Id/Vgs test to observe threshold voltage and gain. However, the important difference is that the file loaded in the `mesh` statement is the output files saved during the transient stress.

The Id/Vgs curves from the second, fourth and fifth runs can be overlaid in TONYPLOT to show the threshold voltage shift caused by the hot carriers trapped at the interface.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

2.1.3. mos2ex03.in: Gate Turn-on Transient

Requires: SSUPREM4/SPISCES

This example demonstrates the transient simulation of a MOS transistor including:

- formation of a MOS structure in ATHENA
- interface from ATHENA to ATLAS

- specification of external RC elements to make an NMOS inverter
- transient simulation of gate turn-on

The process simulation follows a standard LDD MOS process. Further description of the MOS process simulation and the ATHENA to ATLAS interface can be found in the description of the MOS examples.

In ATLAS the first task is setting the gate workfunction using the `contact` statement and interface charge using the `interface` statement. The models used for this simulation are selected using the macro `mos`. This model set uses the CVT mobility model and SRH recombination. A two-carrier solution is also specified on the `models` statement. Two-carrier solutions are necessary for transients and when external passive elements are used irrespective of the type of device being simulated.

The second `contact` statement is used to set the external resistance and capacitance on the drain electrode. A resistance of `1.0e5 ohms.um` is used to correspond to a load resistor in a memory cell. A capacitance of `0.5pF/um` is specified to emulate the gates and interconnect the drain must drive. These external elements emulate the formation of an NMOS inverter in S-PISCES. This contrasts with the previously described example using `MIXEDMODE`.

The initial state of the device is set at `5.0V` on the drain. The local initial guess method is used to allow large change in the drain bias in a single step. This local method will only converge if the change in current caused by the voltage step is small. Since the gate voltage is zero this is true here.

The `solve` statement for the transient simulation contains the final gate voltage, the ramp time of the gate voltage, the initial timestep and the final simulation time. Only the initial timestep is specified in the `solve` statement. All other timestep sizes are calculated by ATLAS based on the local truncation error in the solution.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

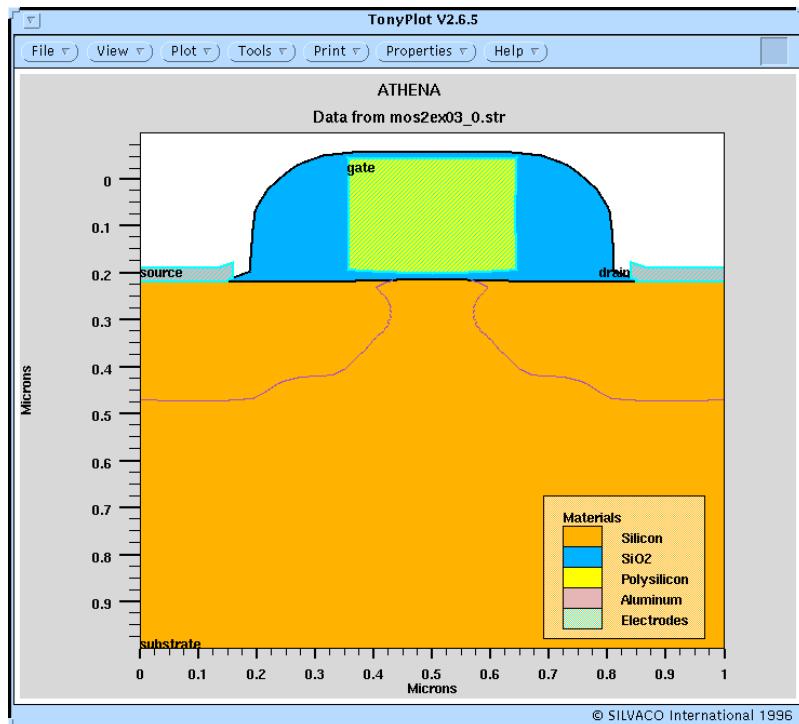


Figure 2.4: MOSFET Geometry and Junctions

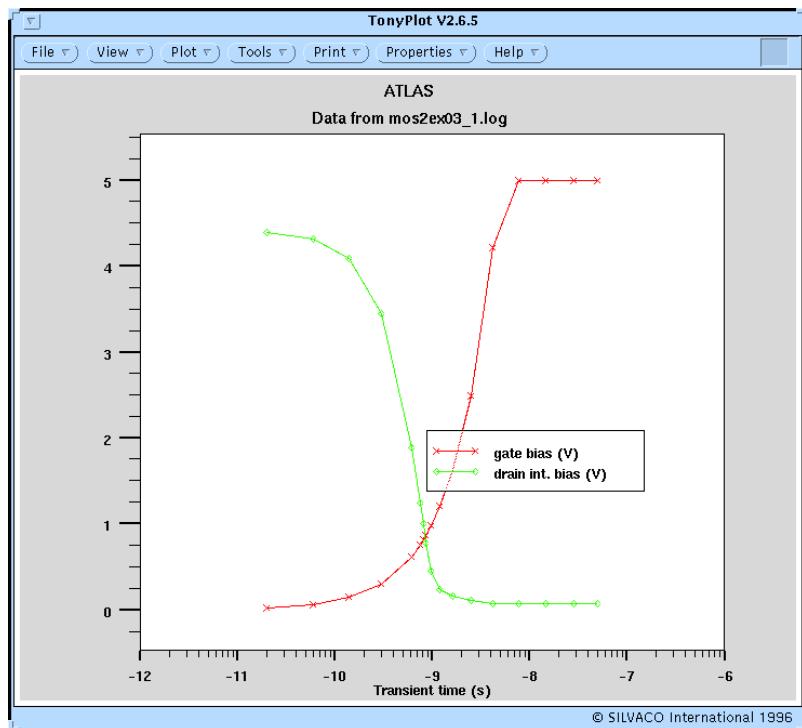


Figure 2.5: Gate and Drain Voltages during switching transient

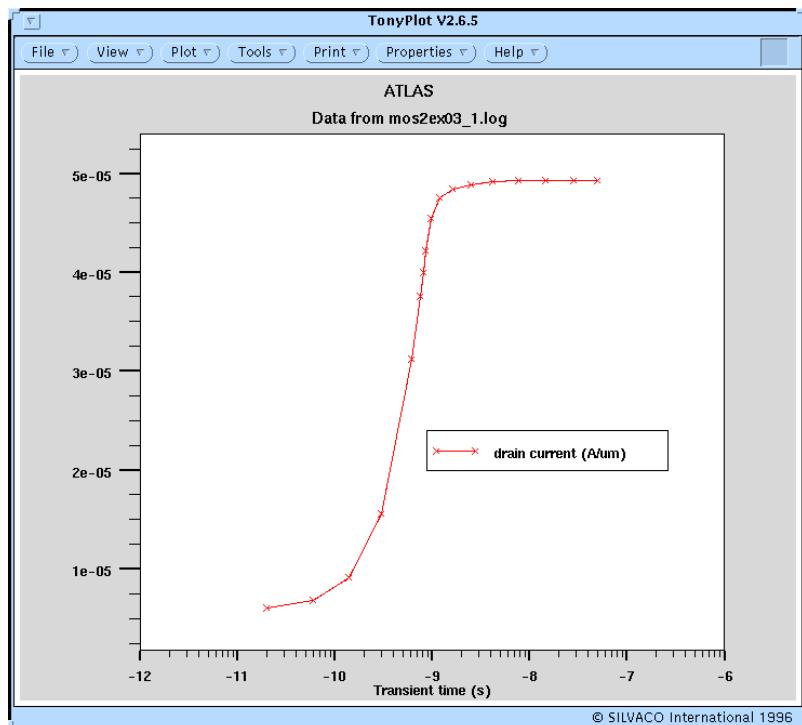


Figure 2.6: Drain Current during turn-on transient

Input File mos2/mos2ex03.in:

1 go athena

```
2  #
3  line x loc=0 spac=0.1
4  line x loc=0.35 spac=0.02
5  line x loc=0.5 spac=0.1
6  #
7  line y loc=0.00 spac=0.01
8  line y loc=0.2 spac=0.01
9  line y loc=0.5 spac=0.02
10 line y loc=1.0 spac=0.2
11 #
12 init orientation=100 c.phos=le14
13 #
14 #pwell formation including masking off of the nwell
15 #
16 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
17 #
18 etch oxide thick=0.02
19 #
20 #P-well Implant
21 #
22 implant boron dose=5.0e12 energy=100 pears
23 #
24 diffus temp=950 time=100 weto2 hcl=3
25 #
26 #N-well implant not shown -
27 #
28 # welldrive
29 diffus time=220 temp=1200 nitro press=1
30 #
31 etch oxide all
32 #
33 #sacrificial "cleaning" oxide
34 diffus time=20 temp=1000 dryo2 press=1 hcl=3
35 #
36 etch oxide all
37 #
38 #gate oxide grown here:-
39 diffus time=10 temp=950 dryo2 press=1.00 hcl=3
40 #
41 extract name="gateox" thickness oxide mat.occno=1 x.val=0
42 #
43 #vt adjust implant
44 implant bf2 dose=1.2e12 energy=35 pearson
```

```
45 #
46 depo poly thick=0.250 div=3
47 #
48 etch poly left p1.x=0.35
49 #
50 relax y.min=0.5
51 method fermi compress
52 diffuse time=5 temp=900 weto2 press=0.8
53 #
54 implant phosphor dose=3.0e13 energy=50 pearson
55 #
56 depo oxide thick=0.150 divisions=5
57 #
58 etch oxide dry thick=0.155
59 #
60 implant arsenic dose=5.0e15 energy=50 pearson
61 #
62 #
63 method fermi compress
64 diffuse time=5 temp=900 nitro press=1.0
65 #
66 # extract final S/D Xj
67 extract name="xj" xj silicon mat.occcno=1 x.val=0.1 junc.occcno=1
68 #
69 etch oxide left p1.x=0.15
70 deposit alumin thick=0.03 div=2
71 etch alumin right p1.x=0.16
72 structure mirror right
73
74 electrode name=gate x=0.5 y=0.1
75 electrode name=source x=0
76 electrode name=drain x=0.9
77 electrode name=substrate backside
78
79 structure outfile=mos2ex03_0.str
80
81 tonyplot mos2ex03_0.str -set mos2ex03_0.set
82
83 ##### LDD MOSFET Gate Turn-On Transient Test #####
84 go atlas
85
86 # Set workfunction for poly gate and interface charge
87 contact name=gate n.polysilicon
```

```
88 interf qf=3E10
89 models mos
90
91 solve init
92
93 # Set drain capacitance to 0.5pF/um, the will mimik a Pchan in an invert-
er...
94 contact name=drain cap=0.5e-12 res=1.0e5
95
96 method newton autonr trap
97
98
99 # Calculate solution at VDS = 5.0V, BGS = 0.0V
100 solve prev
101 solve vdrain=5.0 local
102
103 # Store transient results
104 log      outf=mos2ex03_1.log master
105
106 # Apply Gate turn-on transient
107 solve vgate=5.0 ramptime=5e-09 dt=2e-11 tstop=50e-09
108
109 extract max(curve(v."drain", i."drain")) name="Surge Current (Amps) "
110 tonyplot mos2ex03_1.log -set mos2ex03_1.set
111
112 quit
```

2.1.4. mos2ex04.in: 3D Width Effect Simulation

Requires: SSUPREM4/DevEdit3D/DEVICE3D

This example demonstrates Id/Vg's simulation of a narrow N-channel MOS structure in three dimensions.

In this example, a 2D width cross-section of a MOS transistor is constructed using SSUPREM4. The structure is then passed to DEVEDIT3D for extending to 3D. Then the structure is interfaced to ATLAS for electrical testing. The input file consists of the following main portions:

- process simulation of field oxide bird's beak in ATHENA
- interface of the 2D structure from ATHENA to DevEdit3D
- structure editing to create 3D MOSFET
- interface of the 3D structure from DevEdit3D to ATLAS
- simulation of the Id/Vgs characteristic in ATLAS
- extraction of Vt and sub-threshold leakage parameters

The first stage of the input file simulates width cross section on an NMOS device. The process sequence is for a LOCOS oxidation with a mask edge at X=0.0um. A channel stop implant is done be-

fore the oxidation. Following the mask removal, a gate oxide is grown. Then a channel implant is done before poly deposition.

At the end of the process sequence the gate and substrate electrodes are defined. Only these two electrode are present in this 2D section. The source and drain will be added in DevEdit3D.

DEVEDIT3D is used to convert the 2D ATHENA results to a 2D structure. Each region from the 2D structure is given an extent in the Z direction. This example will be a 0.5 micron long transistor. Thus, the polysilicon region extends only from 0.3 to 0.8 microns. The basic procedure in DevEdit3D is:

- modify existing region extent in Z direction (eg. polysilicon)
- add new aluminum regions for source and drain contacts. Specify these as electrode regions.
- Add N+ arsenic doping for source and drain. Be sure the Z extent of the doping includes a 0.1 micron spacer away from the gate edge. Specify y-rolloff (junction depth) and x and z rolloffs (lateral spread).
- define base level mesh (0.2x0.2 microns) and mesh the structure in X and Y.
- use REFINE to add mesh points in the channel region
- use the `z_plane` statement to control the mesh in the Z direction. The Z direction mesh is made up of planes XY mesh leading to prismatic mesh elements.

To generate DevEdit3D syntax for a given set of structure editing and mesh operations, it is often best to do these same operations in the graphical mode of DEVEDIT3D. DEVEDIT3D allows users to save the commands used in the graphical mode to a command file. It is this command file that is used as the basis for the batch-mode DEVEDIT3D used in this example.

The ATLAS simulation begins by reading in the structure from DevEdit3D. DECKBUILD provides an automatic interface between DEVEDIT3D and ATLAS so that the structure produced by the DEVEDIT3D is transferred to ATLAS without having to indicate the mesh statement in ATLAS.

The contact statement is used to set a work function on the polysilicon gate. The models statement is used to select a set of physical models for this simulation. In this case, these models are SRH recombination, the CVT mobility model, and one carrier model (carriers=1)

The drain voltage is set to 0.1V, and gate voltage is ramped. The IV data is saved to a log file. This file is used as input to the EXTRACT routines for threshold voltage and sub-threshold leakage. This file can also be plotted in Tonyplot. The save statement saves a 3D solution file. This can be plotted in TONYPLOT3D to see 3D distributions of potential and carriers.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

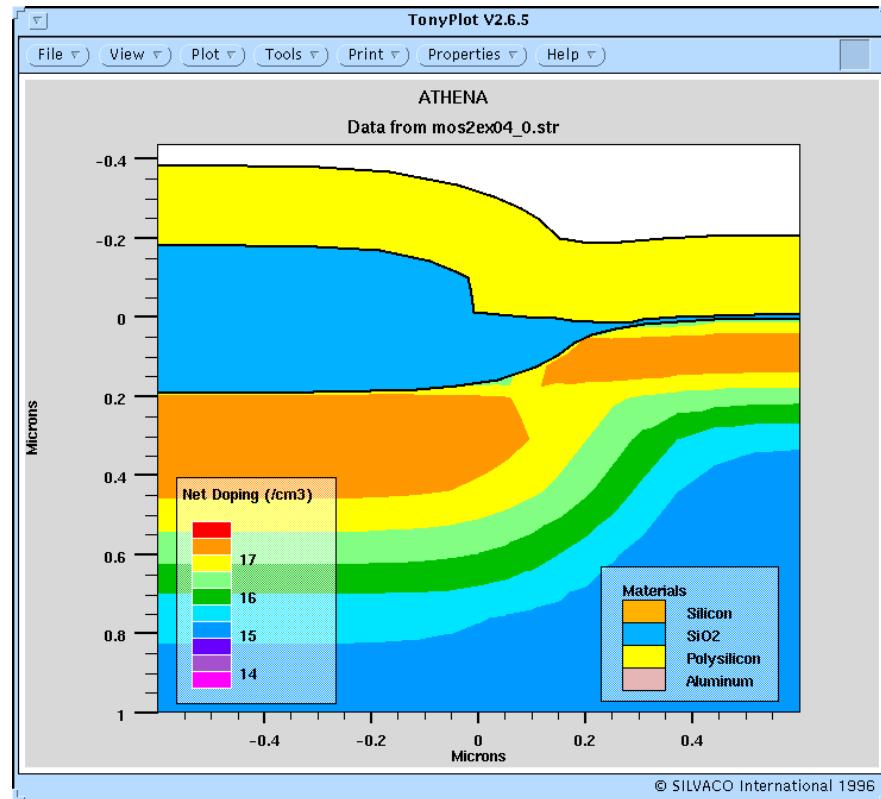


Figure 2.7: 2D channel edge and field structure simulated in ATHENA. This is a simulation across the width of a MOSFET in the center of the channel length

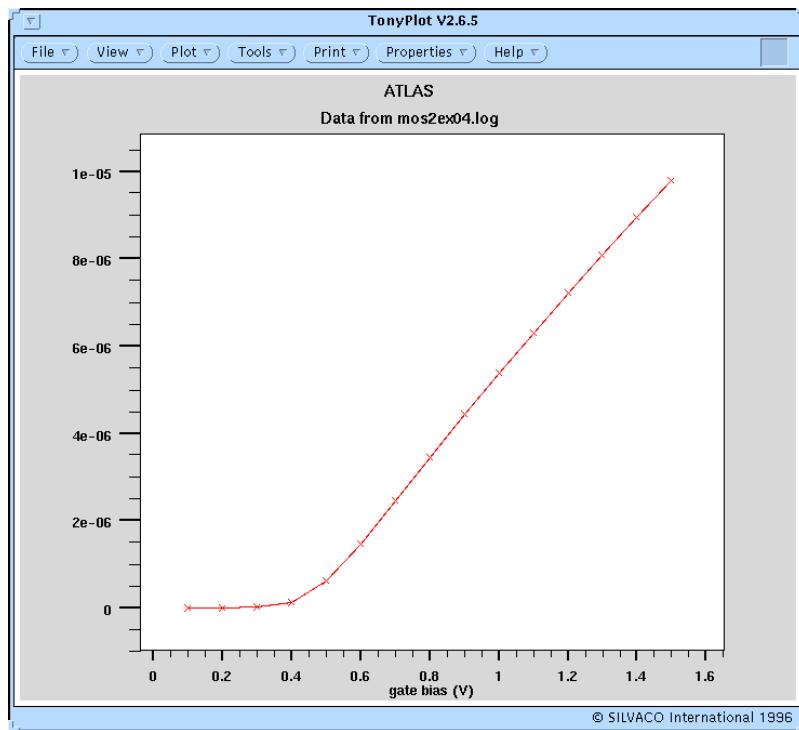


Figure 2.8: IdVg curve from 3D MOSFET including width effect

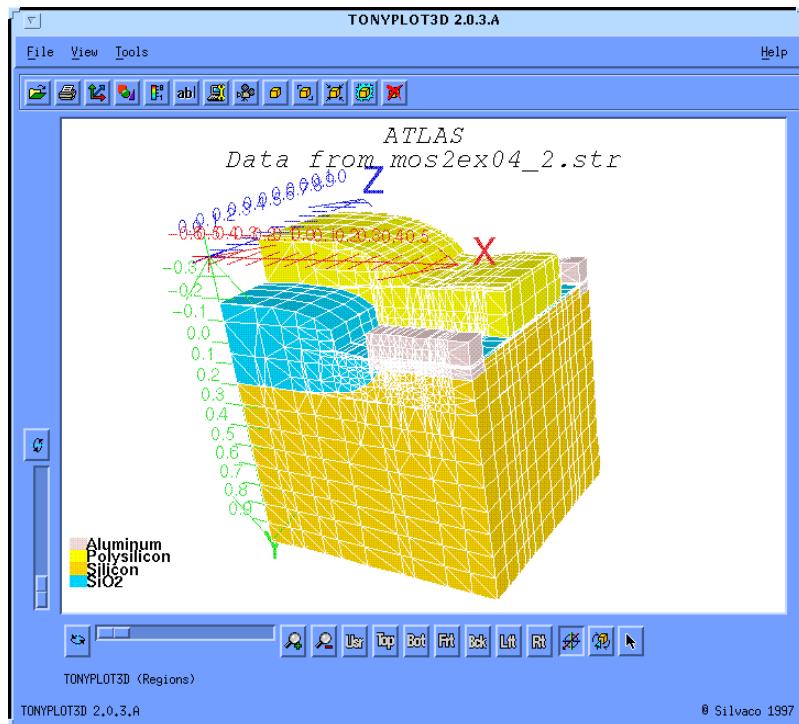


Figure 2.9: Geometry and Mesh of the 3D MOSFET formed in DevEdit3D using the ATHENA channel width simulation

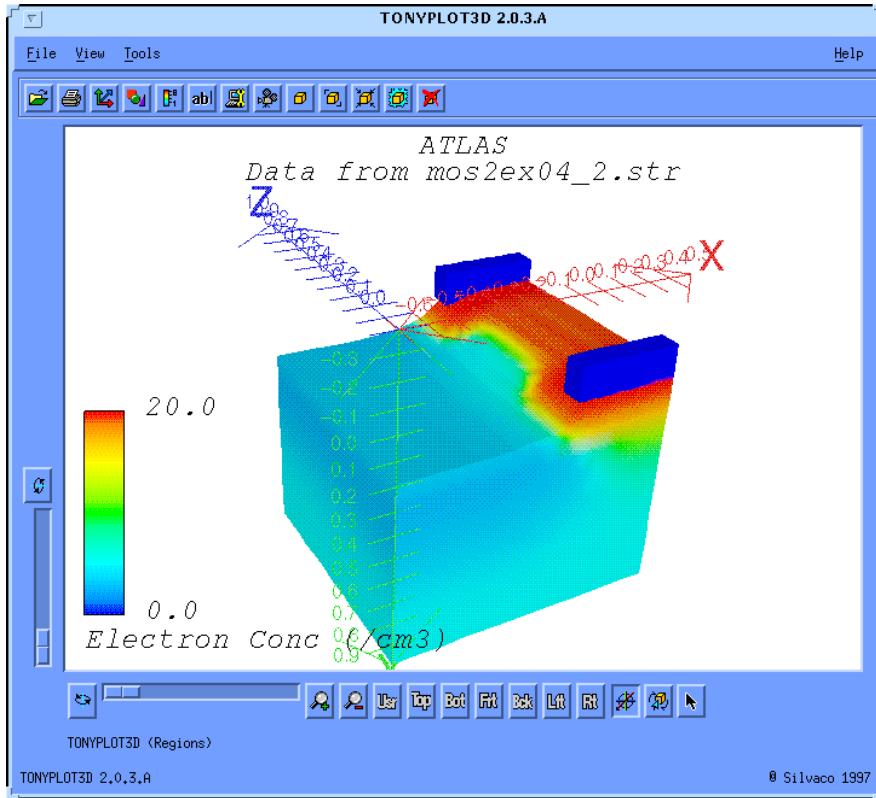


Figure 2.10: Carrier concentration in the 3D MOS channel. The field and gate oxide are removed for clarity. Note the inversion under the bird's beak that might lead in inverse width effect on V_t .

Input File mos2/mos2ex04.in:

```

1 go athena
2
3 # Substrate mesh definition
4 line y loc=0      spac=0.05
5 line y loc=0.6    spac=0.2
6 line y loc=1
7
8 line x loc=-0.6  spac=0.2
9 line x loc=0      spac=0.05
10 line x loc=0.2   spac=0.05
11 line x loc=0.6   spac=0.1
12
13 init orient=100 boron conc=1e15
14
15 # Pad oxide and nitride mask
16 deposit oxide thick=0.01
17 deposit nitride thick=0.25
18 deposit barrier thick=0.01
19 etch    barrier left p1.x=0

```

```
20 etch nitride left p1.x=0
21 etch oxide left p1.x=0
22
23 implant boron dose=1e13 energy=100
24 etch barrier all
25
26 # Field oxidation
27 method compress
28 diffuse tim=60 tem=1000 weto2
29
30 # extract field oxide thickness
31 extract name="Field Tox" thickness material="SiO~2" mat.occno=1 x.val=-0.6
32
33 etch nitride all
34 etch oxide dry thickness=0.05
35
36 # gate oxidation
37 diff tim=12 temp=950 dryo2
38
39 # extract gate oxide thickness
40 extract name="Gate Tox" thickness material="SiO~2" mat.occno=1 x.val=0.5
41
42 # channel implant
43 implant boron dose=3e12 energy=25
44 depo poly thickness=0.2 div=5 c.phos=1e19
45
46 diff time=10 temp=950 nitrogen
47
48 electrode name=gate x=0
49 electrode name=substrate backside
50
51
52 structure outf=mos2ex04_0.str
53
54 tonyplot mos2ex04_0.str -set mos2ex04_0.set
55
56
57
58 go DevEdit simflags="-3d"
59
60 # load file with specified Z extent
61 init inf=mos2ex04_0.str z1=0 z2=1.1
```

```
62
63  region reg=1 mat=Silicon Z1=0 Z2=1.1
64
65  region reg=2 mat="Silicon Oxide" Z1=0 Z2=1.1
66
67  region reg=3 mat=PolySilicon  Z1=0.3 Z2=0.8
68
69  region reg=4 name=source mat=Aluminum elec.id=1 work.func=0 col-
    or=0xfffc8c8 pattern=0x7 Z1=0 Z2=0.1 \
70  points="0.6,-0.007 0.6,0.005 0.6,0.05 0.2018696,0.05 0.15,0.05 0.15,0.004
    0.15,-0.1 0.6,-0.1 0.6,-0.007"
71
72  region reg=5 name=drain mat=Aluminum elec.id=2 work.func=0 color=0xfffc8c8 \
    pattern=0x7 Z1=1 Z2=1.1 \
73  points="0.15,0.05 0.15,0.004 0.15,-0.1 0.6,-0.1 0.6,-0.007 0.6,0.005
    0.6,0.05 0.2018696,0.05 0.15,0.05"
74
75
76  impurity id=1 imp=Arsenic color=0x8c5d00 \
77  x1=0.15 x2=0.6 y1=0 y2=0 \
78  peak.value=1e+20 ref.value=1e+15 z1=0 z2=0.2 comb.func=Multiply \
79  rolloff.y=both conc.func.y="Gaussian (Dist)" conc.param.y=0.25 \
80  rolloff.x=both conc.func.x="Gaussian (Dist)" conc.param.x=0.15 \
81  rolloff.z=both conc.func.z="Gaussian (Dist)" conc.param.z=0.15
82  impurity id=2 imp=Arsenic color=0x8c5d00 \
83  x1=0.15 x2=0.6 y1=0 y2=0 \
84  peak.value=1e+20 ref.value=1e+15 z1=0.9 z2=1.1 comb.func=Multiply \
85  rolloff.y=both conc.func.y="Gaussian (Dist)" conc.param.y=0.25 \
86  rolloff.x=both conc.func.x="Gaussian (Dist)" conc.param.x=0.15 \
87  rolloff.z=both conc.func.z="Gaussian (Dist)" conc.param.z=0.15
88  impurity id=3 imp=Phosphorus color=0x8c5d00 \
89  x1=0.15 x2=0.6 y1=0 y2=0 \
90  peak.value=1e+18 ref.value=1e+15 z1=0.8 z2=1.1 comb.func=Multiply \
91  rolloff.y=both conc.func.y="Gaussian (Dist)" conc.param.y=0.2 \
92  rolloff.x=both conc.func.x="Gaussian (Dist)" conc.param.x=0.1 \
93  rolloff.z=both conc.func.z="Gaussian (Dist)" conc.param.z=0.1
94  impurity id=4 imp=Phosphorus color=0x8c5d00 \
95  x1=0.15 x2=0.6 y1=0 y2=0 \
96  peak.value=1e+18 ref.value=1e+15 z1=0 z2=0.3 comb.func=Multiply \
97  rolloff.y=both conc.func.y="Gaussian (Dist)" conc.param.y=0.2 \
98  rolloff.x=both conc.func.x="Gaussian (Dist)" conc.param.x=0.1 \
99  rolloff.z=both conc.func.z="Gaussian (Dist)" conc.param.z=0.1
100
101 constr.mesh region=1 default max.height=0.2 max.width=0.2
```

```
102
103 #
104 # Perform mesh operations
105 #
106 Mesh Mode=MeshBuild
107 refine mode=both x1=0.4098 y1=0.0048 x2=0.5988 y2=0.1799
108 refine mode=both x1=0.2216 y1=0.0376 x2=0.3718 y2=0.1849
109
110 z.plane z=0 spacing=0.1
111 #
112 z.plane z=0.1 spacing=0.1
113 #
114 z.plane z=0.3 spacing=0.05
115 #
116 z.plane z=0.55 spacing=0.2
117 #
118 z.plane z=0.8 spacing=0.05
119 #
120 z.plane z=1 spacing=0.1
121 #
122 z.plane z=1.1 spacing=0.1
123 #
124 z.plane max.spacing=1000000 max.ratio=1.5
125
126 structure outf=mos2ex04_1.str
127
128
129 go atlas
130
131
132 contact name=gate n.poly
133 interface qf=3e10
134
135 models cvt srh print
136
137 method carriers=1 electrons
138
139 solve vdrain=0.1
140
141 log outf=mos2ex04.log
142 solve vgate=0.1 vstep=0.1 vfinal=1.5 name=gate
143 save outf=mos2ex04_2.str
144
```

```
145 extract name="vt" xintercept(maxslope(curve(v."gate",i."drain")))\ \
146      - ave(v."drain")/2.0
147 extract name="subvt" \
148      1.0/slope(maxslope(curve(v."gate",log10(i."drain")))))
149
150 tonyplot -st mos2ex04.log
151
152 quit
```

2.1.5. mos2ex05.in: Comparison of Id/Vds using EB and NEB models

Requires: SSUPREM4/SPISCES/GIGA

This example demonstrates fabrication and Id/Vd's analysis of a short channel structure with Energy Balance and Non-isothermal Energy Balance Models. The example shows:

- creation of a short channel MOSFET in ATHENA
- regridding in DEVEDIT
- isothermal Id/Vds analysis in ATLAS
- non-isothermal Id/Vds analysis in ATLAS

Deep submicron devices should be simulated using the Energy Balance Model due to velocity overshoot and nonlocal impact ionization effects, which could substantially influence device characteristics. For high current levels (high gate voltages) the thermal self-heating effects can also play an important role by decreasing mobility and impact ionization rate. This example demonstrates a comparison of Id/Vds curves obtained between the Energy Balance and Nonisothermal Energy Balance Models.

The structure is formed using a standard LDD NMOS process and regridding is performed in DevEdit to refine the mesh in the areas where high electric fields will occur in ATLAS. This procedure is described under the Substrate and Gate current example in the MOS example section.

There are two ATLAS runs in this example file. The first ATLAS run uses Energy Balance Model and the second run uses both the energy balance and heat flow equations.

In both runs the material statement is used to assign an energy relaxation time for electrons. The models statement is used to select a set of physical models for this simulation. In this case these models are CONSRH and AUGER recombination, the CVT mobility model, Band Gap Narrowing, two carriers model (carriers=2), and the energy balance equation for electrons only (hcte.el). The impact statement is used to assign the energy relaxation length for the Selberherr model. The contact statement is used to assign the work function on the polysilicon gate.

The gate voltage is ramped to 3V. At this stage, a combined algorithm is used by specifying method gummel newton. This means that if convergence is not reached in decoupled (or gummel) mode the simulator will automatically switch to coupled (or newton) mode; then the drain voltage is ramped. Typically the combined algorithm is used for low and moderate drain biases, and Newton alone for high drain biases.

The drain voltage is ramped to show the Id/Vd's curves obtained up to 8V. This demonstrates the convergence improvements possible by using a fully coupled solution for energy balance simulation. A decoupled solution generally would not converge at higher drain biases.

In the second ATLAS run, the same set of models is used, except that the solution of the lattice energy balance equation is activated using models lat.temp.

As with all lattice heat flow simulation, thermal boundary conditions must be defined. Thermal boundary conditions are defined in the thermcontact statement. A value of the thermal conduc-

tance is specified at the thermal contact located along the substrate, while thermal isolation conditions are assumed on all the other surfaces.

The final Id/Vd's curves can be compared and overlaid using TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

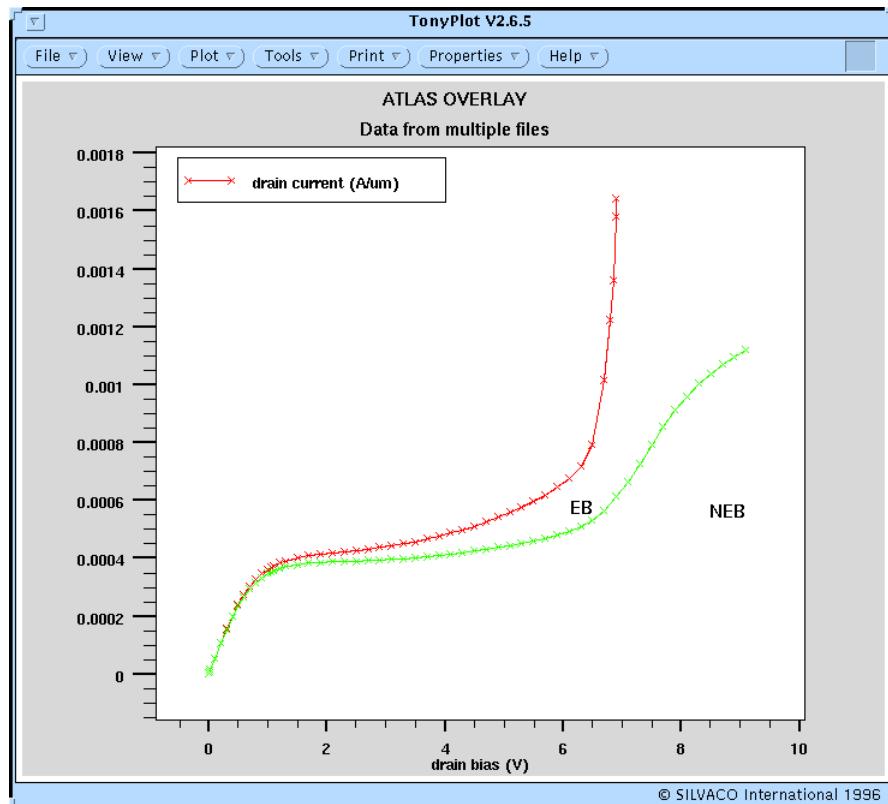


Figure 2.11: Effect of including lattice heating in a submicron MOS Id/Vds simulation using energy balance models. Local heating suppresses impact ionization.

Input File mos2/mos2ex05.in:

```

1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.2 spac=0.01
5 line x loc=0.5 spac=0.01
6 #
7 line y loc=0.00 spac=0.01
8 line y loc=0.2 spac=0.01
9 line y loc=0.5 spac=0.05
10 line y loc=0.8 spac=0.15
11 #
12 init orientation=100 c.phos=1e14 space.mul=3
13

```

```
14 #pwell formation including masking off of the nwell
15 #
16 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
17 #
18 etch oxide thick=0.02
19 #
20 #P-well Implant
21 #
22 implant boron dose=8e12 energy=100 pears
23 #
24 diffus temp=950 time=100 weto2 hcl=3
25 #
26 #N-well implant not shown -
27 #
28 # welldrive starts here
29 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
30 #
31 diffus time=220 temp=1200 nitro press=1
32 #
33 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
34 #
35 etch oxide all
36 #
37 #sacrificial "cleaning" oxide
38 diffus time=20 temp=1000 dryo2 press=1 hcl=3
39 #
40 etch oxide all
41 #
42 #gate oxide grown here:-
43 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
44 #
45 #
46 extract thickness name="gateox" oxide mat.occno=1 min.v=140
47 #
48 #
49 #vt adjust implant
50 implant boron dose=9.5e11 energy=10 pearson
51 #
52 depo poly thick=0.2 divi=10
53 #
54 #from now on the situation is 2-D
55 #
56 etch poly left pl.x=0.35
```

```
57 #
58 method fermi compress
59 diffuse time=3 temp=900 weto2 press=1.0
60 #
61 implant phosphor dose=3.0e13 energy=20 pearson
62 #
63 depo oxide thick=0.120 divisions=8
64 #
65 etch oxide dry thick=0.120
66 #
67 implant arsenic dose=5.0e15 energy=50 pearson
68 #
69 method fermi compress
70 diffuse time=1 temp=900 nitro press=1.0
71 #
72
73 #
74 etch oxide left p1.x=0.2
75 deposit alumin thick=0.03 divi=2
76 etch alumin right p1.x=0.18
77 structure mirror right
78
79 electrode name=gate x=0.5 y=0.1
80 electrode name=source x=0.1
81 electrode name=drain x=0.9
82 electrode name=substrate backside
83
84 structure outfile=mos2ex05.str
85 #
86
87
88
89
90 go DevEdit
91
92
93 # Set Meshing Parameters
94 #
95 base.mesh height=1000000 width=1000000
96 #
97 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.points when=automatic
98 #
```

```
99 imp.refine imp="NetDoping" sensitivity=1
100 imp.refine min.spacing=0.02
101 #
102 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
103 max.width=1 min.height=0.0001 min.width=0.0001
104 #
105 # Perform mesh operations
106 #
107 Mesh Mode=MeshBuild
108 refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
109 refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
110 refine mode=both x1=0.65 y1=0.26 x2=0.83 y2=0.34
111 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
112 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
113 refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
114 structure outf=mos2ex05_0.str
115 tonyplot mos2ex05_0.str -set mos2ex05_0.set
116
117 go atlas
118
119 material taurel.el=0.2e-12 taumob.el=0.2e-12
120
121 models bgn cvt hcte.el consrh auger print
122
123 impact selb length.rel lrel.el=0.02
124
125 contact name=gate n.poly
126
127 solve init
128
129 method gummel newton maxtrap=6 temp.tol=1.e-4 trap
130
131
132
133 output e.velocity
134
135 solve vgate=1
136 solve vgate=2
137 solve vgate=3
138
139
140
141 # Id-Vd caculations with EB model
```

```
142
143 log outf=mos2ex05_3_eb.log master
144
145 method gummel newton trap maxtrap=6 temp.tol=1.e-4
146
147
148 solve vdrain=0.00625
149 solve vdrain=0.0125
150 solve vdrain=0.025
151 solve vdrain=0.1 vstep=0.1 vfinal=1 electr=3
152
153 method newton trap maxtrap=6 temp.tol=1.e-4
154
155 solve vdrain=1.1 vstep=0.2 electr=3 vfinal=8.3 compliance=1.6e-3
      cname=drain
156 save outf=mos2ex05_3_eb.str
157
158
159 go atlas
160
161 material taurel.el=0.2e-12 taumob.el=0.2e-12
162
163 models bgn cvt hcte.el lat.temp consrh auger print
164
165 impact selb length.rel lrel.el=0.02
166
167 contact name=gate n.poly
168
169 thermcontact num=1 x.min=0 x.max=1 y.min=0.799 y.max=0.802 alpha=3000
170
171
172 solve init
173
174 method gummel newton trap maxtrap=6 temp.tol=1.e-4
175
176 output e.velocity
177
178 solve vgate=1
179 solve vgate=2
180 solve vgate=3
181
182 # Id-Vd caculations with NEB model
183
```

```
184
185 log outf=mos2ex05_3_neb.log master
186
187 method gummel newton trap maxtrap=6 temp.tol=1.e-4
188
189 solve vdrain=0.00625
190 solve vdrain=0.0125
191 solve vdrain=0.025
192 solve vdrain=0.1 vstep=0.1 vfinal=1 electr=3
193
194 method newton trap maxtrap=6 temp.tol=1.e-4
195 solve vdrain=1.1 vstep=0.2 electr=3 vfinal=9.1
196 save outf=mos2ex05_3_neb.str
197
198 tonyplot mos2ex05_3_eb.log -overlay mos2ex05_3_neb.log -set
    mos2ex05log.set
199
200
201 quit
202
```

2.1.6. mos2ex06.in: BSIM3 SPICE Model Extraction (Salicide process)

Requires: SSUPREM4/SILICIDES/SPISCES/UTMOST

This example demonstrates extraction of a BSIM3 SPICE model from ATLAS simulation data of an NMOS transistor. The example:

- forms a MOS device in ATHENA using a salicide process
- uses assigned variables to parameterize the structure
- simulates Id/Vgs-Vb's curves in ATLAS
- simulates Id/Vds-Vg's curves in ATLAS
- interfaces to UTMOST for extraction of a BSIM3 parameter set.

The process simulation used for this example is an NMOS process flow. Further description of MOS process simulation can be found in the MOS examples description. As a more advanced technique, this flow has been parameterized in places using the `set` statements. These are used to assign variables such as spacer width, which are then used later in several locations in the input file. Extract statements are used throughout the process simulation to measure important process parameters. In terms of the SPICE model extraction, it is vital to extract the gate oxide thickness in meters for use in UTMOST.

The salicide process creates self-aligned silicides on the source, drain and gate requires the use of the ATHENA/SILICIDES module. Users who do not have this option could replace the silicidation steps with metal deposition and patterning as used in the previous MOS examples. In this transistor, titanium silicide is used. A titanium layer is deposited and a short heat cycle is applied. No special method parameters are needed to enable creation of the silicide layer during this diffusion. The remaining titanium is then stripped. These silicide regions are indicated in the `electrode` definition in ATHENA.

The two ATLAS runs in this example are also parameterized using the `set` statement. This enables easy conversion of the whole Id/Vgs and Id/Vds tests from, say, NMOS to PMOS or 5.0V supply to 3.3V.

The first ATLAS run simulates Id/Vgs curves at three substrate biases. The sequence of `solve` statements is to first save three solutions at each back bias with $V_{ds}=0.1V$ and $V_{gs}=0.0V$. Then in turn each of these three files is loaded using `load` and the gate voltage ramped up to the supply voltage is defined as ' v_{dsmax} '. In this example all three curves are saved to a single log file. However, it is more traditional to save the three curves in separate files. Either approach is possible.

The second ATLAS run simulates Id/Vds curves at three different gate voltages. A similar technique to the first run is used. Three solution files are saved at each gate bias with $V_{ds}=0.0V$. These are then loaded in turn and the drain voltage ramped to ' v_{dsmax} '. All the curves are saved to a single log file although separate ones could be used for each curve.

The final stage of the example is to run UTMOST to extract the SPICE model. Important information about the structure such as gate oxide thickness and gate length is transferred to UTMOST using the results of `extract` statements in the ATHENA simulation. The log files from ATLAS are loaded and appended together. UTMOST then fits the SPICE model to the complete Id/Vgs-Vbs and Id/Vds-Vgs data sets. All the UTMOST parameters are stored to a file and then `extract` is used to print out the parameters of interest.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

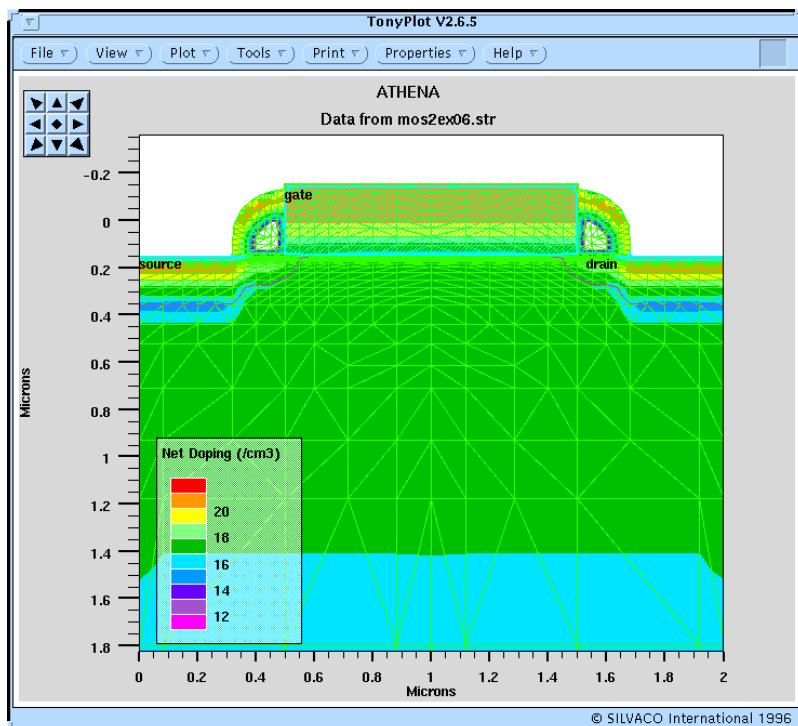


Figure 2.12: Geometry, mesh and doping of a 1.0um MOSFET simulated in ATHENA

Input File mos2/mos2ex06.in:

```

1 go athena
2
3 #Salicided N-MOSFET Full IV Curve Application

```

```
4  =====
5
6  # Define a global grid density multiplier....make this value
7  # bigger to speed up the simulation for demos etc....
8
9  set grid_density=1
10 #
11 #
12 line x loc=0      spac=0.1
13 line x loc=0.2    spac=0.05
14 line x loc=0.32   spac=0.05
15 line x loc=0.4    spac=0.05
16 line x loc=0.5    spac=0.05
17 line x loc=0.6    spac=0.05
18 line x loc=0.8    spac=0.1
19 line x loc=1      spac=0.15
20 #
21 line y loc=0.00   spac=0.01
22 line y loc=0.15   spac=0.005
23 line y loc=0.17   spac=0.005
24 line y loc=0.25   spac=0.05
25 line y loc=2.5    spac=0.15
26 line y loc=5.0    spac=0.5
27 #
28 init c.phos=1.0e14 spac=$grid_density
29 #
30 #pwell formation including masking off of the nwell
31 diffus time=30 temp=900 dryo2 press=1.00 hcl=3
32 #
33 etch oxide thick=0.025
34 #
35 #P-well Implant
36 #
37 implant boron dose=1.5e13 energy=100 pears
38 #
39 diffus temp=925 time=100 weto2 hcl=3
40 #
41 #N-well implant not shown -
42 #
43 # welldrive starts here
44 set welldrive_temp=1200
45 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
46 diffus time=120 temp=$welldrive_temp nitro
```

```
47 diffus time=90 temp=$welldrive_temp t.rate=-4.444 nitro
48 #
49 # Experimentally: Dip off the oxide and measure the peak conc.....
50 extract name="peak conc" max.conc boron silicon mat.occcno=1
51 etch oxide all
52 #
53 #sacrificial "cleaning" oxide
54 diffus time=20 temp=900 dryo2 press=1 hcl=3
55 extract thickness oxide mat.occcno=1 name="sacox"
56 #
57 etch oxide all
58 #
59 # gate oxide grown here:-
60 # make sure it has a couple of grid points....
61 # Set a partial pressure variable for use as a calibration parameter....
62 # note, the grid density has been adjusted during growth to improve accuracy...
63 set ppress=1
64 set gate_temp=875
65 method grid.ox=0.005
66 diffus time=10 temp=800 t.final=$gate_temp nit press=$ppress
67 diffus time=5 temp=$gate_temp nitrogen press=$ppress hcl=3
68 diffus time=28 temp=$gate_temp dryo2 press=$ppress hcl=3
69 diffus time=25 temp=$gate_temp nitrogen press=$ppress hcl=3
70 diffus time=20 temp=$gate_temp t.final=800 dryo2 press=$ppress hcl=3
71 # Extract the gateoxide for use later in the Spice Model extraction...
72 extract thickness oxide mat.occcno=1 name="tox"
73 # Reset the grid during oxide growth, back to default...
74 method grid.ox=0.1
75 #
76 #convert tox to meters for utmost
77 extract name="utmost_tox" ($tox * 1.0e-10)
78 #
79 #vt adjust implant
80 implant boron dose=1.4e12 energy=20 pearson
81 #
82 depo poly thick=0.3 spaces=8
83 #example converts to 2D following this step
84 etch poly left p1.x=0.5
85 #
86 # Relax the mesh below the active device area
87 relax y.min=0.3
88 relax y.min=0.4
```

```
89 relax y.min=0.5
90
91
92 # Name the gate electrode as later it will be covered with TiSix....
93 electrode name=gate x=0.55
94 #
95 method fermi compress
96 diffuse time=10 temp=875 dry press=1.0
97 #
98 implant phosphor dose=1.0e13 energy=35 pear
99 #
100 #Spacer Formation - setup a variable as a spacer thickness....
101 set spacer_width=0.175
102 depo oxide thick=$spacer_width divisions=8
103 etch oxide dry thick="$spacer_width"+0.025
104 #
105 # SD Implant
106 implant arsenic dose=5.0e15 energy=45 pear
107 #
108 # RTA dopant activation
109 diffuse temp=1000 time=0.1667 nitrogen
110 structure outf=activate.str
111 #
112
113 # Create the salicide areas
114 deposit titan thick=0.1 divi=3
115 diffuse temp=800 time=0.5 nitrogen
116 etch titanium all
117
118
119
120 #
121 ##### Extract Design parameters
122 #####
123 #####
124
125 # Extract some design parameters for use with Utmost model extraction lat-
er....
126
127 # Extract a first order approximation for NSUB as the average of the
128 # surface and peak channel conc values.....
```

```
129 #
130 extract name="chan_peak_conc" max.conc impurity="Net Doping" material="Silicon" mat.occcno=1 x.val=0.5
131 #
132 extract name="chan_surf_conc" surf.conc impurity="Net Doping" material="Silicon" mat.occcno=1 x.val=0.5
133 extract name="nsub" ($"chan_peak_conc"+$"chan_surf_conc")/2
134
135
136 # Reflect the structure....
137 structure mirror right
138
139 # Extract the poly Ld at this point.....
140 extract name="ld" thick poly y.val=0
141 extract name="utmost_ld" ($ld * 1.0e-4)
142
143
144
145 #####
146 ##### SET UP ELECTRODE NAMES #####
147 #####
148
149
150 # Name the electrodes for Atlas....in the correct order of use.....
151 # Note the gate has been named before, as we do not want a voltage
152 # drop running down through the poly from the overlying TiSix....
153 electrode name=substrate backside
154 electrode name=source x=0.1
155 electrode name=drain x=1.9
156
157
158 structure outfile=mos2ex06.str
159 tonyplot mos2ex06.str -set mos2ex06_0.set
160
161 #####
162 ##### SET UP ATLAS TEST VARIABLES #####
163 #####
164
165 # These variables are set to enable simple modification of the
166 # MOS level 3 test.
167 #
168 # setup ATLAS runs
169 # general
170 set polarity=1
```

```
171 set vdd=$polarity*5.0
172
173 #idvg
174 set vdslin=$polarity*0.1
175 set vdslinhalf=$polarity*0.05
176 set vgstep=$polarity*0.2
177 set vbsmax=-1*$vdd
178 set vbshalf=$vbsmax/2
179
180 #idvd
181 #      can't change vgcurves w/o syntax change later
182 set vdstep=$polarity*0.2
183 set vgmin=$polarity*2.0
184 set vgcurves=3
185 set vghalf=($vdd+$vgmin)/($vgcurves-1)
186 set vbs=0.0
187
188 ##### START ATLAS SIMULATION #####
189
190
191 go atlas
192
193
194 models cvt srh print
195
196 contact name=gate n.poly
197 interface qf=3e10
198
199
200 solve init
201
202 save outf=init.str master
203
204
205 method newton autonr trap
206 solve prev
207 solve vdrain=$vdslinhalf
208 solve vdrain=$vdslin
209 solve vsubstrate=0 outf=solve_tmp0
210 solve vsubstrate=$vbshalf outf=solve_tmp1
211 solve vsubstrate=$vbsmax outf=solve_tmp2
212
213 ##### Create the IdVg-Vb IV matrix #####
```

```
214 load infile=solve_tmp0
215 log outf=mos2ex06_IdVg-Vb.log
216 solve name=gate vgate=0 vfinal=$vdd vstep=$vgstep
217
218 load infile=solve_tmp1
219
220 solve name=gate vgate=0 vfinal=$vdd vstep=$vgstep
221
222 load infile=solve_tmp2
223
224 solve name=gate vgate=0 vfinal=$vdd vstep=$vgstep
225
226 ##### Create the IdVd-Vg IV matrix #####
#
227 go atlas
228
229 models cvt srh print
230
231 contact name=gate n.poly
232 interface qf=3e10
233
234
235 solve init
236
237
238
239 method newton autonr trap
240 solve prev
241 solve vsubstrate=$vbs
242 #solve vgate=$vgmin outf=solve_tmp0
243 #solve vgate=$vghalf outf=solve_tmp1
244 #solve vgate=$vdd outf=solve_tmp2
245
246 solve vgate=1 vstep=0.25 vfinal=1.5 name=gate outf=solve_tmp0 onefile
247
248 solve vgate=1.75 vstep=0.25 vfinal=3 name=gate outf=solve_tmp1 onefile
249
250 solve vgate=3.25 vstep=0.25 vfinal=4.5 name=gate outf=solve_tmp2 onefile
251
252 ##### Create the IdVd-Vg IV matrix #####
#
253 load infile=solve_tmp0
254 log outf=mos2ex06_IdVd-Vg.log
255 solve name=drain vdrain=0 vfinal=$vdd vstep=$vdstep
```

```
256
257 load infile=solve_tmp1
258
259 solve name=drain vdrain=0 vfinal=$vdd vstep=$vdstep
260
261 load infile=solve_tmp2
262
263 solve name=drain vdrain=0 vfinal=$vdd vstep=$vdstep
264
265
266
267
268 ##### START UTMOST SIMULATION #####
269 go utmost
270 utmost type = mos
271
272 # load the Utmost setup file, this file is the Utmost Setup file created
   by an
273 # interactive Utmost session and stored in $SILVACO/var/utmost .....
274 model MOS_vwf_bsim3_n
275
276 # set value for gate oxide thickness
277 device TOX = $utmost_tox
278
279 # define device specifications
280 setup NRS=0.04 NRD=0.04 width=1.0 length=$utmost_ld polarity=N
281
282 # load Atlas log files
283 init inf=mos2ex06_IdVg-Vb.log master
284 init inf=mos2ex06_IdVd-Vg.log master append
285
286 # select required characteristics for device
287 deselect ID/VG-VB all
288 select ID/VG-VB device 1
289 deselect ID/VD-VG all
290 select ID/VD-VG device 1
291 output ID/VD-VG
292
293 # set up output log file for measured ATLAS data in uniform steps
294 # required by UTMOST
295 log outf=mos2ex06_data.log measured
296
297
```

```
298 # set up output log file for simulated data created by UTMOST
299 log outf=mos2ex06_sim.log simulated
300
301 # perform simulation
302 fit ID/VG-VB
303 fit ID/VD-VG
304 simulate ID/VD-VG
305
306 # output Utmost parameters for extraction
307 save outf=mos2ex06.ssf
308
309 ##### Extract UTMOST parameters #####
310
311 # load output parameter file from UTMOST
312 extract init infile="mos2ex06.ssf"
313
314 # extract UTMOST parameters required for VWF
315
316
317 extract name="N-VTH0" param="VTH0"
318 extract name="N-K1" param="K1"
319 extract name="N-K2" param="K2"
320 extract name="N-K3" param="K3"
321 extract name="N-W0" param="W0"
322 extract name="N-NLX" param="NLX"
323 extract name="N-DVT0" param="DVT0"
324 extract name="N-DVT1" param="DVT1"
325 extract name="N-DL" param="DL"
326 extract name="N-DW" param="DW"
327 extract name="N-UA" param="UA"
328 extract name="N-UB" param="UB"
329 extract name="N-UC" param="UC"
330 extract name="N-VSAT" param="VSAT"
331 extract name="N-A0" param="A0"
332 extract name="N-KETA" param="KETA"
333 extract name="N-A1" param="A1"
334 extract name="N-A2" param="A2"
335 extract name="N-RDSW" param="RDSW"
336 extract name="N-VOFF" param="VOFF"
337 extract name="N-NFACTOR" param="NFACTOR"
338 extract name="N-CDSC" param="CDSC"
339 extract name="N-ETA0" param="ETA0"
340 extract name="N-ETAB" param="ETAB"
```

```
341 extract name="N-DSUB" param="DSUB"
342 extract name="N-PCLM" param="PCLM"
343 extract name="N-PDIBL1" param="PDIBL1"
344 extract name="N-PDIBL2" param="PDIBL2"
345 extract name="N-DROUT" param="DROUT"
346 extract name="N-PSCBE1" param="PSCBE1"
347 extract name="N-PSCBE2" param="PSCBE2"
348 extract name="N-TOX" param="TOX"
349 extract name="N-XJ" param="XJ"
350 extract name="N-PEAK" param="NPEAK"
351 extract name="N-SUB" param="NSUB"
352 extract name="N-SUBTHMOD" param="SUBTHMOD"
353 extract name="N-SATMOD" param="SATMOD"
354 extract name="N-BULKMOD" param="BULKMOD"
355 extract name="N-U0" param="U0"
356
357
358 quit
359
360
```

2.1.7. mos2ex07.in: NMOS Snapback

Requires: SSUPREM4/DEVEDIT/ SPISCES

This example demonstrates the curve tracing algorithm in ATLAS to simulate the snapback of a MOSFET. The example shows:

- Creation of a N-channel MOSFET in ATHENA
- remesh by DEVEDIT,
- the ATLAS curve tracing algorithm is used to trace MOS snapback.

A standard NMOS device is constructed, remeshed and loaded into ATLAS. The process simulation, interface to DEVEDIT and initial setup in ATLAS are described in the previous section under MOS examples.

The initial syntax in ATLAS sets all the required contact, interface and model setting used for MOS simulation. These settings are described in earlier example descriptions. For breakdown and snapback simulation calculation of impact ionization is necessary. The `impact` statement is used to activate Selberherr impact ionization model.

Curve tracing is an algorithm for choosing the boundary conditions for a simulation to trace out an IV curve. It is typically used on curves such as snapback or latchup with many turning points.

For curve tracing simulations the key statement is: `curvetrace end.val=1.e-3 contr.name=drain curr.cont mincur=1e-10 nextst.ratio=1.3`. It is used to initialize parameters for a curve-tracing algorithm. The `contr.name` parameter specifies the name of an electrode for which the load line technique will be applied. Here this is the 'drain'. The `curr.cont` parameter sets the value of the current that will be monitored. The simulation will stop when the current exceeds the value specified by `end.val` parameter. The `mincur` parameter defines the minimum current value after which the load line technique will actually be applied. Before that, pure voltage boundary conditions are used. The `nextst.ratio` parameter defines the factor used

to increase voltage step on a parts of IV curve away from the turning points. The main place this is used is in the pre-breakdown voltage ramp. Solve curvetrace is used to activate a curve-tracing algorithm.

The final snapback curve can be plotted using TONYPLOT. To plot the drain voltage actually applied to the device, the x-axis should be set to drain int. bias and not drain bias. The 'drain int. bias' is the voltage on the drain contact/semiconductor interface. The value of drain bias should be disregarded since it includes the effect of the load line algorithm used for the curve trace.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

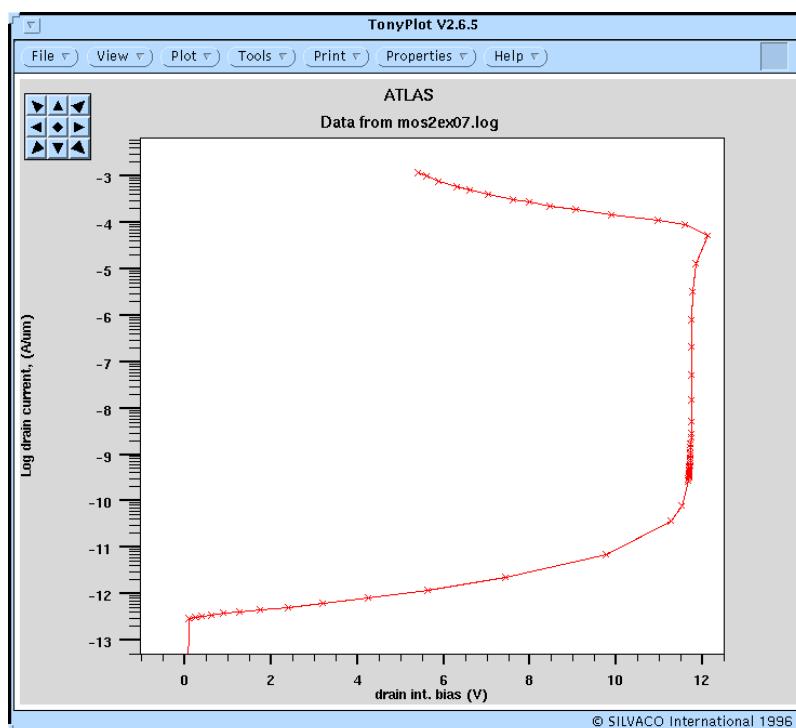


Figure 2.13: NMOS Snapback at zero gate bias using the CURVETRACE feature

Input File mos2/mos2ex07.in:

```

1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.7 spac=0.02
5 line x loc=1 spac=0.1
6 #
7 line y loc=0.00 spac=0.02
8 line y loc=0.5 spac=0.1
9 line y loc=1.2 spac=0.15
10 #
11 init orientation=100 c.phos=1.0e14
12 #pwell formation including masking off of the nwell

```

```
13 #
14 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
15 #
16 etch oxide thick=0.02
17 #
18 #P-well Implant
19 #
20 implant boron dose=5.0e12 energy=100 pears amorphous
21 #
22 diffus temp=950 time=100 weto2 hcl=3
23 #
24 #N-well implant not shown -
25 #
26 # welldrive starts here
27 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
28 #
29 diffus time=220 temp=1200 nitro press=1
30 #
31 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
32 #
33 etch oxide all
34 #
35 #sacrificial "cleaning" oxide
36 diffus time=20 temp=1000 dryo2 press=1 hcl=3
37 #
38 etch oxide all
39 #
40 #gate oxide grown here:-
41 diffus time=10 temp=1000 dryo2 press=1.00 hcl=3
42 #
43 # Here is a possible Target for optimisation....
44 extract thickness oxide mat.occno=1 min.v=140 name="gateox"
45
46 #
47 #vt adjust implant
48 implant boron dose=9.8e11 energy=25 pearson amorphous
49 #
50 # Now extract the surface and peak concs for channel profile optimisa-
      tion...
51 extract name="peak channel conc" max.conc boron silicon mat.occno=1
52 extract name="surface channel conc" surf.conc boron silicon mat.occno=1
53 #
54 depo poly thick=0.387 divis=15
```

```
55 #
56 etch poly left p1.x=0.7
57 #
58 method fermi compress
59 diffuse time=10 temp=850 weto2 press=1.0
60 #
61 implant phosphor dose=3.0e13 energy=60 pearson amorphous
62 #
63 depo oxide thick=0.150 divisions=8
64 #
65 etch oxide dry thick=0.150
66 #
67 implant arsenic dose=5.0e15 energy=90 pearson amorphous
68 #
69 method fermi compress
70 diffuse time=5 temp=900 nitro press=1.0
71 #
72
73 #
74 etch oxide left p1.x=0.3
75 deposit alumin thick=0.03 divi=2
76 etch alumin right p1.x=0.25
77 structure mirror right
78
79
80
81
82 electrode name=gate x=1 y=0.0
83 electrode name=source x=0
84 electrode name=drain x=1.99
85 electrode name=substrate backside
86
87 structure outfile=mos2ex07.str
88
89
90
91 tonyplot mos2ex07.str -set mos2ex07_0.set
92
93
94 go atlas
95 # add workfunction and interface charge
96 contact name=gate n.polysilicon
97 interf qf=3E10
```

```
98
99
100 # select MOS models
101 models cvt consrh print
102 impact selb
103
104 solve init
105 regrid potential abs ratio=0.1    cos.angl=0.6
106
107 solve init
108
109 method newton trap ir.tol=1.e-25 ix.tol=1.e-25 clim.dd=1.e8
110 curvetrace end.val=1.e-3 contr.name=drain curr.cont \
111           mincur=1e-10 nextst.ratio=1.3
112
113
114 # Open log file
115 log      outf=mos2ex07.log
116
117 solve curvetrace
118
119
120
121 # plot the final curve....
122 tonyplot mos2ex07.log -set mos2ex07_log.set
123
124 quit
```

2.1.8. mos2ex08.in: NMOS Second Breakdown Simulation

Requires: SSUPREM4/DevEdit/SPISCES/GIGA

This example demonstrates fabrication and second breakdown analysis of a short channel structure with non-isothermal energy balance models.

- A short channel MOSFET is created in Athena,
- regridding in DEVEDIT
- selection of the coupled solution of energy balance and lattice heating equations
- electrical analysis using the curve tracer algorithm to trace the IV curve

Deep submicron devices should be simulated using the Energy Balance Model due to velocity overshoot, and nonlocal impact ionization effects, which could substantially influence device characteristics. For high current levels the thermal self-heating effects can also play an important role by decreasing mobility and impact ionization rate. This example demonstrates second breakdown simulation with the non-isothermal energy balance model using curve tracing algorithm.

A fully coupled approach is used to solve five equations in this device. This provides much improved convergence over decoupled techniques used in older ATLAS versions.

The work function, interface charge and MOS models are set using the syntax as described in earlier examples. The energy balance equation for electrons and lattice energy balance equation are set by models hcte.el lat.temp. The impact statement is used to assign the energy relaxation length for Selberherr model. Thermal boundary conditions are required with any non-isothermal simulation. These are defined in the thermcontact statement. A value of the thermal conductance is specified at the thermal contact located along the substrate. Thermal isolation conditions are assumed on the all other surfaces.

The curvetrace statement is used to initialize parameters for curve tracing algorithm. A full description of the curve tracing syntax is included with the MOS snapback example. The gate voltage is ramped to 1V, and then the solve curvetrace statement is used to activate curve tracing algorithm.

Plotting the internal drain bias versus drain current in TONYPLOT will display the second breakdown curve. The resulting curve from ATLAS shows several turning points. The second breakdown occurs at the final stage where the voltage drops sharply. At this point both the lattice and carrier temperatures are high.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

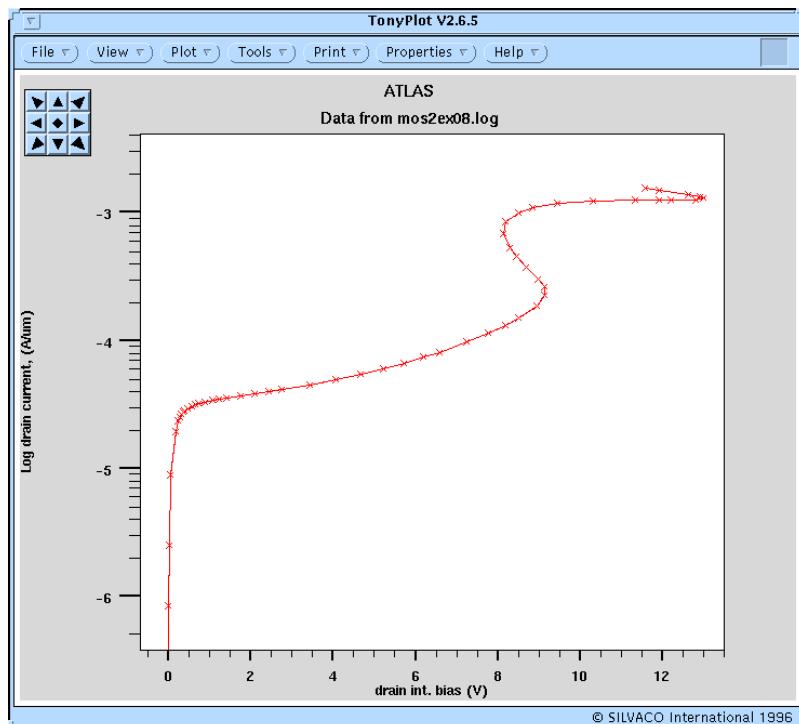


Figure 2.14: MOS second breakdown and snapback using non-isothermal models

Input File mos2/mos2ex08.in:

```

1 go athena
2
3 #
4 line x loc=0 spac=0.1
5 line x loc=0.2 spac=0.01
6 line x loc=0.5 spac=0.01

```

```
7  #
8  line y loc=0.00 spac=0.01
9  line y loc=0.2 spac=0.01
10 line y loc=0.5 spac=0.05
11 line y loc=0.8 spac=0.15
12 #
13 init orientation=100 c.phos=1e14 space.mul=3
14 #
15 moments STD_TABLES
16 #
17 #pwell formation including masking off of the nwell
18 #
19 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
20 #
21 etch oxide thick=0.02
22 #
23 #P-well Implant
24 #
25 implant boron dose=8e12 energy=100 pears amorphous
26 #
27 diffus temp=950 time=100 weto2 hcl=3
28 #
29 #N-well implant not shown -
30 #
31 # welldrive starts here
32 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
33 #
34 diffus time=220 temp=1200 nitro press=1
35 #
36 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
37 #
38 etch oxide all
39 #
40 #sacrificial "cleaning" oxide
41 diffus time=20 temp=1000 dryo2 press=1 hcl=3
42 #
43 etch oxide all
44 #
45 #gate oxide grown here:-
46 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
47 #
48 #
49 extract thickness name="gateox" oxide mat.occcno=1 min.v=140
```

```
50
51 #
52 #vt adjust implant
53 implant boron dose=9.5e11 energy=10 pearson amorphous
54 #
55 depo poly thick=0.2 divi=10
56 #
57 #from now on the situation is 2-D
58 #
59 etch poly left p1.x=0.35
60 #
61 method fermi compress
62 diffuse time=3 temp=900 weto2 press=1.0
63 #
64 implant phosphor dose=3.0e13 energy=20 pearson amorphous
65 #
66 depo oxide thick=0.120 divisions=8
67 #
68 etch oxide dry thick=0.120
69 #
70 implant arsenic dose=5.0e15 energy=50 pearson amorphous
71 #
72 method fermi compress
73 diffuse time=1 temp=900 nitro press=1.0
74 #
75
76 #
77 etch oxide left p1.x=0.2
78 deposit alumin thick=0.03 divi=2
79 etch alumin right p1.x=0.18
80 structure mirror right
81
82 electrode name=gate x=0.5 y=0.1
83 electrode name=source x=0.1
84 electrode name=drain x=0.9
85 electrode name=substrate backside
86
87 structure outfile=mos2ex08.str
88 #
89
90
91
92 go DevEdit
```

```
93
94
95 # Set Meshing Parameters
96 #
97 base.mesh height=1000000 width=1000000
98 #
99 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.points when=manual
100 #
101 imp.refine imp="NetDoping" sensitivity=1
102 imp.refine min.spacing=0.02
103 #
104 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
105 max.width=1 min.height=0.0001 min.width=0.0001
106 #
107 # Perform mesh operations
108 #
109 Mesh Mode=MeshBuild
110 refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
111 refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
112 refine mode=both x1=0.65 y1=0.26 x2=0.83 y2=0.34
113 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
114 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
115 refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
116 structure outf=mos2ex08_0.str
117
118 tonyplot mos2ex08_0.str -set mos2ex08_0.set
119
120
121 go atlas
122
123
124 # Set workfunction for poly gate and interface charge
125 contact name=gate n.polysilicon
126 interf qf=3E10
127 material taurel.el=0.2e-12 taumob.el=0.2e-12
128 # Set models
129 models print cvt consrh      lat.temp hcte.el
130 impact selb length.rel lrel.el=0.02
131
132
133 thermcontact num=1 x.min=0 x.max=1 y.min=0.799 y.max=0.802 alpha=3000
134
```

```

135 solve init
136
137 method newton trap
138 curvetrace end.val=1.5e-3 contr.name=drain curr.cont \
139 mincur=1e-13 nextst.ratio=1.2 step.init=6.e-3
140
141 solve vgate=0.025
142 solve vgate=0.1
143 solve vgate=0.5 vstep=0.25 vfinal=1 name=gate
144
145 # open log file
146
147 log outf=mos2ex08.log master
148
149 solve curvetrace
150 save outf=mos2ex08_1.str
151
152 tonyplot mos2ex08.log -set mos2ex08_log.set
153
154 quit

```

2.1.9. mos2ex09.in: Drain/Gate Overlap Capacitance

Requires: SSUPREM4/DEVEDIT/SPISCES

This example demonstrates the extraction of the gate overlap capacitance for an LDD MOSFET structure. The example shows:

- construction of an LDD MOSFET in ATHENA
- regrid of the structure in DEVEDIT
- gate/drain overlap capacitance extraction using AC analysis

A LDD NMOS device is constructed, remeshed and loaded into ATLAS. The process simulation, interface to DEVEDIT and initial setup in ATLAS are described in the previous section under MOS examples.

One requirement for AC simulation is that a two carrier solution must be specified. This is set with `method carriers=2`. After the initial solution, a solution at a gate bias of -2 volts is obtained using the local initial guess. The local method is convenient when taking large voltage steps, but assumes no current flow.

Next, the `log` statement is used to specify a file for saving the results of the gate ramp. Then, the gate is swept from -2 volts to 2 volts in 0.2 volt increments. At each static solution of gate bias the small signal AC response is solved at a frequency of 1 MHz. These results are saved in the log file. Finally, the overlap capacitance as a function of gate bias is plotted using TONYPLOT. In the list of XY graph variable in the TONYPLOT **display** menu the capacitances and conductances are listed as: `C electrode_name_1 > electrode_name_2`. This means the capacitance between these two electrodes. A similar construction is used with 'G' for conductance between two electrodes. When the two electrode names are the same, the magnitude of this value is the total capacitance on this electrode.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

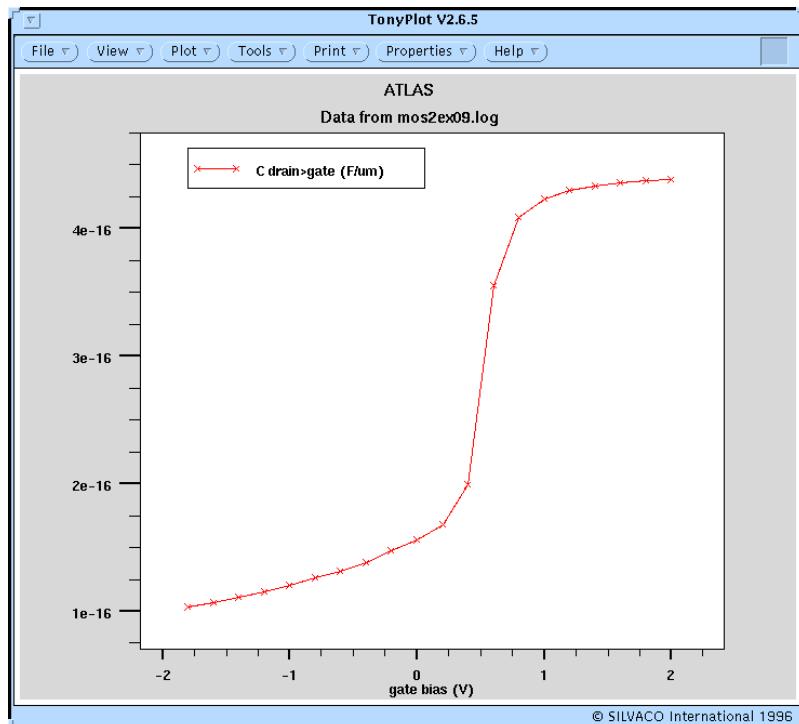


Figure 2.15: Gate/Drain overlap capacitance can be simulated to extract CGDO and other intrinsic capacitance SPICE Model parameters

Input File mos2/mos2ex09.in:

```
1 go athena
2 # LDD MOSFET Gate Overlap Capacitance Extraction
3 # SILVACO International 1996
4
5
6 #
7 line x loc=0 spac=0.1
8 line x loc=0.2 spac=0.01
9 line x loc=0.5 spac=0.01
10 #
11 line y loc=0.00 spac=0.01
12 line y loc=0.2 spac=0.01
13 line y loc=0.5 spac=0.05
14 line y loc=0.8 spac=0.15
15 #
16 init orientation=100 c.phos=1e14 space.mul=3
17
18 #pwell formation including masking off of the nwell
```

```
19 #
20 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
21 #
22 etch oxide thick=0.02
23 #
24 #P-well Implant
25 #
26 implant boron dose=8e12 energy=100 pears
27 #
28 diffus temp=950 time=100 weto2 hcl=3
29 #
30 #N-well implant not shown -
31 #
32 # welldrive starts here
33 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
34 #
35 diffus time=220 temp=1200 nitro press=1
36 #
37 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
38 #
39 etch oxide all
40 #
41 #sacrificial "cleaning" oxide
42 diffus time=20 temp=1000 dryo2 press=1 hcl=3
43 #
44 etch oxide all
45 #
46 #gate oxide grown here:-
47 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
48 #
49 #
50 extract thickness name="gateox" oxide mat.occno=1 min.v=140
51 #
52 #
53 #vt adjust implant
54 implant boron dose=9.5e11 energy=10 pearson
55 #
56 depo poly thick=0.2 divi=10
57 #
58 #from now on the situation is 2-D
59 #
60 etch poly left pl.x=0.35
61 #
```

```
62 method fermi compress
63 diffuse time=3 temp=900 weto2 press=1.0
64 #
65 implant phosphor dose=3.0e13 energy=20 pearson
66 #
67 depo oxide thick=0.120 divisions=8
68 #
69 etch oxide dry thick=0.120
70 #
71 implant arsenic dose=5.0e15 energy=50 pearson
72 #
73 method fermi compress
74 diffuse time=1 temp=900 nitro press=1.0
75 #
76 #
77 #
78 etch oxide left p1.x=0.2
79 deposit alumin thick=0.03 divi=2
80 etch alumin right p1.x=0.18
81 structure mirror right
82
83 electrode name=gate x=0.5 y=0.1
84 electrode name=source x=0.1
85 electrode name=drain x=0.9
86 electrode name=substrate backside
87
88 structure outfile=mos2ex09.str
89
90
91 go DevEdit
92
93
94 # Set Meshing Parameters
95 #
96 base.mesh height=1000000 width=1000000
97 #
98 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.points when=automatic
99 #
100 imp.refine imp="NetDoping" sensitivity=1
101 imp.refine min.spacing=0.02
102 #
103 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
```

```
104 max.width=1 min.height=0.0001 min.width=0.0001
105 #
106 # Perform mesh operations
107 #
108 Mesh Mode=MeshBuild
109 refine mode=y x1=0.34 y1=0.22 x2=0.65 y2=0.24
110 refine mode=y x1=0.35 y1=0.22 x2=0.67 y2=0.23
111 refine mode=both x1=0.65 y1=0.26 x2=0.82 y2=0.34
112 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.57
113 refine mode=y x1=0 y1=0.40 x2=1.0 y2=0.53
114 refine mode=y x1=0.80 y1=0.34 x2=1.0 y2=0.38
115
116 structure outf=mos2ex09_0.str
117
118 tonyplot mos2ex09_0.str -set mos2ex09_0.set
119
120 go atlas
121
122 # Set workfunction for poly gate and interface charge
123 contact name=gate n.polysilicon
124 interf qf=3E10
125
126 # Set models
127 models mos print
128
129 solve init
130
131 method newton trap
132
133 # initialise and ramp VGS to get GATE and OVERLAP CAPACITANCE
134 solve prev
135 solve vgate=-2 local
136 log outf=mos2ex09.log master
137 solve vstep=0.2 vfinal=2 name=gate ac freq=1e6 aname=gate
138
139 # plot results
140 tonyplot mos2ex09.log -set mos2ex09_log.set
141
142 quit
```

2.1.10. mos2ex10.in: 2D NMOS simulation from 1D SSUPREM3 Doping

Requires: SSUPREM3/SPISCES

This example demonstrates the interface between SSUPREM3 (1D process simulation) and ATLAS (2D device simulation). The main features are:

- run SSUPREM3 simulation of NMOS source/drain doping
- run SSUPREM3 simulation of NMOS channel
- combine two SSUPREM3 doping files into a 2D structure in ATLAS
- regrid the structure based on net doping level

The key syntax for reading the SSUPREM3 data into ATLAS are the doping statements. The parameters of the doping statement specifies the input filename, which dopant is to be used from the file and the 2D extent of the doping. The master parameter must be used to specify the data format of the SSUPREM3 result. Note that the old ssuprem3 parameter should *not* be used with versions of SSUPREM3 later than 5.0.

The lateral spread of the dopant in each doping statement is controlled by the RATIO.LAT parameter. This is a multiplier to the vertical rolloff.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

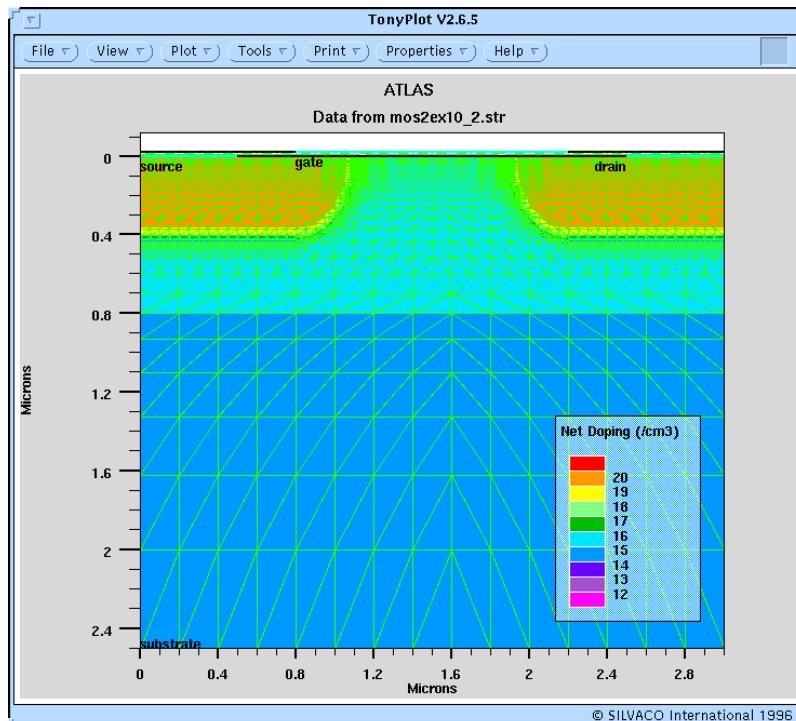


Figure 2.16: 2D NMOS Transistor defined in ATLAS syntax from 1D SSUPREM3 process simulations

Input File mos2/mos2ex10.in:

```

1 go ssuprem3
2 TITLE:      NMOS Silicon Gate Example
3 #          Active device region initial processing.
4

```

```
5 # Initialize silicon substrate.
6 Initialize <100> Silicon c.boron=1e15 Thick=1.5 \
7 dx=.005 xdx=.02 Spaces=150
8
9 # Grow pad oxide, 400A.
10 Diffusion Temperature=1000 Time=40 DryO2
11
12 # Deposit 800A of CVD Nitride.
13 Deposit Nitride Thickness=.0800 Spaces=15
14
15 # Grow field oxide.
16 Diffusion Temperature=1000 Time=180 WetO2
17
18
19 # Etch to silicon surface.
20 Etch Oxide all
21 Etch Nitride all
22 Etch Oxide all
23
24 # Implant boron to shift the threshold voltage.
25 Implant Boron Dose=4e11 Energy=50
26
27 # Grow gate oxide in dry oxygen ambient with 3% HCl.
28 Diffusion Temperature=1050 Time=30 DryO2 HCL%=3
29
30 # Deposit polysilicon
31 Deposit Polysilicon Thickness=0.5 Temperature=600
32
33 # Heavily dope the polysilicon using POCl3
34 Diffusion Temperature=1000 Time=25 dTmin=.3 \
35 Phosphorus Solidsolubility
36
37 # Save the structure at this point. The simulation runs
38 # are split for the gate and source/drain regions.
39 structure outfile=mos2ex10.str
40
41 # Carry on processing the Source/drain regions.
42
43 # Etch polysilicon and oxide over source/drain regions.
44 Etch Polysilicon
45 Etch Oxide
46
47 # Implant Arsenic for source/drain regions.
```

```
48 Implant      Arsenic Dose=5E15 Energy=150
49
50 #           Drive-in Arsenic and re-oxidize source/drain regions.
51 Diffusion    Temperature=1000 Time=30 DryO2
52
53 #           Etch contact holes to gate, source, and drain regions.
54 Etch        oxide
55
56 #           Deposit Phosphorus doped SiO2 using CVD.
57 Deposit     Oxide Thickness=.7500 Phosphorus Concentration=1e21
58
59 #           Reflow glass to smooth surface and dope contact holes.
60 Diffusion    Temperature=1000 Time=30
61
62 #           Reopen contact holes.
63 Etch        Oxide
64
65 #           Deposit Aluminum.
66 Deposit     Aluminum Thickness=1.2 Spaces=10
67
68 #           Save the structure.
69 structure   outfile=mos2ex10_0.str
70
71 #           Process the gate region.
72
73 #           Initialize previously saved structure
74 Initialize  infile=mos2ex10.str
75
76 #           Implant Arsenic for source/drain regions.
77 Implant     Arsenic Dose=5E15 Energy=150
78
79 #           Drive-in Arsenic and re-oxidize source/drain regions.
80 Diffusion    Temperature=1000 Time=30 DryO2
81
82 #           Etch contact holes to gate, source, and drain regions.
83 Etch        Oxide
84
85 #           Deposit Phosphorus doped SiO2 using CVD.
86 Deposit     Oxide Thickness=.75 Phosphorus Concentration=1.E21
87
88 #           Reflow glass to smooth surface and dope contact holes.
89 Diffusion    Temperature=1000 Time=30
90
```

```
91 # Reopen contact holes.
92 Etch Oxide
93
94 # Deposit Aluminum.
95 Deposit Aluminum Thickness=1.2 Spaces=10
96
97 # Save the structure.
98 Structure outfile=mos2ex10_1.str
99
100
101 go atlas
102
103 # N-channel MOSFET grid generation from SSUPREM3 doping
104
105 # Form grid of the structure and give doping distribution
106
107 # define rectangular grid
108 mesh rect diag.flip
109 x.mesh l=0 spac=0.1
110 x.mesh l=3.0 spac=0.1
111 y.mesh l=-0.02 spac=0.01
112 y.mesh l=0 spac=0.01
113 y.mesh l=0.7 spac=0.1
114 y.mesh l=2.5 spac=0.5
115
116 # eliminate substrate mesh
117 elim columns y.min=0.7
118
119 # regions
120
121 region num=1 y.max=0 oxide
122 region num=2 y.min=0 silicon
123
124 # electrodes
125
126 electrode num=1 name=gate x.min=0.8 length=1.4
127 electrode num=2 name=substrate substrate
128 electrode num=3 name=source left length=0.5 y.min=0 y.max=0
129 electrode num=4 name=drain right length=0.5 y.min=0 y.max=0
130
131 # doping and fixed charge
132
133 doping master inf=mos2ex10_1.str boron outfile=mos2ex10.dat
```

```
134 doping      master inf=mos2ex10_0.str arsenic x.right=0.8 ratio=0.75
135 doping      master inf=mos2ex10_0.str arsenic x.left=2.2   ratio=0.75
136
137 # regrid on doping
138
139 regrid      doping log reg=2 ratio=4 smooth.k=4 dopfile=mos2ex10.dat
140 regrid      doping log reg=2 ratio=4 smooth.k=4 dopfile=mos2ex10.dat
141
142 savefile outfile=mos2ex10_2.str
143 tonyplot mos2ex10_2.str -set mos2ex10.set
144
145 quit
146
```

2.1.11. mos2ex11.in: Breakdown Voltage using Ionization Integrals

Requires: SSUPREM4/SPISCES

This example uses a standard NMOS structure similar to that used in the MOS1 section. In this example the ATLAS simulation is done using zero carriers. The breakdown voltage is extracted using **ionization integrals** or **electric field lines**

The **solve** statement used to ramp the drain electrode has extra parameters for calculating the ionization integrals at each step. When using ionization integrals, it is not necessary to solve for both carriers so simulations are very quick. However, the statement, **impact selb**, must be used to activate the ionization rate calculation.

The syntax of the **solve** statement sets the number of ionization integrals, their position relative to the ramped contact (ie. drain), and the voltage drop from the contact to the start point of the electric field lines. Details of the syntax can be found in the ATLAS User Manual. In summary **deltav** controls the distance of the start of each electric field line from the ramped contact. **ionlines** controls the number of electric field lines calculated **lratio** controls the spacing ratio between each line. **Lratio <1.0** means more lines to the left of the contact. **Lratio >1.0** means more lines to the right.

The breakdown voltage is defined as the point at which the ionization integrals are equal to 1.0. Although the **solve** statement specifies a voltage ramp to 50V, the bias ramp will automatically stop when the ionization integrals exceed 1.0. The parameter, **^ionstop**, can be included to disable this feature. If the position of the electric field lines are chosen correctly the electron and hole ionization integrals should equal 1.0 at the same voltage. If this is not the case, users should check the position of the electric field lines.

The **output** statement is used to specify the electric field line parameters for the saved solution file. Note that users must specify these parameters on the output as well as solve statements to save the electric field lines. The lines can be plotted in TONYPLOT by selecting the **Lines** icon from the **Plot/display** menu.

Following the simulation, the peak electric field is extracted from the solution file. The **extract** statement also reports the XY position of the peak. See the Simulation Standard Hints and Tips page for August 1996 for more details.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

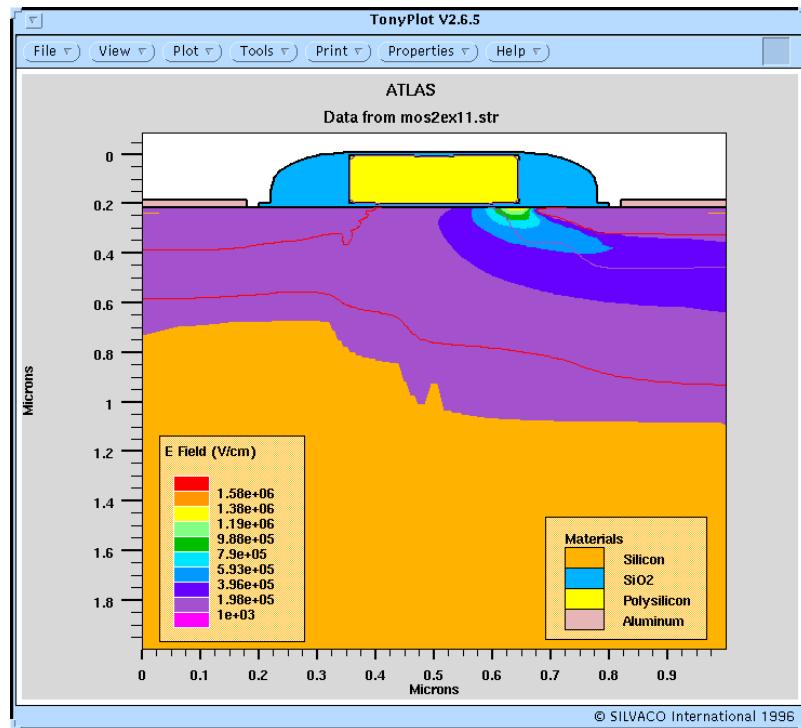


Figure 2.17: Contours of Electric field in a MOSFET at breakdown. A zero carrier solution was used in the simulation

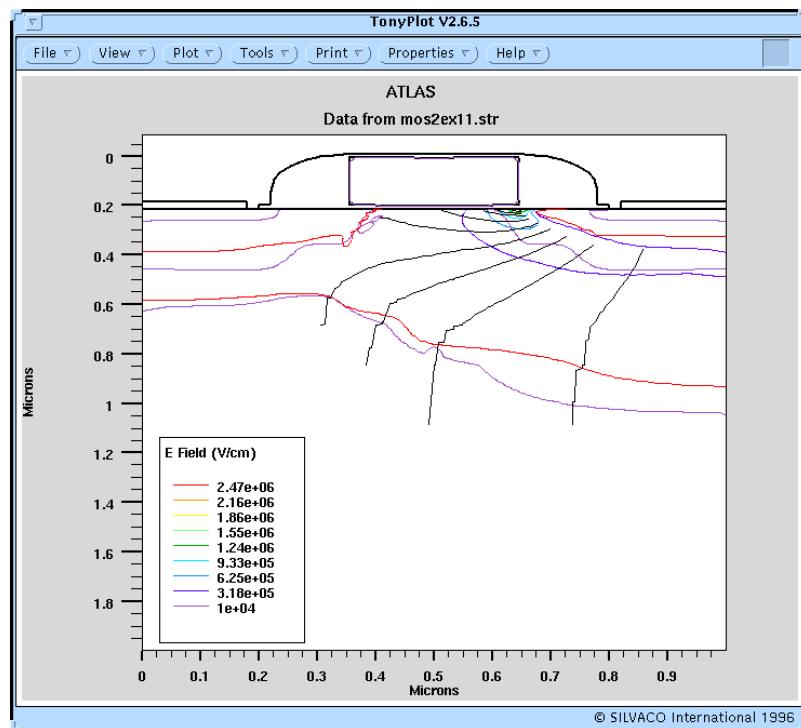


Figure 2.18: Electric field lines displayed with electric field contours, junctions and depletion edges. Ionization rate is integrated along each field line to determine the ionization integral

Input File mos2/mos2ex11.in:

```
1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.2 spac=0.006
5 line x loc=0.4 spac=0.006
6 line x loc=0.5 spac=0.01
7 #
8 line y loc=0.00 spac=0.002
9 line y loc=0.215 spac=0.001
10 line y loc=0.5 spac=0.05
11 line y loc=2.0 spac=0.5
12
13 init orientation=100 c.phos=1e14 space.mul=2
14
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=8e12 energy=100 pears
24
25 #
26 diffus temp=950 time=100 weto2 hcl=3
27 #
28 #N-well implant not shown -
29 #
30 # welldrive starts here
31 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
32 #
33 diffus time=220 temp=1200 nitro press=1
34 #
35 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
36 #
37 etch oxide all
38 #
39 #sacrificial "cleaning" oxide
40 diffus time=20 temp=1000 dryo2 press=1 hcl=3
41 #
42 etch oxide all
```

```
43 #
44 #gate oxide grown here:-
45 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
46
47 # Extract a design parameter.
48
49 extract name="gateox" thickness oxide mat.occno=1 x.val=0.49
50 #
51 #vt adjust implant
52 implant boron dose=9.5e11 energy=10 pearson
53
54 #
55 depo poly thick=0.2 divi=10
56 #
57 #from now on the situation is 2-D
58 #
59 etch poly left p1.x=0.35
60 #
61 method fermi compress
62 diffuse time=3 temp=900 weto2 press=1.0
63 #
64 implant phosphor dose=3.0e13 energy=20 pearson
65 #
66 depo oxide thick=0.120 divisions=8
67 #
68 etch oxide dry thick=0.120
69 #
70 implant arsenic dose=5.0e15 energy=50 pearson
71 #
72 method fermi compress
73 diffuse time=1 temp=900 nitro press=1.0
74 #
75
76 #
77 etch oxide left p1.x=0.2
78 deposit alumin thick=0.03 divi=2
79 etch alumin right p1.x=0.18
80
81
82 # Extract another design parameters...
83 # extract final S/D Xj...
84 extract name="nxj" xj silicon mat.occno=1 x.val=0.1 junc.occno=1
85 # extract the long chan Vt...
```

```
86 extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.49
87 # extract a curve of conductance versus bias
88 extract start material="Polysilicon" mat.occno=1 bias=0.0 bias.step=0.2
     bias.stop=2 x.val=0.45
89 extract done name="sheet cond v bias" curve(bias,ldn.conduct material=
     "Silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
90 # extract the N++ regions sheet resistance...
91 extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1
     x.val=0.05 region.occno=1
92 # extract the sheet rho under the spacer, of the LDD region...
93 extract name="ldd sheet rho" sheet.res material="Silicon" mat.occno=1
     x.val=0.3 region.occno=1
94 # extract the surface conc under the channel
95 extract name="chan surf conc" surf.conc impurity="Net Doping" material=
     "Silicon" mat.occno=1 x.val=0.45
96
97 structure mirror right
98
99 electrode name=gate x=0.5 y=0.1
100 electrode name=source x=0.1
101 electrode name=drain x=0.9
102 electrode name=substrate backside
103
104
105 ### start Atlas from here ###
106 go atlas
107
108 # define the Gate workfunction
109 contact name=gate n.poly
110
111 # Define the Gate Qss
112 interface qf=3e10
113
114 # Use the cvt mobility model for MOS
115 models cvt srh
116 impact selb
117
118 method carr=0
119
120 solve vdrain=0.25 vstep=0.25 vfinal=50.0 name=drain ioniz ionlines=100
     lratio=0.7 deltav=0.7
121
122 output      e.field e.lines iname=drain n.lines=100 lratio=0.7 deltav=0.7
123 save        outf=mos2ex11.str
124
```

```

125 tonyplot mos2ex11.str -set mos2ex11.set
126
127 # Extract the maximum electric field value and x,y postition, from the
128 # current solution.
129 extract init inf="mos2ex11.str"
130 extract name="max electric field" 2d.max.conc impurity="E Field" \
131 material="Silicon" x.min=0.6 x.max=1.3 y.min=0 y.max=0.5
132 extract name="xposition of max field" x.pos
133 extract name="yposition of max field" y.pos
134
135
136
137

```

2.1.12. mos2ex12.in: SiGe PMOS Process and Device Simulation

Requires: FLASH/ELITE/BLAZE

This example demonstrates the interface from process to device simulation for a SiGe PMOS structure. Physical deposition and etch models are used to provide realistic topography. It shows:

- PMOS process simulation using ATHENA
- specification of Ge mole fraction in ATHENA
- use of ELITE deposition and etching for contact topography
- definition of SiGe dopants
- interface to ATLAS
- saving and plotting of the band structure for the SiGe/Si heterojunction.
- Id/Vgs characteristic using ATLAS

In this example a SiGe MOSFET structure is formed using process simulation. This contrasts with the previous examples in this section. To repeat the electrical analysis of the previous examples using this structure the ATLAS simulation of this example should be replaced with the ATLAS syntax for parameter settings, model selection, numerical methods and solve sequences from the previous examples.

The simulation of SiGe structures in ATHENA is similar to pure silicon MOSFET structures documented under the MOS examples section. The differences described here are limited to the special syntax needed for SiGe.

The Ge mole fraction in the deposited SiGe film is set by the `c.frac` parameter on the deposit statement.

In FLASH it is necessary to define whether a dopant is donor or acceptor explicitly for each material. The command,

```
impurity i.boron acceptor sige
```

is used to set boron as a p-type dopant in SiGe. A similar command is used to define phosphorus as a donor.

The interface from ATHENA to ATLAS is simply the `go atlas` statement. It saves the structure from ATHENA and transfers it to ATLAS. No `mesh` statement is needed at the start of the ATLAS run. The `electrode` statement in ATHENA is required to identify which regions are defined as electrodes in ATLAS.

The ATLAS run in this file is very simple. It solves only a single bias point with $V_{ds}=2.0V$. To save the band structure, the command, `output con.band val.band`, is used. This tells ATLAS to save the conduction and valence band edge energies to any solution files saved using `save`. The final structure in ATLAS is displayed using TONYPLOT. The band diagram can be seen by taking a vertical 1D cross section in TONYPLOT, selecting the 1D plot and changing the display variables from the scrolling list to be the two band edges.

Note: For details on more complex applications of SiGe MOSFETs, users should consult the other MOS examples. All S-PISCES analysis in these sections can be applied under BLAZE to SiGe MOSFETs.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

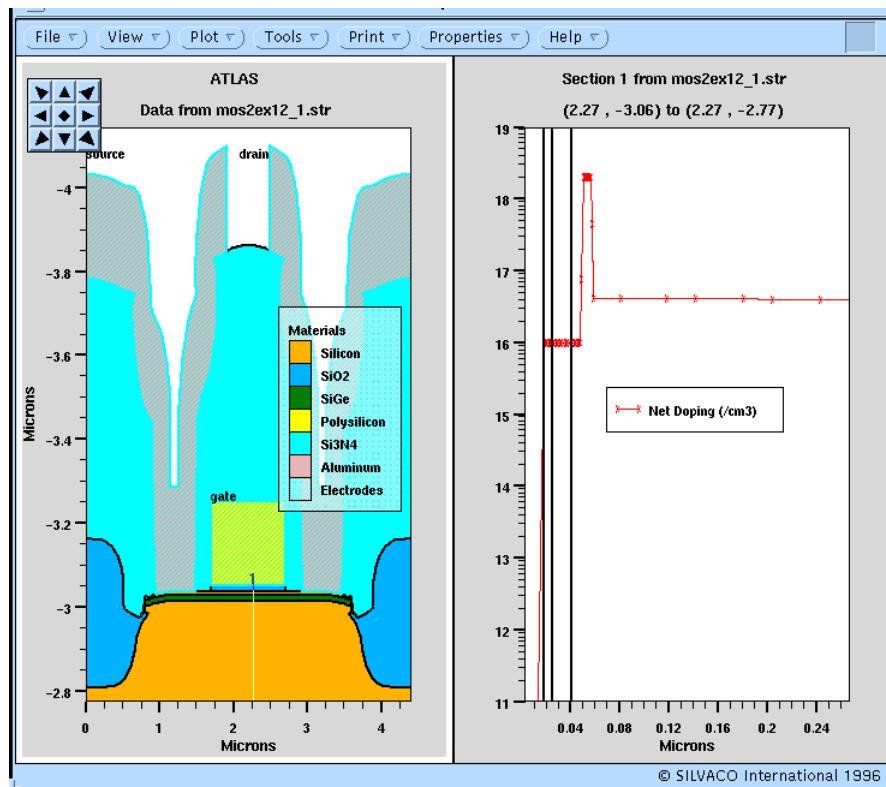


Figure 2.19: SiGe MOSFET simulated in ATHENA. The 1D plot (right) shows the doping profile with doped layer under the channel.

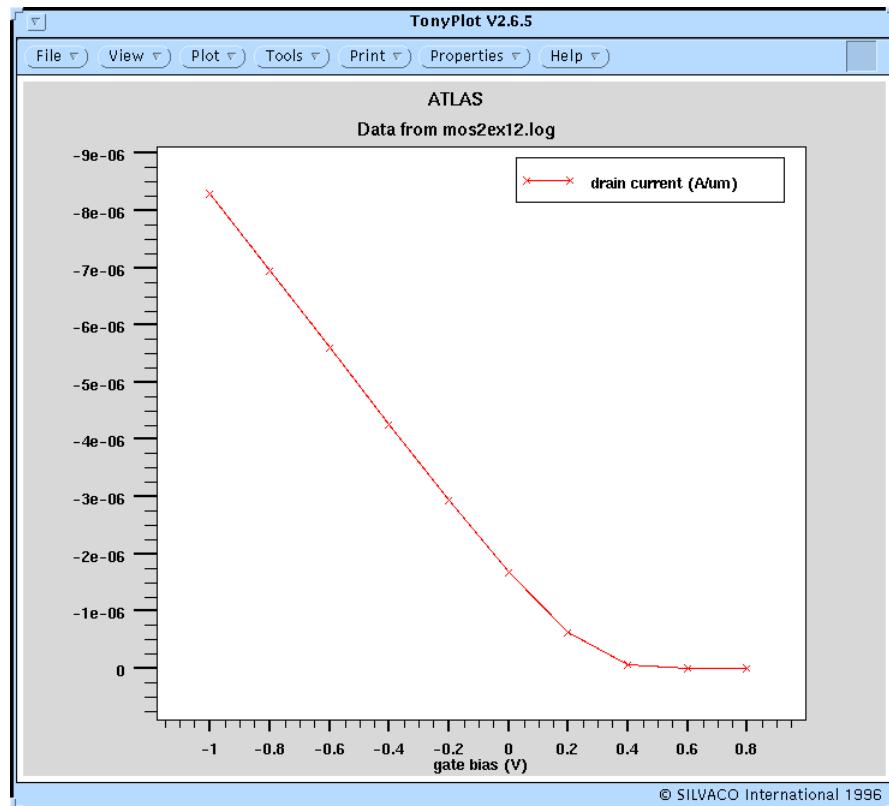


Figure 2.20: Threshold voltage curve for the SiGe PMOSFET

Input File mos2/mos2ex12.in:

```

1 go athena
2 # SiGe MOS simulation
3 # SILVACO International 1996
4
5 # Establish initial grid and substrate material
6 line x location=0.0    spacing=0.1
7 line x location=0.5    spacing=0.05
8 line x location=0.75   spacing=0.1
9 line x location=1.7    spacing=0.05
10 line x location=2.2   spacing=0.05
11
12 line y location=0.0   spacing=0.5
13 line y location=1.0   spacing=0.5
14
15 init silicon c.phos=2e18
16
17 epitaxy thick=2.5 divis=6 c.phos=4e16 time=25 temp=800
18 epitaxy thick=0.5 divis=8 c.phos=4e16 time=5   temp=800
19
20

```

```
21 diff time=20 temp=900 dryo2
22
23 deposit nitride thick=.35
24
25 etch nitride left p1.x=0.5
26
27 relax y.min=-2.5 dir.y=f
28 relax y.min=-2.5 dir.y=f
29
30
31 method grid.ox=0.05
32 diffuse time=60 temp=1000 weto2
33
34 strip nitride
35 etch oxide thick=0.05
36
37
38 # create the effect of selective epitaxy by
39 # depositing and then removing from atop oxide
40
41 # Deposit Silicon and Silicon Germanium layers
42 deposit silicon thick=0.008 divis=4 c.boron=2e18
43 deposit silicon thick=0.010 divis=4 c.phos=1e16
44 deposit sige thick=0.015 divis=5 c.frac=0.35 c.phos=1e16
45 deposit silicon thick=0.007 divis=4 c.phos=1e16
46
47 deposit photo thick=.4 divis=5
48 etch photo left x=0.75
49
50 # define the etch rates
51 rate.etch machine=test rie n.m silicon isotropic=20.0 directional=20.0
52 rate.etch machine=test rie n.m sige isotropic=20.0 directional=20.0
53 rate.etch machine=test rie n.m oxide isotropic=0.0 directional=5.0
54
55 # perform the etch
56 etch mach=test time=4. minutes dx.mult=0.25
57
58
59 strip
60
61
62 # deposit gate oxide to get exact thickness
63 deposit oxide thick=0.016
```

```
64
65
66 # Deposit poly for the gate
67
68 deposit poly thick=0.2 divis=8 c.phos=1.e15
69
70 # Pattern the gate
71 etch poly      left p1.x=1.7
72 etch oxide     thick=0.02
73
74 # implant source drain
75 implant boron dose=1e15 energy=20
76
77
78 rate.depo machine=BPSG nitride u.m sigma.dep=0.20 smooth.win=0.5 \
79           smooth.step=1 unidirec dep.rate=1.0 angle1=0.00
80
81 deposit machine=BPSG time=0.7 minute divis=5
82
83 deposit photo thick=.75 divis=4
84
85 etch photo    start x=0.9 y=10.
86 etch          cont  x=0.9 y=-10.
87 etch          cont  x=1.5 y=-10.
88 etch          done   x=1.5 y=10.
89
90
91 rate.etch machine=test1 nitride u.m wet.etch isotropic=0.3
92 etch machine=test1 time=1. minutes dx.mult=0.2
93
94 rate.etch machine=test2 nitride u.m rie      direct=0.3
95 etch machine=test2 time=1.5 minutes
96
97 strip
98
99 # Deposit and pattern the contact metal
100 deposit aluminum thick=.25 divis=2
101
102
103 etch aluminum right p1.x=1.9
104
105
106 # reflect the structure
```

```
107 structure right mirror
108
109
110 # Define the electrodes
111 electrode      name=source   left
112 electrode      name=drain    right
113 electrode      name=gate     x=2.5 y=-3.1
114 electrode      name=substrate backside
115
116 # Define impurity as acceptor or donor in SiGe material
117
118 impurity i.boron acceptor sige
119 impurity i.phos   donor    sige
120
121
122 structure outfile=mos2ex12_0.str
123
124
125 go atlas
126
127 # Material parameter, model, method, and output specification
128
129 material material=Si      taun0=1e-7  taup0=1e-7
130 material material=SiGe   taun0=1.e-8 taup0=1.e-8
131 model      bgn  consrh  auger fldmob connmob print
132
133 contact name=gate n.polysilicon
134
135 # use newton method
136 method newton
137
138 # Perform zero bias solution
139 solve
140
141 # Save the structure with band diagram and plot it
142 output con.band val.band
143 save outf=mos2ex12_1.str
144 tonyplot mos2ex12_1.str -set mos2ex12.set
145
146 solve vgate=1.0
147 solve vdrain=-0.1
148
149 log outf=mos2ex12.log
```

```

150 solve vstep=-0.2 vfinal=-1.0 name=gate
151
152 tonyplot mos2ex12.log
153
154 quit
155

```

2.1.13. mos2ex13.in: SiGe PMOS Id/Vds with NEB Model

Requires: BLAZE/GIGA

This example demonstrates a comparison of Id/Vds analyses including second breakdown of a short PMOS structure with a SiGe channel using the non-isothermal Energy Balance (NEB) models. It shows:

- specification of PMOS structure using ATLAS syntax
- specification of abrupt SiGe heterojunctions
- selection of the energy balance model, lattice heat flow solution and coupled solve
- simulation of Id/Vds characteristic for Vgs=-1.0V

Many of the models and methods required for Id/Vds and breakdown simulation are described in the snapback and second breakdown examples in the MOS examples section. Some tips in defining SiGe structures are also given in the HBT examples section. Users should consult both these sections for more details on these two areas.

Submicron devices should be simulated using the energy balance model due to velocity overshoot, and nonlocal impact ionization effects, which could substantially influence device characteristics. For high current levels the thermal self-heating effects could also play an important role decreasing mobility and impact ionization rate. This example demonstrates comparison of Id/Vds curves obtained with energy balance and nonisothermal energy balance models. The curve tracing algorithm is used to obtain these curves.

The example contains two ATLAS runs. The first uses non-isothermal energy balance simulation of an Id/Vds curve and the second repeats this simulation without the lattice heating model.

In the first part of the input file the device is described, including mesh, regions locations, electrodes locations, and doping distribution. The `region` statements are used to define SiO₂, Si and SiGe regions. The Ge composition fraction is defined using `x.composition=<num>`. Since no `grad.*` parameters were used on the `region` statement, the Ge composition fraction has an abrupt change from 0.25 to zero at the region boundary. This constitutes the abrupt heterojunction. Discontinuities in band potentials will be seen at the SiGe/Si region boundaries.

After the device description, the `material` statements are used to specify the electron and hole lifetimes, hole energy relaxation times both in Si and SiGe, and N_c and N_v in SiGe. The `model hcte.ho lat.temp` statement is used to specify solution of the hole energy balance and lattice heating equations respectively. Other carrier and lattice temperature physical models are also set on the same statement. The `impact` statement is used to assign the energy relaxation length for Selberherr model.

Thermal boundary conditions are defined in the `thermcontact` statement. A value of the thermal resistance is specified at the thermocontact located along the substrate, and thermal isolation conditions are assumed on the all other surfaces.

Then the gate voltage is ramped to -2V. After that the curve tracing algorithm is used for ramping the drain voltage. The `curvetrace` statement is used to initialize parameters for the curve tracing algorithm. The `contr.name` parameter specifies the name of the electrode for which the load line technique will be applied (drain in this case). The `curr.cont` parameter means that value of current

will be monitored, and the simulation will be stopped when the current exceeds the value specified by end.val parameter. The mincur parameter defines the minimum current value after which the load line technique will actually be applied (before that voltage boundary conditions are used). The nextst.ratio parameter defines the factor which to use to increase voltage step on the smooth parts of the IV curve. The command, solve curvetrace, is used to activate the curve tracing algorithm.

The second ATLAS run uses the same syntax, except that the solution of the lattice energy balance equation is turned off in the models statement. The Id/Vds curves from both runs can be overlaid using TONYPLOT. In plotting the drain voltage the quantity, drain int. bias should be used in TONYPLOT. This is the value of the voltage on the metal/semiconductor interface at the drain as opposed to 'drain bias' which includes the load resistor used in the curve trace algorithm.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

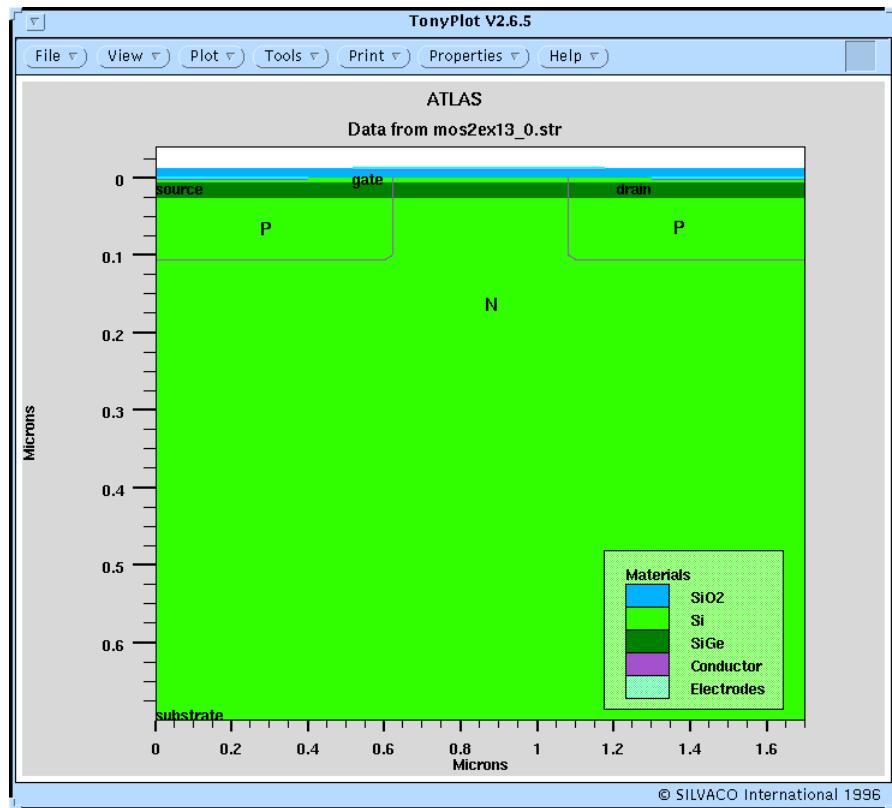


Figure 2.21: SiGe MOSFET defined using ATLAS syntax.

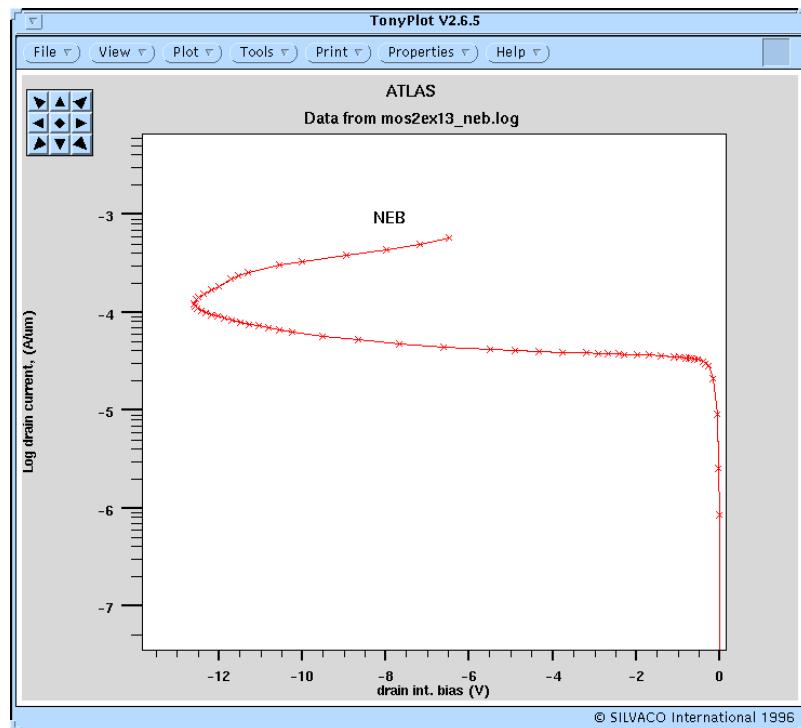


Figure 2.22: Breakdown curve of SiGe PMOS device using lattice heating and energy balance models

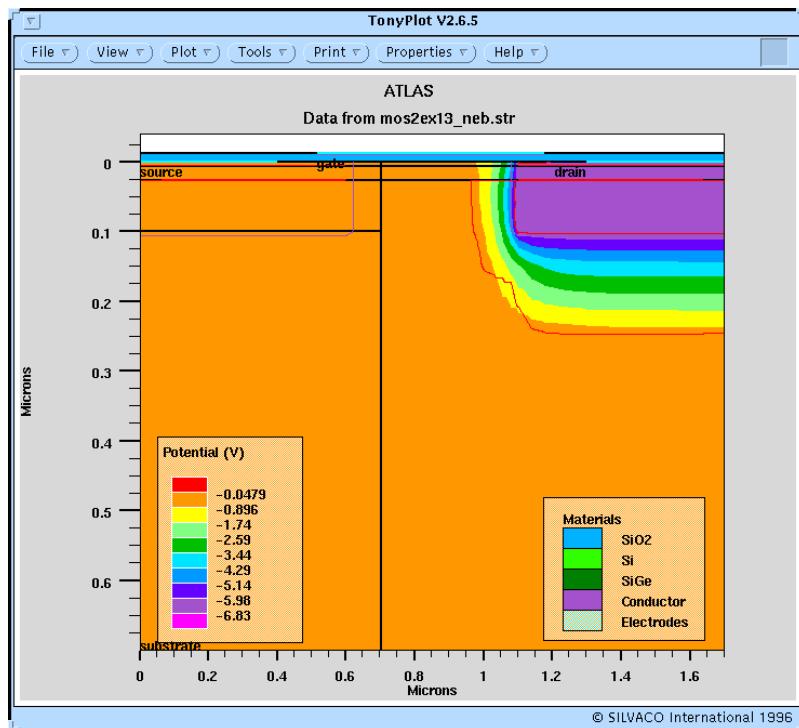


Figure 2.23: Potential contours at the breakdown point in the SiGe PMOSFET

Input File mos2/mos2ex13.in:

1 go atlas

```
2 TITLE SiGe PMOS Id-Vd simulation with Energy Balance
3 # and Nonisothermal Energy Balance Models
4 # SILVACO International 1996
5
6
7 mesh nx=34 ny=41
8
9 x.m n=1 l=0.00 r=1.0
10 x.m n=4 l=0.4 r=1.0
11 x.m n=10 l=0.6 r=0.9
12 x.m n=18 l=0.85 r=1.1
13 x.m n=26 l=1.1 r=0.9
14 x.m n=31 l=1.3 r=1.02
15 x.m n=34 l=1.7 r=1.0
16
17
18 y.m n=1 l=-0.012 r=1.0
19 y.m n=3 l=0.0000 r=1.0
20 y.m n=8 l=0.005 r=1.0
21 y.m n=13 l=0.007 r=1.0
22 y.m n=20 l=0.025 r=1.0
23 y.m n=25 l=0.027 r=1.0
24 y.m n=30 l=0.08 r=1.0
25 y.m n=33 l=0.10 r=1.0
26 y.m n=37 l=0.15 r=1.5
27 y.m n=41 l=0.7 r=1.3
28
29
30
31 region num=1 material=SiO2 x.min=0 x.max=1.7 y.min=-0.012 y.max=0.0
32 region num=2 material=Si y.min=0. y.max=0.006 x.min=0. x.max=0.7
33 region num=3 material=Si y.min=0. y.max=0.006 x.min=0.7 x.max=1.7
34 region num=4 material=SiGe y.min=0.006 y.max=0.026 x.min=0 x.max=0.7 \
35 x.composition=0.25
36 region num=5 material=SiGe y.min=0.006 y.max=0.026 x.min=0.7 \
x.max=1.7 \
37 x.composition=0.25
38 region num=6 material=Si y.min=0.026 y.max=0.1 x.min=0. x.max=0.7
39 region num=7 material=Si y.min=0.1 y.max=0.7 x.min=0. x.max=0.7
40 region num=8 material=Si y.min=0.026 y.max=0.7 x.min=0.7 x.max=1.7
41
42
43
```

```

44
45 elec      num=1   name=source x.min=0.0 x.max=0.4 y.min=0.00 y.max=0.00
46 elec      num=2   name=gate   x.min=0.5 x.max=1.2 y.min=-0.012 y.max=-0.012
47 elec      num=3   name=drain  x.min=1.3 x.max=1.7 y.min=0.00 y.max=0.00
48 elec      num=4   name=substrate x.min=0 x.max=1.7 y.min=0.7 y.max=0.7
49
50
51
52
53 doping    uniform n.type conc=1.e12 x.left=0.6 x.right=1.1 y.top=0 y.bot-
     tom=0.026
54 doping    uniform n.type conc=1.e17 x.left=0.6 x.right=1.1 y.top=0.026
     y.bottom=0.7
55 doping    uniform n.type conc=1.e17 x.left=1.1 x.right=1.7 y.top=0.1
     y.bottom=0.7
56 doping    uniform n.type conc=1.e17 x.left=0. x.right=0.6 y.top=0.1
     y.bottom=0.7
57 doping    uniform p.type conc=5.e19 x.left=0 x.right=0.6 y.top=0.0 y.bot-
     tom=0.1
58 doping    uniform p.type conc=5.e19 x.left=1.1 x.right=1.7 y.top=0.0
     y.bottom=0.1
59
60
61 thermcontact num=1   x.min=0 x.max=1.7 y.min=0.7 y.max=0.7 alpha=300
62
63
64 material material=Si   taun0=1.e-7 taup0=1.e-7 \
65           taurel.ho=2.e-13 taumob.ho=2.e-13
66 material material=SiGe   taun0=1.e-7 taup0=1.e-7 \
67           nv300=1.55e19 nc300=2.86e19 \
68           taurel.ho=2.e-13 taumob.ho=2.e-13
69
70
71 models   conmob bgn fldmob hcte.ho lat.temp consrh auger print
72 impact   selb length.rel lrel.ho=0.02
73
74 contact  number=2 n.polysilicon
75
76
77 solve
78
79 output con.band val.band h.velocity
80 save outf=mos2ex13_0.str
81 tonyplot mos2ex13_0.str -set mos2ex13_0.set
82

```

```
83
84
85 # Calculations with NEB model
86
87 # Ramp gate to -2V
88
89 method block newton temp.tol=1.e-4 trap
90
91
92 solve vgate= 0.0 vstep=-1 name=gate vfinal=-2
93
94 # Id-Vd calculations
95
96 method newton temp.tol=1.e-4 trap
97 curvetrace end.val=-5.e-4 contr.name=drain step.init=-0.01 \
98 curr.con mincur=5e-12 nextst.ratio=1.2
99
100 log outf=mos2ex13_neb.log master
101 solve curvetrace
102 save outf=mos2ex13_neb.str
103
104
105 tonyplot mos2ex13_neb.log -set mos2ex13_1.set
106 tonyplot mos2ex13_neb.str -set mos2ex13_2.set
107
108 quit
109
110
111
112
113
```

2.1.14. mos2ex14.in: Comparison of CVT, SHIRAHATA and WATT Mobility Models

Requires: S-PISCES

The example demonstrates a comparison between three different surface mobility models used in MOSFETs. The example consists of four ATLAS runs that:

- define optimum MOS mesh using a variable for surface mesh spacing
- select in turn one of three MOS Mobility Models
- run a Id/Vgs simulation at low Vds
- overlay of Id/Vgs curves and mobility in TONYPLOT

The mesh generation and structure definition part of this input file follows that standard syntax outlined in the Getting Started Chapter of the ATLAS manual. The variable, `surf_a`, is used to

set the mesh spacing at the silicon surface. This mesh spacing is important to resolve the high electric field and carrier concentration gradients at the surface. The sensitivity of the mobility models to mesh variations can also be easily examined by re-running this example with different settings of `surf_a`.

The three models compared in this example are *CVT*, *Shirahata* and *Modified Watt*. The *CVT* model is selected simply with the syntax,

```
models cvt
```

since it contains doping and parallel field dependence. The *Shirahata* model contains only a perpendicular field dependence. It must be combined with *Klaassen's* model and the standard field dependent mobility model using

```
models kla shi fldmob.
```

The modified *Watt* model also needs to be combined with other models. The syntax is:

```
models commob fldmob
mobility watt.n mod.watt.n
```

Extra parameters are also required to determine the range of the modified *Watt* model. These parameters are `ymaxn.watt` that specifies the depth of the *Watt* model and `min.surf` that specifies the lateral extent by restricting the model to minority regions. Here, this means the channel and not the LDD or source and drain regions.

The *Id/Vgs* simulation is similar to that in the previous section. For the initial drain biasing, the syntax, `mehod gummel newton`, is used. This provides better convergence at low biases. Once the drain is biased, the simulation reverts to `method newton`. Note that in this case only electrons are needed. The syntax, `method carriers=1 electrons`, is used to select only electron continuity and poisson equations are to be solved.

The `probe` statement is used to save the surface mobility and perpendicular field at the center of the channel. Values for both these parameters are saved to the `log` file. *TONYPLOT* can be used to display graphs of mobility vs. field. Note that the `probe` statement reports the exact mobility used in *ATLAS* calculations. The value is calculated at the center of the side of each triangle. The nearest such point to the location of the probe is used. Values of mobility or field from the probe might differ from values saved in the solution file. The solution file saves the average value of such quantities at a node point. With coarse or bad meshes, this may result in inaccurate plots.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into *DeckBuild*, select the **run** button to execute the example.

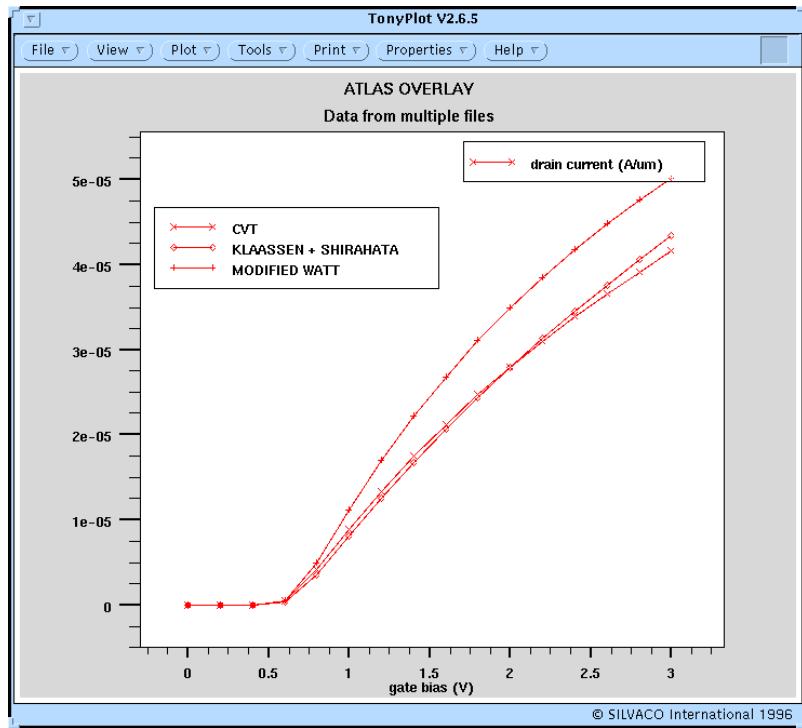


Figure 2.24: Comparison of I_d/V_g curve for three surface mobility models

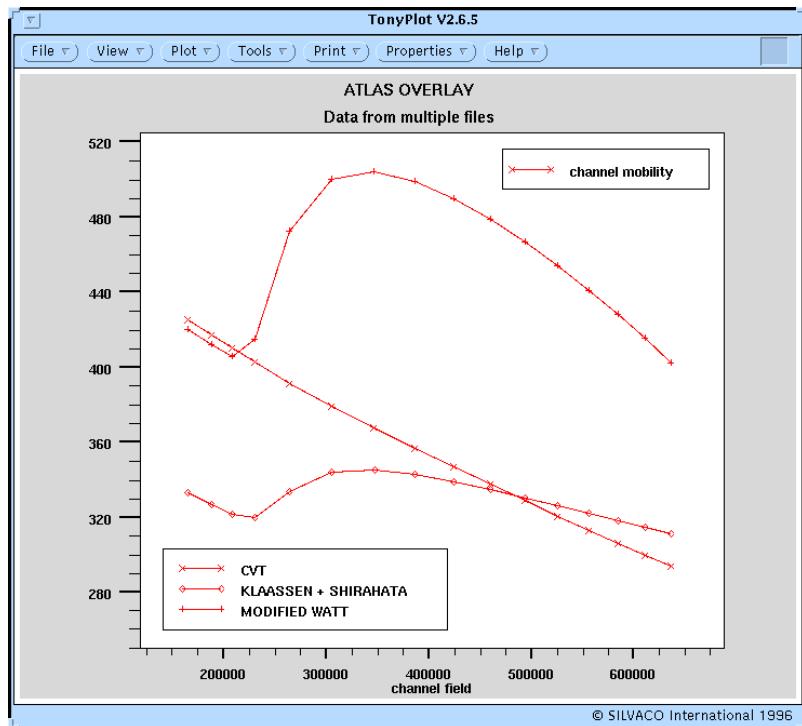


Figure 2.25: Channel Mobility versus Field plots extracted using the PROBE statement

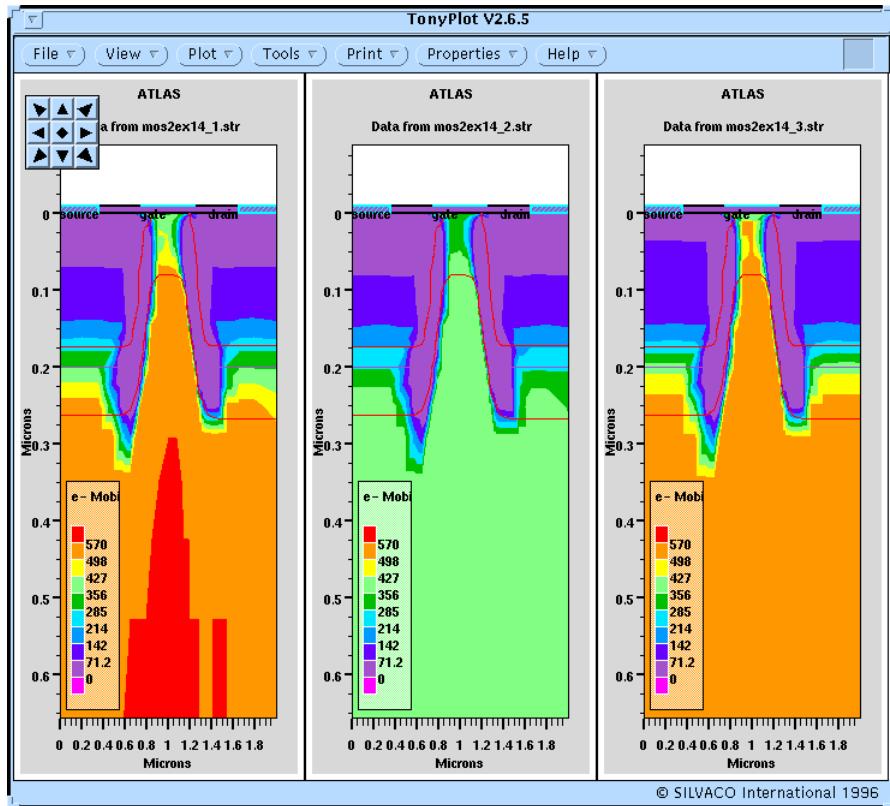


Figure 2.26: 2D contours of Mobility for CVT(left), SHI(center) and MOD.WATT(right) models. Although mobility can be plotted in 2D, the PROBE statement is best for getting accurate values for every bias point.

Input File mos2/mos2ex14.in:

```

1 go atlas
2
3 # define fine mesh at surface
4 set surf_a=0.0005
5
6 mesh outf=mmos.str
7 x.m l=0      spac=0.2
8 x.m l=0.75   spac=0.04
9 x.m l=1      spac=0.08
10 x.m l=1.17  spac=0.01
11 x.m l=1.27  spac=0.01
12 x.m l=2      spac=0.2
13 y.m l=-0.010 spac=0.005
14 y.m l=0      spac=$"surf_a"
15 y.m l=0.2    spac=0.02
16 y.m l=2      spac=0.5
17
18 eliminate columns y.min=0.6
19 eliminate columns y.min=1.0

```

```
20 eliminate columns y.min=1.5
21 eliminate rows      x.max=0.8 y.min=0.01 y.max=0.1
22 eliminate rows      x.min=1.5 y.min=0.01 y.max=0.15
23
24 region num=1 material=Silicon y.min=0
25 region num=2 material=Oxide    y.max=0
26
27 electrode name=gate x.min=0.75 length=0.5
28 electrode name=source y.max=0.0 left length=0.4
29 electrode name=drain y.max=0.0 right length=0.4
30 electrode name=substrate bottom
31
32 doping uniform conc=2e17 p.type
33 doping gauss    conc=1e18 n.type junc=0.1 x.right=0.75 rat=0.5
34 doping gauss    conc=1e18 n.type junc=0.1 x.left=1.25  rat=0.5
35 doping gauss    conc=1e20 n.type junc=0.2 x.right=0.65 rat=0.5
36 doping gauss    conc=1e20 n.type junc=0.2 x.left=1.35 rat=0.5
37
38 save outf=mos2ex14_0.str
39
40
41 go atlas
42
43 mesh inf=mos2ex14_0.str
44
45 contact name=gate n.poly
46
47 models cvt srh  print
48
49 method newton gummel carriers=1 electron
50 solve init
51 solve vdrain=0.1
52
53 # define probe of electron mobility vs. perpendicular field
54 probe name="channel mobility" n.mob dir=0 x=1 y=0.0001
55 probe name="channel field" field dir=90 x=1 y=0.0001
56
57 method newton carriers=1 electron
58 log outf=mos2ex14_1.log
59 solve vgate=0.0 vfinal=3.0 vstep=0.2 name=gate
60 output e.mob h.mob
61 save outf=mos2ex14_1.str
62
```

```
63 go atlas
64
65 mesh inf=mos2ex14_0.str
66
67 contact name=gate n.poly
68
69 models kla shi fldmob srh print
70
71 method newton gummel carriers=1 electron
72 solve init
73 solve vdrain=0.1
74
75 # define probe of electron mobility vs. perpendicular field
76 probe name="channel mobility" n.mob dir=0 x=1 y=0.0001
77 probe name="channel field" field dir=90 x=1 y=0.0001
78
79 method newton carriers=1 electron
80 log outf=mos2ex14_2.log
81 solve vgate=0.0 vfinal=3.0 vstep=0.2 name=gate
82 output e.mob h.mob
83 save outf=mos2ex14_2.str
84
85 go atlas
86
87 mesh inf=mos2ex14_0.str
88
89 contact name=gate n.poly
90
91 models conmob fldmob srh print min.surf
92 mobility watt.n mod.watt.n ymaxn.watt=0.01
93
94 method newton gummel carriers=1 electron
95 solve init
96 solve vdrain=0.1
97
98 # define probe of electron mobility vs. perpendicular field
99 probe name="channel mobility" n.mob dir=0 x=1 y=0.0001
100 probe name="channel field" field dir=90 x=1 y=0.0001
101
102 method newton carriers=1 electron
103 log outf=mos2ex14_3.log
104 solve vgate=0.0 vfinal=3.0 vstep=0.2 name=gate
105 output e.mob h.mob
```

```
106 save outf=mos2ex14_3.str
107
108 tonyplot -overlay mos2ex14*.log -set mos2ex14_1.set
109 tonyplot -overlay mos2ex14*.log -set mos2ex14_1a.set
110 tonyplot mos2ex14_1.str mos2ex14_2.str mos2ex14_3.str -set mos2ex14_2.set
```

2.1.15. mos2ex15.in : Effect of Poly Depletion on C-V curves

Requires: SPISCES

This example shows how reduced poly doping can result in depletion occurring in the poly gate under bias. This undesirable effect shows up in Capacitance-Voltage (C-V) curves as anomalies in the shape of the plot.

The effect of reduced poly doping in a MOSFET with a thin gate is to reduce drain current drive and increase the threshold voltage, since some of the voltage that should be dropped across the gate oxide is now dropped across the depletion region in the poly gate.

The usual cause of reduced doping in the poly is counter doping process flows, insufficient source-drain implant dose and evaporation of dopant during thermal anneals due to the lack of a capping oxide.

The example shows both the band diagram and Capacitance-Voltage curve of a P+ poly gate doped to a concentration of $1e19/cm^3$. The program then goes on to compare the same C-V plot and band diagram for the poly gate doped to $1e20/cm^3$ and $1e21/cm^3$ by overlaying the three cases.

It will be observed that even for a poly gate doped to $1e20/cm^3$, depletion occurs in the poly gate giving anomalous C-V characteristics. This can have serious consequences if the maximum value from the C-V curve is used to measure the thickness of the gate oxide.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

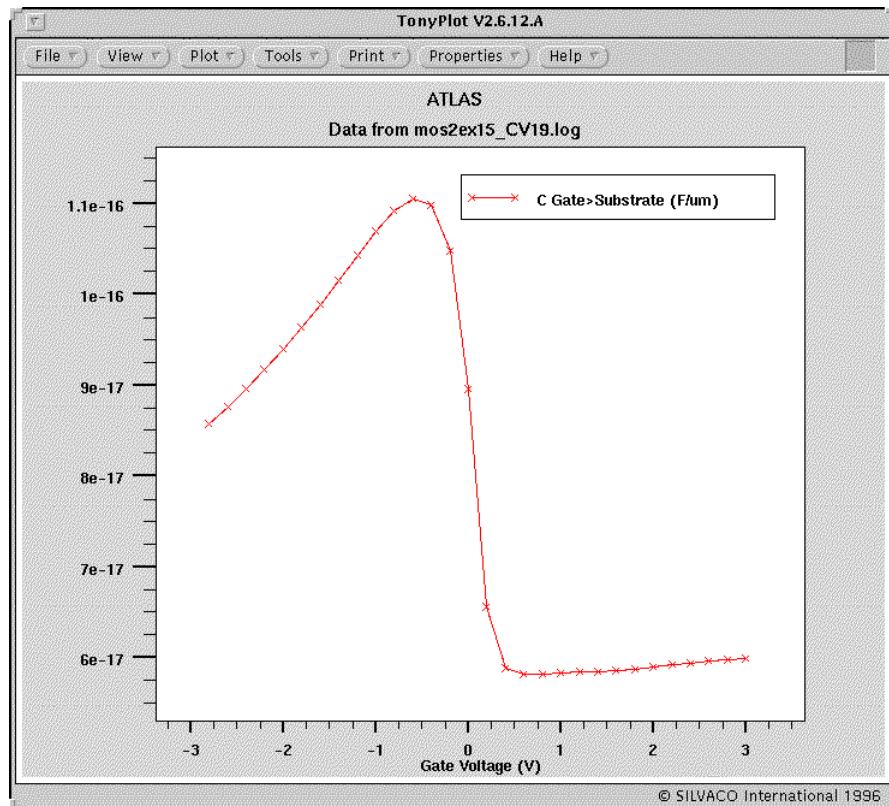


Figure 2.27: Standard C-V characteristic of a MOS capacitor at 100MHz

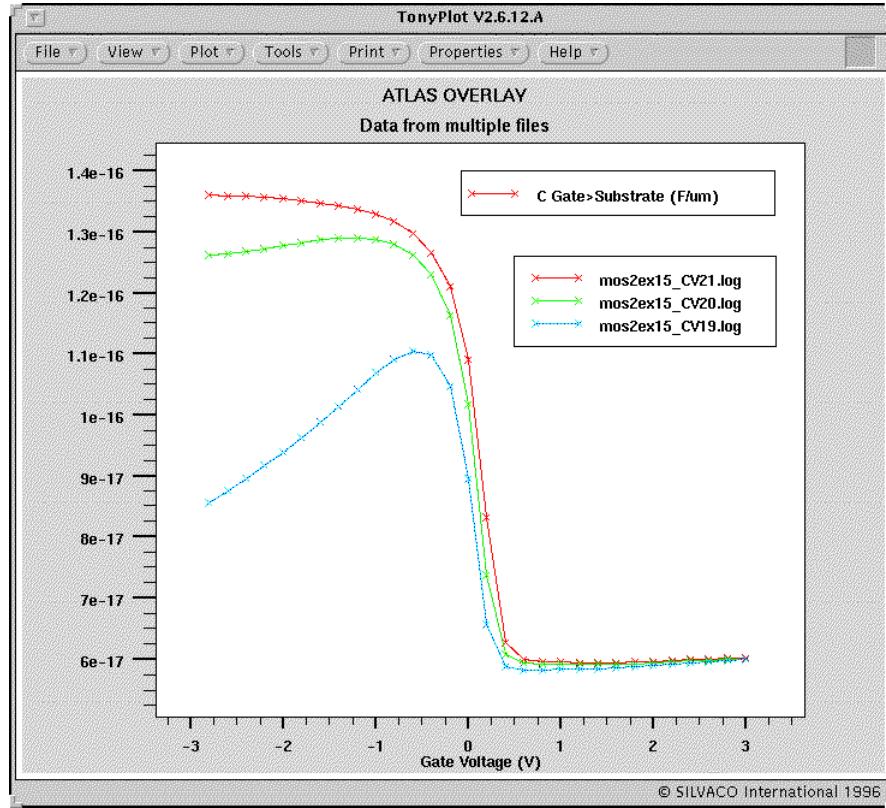


Figure 2.28: Comparison of C-V characteristics of a MOS capacitor with different poly gate doping concentrations

Input Deck mos2/mos2ex15.in :

```

1
2      go atlas
3
4      mesh
5
6      x.mesh loc=-0.01 spac=0.01
7      x.mesh loc=0.01   spac=0.01
8
9      y.mesh loc=-0.04 spac=0.001
10     y.mesh loc=0.02   spac=0.001
11
12     region number=1 x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 \
13         material=aluminum
14     region number=2 x.min=-0.01 x.max=0.01 y.min=-0.03 y.max=-0.005 \
15         material=poly
16     region number=3 x.min=-0.01 x.max=0.01 y.min=-0.005 y.max=0.0 \
17         material=oxide
18     region number=4 x.min=-0.01 x.max=0.01 y.min=0.0 y.max=0.02 \
19         material=silicon

```

```
20
21 electrode x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 name=gate
22 electrode bottom name=substrate
23
24 doping region=2 p.type concentration=1e19 uniform
25 doping region=4 p.type concentration=1e17 uniform
26
27 solve init
28 solve vgate=-1.5
29 solve vgate=-3
30
31 save outfile=mos2ex15-3V19.str
32 # tonyplot mos2ex15-3V19.str -set mos2ex15_BD.set
33
34 log outfile=mos2ex15_CV19.log
35 solve vgate=-2.8 vstep=0.2 vfinal=3.0 name=gate ac freq=1e6 previous
36 tonyplot mos2ex15_CV19.log -set mos2ex15_CV.set
37
38
39 go atlas
40
41 mesh
42
43 x.mesh loc=-0.01 spac=0.01
44 x.mesh loc=0.01 spac=0.01
45
46 y.mesh loc=-0.04 spac=0.001
47 y.mesh loc=0.02 spac=0.001
48
49 region number=1 x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 \
50 material=aluminum
51 region number=2 x.min=-0.01 x.max=0.01 y.min=-0.03 y.max=-0.005 \
52 material=poly
53 region number=3 x.min=-0.01 x.max=0.01 y.min=-0.005 y.max=0.0 \
54 material=oxide
55 region number=4 x.min=-0.01 x.max=0.01 y.min=0.0 y.max=0.02 \
56 material=silicon
57
58 electrode x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 name=gate
59 electrode bottom name=substrate
60
61 doping region=2 p.type concentration=1e20 uniform
62 doping region=4 p.type concentration=1e17 uniform
```

```
63
64 solve init
65 solve vgate=-1.5
66 solve vgate=-3
67
68 save outfile=mos2ex15-3V20.str
69 # tonyplot mos2ex15-3V20.str -set mos2ex15_BD.set
70
71 log outfile=mos2ex15_CV20.log
72 solve vgate=-2.8 vstep=0.2 vfinal=3.0 name=gate ac freq=1e6 previous
73
74
75 go atlas
76
77 mesh
78
79 x.mesh loc=-0.01 spac=0.01
80 x.mesh loc=0.01 spac=0.01
81
82 y.mesh loc=-0.04 spac=0.001
83 y.mesh loc=0.02 spac=0.001
84
85 region number=1 x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 \
86     material=aluminum
87 region number=2 x.min=-0.01 x.max=0.01 y.min=-0.03 y.max=-0.005 \
88     material=poly
89 region number=3 x.min=-0.01 x.max=0.01 y.min=-0.005 y.max=0.0 \
90     material=oxide
91 region number=4 x.min=-0.01 x.max=0.01 y.min=0.0 y.max=0.02 \
92     material=silicon
93
94 electrode x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 name=gate
95 electrode bottom name=substrate
96
97 doping region=2 p.type concentration=1e21 uniform
98 doping region=4 p.type concentration=1e17 uniform
99
100 solve init
101 solve vgate=-1.5
102 solve vgate=-3
103
104 save outfile=mos2ex15-3V21.str
105 # tonyplot mos2ex15-3V21.str -set mos2ex15_BD.set
```

```
106
107 log outfile=mos2ex15_CV21.log
108 solve vgate=-2.8 vstep=0.2 vfinal=3.0 name=gate ac freq=1e6 previous
109
110 tonyplot -overlay mos2ex15_CV21.log mos2ex15_CV20.log mos2ex15_CV19.log -
    set mos2ex15.CV.set
111
```

2.1.16. mos2ex16.in : Effect of Poly Doping on Threshold Voltage

Requires: SPISCES

This example shows the dramatic effect of depletion in the poly gate when the doping in the poly is reduced below it's maximum level. The I-V curves show that even a doping density of 1e20/cm³ in the poly is not sufficient to prevent depletion, loss of current drive and a shift in the threshold voltage of the n-MOSFET.

The first indication of poly depletion is non ideal C-V curves as shown in the previous "Poly Depletion" example. Reduced doping in the poly gate can be a combination of insufficient implant dose, counter doping of P+ poly and dopant evaporation during uncapped anneals.

The program runs three identical simulations the only difference being the doping in the poly gate. Three doping levels are simulated, 1e19, 1e20 and 1e21/cm³. At the end of the three simulations, the I-V curves of the n-MOSFET in the region of the threshold voltage are plotted. The effect of poly doping is demonstrated by the increased threshold voltage and reduced current drive with reduced poly doping.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

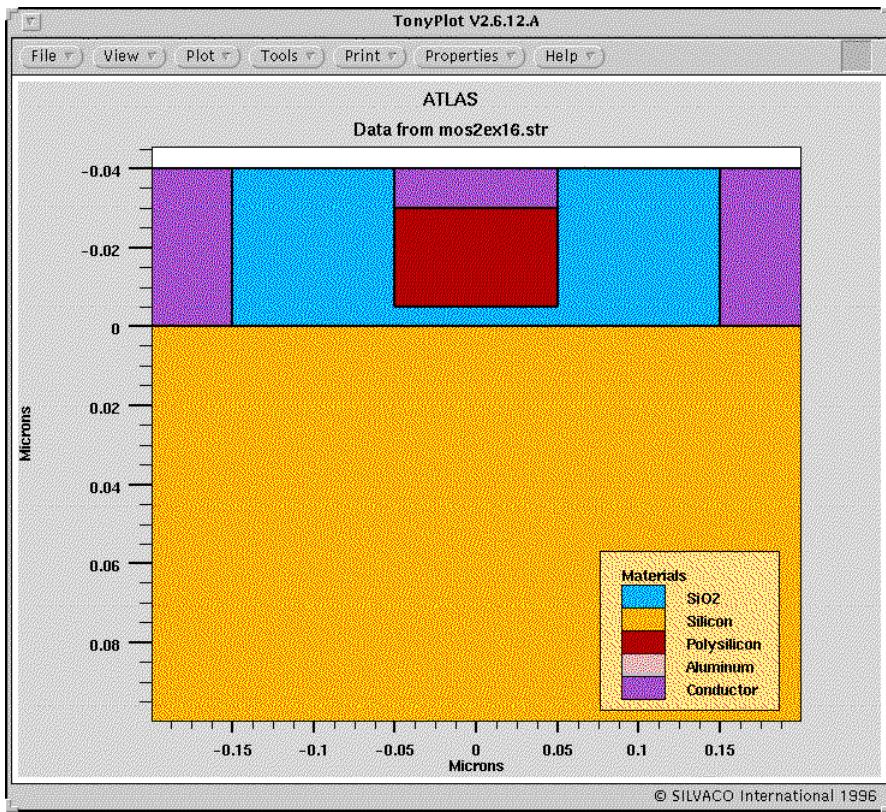


Figure 2.29: 2D plot of a simple MOSFET

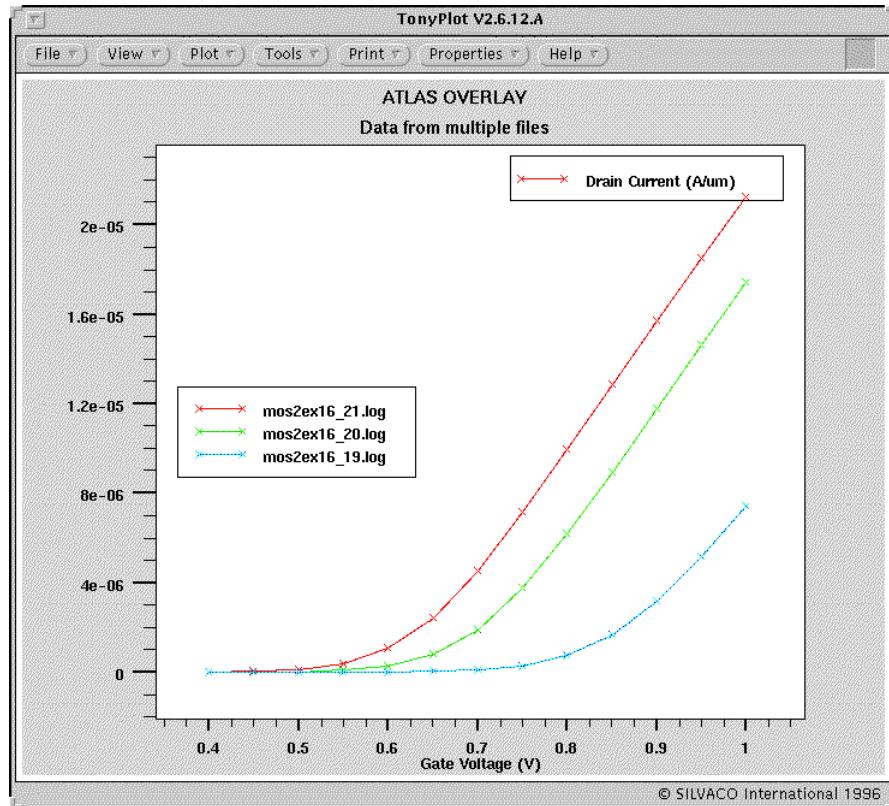


Figure 2.30: Comparison of Gate Current versus Gate voltage characteristics for different poly gate doping concentrations

Input Deck mos2/mos2ex16.in :

```

1
2      go atlas
3
4      mesh
5
6      x.mesh loc=-0.20    spac=0.025
7      x.mesh loc=-0.15    spac=0.025
8      x.mesh loc=-0.05    spac=0.010
9      x.mesh loc=0.05     spac=0.010
10     x.mesh loc=0.15     spac=0.025
11     x.mesh loc=0.20     spac=0.025
12
13     y.mesh loc=-0.04    spac=0.005
14     y.mesh loc=-0.03    spac=0.005
15     y.mesh loc=-0.005   spac=0.0025
16     y.mesh loc=0.0       spac=0.0005
17     y.mesh loc=0.01     spac=0.002
18     y.mesh loc=0.10     spac=0.02
19

```

```
20 region number=1 x.min=-0.20 x.max=0.20 y.min=-0.04 y.max=0.0      \
21     material=oxide
22 region number=2 x.min=-0.20 x.max=0.20 y.min=0.0 y.max=0.10      \
23     material=silicon
24 region number=3 x.min=-0.05 x.max=0.05 y.min=-0.03 y.max=-0.005 \
25     material=poly
26 region number=4 x.min=-0.05 x.max=0.05 y.min=-0.04 y.max=-0.03 \
27     material=aluminum
28 region number=5 x.min=-0.20 x.max=-0.15 y.min=-0.04 y.max=0.0      \
29     material=aluminum
30 region number=5 x.min=0.15  x.max=0.20  y.min=-0.04 y.max=0.0      \
31     material=aluminum
32
33 electrode x.min=-0.20 x.max=-0.15 y.min=-0.04 y.max=0.0 name=source
34 electrode x.min=-0.05 x.max=0.05  y.min=-0.04 y.max=-0.03 name=gate
35 electrode x.min=0.15  x.max=0.20  y.min=-0.04 y.max=0.0 name=drain
36 electrode bottom name=substrate
37
38 doping region=2 p.type concentration=1e18 uniform
39 doping region=3 n.type concentration=1e19 uniform
40 doping x.min=-0.2 x.max=-0.05 y.min=0.0 y.max=0.01 concentration=1e20 \
41     n.type uniform
42 doping x.min=0.05 x.max=0.2    y.min=0.0 y.max=0.01 concentration=1e20 \
43     n.type uniform
44
45 models cvt srh
46
47 solve init
48 solve vdrain=0.005
49 solve vdrain=0.05
50 solve vgate=0.05
51 log outfile=mos2ex16_19.log
52 solve vgate=0.4 vstep=0.05 vfinal=1.0 name=gate
53 extract name="nVt" x.val from curve(v."gate",i."drain") where y.val=0.5e-
8/0.1
54
55 save outfile=mos2ex16.str
56 tonyplot mos2ex16.str
57
58
59 go atlas
60
61 mesh
```

```
62
63 x.mesh loc=-0.20 spac=0.025
64 x.mesh loc=-0.15 spac=0.025
65 x.mesh loc=-0.05 spac=0.010
66 x.mesh loc=0.05 spac=0.010
67 x.mesh loc=0.15 spac=0.025
68 x.mesh loc=0.20 spac=0.025
69
70 y.mesh loc=-0.04 spac=0.005
71 y.mesh loc=-0.03 spac=0.005
72 y.mesh loc=-0.005 spac=0.0025
73 y.mesh loc=0.0 spac=0.0005
74 y.mesh loc=0.01 spac=0.002
75 y.mesh loc=0.10 spac=0.02
76
77 region number=1 x.min=-0.20 x.max=0.20 y.min=-0.04 y.max=0.0 \
78     material=oxide
79 region number=2 x.min=-0.20 x.max=0.20 y.min=0.0 y.max=0.10 \
80     material=silicon
81 region number=3 x.min=-0.05 x.max=0.05 y.min=-0.03 y.max=-0.005 \
82     material=poly
83 region number=4 x.min=-0.05 x.max=0.05 y.min=-0.04 y.max=-0.03 \
84     material=aluminum
85 region number=5 x.min=-0.20 x.max=-0.15 y.min=-0.04 y.max=0.0 \
86     material=aluminum
87 region number=5 x.min=0.15 x.max=0.20 y.min=-0.04 y.max=0.0 \
88     material=aluminum
89
90 electrode x.min=-0.20 x.max=-0.15 y.min=-0.04 y.max=0.0 name=source
91 electrode x.min=-0.05 x.max=0.05 y.min=-0.04 y.max=-0.03 name=gate
92 electrode x.min=0.15 x.max=0.20 y.min=-0.04 y.max=0.0 name=drain
93 electrode bottom name=substrate
94
95 doping region=2 p.type concentration=1e18 uniform
96 doping region=3 n.type concentration=1e20 uniform
97 doping x.min=-0.2 x.max=-0.05 y.min=0.0 y.max=0.01 concentration=1e20 \
98     n.type uniform
99 doping x.min=0.05 x.max=0.2 y.min=0.0 y.max=0.01 concentration=1e20 \
100     n.type uniform
101
102 models cvt srh
103
104 solve init
```

```
105 solve vdrain=0.005
106 solve vdrain=0.05
107 solve vgatet=0.05
108 log outfile=mos2ex16_20.log
109 solve vgatet=0.4 vstep=0.05 vfinal=1.0 name=gate
110 extract name="nVt" x.val from curve(v."gate",i."drain") where y.val=0.5e-
    8/0.1
111
112
113 go atlas
114
115 mesh
116
117 x.mesh loc=-0.20 spac=0.025
118 x.mesh loc=-0.15 spac=0.025
119 x.mesh loc=-0.05 spac=0.010
120 x.mesh loc=0.05 spac=0.010
121 x.mesh loc=0.15 spac=0.025
122 x.mesh loc=0.20 spac=0.025
123
124 y.mesh loc=-0.04 spac=0.005
125 y.mesh loc=-0.03 spac=0.005
126 y.mesh loc=-0.005 spac=0.0025
127 y.mesh loc=0.0 spac=0.0005
128 y.mesh loc=0.01 spac=0.002
129 y.mesh loc=0.10 spac=0.02
130
131 region number=1 x.min=-0.20 x.max=0.20 y.min=-0.04 y.max=0.0 \
132     material=oxide
133 region number=2 x.min=-0.20 x.max=0.20 y.min=0.0 y.max=0.10 \
134     material=silicon
135 region number=3 x.min=-0.05 x.max=0.05 y.min=-0.03 y.max=-0.005 \
136     material=poly
137 region number=4 x.min=-0.05 x.max=0.05 y.min=-0.04 y.max=-0.03 \
138     material=aluminum
139 region number=5 x.min=-0.20 x.max=-0.15 y.min=-0.04 y.max=0.0 \
140     material=aluminum
141 region number=5 x.min=0.15 x.max=0.20 y.min=-0.04 y.max=0.0 \
142     material=aluminum
143
144 electrode x.min=-0.20 x.max=-0.15 y.min=-0.04 y.max=0.0 name=source
145 electrode x.min=-0.05 x.max=0.05 y.min=-0.04 y.max=-0.03 name=gate
146 electrode x.min=0.15 x.max=0.20 y.min=-0.04 y.max=0.0 name=drain
```

```
147 electrode bottom name=substrate
148
149 doping region=2 p.type concentration=1e18 uniform
150 doping region=3 n.type concentration=1e21 uniform
151 doping x.min=-0.2 x.max=-0.05 y.min=0.0 y.max=0.01 concentration=1e20 \
152         n.type uniform
153 doping x.min=0.05 x.max=0.2     y.min=0.0 y.max=0.01 concentration=1e20 \
154         n.type uniform
155
156 models cvt srh
157
158 solve init
159 solve vdrain=0.005
160 solve vdrain=0.05
161 solve vgate=0.05
162 log outfile=mos2ex16_21.log
163 solve vgate=0.4 vstep=0.05 vfinal=1.0 name=gate
164 extract name="nVt" x.val from curve(v."gate",i."drain") where y.val=0.5e-
      8/0.1
165
166 tonyplot -overlay mos2ex16_21.log mos2ex16_20.log mos2ex16_19.log
```

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3.1. BJT: Bipolar Application Examples

3.1.1. bjtex01.in: NPN Gummel Plot and fT Extraction

Requires: SSUPREM4/DEVEDIT/SPISCES

This example demonstrates the processing, remeshing and electrical test of a polysilicon emitter NPN bipolar transistor. Design parameters are finally extracted from the IV Curve, including fT and Gain. This example demonstrates the use of:

- process simulation of a polysilicon emitter bipolar device
- re-meshing of the structure in DEVEDIT
- DC ramp of Vbe with fixed Vce
- Simultaneous AC simulation during Vbe ramp
- Extraction of peak gain and fT

The file starts with the definition of the process flow for an NPN bipolar transistor in ATHENA. The first boron implant forms the intrinsic base region. A second boron implant is self-aligned to the polysilicon emitter region to form a connection between the intrinsic base and p+ base contact regions. Spacer-like structures are used on the side of the poly emitter to space the p+ base contact and provide self-alignment. During the simulation the `relax` statement is used to reduce the mesh density in the deep regions of the structure. Only half of the full device is simulated. Mirroring of this half device into a full structure is done with `structure mirror left`. The final stage of the ATHENA syntax defines the electrode positions. In this example only one base contact is used. A subsequent example describes how two base contacts can be specified and linked together.

Often a mesh that is used for process simulation, is not optimal for use with device simulation. In this example, the mesh generation tool DEVEDIT is used to recreate a mesh that has zero obtuse triangles in the semiconductor region. It is then refined as a function of a number of solution quantities on the mesh (eg: boron conc).

Popup windows under the DECKBUILD command window were used to create this set of commands to control DEVEDIT. To switch to DEVEDIT commands select the current simulator to DEVEDIT from the Main Control window. Further use of DEVEDIT in more advanced applications is shown in later examples.

In ATLAS the solution procedure starts with a solution for a collector bias of 2V. Next, the `log` statement is used to specify a file for collection of Gummel plot data. The Gummel data is collected by applying a bias ramp on the base electrode up to 0.9. The parameter, `ac`, on the `solve` statement sets the ac analysis on. The frequency of this signal is set to 1MHz. Once the bias ramp is completed the data is plotted using TONYPLOT.

Finally, the `extract` statement is used to extract the maximum gain, "maxgain", and the maximum ft, "maxft", for the BJT. The extracted parameters may be used as optimization targets for simulator tuning.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

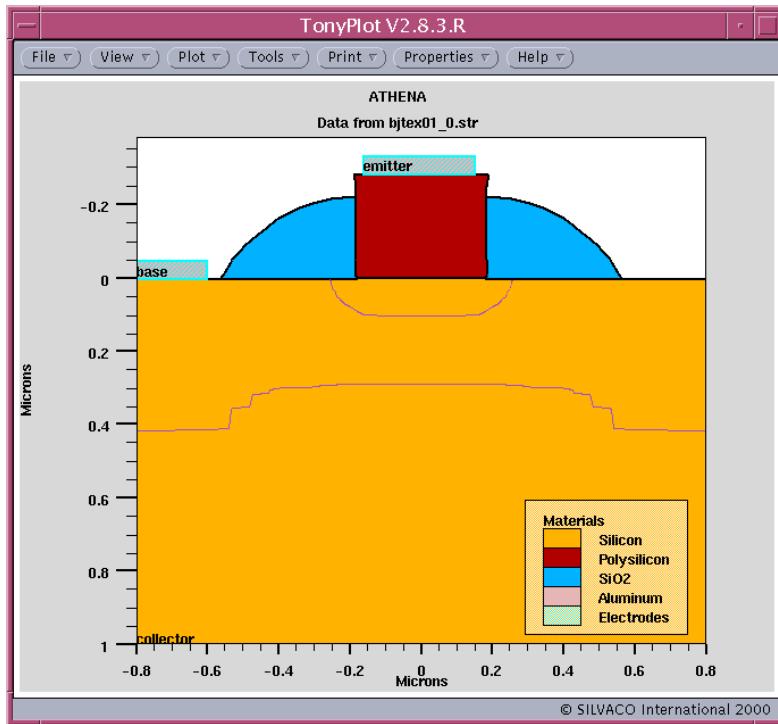


Figure 3.1: Structure of Poly Emitter Bipolar Transistor including dopant junctions, regions and electrodes

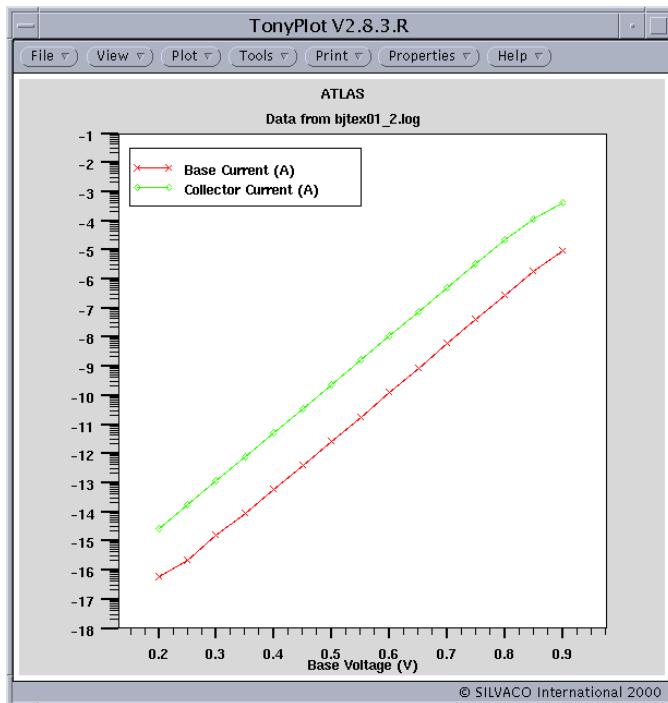


Figure 3.2: Gummel Plot from Bipolar Device. Gain can be calculated from a function of the collector and base currents

Input File bjt/bjtex01.in:

```
1 go athena
2 #TITLE: Polysilicon Emitter Bipolar Example - Ssuprem4->DevEdit->Spisces2
3 # If you do not have DevEdit: Please comment these lines out....
4 line x loc=0.0      spacing=0.03
5 line x loc=0.2      spacing=0.02
6 line x loc=0.24     spacing=0.015
7 line x loc=0.3      spacing=0.015
8 line x loc=0.8      spacing=0.15
9 #
10 line y loc=0.0     spacing=0.01
11 line y loc=0.07    spacing=0.01
12 line y loc=0.1     spacing=0.01
13 line y loc=0.12    spacing=0.01
14 line y loc=0.3     spacing=0.02
15 line y loc=0.5     spacing=0.06
16 line y loc=1.0     spacing=0.35
17 #
18 init c.arsenic=2e16
19 #
20 implant boron energy=18 dose=2.5e13
21 diffuse time=60 temp=920
22 # deposit polysilicon
23 deposit poly thick=0.3 divisions=6 min.space=0.05
24
25 # Implant to dope polysilicon
26 implant arsenic dose=7.5e15 energy=50
27
28 # Pattern the poly
29 etch poly right p1.x=0.2
30
31 relax y.min=.2 x.min=0.2
32 relax y.min=.2 x.min=0.2
33
34 method compress fermi
35 diffuse time=25   temp=920 dryo2
36 diffuse time=50   temp=900 nitrogen
37
38 implant boron dose=2.5e13 energy=18
39
40 # deposit spacer
41 deposit oxide thick=0.4 divisions=10 min.space=0.1
42
```

```
43 # etch the spacer back
44 etch oxide dry thick=0.5
45
46 implant boron dose=1e15 energy=30
47
48 diffuse time=60 temp=900    nitrogen
49
50 structure reflect left
51
52 # put down Al and etch to form contacts
53 deposit alum thick=0.05 div=2
54
55 etch alum start x=-0.16 y=-4
56 etch continue x=-0.16 y=0.2
57 etch continue x=-0.6 y=0.2
58 etch done  x=-0.6 y=-4
59
60 etch alum right p1.x=0.15
61
62 # Name the electrodes for use with Atlas.....1,2,3
63 electrode x=0.0      name=emitter
64 electrode x=-0.65   name=base
65 electrode backside name=collector
66
67 # Save the final structure
68 structure outfile=bjtex01_0.str
69
70
71 # Completely remesh the structure without obtuse triangles in the semi-
    conductor
72 # Use the Sensitivity & Minspacing parameters to adjust the mesh densi-
    ty....
73 # .. the smaller the Sensitivity, the denser the mesh...
74 go DevEdit
75
76 base.mesh height=0.25 width=0.25
77 bound.cond apply=false max.ratio=300
78 constr.mesh max.angle=90 max.ratio=300 max.height=1 max.width=1 \
79             min.height=0.0001 min.width=0.0001
80 constr.mesh type=Semiconductor default
81 constr.mesh type=Insulator default max.angle=170
82 constr.mesh type=Metal default max.angle=180
83
84 # Define the minimum mesh spacing globally...
```

```
85 imp.refine min.spacing=0.025
86
87 # Select a list of solution (impurity) gradients to refine upon....
88 imp.refine imp="Arsenic" sensitivity=0.5
89 imp.refine imp="Boron" sensitivity=0.5
90
91 # now mesh the structure....
92 mesh
93 #
94 struct outfile=bjtex01_1.str
95 #
96 ##### Gummel Plot Test #####
97 # Electrode names used in this test: Base, Collector, Emitter
98 go atlas
99 # set material models etc.
100 material taun0=5e-6 taup0=5e-6
101 contact name=emitter n.poly surf.rec
102 models bipolar print
103
104 # initial solution
105
106 solve init
107
108 # change to two carriers
109 method newton autonr trap
110 solve prev
111 # set the collector bias
112 solve vcollector=2 local
113 # start ramping the base
114 solve vbase=0.1
115 # Ramp the base to 0.9 volts....
116 log outf=bjtex01_2.log master
117 solve vbase=0.2 vstep=0.05 vfinal=0.9 name=base ac freq=1e6 aname=base
118
119 # Now dump a structure file, for tonyplotting... but first decide what
120 # you want in it, on top of the default quantities.....
121 output e.field flowlines jx.el jx.ho jy.el jy.ho
122 save outf=bjtex01_3.str
123 tonyplot bjtex01_3.str -set bjtex01_1.set
124
125 # Now extract some design parameters...
126 extract name="peak collector current" max(curve(abs(v."base"),abs(i."collector")))
```

```
127 extract name="peak gain" max(i."collector"/ i."base")
128 extract name="max fT" max(g."collector" "base"/(2*3.1415*c."base" "base"))
129 # plot the results
130 tonyplot bjtex01_2.log -set bjtex01_2.set
131 quit
132
```

3.1.2. bjtex02.in: 3D Bipolar Simulation

Requires: DEVEDIT3D/DEVICE3D

This example demonstrates Gummel plot simulation of a BJT structure in three dimensions. It shows:

- construction of the device in DEVEDIT3D
- simulation of the Gummel plot in ATLAS

In this example a bipolar transistor is constructed using DEVEDIT3D. The structure is then passed to ATLAS for electrical testing. The input file consists of the two following main portions:

The first stage of the input constructs the BJT geometry, material regions, doping profiles, and electrodes in DEVEDIT3D. The structure was created in DEVEDIT3D by drawing the device regions in interactive mode and specifying 3D doping distribution. Finally the mesh was generated automatically by specifying basic mesh constraints and refining in the important areas of the device.

The ATLAS simulation begins by reading in the structure from DEVEDIT3D. DeckBuild provides auto-interface between DEVEDIT3D and ATLAS so that the structure produced by DEVEDIT3D is transferred to ATLAS without having to indicate the mesh statement.

The models statement is used to select a set of physical models for this simulation. In this case, these models are 'srh' and 'auger' recombination, the concentration and field dependent mobility model, and two carriers model

The initial solution for zero biases then, is obtained using solve init. The emitter voltage is then ramped negatively. The Newton algorithm is used for these calculations. This is the default method in ATLAS.

The results of simulation are then displayed using TONYPLOT.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

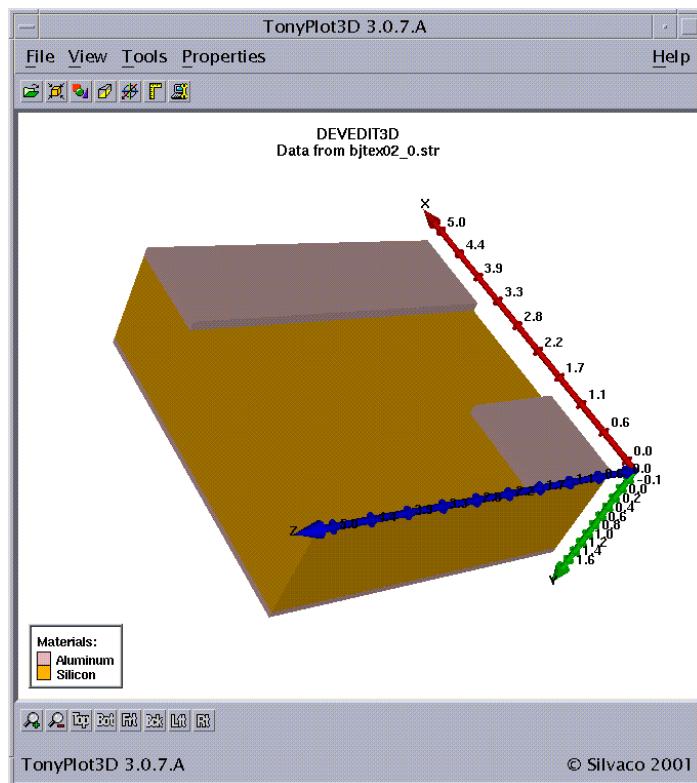


Figure 3.3: 3D Bipolar Structure showing electrode locations

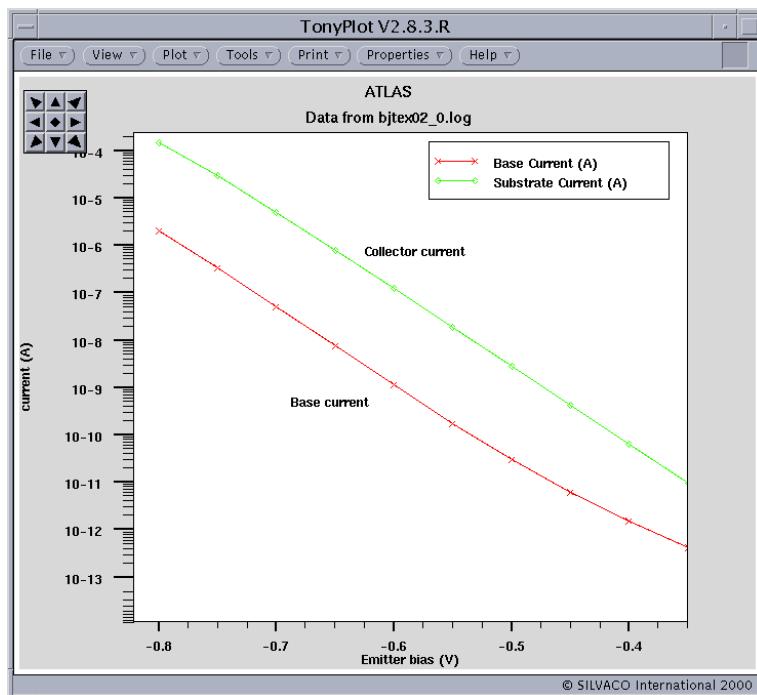


Figure 3.4: Gummel Plot from a 3D Bipolar simulation

Input File bjt/bjtex02.in:

```
1 go DevEdit
2
3 DevEdit version="2.0" library="1.14"
4
5 work.area left=0 top=-0.5 right=5 bottom=1.6
6
7 # SILVACO Library V1.14
8
9 region reg=1 name=Silicon mat=Silicon color=0xffffc000 pattern=0x3 z1=0
   z2=5 \
10 points="0,0 1.5,0 3.5,0 5,0 5,1.5 0,1.5 0,0"
11 #
12 impurity id=1 region.id=1 imp=Phosphorus color=0x906000 \
13 x1=0 x2=0 y1=0 y2=0 \
14 peak.value=1e+16 ref.value=0 z1=0 z2=0 comb.func=Multiply \
15 rolloff.y=both conc.func.y=Constant \
16 rolloff.x=both conc.func.x=Constant \
17 rolloff.z=both conc.func.z=Constant
18 #
19 constr.mesh region=1 default
20
21 region reg=2 name=Emitter mat=Aluminum elec.id=1 work.func=4.1 col-
   or=0xffffc8c8 pattern=0x6 z1=0 z2=1.5 \
22 points="0,0 0,-0.15 1.5,-0.15 1.5,0 0,0"
23 #
24 constr.mesh region=2 default
25
26 region reg=3 name=Base mat=Aluminum elec.id=2 work.func=4.1 col-
   or=0xffffc0c0 pattern=0x6 z1=0 z2=5 \
27 points="3.5,0 3.5,-0.15 5,-0.15 5,0 3.5,0"
28 #
29 constr.mesh region=3 default
30
31 region reg=4 name=substrate mat=Aluminum elec.id=3 work.func=0 col-
   or=0xffffc8c8 pattern=0x6 z1=0 z2=5 \
32 points="0,1.5 5,1.5 5,1.6 0,1.6 0,1.5"
33 #
34 constr.mesh region=4 default
35
36
37 impurity id=1 imp=Boron color=0x906000 \
38 x1=0 x2=5 y1=0 y2=0 \
39 peak.value=5e+18 ref.value=0 z1=0 z2=5 comb.func=Multiply \
```

```
40 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.16 \
41 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.25 \
42 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.25
43 impurity id=2 imp=Arsenic color=0x906000 \
44 x1=0 x2=5 y1=1.5 y2=1.5 \
45 peak.value=4e+19 ref.value=0 z1=0 z2=5 comb.func=Multiply \
46 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.1 \
47 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.25 \
48 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.25
49 impurity id=3 imp=Arsenic color=0x906000 \
50 x1=0 x2=1.5 y1=0 y2=0 \
51 peak.value=1e+20 ref.value=0 z1=0 z2=1.5 comb.func=Multiply \
52 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.1 \
53 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.1 \
54 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.1
55
56 # Set Meshing Parameters
57 #
58 base.mesh height=1000000 width=1000000
59 #
60 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
       line.straightening=1 align.points when=automatic
61 #
62 imp.refine imp="NetDoping" sensitivity=0.25
63 imp.refine min.spacing=0.05 z=
64 #
65 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
66 max.width=1 min.height=0.0001 min.width=0.0001
67 #
68 constr.mesh type=Semiconductor default
69 #
70 constr.mesh type=Insulator default
71 #
72 constr.mesh type=Metal default
73 #
74 constr.mesh type=Other default
75 #
76 constr.mesh region=1 default
77 #
78 constr.mesh region=2 default
79 #
80 constr.mesh region=3 default
81 #
```

```
82 constr.mesh region=4 default
83 #
84 # Perform mesh operations
85 #
86 Mesh Mode=MeshBuild
87
88 imp.refine imp="NetDoping" sensitivity=0.25
89 imp.refine min.spacing=0.05 z=0
90
91 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
92 max.width=1 min.height=0.0001 min.width=0.0001
93 #
94 constr.mesh type=Semiconductor default
95 #
96 constr.mesh type=Insulator default
97 #
98 constr.mesh type=Metal default
99 #
100 constr.mesh type=Other default
101
102 z.plane z=0 spacing=1.5
103 #
104 z.plane z=1.55 spacing=0.05
105 #
106 z.plane z=2 spacing=1
107 #
108 z.plane max.spacing=1000000 max.ratio=1.5
109
110 base.mesh height=1000000 width=1000000
111
112 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.Points when=automatic
113
114 structure outfile=bjtex02_0.str
115
116 go atlas
117 #
118 models    srh auger bgn conmob fldmob
119 #
120 solve init
121 #
122 solve prev
123 #
```

```

124 log outfile=bjtex02_0.log
125 solve v1=-0.3 vstep=-0.05 nstep=10 elec=1 v3=1 outf=bjtex02_1.str onefile
126 #
127 tonyplot bjtex02_0.log -set bjtex02_0.set
128 #
129 quit

```

3.1.3. bjtex03.in: Analysis of NPN Device with 2 Base Contacts

Requires: SSUPREM4/DEVEDIT/SPISCES

This example has been created with two symmetrical extrinsic base contacts in an effort to more clearly demonstrate the use of the contact statement for *slaving* electrode contacts together. This example is equivalent to the first example in this section in all other respects. It shows:

- process simulation of a polysilicon emitter bipolar device
- re-meshing of the structure in DEVEDIT
- specification of the linking of two electrode together
- DC ramp of Vbe with fixed Vce
- simultaneous AC simulation during the Vbe ramp
- extraction of peak gain and fT

The process simulation, remeshing and basic device simulation syntax used in this example is exactly equivalent to the first example in this section. The difference is in the use of two 'tied' electrodes.

The electrode names *base* and *base1* are defined within ATHENA and are then held together with the contact name=*base* common=*base1* statement within ATLAS. Thus, the subsequent use of the name, v. "base", in the solve statements will apply to both the *base* contact and the *base1* contact.

The extract statement at the end of the file makes the addition of the currents from two base contacts for parameter extraction purposes.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

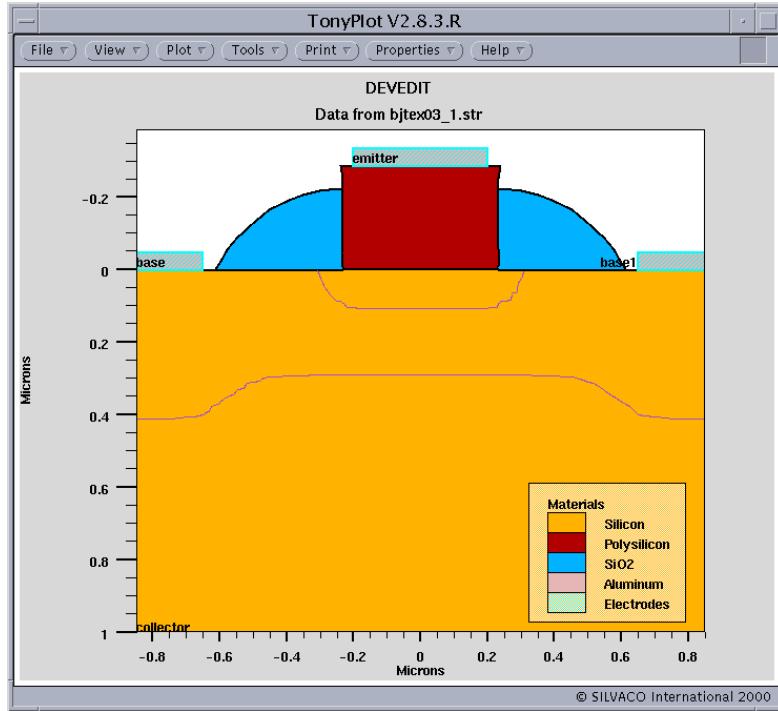


Figure 3.5: Structure of Poly Emitter Bipolar Transistor including dopant junctions, regions and electrodes. The structure differs from the first bipolar example by having two base contacts. This structure has been remeshed in DevEdit.

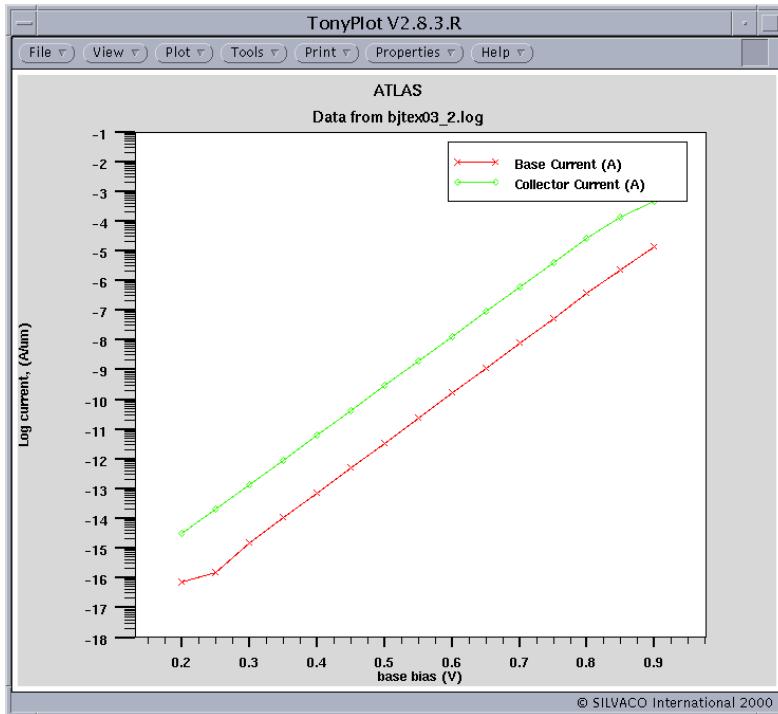


Figure 3.6: Gummel Plot from the double base BJT. Gain is calculated by dividing collector current by the sum of the two base currents.

Input File bjt/bjtex03.in:

```
1 go athena
2 #TITLE: Polysilicon Emitter Bipolar Example - Ssuprem4->DevEdit->Spisces2
3 # If you do not have DevEdit: Please comment these lines out....
4 line x loc=0.0      spacing=0.03
5 line x loc=0.2      spacing=0.02
6 line x loc=0.24     spacing=0.015
7 line x loc=0.3      spacing=0.015
8 line x loc=0.8      spacing=0.15
9 #
10 line y loc=0.0     spacing=0.01
11 line y loc=0.07    spacing=0.01
12 line y loc=0.1     spacing=0.01
13 line y loc=0.12    spacing=0.01
14 line y loc=0.3     spacing=0.02
15 line y loc=0.5     spacing=0.06
16 line y loc=1.0     spacing=0.35
17 #
18 init c.arsenic=2e16
19 #
20 implant boron energy=18 dose=2.5e13
21 diffuse time=60 temp=920
22 # deposit polysilicon
23 deposit poly thick=0.3 divisions=6 min.space=0.05
24
25 # Implant to dope polysilicon
26 implant arsenic dose=7.5e15 energy=50
27
28 # Pattern the poly
29 etch poly right p1.x=0.2
30
31 relax y.min=.2 x.min=0.2
32 relax y.min=.2 x.min=0.2
33
34 method compress fermi
35 diffuse time=25   temp=920 dryo2
36 diffuse time=50   temp=900 nitrogen
37
38 implant boron dose=2.5e13 energy=18
39
40 # deposit spacer
41 deposit oxide thick=0.4 divisions=10 min.space=0.1
42
```

```
43 # etch the spacer back
44 etch oxide dry thick=0.5
45
46 implant boron dose=1e15 energy=30
47
48 diffuse time=60 temp=900    nitrogen
49
50
51 # put down Al and etch to form contacts
52 deposit alum thick=0.05 div=2
53
54 etch alumin start x=0.15 y=-10
55 etch continue      x=0.15 y=10
56 etch continue      x=0.6 y=10
57 etch done          x=0.6 y=-10
58
59 structure reflect left
60
61 stretch stretch.val=0.1 x.val=0.0
62
63
64 # Name the electrodes for use with ATLAS.....base and basel will be slaved
65 #during device simulation with the 'CONTACT' statement....
66 electrode x=0.0      name=emitter
67 electrode x=-0.7     name=base
68 electrode backside   name=collector
69 electrode x=0.7      name=basel
70
71 # Save the final structure
72 structure outfile=bjtex03_0.str
73
74
75 # Completely remesh the structure without obtuse triangles in the semi-
    conductor
76 # Use the Sensitivity & Minspacing parameters to adjust the mesh densi-
    ty....
77 # ... the smaller the Sensitivity, the denser the mesh...
78 go DevEdit
79
80 base.mesh height=0.25 width=0.25
81 bound.cond apply=false max.ratio=300
82 constr.mesh max.angle=90 max.ratio=300 max.height=1 max.width=1 \
83             min.height=0.0001 min.width=0.0001
84 constr.mesh type=Semiconductor default
```

```
85 constr.mesh type=Insulator default max.angle=170
86 constr.mesh type=Metal default max.angle=180
87
88 # Define the minimum mesh spacing globally...
89 imp.refine min.spacing=0.025
90
91 # Select a list of solution (impurity) gradients to refine upon....
92 imp.refine imp="Arsenic" sensitivity=0.5
93 imp.refine imp="Boron" sensitivity=0.5
94
95 # now mesh the structure....
96 mesh
97 #
98 struct outfile=bjtex03_1.str
99 tonyplot bjtex03_1.str -set bjtex03_1.set
100 #
101 ##### Gummel Plot Test #####
102
103 go atlas
104 # set material models etc.
105 material taun0=5e-6 taup0=5e-6
106 contact name=emitter n.poly surf.rec
107 contact name=basel common=base
108
109 models bipolar print
110
111 # initial solution
112
113 solve init
114
115 # change to two carriers
116 method newton autonr trap
117 solve prev
118 # set the collector bias
119 solve vcollector=2 local
120 # start ramping the base
121 solve vbase=0.1
122 # Ramp the base to 0.9 volts....
123 log outf=bjtex03_2.log master
124 solve vbase=0.2 vstep=0.05 vfinal=0.9 name=base ac freq=1e6 aname=base
125
126 # Now dump a structure file, for tonyplotting... but first decide what
127 # you want in it, on top of the default quantities.....
```

```
128 output e.field flowlines jx.el jx.ho jy.el jy.ho
129 save outf=bjtex03_3.str
130
131 # Now extract some design parameters...
132 extract name="peak collector current" max(curve(abs(v."base"),abs(i."collector")))
133 extract name="peak gain" max(i."collector"/ i."base")
134 extract name="max fT" max(g."collector""base"/(2*3.1415*c."base""base"))
135 # plot the results
136 tonyplot bjtex03_2.log -set bjtex03_2.set
137
138 quit
```

3.1.4. bjtex04.in: NPN - Gummel Plot and Ic/Vce Characterization

Requires: SPISCES

This example simulates a Gummel plot and the Ic vs. Vce characteristics for different values of base current of a silicon BJT. It shows:

- formation of an NPN BJT using ATLAS syntax
- Ic and Ib extraction versus Vbe (Gummel plot)
- Ic extraction versus Vce for various Ib

The initial stage of the example uses the `mesh`, `region`, and `electrode` statements in ATLAS to construct the NPN structure. Analytical doping profiles are added in the `doping` statement. The structure has a heavy n+ emitter, 1.0e18 peak base concentration, a buried collector layer and heavy p+ extrinsic base contact.

The `contact` statement is used to define the emitter contact as a N-type polysilicon emitter. Surface recombination is also specified at the polysilicon/silicon interface. Next, the `material` statement is used to specify the electron and hole SRH lifetimes. The `models bipolar` statement is set to specify that the default set of bipolar models is to be used. The default set of bipolar models includes: concentration dependent mobility, field dependent mobility, band-gap narrowing, concentration dependent lifetimes and Auger recombination.

The gummel plot syntax is similar to that described in the first example of this section. The syntax for the Ic/Vce simulation is described under the PNP example in this section. The key point is the use of current boundary conditions on the base contact as defined by `contact name=base current`. This allows a constant base current to be forced while Vce is ramped. The family of Ic/Vce curves can be overlaid in TONYPLOT or exported to UTMOST for SPICE model extraction.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

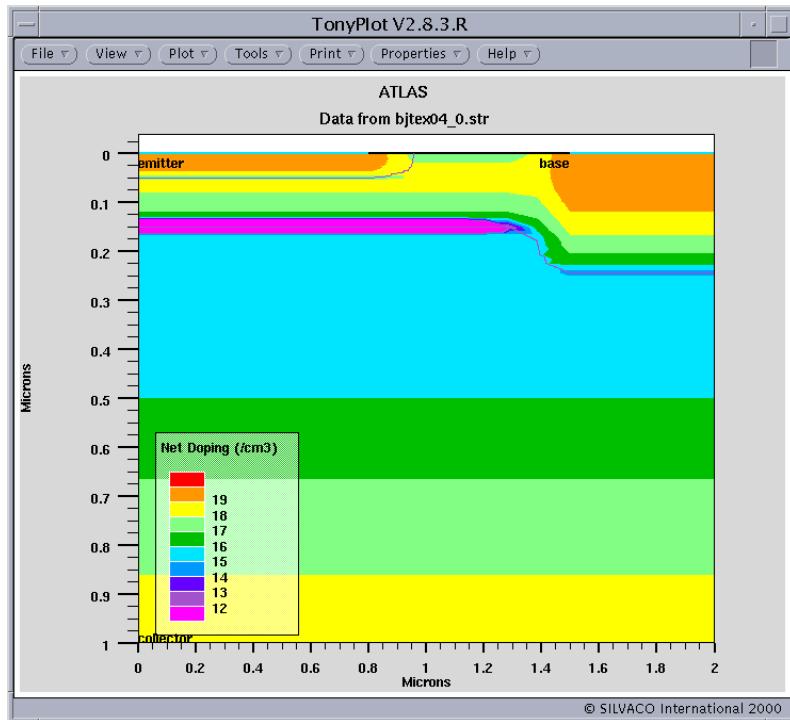


Figure 3.7: Planar bipolar device defined using ATLAS syntax

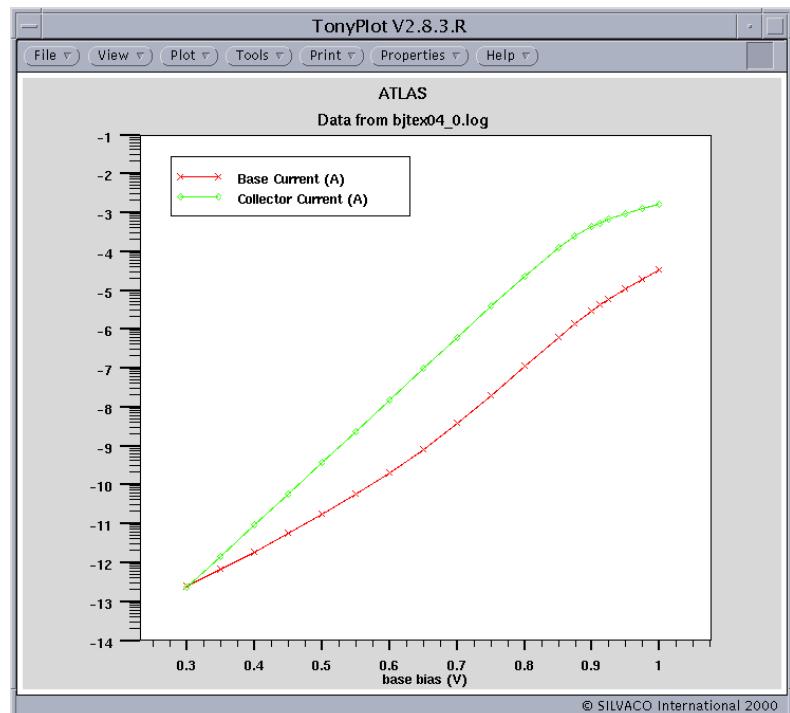
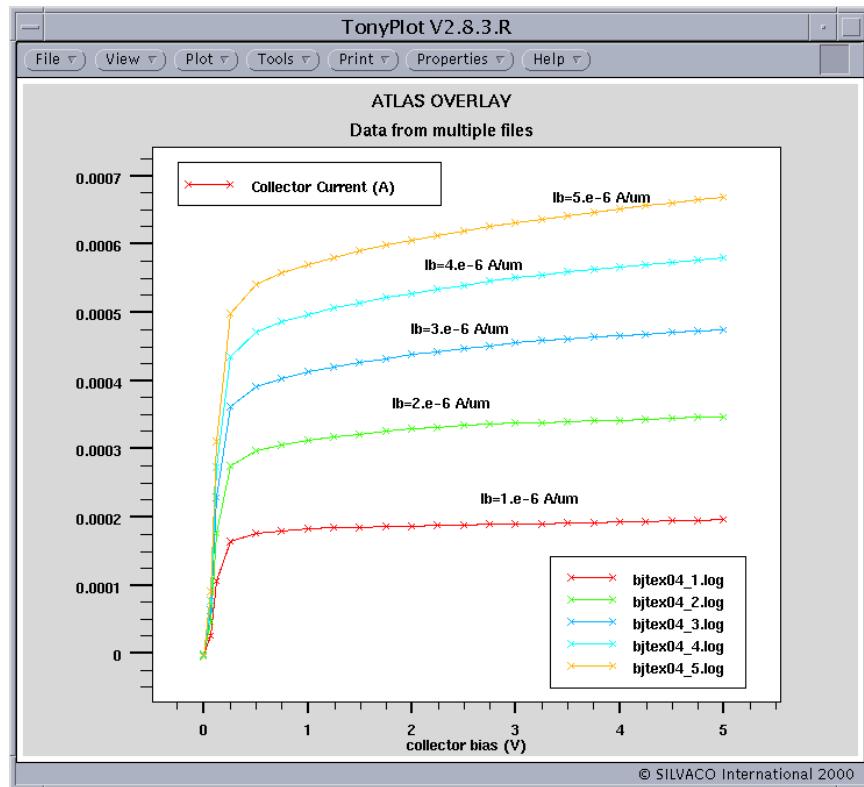


Figure 3.8: Gummel Plot from the planar bipolar device

**Figure 3.9:** Families of I_C/V_{CE} curves for various I_B **Input File bjt/bjtex04.in:**

```

1 go atlas
2 TITLE Bipolar Gummel plot and IC/VCE with constant IB
3 # Silvaco International 1992, 1993, 1994
4
5
6 mesh
7 x.m l=0    spacing=0.15
8 x.m l=0.8   spacing=0.15
9 x.m l=1.0   spacing=0.03
10 x.m l=1.5  spacing=0.12
11 x.m l=2.0  spacing=0.15
12
13
14 y.m l=0.0  spacing=0.006
15 y.m l=0.04 spacing=0.006
16 y.m l=0.06 spacing=0.005
17 y.m l=0.15 spacing=0.02
18 y.m l=0.30 spacing=0.02
19 y.m l=1.0  spacing=0.12

```

```
20
21
22
23 region num=1 silicon
24
25 electrode num=1 name=emitter left length=0.8
26 electrode num=2 name=base      right length=0.5 y.max=0
27 electrode num=3 name=collector bottom
28
29 doping reg=1 uniform n.type conc=5e15
30 doping reg=1 gauss   n.type conc=1e18 peak=1.0 char=0.2
31 doping reg=1 gauss   p.type conc=1e18 peak=0.05 junct=0.15
32 doping reg=1 gauss   n.type conc=5e19 peak=0.0  junct=0.05 x.right=0.8
33 doping reg=1 gauss   p.type conc=5e19 peak=0.0  char=0.08 x.left=1.5
34
35
36
37
38 # set bipolar models
39 models commob fldmob consrh auger print
40 contact name=emitter n.poly surf.rec
41
42
43
44 solve init
45
46 save outf=bjtex04_0.str
47
48 tonyplot bjtex04_0.str -set bjtex04_0.set
49
50 # Gummel plot
51
52 method newton autonr trap
53 solve vcollector=0.025
54 solve vcollector=0.1
55 solve vcollector=0.25 vstep=0.25 vfinal=2 name=collector
56
57
58 solve vbase=0.025
59 solve vbase=0.1
60 solve vbase=0.2
61
62
```

```
63 log outf=bjtex04_0.log
64 solve vbase=0.3 vstep=0.05 vfinal=1 name=base
65
66 tonyplot bjttx04_0.log -set bjttx04_0_log.set
67
68
69
70
71 #IC/VCE with constant IB
72
73 #ramp Vb
74
75 log off
76 solve init
77 solve vbase=0.025
78 solve vbase=0.05
79
80
81 solve vbase=0.1 vstep=0.1 vfinal=0.7 name=base
82
83
84 # switch to current boundary conditions
85
86 contact name=base current
87
88 # ramp IB and save solutions
89 solve ibase=1.e-6
90 save outf=bjtex04_1.str master
91 solve ibase=2.e-6
92 save outf=bjtex04_2.str master
93 solve ibase=3.e-6
94 save outf=bjtex04_3.str master
95 solve ibase=4.e-6
96 save outf=bjtex04_4.str master
97 solve ibase=5.e-6
98 save outf=bjtex04_5.str master
99
100
101 # load in each initial guess file and ramp VCE
102 load inf=bjtex04_1.str master
103 log outf=bjtex04_1.log
104 solve vcollector=0.0 vstep=0.25 vfinal=5.0 name=collector
105
```

```

106 load inf=bjtex04_2.str master
107 log outf=bjtex04_2.log
108 solve vcollector=0.0 vstep=0.25 vfinal=5.0 name=collector
109
110 load inf=bjtex04_3.str master
111 log outf=bjtex04_3.log
112 solve vcollector=0.0 vstep=0.25 vfinal=5.0 name=collector
113
114 load inf=bjtex04_4.str master
115 log outf=bjtex04_4.log
116 solve vcollector=0.0 vstep=0.25 vfinal=5.0 name=collector
117
118 load inf=bjtex04_5.str master
119 log outf=bjtex04_5.log
120 solve vcollector=0.0 vstep=0.25 vfinal=5.0 name=collector
121
122
123
124
125 # plot results
126 tonyplot -overlay bjt04_1.log bjt04_2.log bjt04_3.log
      bjt04_4.log bjt04_5.log -set bjt04_1_log.set
127 quit

```

3.1.5. **bjtex05.in:** NPN - BVCEO Breakdown Voltage

Requires: S-PISCES

This example calculates the BVCEO breakdown voltage in an NPN transistor. It shows:

- formation of an NPN BJT using ATLAS syntax
- selection of the correct models and methods for breakdown simulation
- setting of current boundary conditions to force an open base contact
- I_c extraction versus V_{ce} with an open base contact

In the first part of the input file the device is described, including mesh, electrodes location, and doping distribution. The device geometry and doping are as used in the previous example.

The **{bold}** impact statement is used to specify the Selberherr impact ionization model required for breakdown analysis.

For increased stability which is typically needed for such kind of simulation with zero base current, the solution with small value of base current, $I_b=3.e-15$ A/ μm , is obtained at the first stage of simulation. Then the collector voltage is ramped until the collector current reaches the value $5.e-11$ A/ μm .

To set the open base contact, it is necessary to define zero current passing through the base electrode. This is done by setting current boundary conditions on the base using `contact name=base current`. Then throughout the breakdown simulation I_b is held at zero. This is the most effective approach for BVCEO simulation.

The ramp of collector voltage is set on the final `solve` statement. The ramp continues up to 10V. However, a compliance limit on the collector current is set using the parameters, `compl=<num>`, `cname=collector`. The `<num>` specifies the value of the compliance limit in A/um, while the `cname` indicates which contact the compliance current should be measured on. Once the simulated collector current exceeds the compliance value, the simulation steps on to the next line of syntax. Here that line is to plot the results in TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

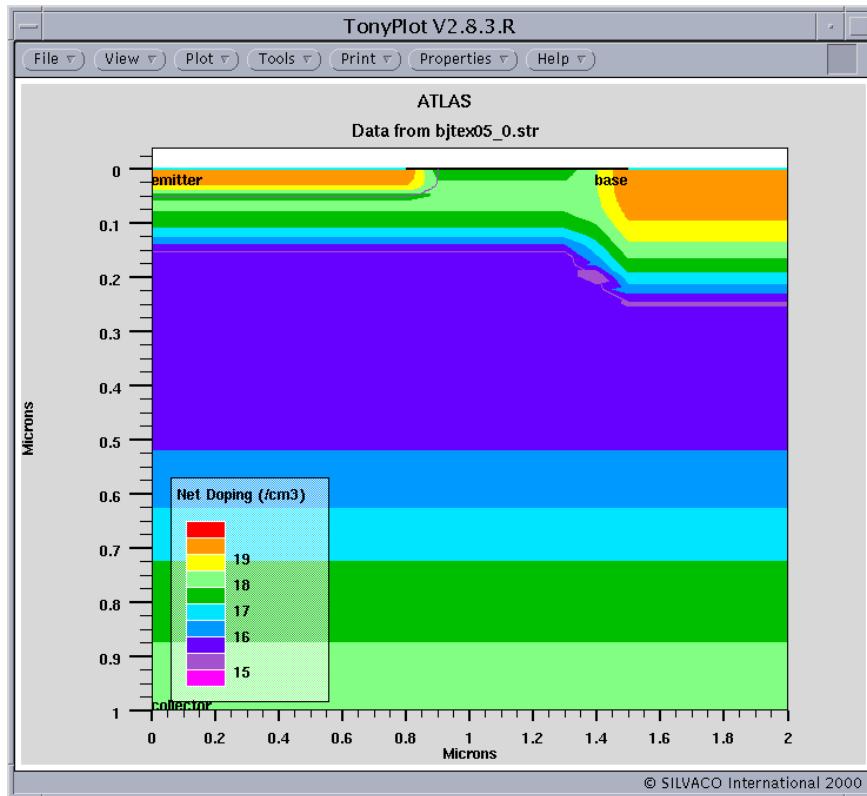


Figure 3.10: Doping profile and junctions of planar bipolar device defined using ATLAS syntax

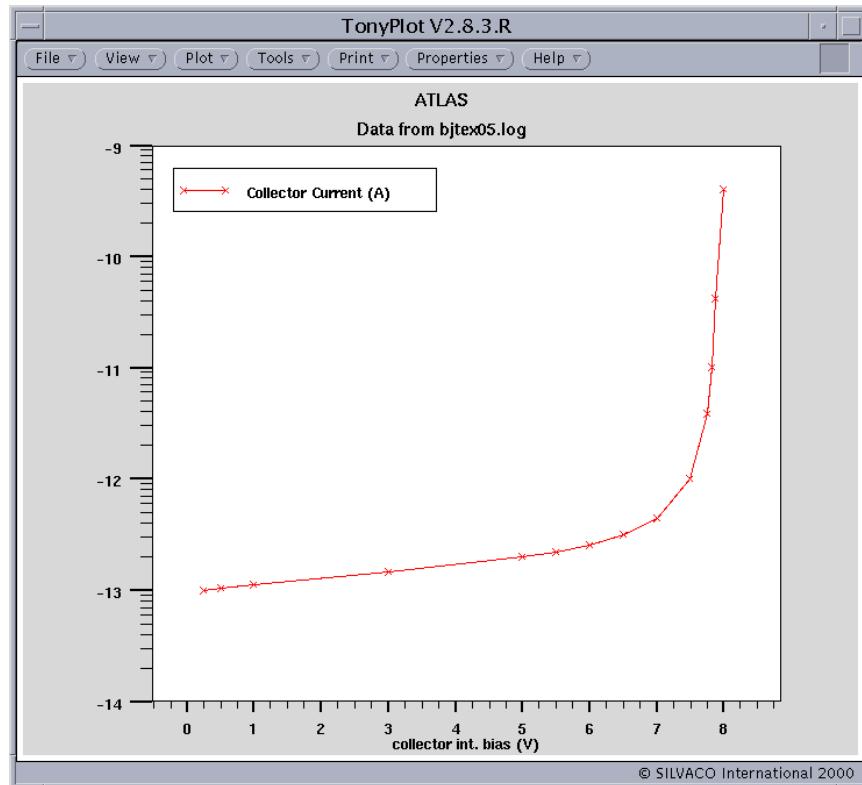


Figure 3.11: BVCEO curve for the planar bipolar device. Onset of breakdown is clear from the curve. In ATLAS it is not always necessary to simulate the high current levels test equipment use.

Input File bjt/bjtex05.in:

```

1 go atlas
2 TITLE Bipolar BVCEO simulation
3 # Silvaco International 1994
4
5 mesh
6 x.m l=0 spac=0.1
7 x.m l=2 spac=0.1
8
9 y.m l=0 spac=0.002
10 y.m l=1 spac=0.10
11
12 region num=1 silicon
13
14 electrode num=1 name=emitter left length=0.8
15 electrode num=2 name=base right length=0.5 y.max=0
16 electrode num=3 name=collector bottom
17
18 doping reg=1 uniform n.type conc=5e15
19 doping reg=1 gauss n.type conc=1e18 peak=1.0 char=0.2

```

```
20 doping reg=1 gauss    p.type conc=1e18 peak=0.05 junct=0.15
21 doping reg=1 gauss    n.type conc=5e19 peak=0.0   junct=0.05 x.right=0.8
22 doping reg=1 gauss    p.type conc=5e19 peak=0.0   char=0.08 x.left=1.5
23
24 save outf=bjtex05_0.str
25 tonyplot bjtex05_0.str -set bjtex05_0.set
26
27 # set poly emitter
28 contact name=emitter n.poly surf.rec
29
30 material taun0=5e-6 taup0=5e-6
31
32 # set models
33 models bipolar print
34 impact selb
35
36 solve init
37
38 method newton trap
39
40
41 solve prev
42 solve vbase=0.025
43 solve vbase=0.05
44 solve vbase=0.2
45
46 contact name=base current
47
48
49 method newton trap ir.tol=1.e-20 ix.tol=1.e-20
50
51 solve ibase=3.e-15
52
53 log outf=bjtex05.log master
54
55 # ramp collector voltage
56 solve vcollector=0.25
57 solve vcollector=0.5
58 solve vcollector=1
59 solve vcollector=3
60 solve vcollector=5
61
62 solve vstep=0.5 vfinal=10  name=collector compl=5.e-11 e.comp=3
```

```

63
64
65 # plot results
66 tonyplot bjtex05.log -set bjtex05_log.set
67
68 quit

```

3.1.6. bjtex06.in: NPN - AC Frequency Response

Requires: S-PISCES

This example calculates the frequency response of an NPN transistor at a single DC bias point. It shows:

- formation of an NPN BJT using ATLAS syntax
- DC ramp of Vbe up to 0.8V, with Vce=2.0V
- AC simulation with ramped frequency

The device structure and DC biasing of this device are as described in the NPN Gummel plot example in this section. All models and numerical methods are in common with the other NPN examples.

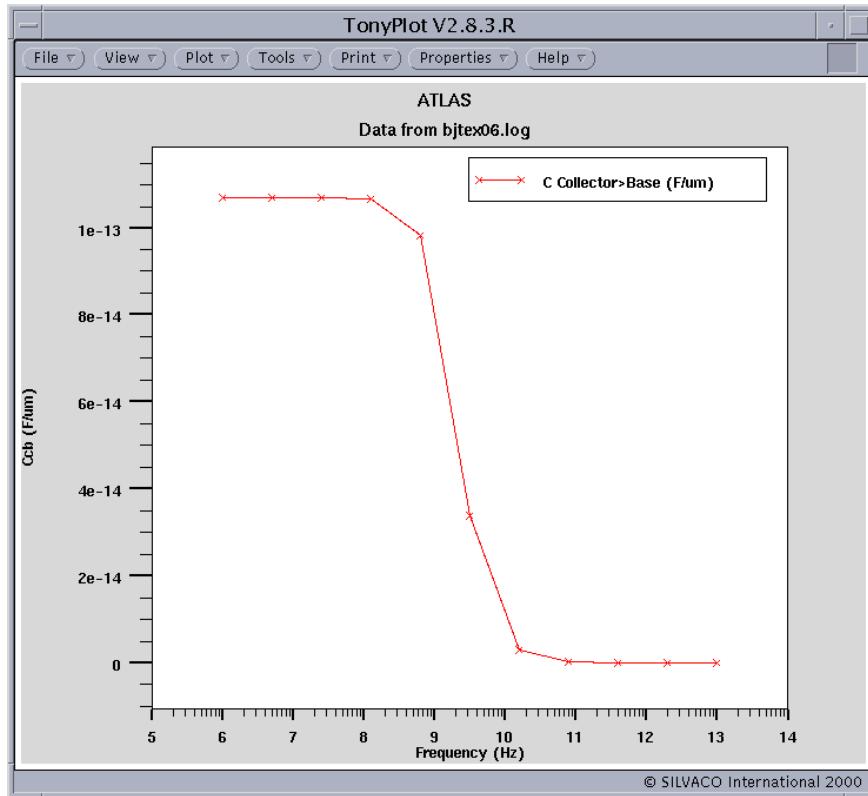
The key line of syntax is:

```
solve prev ac freq=1e6 aname=base fstep=5 mult.f nfstep=10
```

This line specifies the solution of the previous DC bias point with a small AC signal. The `freq` parameter sets the initial frequency. The `aname` parameter sets the contact on which the AC signal is applied. If no `aname` is given, the AC signal is applied to all contacts in turn. The `fstep` parameter sets the step in frequency, `nfstep` sets the number of frequency steps and `mult.f` indicates that this is a multiplier. At each step, the frequency is multiplied by `mult.f` rather than having `mult.f` added to the initial frequency.

The resulting capacitance and conductance parameters are stored in the log file. They can be plotted against log(frequency) to see the frequency response in TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

**Figure 3.12:** Frequency Response of Bipolar Transistor**Input File bjt/bjtex06.in:**

```

1 go atlas
2 TITLE Bipolar frequency response
3 # Silvaco International 1992, 1993, 1994
4
5 mesh
6 x.m l=0 spac=0.1
7 x.m l=2 spac=0.1
8
9 y.m l=0 spac=0.002
10 y.m l=1 spac=0.10
11
12 region num=1 silicon
13
14 electrode num=1 name=emitter left length=0.8
15 electrode num=2 name=base right length=0.5 y.max=0
16 electrode num=3 name=collector bottom
17
18 doping reg=1 uniform n.type conc=5e15
19 doping reg=1 gauss n.type conc=1e18 peak=1.0 char=0.2

```

```

20 doping reg=1 gauss    p.type conc=1e18 peak=0.05 junct=0.15
21 doping reg=1 gauss    n.type conc=5e19 peak=0.0   junct=0.05 x.right=0.8
22 doping reg=1 gauss    p.type conc=5e19 peak=0.0   char=0.08 x.left=1.5
23
24
25 # set poly emitter and lifetimes
26 contact name=emitter n.poly surf.rec
27 material taun0=5e-6 taup0=5e-6
28
29 # set bipolar models
30 models bipolar print
31
32
33 solve init
34
35 save outf=bjtex06.str
36 tonyplot bjtex06.str -set bjtex06.set
37
38 method newton trap
39 solve
40 solve vcollector=2 local
41
42 solve vbase=0.1
43 solve vbase=0.2 vstep=0.05 vfinal=0.8 name=base
44
45 log outf=bjtex06.log master
46 solve prev ac freq=1e6 term=2 fstep=5 mult.f nfstep=10
47
48 # plot results
49 tonyplot bjtex06.log -set bjtex06_log.set
50 quit

```

3.1.7. bjtex07.in: 3D NPN Transient Response

Requires: DEVEDIT3D/DEVICE3D

This examples demonstrates transient simulation of a BJT structure in three dimensions.

In this example a bipolar transistor is constructed using DEVEDIT3D. The structure is then passed to ATLAS for electrical testing. The input file consists of the two following main portions:

- construction of the device in DEVEDIT3D
- simulation of the Gummel plot in ATLAS

The first stage of the input constructs the BJT geometry, material regions, doping profiles, and electrodes in DEVEDIT3D. The structure was created in DEVEDIT3D by drawing the device regions in interactive mode and specifying 3D doping distribution. Finally the mesh was generated

automatically by specifying basic mesh constraints and refining in the important areas of the device.

The ATLAS simulation begins by reading in the structure from DEVEDIT3D. DECKBUILD provides the autointerface between DEVEDIT3D and ATLAS so that the structure produced by DEVEDIT3D is transferred to ATLAS without having to indicate the mesh statement.

The models statement is used to select a set of physical models for this simulation. In this case, these models are SRH and AUGER recombination, the concentration and field dependent mobility model, and two carriers model

Then the initial solution for zero biases is obtained using `solve init`. The next step is the steady-state solution for $V_{eb}=-0.4V$ and $V_{cb}=1V$ is obtained.

The emitter voltage is then ramped to $-0.8V$ with a ramptime of $0.1ns$, and transient simulation are performed. The Newton algorithm, which is the default method in ATLAS is used for these calculations.

The results of simulation are then displayed using TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

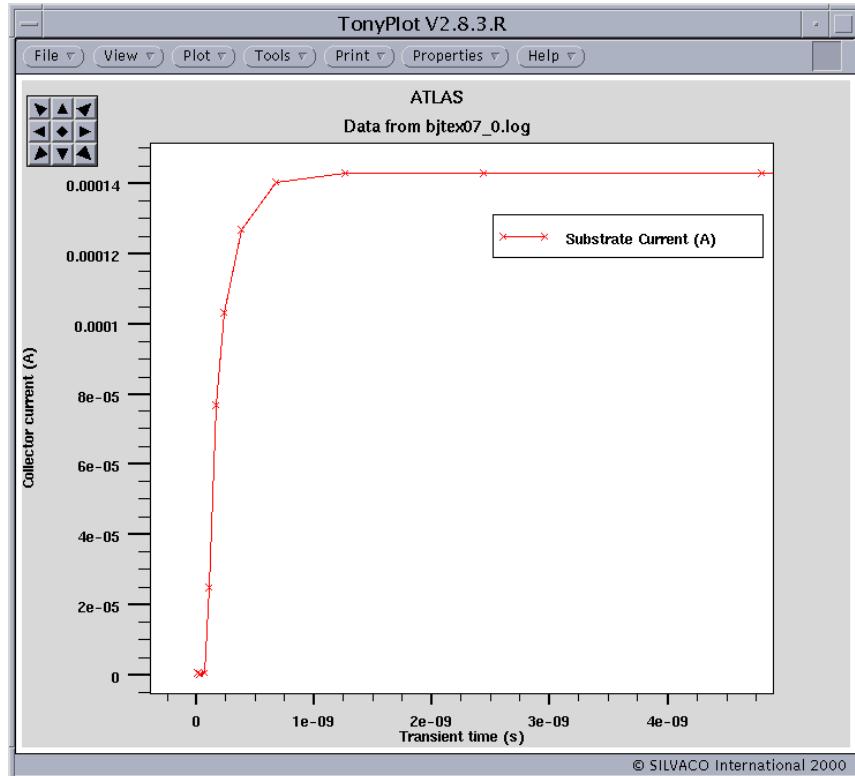


Figure 3.13: Transient switching of collector current in 3D bipolar transistor

Input File bjt/bjtex07.in:

```

1 go DevEdit
2
3 DevEdit version="2.0" library="1.14"
4

```

```
5   work.area left=0 top=-0.5 right=5 bottom=1.6
6
7   # SILVACO Library V1.14
8
9   region reg=1 name=Silicon mat=Silicon color=0xffc000 pattern=0x3 Z1=0
10  Z2=5 \
11  points="0,0 1.5,0 3.5,0 5,0 5,1.5 0,1.5 0,0"
12  #
13  impurity id=1 region.id=1 imp=Phosphorus color=0x906000 \
14  x1=0 x2=0 y1=0 y2=0 \
15  peak.value=1e+16 ref.value=0 z1=0 z2=0 comb.func=Multiply \
16  rolloff.y=both conc.func.y=Constant \
17  rolloff.x=both conc.func.x=Constant \
18  rolloff.z=both conc.func.z=Constant
19  #
20  constr.mesh region=1 default
21
22  region reg=2 name=Emitter mat=Aluminum elec.id=1 work.func=4.1 col-
23  or=0xffc8c8 pattern=0x6 Z1=0 Z2=1.5 \
24  points="0,0 0,-0.15 1.5,-0.15 1.5,0 0,0"
25  #
26  constr.mesh region=2 default
27
28  region reg=3 name=Base mat=Aluminum elec.id=2 work.func=4.1 col-
29  or=0xffc0c0 pattern=0x6 Z1=0 Z2=5 \
30  points="3.5,0 3.5,-0.15 5,-0.15 5,0 3.5,0"
31  #
32  constr.mesh region=3 default
33
34  region reg=4 name=substrate mat=Aluminum elec.id=3 work.func=0 col-
35  or=0xffc8c8 pattern=0x6 Z1=0 Z2=5 \
36  points="0,1.5 5,1.5 5,1.6 0,1.6 0,1.5"
37  #
38  constr.mesh region=4 default
39
40  impurity id=1 imp=Boron color=0x906000 \
41  x1=0 x2=5 y1=0 y2=0 \
42  peak.value=5e+18 ref.value=0 z1=0 z2=5 comb.func=Multiply \
43  rolloff.y=both conc.func.y=Gaussian conc.param.y=0.16 \
44  rolloff.x=both conc.func.x=Gaussian conc.param.x=0.25 \
45  rolloff.z=both conc.func.z=Gaussian conc.param.z=0.25
46  impurity id=2 imp=Arsenic color=0x906000 \
47  x1=0 x2=5 y1=1.5 y2=1.5 \
```

```
45 peak.value=4e+19 ref.value=0 z1=0 z2=5 comb.func=Multiply \
46 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.1 \
47 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.25 \
48 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.25
49 impurity id=3 imp=Arsenic color=0x906000 \
50 x1=0 x2=1.5 y1=0 y2=0 \
51 peak.value=1e+20 ref.value=0 z1=0 z2=1.5 comb.func=Multiply \
52 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.1 \
53 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.1 \
54 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.1
55
56 # Set Meshing Parameters
57 #
58 base.mesh height=1000000 width=1000000
59 #
60 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
       line.straightening=1 align.points when=automatic
61 #
62 imp.refine imp="NetDoping" sensitivity=0.25
63 imp.refine min.spacing=0.05 z=0
64 #
65 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
66 max.width=1 min.height=0.0001 min.width=0.0001
67 #
68 constr.mesh type=Semiconductor default
69 #
70 constr.mesh type=Insulator default
71 #
72 constr.mesh type=Metal default
73 #
74 constr.mesh type=Other default
75 #
76 constr.mesh region=1 default
77 #
78 constr.mesh region=2 default
79 #
80 constr.mesh region=3 default
81 #
82 constr.mesh region=4 default
83 #
84 # Perform mesh operations
85 #
86 Mesh Mode=MeshBuild
```

```
87
88 imp.refine imp="NetDoping" sensitivity=0.25
89 imp.refine min.spacing=0.05 z=0
90
91 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
92 max.width=1 min.height=0.0001 min.width=0.0001
93 #
94 constr.mesh type=Semiconductor default
95 #
96 constr.mesh type=Insulator default
97 #
98 constr.mesh type=Metal default
99 #
100 constr.mesh type=Other default
101
102 z.plane z=0 spacing=1.5
103 #
104 z.plane z=1.55 spacing=0.05
105 #
106 z.plane z=2 spacing=1
107 #
108 z.plane max.spacing=1000000 max.ratio=1.5
109
110 base.mesh height=1000000 width=1000000
111
112 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
     line.straightening=1 align.Points when=automatic
113 structure outf=bjtex07_0.str
114
115 go atlas
116 #
117 models    srh auger bgn conmob fldmob
118 #
119 solve init
120 #
121 solve v1=-0.4 v3=1.
122 #
123 log outfile=bjtex07_0.log
124 solve v1=-0.8 ramptime=0.1e-9 tstep=0.01e-9 tfinal=2.e-8
125 #
126 tonyplot bjtex07_0.log -set bjtex07_0.set
127 #
128 quit
```

3.1.8. **bjtex08.in**: PNP Gummel Plot and Ic/Vce Characteristic

Requires: SSUPREM4/S-PISCES

This example demonstrates the formation and characterization of a PNP bipolar transistor. It consists of:

- structure formation in ATHENA
- Gummel plot simulation in ATLAS
- Ic/Vce simulation in ATLAS

The first part of this input file uses ATHENA to construct the geometry and doping of the PNP transistor. The device is a polysilicon emitter PNP with an emitter length of 0.4um. Since the device is symmetrical through the center of the emitter, only half the device needs to be simulated. The resulting currents from ATLAS can always be doubled to account for this reflection. The intrinsic base is formed by a 100keV phosphorus implant at the start of the process. Extrinsic base is formed by spacers on the sidewall of the emitter polysilicon. The emitter area is formed by p+ doped polysilicon directly deposited onto the silicon.

At the end of the process, metal contacts are patterned to give an emitter contact on top of the polysilicon and a base contact to the right. These metal regions are defined as electrodes in ATHENA to prepare the structure for ATLAS.

The final step in the process simulation is to extract some process parameters. The base width is extracted by measuring the base/collector and emitter/base junctions individually and subtracting the two results. Using the 1D Poisson solver in DECKBUILD the sheet resistances of the base and polysilicon emitter region are obtained.

The first of the two ATLAS runs in this file is to extract the Gummel plot characteristics. From this plot, the gain and fT can be obtained. The material parameters for polysilicon and silicon regions are set in separate lines in the ATLAS input file.

The material parameters for polysilicon reflect the low mobility and short carrier lifetimes seen in this material. They also contribute to the reduction in base current and consequent increase in gain seen in polysilicon emitter bipolar transistors. The effect of the native oxide layer that exists between the polysilicon and silicon is emulated by these material parameters. The effect of the native oxide is to force recombination of carriers at the polysilicon/silicon interface rather than the carriers diffusing further in to emitter region. The short lifetime and low mobility in the polysilicon accomplish the same effect and have been widely used in polysilicon emitter bipolar device simulation.

The Gummel plot is simulated at Vce=-2.0V by ramping Vbe from -0.4 to -1.0V. In addition to the DC solution, a small AC signal is also applied. This enables fT vs. Ic to be extracted. The AC signal is specified using the parameter, AC, on the solve statement. The frequency of this signal is 1MHz. At the end of the solve sequence several device parameters are extracted: peak gain, peak collector current and peak fT.

The second ATLAS run extracts a family of Ic/Vce curves for different base currents. For each curve it is necessary to force a constant current through the base electrode. This is done using the current boundary condition set by contact name=base current.

Since the base currents used are quite high, it is easier to first ramp the base voltage up close to the initial current level required. In this case Vbe is ramped to -0.7V. Then the current boundary conditions are applied and solutions for base currents of 1uA/um to 5uA/um were obtained. At each step in Ib a solution file is stored for later use.

During the ramp up and storing of files with different Ib the collector voltage is left at ground. Next a sequence of statements is used to **Load** the stored file for a particular Ib value, open a **log** file for the results, and **solve** a ramp of collector voltage to -5V. This sequence is repeated for each Ib considered. Separate results files for each Ib value are recommended for use in TONYPLOT and for extracting parameters from the results. It is possible to store all IV data output for this simulation

into one file. A full bipolar extraction for SPICE models can be done by interfacing these log files with UTMOST.

Finally some extraction on the Ic/Vce data with Ib=5uA/um is done. The peak current in mA, the peak slope in the linear region and the slope of the saturation region can all be obtained using extract.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

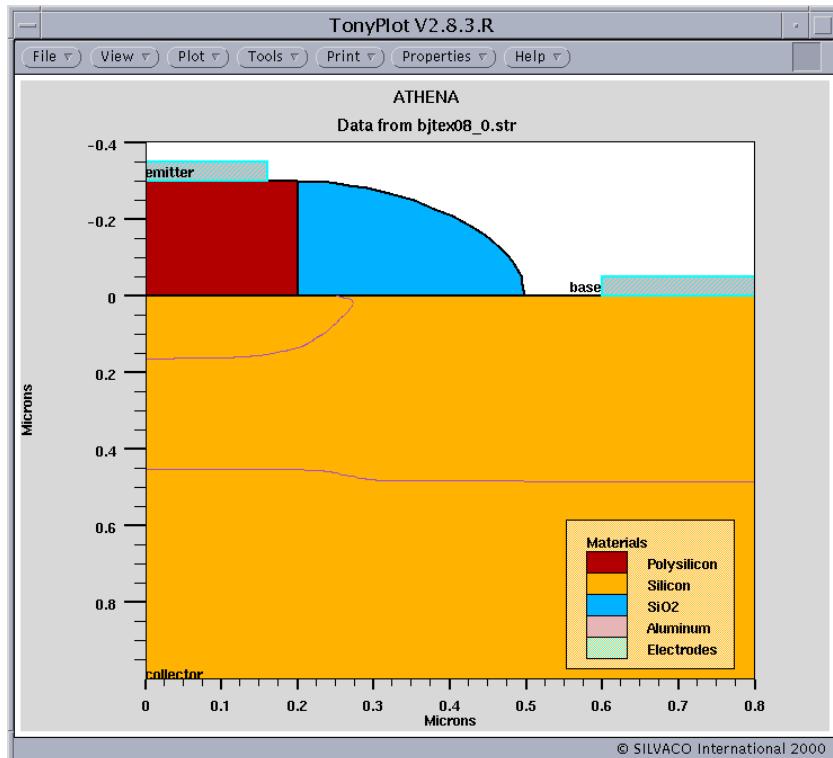


Figure 3.14: Poly Emitter PNP BJT showing junction and electrode location

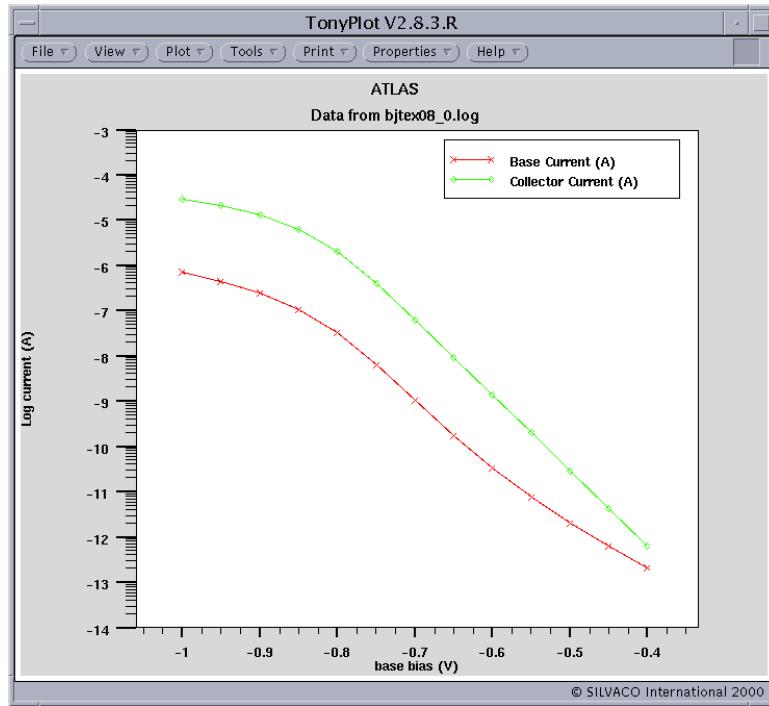


Figure 3.15: Gummel Plot for PNP device. Gain can be extracted from a function as I_c/I_b

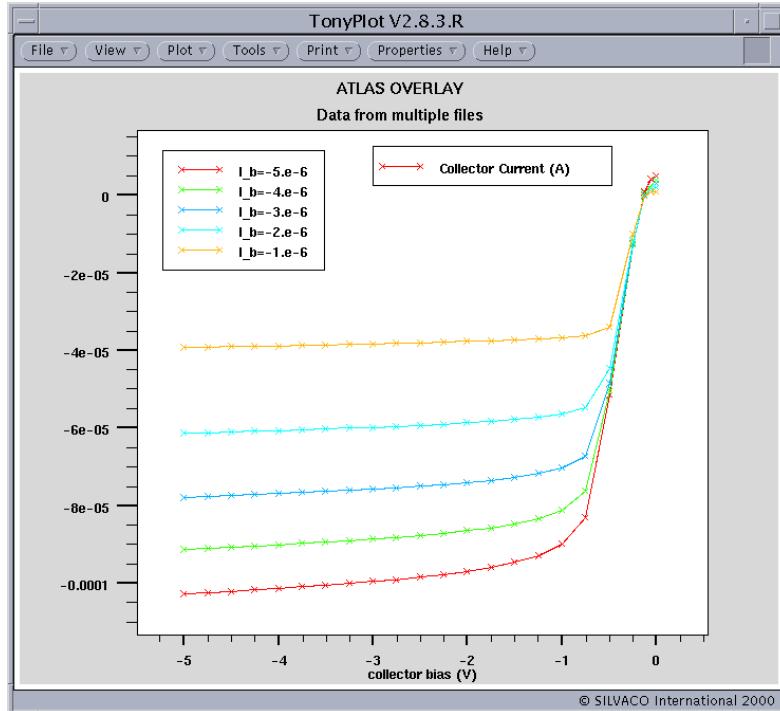


Figure 3.16: I_c/Vce curves for PNP device

Input File bjt/bjtex08.in:

1 go athena

```
2 #TITLE: Polysilicon Emitter Bipolar Example (PNP)
3 #Silvaco International 1994
4
5 line x loc=0.0      spacing=0.03
6 line x loc=0.2      spacing=0.02
7 line x loc=0.24     spacing=0.01
8 line x loc=0.3      spacing=0.015
9 line x loc=0.8      spacing=0.15
10
11 line y loc=0.0      spacing=0.01
12 line y loc=0.1      spacing=0.01
13 line y loc=0.4      spacing=0.02
14 line y loc=0.5      spacing=0.06
15 line y loc=1.0      spacing=0.15
16
17 init boron conc=2e16
18
19 # base implant
20 implant phos energy=100 dose=8e13
21
22 # base drive
23 diffuse time=5 temp=900
24
25 # deposit polysilicon
26 deposit poly thick=0.3 divisions=6 min.space=0.05
27
28 # Implant to dope polysilicon
29 implant bf2 dose=3e15 energy=35
30
31 # Pattern the poly
32 etch poly right p1.x=0.2
33
34 # relax the mesh in the substrate and extrinsic areas
35 relax y.min=.5
36 relax x.min=0.4
37
38 # emitter drive
39 method compress fermi
40 diffuse time=45 temp=900 nitrogen
41
42 # extrinsic emitter implant under spacer
43 implant phos dose=2e14 energy=70
44
```

```
45 # deposit spacer
46 deposit oxide thick=0.3 divisions=10 min.space=0.1
47
48 # etch the spacer back
49 etch oxide dry thick=0.3
50
51 # n+ base contact implant
52 implant arsenic dose=1e15 energy=50
53
54 # contact drive
55 diffuse time=30 temp=900 nitrogen
56
57
58 # put down Al and etch to form contacts
59 deposit alum thick=0.05 div=2
60
61 etch alum start x=0.16 y=-4
62 etch continue x=0.16 y=0.2
63 etch continue x=0.6 y=0.2
64 etch done x=0.6 y=-4
65
66
67
68 # Name the electrodes for use with Atlas
69 electrode x=0.0 name=emitter
70 electrode x=0.7 name=base
71 electrode backside name=collector
72
73
74
75 # extract junction depths
76 extract name="EB_xj" xj material="Silicon" mat.occno=1 x.val=0.1 junc.oc-
    cno=1
77 extract name="BC_xj" xj material="Silicon" mat.occno=1 x.val=0.1 junc.oc-
    cno=2
78 extract name="base_width" $BC_xj - $EB_xj
79
80 #extract 1D electrical parameters
81 extract name="base_rho" n.sheet.res material="Silicon" mat.occno=1
    x.val=0.1 region.occno=2
82 extract name="poly_emitter_rho" p.sheet.res material="Polysilicon"
    mat.occno=1 x.val=0.1 region.occno=1 semi.poly
83
84
```

```
85
86 # Save the final structure
87 structure outfile=bjtex08_0.str
88 tonyplot bjtex08_0.str -set bjtex08_0.set
89
90
91
92
93
94 ##### Gummel Plot Test #####
95
96
97
98 go atlas
99
100 # set poly lifetime and mobility
101 material material=Polysilicon taun0=1e-9 taup0=1e-9 mun=40 mup=2
102 material material=Silicon      taun0=5e-6 taup0=5e-6
103
104 models
105 models material=Silicon bipolar print
106 models material=Polysilicon srh
107
108 solve init
109
110 method newton autonr trap
111 solve prev
112
113 solve vcollector=-2
114 solve vbase=-0.1 vstep=-0.1 vfinal=-0.4 name=base
115
116
117 log outf=bjtex08_0.log
118
119 solve vbase=-0.4 vstep=-0.05 vfinal=-1.0 name=base ac freq=1e6 aname=base
120
121 # extract electrical parameters
122 extract name="peak collector current" max(abs(i."collector"))
123
124 extract name="peak gain" max(i."collector"/ i."base")
125
126 extract name="max fT" max(g."collector" "base" / (2*3.1415*c."base" "base"))
127
```

```
128 tonyplot bjttx08_0.log -set bjttx08_0_log.set
129
130
131
132 go atlas
133 # IV/VCE simulation for PNP
134 # SILVACO International 1994
135
136 # set poly lifetime and mobility
137 material material=Polysilicon taun0=1e-9 taup0=1e-9 mun=40 mup=2
138 material material=Silicon      taun0=5e-6 taup0=5e-6
139 models
140 models material=Silicon bipolar print
141 models material=Polysilicon srh
142
143 solve init
144
145 solve vbase=-0.025
146 solve vbase=-0.05
147 solve vbase=-0.1 vstep=-0.1 vfinal=-0.7 name=base
148
149
150 # switch to current boundary conditions
151
152 contact name=base current
153
154 # ramp IB and save solutions
155
156
157 solve ibase=-1.e-6 outf=bjttx08_1.str master
158 solve ibase=-2.e-6 outf=bjttx08_2.str master
159 solve ibase=-3.e-6 outf=bjttx08_3.str master
160 solve ibase=-4.e-6 outf=bjttx08_4.str master
161 solve ibase=-5.e-6 outf=bjttx08_5.str master
162
163
164
165 # load in each initial guess file and ramp VCE
166
167 load inf=bjttx08_1.str master
168 log outf=bjttx08_1.log
169 solve vcollector=0.0 vstep=-0.25 vfinal=-5.0 name=collector
170
```

```

171
172 load inf=bjtex08_2.str master
173 log outf=bjtex08_2.log
174 solve vcollector=0.0 vstep=-0.25 vfinal=-5.0 name=collector
175
176 load inf=bjtex08_3.str master
177 log outf=bjtex08_3.log
178 solve vcollector=0.0 vstep=-0.25 vfinal=-5.0 name=collector
179
180 load inf=bjtex08_4.str master
181 log outf=bjtex08_4.log
182 solve vcollector=0.0 vstep=-0.25 vfinal=-5.0 name=collector
183
184 load inf=bjtex08_5.str master
185 log outf=bjtex08_5.log
186 solve vcollector=0.0 vstep=-0.25 vfinal=-5.0 name=collector
187
188 # extract peak current and slopes
189 extract name="pnp_max_ic_mA" max(abs(i."collector"))*1.0e+3
190 extract name="pnp_lin_slope" slope(maxslope(curve(v."collector",i."col-
    lector")))
191 extract name="pnp_sat_slope" slope(minslope(curve(v."collector",i."col-
    lector")))
192
193 tonyplot -overlay bjtex08_5.log bjtex08_4.log bjtex08_3.log bjtex08_2.log
      bjtex08_1.log -set bjtex08_1_log.set
194
195
196 quit

```

3.1.9. bjtex09.in: Emitter-Coupled Logic Element Simulation

Requires: S-PISCES/MIXEDMODE

This simulation shows a transient process of gate switching in an ECL circuit. A SPICE-like circuit description is used by ATLAS/MIXEDMODE to specify two ECL inverters. Two NPN transistors modeled using device simulation are included in the circuit alongside two devices simulated using a simple SPICE model. This example shows:

- specification of an NPN device using ATLAS syntax
- specification of an ECL inverter circuit using MIXEDMODE netlist syntax.
- inclusion of two S-PISCES devices within the SPICE circuit.
- specification of device simulation models and parameters in MIXEDMODE syntax
- simulation of the DC initial bias point
- simulation of transient switching characteristics

This example file consists of three runs. The first uses ATLAS syntax to define the NPN device geometry, mesh and doping, the second sets up the MIXEDMODE circuit to simulate the initial DC bias point, the third performs the transient circuit simulation using ATLAS/MIXEDMODE.

The first run uses ATLAS syntax to define the NPN structure. There are two identical NPN devices in the ECL circuit. Both devices can be loaded from a single mesh file `bjtex09_0.str`.

The second run starts with a netlist description of the ECL circuit. For details of the syntax used in MIXEDMODE, please see the MIXEDMODE section of ATLAS Manual. The key non-standard element in the circuit is the ATLAS device. These are circuit elements where ATLAS device simulation is used to give the terminal characteristics as opposed to a SPICE model equation. The primitives letter `a` is used to identify these devices. In this example there are two such primitives; `ai` and `an`. There are also two more NPN bipolar transistors simulated using the SPICE model modbjt. These are labeled `qi` and `qn`.

After the `.end` statement, regular S-PISCES syntax is used to define parameters for the device simulation. `Models` is used to set the physical models to be used in each of the devices to be modeled by device simulation. Note use of the `device=<name>` parameter. This is compulsory in MIXED-MODE simulation to identify the device to which these parameters are applied. This is true even if only one device simulation element exists in the circuit.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

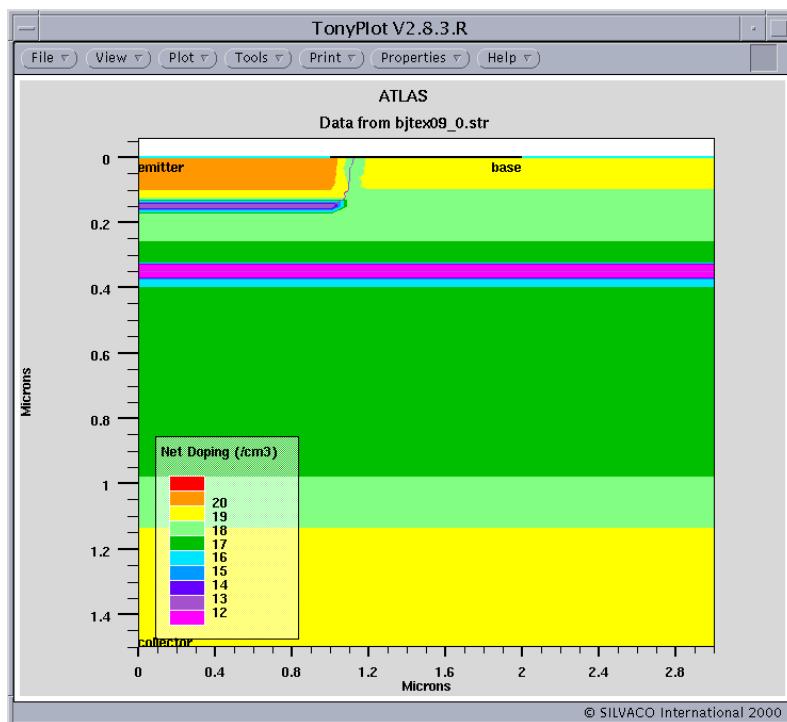


Figure 3.17: Device Structure and doping as input to the MIXEDMODE simulation

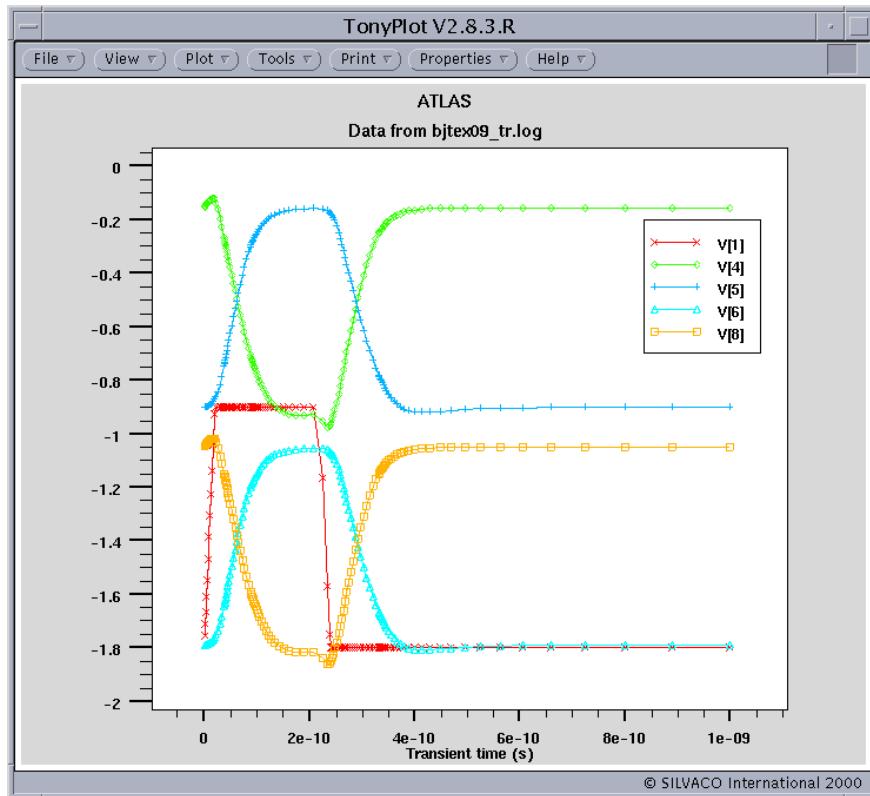


Figure 3.18: Switching waveforms from the ECL inverter simulation

Input File bjt/bjtex09.in:

```

1 go atlas
2 #   SILVACO International, 1992, 1993, 1994
3 #
4 mesh      nx=31 ny=31
5 x.m      n=1    l=0.0    r=1.0
6 x.m      n=31   l=3.0    r=1.0
7 y.m      n=1    l=0.0    r=1.0
8 y.m      n=7    l=0.15   r=1.0
9 y.m      n=20   l=0.5    r=1.0
10 y.m     n=31   l=1.5    r=1.0
11 #
12 region   num=1 silicon
13 #
14 #   Electrodes #1 -emitter; #2 -base; #3 -collector
15 #
16 elec     num=1 left  length=1.0 name=emitter
17 elec     num=2 right length=1.0 name=base
18 elec     num=3 substrate       name=collector
19 #

```

```
20 # Impurity profile
21 #
22 doping uniform conc=3.0e16 n.type
23 doping gauss conc=5.0e18 p.type junc=0.35
24 doping gauss conc=5.0e20 n.type junc=0.15 x.r=1.0 ratio=0.75
25 doping gauss conc=2.e19 n.type char=0.2 peak=1.4
26
27 save outf=bjtex09_0.str
28 tonyplot bjtex09_0.str -set bjtex09_0.set
29 #
30
31 go atlas
32 .begin
33 #
34 # ECL inverter - DC point simulation
35 # SILVACO International, 1992
36 #
37 vin 1 0 -1.8
38 ai 1=base 4=collector 2=emitter infile=bjtex09_0.str width=1.
39 an 3=base 5=collector 2=emitter infile=bjtex09_0.str width=1.
40 rci 4 0 2k
41 rcn 5 0 2k
42 vref 3 0 -1.4
43 iee 2 7 0.4mA
44 ree 2 7 100k
45 vcc 7 0 -5.2
46 rei 8 7 500
47 ren 6 7 500
48 cei 8 0 5f
49 cen 6 0 5f
50 qi 0 4 8 7 modbjt
51 qn 0 5 6 7 modbjt
52 #
53 .model modbjt npn is=1.e-17 bf=100 cje=1f tf=5ps cjc=0.3f rb=100 \
54 rbm=20
55 #
56 .nodeset v(1)=-1.8 v(2)=-1.8 v(3)=-1.4 v(4)=-1. v(5)=-1. v(6)=-1. v(7)=-
5.2 v(8)=-1.8
57 .numeric vchange=0.25 imaxdc=50
58 .options m2ln print
59 #
60 .save outfile=ecldc
61 #
```

```
62 .end
63 #
64 #      ATLAS models
65 #
66 models device=ai reg=1 bipolar
67 models device=an reg=1 bipolar
68
69 go atlas
70 .begin
71 #
72 #      ECL inverter - transient simulation
73 #
74 vin 1 0  -1.8 pulse -1.8 -0.9 0. 20ps 20ps 200ps 2000
75 ai      1=base 4=collector 2=emitter infile=bjtex09_0.str width=1.
76 an      3=base 5=collector 2=emitter infile=bjtex09_0.str width=1.
77 rci     4 0  2k
78 rcn     5 0  2k
79 vref    3 0  -1.4
80 iee     2 7   0.4mA
81 ree     2 7   100k
82 vcc     7 0   -5
83 rei     8 7   500
84 ren     6 7   500
85 cei     8 0   5f
86 cen     6 0   5f
87 qi      0 4 8 7 modbjt
88 qn      0 5 6 7 modbjt
89 #
90 .model modbjt npn is=1.e-17 bf=100 cje=1f tf=5ps cjc=0.3f rb=100 \
91 rbm=20
92 #
93 .options print
94 #
95 .log outfile=bjtex09
96 .load infile=ecldc
97 #
98 .tran 1ps 1ns
99 #
100 .end
101 #
102 #      ATLAS device Input File
103 #
104 models device=ai reg=1 bipolar
```

```
105 models device=an reg=1 bipolar
106
107 go atlas
108 tonyplot bjtex09_tr.log -set bjtex09_tr_log.set
109
110 quit
111
112
113
```

3.1.10. bjtex10.in: SSUPREM3/ATLAS Simulation of an NPN BJT

Requires: SSUPREM3/S-PISCES

This example demonstrates how to use combination of several SSUPREM3 runs and ATLAS to simulate the electrical characteristics of a vertical NPN bipolar transistor. This example shows:

- Four SSUPREM3 simulations of various doping distributions in a 1D NPN bipolar structure
- SSUPREM3-ATLAS interface for 1D doping profiles
- I_c and I_b extraction versus V_{be} (Gummel Plot)

The process simulation is optimized in the example s3ex14.in. See the SSUPREM3 examples section for more details. 1-D process simulation is taken as the starting point for this simulation. P+ and n+ contact implants and final anneal are added at the very end.

The input file is run four times with different steps commented out. As the result, four doping profiles in different vertical sections of the NPN device are obtained. The structure file names correspond to areas where the vertical sections are taken.

When all four SSUPREM3 simulations are completed DECKBUILD switches simulation to ATLAS where mesh and electrodes are set. After that, doping profiles from all four SSUPREM3 structures are used to build 2-D doping in ATLAS. Uniform antimony (buried layer) and arsenic (epi layer) profiles are imported from bjtex10_1.str. Afterwards, emitter doping is specified in the area between $x=0$ and $x=1$ using phosphorus component of the bjtex10_1.str profile. The parameter, ratio.lat, represent lateral diffusion during emitter formation. Base boron doping is specified in the area between $x=0$ and $x=5$ from bjtex10_2.str. P+ contact boron doping and N+ phosphorus doping under collector contact are imported from corresponding SSUPREM3 structure files.

A standard Gummel plot simulation with ATLAS is then performed. This is described in detail in the first example in this section.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory . Once loaded into DECKBUILD, select the **run** button to execute the example.

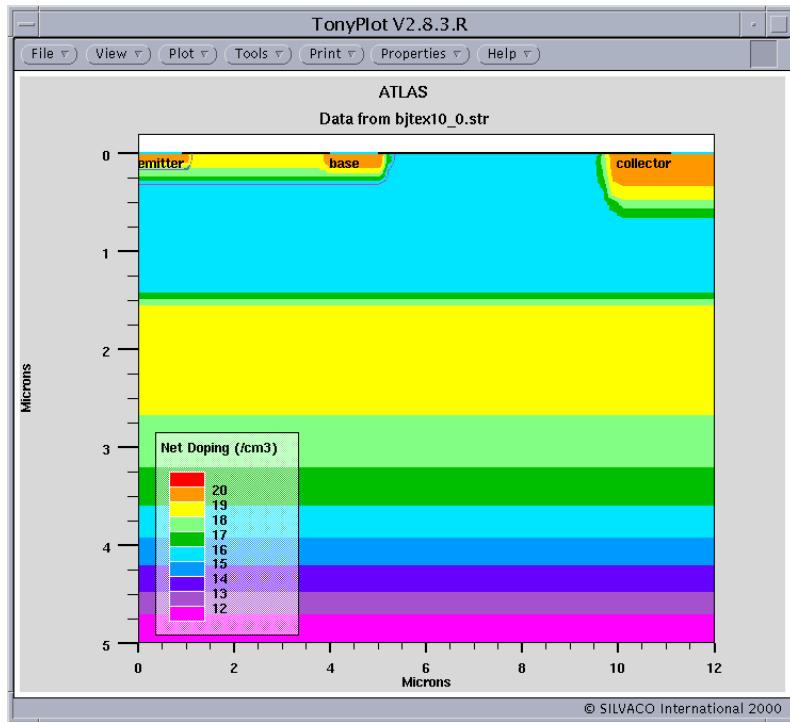


Figure 3.19: 2D Bipolar Structure and doping created in ATLAS from multiple 1D SSUPREM3 process simulations

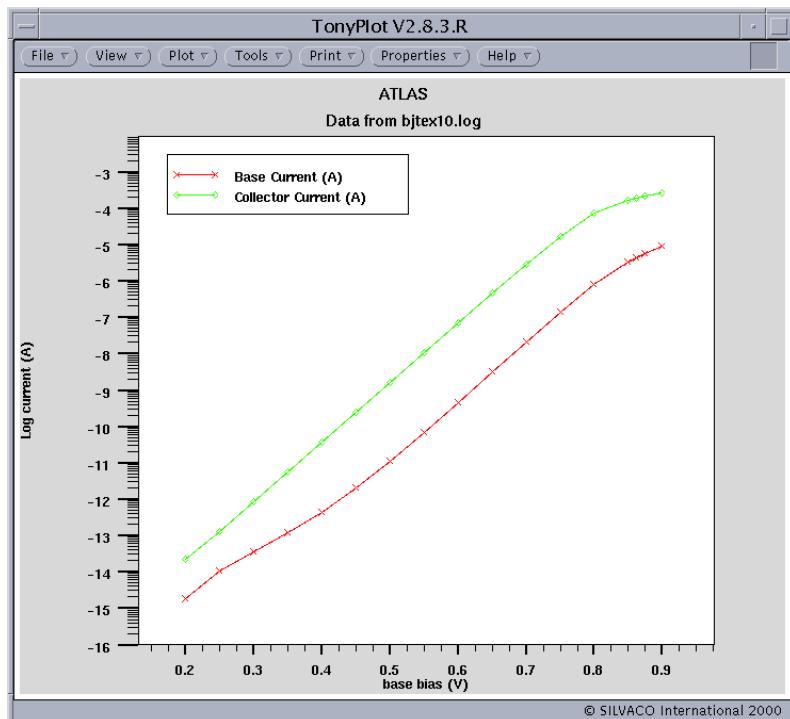


Figure 3.20: Extracted ATLAS results from device using SSUPREM3 doping

Input File bjt/bjtex10.in:

```
1 go ssuprem3
2 Title      Combined SSUPREM3/ATLAS Simulation of Bipolar Device
3 #
4 # First run: Through emitter
5 #
6 Initialize <100> Silicon Thick=5. \
7           dx=.01 XdX=.05 Spaces=100
8
9
10 #          Implant and drive-in the antimony buried layer.
11 Implant    Antimony Dose=5E14 Energy=120
12 Diffusion   Temperature=1150 Time=15 DryO2
13 Diffusion   Temperature=1150 Time=300
14
15 Etch       Oxide all
16
17 #          Epi-layer formation
18 Epitaxy    Temperature=1050 Time=4 Growth.Rate=.4 \
19           Arsenic Gas.Conc=5E15
20
21 #          Base screen oxide
22 diffuse    time=20 temp=950 wet
23
24 #          Base implant
25 Implant    Boron Dose=5E13 Energy=40 am
26
27 #          Base drive
28 diffuse    time=30 temp=950
29
30 etch oxide all
31
32 #          Polysilicon deposition
33 Deposit    Polysilicon Thickness=.5 Temp=620
34
35 #          Polyemitter implant
36 implant    phos energy=40 dose=5e15
37
38 #          emitter drive-in
39 Diffusion   Temperature=1000 Time=10
40
41 #          p+ contact implant
42 #implant   boron dose=7e14 energy=40
```

```
43 # n+ contact implant
44 #implant phos dose=4e15 energy=40
45 # final anneal
46 diffuse time=60 temp=900
47 etch oxide all
48 etch poly all
49 # Extract base sheet resistance
50 extract name="bshro" sheet.res material="Silicon" mat.occno=1 region.oc-
    cno=1
51
52 # Extract basewidth
53 extract name="Xj1" xj silicon mat.occno=1 junc.occno=1
54 #
55 extract name="Xj2" xj silicon mat.occno=1 junc.occno=2
56 #
57 extract name="basewidth" $Xj2 - $Xj1
58
59 Structure outfile=bjtex10_1.str
60
61 #
62 # Second run: Through base
63 #
64 Initialize <100> Silicon Thick=5. \
65             dX=.01 xdx=.05 Spaces=100
66
67
68 # Implant and drive-in the antimony buried layer.
69 Implant Antimony Dose=5E14 Energy=120
70 Diffusion Temperature=1150 Time=15 DryO2
71 Diffusion Temperature=1150 Time=300
72
73 Etch Oxide all
74
75 # Epi-layer formation
76 Epitaxy Temperature=1050 Time=4 Growth.Rate=.4 \
77             Arsenic Gas.Conc=5E15
78
79 # Base screen oxide
80 diffuse time=20 temp=950 wet
81
82 # Base implant
83 Implant Boron Dose=5E13 Energy=40 am
84
```

```
85 #           Base drive
86 diffuse      time=30 temp=950
87
88 #etch oxide all
89
90 #           Polysilicon deposition
91 #Deposit    Polysilicon Thickness=.5 Temp=620
92
93 #           Polyemitter implant
94 #implant   phos energy=40 dose=5e15
95
96 #           emitter drive-in
97 Diffusion   Temperature=1000 Time=10
98
99 #           p+ contact implant
100 #implant   boron dose=7e14 energy=40
101 #           n+ contact implant
102 #implant   phos dose=4e15 energy=40
103 #           final anneal
104 diffuse     time=60 temp=900
105 etch oxide all
106 struct outfile=bjtex10_2.str
107 extract name="basexj" xj silicon mat.occno=1 junc.occno=1
108
109 #
110 # Third run run: Through P= contact
111 #
112 Initialize <100> Silicon Thick=5. \
113             dX=.01 XdX=.05 Spaces=100
114
115
116 #           Implant and drive-in the antimony buried layer.
117 Implant     Antimony Dose=5E14 Energy=120
118 Diffusion   Temperature=1150 Time=15 DryO2
119 Diffusion   Temperature=1150 Time=300
120
121 Etch        Oxide all
122
123 #           Epi-layer formation
124 Epitaxy    Temperature=1050 Time=4 Growth.Rate=.4 \
125             Arsenic Gas.Conc=5E15
126
127 #           Base screen oxide
```

```
128 diffuse      time=20 temp=950 wet
129
130 #           Base implant
131 #Implant    Boron Dose=5E13 Energy=40 am
132
133 #           Base drive
134 diffuse      time=30 temp=950
135
136 #etch oxide all
137
138 #           Polysilicon deposition
139 #Deposit     Polysilicon Thickness=.5 Temp=620
140
141 #           Polyemitter implant
142 #implant    phos energy=40 dose=5e15
143
144 #           emitter drive-in
145 Diffusion    Temperature=1000 Time=10
146
147 #           p+ contact implant
148 implant      boron dose=8e14 energy=30 am
149 #           n+ contact implant
150 #implant    phos dose=4e15 energy=40
151 #           final anneal
152 diffuse      time=60 temp=900
153 etch oxide all
154 struct outfile=bjtex10_3.str
155
156 #
157 # Fourth run: Through collector
158 #
159 Initialize <100> Silicon Thick=5. \
160             dX=.01 XdX=.05 Spaces=100
161
162
163 #           Implant and drive-in the antimony buried layer.
164 Implant      Antimony Dose=5E14 Energy=120
165 Diffusion    Temperature=1150 Time=15 DryO2
166 Diffusion    Temperature=1150 Time=300
167
168 Etch        Oxide all
169
170 #           Epi-layer formation
```

```
171 Epitaxy      Temperature=1050 Time=4 Growth.Rate=.4 \
172          Arsenic Gas.Conc=5E15
173
174 #           Base screen oxide
175 diffuse     time=20 temp=950 wet
176
177 #           Base implant
178 #Implant    Boron Dose=5E13 Energy=40 am
179
180 #           Base drive
181 diffuse     time=30 temp=950
182
183 #etch oxide all
184
185 #           Polysilicon deposition
186 #Deposit    Polysilicon Thickness=.5 Temp=620
187
188 #           Polyemitter implant
189 #implant    phos energy=40 dose=5e15
190
191 #           emitter drive-in
192 Diffusion   Temperature=1000 Time=10
193
194 #           p+ contact implant
195 #implant    boron dose=8e14 energy=30 am
196 #           n+ contact implant
197 implant     phos dose=4e15 energy=80
198 #           final anneal
199 diffuse     time=60 temp=900
200 etch oxide all
201 struct outfile=bjtex10_4.str
202
203 go atlas
204
205 mesh
206 x.m l=0 spac=0.2
207 x.m l=1.2 spac=0.08
208 x.m l=2.7 spac=0.2
209 x.m l=4 spac=0.1
210 x.m l=5 spac=0.1
211 x.m l=7.5 spac=0.5
212 x.m l=9.5 spac=0.2
213 x.m l=12 spac=0.5
```

```
214
215 y.m l=0 spac=0.04
216 y.m l=0.3 spac=0.04
217 y.m l=1.5 spac=0.1
218 y.m l=5 spac=0.5
219
220 eliminate x.min=0 x.max=12 y.min=0.5 y.max=5 columns
221
222 region num=1 silicon
223
224 electrode name=emitter length=1.0
225 electrode name=base x.min=4 length=1.0
226 electrode name=collector right length=1.0
227
228 # emitter
229 doping master inf=bjtex10_1.str antimony
230 doping master inf=bjtex10_1.str arsenic
231 doping master inf=bjtex10_1.str phos x.right=1 ratio.lat=0.75
232 # base
233 doping master inf=bjtex10_2.str boron x.right=5 ratio.lat=0.8
234 # ppcontact
235 doping master inf=bjtex10_3.str boron x.left=4 x.right=5 ratio.lat=0.8
236 # collector
237 doping master inf=bjtex10_4.str phos x.left=10 ratio.lat=0.6
238
239 save outf=bjtex10_0.str
240 tonyplot bjtex10_0.str -set bjtex10_0.set
241
242 contact name=emitter n.poly surf.rec
243 models bipolar print
244 material taun0=1e-6 taup0=1e-6
245
246 solve init
247 method newton trap
248 solve init
249 solve vcollector=2 local
250 solve vbase=0.1
251
252 log outf=bjtex10.log
253 solve vbase=0.2 vstep=0.05 vfinal=0.9 name=base
254
255 tonyplot bjtex10.log -set bjtex10_log.set
```

256

257 quit

3.1.11. **bjtex11.in: NPN - Gummel plot in 2D and 3D**

Requires: SPISCES/DEVICE3D

This example simulates a Gummel plot for a silicon BJT in 2D and 3D. It shows:

- formation of a 2D NPN BJT using ATLAS syntax
- I_c and I_b extraction versus V_{be} (Gummel plot) of the 2D structure
- formation of a 3D NPN BJT using ATLAS syntax
- I_c and I_b extraction versus V_{be} (Gummel plot) of the 3D structure

The initial stage of the example uses the `mesh`, `region`, and `electrode` statements in ATLAS to construct the 2D NPN structure. Analytical doping profiles are added in the `doping` statement. The structure has a heavy n+ emitter, $1.0e18$ peak base concentration, a buried collector layer and heavy p+ extrinsic base contact.

The `models bipolar` statement is set to specify that the default set of bipolar models is to be used. The default set of bipolar models includes: concentration dependent mobility, field dependent mobility, band-gap narrowing, concentration dependent lifetimes and Auger recombination.

The Gummel plot syntax is similar to that described in the first example of this section. Following the calculation of the Gummel plot for the 2D structure, `go atlas` triggers the initiation of an ATLAS run that will be used to perform an equivalent calculation in 3D. The 3D mode of ATLAS is triggered by the inclusion of the `three.d` parameter on the `mesh` statement. The extent in the z-direction is set by the `z.mesh` statements. The syntax for the remainder of the input is similar to that used in 2D.

Following the completion of the calculation of the Gummel plot for the 3D structure, the characteristics of the two structures are plotted for comparison.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory. Once loaded into DECKBUILD, select the **run** button to execute the example.

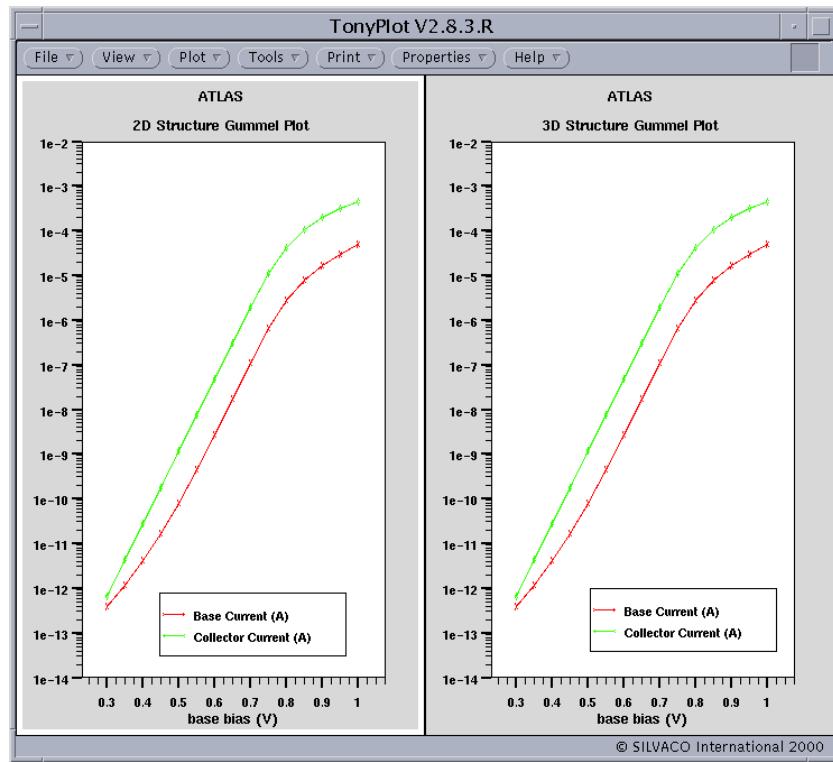


Figure 3.21: Comparison of 2D and 3D results for bipolar device. Current crowding at high V_{be} causes a reduction in current compared with a 2D approximation.

Input File bjt/bjtex11.in:

```

1 go atlas
2 TITLE Bipolar Gummel plot for 2D and 3D
3 # Silvaco International 1992, 1993, 1994
4 mesh
5 x.m l=0    spacing=0.15
6 x.m l=0.8  spacing=0.15
7 x.m l=1.0  spacing=0.03
8 x.m l=1.5  spacing=0.12
9 x.m l=2.0  spacing=0.15
10
11
12 y.m l=0.0  spacing=0.006
13 y.m l=0.04 spacing=0.006
14 y.m l=0.06 spacing=0.005
15 y.m l=0.15 spacing=0.02
16 y.m l=0.30 spacing=0.02
17 y.m l=1.0  spacing=0.12
18
19

```

```
20
21
22 region num=1 silicon
23
24 electrode num=1 name=emitter left length=0.8
25 electrode num=2 name=base      right length=0.5 y.max=0
26 electrode num=3 name=collector bottom
27
28 doping reg=1 uniform n.type conc=5e15
29 doping reg=1 gauss   n.type conc=1e18 peak=1.0 char=0.2
30 doping reg=1 gauss   p.type conc=1e18 peak=0.05 junct=0.15
31 doping reg=1 gauss   n.type conc=5e19 peak=0.0  junct=0.05 x.right=0.8
32 doping reg=1 gauss   p.type conc=5e19 peak=0.0  char=0.08 x.left=1.5
33
34
35 # set bipolar models
36 models bipolar
37
38 # Gummel plot
39 solve vcollector=0.025
40 solve vcollector=0.1
41 solve vcollector=0.25 vstep=0.25 vfinal=2 name=collector
42
43 solve vbase=0.025
44 solve vbase=0.1
45 solve vbase=0.2
46
47
48 log outf=bjtex11_0.log
49 solve vbase=0.3 vstep=0.05 vfinal=1 name=base
50
51
52 go atlas
53
54 mesh three.d
55
56 x.m l=0    spacing=0.15
57 x.m l=0.8  spacing=0.15
58 x.m l=1.0  spacing=0.03
59 x.m l=1.5  spacing=0.12
60 x.m l=2.0  spacing=0.15
61
62
```

```
63 y.m l=0.0 spacing=0.006
64 y.m l=0.04 spacing=0.006
65 y.m l=0.06 spacing=0.005
66 y.m l=0.15 spacing=0.02
67 y.m l=0.30 spacing=0.02
68 y.m l=1.0 spacing=0.12
69
70
71 z.m l=0 spacing=1
72 z.m l=1 spacing=1
73
74 region num=1 silicon
75
76 electrode num=1 name=emitter left length=0.8
77 electrode num=2 name=base      right length=0.5 y.max=0
78 electrode num=3 name=collector bottom
79
80 doping reg=1 uniform n.type conc=5e15
81 doping reg=1 gauss   n.type conc=1e18 peak=1.0 char=0.2
82 doping reg=1 gauss   p.type conc=1e18 peak=0.05 junct=0.15
83 doping reg=1 gauss   n.type conc=5e19 peak=0.0 junct=0.05 x.right=0.8
84 doping reg=1 gauss   p.type conc=5e19 peak=0.0 char=0.08 x.left=1.5
85
86
87 # set bipolar models
88 models bipolar
89
90 # Gummel plot
91 solve vcollector=0.025
92 solve vcollector=0.1
93 solve vcollector=0.25 vstep=0.25 vfinal=2 name=collector
94
95 solve vbase=0.025
96 solve vbase=0.1
97 solve vbase=0.2
98
99
100 log outf=bjtex11_1.log
```

```
101 solve vbase=0.3 vstep=0.05 vfinal=1 name=base  
102  
103 tonyplot bjttx11_0.log bjttx11_1.log -set bjttx11.set  
104  
105 quit  
106
```

4.1. DIODE: Diode Application Examples

4.1.1. diodeex01.in: Schottky Diode Forward Characteristic

Requires: S-PISCES

This example demonstrates simulation of a Schottky Diode Forward Characteristic. It shows:

- formation of a diode structure using ATLAS syntax
- setting of Schottky barrier height for the anode
- forward biasing the anode

In the first part of the input file the device is described, including mesh, electrodes locations, and doping distribution. This is a 2D n-type device with heavily doped floating p-type guard ring regions, located at the left and right sides of the structure. The Schottky anode is located at the top of the device, and a heavily doped cathode is located at the bottom of the device.

After the device description the `model` statement is used to specify the following set of models: carrier concentration dependent mobility (`ccsmob`), field dependent mobility, band-gap narrowing, SRH and Auger recombination. The two carrier model is specified here as well (`carriers=2`).

The key statement for setting a Schottky contact is `contact name=<char> work=<val>`. It is used to specify the workfunction of the Schottky electrode. In this example since the substrate is n-type silicon with an affinity of 4.17, the specified work function of 4.97 provides a Schottky-barrier height of 0.8V. The default barrier height is zero (a perfect ohmic contact). This condition is assumed for the cathode.

The electrical simulation simply ramps the anode voltage to 1.0V in 0.05V steps using the `solve` statement. The results of simulation are then displayed using TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory. Once loaded into DECKBUILD, select the **run** button to execute the example.

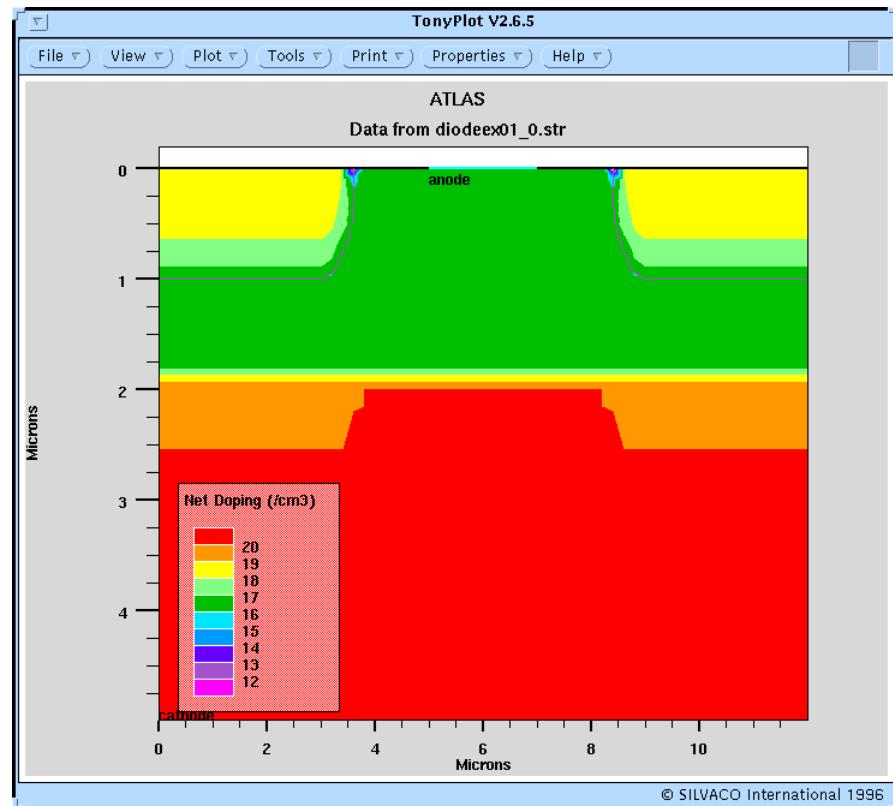


Figure 4.1: Doping for Schottky Diode Structure. The anode is a Schottky contact

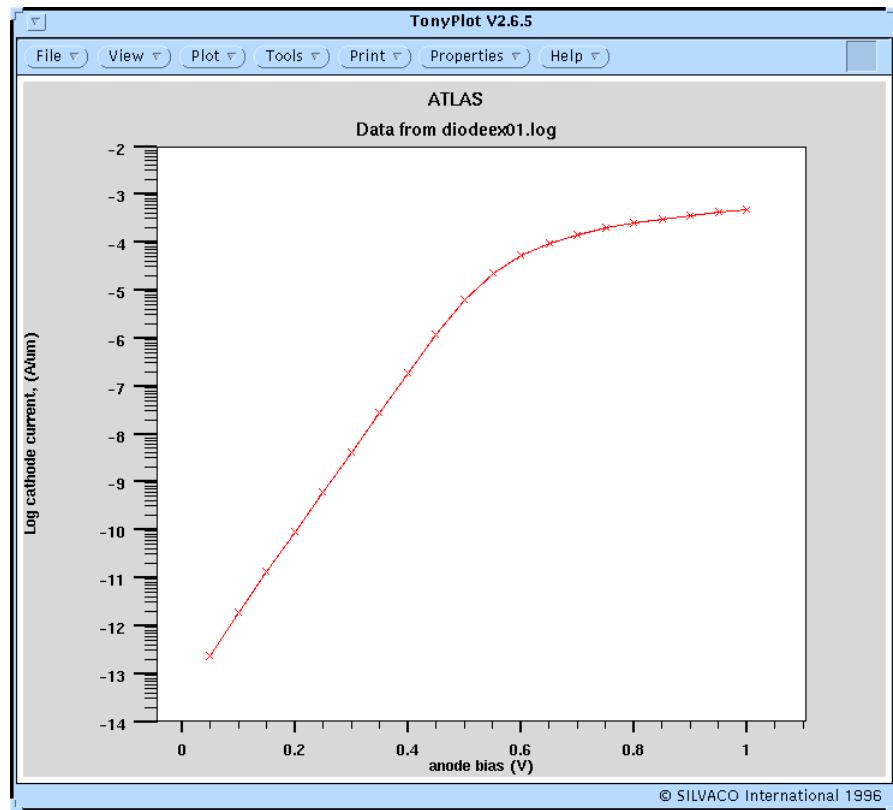


Figure 4.2: Forward characteristics of the Schottky diode

Input File diode/diodeex01.in:

```

1 go atlas
2
3 mesh      nx=36   ny=30
4
5 x.m      loc=0      n=1
6 x.m      loc=3      n=7
7 x.m      loc=4      n=12
8 x.m      loc=5      n=16
9 x.m      loc=7      n=21
10 x.m     loc=8      n=25
11 x.m     loc=9      n=30
12 x.m     loc=12     n=36
13
14
15
16 y.m      loc=0      n=1
17 y.m     loc=0.8    n=9
18 y.m     loc=1.2    n=14
19 y.m     loc=2.0    n=18

```

```
20 y.m      loc=2.2      n=22
21 y.m      loc=5       n=30
22
23 region num=1 silicon
24
25 electr name=anode x.min=5 length=2
26 electr name=cathode bot
27
28 #.... N-epi doping
29 doping n.type conc=5.e16 uniform
30
31 #.... Guardring doping
32 doping p.type conc=1e19 x.min=0 x.max=3 junc=1 rat=0.6 gauss
33 doping p.type conc=1e19 x.min=9 x.max=12 junc=1 rat=0.6 gauss
34
35 #.... N+ doping
36 doping n.type conc=1e20 x.min=0 x.max=12 y.top=2 y.bottom=5 uniform
37
38 save outf=diodeex01_0.str
39 tonyplot diodeex01_0.str -set diodeex01_0.set
40
41
42 model    conmob fldmob srh auger bgn
43 contact   name=anode workf=4.97
44
45 solve     init
46
47 method newton
48
49 log      outfile=diodeex01.log
50 solve     vanode=0.05 vstep=0.05 vfinal=1 name=anode
51 tonyplot diodeex01.log -set diodeex01_log.set
52 quit
53
54
```

4.1.2. diodeex02.in: Breakdown Simulation with EB and NEB Models

Requires: S-PISCES/GIGA

This example demonstrates breakdown simulation of a 1D diode, including second breakdown, with Energy Balance (EB) and Nonisothermal Energy Balance (NEB) Models.

Breakdown simulation for submicron devices should be simulated using Energy Balance Model due to nonlocal impact ionization effects, which can substantially influence device characteristics. For high current levels the thermal self-heating effects can also play an important role by decreasing

the mobility and impact ionization rate. This example demonstrates comparison of breakdown calculations obtained with Energy Balance and Nonisothermal Energy Balance Models.

The first ATLAS run uses the Energy Balance Model: Poisson's equation, carrier continuity equations, and energy balance equation for electrons and holes are solved self-consistently.

In the first part of the input file the device is described, including mesh, electrodes locations, and doping distribution. After the device description the material statement is used to assign energy relaxation times for electrons and holes. The models statement is used to select a set of physical models for this simulation. In this case, these models are SRH and AUGER recombination, the concentration and field dependent mobility model, band gap narrowing, and energy balance equations for electrons and holes (`hcte`). The impact statement is used to assign the energy relaxation lengths for the Selberherr model. The contact statement is used to specify a large resistor at the emitter electrode, providing smooth transition from voltage boundary conditions to current boundary conditions. It is not needed if the curve tracing algorithm is used (see the following example).

The numerical methods used in EB simulation can strongly affect convergence and CPU time. Here method block newton is used. This decouples the carrier temperature calculation from the potential and continuity equations at lower biases. This allows for larger bias steps at low bias.

The initial biasing is done by ramping the emitter contact towards 25V. A compliance limit is set on the emitter current as defined by: `cname=emitter compl=<value>`. Once this current is exceeded, the voltage ramp stops and ATLAS proceeds to the next simulation line. This is to specify *current forcing* on the emitter contact. The syntax `contact name=emitter current` does this.

After setting the Newton method, the biasing proceeds by specifying `istep=<value> imul`. The parameter `imult` indicates the `istep` is a *multiplier* to the current as opposed to an additive step. Therefore, at each bias step, the forced current is multiplied by `istep.ifinal` indicates the maximum current to be simulated.

Note that due to the use of current forcing, `emitter int. bias` should be used as the *x* axis on the IV data plots.

The second ATLAS run uses Nonisothermal Energy Balance Model: Poisson's equation, carrier continuity equations, energy balance equations for electrons and holes, and the lattice heat flow equations are solved self-consistently.

The same set of models is used, except that the solution of the lattice energy balance equation is activated using the `models lat.temp` statement.

In addition, the thermal boundary conditions should be defined in this case. Thermal boundary conditions are defined in the `thermcontact` statement. Values of the thermal conductances are specified at the thermal contact located along the emitter and base electrodes.

The results of the two simulation runs are then overlaid using TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

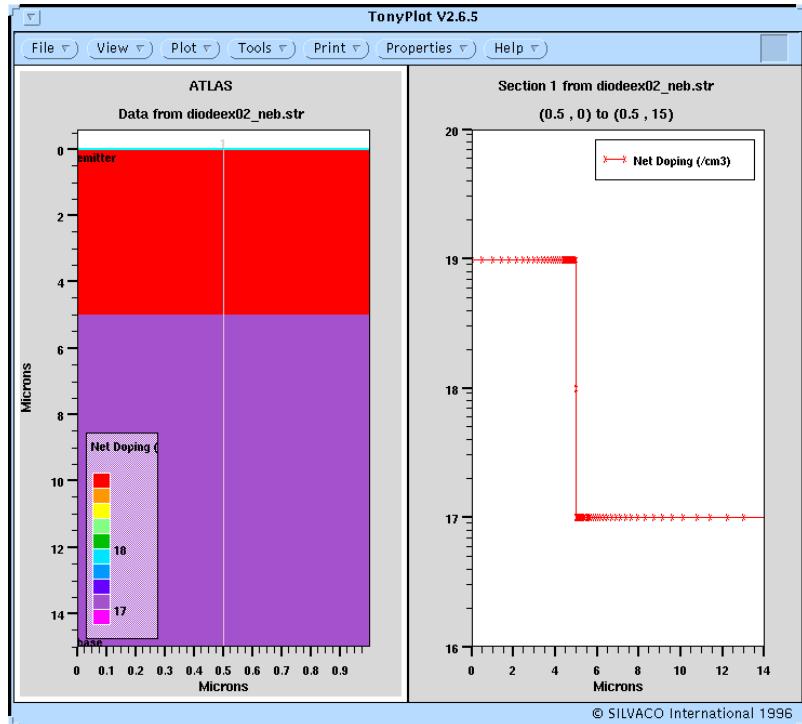


Figure 4.3: Structure and doping of an abrupt doping diode.

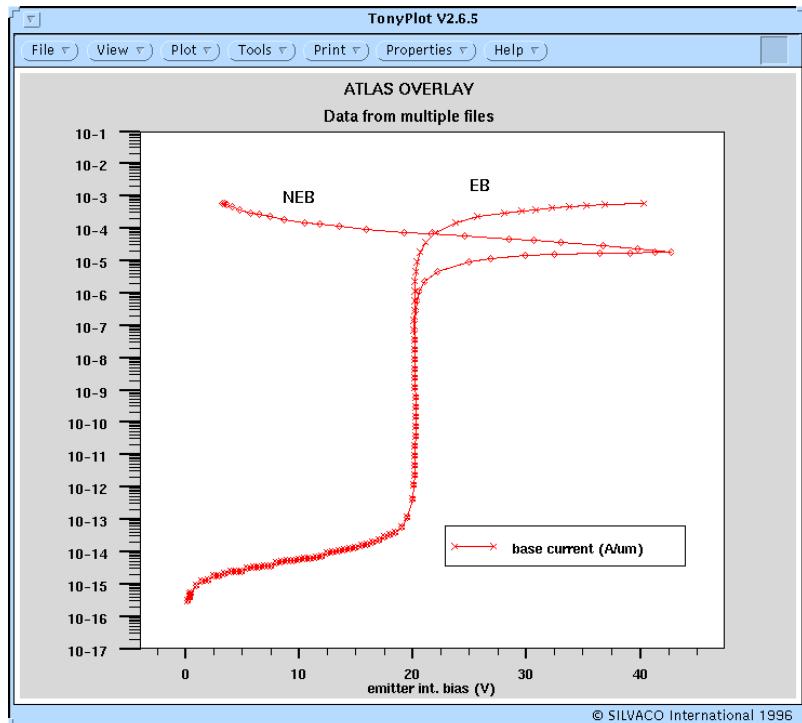


Figure 4.4: Breakdown and Second Breakdown of the diode. NEB Models allow s simulation of the second breakdown behavior through heating effects.

Input File diode/diodeex02.in:

```
1 go atlas
2 TITLE PN Diode Breakdown with Energy Balance and Nonisothermal Energy Bal-
   ance Models
3 # SILVACO International 1996
4
5 # EB simulation
6
7 mesh
8 x.m l=0.0 spac=1.0
9 x.m l=1.0 spac=1.0
10 y.m l=0    spac=1.0
11 y.m l=5.0  spac=0.005
12 y.m l=15   spac=2
13
14
15 region num=1 silicon
16
17 electrode top name=emitter
18 electrode bottom name=base
19
20 doping uniform conc=1e17 p.type
21 doping uniform n.type conc=1.e19  x.l=0. x.r=1 y.t=0.0 y.b=5.0
22
23 #contact name=emitter resis=1.e10
24
25 models srh conmob bgn auger fldmob hcte
26
27 impact selb length.rel lrel.ho=0.025  lrel.el=0.025
28
29 material taurel.el=0.25e-12 taumob.el=0.25e-12 taurel.ho=0.25e-12 tau-
   mob.ho=0.25e-12
30
31
32 method block newton climit=1.e-5
33
34 solve vmitter=0.0
35
36 log outf=diodeex02_eb.log
37
38 solve vmitter=0.5 vstep=0.5 vfinal=25 name=emitter cname=emitter com-
   pl=1e-12
39 save outf=diodeex02_eb.str
40
```

```
41 contact name=emitter current
42 method newton climit=1e-5
43 solve imult istep=2 ifinal=1e-3 name=emitter
44
45
46 go atlas
47
48 # NEB simulation
49
50 mesh
51 x.m l=0.0 spac=1.0
52 x.m l=1.0 spac=1.0
53 y.m l=0 spac=1.0
54 y.m l=5.0 spac=0.005
55 y.m l=15 spac=2
56
57
58 region num=1 silicon
59
60 electrode top name=emitter
61 electrode bottom name=base
62
63
64 doping uniform conc=1e17 p.type
65 doping uniform n.type conc=1.e19 x.l=0. x.r=1 y.t=0.0 y.b=5.0
66
67
68 thermcontact num=1 x.min=0 x.max=1 y.min=0 y.max=0 alpha=100
69 thermcontact num=2 x.min=0 x.max=1 y.min=15 y.max=15 alpha=100
70
71
72 models srh conmob bgn auger fldmob hcte lat.temp
73
74 impact selb length.rel lrel.ho=0.025 lrel.el=0.025
75
76 material taurel.el=0.25e-12 taumob.el=0.25e-12 taurel.ho=0.25e-12 tau-
    mob.ho=0.25e-12
77
78
79 method block newton climit=1.e-5
80
81 solve vmitter=0.0
82
```

```

83 log outf=diodeex02_neb.log
84
85 solve vemitter=0.5 vstep=0.5 vfinal=25 name=emitter cname=emitter com-
      pl=1e-12
86 save outf=diodeex02_neb.str
87
88 contact name=emitter current
89 method newton climit=1e-5
90 solve imult istep=2 ifinal=1e-3 name=emitter
91
92 tonyplot diodeex02_neb.str -set diodeex02_0.set
93 tonyplot diodeex02_eb.log -overlay diodeex02_neb.log -set diodeex02.set
94 quit

```

4.1.3. diodeex03.in: Breakdown Simulation with the Curve Tracer

Requires: S-PISCES

This example demonstrates breakdown simulation for a 1D diode using the automatic curve tracing algorithm. It shows:

- 1D diode structure formation using ATLAS syntax
- setting of models for breakdown simulation
- setting of curve tracing parameters
- automatic reverse bias curve trace simulation.

In the first part of the input file the device structure is specified, including mesh, electrodes locations, and doping distribution.

After the device description the MODELS statement is used to select a set of physical models for this simulation. In this case, these models are SRH and AUGER recombination, the concentration and field dependent mobility model, band gap narrowing and two carriers solution. The impact statement is used to activate the Crowell-Sze impact ionization model. The method statement is used to activate coupled Newton algorithm.

The curvetrace statement is used to initialize parameters for curve tracing algorithm. The contr.name parameter specifies the name of electrode for which the load line technique will be applied. In this example it is the emitter. The curr.cont parameter means that value of current will be monitored, and simulation will be stopped when the current exceeds the value specified by the end.val parameter (1.e-3 A/micron in this case). The mincur parameter defines the minimum current value after which the load line technique will actually be applied. Before that point, a standard voltage boundary conditions are used. The nextst.ratio parameter defines the maximum factor to use in increasing the voltage step on flat parts of the IV curve away from the turning points.

The statement solve curvetrace is used to activate curve tracing algorithm.

The results of simulation are then displayed using TONYPLOT. The drain voltage should be plotted as drain int.bias from the TONYPLOT menu, since the drain bias value includes the effect of the varying load used in the curve tracing algorithm.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

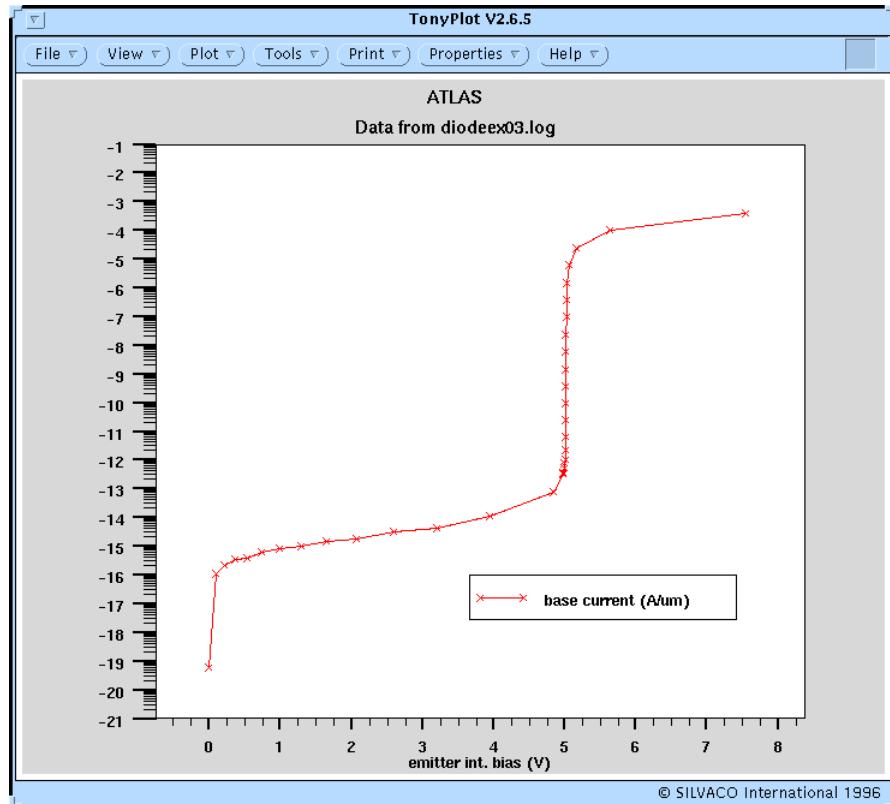


Figure 4.5: Diode breakdown curve traced out by the CURVETRACE feature. Note the non-uniform voltage steps.

Input File diode/diodeex03.in:

```

1 go atlas
2 TITLE PN Diode Breakdown Simulation with curve tracing algorithm
3 # SILVACO International 1996
4
5
6 mesh
7 x.m l=0.0 spac=1.0
8 x.m l=1.0 spac=1.0
9 y.m l=0 spac=1.0
10 y.m l=5.0 spac=0.005
11 y.m l=15 spac=2
12
13 region num=1 silicon
14
15 electrode top name=emitter
16 electrode bottom name=base
17
18 doping uniform conc=5e17 p.type
19 doping uniform n.type conc=1.e20 x.l=0. x.r=1 y.t=0.0 y.b=5.0

```

```

20
21 save outf=diodeex03_0.str
22 #tonyplot diodeex03_0.str -set diodeex03_0.set
23
24 models srh conmob bgn auger fldmob
25 impact crowell
26
27 solve init
28
29
30 method newton climit=1.e-4
31
32 curvetrace end.val=1e-4 contr.name=emitter curr.cont mincur=1e-13
      nextst.ratio=1.2
33
34
35 log outf=diodeex03.log
36 solve curvetrace
37 tonyplot diodeex03.log -set diodeex03.set
38
39
40 quit
41
42

```

4.1.4. diodeex04.in: Silicon Carbide Diode Characteristics

Requires: BLAZE

In this example a SiC diode is simulated to demonstrate the ATLAS capabilities to handle wide band gap semiconductor devices under room and elevated temperature conditions. The interest toward SiC technologies is growing due to the thermal and electronic properties of the material potentially leading to very high figures of merit for high-power, high-speed, high-temperature, and radiation hard applications.

The p+/n+ diode structure considered is a device based on one of the SiC polytypes called alpha-SiC (or 6H-SiC), and is constructed using ATLAS syntax. The input file consists of the following main parts:

- mesh, regions, electrodes and doping specification using ATLAS syntax
- material and models definition for SiC
- calculation of forward I-V characteristic under the room temperature conditions
- calculation of forward I-V characteristics under elevated temperature 623K
- calculation of reverse and breakdown characteristics at 623K

The simulations at elevated temperatures are done in a separate ATLAS run within the same input file with the respective resetting/changing of the material and models definition.

The input file starts by defining the mesh. The location and grid spacing along x and y directions are specified in the `x.m` and `y.m` statements. This simulation employs cylindrical symmetry and is therefore quasi-3-dimensional. To activate this feature the parameter, `cylindrical`, is included in the `mesh` statement.

The structure consists of 3 regions: p+ emitter, n base, and n+ emitter regions, each uniformly doped. The dimensions of the regions and their doping are defined in the `region` and `doping` statements respectively. The anode and cathode contacts are specified in the `electrode` statements.

Basic material parameters of alpha-SiC are defined in the `material` statements. These include dielectric permittivity, energy band gap, parameters related to the band gap narrowing, auger recombination coefficients, saturation velocity, and parameters describing mobility and lifetime temperature dependencies. The low field mobilities and lifetimes are specified on a region-by-region basis, taking into consideration the level of doping in the respective regions.

The set of physical models in the `model` statement includes electric field mobility dependence, Shockley-Read-Hall and Auger recombination, and band gap narrowing. The temperature is also specified in the `model` statement.

The first run is completed by the `solve` statement in which the anode bias is stepped from 0.1 up to 4 V to calculate the diode forward characteristic under room temperature conditions. The I-V data is saved in the log file.

The second ATLAS run simulates the forward, reverse, and breakdown characteristics under elevated temperature conditions. It starts by reading in the mesh and structure data from the file produced by the first run. In order to use the same cylindrical symmetry as the first run the `cylindrical` parameter must be specified whilst loading the mesh. The same material and model statements are used in this input file with the temperature of 623K set. Then the solving procedure is repeated to obtain the forward I-V characteristic which is saved in the log file.

The set of physical models needs to be extended for simulating reverse and breakdown characteristics to include the impact ionization-generation model. This is done in the following part of the input file, in the `impact` statement. The Selberherr impact ionization model is used with the parameters changed to reflect the properties of alpha-SiC. The other material and model statements are repeated here to ensure proper reinitialization of the material and models parameters. Since the breakdown in diode structures is typically very sharp, the `curvetrace` feature of ATLAS is used to bias the curve. Note that the parameter `step.init` is negative. This is sufficient to force a negative voltage sweep on the anode. The reverse/breakdown characteristic is saved in the log file. To plot the breakdown, the anode `int.bias` should be used as the x-axis.

The graphs with the forward I-V characteristics at the room and elevated temperatures, and the reverse and breakdown characteristic at 623K are displayed using TONYPLOT.

Since cylindrical coordinates were used, Note that in all I-V plots the units of current is Amps and not Amps/micron.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

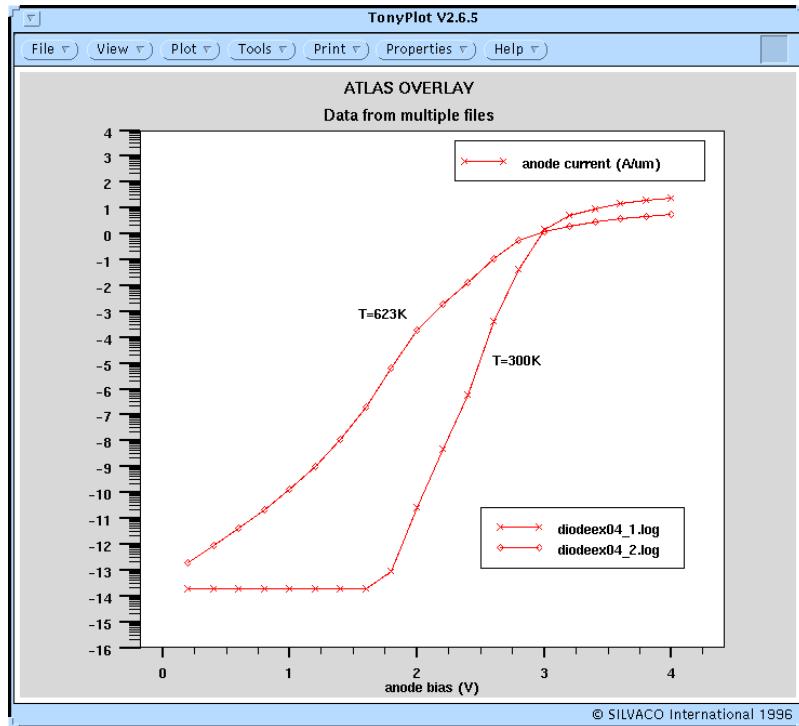


Figure 4.6: Forward characteristics of SiC diode at two temperatures

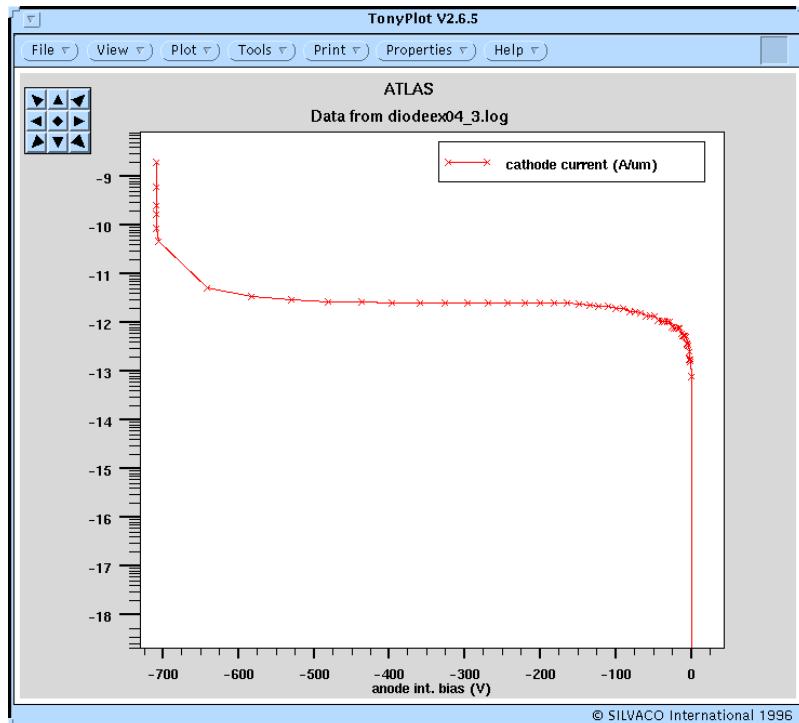


Figure 4.7: Reverse Breakdown of SiC diode

Input File diode/diodeex04.in:

```
1 go atlas
2 #
3 Title alpha-SiC Diode DC Forward, Reverse, and Breakdown Characteristics
4 #
5 # SECTION 1: Mesh Input
6 #
7 mesh      rect      smooth=1 diag.flip cylindrical
8 x.m       l=0.0     spac=20
9 x.m       l=80.0    spac=10
10 x.m      l=200.0   spac=50
11 #
12 y.m      l=0.0     spac=1.0
13 y.m      l=3.2     spac=0.1
14 y.m      l=5.0     spac=0.5
15 y.m      l=7.0     spac=0.1
16 y.m      l=15.0    spac=3.0
17 #
18 # SECTION 2: Regions & Electrodes
19 #
20 region    num=1    material=a-SiC           y.max=3.2
21 region    num=2    material=a-SiC y.min=3.2 y.max=7.0
22 region    num=3    material=a-SiC y.min=7.0
23 #
24 elec      name=anode  x.max=100.0
25 elec      name=cathode bottom
26 #
27 # SECTION 3: Doping Definition
28 #
29 # p+ emitter
30 doping    region=1 uniform conc=2.0e19 p.type
31 # n-base
32 doping    region=2 uniform conc=1.0e16 n.type
33 # n+ emitter
34 doping    region=3 uniform conc=5.0e18 n.type
35 #
36 save outf=diodeex04.str master
37 #
38 # SECTION 4: Material & Models Definitions
39 #
40 material  permittivity=9.66 eg300=3.00 egbeta=0. egalpha=3.3e-4 \
41          augn=2.8e-31 augp=9.9e-32 vsat=2.0e7 \
42          tmun=2.25 tmup=2.25 lt.taun=2.3 lt.taup=2.3
```

```
43 #
44 material num=1 mun0= 35.0 mup0= 25.0 taun0=1.e-9 taup0=1.e-9
45 material num=2 mun0=330.0 mup0= 60.0 taun0=1.e-7 taup0=1.e-7
46 material num=3 mun0=120.0 mup0= 35.0 taun0=5.e-9 taup0=5.e-9
47 #
48 model fldmob srh auger bgn print temperature=300
49 impact selb an1=1.66e6 an2=1.66e6 bn1=1.273e7 bn2=1.273e7 \
50 ap1=5.18e6 ap2=5.18e6 bpl=1.4e7 bp2=1.4e7
51 #
52 #
53 #
54 # SECTION 5: Forward I-V Characteristic Room Temperature
55 #
56 solve init
57 log outf=diodeex04_1.log
58 solve vanode=0.2 vstep=0.2 name=anode vfinal= 4.0
59 #
60 #
61
62 go atlas
63 #
64 # Simulation at Elevated Temperature
65 #
66 # SECTION 6: Read in Mesh and Structure Data
67 #
68 mesh inf=diodeex04.str cylindrical
69 #
70 # SECTION 7: Set Material, Models Definitions & Temperature
71 #
72 material permittivity=9.66 eg300=3.00 egbeta=0. egalpha=3.3e-4 \
73 augn=2.8e-31 augp=9.9e-32 vsat=2.0e7 \
74 tmun=2.25 tmup=2.25 lt.taun=2.3 lt.taup=2.3
75 #
76 material num=1 mun0= 35.0 mup0= 25.0 taun0=1.e-9 taup0=1.e-9
77 material num=2 mun0=330.0 mup0= 60.0 taun0=1.e-7 taup0=1.e-7
78 material num=3 mun0=120.0 mup0= 35.0 taun0=5.e-9 taup0=5.e-9
79 #
80 model fldmob srh auger bgn print temperature=623
81 impact selb an1=1.66e6 an2=1.66e6 bn1=1.273e7 bn2=1.273e7 \
82 ap1=5.18e6 ap2=5.18e6 bpl=1.4e7 bp2=1.4e7
83 #
84 #
85 # SECTION 8: Forward I-V Characteristic 623K
```

```
86 #
87
88 solve init
89 log outf=diodeex04_2.log
90 solve vanode=0.2 vstep=0.2 name=anode vfinal= 4.0
91
92 #
93 # SECTION 10: Calculate Reverse I-V Characteristic & Breakdown
94 #
95
96 method newton dvmax=1e8 climit=1.e-5
97 log off
98 solve init
99
100 log outf=diodeex04_3.log
101 curvetrace end.val=1e-9 contr.name=anode curr.cont \
102      mincur=1e-11 nextst.ratio=1.1 step.init=-0.5
103
104 solve curvetrace
105 save outf=diodeex04_1.str
106
107 # Forward Characteristics at 300K and 623K
108 tonyplot -overlay diodeex04_1.log diodeex04_2.log -set diodeex04_log1.set
109
110
111 # Reverse and Breakdown Characteristic at 623K
112 tonyplot diodeex04_3.log -set diodeex04_log2.set
113
114 quit
115
116
117
```

4.1.5. diodeex05.in: Zener Diode Breakdown

Requires: SSUPREM4/S-PISCES

This example demonstrates electrical simulation of a Zener diode breakdown. It shows:

- the formation of a 2D Zener diode structure in ATHENA
- the transfer of the structure to ATLAS
- specification of models for Zener breakdown simulation
- reverse bias simulation to the breakdown voltage

The structure formation is done by implanting a heavy boron dose into a heavily doped n-type substrate. The 2D extent of the p+ region is controlled by the etch coordinate of an oxide mask. A short diffusion is performed in ATHENA to drive in the p+ dopant.

After the diffusion, `extract` statements are used to measure the junction depth and sheet resistance of the p+ region. After this, metal is added and patterned. The electrode positions are then defined using the `electrode` statements in ATHENA.

The statement, `go atlas`, enables the automatic interface from ATHENA to ATLAS. DECKBUILD will switch simulators to ATLAS and load in the final ATHENA structure as the initial ATLAS mesh.

In ATLAS the first lines of syntax define the models to be used in the simulation. The statement, `models bip`, defines the standard bipolar model set that is also recommended for diode simulation. This consists of concentration, temperature and electric field dependent mobilities, concentration dependent SRH and Auger recombination and band gap narrowing. The parameter, `bbt.std`, enables the Lombardi band-to-band tunneling model. In heavily doped diodes this mechanism is the principal leakage current mechanism at voltages less than the avalanche breakdown. The `impact` statement enables the impact ionization model of Selberherr.

Newton's method is chosen on the `method` statement. The parameter, `climit=1e-4`, is highly recommended for all reverse bias simulations in ATLAS. It enables higher accuracy in the calculation of carrier concentration in the depletion regions.

The anode voltage is then ramped up to -10V in 0.25V steps. The breakdown voltage of this device is around -5.5V. ATLAS will converge up to this voltage and then stop as no solutions beyond this voltage are possible. By plotting the output log file in TONYPLOT, the breakdown can clearly be seen. The pre-breakdown current is dominated by band-to-band tunneling. An equivalent simulation excluding the '`bbt.std`' parameter might be run to demonstrate this.

The final statements use the `extract` feature of DECKBUILD to measure the maximum anode voltage at which convergence was obtained and the anode voltage for a particular value of anode current.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

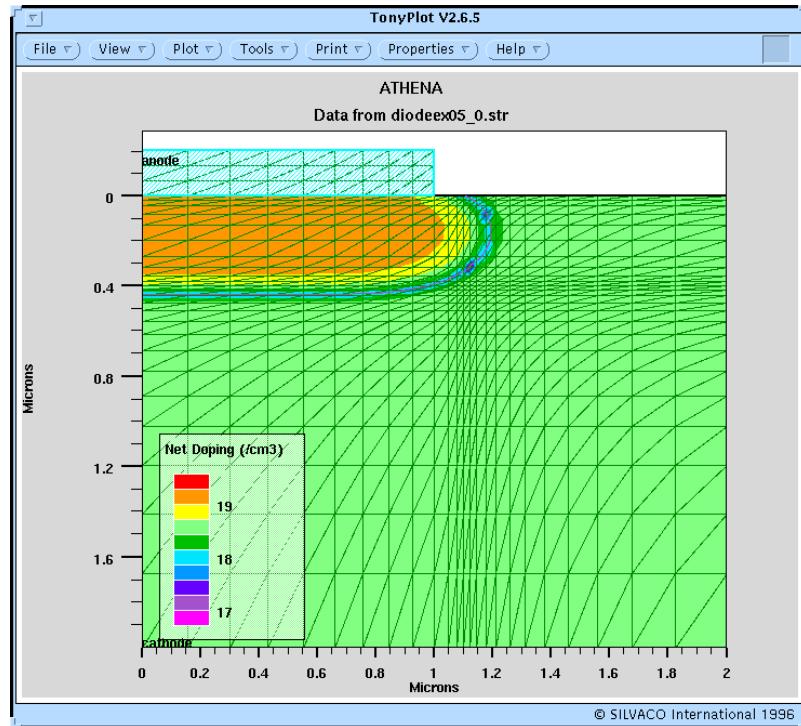


Figure 4.8: Zener diode structure, mesh and doping defined in ATHENA

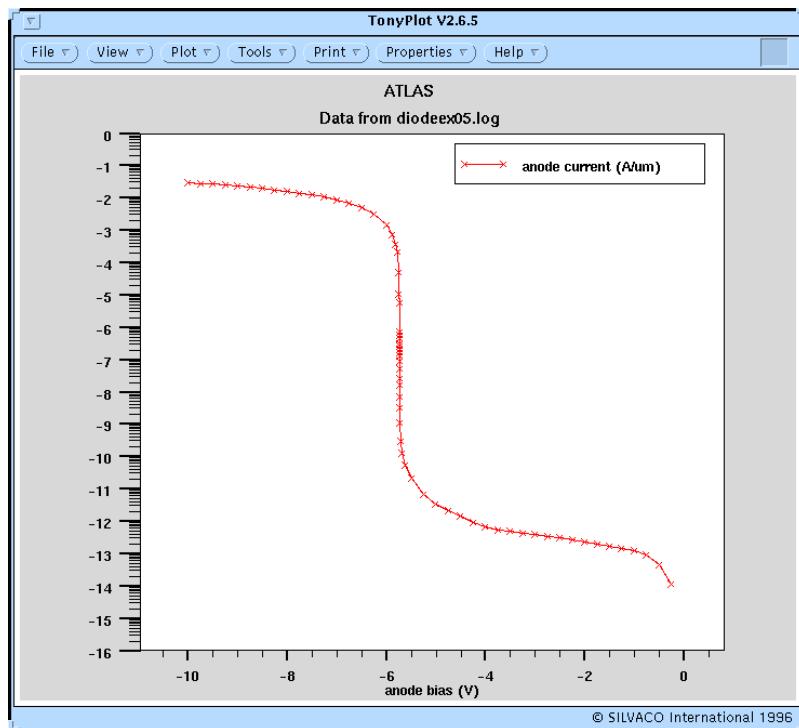


Figure 4.9: Reverse breakdown of Zener diode. Note the 'soft' breakdown starting at -4V

Input File diode/diodeex05.in:

```
1 go athena
2 #
3 line x loc=0.00 spac=0.2
4 line x loc=1 spac=0.1
5 line x loc=1.1 spac=0.02
6 line x loc=2 spac=0.25
7 #
8 line y loc=0.00 spac=0.02
9 line y loc=0.2 spac=0.1
10 line y loc=0.4 spac=0.02
11 line y loc=2 spac=0.5
12 #
13 init silicon c.phos=5.0e18 orientation=100
14 #
15 deposit oxide thick=0.50 divisions=5
16 #
17 etch oxide left p1.x=1
18 #
19 implant boron dose=1.0e15 energy=50 pearson tilt=7 rotation=0 amorph
20 #
21 method fermi compress
22 diffus time=30 temp=1000 nitro press=1.00
23 #
24 extract name="xj" xj material="Silicon" mat.occno=1 x.val=0 junc.occno=1
25 #
26 extract name="rho" sheet.res material="Silicon" mat.occno=1 x.val=0 re-
    gion.occno=1
27
28 etch oxide all
29 deposit alum thickness=0.2 div=3
30 etch alum right p1.x=1.0
31
32 electrode name=anode x=0.0
33 electrode name=cathode backside
34
35 structure outf=diodeex05_0.str
36 tonyplot diodeex05_0.str -set diodeex05_0.set
37
38 go atlas
39
40 models bip bbt.std print
41 impact selb
```

```
42
43 method newton trap maxtrap=10 climit=1e-4
44 solve init
45
46 log outf=diodeex05.log
47 solve vanode=-0.25 vstep=-0.25 vfinal=-10 name=anode
48
49 tonyplot diodeex05.log -set diodeex05_log.set
50
51 extract init infile="diodeex05.log"
52 extract name="bv" min(v."anode")
53 extract name="leakage" x.val from curve(v."anode",abs(i."anode")) where
      y.val=1e-10
54
55
56 quit
```

4.1.6. diodeex06.in: 3D Diode Characteristic

Requires: DEVICE3D

This example demonstrates electrical simulation of a diode. It shows:

- the formation of a 3D diode structure in ATLAS
- forward bias simulation

The z.mesh statement is used in a similar manner to x.mesh and y.mesh to create a 3D structure using the ATLAS syntax. Following this the region, electrode and doping statements each have Z related parameters that correspond with the X and Y parameters familiar from 2D simulation.

The syntax for setting material and model parameters and for biasing the device and saving results is identical to the previous 2D examples. Note that TONYPLOT3D is required to plot the 3D mesh and solution files. TONYPLOT is used for plotting the log files.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

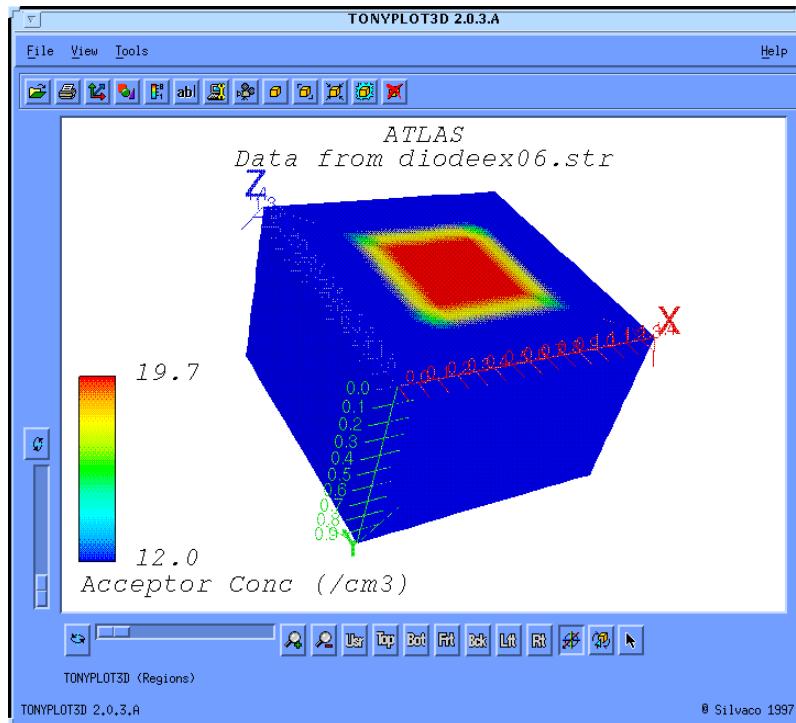


Figure 4.10: Doping in a 3D Diode defined in DEVICE3D syntax

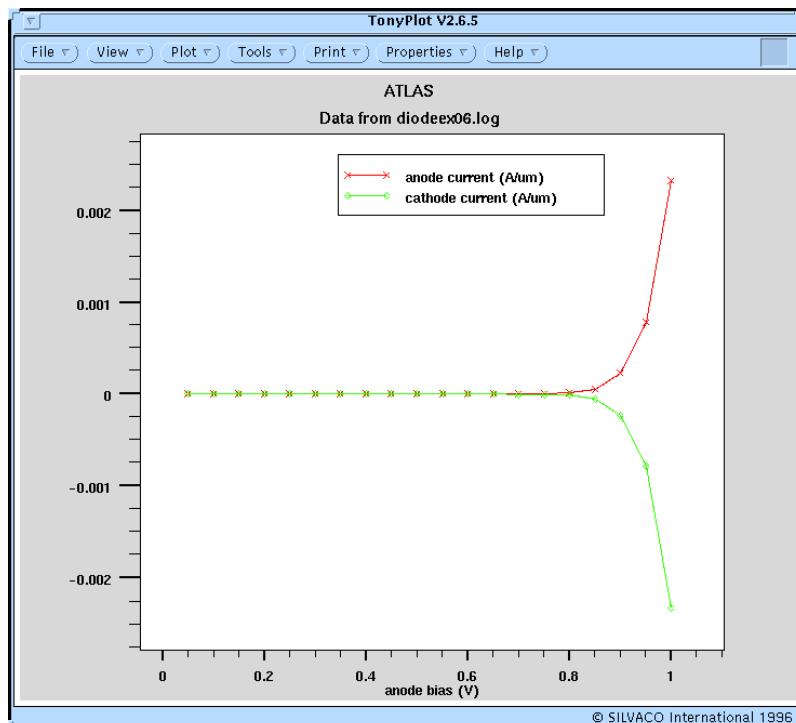


Figure 4.11: Forward simulation of diode in 3D

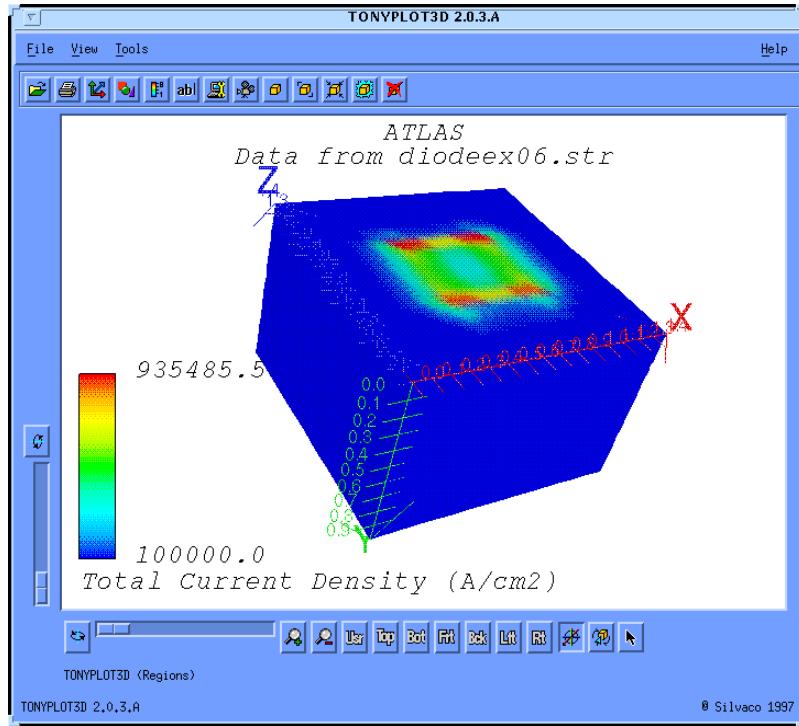


Figure 4.12: 3D current density plot shows current crowding at the corners of the high doped region

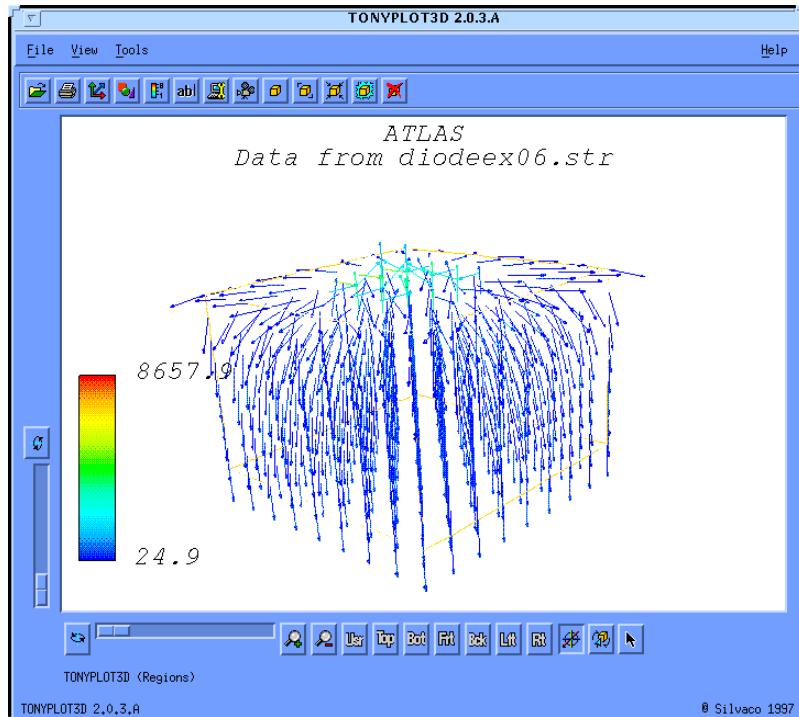


Figure 4.13: Vectors show the 3D distribution of Electric Field in the Diode

Input File diode/diodeex06.in:

```
1 go atlas
2 mesh three.d
3
4 x.mesh l=0 spacing=0.1
5 x.mesh l=1.5 spacing=0.1
6
7 y.mesh l=0.0 spacing=0.02
8 y.mesh l=1.0 spacing=0.1
9
10 z.mesh l=0.0 spacing=0.1
11 z.mesh l=1.5 spacing=0.1
12
13 region num=1 silicon
14
15 electrode num=1 name=anode x.min=0.5 x.max=1.0 z.min=0.5 z.max=1.0
16 electrode num=2 name=cathode bottom
17
18 doping reg=1 uniform n.type conc=5e15
19 doping reg=1 gauss n.type conc=1e18 peak=1.0 char=0.2
20 doping reg=1 gauss p.type conc=5e19 peak=0.0 junct=0.2 \
21     x.left=0.5 x.right=1.0 z.left=0.5 z.right=1.0
22
23
24 log outfile=diodeex06.log
25 solve init
26
27 method carrier=2
28 solve vanode=0.05 vstep=0.05 vfinal=1 name=anode
29
30 tonyplot diodeex06.log
31
32 save outfile=diodeex06.str
33 tonyplot diodeex06.str -set diodeex06.set
34
35
36
37 quit
38
39
40
41
```

4.1.7. diodeex07.in: Gunn Diode

Requires: DEVEDIT/BLAZE

This example shows the transient oscillatory behavior of a Gunn device due to the negative differential resistance of behavior exhibited by GaAs (as a result of electron intervalley transfer).

In the first part of the input file, the structure is defined within DEVEDIT. The device is a sandwich structure made up of two gold electrode layers on the top and bottom, one low doped transit layer in the middle and two high doped layers acting as low resistivity contact regions and carrier injectors.

The thickness of the transit layer together with the applied electric field is one of the key design features determining the frequency of the oscillations.

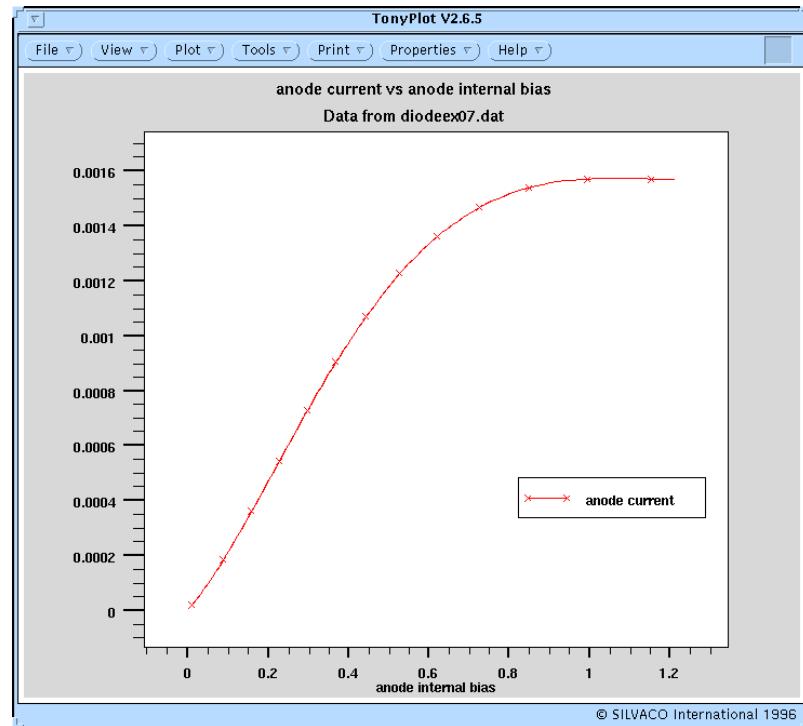
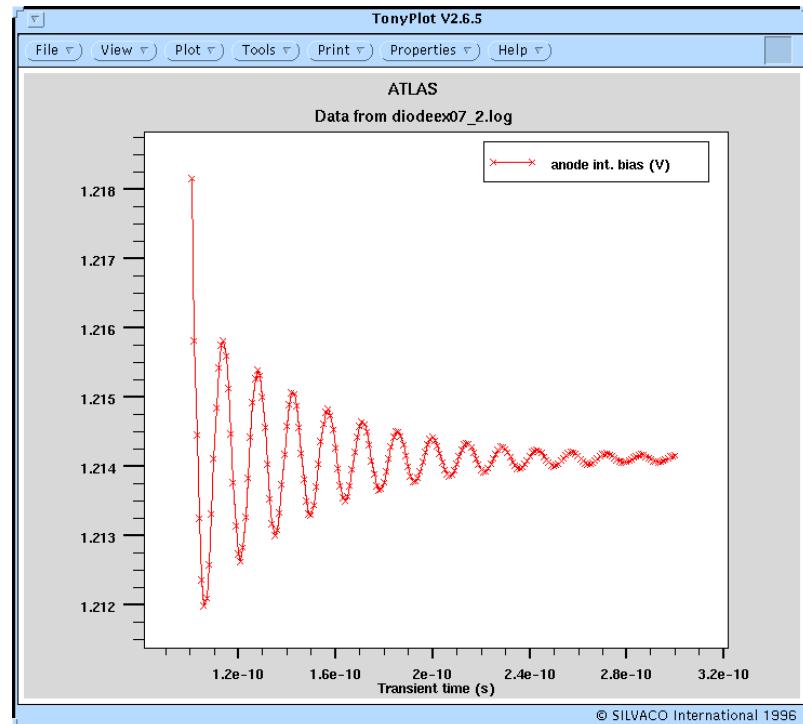
In the second part of the file after the 'go atlas' statement transient device simulations are performed for different biases.

After loading the structure from DEVEDIT a load resistor is attached at the anode side with the contact statement. In order to model the negative differential velocity saturation behavior for electrons, fldmob in the model statement is specified together with the evsatmod=1 parameter. This switches on the negative differential mobility model for GaAs like materials. As the function of holes is negligible, the solution of the hole continuity equation can be disabled by specifying carriers=1.

By ramping up the bias of the anode to 2 V, one can clearly see the effect of the negative resistance when extract is used to calculate the critical electric field from the log-file. With the following stationary simulation, it can be shown that the bias is not sufficient to feed an oscillation with the given load, the oscillation is damped. The frequency is calculated by extracting the time required for four full periods.

In contrast, the device is able to operate at 4V bias. To monitor the movement of the domains, select several of the different electron distributions from different points in time (as 2d contours or the corresponding cutlines) displayed with TONYPLOT at the end of the simulation, and make a movie using the Tools: Movie menu.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DeckBuild, select the run button to execute the example.

**Figure 4.14:** DC IV Curve for Gunn Diode**Figure 4.15:** Transient Oscillation Behavior of the Gunn Diode at 2V

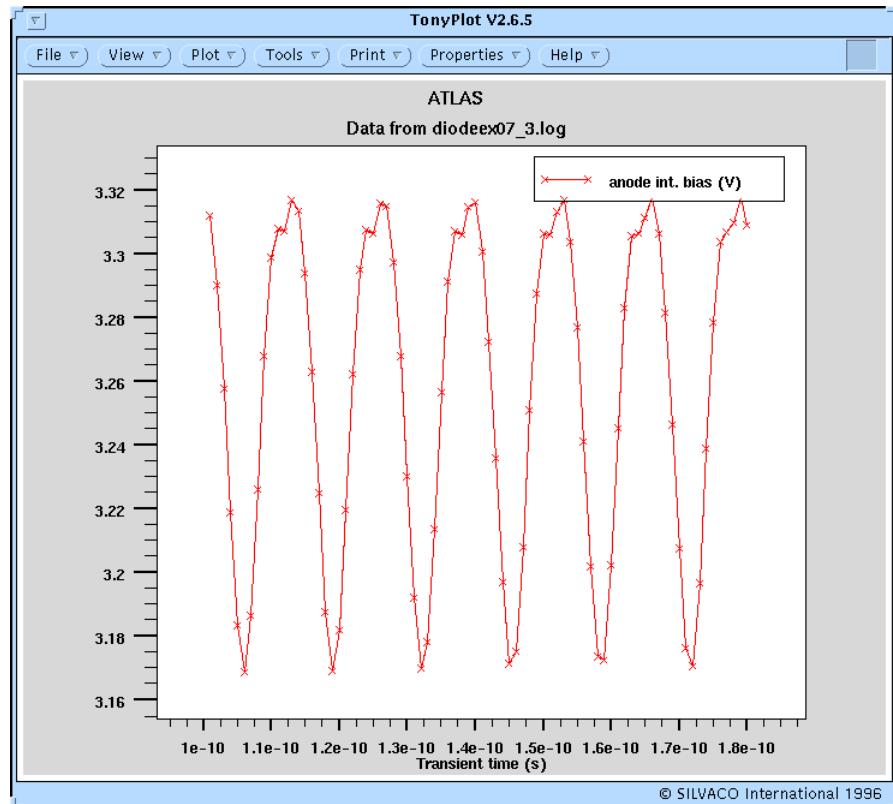


Figure 4.16: Transient Oscillation Behavior of the Gunn Diode at 4V

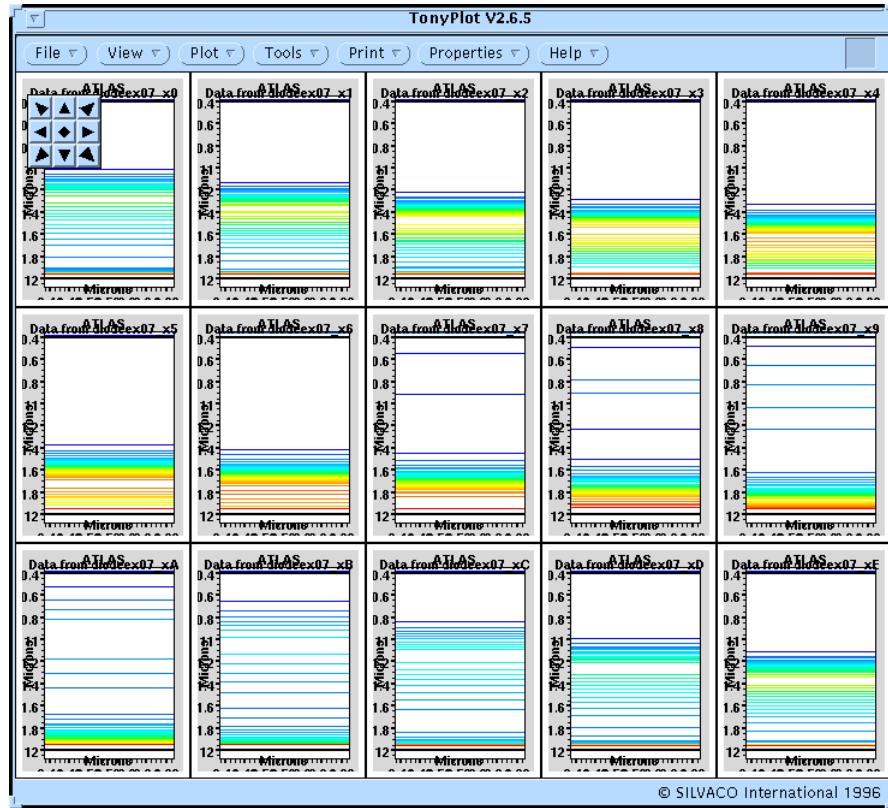


Figure 4.17: Sequence showing the ‘waves’ of carriers moving though the Gunn Diode. The Movie feature in Tony-Plot can be used to animate the carrier flow.

Input File diode/diodeex07.in:

```

1 go DevEdit
2 DevEdit version="2.2.1" library="1.17"
3
4 work.area left=0 top=-34.6 right=5 bottom=38
5
6 # SILVACO Library V1.17
7
8 region reg=1 name=anode mat=Gold elec.id=1 work.func=0 color=0x595959
   pattern=0xb \
9 points="5,38 0,38 0,13 5,13 5,38"
10 #
11 constr.mesh region=1 default
12
13 region reg=2 name=contact mat=GaAs color=0x7f00 pattern=0x9 \
14 points="5,13 0,13 0,12 5,12 5,13"
15 #
16 impurity id=1 region.id=2 imp=Donors \
17 x1=0 x2=0 y1=0 y2=0 \
18 peak.value=2.5e+18 ref.value=1000000000000 comb.func=Multiply \

```

```
19 rolloff.y=both conc.func.y=Constant \
20 rolloff.x=both conc.func.x=Constant
21 #
22 constr.mesh region=2 default max.height=0.5
23
24 region reg=3 name=transit mat=GaAs color=0x7f00 pattern=0x9 \
25 points="5,12 0,12 0,10.4 5,10.4 5,12"
26 #
27 impurity id=1 region.id=3 imp=Donors \
28 x1=0 x2=0 y1=0 y2=0 \
29 peak.value=1.2e+16 ref.value=1000000000000 comb.func=Multiply \
30 rolloff.y=both conc.func.y=Constant \
31 rolloff.x=both conc.func.x=Constant
32 #
33 constr.mesh region=3 default max.height=0.08
34
35 region reg=4 name=substrate mat=GaAs color=0x7f00 pattern=0x9 \
36 points="5,10.4 0,10.4 0,0.4 5,0.4 5,10.4"
37 #
38 impurity id=1 region.id=4 imp=Donors \
39 x1=0 x2=0 y1=0 y2=0 \
40 peak.value=2.5e+18 ref.value=1000000000000 comb.func=Multiply \
41 rolloff.y=both conc.func.y=Constant \
42 rolloff.x=both conc.func.x=Constant
43 #
44 constr.mesh region=4 default max.height=5
45
46 region reg=5 name=cathode mat=Gold elec.id=2 work.func=0 color=0x595959
    pattern=0xb \
47 points="5,0.4 0,0.4 0,-9.6 5,-9.6 5,0.4"
48 #
49 constr.mesh region=5 default
50
51
52
53 # Set Meshing Parameters
54 #
55 base.mesh height=50 width=100
56 #
57 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.01 line.straight-
    ening=1 align.points when=automatic
58 #
59 imp.refine imp="Donors" sensitivity=1
60 imp.refine min.spacing=0.02
```

```
61 #
62 constr.mesh max.angle=90 max.ratio=300 max.height=1000 \
63 max.width=1000 min.height=0.0001 min.width=0.0001
64 #
65 constr.mesh type=Semiconductor default
66 #
67 constr.mesh type=Insulator default
68 #
69 constr.mesh type=Metal default max.angle=127.2
70 #
71 constr.mesh type=Other default
72 #
73 constr.mesh region=1 default
74 #
75 constr.mesh region=2 default max.height=0.5
76 #
77 constr.mesh region=3 default max.height=0.08
78 #
79 constr.mesh region=4 default max.height=5
80 #
81 constr.mesh region=5 default
82 #
83 # Perform mesh operations
84 #
85 Mesh Mode=MeshBuild
86 struct outf=diodeex07.str
87
88 go atlas
89 #
90 #mesh infile=diodeex07.str
91 #
92 #
93 # #1=anode #2=cathode
94 contact name=anode neutral resist=5e2
95
96 # set GaAs-saturation velocity model with negative slope (evsatmod=1)
97 # carriers=1 solves the electron continuity equation only, since holes
98 # play no role here
99 models consrh analytic fldmob evsatmod=1 b.elec=2 \
100 boltzman print temperature=300
101
102 method carriers=1
103 #
```

```
104
105 output      e.field
106
107 solve init
108 solve
109
110 # ramp up the bias
111 log outf=diodeex07_1.log
112 solve vanode=2 ramptime=1e-10 tstop=1e-10 dt=1e-12
113 save outf=diodeex07_1.str
114
115 # extract the i-v characteristic and the crittical field, above which
116 # the negative resistance begins
117 extract name="diodeex07.dat" curve (vint."anode",i."anode")
     outf="diodeex07.dat"
118 extract name="Icrit" max(i."anode")
119 extract name="Ucrit" x.val from curve(vint."anode",i."anode") where
     y.val=$Icrit
120 extract name="Ecrit" $Ucrit/1.6e-4
121 tonyplot diodeex07.dat
122
123 # do transient simulation at 2V constant external bias
124 log outf=diodeex07_2.log
125 solve tstop=3e-10 dt=1e-12
126 log off
127
128 # extract the oscillation frequency by measuring the time for 4 periods
129 extract init inf="diodeex07_2.log"
130 extract name="v_ave" ave(vint."anode")
131 extract name="t1" x.val from curve(time,vint."anode") where
     y.val=$"v_ave"
132 extract name="t2" x.val from curve(time,vint."anode") where
     y.val=$"v_ave" and val.occno=9
133 extract name="delta" ("$t2" - "$t1") / 4
134 extract name="f@2V" 1 / $"delta"
135 tonyplot diodeex07_2.log -set diodeex07_2.set
136
137 # ramp up to 4V external bias
138 load inf=diodeex07_1.str master
139 solve prev
140 solve vanode=4 ramptime=1e-10 tstop=1e-10 dt=1e-12
141 save outf=diodeex07_3.str
142
143 # do transient simulation at 4V constant external bias
```

```

144 log outf=diodeex07_3.log
145 solve tstop=1.8e-10 dt=1e-12 outfile=diodeex07_x0 master
146 log off
147 tonyplot diodeex07_3.log -set diodeex07_3.set
148
149 extract init inf="diodeex07_3.log"
150 extract name="v_ave" ave(vint."anode")
151 extract name="t1" x.val from curve(time,vint."anode") where
      y.val=$"v_ave"
152 extract name="t2" x.val from curve(time,vint."anode") where
      y.val=$"v_ave" and val.occno=9
153 extract name="delta" ($"t2" - $"t1") / 4
154 extract name="f@4V" 1 / $"delta"
155
156 tonyplot -st diodeex07_x0 diodeex07_x1 diodeex07_x2 diodeex07_x3
      diodeex07_x4 diodeex07_x5 diodeex07_x6 diodeex07_x7 diodeex07_x8
      diodeex07_x9 diodeex07_xA diodeex07_xB diodeex07_xC diodeex07_xD
      diodeex07_xE -set diodeex07_4.set
157
158 quit

```

4.1.8. diodeex08.in : 3D Diode Using Lifetime Killing

Requires: DEVEDIT3D/DEVICE3D/GIGA3D

A common practice in high power electronics is to vary carrier lifetime across a device by bombarding the region of silicon with particles or introducing gold impurities. This example demonstrates how such an analysis may be performed using device simulation. This example shows:

- the formation of a 3D diode structure in DEVEDIT3D
- device simulation driving the diode into forward bias
- how to create a 3D plot showing the current crowding effect

The structure is first created by running DEVEDIT3D in batch mode using the command `go devedit`. DEVEDIT3D performs three functions: creation of the diode topology with the `region` statement, addition of impurities with the `impurity` statement and finally creates the mesh for the device simulation by setting various `Meshing Parameters` options. Further information on these statements may be found in the `VWF INTERACTIVE TOOLS USER'S MANUAL: VOLUME 1`.

Only the top left quarter of the complete cell will be simulated as the three quarters are identical. The structure created by DEVEDIT3D contains two different silicon regions which will exhibit different carrier lifetimes during the device simulation.

The completed structure is then piped into the device simulator which is started with the `go atlas` command. The `Atlas` syntax is then used to modify the material parameters in the different regions. The `material` statement is used to specify the electron and hole lifetime in each silicon region. In this example we have made the carrier lifetime 20 times smaller in the region which has undergone a lifetime killing process- region number 1. It is also highly important that the necessary physical models are switched on if the simulation is to be accurate. The `model` statement is used to switch on the appropriate models for the simulation. In this case the example uses `analytic` and `connmob`: the doping and temperature dependent low field mobility model, `fldmob`: the lateral electric field-dependent mobility model, `srh`: Shockley-Read-Hall recombination, `auger`: recombination accounting for high level injection effects, and `bgn`: band gap narrowing.

In addition if thermal self heating effects are required in the simulation an additional parameter lat.temp will be required to cause the simulator to solve the lattice heat flow equation. If this is the case a thermal boundary condition must also be specified using the thermcontact statement. This example uses the cathode electrode, number 2, as the thermal boundary condition and specifies a fixed temperature there of 300 K.

As the solution procedes all terminal characteristics are saved into a file, with the command log outf=<filename>, which can then be plotted at the end of the simulation. Two simulations are performed in this example, with and without the lattice heating model switched on, both driving the diode into forward bias. TONYPLOT is then used to display both of the I-V results on the same plot as well as the change in lattice temperature. When the lattice heating model is turned on the increase in lattice temperature causes a decrease in carrier mobility and thereby a roll-off in current under forward bias.

Note that the user can use TONYPLOT3D to plot the 3D mesh and solution files. By displaying the total current density in an isosurface contour plot, the current crowding effect can be seen.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

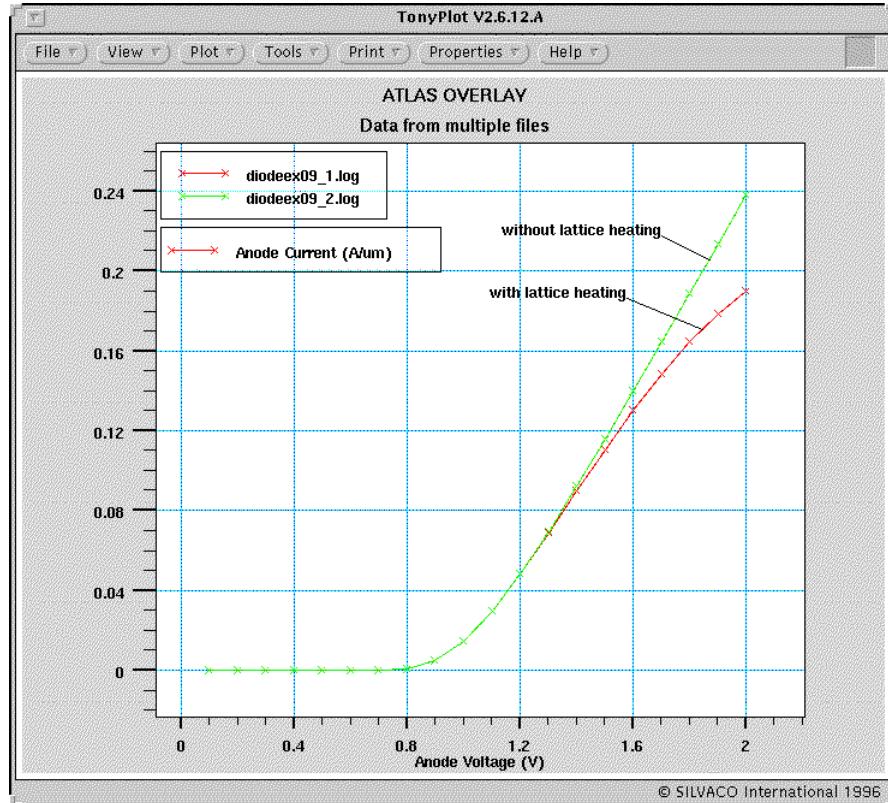


Figure 4.18: Anode current versus anode voltage of a 3D Diode both with and without lattice heating

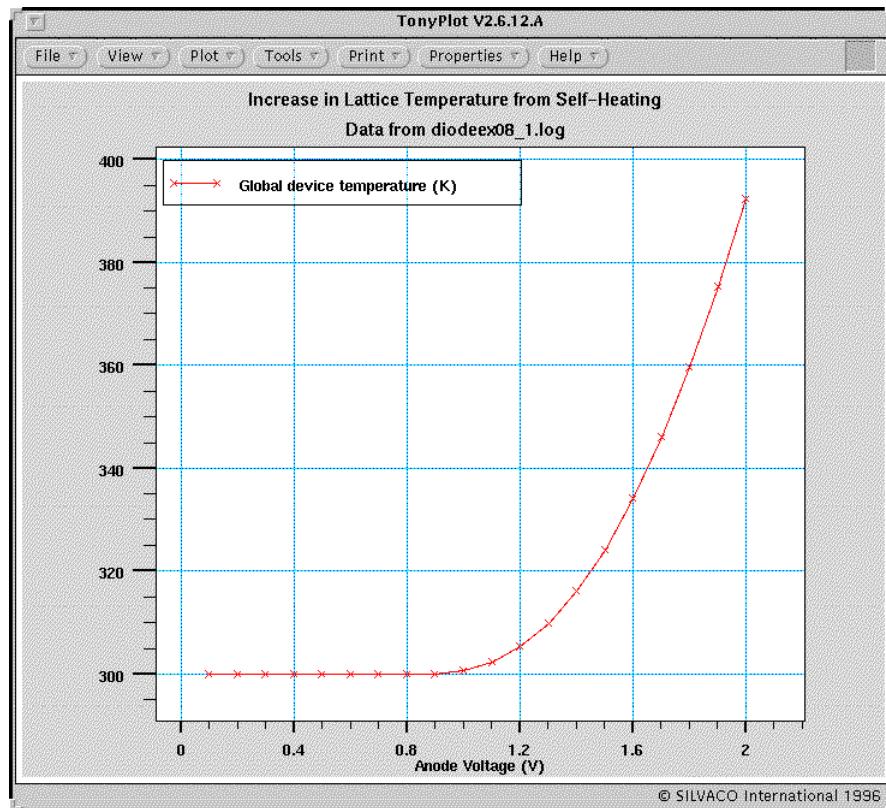


Figure 4.19: Maximum semiconductor temperature versus anode voltage for the 3D diode

Input Deck diode/diodeex08.in :

```

1  #
2
3  # first generate the structure using devedit
4  go devedit
5
6  region reg=1 name=low1 mat=Silicon color=0xffffcc00 pattern=0x4 z1=0 z2=50 \
7  polygon="5,0 5,5 0,5 0,0"
8  #
9  impurity id=1 region.id=1 imp=Phosphorus \
10 peak.value=1e14 ref.value=1e12 comb.func=Multiply
11 #
12 constr.mesh region=1 default
13
14 region reg=2 mat=Silicon color=0xffffcc00 pattern=0x4 z1=0 z2=50 \
15 polygon="25,0 25,25 0,25 0,5 5,5 5,0"
16 #
17 impurity id=1 region.id=2 imp=Phosphorus \
18 peak.value=1e14 ref.value=1e12 comb.func=Multiply
19 #

```

```
20 constr.mesh region=2 default
21
22 region reg=3 name=anode mat=Aluminum elec.id=1 work.func=0 color=0xffc8c8
   pattern=0x7 z1=-1 z2=0 \
23 polygon="0,0 5,0 25,0 25,25 0,25 0,5"
24 #
25 constr.mesh region=3 default
26
27 region reg=4 name=cathode mat=Aluminum elec.id=2 work.func=0 col-
   or=0xffc8c8 pattern=0x7 z1=50 z2=51 \
28 polygon="0,0 5,0 25,0 25,25 0,25 0,5"
29 #
30 constr.mesh region=4 default
31
32
33 impurity id=1 imp=Boron color=0x8c5d00 \
34 peak.value=1e+17 ref.value=1e14 comb.func=Multiply \
35 y1=0 y2=25 rolloff.y=step \
36 x1=0 x2=25 rolloff.x=step \
37 z1=0 z2=0 rolloff.z=both conc.func.z="Gaussian (Dist)" conc.param.z=15
38 impurity id=2 imp=Phosphorus color=0x8c5d00 \
39 peak.value=5e+18 ref.value=1e14 comb.func=Multiply \
40 y1=0 y2=25 rolloff.y=step \
41 x1=0 x2=25 rolloff.x=step \
42 z1=40 z2=50 rolloff.z=both conc.func.z="Step Function" conc.param.z=15
43
44 # Set Meshing Parameters
45 #
46 base.mesh height=5 width=5
47 #
48 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001 \
49 line.straightening=1 align.points when=automatic
50 #
51 imp.refine min.spacing=0.02 z=0
52 #
53 constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
54 max.width=10000 min.height=0.0001 min.width=0.0001
55 #
56 constr.mesh type=Semiconductor default
57 #
58 constr.mesh type=Insulator default
59 #
60 constr.mesh type=Metal default
61 #
```

```
62 constr.mesh type=Other default
63 #
64 constr.mesh region=1 default
65 #
66 constr.mesh region=2 default
67 #
68 constr.mesh region=3 default
69 #
70 constr.mesh region=4 default
71 constr.mesh id=1 x1=0 y1=0 x2=10 y2=10 max.height=1.5 max.width=1.5
72 Mesh Mode=MeshBuild
73
74 z.plane z=0 spacing=1
75 #
76 z.plane z=14 spacing=1
77 #
78 z.plane z=15 spacing=0.1
79 #
80 z.plane z=16 spacing=1
81 #
82 z.plane z=40 spacing=5
83 #
84 z.plane z=50 spacing=5
85 #
86 z.plane max.spacing=1000000 max.ratio=1.5
87
88 struct outf=diodeex08_0.str
89
90 go atlas
91
92 material region=1 taup0=0.05e-6 taun0=0.15e-6
93 material region=2 taup0=1e-6 taun0=3e-6
94
95 model analytic conmob fldmob srh auger bgn lat.temp
96 thermcont numb=1 elec.num=2 ext.temp=300
97
98 solve init
99 solve prev
100
101 log outf=diodeex08_1.log
102 solve vanode=0.1 vfinal=2 vstep=0.1 name=anode
103 save outf=diodeex08_1.str
104
```

```
105
106
107 go atlas
108
109 material region=1 taup0=0.05e-6 taun0=0.15e-6
110 material region=2 taup0=1e-6 taun0=3e-6
111
112 model analytic commob fldmob srh auger bgn
113
114 solve init
115 solve prev
116
117 log outf=diodeex08_2.log
118 solve vanode=0.1 vfinal=2 vstep=0.1 name=anode
119 save outf=diodeex08_2.str
120
121 tonyplot -overlay diodeex08_1.log diodeex08_2.log -set diodeex08_1.set
122 tonyplot diodeex08_1.log -set diodeex08_2.set
123
124 quit
```

4.1.9. diodeex09.in : Temperature Ramping – Effect on Leakage

Requires: ATLAS

This example demonstrates the correct method for global temperature ramping in Atlas for any device. A diode structure was chosen here for simplicity. In ATLAS the global temperature of the device is set using the models statement. However, the global temperature can only be set ONCE in the input deck if ALL the temperature dependent parameters are to be set. If the temperature is re-set during a single input deck with a second “models statement” an incorrect result is obtained, since not all the temperature dependent parameters are set in subsequent models statements.

The solution is to use the combination of a go atlas statement, together with a mesh infile= statement. After the mesh statement, re-set the global temperature with a new “models” statement.

The device bias conditions can then either be ramped up from zero, as in this example or can be loaded in from the previous solution with a load infile= statement. In order to end up with one continuous log outfile the keyword append must be added to the log outfile name after the second and subsequent "log outfile=" statements in order to prevent the original log file being over written.

This example also plots the electron and hole mobility versus temperature. Substituting different mobility models allows the temperature effects of each to be compared.

To load and run this example, select the **Load Example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

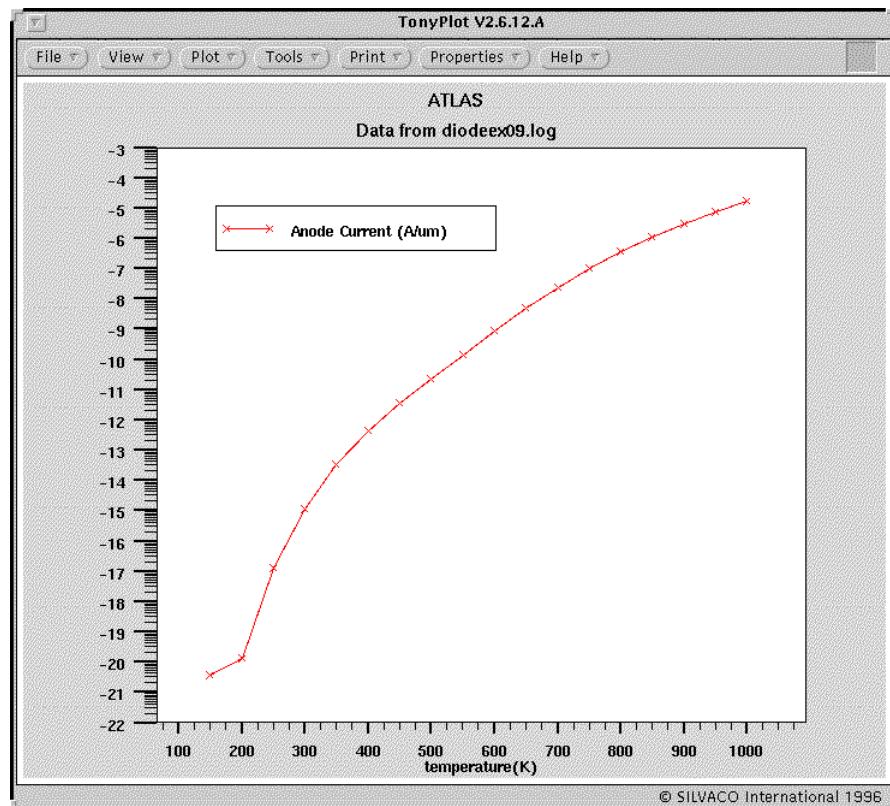


Figure 4.20: Increase in anode leakage current as the ambient lattice temperature is increased

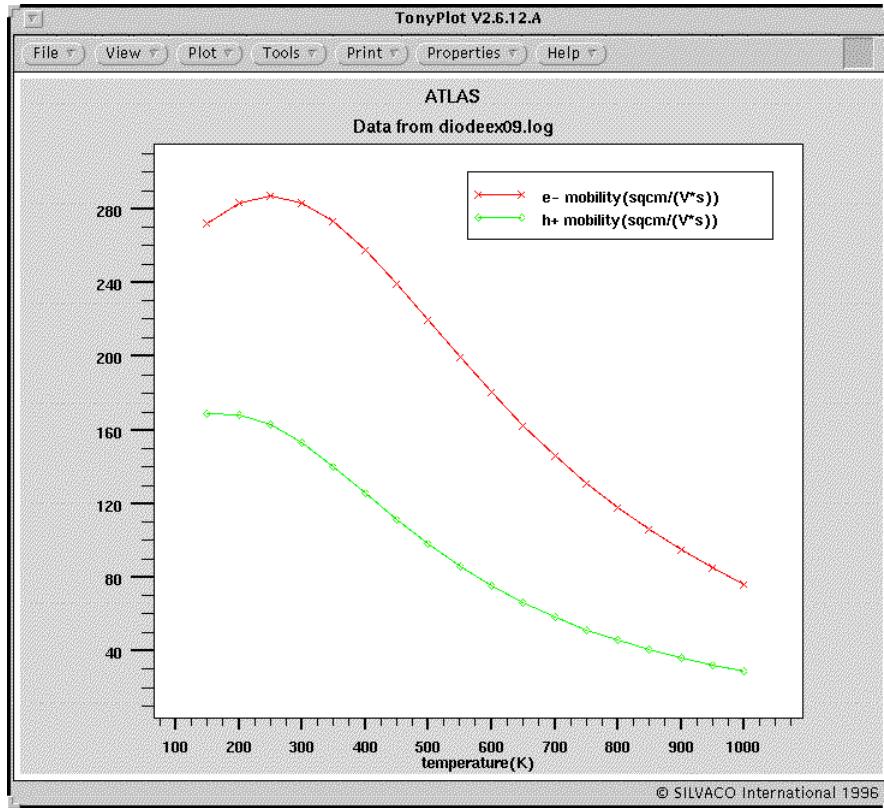


Figure 4.21: Plot of electron and hole mobility as a function of ambient lattice temperature

Input Deck diode/diodeex09.in :

```

1
2 go atlas
3
4 mesh
5
6 x.mesh loc=0.00 spac=0.05
7 x.mesh loc=0.10 spac=0.05
8
9 y.mesh loc=0.00 spac=0.20
10 y.mesh loc=1.00 spac=0.01
11 y.mesh loc=2.00 spac=0.20
12
13 region number=1 x.min=0.0 x.max=0.1 y.min=0.0 y.max=1.0 material=silicon
14 region number=2 x.min=0.0 x.max=0.1 y.min=1.0 y.max=2.0 material=silicon
15
16 electrode name=anode top
17 electrode name=cathode bottom
18
19 doping uniform conc=1e18 n.type region=1

```

```
20 doping uniform conc=1e18 p.type region=2
21
22 models bipolar temperature=150 kla analytic
23
24 probe lat.temp x=0.05 y=1.0
25 probe n.mob     x=0.05 y=0.2
26 probe p.mob     x=0.05 y=1.8
27 solve
28 save outfile=diodeex09.str
29 solve vanode=0.01
30 log outfile=diodeex09.log
31 solve vanode=1
32
33 go atlas
34 mesh infile=diodeex09.str
35 models bipolar temperature=200 kla analytic
36 probe lat.temp x=0.05 y=1.0
37 probe n.mob     x=0.05 y=0.2
38 probe p.mob     x=0.05 y=1.8
39 solve vanode=0.1
40 log outfile=diodeex09.log append
41 solve vanode=1.0
42
43 go atlas
44 mesh infile=diodeex09.str
45 models bipolar temperature=250 kla analytic
46 probe lat.temp x=0.05 y=1.0
47 probe n.mob     x=0.05 y=0.2
48 probe p.mob     x=0.05 y=1.8
49 solve vanode=0.1
50 log outfile=diodeex09.log append
51 solve vanode=1.0
52
53 go atlas
54 mesh infile=diodeex09.str
55 models bipolar temperature=300 kla analytic
56 probe lat.temp x=0.05 y=1.0
57 probe n.mob     x=0.05 y=0.2
58 probe p.mob     x=0.05 y=1.8
59 solve vanode=0.1
60 log outfile=diodeex09.log append
61 solve vanode=1.0
62
```

```
63 go atlas
64 mesh infile=diodeex09.str
65 models bipolar temperature=350 kla analytic
66 probe lat.temp x=0.05 y=1.0
67 probe n.mob    x=0.05 y=0.2
68 probe p.mob    x=0.05 y=1.8
69 solve vanode=0.1
70 log outfile=diodeex09.log append
71 solve vanode=1.0
72
73 go atlas
74 mesh infile=diodeex09.str
75 models bipolar temperature=400 kla analytic
76 probe lat.temp x=0.05 y=1.0
77 probe n.mob    x=0.05 y=0.2
78 probe p.mob    x=0.05 y=1.8
79 solve vanode=0.1
80 log outfile=diodeex09.log append
81 solve vanode=1.0
82
83 go atlas
84 mesh infile=diodeex09.str
85 models bipolar temperature=450 kla analytic
86 probe lat.temp x=0.05 y=1.0
87 probe n.mob    x=0.05 y=0.2
88 probe p.mob    x=0.05 y=1.8
89 solve vanode=0.1
90 log outfile=diodeex09.log append
91 solve vanode=1.0
92
93 go atlas
94 mesh infile=diodeex09.str
95 models bipolar temperature=500 kla analytic
96 probe lat.temp x=0.05 y=1.0
97 probe n.mob    x=0.05 y=0.2
98 probe p.mob    x=0.05 y=1.8
99 solve vanode=0.1
100 log outfile=diodeex09.log append
101 solve vanode=1.0
102
103 go atlas
104 mesh infile=diodeex09.str
105 models bipolar temperature=550 kla analytic
```

```
106 probe lat.temp x=0.05 y=1.0
107 probe n.mob     x=0.05 y=0.2
108 probe p.mob     x=0.05 y=1.8
109 solve vanode=0.1
110 log outfile=diodeex09.log append
111 solve vanode=1.0
112
113 go atlas
114 mesh infile=diodeex09.str
115 models bipolar temperature=600 kia analytic
116 probe lat.temp x=0.05 y=1.0
117 probe n.mob     x=0.05 y=0.2
118 probe p.mob     x=0.05 y=1.8
119 solve vanode=0.1
120 log outfile=diodeex09.log append
121 solve vanode=1.0
122
123 go atlas
124 mesh infile=diodeex09.str
125 models bipolar temperature=650 kia analytic
126 probe lat.temp x=0.05 y=1.0
127 probe n.mob     x=0.05 y=0.2
128 probe p.mob     x=0.05 y=1.8
129 solve vanode=0.1
130 log outfile=diodeex09.log append
131 solve vanode=1.0
132
133 go atlas
134 mesh infile=diodeex09.str
135 models bipolar temperature=700 kia analytic
136 probe lat.temp x=0.05 y=1.0
137 probe n.mob     x=0.05 y=0.2
138 probe p.mob     x=0.05 y=1.8
139 solve vanode=0.1
140 log outfile=diodeex09.log append
141 solve vanode=1.0
142
143 go atlas
144 mesh infile=diodeex09.str
145 models bipolar temperature=750 kia analytic
146 probe lat.temp x=0.05 y=1.0
147 probe n.mob     x=0.05 y=0.2
148 probe p.mob     x=0.05 y=1.8
```

```
149 solve vanode=0.1
150 log outfile=diodeex09.log append
151 solve vanode=1.0
152
153 go atlas
154 mesh infile=diodeex09.str
155 models bipolar temperature=800 kla analytic
156 probe lat.temp x=0.05 y=1.0
157 probe n.mob x=0.05 y=0.2
158 probe p.mob x=0.05 y=1.8
159 solve vanode=0.1
160 log outfile=diodeex09.log append
161 solve vanode=1.0
162
163 go atlas
164 mesh infile=diodeex09.str
165 models bipolar temperature=850 kla analytic
166 probe lat.temp x=0.05 y=1.0
167 probe n.mob x=0.05 y=0.2
168 probe p.mob x=0.05 y=1.8
169 solve vanode=0.1
170 log outfile=diodeex09.log append
171 solve vanode=1.0
172
173 go atlas
174 mesh infile=diodeex09.str
175 models bipolar temperature=900 kla analytic
176 probe lat.temp x=0.05 y=1.0
177 probe n.mob x=0.05 y=0.2
178 probe p.mob x=0.05 y=1.8
179 solve vanode=0.1
180 log outfile=diodeex09.log append
181 solve vanode=1.0
182
183 go atlas
184 mesh infile=diodeex09.str
185 models bipolar temperature=950 kla analytic
186 probe lat.temp x=0.05 y=1.0
187 probe n.mob x=0.05 y=0.2
188 probe p.mob x=0.05 y=1.8
189 solve vanode=0.1
190 log outfile=diodeex09.log append
191 solve vanode=1.0
```

```
192
193 go atlas
194 mesh infile=diodeex09.str
195 models bipolar temperature=1000 kla analytic
196 probe lat.temp x=0.05 y=1.0
197 probe n.mob     x=0.05 y=0.2
198 probe p.mob     x=0.05 y=1.8
199 solve vanode=0.1
200 log outfile=diodeex09.log append
201 solve vanode=1.0
202
203 tonyplot diodeex09.log -set diodeex09.set
204 tonyplot diodeex09.log -set diodeex09_mob.set
205
206 quit
```

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5.1. SOI: SOI Application Examples

5.1.1. soiex01.in: Partially Depleted SOI - V_t and Subthreshold Slope

Required: S-PISCES

This example simulates the Ids/Vgs characteristics of a thick film SOI MOSFET and from these results extracts the threshold voltage and subthreshold slope. These are two key parameters involved in the design of any SOI MOSFET. It demonstrates:

- Basic SOI structure definition using ATLAS syntax
- Setting transport models including impact ionization
- Generating an Ids/Vgs curve with Vds=0.1V
- Extracting threshold voltage and subthreshold slope from the results
- Plotting output curves and structures

The SOI device is a partially depleted device composed of a 0.2 micron layer of silicon on a 0.4 micron silicon dioxide substrate. The device has a 17 nm thick gate oxide and a gate length of 1.0 microns. For simplicity there is no silicon below the back oxide. Other examples in this section do include a silicon substrate.

The device mesh, region specification and electrode definition are done using the mesh, region and electrode statements at the start of the input file. The doping is added as simple analytical functions. The channel doping in this simple example is presumed a constant. Gaussian source and drain profiles are used. No LDD or spacer is considered in this case.

After the structure description the interface statement is used to define fixed oxide charges on both silicon - silicon dioxide interfaces. Next the contact statement is used to specify the work-function on the poly-silicon gate.

The model statement is used to specify a reasonable set of physical models for SOI simulation. In this case, concentration dependent mobility, SRH recombination, Auger recombination, band-gap narrowing, and parallel electric field dependent mobility are specified.

After the initial solution, a negative gate voltage is applied followed by solutions at drain biases of 0.05 and 0.1 volts are obtained. Next, the log statement is used to specify a file for collection of the Id/Vgs characteristics of the SOI device. These characteristics are captured with the following solve statement where the gate bias is ramped in 0.1 volt increments from -0.2 volts up to 1.5 volt.

After the voltages have been solved extract statements are used to find the threshold voltage and the subthreshold slope of the SOI MOSFET.

Finally, the resultant Id/Vgs curve is plotted using TONYPLOT.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

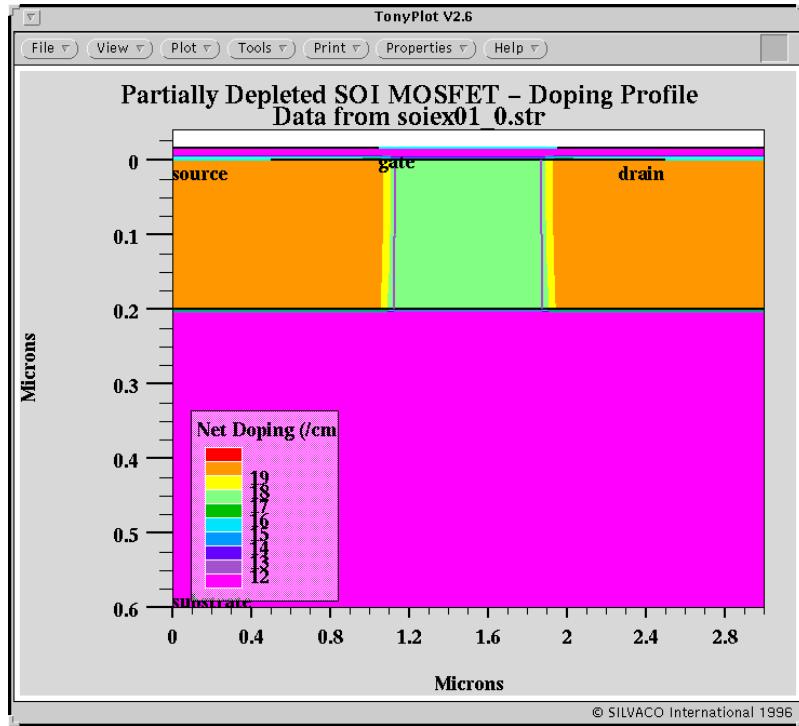


Figure 5.1: Doping and Geometry of a partially depleted SOI device defined using ATLAS syntax

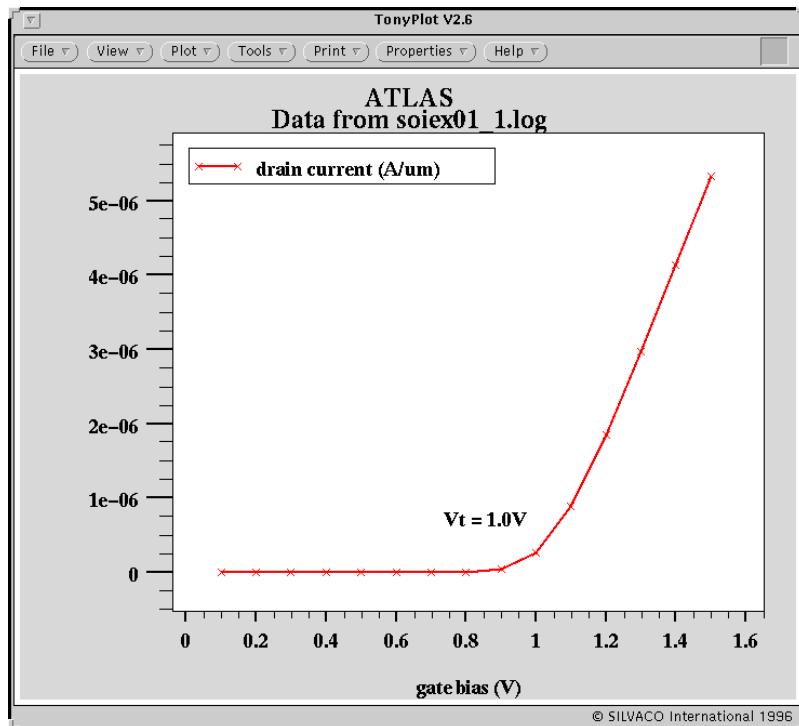


Figure 5.2: Id/Vgs curve from the partially depleted SOI

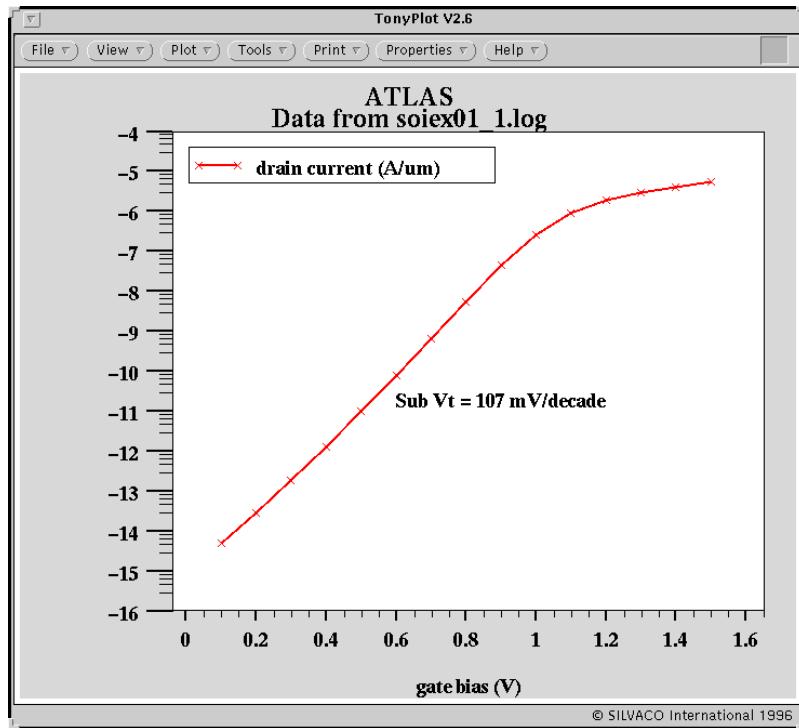


Figure 5.3: Subthreshold behavior of the PD-SOI

Input File soi/soiex01.in:

```

1 go atlas
2 TITLE SOI device simulation
3 # SILVACO International 1992, 1993, 1994, 1995, 1996
4 #
5 # 0.2um of silicon on 0.4um oxide substrate
6 #
7 mesh space.mult=1.0
8 #
9 x.mesh loc=0.00    spac=0.50
10 x.mesh loc=1.15   spac=0.02
11 x.mesh loc=1.5    spac=0.1
12 x.mesh loc=1.85   spac=0.02
13 x.mesh loc=3      spac=0.5
14 #
15 y.mesh loc=-0.017 spac=0.02
16 y.mesh loc=0.00    spac=0.005
17 y.mesh loc=0.1     spac=0.02
18 y.mesh loc=0.2     spac=0.01
19 y.mesh loc=0.6     spac=0.25
20 #
21 region      num=1 y.max=0 oxide

```

```
22 region      num=2 y.min=0 y.max=0.2 silicon
23 region      num=3 y.min=0.2   oxide
24 #
25 ***** define the electrodes *****
26 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
27 #
28 electrode    name=gate    x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
29 electrode    name=source  x.max=0.5 y.min=0 y.max=0
30 electrode    name=drain   x.min=2.5 y.min=0 y.max=0
31 electrode    substrate
32 #
33 ***** define the doping concentrations *****
34 #
35 doping       uniform conc=2e17 p.type  reg=2
36 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
37 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
38 save        outf=soiex01_0.str
39 tonyplot    soiex01_0.str -set soiex01_0.set
40 #
41 # set interface charge separately on front and back oxide interfaces
42 interf      qf=3e10 y.max=0.1
43 interf      qf=1e11 y.min=0.1
44 #
45 # set workfunction of gate
46 contact     name=gate n.poly
47 #
48 # select models
49 models      conmob srh auger bgn fldmob print
50 #
51 solve init
52 #
53 # do IDVG characteristic
54 #
55 method      newton    trap
56 solve       prev
57 solve       vgate=-0.2
58 solve       vdrain=0.05
59 solve       vd़rain=0.1
60 #
61 # ramp gate voltage
62 log         outf=soiex01_1.log master
63 solve       vgate=0.1 vstep=0.1 name=gate vfinal=1.5
64 #
```

```

65 # plot resultant IDVG threshold voltage curve
66 tonyplot    soiex01_1.log -set soiex01_1.set
67 #
68 # plot resultant IDVG subthreshold slope curve
69 tonyplot    soiex01_1.log -set soiex01_2.set
70 #
71 #
72 extract name="subvbt" \
73     1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
74 #
75 #
76 extract name="vt" (xintercept(maxs-
    llope(curve(abs(v."gate"),abs(i."drain")))) ) \
77     - abs(ave(v."drain"))/2.0)
78 #
79 quit
80
81
82

```

5.1.2. soiex02.in: Fully Depleted SOI - Vt and Subthreshold Slope

Required: S-PISCES

This example repeats soiex01.in but for a device that has been designed to operate with a fully depleted SOI film. It demonstrates:

- Basic SOI structure definition using ATLAS syntax
- Setting transport models including impact ionization
- Generating an Id/Vgs curve with Vds=0.1V
- Extracting threshold voltage and subthreshold slope from the results
- Plotting output curves and structures.

Thin film fully depleted SOI MOSFETs have been shown to achieve low threshold voltages and near ideal inverse subthreshold slopes. This makes them ideal for low power operation. This example demonstrates that ATLAS is capable of reproducing the differences between a partially depleted transistor in soiex01.in and the fully depleted transistor in this example.

The syntax and methodology used within this example are identical to that of soiex01.in with only two three modifications.

The mesh has been modified to support the thinner SOI film thickness of 0.1um and the definition of the SOI layers on the region statement has similarly been adapted. Also, the channel doping has been reduced on the doping statement to ensure the film is fully depleted.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

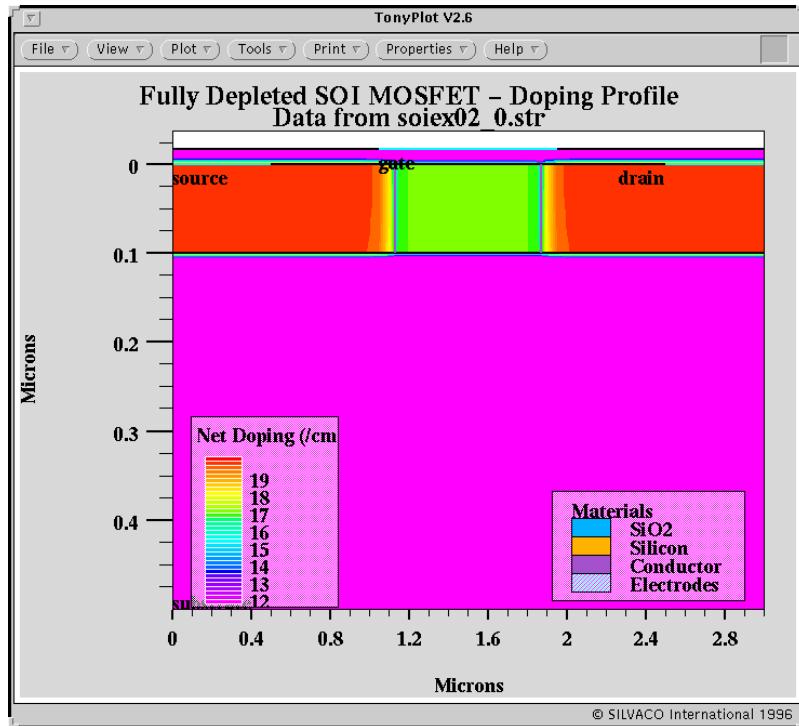


Figure 5.4: Doping and Geometry of a fully depleted SOI device defined using ATLAS syntax

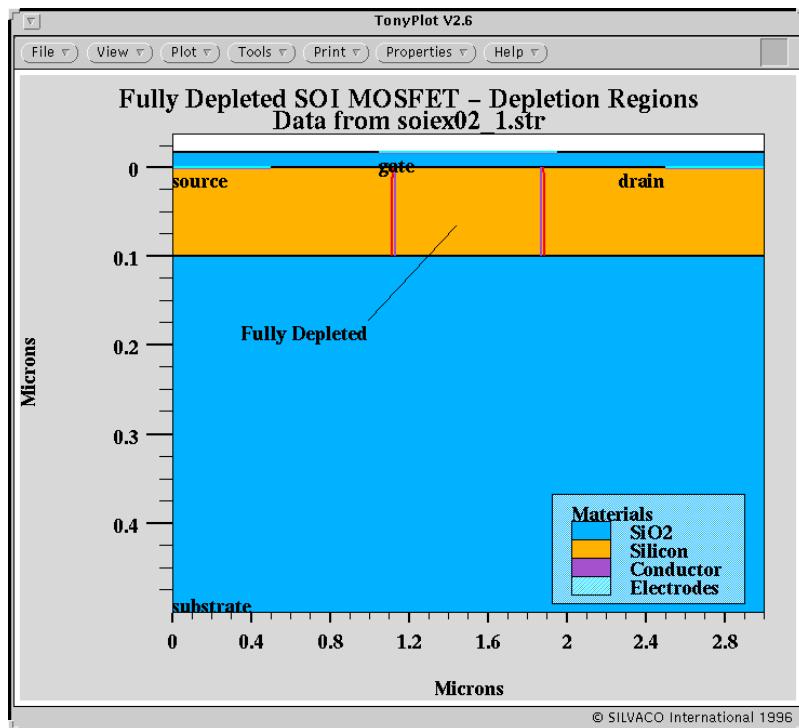


Figure 5.5: Regions and junction for the FD-SOI

Input File soi/soiex02.in:

```

1 go atlas
2 TITLE SOI device simulation
3 # SILVACO International 1992, 1993, 1994, 1995, 1996
4 #
5 # 0.1um of silicon on 0.4um oxide substrate
6 #
7 mesh space.mult=1.0
8 #
9 x.mesh loc=0.00 spac=0.50
10 x.mesh loc=1.15 spac=0.02
11 x.mesh loc=1.5 spac=0.1
12 x.mesh loc=1.85 spac=0.02
13 x.mesh loc=3 spac=0.5
14 #
15 y.mesh loc=-0.017 spac=0.02
16 y.mesh loc=0.00 spac=0.005
17 y.mesh loc=0.05 spac=0.02
18 y.mesh loc=0.1 spac=0.01
19 y.mesh loc=0.5 spac=0.25
20 #
21 region num=1 y.max=0 oxide
22 region num=2 y.min=0 y.max=0.1 silicon
23 region num=3 y.min=0.1 oxide
24 #
25 ***** define the electrodes *****
26 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
27 #
28 electrode name=gate x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
29 electrode name=source x.max=0.5 y.min=0 y.max=0
30 electrode name=drain x.min=2.5 y.min=0 y.max=0
31 electrode substrate
32 #
33 ***** define the doping concentrations *****
34 #
35 doping uniform conc=1e17 p.type reg=2
36 doping gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
37 doping gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
38 save outf=soiex02_0.str
39 tonyplot soiex02_0.str -set soiex02_0.set
40 #
41 # set interface charge separately on front and back oxide interfaces
42 interf qf=3e10 y.max=0.05

```

```
43 interf      qf=lell1 y.min=0.05
44 #
45 # set workfunction of gate
46 contact      name=gate n.poly
47 #
48 # select models
49 models       conmob srh auger bgn fldmob print
50 #
51 solve init
52 #
53 # do IDVG characteristic
54 #
55 method       newton   trap
56 solve        prev
57 solve        vgate=-0.2
58 solve        vdrain=0.05
59 solve        vdऱain=0.1
60 #
61 # ramp gate voltage
62 log          outf=soiex02_1.log master
63 solve        vgate=0.1 vstep=0.1 name=gate vfinal=1.5
64 #
65 # plot resultant IDVG threshold voltage curve
66 tonyplot     soiex02_1.log -set soiex02_1.set
67 #
68 # plot resultant IDVG subthreshold slope curve
69 tonyplot     soiex02_1.log -set soiex02_2.set
70 #
71 #
72 extract name="subvt" \
73           1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))
74 #
75 #
76 extract name="vt" (xintercept(maxs-
    lope(curve(abs(v."gate"),abs(i."drain")))) \
77           - abs(ave(v."drain"))/2.0)
78 #
79 quit
80
81
82
```

5.1.3. soiex03.in: Partially vs Fully Depleted SOI - Leakage Current Analysis

Required: S-PISCES

This example simulates leakage current at high drain bias and shows how this value can be extracted as a design parameter. The analysis is repeated for both fully depleted and partially depleted SOI MOSFETs. It demonstrates:

- Basic SOI structure definition using ATLAS syntax
- DECKBUILD syntax for defining general structure dimensions
- Setting transport models including impact ionization
- Generating an Id/Vds curve with Vgs=0.0V
- Extracting the leakage current design parameter
- Plotting output curves and structures.

The leakage current in SOI MOSFETs has in the past been seen as a barrier to its development. The source of this current has, in some cases, been due to the existence of interface charge at the bottom oxide-silicon interface. This example simulates the leakage current analysis for both partially and fully depleted SOI MOSFETs.

In this example, rather than use two ATLAS input files for thick and thin SOI films, a more general purpose input file has been created. By using DECKBUILD set commands it is possible to create variables inside the input file. These variables may then be used to define the location of mesh lines or region boundaries.

In this example specifically, there have been three modifications made to the input file. The `y.mesh` definition has been modified to use the created variables to define the location of `y` mesh lines and, in a similar manner, the `region` statement has also been changed to use these variables to define the region boundaries. Interface charges, on both the top and bottom interfaces, are defined on the `interface` statement. In SOI MOSFET's, these two interfaces can have very different values of interface charge as is shown in this example. Once again the predefined variables have been used to define the regions where the charge exists.

Submicron devices should be simulated using the Energy Balance Model due to velocity overshoot, and nonlocal impact ionization effects, which could substantially influence device characteristics. The `models hcte` statement is used to set the solution for electron and hole energy balance. Next, the `impact` statement is used to specify that the Selberherr impact ionization model is to be used. Impact ionization is an important phenomena in SOI devices even at relatively low voltages. The `impact` model is required here for this SOI Id/Vds analysis.

The remaining ATLAS syntax and methodology is based upon that of `soiex01.in` and a description of it may be found there.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DeckBuild, select the **run** button to execute the example. This example initially has been set up to simulate a thick film partially depleted transistor. To simulate the thin film fully depleted transistor case, the `set` statements need to be changed to:

```
set simid=0.05 set sibot=0.1 set oxbot=0.5
```

and the example executed once again.

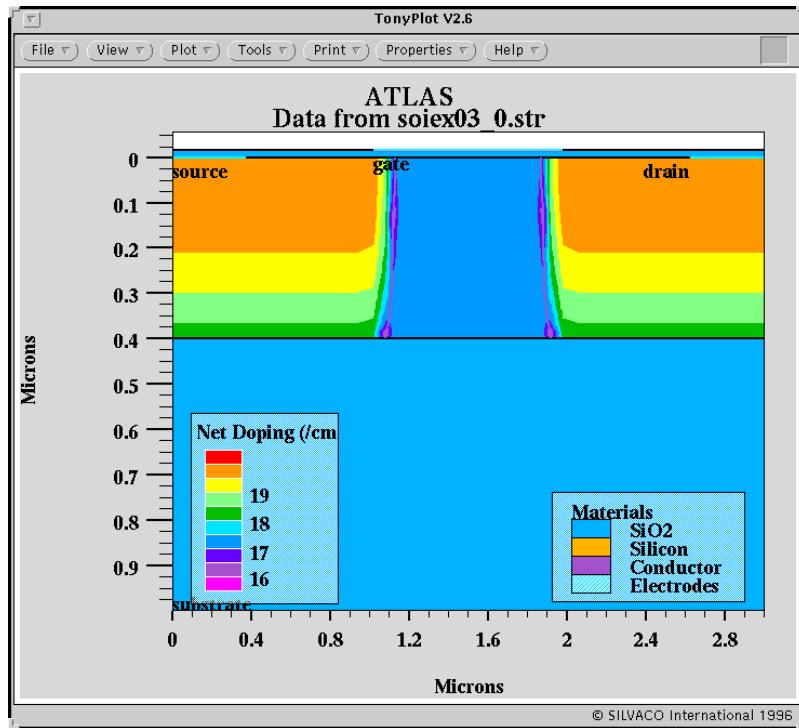


Figure 5.6: SOI device defined using variable substitutions in ATLAS. The layer thicknesses can be scaled by altering a single number in the input file

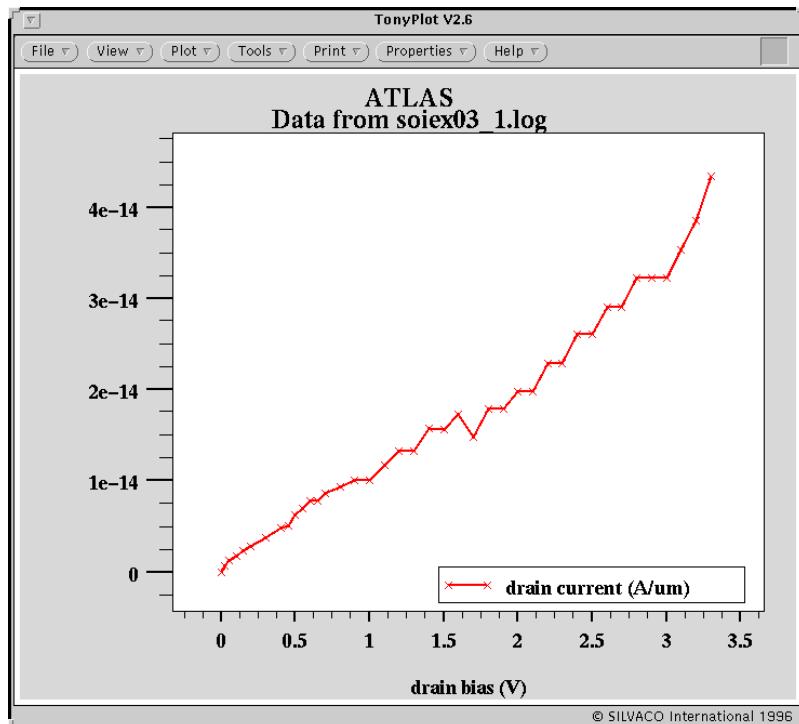


Figure 5.7: Leakage current from a typical SOI case

Input File soi/soiex03.in:

```
1 go atlas
2 #
3 # Define deckbuild variables
4 set simid=0.2
5 set sibot=0.4
6 set oxbot=1.0
7 #
8 TITLE SOI device simulation
9 # SILVACO International 1992, 1993, 1994, 1995, 1996
10 #
11 # 0.4um of silicon on 0.6um oxide substrate
12 #
13 mesh space.mult=1.5
14 #
15 x.mesh loc=0.00    spac=0.250
16 x.mesh loc=1.15    spac=0.02
17 x.mesh loc=1.5     spac=0.05
18 x.mesh loc=1.85    spac=0.02
19 x.mesh loc=3       spac=0.25
20 #
21 y.mesh loc=-0.017  spac=0.25
22 y.mesh loc=0.00    spac=0.0025
23 y.mesh loc=$simid spac=0.02
24 y.mesh loc=$sibot spac=0.005
25 y.mesh loc=$oxbot spac=0.1
26 #
27 region      num=1 y.max=0 oxide
28 region      num=2 y.min=0 y.max=$sibot silicon
29 region      num=3 y.min=$sibot oxide
30 #
31 ***** define the electrodes *****
32 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
33 #
34 electrode   name=gate    x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
35 electrode   name=source  x.max=0.5 y.min=0 y.max=0
36 electrode   name=drain   x.min=2.5 y.min=0 y.max=0
37 electrode   substrate
38 #
39 ***** define the doping concentrations *****
40 #
41 doping      uniform conc=1.75e17 p.type reg=2
42 doping      gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
```

```
43 doping      gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
44 save        outf=soiex03_0.str
45 tonyplot    soiex03_0.str -set soiex03_0.set
46 #
47 # set interface charge separately on front and back oxide interfaces
48 interf      qf=3e10 y.max=$simid
49 interf      qf=1e11 y.min=$simid
50 #
51 # set workfunction of gate
52 contact     name=gate n.poly
53 #
54 # select models
55 models      conmob srh bgn fldmob print hcte
56 impact      selb
57 #
58 solve init
59 #
60 method      newton autonr trap maxtrap=10
61 #
62 # Perform leakage current analysis
63 log         outf=soiex03_1.log
64 solve      prev
65 solve      vdrain=0.05
66 solve      vdrain=0.1 vfinal=3.3 vstep=0.1 name=drain
67 #
68 extract name="ids_leakage" max(abs(i."drain"))
69 #
70 # plot resultant IDVD leakage current curve
71 tonyplot   soiex03_1.log -set soiex03_1.set
72 #
73 quit
```

5.1.4. soiex04.in: The “Kink” Effect in Partially Depleted SOI MOSFETs

Requires: S-PISCES

This example simulates the Id_s/V_{ds} characteristics of a partially depleted SOI MOSFET, described in example soiex01.in, for three gate voltages. The effect of impact ionization at the drain junction causes the silicon film to be raised in potential and causes a shift in the threshold voltage. This is seen as a “kink” in the Id_s/V_{gs} curves. The file shows:

- Basic SOI structure definition using ATLAS syntax
- Setting transport models including impact ionization
- Generating an Id_s/V_{ds} curve with $V_{gs}=1V$, $2V$ and $3V$
- Plotting output curves and structures.

The ATLAS syntax and methodology is based upon that of `soiex01.in` and a description of it may be found there.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

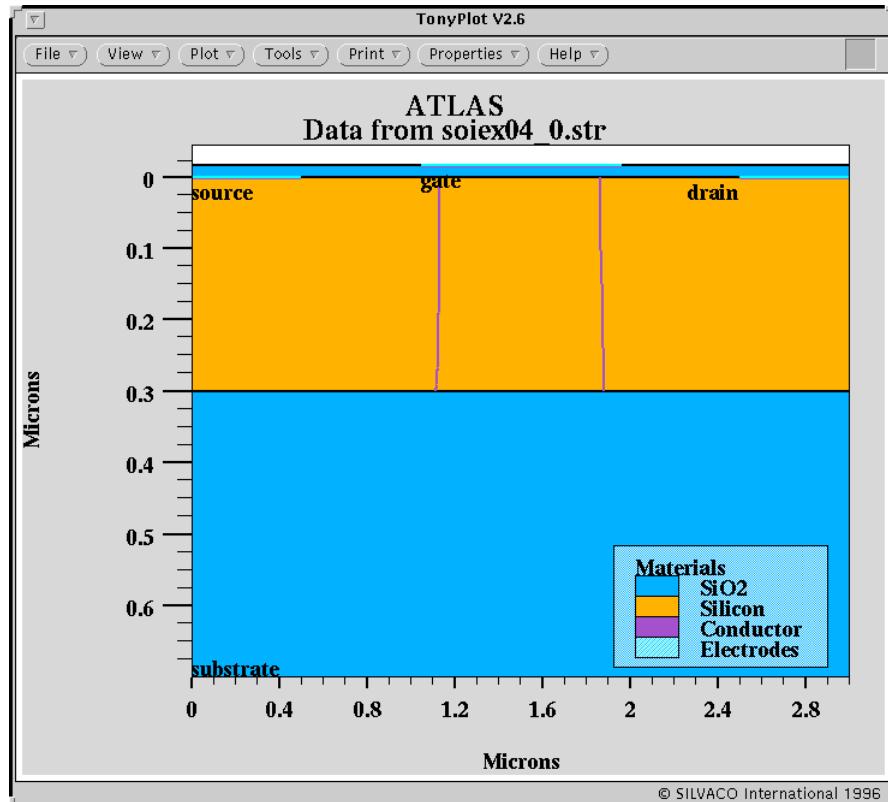


Figure 5.8: Regions and junctions for a PD-SOI

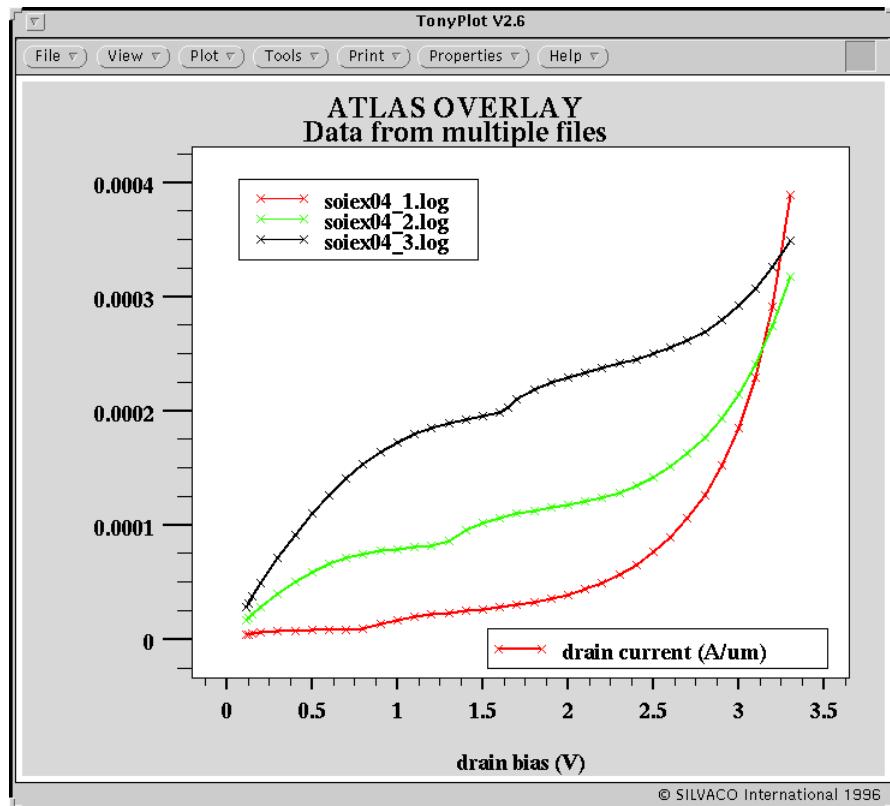


Figure 5.9: Id/Vds curves showing the 'kink' effect at various Vgs for PD-SOI

Input File soi/soiex04.in:

```

1 go atlas
2 TITLE SOI device simulation
3 # SILVACO International 1992, 1993, 1994, 1995, 1996
4 #
5 # 0.2um of silicon on 0.4um oxide substrate
6 #
7 mesh space.mult=1.0
8 #
9 x.mesh loc=0.00 spac=0.50
10 x.mesh loc=1.15 spac=0.02
11 x.mesh loc=1.5 spac=0.1
12 x.mesh loc=1.85 spac=0.01
13 x.mesh loc=3 spac=0.5
14 #
15 y.mesh loc=-0.017 spac=0.02
16 y.mesh loc=0.00 spac=0.005
17 y.mesh loc=0.15 spac=0.02
18 y.mesh loc=0.3 spac=0.01
19 y.mesh loc=0.7 spac=0.25

```

```
20 #
21 region      num=1 y.max=0 oxide
22 region      num=2 y.min=0 y.max=0.3 silicon
23 region      num=3 y.min=0.3  oxide
24 #
25 ***** define the electrodes *****
26 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
27 #
28 electrode   name=gate    x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
29 electrode   name=source  x.max=0.5 y.min=0 y.max=0
30 electrode   name=drain   x.min=2.5 y.min=0 y.max=0
31 electrode   substrate
32 #
33 ***** define the doping concentrations *****
34 #
35 doping       uniform conc=1e17 p.type  reg=2
36 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
37 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
38 save        outf=soiex04_0.str
39 tonyplot    soiex04_0.str -set soiex04_0.set
40 #
41 # set interface charge separately on front and back oxide interfaces
42 interf      qf=3e10 y.max=0.1
43 interf      qf=1e11 y.min=0.1
44 #
45 # set workfunction of gate
46 contact     name=gate n.poly
47 #
48 # select models
49 models      cvt srh bgn print
50 #
51 impact      selb
52 solve       init
53 #
54 # do IDVG characteristic
55 #
56 method      newton trap maxtrap=10
57 solve       prev
58 solve       vdrain=0.05
59 solve       vdrain=0.1
60 #
61 # ramp gate voltage to 1, 2 and 3V
62 solve       vgate=0.2 vstep=0.2 name=gate vfinal=1
```

```
63 save      outf=soiex04_1.str
64 solve     vgate=0.2 vstep=0.2 name=gate vfinal=2
65 save      outf=soiex04_2.str
66 solve     vgate=0.2 vstep=0.2 name=gate vfinal=3
67 save      outf=soiex04_3.str
68 #
69 # Now do ID/VDS characteristic
70 load      infile=soiex04_1.str master
71 solve     prev
72 log       outf=soiex04_1.log
73 solve     vfinal=3.3 vstep=0.1 name=drain
74 log       outf=tmp
75 #
76 load      infile=soiex04_2.str master
77 solve     prev
78 log       outf=soiex04_2.log
79 solve     vfinal=3.3 vstep=0.1 name=drain
80 log       outf=tmp
81 #
82 load      infile=soiex04_3.str master
83 solve     prev
84 log       outf=soiex04_3.log
85 solve     vfinal=3.3 vstep=0.1 name=drain
86 #
87 tonyplot -overlay soiex04_1.log soiex04_2.log soiex04_3.log -set
    soiex04_1.set
88 quit
```

5.1.5. soiex05.in: Negative Transconductance - Effect of Lattice Heating

Requires: S-PISCES/GIGA

This example compares the results of Ids/Vds curves for an SOI transistor using isothermal and non-isothermal approaches. The heating of the silicon film causes a negative saturation slope. The file shows:

- SOI structure formation using ATLAS syntax
- selection of the lattice heating model
- selection of thermal boundary conditions
- Id/Vds simulation for Vgs=10V
- repetition of the Ids/Vds curve excluding lattice heating for comparison

There are two ATLAS runs in this example file. The first uses lattice heating and the second uses isothermal models.

The initial phase of the input file constructs an SOI device using the ATLAS syntax. The mesh, region and electrode statements are used to define the geometry and mesh of the structure. The

doping statement is used to define analytical doping profiles. A uniformly p-doped silicon film is used with heavy Gaussian n+ source and drain regions.

The heat flow equation is selected using models lat.temp. Other models such as arora are used to define a temperature dependent mobility model. Local lattice temperature is used in the documented mobility model equations. In simulations with lattice heating the thermal boundary conditions are crucial. The thermcontact statement defines the heat sink. The heat sink is on the bottom of the silicon substrate region. All other boundaries are presumed to be in thermal isolation.

The choice of numerical method in SOI device simulation is also important. The standard newton method has some convergence problems in floating body devices. As impact ionization occurs the initial guess to the potential of the floating channel region becomes more difficult. The newton method, which relies on a good initial guess, can encounter convergence difficulties. These difficulties are generally not fatal to the simulation, but require small voltage steps to be used. This adds to the CPU time considerably. A more robust method available in ATLAS is by choosing the combined gummel/newton algorithm.

In addition, the solution of the heat flow equation must also be included. The most robust method once the temperature rises above the heat sink level is newton. However in the early stages of the solution the decoupled block method is better. ATLAS can switch between these methods so all are included in the method gummel block newton statement.

The electrical solutions for Ids/Vds is defined in a similar manner to the regular NMOS example described in the MOS examples section.

The simulation with lattice heat is exactly analogous to the subsequent one using isothermal models. The run differs only in having no lat.temp or thermcontact definition.

Id/Vds curves from the two runs can be overlaid in TONYPLOT showing the effect of lattice heating on the device performance. The increased temperature causes the mobility to decrease as the drain bias rises leading to a negative saturation slope. Comparison of the physical variables at the same bias is also possible from the saved solution files. Plotting impact ionization in each case shows how the elevated lattice temperature reduces the impact ionization rate.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

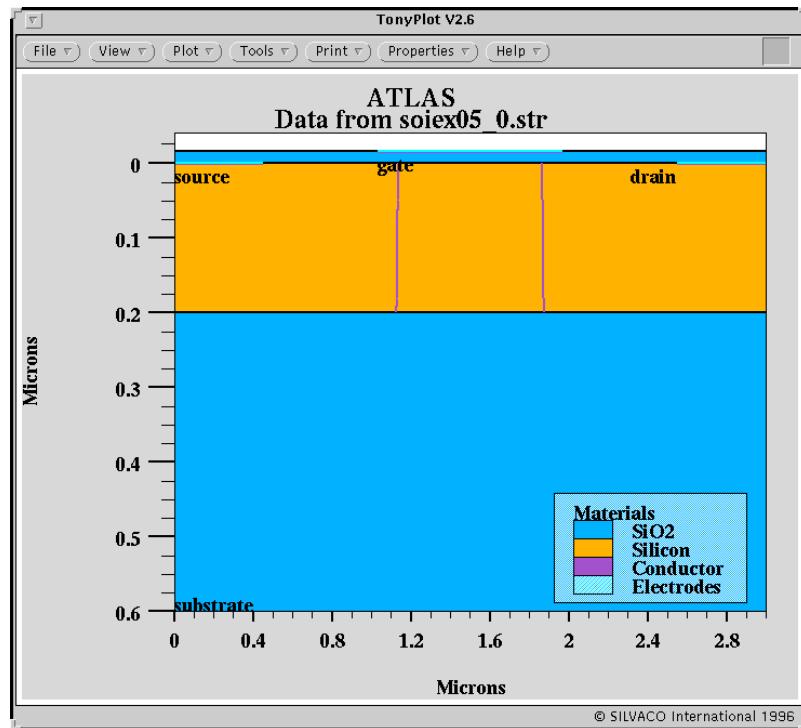


Figure 5.10: Geometry and junction for an FD-SOI

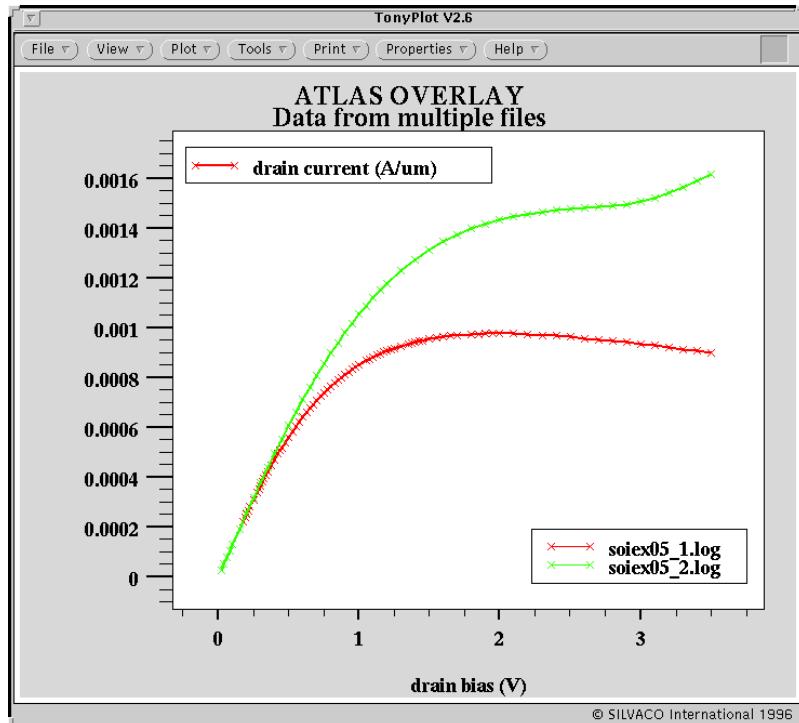


Figure 5.11: Demonstration of the effect of lattice heating (lower curve) on I_d/V_{ds} . Heating the SOI film causes negative conductance.

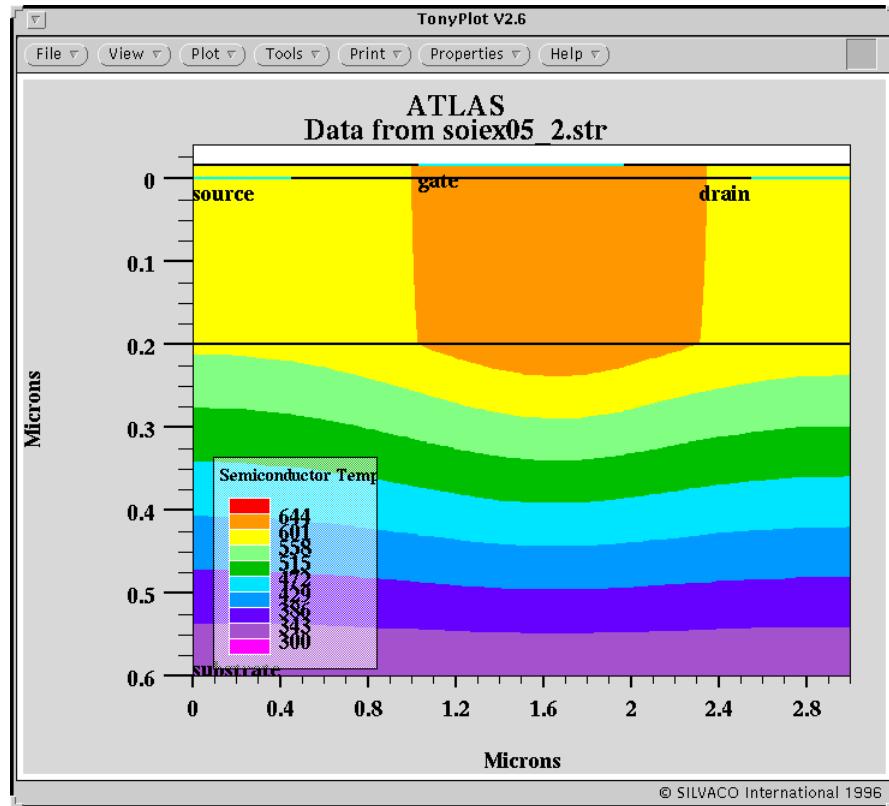


Figure 5.12: Contours showing heated SOI film. Heat sink is at the bottom below the BOX insulator.

Input File soi/soiex05.in:

```

1 go atlas
2 TITLE SOI ID/VDS @ VGS=10V with LATTICE HEATING
3 # SILVACO International 1992, 1993, 1994, 1995, 1996
4
5 mesh space.mult=1.0
6 #
7 x.mesh loc=0.00    spac=0.250
8 x.mesh loc=1.15    spac=0.02
9 x.mesh loc=1.5     spac=0.1
10 x.mesh loc=1.85   spac=0.02
11 x.mesh loc=3      spac=0.25
12 #
13 y.mesh loc=-0.017 spac=0.02
14 y.mesh loc=0.00    spac=0.005
15 y.mesh loc=0.1     spac=0.02
16 y.mesh loc=0.2     spac=0.01
17 y.mesh loc=0.6     spac=0.1
18 #
19 region      num=1 y.max=0 oxide

```

```
20 region      num=2 y.min=0 y.max=0.2 silicon
21 region      num=3 y.min=0.2   oxide
22 #
23 ***** define the electrodes *****
24 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
25 #
26 electrode    name=gate     x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
27 electrode    name=source   x.max=0.5 y.min=0 y.max=0
28 electrode    name=drain    x.min=2.5 y.min=0 y.max=0
29 electrode    substrate
30 #
31 ***** define the doping concentrations *****
32 #
33 doping       uniform conc=1e17 p.type  reg=2
34 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
35 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
36 #
37 contact     name=gate n.poly
38 #
39 models      arora consrh auger bgn fldmob lat.temp
40 impact      selb
41 #
42 thermcontact number=1 y.min=0.6 ext.temper=300
43 #
44 solve       init
45 save        outf=soiex05_0.str
46 #
47 tonyplot    soiex05_0.str -set soiex05_0.set
48 #
49 method      block newton itlimit=15 trap
50 solve       vgate=0.1
51 solve       vgate=0.2
52 solve       vgate=0.3
53 solve       vgate=0.4
54 solve       vgate=0.5
55 solve       vgate=0.75
56 solve       vgate=1 vstep=1 vfinal=10.0 name=gate
57 #
58 method      block newton itlimit=15 trap
59 #
60 log         outf=soiex05_1.log master
61 solve       vstep=0.020 vfinal=0.1 name=drain
62 solve       vstep=0.050 vfinal=1.2 name=drain
```

```
63 solve      vdrain=1.3 vstep=0.1 vfinal=3.5 name=drain
64 save       outf=soiex05_2.str
65 #
66 go atlas
67 TITLE SOI ID/VDS @ VGS=10V without LATTICE HEATING
68 # SILVACO International 1992, 1993, 1994
69 #
70 mesh space.mult=1.0
71 #
72 x.mesh loc=0.00    spac=0.250
73 x.mesh loc=1.15    spac=0.02
74 x.mesh loc=1.5     spac=0.1
75 x.mesh loc=1.85    spac=0.02
76 x.mesh loc=3       spac=0.25
77 #
78 y.mesh loc=-0.017  spac=0.02
79 y.mesh loc=0.00    spac=0.005
80 y.mesh loc=0.1     spac=0.02
81 y.mesh loc=0.2     spac=0.01
82 y.mesh loc=0.6     spac=0.1
83 #
84 region      num=1 y.max=0 oxide
85 region      num=2 y.min=0 y.max=0.2 silicon
86 region      num=3 y.min=0.2  oxide
87 #
88 ***** define the electrodes *****
89 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
90 #
91 electrode   name=gate    x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
92 electrode   name=source  x.max=0.5 y.min=0 y.max=0
93 electrode   name=drain   x.min=2.5 y.min=0 y.max=0
94 electrode   substrate
95 #
96 ***** define the doping concentrations *****
97 #
98 doping      uniform conc=1e17 p.type  reg=2
99 doping      gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
100 doping     gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
101 #
102 contact    name=gate n.poly
103 #
104 models     arora consrh auger bgn fldmob
105 impact     selb
```

```
106 #
107 solve      init
108 #
109 method      newton itlimit=15 trap
110 solve      vgate=0.1
111 solve      vgate=0.2
112 solve      vgate=0.3
113 solve      vgate=0.4
114 solve      vgate=0.5
115 solve      vgate=0.75
116 solve      vgate=1 vstep=1 vfinal=10.0 name=gate
117 #
118 method      gummel newton single itlimit=15 trap
119 #
120 log        outf=soiex05_2.log master
121 solve      vstep=0.020 vfinal=0.1 name=drain
122 #
123 method      newton itlimit=15 trap
124 solve      vstep=0.050 vfinal=1.2 name=drain
125 solve      vdrain=1.3 vstep=0.1 vfinal=3.5 name=drain
126 #
127 tonyplot -overlay soiex05_1.log soiex05_2.log -set soiex05_1.set
128 tonyplot soiex05_2.str -set soiex05_2.set
129 #
130 quit
```

5.1.6. soiex06.in: Breakdown in SOI MOSFETs - Effect of Lattice Heating

Requires: S-PISCES/GIGA

This example compares Ids/Vds analyses of a short channel ultra-thin SOI transistor with Energy Balance (EB) and Nonisothermal Energy Balance Models (NEB). It shows:

- SOI structure formation using ATLAS syntax
- selection of energy balance and lattice heating models
- selection of numerical methods for coupled solution technique
- Id/Vds simulation for Vgs=4.0V

The example file consists of two runs. The first simulates the device using energy balance models, the second using energy balance and lattice heating models combined.

Submicron devices should be simulated using the Energy Balance Model due to velocity overshoot, and nonlocal impact ionization effects, which could substantially influence device characteristics. For high current levels (high gate voltages) the thermal self-heating effects could also play an important role decreasing mobility and impact ionization rate. These effects are very pronounced in SOI transistors due to low heat conductivity of the oxide. This leads to the negative output conductance. This example demonstrates comparison of Ids/Vds curves obtained with Energy Balance and Nonisothermal Energy Balance Models.

The first ATLAS run uses the Energy Balance Model: Poisson's equation, carrier continuity equations, and the energy balance equation for electrons are solved self-consistently.

In the first part of the input file the device is described. The SOI device is composed of a 0.05 micron layer of silicon on a 0.45 micron silicon dioxide substrate. The device has a 12 nm thick gate oxide and a gate length of 0.8 microns (effective channel length is 0.5 microns).

After the device description the material statement is used to assign an energy relaxation time for electrons. The models hcte.el statement is used to set the solution for electron energy balance. Other parameters on the model statement select a set of physical models for this simulation. In this case, these models are CONSRH and AUGER recombination, the conmob and fldmob mobility model and Band Gap Narrowing. The impact length.rel lrel.el=0.02 statement is used to assign the energy relaxation length for Selberherr model. The contact statement is used to assign the work function on the polysilicon gate.

The gate voltage is ramped to 4V. At this stage combined algorithm is used method gummel newton carr=2. Thus if convergence is not reached in decoupled mode (gummel) the simulator will automatically switch to coupled mode (newton). Then the drain voltage is ramped. Again combined algorithm is used for low drain biases, and full newton scheme for higher drain biases. The method statement also defines that a two carrier solution is performed using carr=2 whereby ATLAS will solve Poisson's equation for potential and the electron and hole continuity equations.

The second ATLAS run uses Nonisothermal Energy Balance Model: Poisson's equation, carrier continuity equations, energy balance equation for electrons, and a lattice energy balance equation are solved self-consistently.

The same set of models is used, except that the solution of the lattice energy balance equation is activated using lat.temp parameter in the models statement.

In addition, thermal boundary conditions should be defined in this case. Thermal boundary conditions are defined in the thermcontact statement. A 300K temperature is specified at the thermcontact located along the bottom of the device. Thermal isolation conditions are assumed on the all other surfaces.

Id/Vds curves from the two simulations can be compared in TONYPLOT. Internal variables at the same bias point can also be compared using the saved solution files. Plots of impact ionization rate and electron temperature show the effect of the elevated temperature in the silicon film of these quantities.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

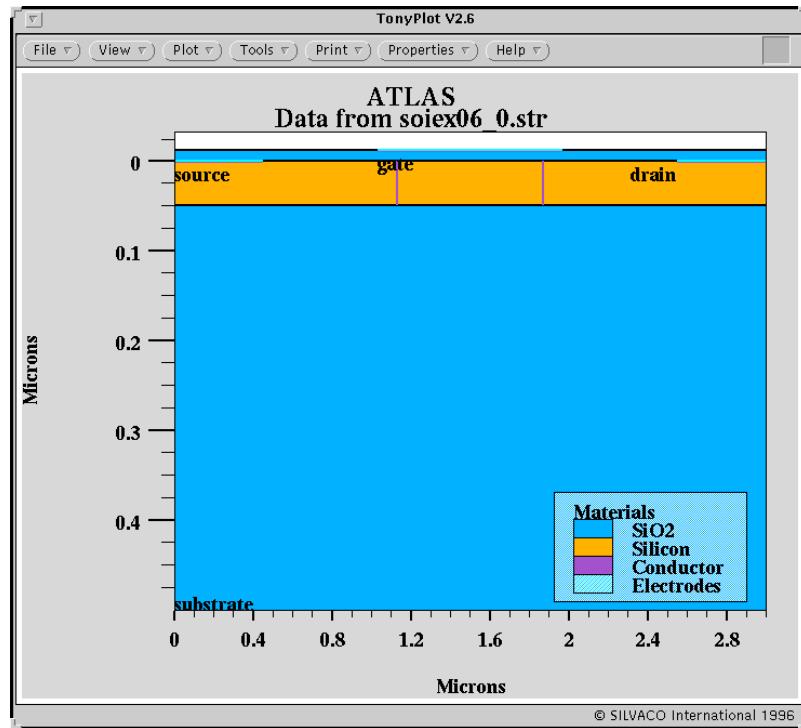


Figure 5.13: Thin film SOI device defined in ATLAS syntax

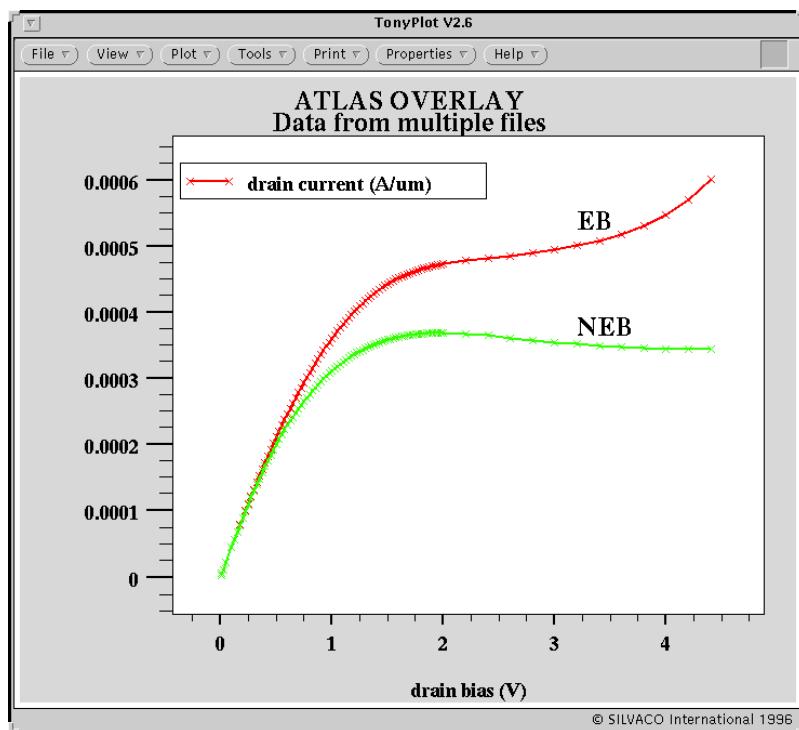


Figure 5.14: Demonstration of the effect of lattice heating (lower curve) on breakdown behavior. Heating the SOI film suppresses impact ionization and increases breakdown voltage

Input File soi/soiex06.in:

```

1 go atlas
2 TITLE Ultra-Thin SOI simulation with Energy Balance and Nonisothermal En-
   ergy Balance Models
3 # SILVACO International 1994
4
5 mesh space.mult=1.0
6 #
7 x.mesh loc=0.00    spac=0.250
8 x.mesh loc=1.15    spac=0.02
9 x.mesh loc=1.5     spac=0.05
10 x.mesh loc=1.85   spac=0.02
11 x.mesh loc=3      spac=0.25
12 #
13 y.mesh loc=-0.012 spac=0.25
14 y.mesh loc=0.00    spac=0.0025
15 y.mesh loc=0.025   spac=0.02
16 y.mesh loc=0.05    spac=0.005
17 y.mesh loc=0.5     spac=0.1
18 #
19 region      num=1 y.max=0 oxide
20 region      num=2 y.min=0 y.max=0.05 silicon
21 region      num=3 y.min=0.05  oxide
22 #
23 ***** define the electrodes *****
24 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
25 #
26 electrode   name=gate    x.min=1 x.max=2 y.min=-0.012 y.max=-0.012
27 electrode   name=source   x.max=0.5 y.min=0 y.max=0
28 electrode   name=drain    x.min=2.5 y.min=0 y.max=0
29 electrode   substrate
30 #
31 ***** define the doping concentrations *****
32 #
33 doping       uniform conc=1.75e17 p.type  reg=2
34 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
35 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
36 #
37 material    taurel.el=0.2e-12 taumob.el=0.2e-12
38 models      conmob bgn fldmob hcte.el  consrh auger print
39 #
40 impact      selb length.rel lrel.el=0.02
41 #

```

```
42 contact      number=2 n.polysilicon
43 #
44 solve        init
45 save         outf=soiex06_0.str
46 tonyplot     soiex06_0.str -set soiex06_0.set
47 #
48 method       gummel newton maxtrap=6 temp.tol=1.e-4 trap
49 #
50 # Id-Vd calculations EB model
51 solve        vgate=1
52 solve        vgate=2
53 solve        vgate=4
54 #
55 log          outf=soiex06_eb.log master
56 #
57 solve        vdrain=0.00625
58 solve        vdrain=0.0125
59 solve        vdrain=0.025
60 solve        vdrain=0.05
61 #
62 method       newton maxtrap=6 temp.tol=1.e-4 trap
63 #
64 solve        vdrain=0.1 vstep=0.025 vfinal=2 electr=3
65 #
66 solve        vdrain=2.2 vstep=0.2 electr=3 vfinal=4.5
67 save         outf=soiex06_eb.str
68 #
69 go atlas
70 #
71 mesh         space.mult=1.0
72 #
73 x.mesh loc=0.00    spac=0.250
74 x.mesh loc=1.15    spac=0.02
75 x.mesh loc=1.5     spac=0.05
76 x.mesh loc=1.85    spac=0.02
77 x.mesh loc=3       spac=0.25
78 #
79 y.mesh loc=-0.012  spac=0.25
80 y.mesh loc=0.00    spac=0.0025
81 y.mesh loc=0.025   spac=0.02
82 y.mesh loc=0.05    spac=0.005
83 y.mesh loc=0.5     spac=0.1
84 #
```

```

85 region      num=1 y.max=0 oxide
86 region      num=2 y.min=0 y.max=0.05 silicon
87 region      num=3 y.min=0.05 oxide
88 #
89 ***** define the electrodes *****
90 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
91 #
92 electrode   name=gate    x.min=1 x.max=2 y.min=-0.012 y.max=-0.012
93 electrode   name=source  x.max=0.5 y.min=0 y.max=0
94 electrode   name=drain   x.min=2.5 y.min=0 y.max=0
95 electrode   substrate
96 #
97 ***** define the doping concentrations *****
98 #
99 doping      uniform conc=1.75e17 p.type reg=2
100 doping     gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
101 doping     gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
102 #
103 thermcontact num=1   x.min=0 x.max=6.5 y.min=0.5 y.max=0.5
104 #
105 material   taurel.el=0.2e-12 taumob.el=0.2e-12
106 models     conmob bgn fldmob hcte.el lat.temp consrh auger print
107 #
108 impact     selb length.rel lrel.el=0.02
109 #
110 contact   number=2 n.polysilicon
111 #
112 solve      init
113 #
114 method     gummel newton maxtrap=6 temp.tol=1.e-4 trap
115 #
116 # Id-Vd calculations NEB model
117 #
118 solve      vgate=1
119 solve      vgate=2
120 solve      vgate=4
121 #
122 log       outf=soiex06_neb.log master
123 #
124 solve      vdrain=0.00625
125 solve      vdrain=0.0125
126 solve      vdrain=0.025
127 solve      vdrain=0.05

```

```
128 #
129 method      newton  maxtrap=6  temp.tol=1.e-4  trap
130 #
131 solve       vdrain=0.1 vstep=0.025 vfinal=2 electr=3
132 #
133 solve       vdrain=2.2 vstep=0.2 electr=3 vfinal=4.5
134 #
135 save        outf=soiex06_neb.str
136 #
137 tonyplot    -overlay  soiex06_eb.log soiex06_neb.log -set soiex06.set
138 #
139 quit
```

5.1.7. soiex07.in: 3D Device Simulation - Effect of a Body Contact

Requires: DEVICE3D

This example demonstrates Ids/Vgs and Id/Vds 3D analysis of a short channel ultra-thin SOI transistor with body contact. Such simulations cannot be performed using a 2D simulator because the body electrode is located in the out of the plane of the drain, gate and source. The example shows:

- formation of 3D structure using ATLAS syntax
- Id/Vgs solution with Vds=0.1V
- Id/Vds solution with Vgs=1.5V

The formation of this 3D structure is performed using the ATLAS syntax. The syntax used is very similar to that in the previous 2D example. The definition of dimensions in the third direction is defined by the **z** indicator. Thus, **z.min** and **z.max** define extents in the **z** direction, just as **x.min** and **x.max** do in the **x** direction.

The SOI device is composed of a 0.05 micron layer of silicon on a 0.45 micron silicon dioxide substrate. The device has a 12 nm thick gate oxide and a gate length of 0.8 microns (effective channel length is 0.5 microns). The gate width is 2.5um. The body contact location is defined by the following statement

```
elec num=4 x.min=2.8 x.max=3.6 y.min=-0.012 y.max=0.00 z.min=3.5 z.max=4
```

After the device description the **model** statement is used to select a set of physical models for this simulation. In this case, these models are ‘**consrh**’ and ‘**auger**’ recombination, the **conmob** and **fld-mob** mobility models, Band Gap Narrowing. The **impact** statement is used to specify Selberherr model. The **contact** statement is used to assign the work function on the polysilicon gate.

The numerical methods used are also similar to the previous example: METHOD **gummel** **newton** **carr=2**. This means that if convergence is not reached in decoupled mode (**gummel**) the simulator will automatically switch to coupled mode (**newton**). In addition a two carrier solution is performed by solving Poisson’s equation for potential and the electron and hole continuity equations.

The drain voltage is set to 0.1V, and then the gate voltage is swept to 1.5V to measure the Ids/Vgs curve.

Then the gate voltage is set to 1.5V, and then the drain voltage is swept to 3V. At this point faster solutions are obtained using the coupled newton algorithm so the simulation switches to this method. The drain voltage is then ramped to 4V.

The IV results are displayed using TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

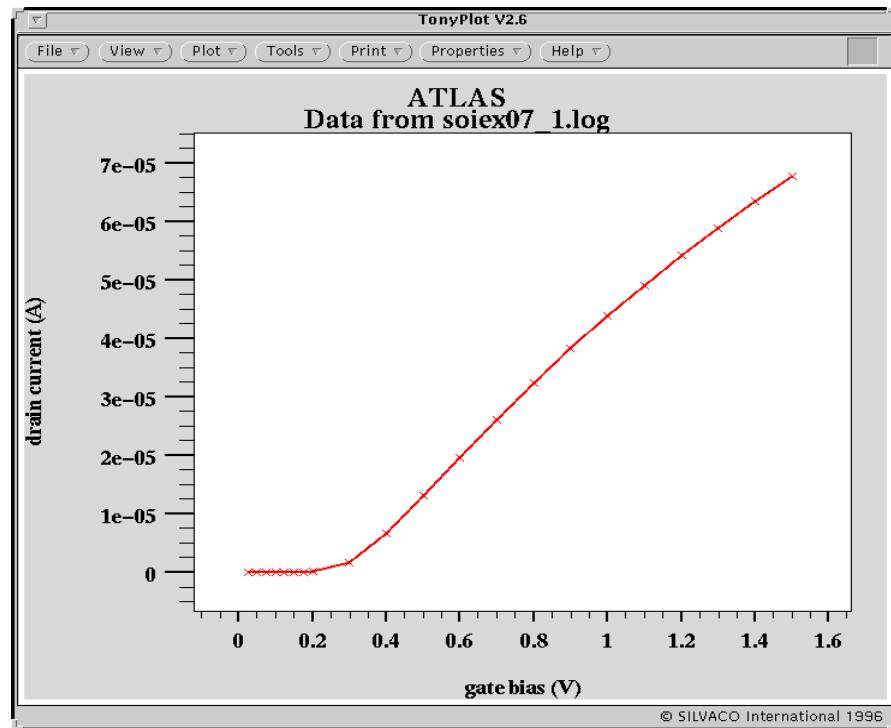


Figure 5.15: Id/Vgs for 3D SOI device, including width effect.

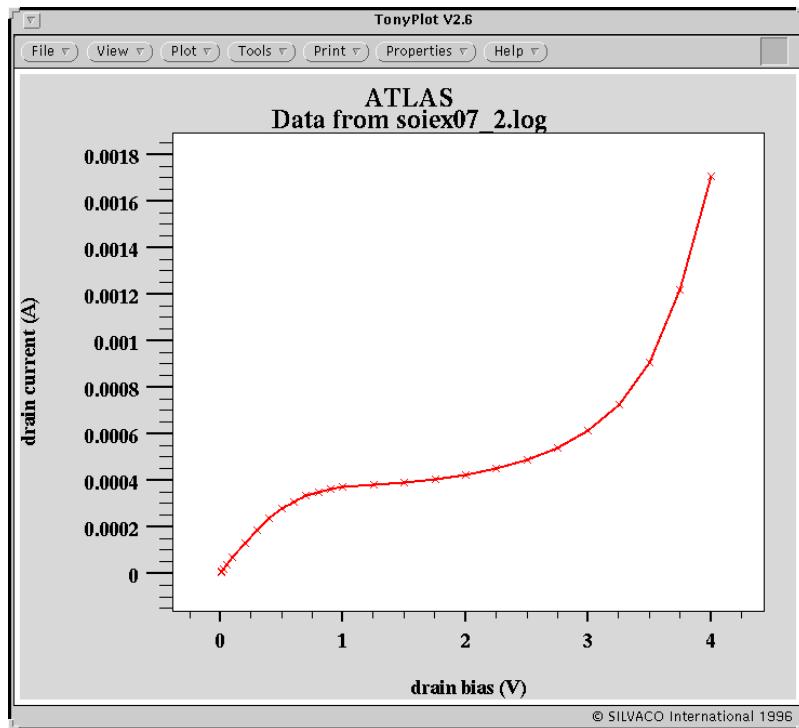


Figure 5.16: Id/Vds curve for PD-SOI with body contact. The expected kink is eliminated due to current flow to the body contact

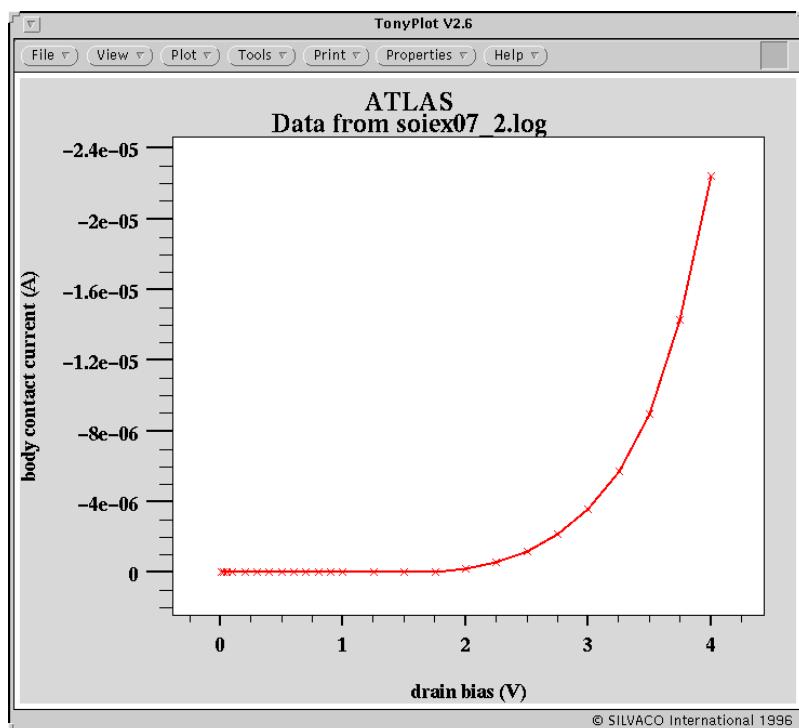


Figure 5.17: Current through body contact during Id/Vds sweep

Input File soi/soiex07.in:

```
1 go atlas
2
3 # SILVACO International 1994
4
5 # Id-Vg and Id-Vd simulation of 3D SOI Transistor with body electrode
6
7 mesh three.d rect nx=30 ny=21 nz=16 outf=soi.str
8
9
10 x.m      n=1      l=0.00      r=1.00
11 x.m      n=4      l=2.0       r=1.00
12 x.m      n=7      l=2.8       r=1.00
13 x.m      n=11     l=3.0       r=1.0
14 x.m      n=15     l=3.25      r=1.0
15 x.m      n=20     l=3.50      r=1.0
16 x.m      n=24     l=3.70      r=1.0
17 x.m      n=27     l=4.5       r=1.0
18 x.m      n=30     l=6.5       r=1.0
19
20 y.m      n=1      l=-0.022    r=1.00
21 y.m      n=2      l=-0.012    r=1.00
22 y.m      n=4      l=0.0000    r=1.00
23 y.m      n=8      l=0.005     r=1.0
24 y.m      n=17     l=0.05      r=1.02
25 y.m      n=21     l=0.5       r=1.25
26
27 z.m      n=1      l=0         r=1.00
28 z.m      n=4      l=1         r=1.00
29 z.m      n=8      l=2         r=0.95
30 z.m      n=11     l=2.5       r=1.05
31 z.m      n=13     l=3.5       r=1.0
32 z.m      n=16     l=4         r=1.0
33
34
35 region   num=1 material=SiO2 x.min=0 x.max=6.5 y.min=-0.022 y.max=0.0
           z.min=0 z.max=4
36 region   num=2 material=Silicon y.min=0. y.max=0.05 x.min=0. x.max=6.5
           z.min=0 z.max=4
37 region   num=3 material=SiO2 y.min=0.05 y.max=0.5 x.min=0. x.max=6.5
           z.min=0 z.max=4
38
39 # Electrodes #1 source, #2 gate, #3 drain, #4 substrate (Body electrode)
40
```

```
41 elec      num=1      x.min=0.0 x.max=2.0 y.min=-0.012 y.max=0.00 z.min=0
      z.max=1
42 elec      num=2      x.min=2.8 x.max=3.6 y.min=-0.022 y.max=-0.012 z.min=0
      z.max=2.5
43 elec      num=3      x.min=4.5 x.max=6.5 y.min=-0.012 y.max=0.00 z.min=0
      z.max=1
44
45 # Body electrode
46 elec      num=4      x.min=2.8 x.max=3.6 y.min=-0.012 y.max=0.00 z.min=3.5
      z.max=4
47
48
49 doping    uniform p.type conc=1.5e17
50 doping    uniform n.type conc=5.e19 x.left=0. x.right=3.0 y.top=0.0
      y.bottom=0.05 z.min=0 z.max=2
51 doping    uniform n.type conc=5.e19 x.left=3.5 x.right=6.5 y.top=0.0
      y.bottom=0.05 z.min=0 z.max=2
52 doping    uniform p.type conc=5.e19 x.left=2.8 x.right=3.6 y.top=0.0
      y.bottom=0.05 z.min=3.5 z.max=4
53
54 save outf=soiex07_0.str
55
56
57 contact   number=2 n.polysilicon
58
59 models    conmob bgn fldmob consrh auger print
60
61 impact    selb
62
63 # Id-Vg calculations
64
65 solve init
66 #ramp the drain to 0.1V
67
68 method gummel newton maxtrap=6 trap
69 solve v3=0.025
70 solve v3=0.05
71 solve v3=0.1
72
73 #ramp the gate and store the results
74
75 log outf=soiex07_1.log
76
77 solve v2=0.025 vstep=0.025 vfinal=0.2 electr=2
78 solve v2=0.3 vstep=0.1 vfinal=1.5 electr=2
```

```
79
80 tonyplot soiex07_1.log -set soiex07_1.set
81
82
83
84
85 # Id-Vd calculations
86
87 #ramp the gate to 1.5V
88
89 log off
90 solve init
91
92 method gummel newton maxtrap=6 trap
93
94 solve v2=0.5
95 solve v2=1
96 solve v2=1.5
97
98 #ramp the drain and store the results
99
100 log outf=soiex07_2.log master
101 solve v3=0.00625
102 solve v3=0.0125
103 solve v3=0.025
104 solve v3=0.05
105 solve v3=0.1 vstep=0.1 vfinal=1 electr=3
106 solve v3=1.25 vstep=0.25 vfinal=3 electr=3
107
108 method newton maxtrap=6 trap
109
110 solve v3=3.25 vstep=0.25 electr=3 vfinal=4
111
112 tonyplot soiex07_2.log -set soiex07_2.set
113 tonyplot soiex07_2.log -set soiex07_3.set
114
115
116 quit
```

5.1.8. soiex08.in: Modeling for Deep Submicron - Process to Device

Requires: SSUPREM4/S-PISCES/GIGA

This example uses process simulation to construct a SOI MOSFET that has full dielectric isolation. Device simulations are then performed that use Non-isothermal Energy Balance (NEB) calculations to obtain Ids/Vds characteristics. It shows:

- SOI structure formation using SSUPREM4 process simulation
- partially depleted SOI design
- selection of energy balance and lattice heating models in ATLAS
- selection of numerical methods for coupled solution technique
- Id/Vds simulation for Vgs=1.0, 3.0 and 5.0 V

A silicon-oxide-silicon structure was formed in SSUPREM4 by use of the `region` statement of ATHENA. This structure was then subjected to a standard bulk MOSFET processing sequence, which has been described in `mos1ex01.in`. The structure in this example has been designed so that the SOI thickness is greater than the depth of the source and drain junctions. This ensures that the device will operate in a partially depleted mode of operation during later device simulations.

One major modification made to the original processing sequence was to introduce a LOCOS isolation step. The result of this step was the creation of a fully oxide isolated island of silicon. The `compress` model for oxidation has been used in this example but more complex and accurate models may be used to study birds beak effects in SOI MOSFETs, as described in the ATHENA/SSUPREM4 section.

Using DECKBUILD's auto-interface the process simulation structure will be passed into ATLAS automatically. This auto-interface therefore allows global optimization from process simulation to device simulation to spice model parameter extraction.

In ATLAS the `contact` statement is used to define the workfunction of the gate electrode. The `interface` command is used to define the fixed charge at the oxide/silicon interfaces. The `models` statement defines a set of physical models for the simulation. CVT and SRH are standard models for MOSFET simulation. The energy balance equation for electrons is specified by `hcte.el` parameter and the lattice heat flow equation is solved with GIGA by setting the parameter `lat.temp`. A thermal contact must also be defined when solving the heat flow equation with GIGA and is defined using the `thermcontact` statement. In this example this thermal electrode is defined to be the same as contact number #4 which is the substrate electrode.

The numerical algorithm chosen for this system of equations is the newton approach defined on the `method` statement. This statement is also used to define the semiconductor equations. `carr=2` will solve for potential and the hole and electron continuity equations. The `trap` parameter allows the bias step to be reduced in cases of non-convergence for a total of `maxtrap` times.

The solution begins by applying zero volts to all contacts and only solving for potential. Then a small voltage is applied to the drain contact. This is normally advised in the case of SOI simulations due to the presence of a floating region of potential. As described in previous SOI examples this floating region of potential can cause great numerical difficulties. However, by solving for five equations, which couples the equations very tightly and applying only small voltage steps, the convergence in this example is excellent.

The gate voltage is ramped to 1, 2 and 3 V and a solution saved at each of these bias conditions. Each solution is then used as the initial starting point for simulating the Ids/Vds characteristics by using the `load` command. A log file is then opened to store the terminal characteristics and a `solve` statement applies the drain bias sweep. This procedure is then repeated for each gate voltage.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

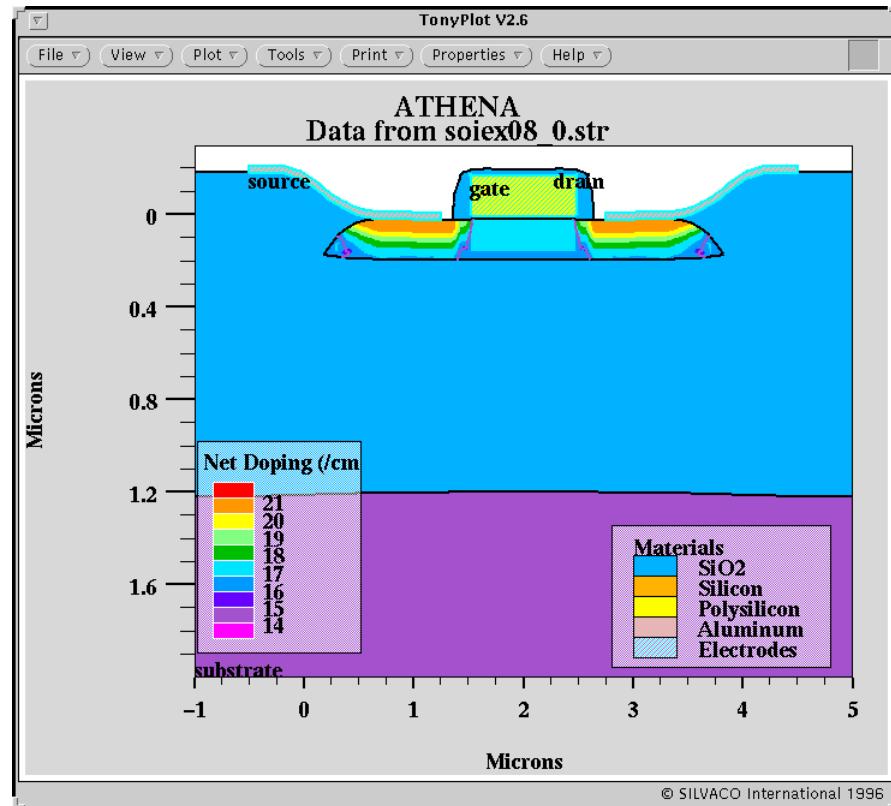


Figure 5.18: Sub-micron SOI structure and doping defined in ATHENA. Film isolation using LOCOS is also simulated

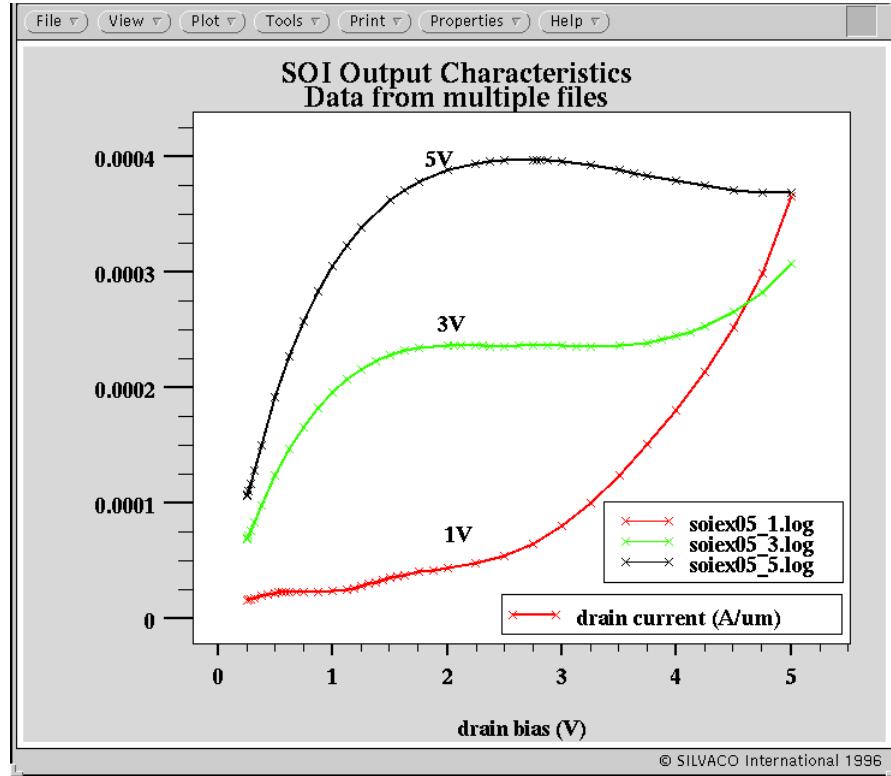


Figure 5.19: I_d/V_{ds} curve from the processed device. Kink and strong avalanche are seen at low V_{gs} . At higher V_{gs} lattice heating suppresses these effects

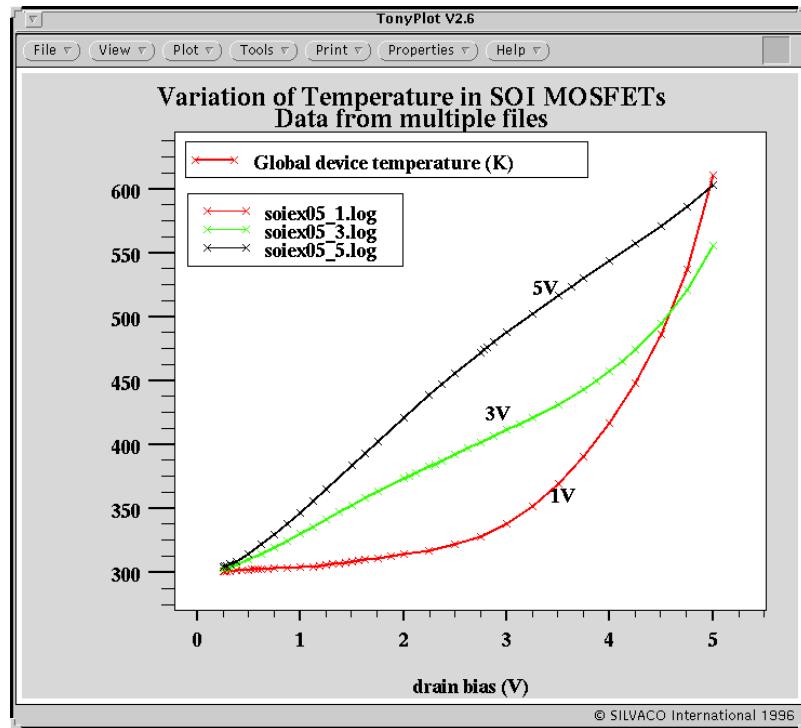
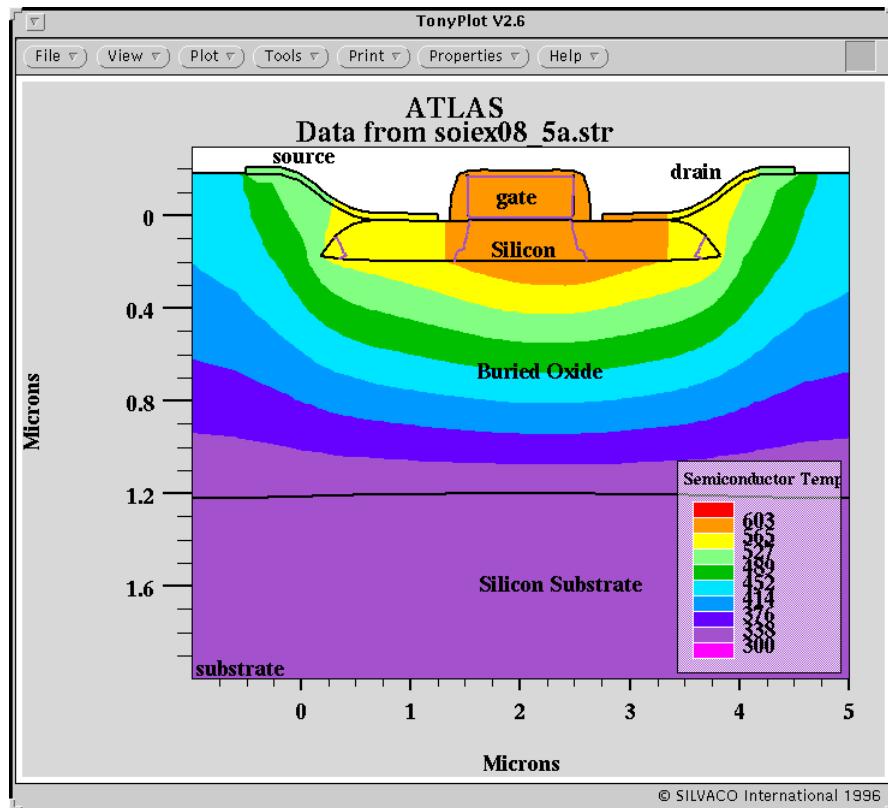
Figure 5.20: Peak Temperature in the SOI film during I_d/V_{ds} simulations

Figure 5.21: Temperature distribution in the SOI transistor and surrounding oxide

Input File soi/soiex08.in:

```
1 go athena
2
3 #TITLE: SOI Process and Device Simulation Example
4
5 # Substrate mesh definition
6 line y loc=0      spac=0.02    tag=top
7 line y loc=0.13   spac=0.01
8 line y loc=0.2    spac=0.02    tag=oxtop
9 line y loc=0.7    spac=0.5
10 line y loc=1.2   spac=0.1     tag=oxbot
11 line y loc=2     spac=0.5     tag=bot
12
13 line x loc=-1   spac=0.5     tag=left
14 line x loc=0     spac=0.1
15 line x loc=1.55  spac=0.01
16 line x loc=2     spac=0.25    tag=right
17 #
18 region silicon xlo=left xhi=right ylo=top yhi=oxtop
19 region oxide xlo=left xhi=right ylo=oxtop yhi=oxbot
20 region silicon xlo=left xhi=right ylo=oxbot yhi=bot
21 #
22 init orient=100 c.phos=1e14 space.mult=1.5
23 #
24 # pad oxide and nitride mask
25 deposit oxide thick=0.02
26 deposit nitride thick=0.1
27 #
28 # from now on the situation is 2-D
29 #
30 etch    nitride left p1.x=0
31 etch    oxide    left p1.x=0
32 #
33 # field oxidation
34 #
35 method compress fermi
36 diffus time=90 temp=1000 weto2 press=1.00 hcl.pc=0
37 #
38 etch nitride all
39 #
40 etch oxide start x=1 y=-1
41 etch continue x=3 y=-1
42 etch continue x=3 y=0.1
```

```
43 etch done x=1 y=0.1
44 #
45 # pwell formation including masking off of the nwell
46 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
47 #
48 etch oxide thick=0.02
49 #
50 # P-well Implant
51 implant boron dose=8e12 energy=100 pears
52
53 # N-well implant not shown -
54 #
55 # welldrive starts here
56 diffus time=220 temp=1200 nitro press=1
57 #
58 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
59 #
60 etch oxide thickness=0.03
61 #
62 # gate oxide grown here:-
63 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
64
65 # extract a design parameter.....
66
67 extract name="gateox" thickness oxide mat.occno=1 x.val=2.0
68 #
69 # vt adjust implant
70 implant boron dose=9.5e11 energy=10 pearson
71 #
72 # polysilicon gate formation
73 depo poly thick=0.2 divi=2 c.phosphor=2e20
74 #
75 etch poly left p1.x=1.5
76 #
77 # oxidise polysilicon
78 method fermi compress
79 diffuse time=3 temp=900 weto2 press=1.0
80 #
81 # N- LDD implant
82 implant phosphor dose=3.0e13 energy=20 pearson
83 #
84 # create sidewalls
85 depo oxide thick=0.120 divisions=8
```

```
86 #
87 etch oxide dry thick=0.120
88 #
89 # S/D implant
90 implant arsenic dose=5.0e15 energy=50 pearson
91 #
92 method fermi compress
93 diffuse time=2 temp=900 nitro press=1.0
94 #
95 etch oxide thickness=0.02
96 #
97 # metal deposition and patterning for S/G/D
98 deposit alumin thick=0.03 divi=2
99 #
100 struct mirror right
101 #
102 etch alumin right p1.x=4.5
103 etch alumin left p1.x=-0.5
104 #
105 etch alumin start x=1.25 y=-1
106 etch continue x=2.75 y=-1
107 etch continue x=2.75 y=0.1
108 etch done x=1.25 y=0.1
109 #
110 # electrode definition
111 electrode name=gate x=2.0 y=-0.1
112 electrode name=source x=0.0
113 electrode name=drain x=4.0
114 electrode name=substrate backside
115 #
116 # Save Final Structure
117 structure outfile=soiex08_0.str
118 #
119 tonyplot soiex08_0.str -set soiex08_0.set
120 #
121 go atlas
122 #
123 #
124 # define the Gate workfunction....
125 contact name=gate n.poly
126
127 # Define the Gate Qss
128 interface qf=3e10
```

```
129
130 # Use the cvt mobility model for MOS....
131 models cvt srh hcte.el lat.temp
132
133 impact selb
134
135 thermcontact num=1 elec.num=4 ext.temp=300
136
137 # initial solution to get it started.....
138 method newton trap autonr maxtrap=10
139
140 solve init
141 #
142 output e.field j.electron j.hole j.conduc j.total ex.field ey.field \
143     flowlines e.mobility h.mobility qss e.temp h.temp val.band con.band \
\ 
144     qfn qfp j.disp photogen impact
145
146 # apply a small initial drain bias
147 solve vfinal=0.25 vstep=0.05 name=drain
148
149 # solve for Vg=1,3,5V
150 solve vfinal=1 vstep=0.25 name=gate
151 save outf=soiex08_1.str
152
153 solve vfinal=3 vstep=0.25 name=gate
154 save outf=soiex08_3.str
155
156 solve vfinal=5 vstep=0.25 name=gate
157 save outf=soiex08_5.str
158
159 # obtain Id-Vd curve for Vg=1V
160 load infile=soiex08_1.str master
161 solve prev
162 log outf=soiex08_1.log
163 solve vfinal=5 vstep=0.25 name=drain
164 save outf=soiex08_1a.str
165
166 log outf=tmp
167
168 # obtain Id-Vd curve for Vg=3V
169 load infile=so iex08_3.str master
170 solve prev
```

```
171 log outf=soiex08_3.log
172 solve vfinal=5 vstep=0.25 name=drain
173 save outf=soiex08_3a.str
174
175 log outf=tmp
176
177 # obtain Id-Vd curve for Vg=5V
178 load infile=soiex08_5.str master
179 solve prev
180 log outf=soiex08_5.log
181 solve vfinal=5 vstep=0.25 name=drain
182 save outf=soiex08_5a.str
183
184 tonyplot -overlay soiex08_1.log soiex08_3.log soiex08_5.log -set
    soiex08_1.set
185 tonyplot -overlay soiex08_1.log soiex08_3.log soiex08_5.log -set
    soiex08_2.set
186 tonyplot soiex08_5a.str -set soiex08_5a.sel*t
187
188 quit
```

5.1.9. soiex09.in : 3D Device Simulation - Effect of Lattice Heating

Requires: DEVICE3D/GIGA3D

This example demonstrates an Id/Vds 3D analysis of a short channel ultra-thin SOI transistor with a body contact. Two simulations are performed with and without lattice heating turned on.

Such simulations cannot be performed accurately using a 2D simulator because the body electrode is located in a different z-plane compared with the drain, gate and source. The example shows:

formation of 3D structure using ATLAS syntax

Id/Vds solution with Vgs=3.0V

The formation of this 3D structure is performed using the ATLAS syntax. The syntax used is very similar to that of a 2D example. The definition of dimensions in the third direction is defined by the z indicator. Thus z.min and z.max define extents in the z direction, just as x.min and x.max do in the x direction.

The SOI device is composed of a 0.2 micron layer of silicon on a 0.4 micron silicon dioxide substrate. The device has a 17 nm thick gate oxide and a gate length of 1.0 microns (effective channel length is 0.8 microns). The gate width is 2.5um. The body contact location is defined by the following statement:

```
electrode      name=body      x.min=1 x.max=2 y.min=0.0 y.max=0.0 z.min=3.5
               z.max=4
```

After the device description the model statement is used to select a set of physical models for this simulation. In this case the example uses commob: the doping dependent low field mobility model, fldmob: the lateral electric field-dependent mobility model, srh: Shockley-Read-Hall recombination, auger: recombination accounting for high level injection effects, and bgn: band gap narrowing.

Also, in the lattice heating simulation input file, an additional parameter, lat.temp, is placed on the model statement. This switches on lattice heating inside the simulation. With this option it is

also necessary to include a thermal boundary condition. This is included using the following statement:

```
thermcontact num=1 ext.temp=300 x.min=0 x.max=3 y.min=0.35 z.min=0
z.max=4,
```

and forces the temperature on the bottom of the device to be fixed at 300K.

The `impact` statement is used to specify Selberherr model. The `contact` statement is used to assign the work function on the polysilicon gate.

The numerical methods used are different to previous 2D examples and are chosen by the statement method `bicgst`. This chooses a bi-conjugate gradient solution scheme which has been found to give robust and fast simulations of three dimensional devices.

The drain voltage is set to 0.1V, and then the gate voltage is swept to 3.0V to obtain the operating gate voltage.

Then the gate voltage is set to 3.0V, and then the drain voltage is swept to its final value.

The IV results are displayed using TONYPLOT showing the ID-VG characteristics both with and without lattice heating.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

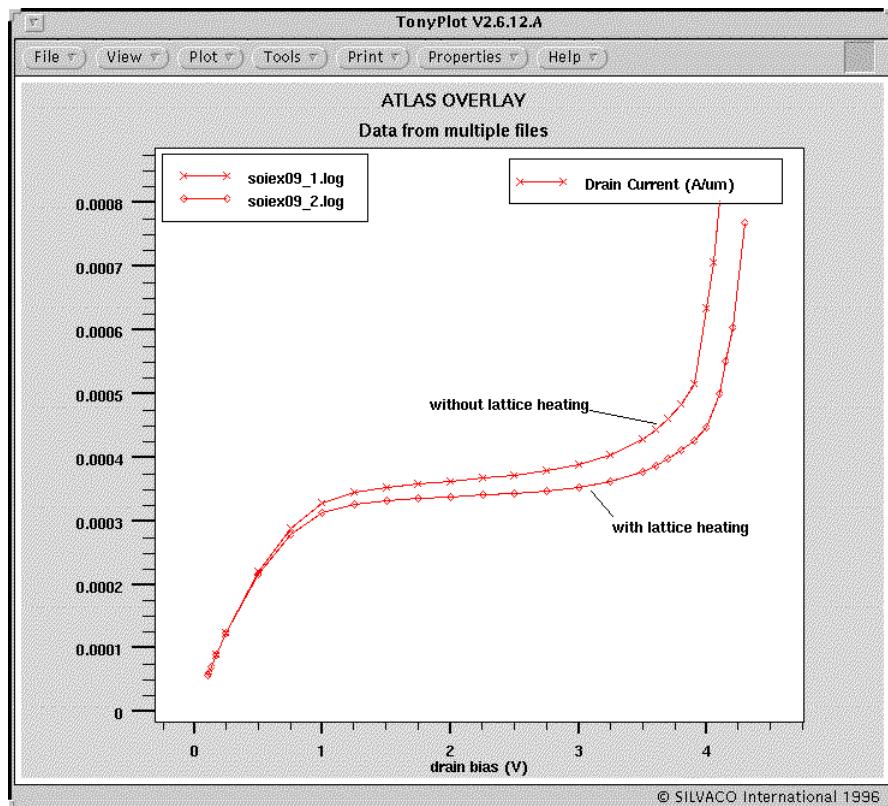


Figure 5.22: Comparison of the forward ID-VD characteristics for VG=1.5V with and without lattice heating in a 3D SOI MOSFET

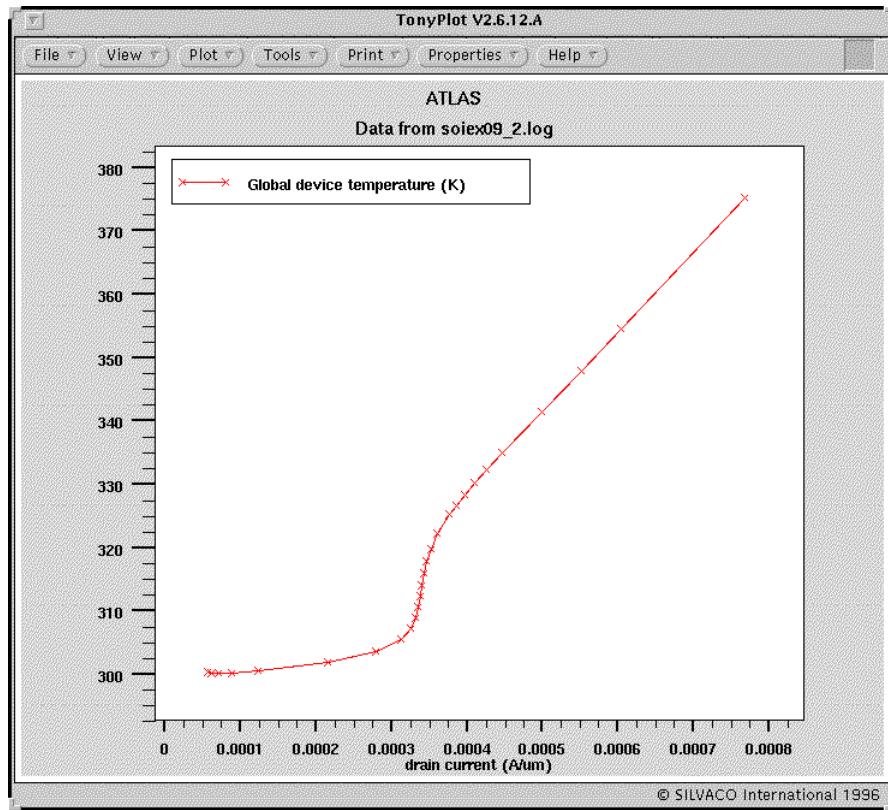


Figure 5.23: Maximum Lattice Temperature versus drain current in the 3D SOI MOSFET

Input Deck soi/soiex09.in :

```

1 go atlas
2 #
3 TITLE SOI device simulation WITHOUT lattice heating
4 #
5 # SILVACO International 1992, 1993, 1994, 1995, 1996, 1997
6 #
7 # 0.2um of silicon on 0.4um oxide substrate
8 #
9 mesh three.d space.mult=1.0
10 #
11 x.mesh loc=0.00    spac=0.25
12 x.mesh loc=0.5     spac=0.25
13 x.mesh loc=1.00    spac=0.02
14 x.mesh loc=1.15    spac=0.02
15 x.mesh loc=1.5     spac=0.2
16 x.mesh loc=1.85    spac=0.02
17 x.mesh loc=2.00    spac=0.02
18 x.mesh loc=2.50    spac=0.25

```

```

19 x.mesh loc=3      spac=0.25
20 #
21 y.mesh loc=-0.017 spac=0.02
22 y.mesh loc=0.00    spac=0.0075
23 y.mesh loc=0.1     spac=0.025
24 y.mesh loc=0.2     spac=0.015
25 y.mesh loc=0.6     spac=0.25
26 #
27 z.mesh loc=0 spac=0.5
28 z.mesh loc=1 spac=0.5
29 z.mesh loc=2 spac=0.5
30 z.mesh loc=2.5 spac=0.1
31 z.mesh loc=3.5 spac=0.25
32 z.mesh loc=4 spac=0.1
33
34 region      num=1 y.max=0  z.min=0 z.max=4 oxide
35 region      num=2 y.min=0 y.max=0.2 z.min=0 z.max=4 silicon
36 region      num=3 y.min=0.2  z.min=0 z.max=4 oxide
37 #
38 ***** define the electrodes *****
39 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
40 #
41 electrode    name=gate      x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
        z.min=0 z.max=2.5
42 electrode    name=source    x.max=0.5 y.min=0 y.max=0 z.min=0 z.max=1
43 electrode    name=drain     x.min=2.5 y.min=0 y.max=0 z.min=0 z.max=1
44 electrode    substrate
45 electrode    name=body      x.min=1 x.max=2 y.min=0.0 y.max=0.0 z.min=3.5
        z.max=4
46 #
47 ***** define the doping concentrations *****
48 #
49 doping       uniform conc=2e17 p.type  reg=2
50 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
        z.min=0 z.max=2
51 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
        z.min=0 z.max=2
52 doping       uniform p.type conc=5.e19 x.left=1 x.right=2 y.top=0.0 y.bot-
        tom=0.2 z.min=3.5 z.max=4
53 #
54 save        outf=soiex09_0.str
55 #
56 # set interface charge separately on front and back oxide interfaces
57 interf      qf=3e10 y.max=0.1

```

```
58 interf      qf=lell y.min=0.1
59 #
60 # set workfunction of gate
61 contact      name=gate n.poly
62 #
63 # select models
64 models       conmob srh auger bgn fldmob print
65 #
66 impact selb
67 #
68 # do IDVG characteristic
69 #
70 method       bicgst   trap
71 #
72 solve init
73 solve prev
74 solve vdrain=0.005
75 solve vdrain=0.025 vfinal=0.1 vstep=0.025 name=drain
76 #
77 # Ramp up gate voltage
78 solve vgat=0.2 vfinal=3 vstep=0.2 name=gate
79 #
80 # Perform ID-VG sweep
81 log outf=soiex09_1.log
82 solve vdrain=0.25 vfinal=3.5 vstep=0.25 name=drain
83 solve vdrain=3.6 vfinal=4.1 vstep=0.1 name=drain
84 #
85 save        outf=soiex09_1.str
86 #
87 go atlas
88 #
89 TITLE SOI device simulation WITH lattice heating
90 #
91 # SILVACO International 1992, 1993, 1994, 1995, 1996, 1997
92 #
93 # 0.2um of silicon on 0.4um oxide substrate
94 #
95 mesh three.d space.mult=1.0
96 #
97 x.mesh loc=0.00    spac=0.25
98 x.mesh loc=0.5     spac=0.25
99 x.mesh loc=1.00    spac=0.04
100 x.mesh loc=1.15   spac=0.04
```

```

101 x.mesh loc=1.5      spac=0.1
102 x.mesh loc=1.85     spac=0.02
103 x.mesh loc=2.00     spac=0.02
104 x.mesh loc=2.50     spac=0.25
105 x.mesh loc=3        spac=0.25
106 #
107 y.mesh loc=-0.017   spac=0.02
108 y.mesh loc=0.00     spac=0.0075
109 y.mesh loc=0.1       spac=0.025
110 y.mesh loc=0.2       spac=0.015
111 y.mesh loc=0.4       spac=0.25
112 y.mesh loc=0.5       spac=0.25
113 y.mesh loc=0.6       spac=0.25
114 #
115 z.mesh loc=0 spac=0.5
116 z.mesh loc=1 spac=0.5
117 z.mesh loc=2 spac=0.5
118 z.mesh loc=2.5 spac=0.1
119 z.mesh loc=3.5 spac=0.25
120 z.mesh loc=4 spac=0.1
121 #
122 region      num=1 y.max=0  z.min=0 z.max=4 oxide
123 region      num=2 y.min=0 y.max=0.2 z.min=0 z.max=4 silicon
124 region      num=3 y.min=0.2  z.min=0 z.max=4 oxide
125 #
126 ***** define the electrodes *****
127 # #1-GATE #2-SOURCE #3-DRAIN #4-SUBSTRATE(below oxide)
128 #
129 electrode    name=gate    x.min=1 x.max=2 y.min=-0.017 y.max=-0.017
           z.min=0 z.max=2.5
130 electrode    name=source   x.max=0.5 y.min=0 y.max=0 z.min=0 z.max=1
131 electrode    name=drain    x.min=2.5 y.min=0 y.max=0 z.min=0 z.max=1
132 electrode    substrate
133 electrode    name=body    x.min=1 x.max=2 y.min=0.0 y.max=0.0 z.min=3.5
           z.max=4
134 #
135 ***** define the doping concentrations *****
136 #
137 doping       uniform conc=2e17 p.type  reg=2
138 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.r=1.0
           z.min=0 z.max=2
139 doping       gauss n.type conc=1e20 char=0.2 lat.char=0.05 reg=2 x.l=2.0
           z.min=0 z.max=2

```

```
140 doping      uniform p.type conc=5.e19 x.left=1 x.right=2 y.top=0.0 y.bot-
    tom=0.2 z.min=3.5 z.max=4
141 #
142 # set interface charge separately on front and back oxide interfaces
143 interf      qf=3e10 y.max=0.1
144 interf      qf=1e11 y.min=0.1
145 #
146 # set workfunction of gate
147 contact     name=gate n.poly
148 #
149 # select models
150 models      conmob srh auger bgn fldmob lat.temp print
151 #
152 thermcontact num=1 ext.temp=300 x.min=0 x.max=3 y.min=0.35 z.min=0
    z.max=4
153 #
154 impact selb
155 #
156 # do IDVG characteristic
157 #
158 method      bicgst   trap
159 #
160 solve init
161 solve prev
162 solve vdrain=0.005
163 solve vdrain=0.025 vfinal=0.1 vstep=0.025 name=drain
164 #
165 # Ramp up gate voltage
166 #
167 solve vgate=0.2 vfinal=3 vstep=0.2 name=gate
168 #
169 # Perform ID-VG sweep
170 #
171 log outf=soiex09_2.log
172 solve vdrain=0.25 vfinal=3.5 vstep=0.25 name=drain
173 solve vdrain=3.6 vfinal=4.3 vstep=0.1 name=drain
174 #
175 save       outf=soiex09_2.str
176 #
177 tonyplot -overlay soiex09_1.log soiex09_2.log -set soiex09_1.set
178 tonyplot soiex09_2.log -set soiex09_2.set
179 #
180 quit
```

6.1. EPROM: Application Examples

6.1.1. eprmex01.in: Flash EEPROM Programming and Erasing

Requires: SSUPREM4/DEVEDIT/S-PISCES

The example file supplied simulates the structure definition and electrical test of a FLASH EEPROM cell. The example consists of :

- dual gate EEPROM structure formation in ATHENA
- re-meshing in DEVEDIT
- threshold voltage simulation before programming
- transient programming simulation
- threshold voltage simulation after programming
- transient erasure simulation

For accurate simulation of programming and erasure it is vital to have a very accurate representation of the device structure. The gate and tunneling currents are very sensitive to geometry and doping profiles. It will be possible for you to alter process parameters and observe their effect on device performance directly with this input file.

The interface between ATHENA and ATLAS is automatic. The electrode statements in ATHENA are used to define the electrode positions for ATLAS. Any metal or polysilicon layer can optionally be set as an electrode region. The electrode names given in ATHENA are transferred into ATLAS.

As with many of the examples provided the grid structure for the example EEPROM device is rather coarse. This allows a realistic execution times for the example. When comparing simulated and real EEPROM devices a finer grid is recommended. This can be done quickly by decreasing the space .mult parameter of the initialize statement.

To obtain a finer grid DEVEDIT is used. This can effectively refine the grid for the electrical simulation. A finer mesh for resolving the dopant distribution is still recommended though.

The ATLAS programming simulation consists of 3 basic parts. First, a threshold voltage simulation is done to obtain the EEPROM cell threshold in it's unprogrammed state. Then the device is biased into the initial condition of the transient with the high programming control gate voltage. Here 12V is used.

Next the programming transient is done. Since the times involved in programming are much greater than the relaxation time of the device, the syntax {bold} method quasi can be used to specify the quasistatic method. This results in a large improvement in the speed of calculation.

The programming consists of two solve statements. The first ramps the drain to 5.0V in 1ns. At this point a solution file is saved. This can be used to examine the potentials before charge is applied to the floating gate. The second line gives no change in the applied voltages. It simply leaves the device biased in the condition VCG=12.0V and Vds=5.0V. During this time the hot electron injection model will predict values of gate current. This current, coupled with the transient time step size, is used to add charge self-consistently to the floating gate. At the end of the transient a solution file is saved.

Comparisons of device internal distributions, such as potentials can be done by comparing the two solution files from before programming and after the programming.

The final part of this run consists of a copy of the first part. A threshold voltage test is run on the EEPROM cell. In this case however the device is programmed and a large threshold voltage shift is seen.

The graphics output of this section show plots of threshold voltage before and after programming. A plot of floating gate charge vs. time can be obtained from result of the transient simulation. Also the actual programming gate current can be seen falling off with time. This is because the increasing charge on the floating gate increases the threshold voltage of the device. This in turn reduces the drain current which will cause a drop in hot carrier density and hence a reduction in programming current.

It is possible to plot showing the floating gate charge charge vs. time curve. This can be quickly converted to threshold voltage shift using the following formula:

$$\text{Threshold Shift} = Q_{\text{Tox}} / L_{\text{Eox}}$$

Where

Q = floating gate charge per unit width

Tox = inter-poly oxide thickness

L = length of floating gate

Eox = absolute permittivity of oxide

In this case Tox is converted into an effective Tox based on the thickness of each layer of the inter-poly ONO di-electric. This is done by:

$$\text{Effective Tox} = E_{\text{oxide}} * (T_{\text{oxide}}/\text{Eox1} + T_{\text{nitride}}/\text{Eox2} + T_{\text{oxide}}/\text{Eox2})$$

where T_x is thickness of x and E_x is relative permittivity of x.

The final run of this example is a transient erasure simulation. ATLAS is restarted using the command `go atlas`. The correct set of erasing models for EEPROMs is chosen. The key models are `fnord` and `bbt.std`. `fnord` specifies the solution for Fowler Nordheim tunneling the main erasure mechanism for EEPROMs. `bbt.std` specifies the band to band tunneling model. This is required due to the high electric fields at the source/channel junction. Tunneling due to these fields leads to high substrate current during erasing.

After the models and other material parameters are set, the charge on the floating gate is ramped using the parameter `q1`. This 'q' works in an analogous manner to ramping voltages using 'v': `q1` and `qstep` are the equivalent in charge to `v1` and `vstep`. In EEPROM erasure the drain is disconnected to avoid large power consumption from source to drain breakdown currents. One way to disable a contact is to use current boundary conditions and force zero current. An alternative used here is to attach a very large resistor to the contact.

The transient erasure is performed in a single solve statement. The source electrode is ramped to 12.5V. The mechanism to remove charge from the floating gate is exactly analogous to programming. The only difference is the Fowler-Nordheim tunneling rather than hot electron injection as gate current. Obviously this will change the direction of the current through the gate oxide.

The resultant graphics show the transient erasing characteristic. To plot the threshold voltage shift the same calculation given in the programming section can be used.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

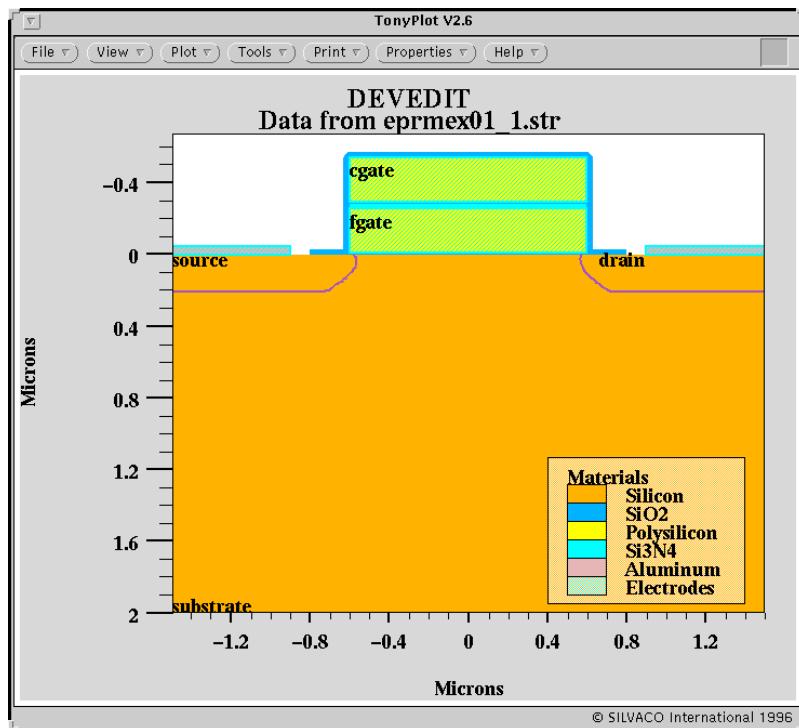


Figure 6.1: Flash Structure defined in ATHENA and remeshed in DevEdit

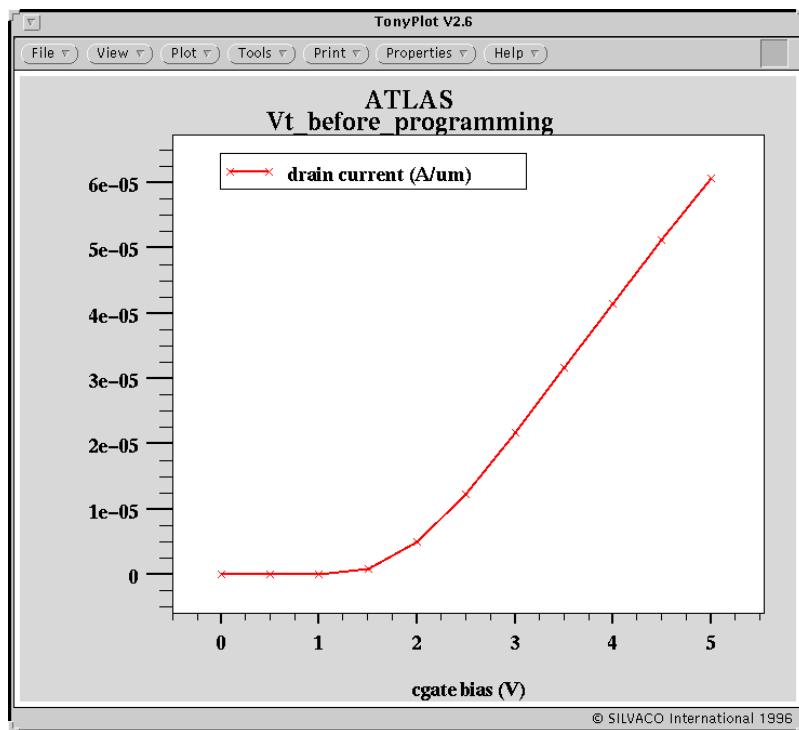


Figure 6.2: Threshold voltage Curve for EEPROM before programming

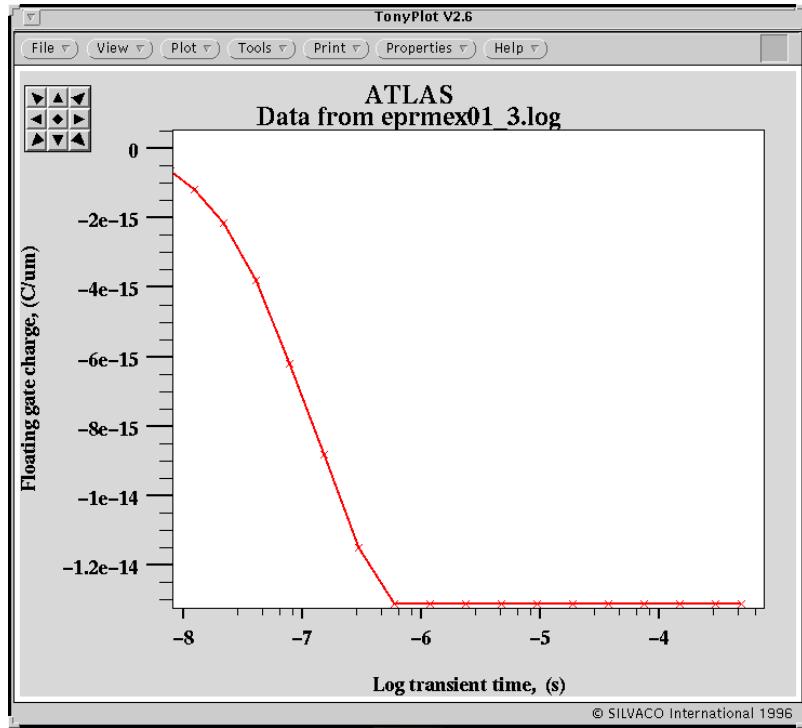


Figure 6.3: Charge on the floating gate versus time during a programming transient. Threshold voltage shift can also be plotted as a function in TonyPlot

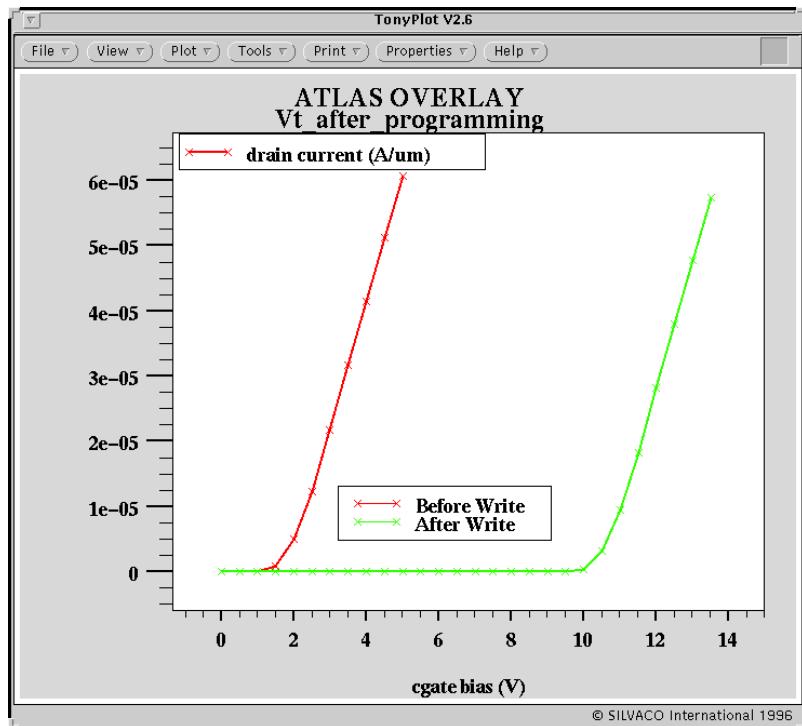


Figure 6.4: Comparison of Id/Vcg for the EEPROM before and after programming

Input File eprom/eprmex01.in:

```
1 go athena
2 #TITLE: EEPROM cell formation example
3 #
4
5 line x loc=0.0 spac=0.1
6 line x loc=0.6 spac=0.025
7 line x loc=0.9 spac=0.05
8 line x loc=1.5 spac=0.2
9 #
10 line y loc=0.00 spac=0.01
11 line y loc=0.3 spac=0.03
12 line y loc=2.0 spac=0.25
13
14 #
15 init c.boron=3e16 orientation=100 space.mult=1
16
17 #
18 method compress fermi
19 diffuse time=10 temp=950 dryo2
20 #
21 extract name="tunnelox" thickness oxide mat.occno=1 x.val=0
22 #
23 implant boron dose=1e12 energy=25
24 #
25 deposit poly thick=.25 div=4
26 #
27 implant phos dose=6e14 energy=30
28 #
29 diffuse time=5 temp=950 dryo2
30 #
31 deposit nitride th=.02
32 #
33 deposit oxide th=.01
34 #
35 deposit poly thick=.25 div=4 phos conc=8e19
36 #
37 etch poly right p1.x=.6
38 #
39 etch oxide right p1.x=.6
40 #
41 etch nitride right p1.x=.6
42 #
```

```
43 etch oxide right p1.x=.6
44 #
45 etch poly right p1.x=.6
46 #
47 etch oxide right p1.x=.6
48 #
49 relax y.min=.3 dir.y=f
50 #
51 implant arsenic dose=1e15 energy=40
52 #
53 diff time=50 temp=950
54 deposit oxide thick=.03 div=2
55
56
57
58 #
59 structure mirror left
60 #
61 etch oxide left p1.x=-0.8
62 etch oxide right p1.x=0.8
63
64 deposit alum th=.05
65 #
66 etch alum start x=0.9 y=-10.
67 etch alum cont x=0.9 y=10.
68 etch alum cont x=-.9 y=10.
69 etch alum done x=-.9 y=-10.
70 #
71 # define electrode names
72 electrode name=fgate x=0 y=-0.1
73 electrode name=cgate x=0 y=-0.4
74 electrode name=source x=-1.5
75 electrode name=drain x=1.5
76 electrode name=substrate backside
77 # save the structure
78 structure outfile=eprmex01_0.str
79
80
81 # Switch to DevEdit for remeshing...
82 go DevEdit
83
84 # Set Meshing Parameters
85 #
```

```
86 base.mesh height=0.4 width=0.4
87 #
88 # Make sure impurity gradiants have enough detail. (i.e. no triangle
89 # spans more than 1 (sensitivity=1) power of 10)
90 imp.refine imp="NetDoping" sensitivity=1
91 imp.refine min.spacing=0.02
92 #
93 # Make sure channel has enough triangles.
94 constr.mesh depth=0.25 under.material="PolySilicon" max.height=0.05 \
95     max.width=0.05
96 constr.mesh depth=0.05 under.material="PolySilicon" max.height=0.015
97 #
98 # Make sure contacts have enough connection points.
99 constr.mesh depth=0.05 under.material="Aluminum" max.width=0.1
100
101 # Create a mesh, using the parameters set above.
102 mesh mode=meshbuild
103
104 # save structure
105 struct outfile=eprmex01_1.str
106 tonyplot eprmex01_1.str -set eprmex01_1.set
107
108
109 # switch to Atlas for the Device Tests....
110
111 go atlas
112
113
114 # Set workfunction for the poly gates,
115
116 contact name=fgate n.polysilicon floating
117 contact name=cgate n.polysilicon
118
119 #Define some Qss...
120 interface qf=3e10
121 models srh cvt hei fnord print nearflg
122 impact selb
123
124 ##### This is the Vt Test before programming #####
125 #####
126 solve init
127
128
```

```
129 method newton trap maxtraps=8 autonr
130
131 log outf=eprmex01_2.log
132 solve vdrain=0.5
133 solve vstep=0.5 vfinal=25 name=cgate comp=5.5e-5 cname=drain
134 # plot idvg
135
136 tonyplot eprmex01_2.log -s eprmex01_2.set
137 # extract vt
138 extract name="initial vt" ((xintercept(maxs-
    lope(curve(v."cgate",i."drain"))))-abs(ave(v."drain")))/2.0)
139
140 ##### This is the Programming/Writing Transient #####
141 #####
142
143 # use zero carriers to get vg=12v solution
144 models srh cvt hei fnord print nearflg
145 method carriers=0
146 log off
147 solve init
148 solve vcgate=3
149 solve vcgate=6
150 solve vcgate=12
151 # now use 2 carriers
152
153 models srh cvt hei fnord print nearflg
154 impact selb
155
156 method newton trap maxtraps=8 quasi carriers=2
157 solve prev
158
159 log    outf=eprmex01_3.log master
160 # ramp up drain voltage
161 solve vdrain=5.85 ramptime=1e-9 tstep=1e-10 tfinal=1e-9 proj
162 # keep voltages constant and perform transient programming
163 solve tstep=1e-9 tfinal=5.e-4
164 # plot programming curve
165 tonyplot eprmex01_3.log -set eprmex01_3.set
166
167 ##### This is the Vt Test After Programming #####
168 #####
169
170 method newton trap maxtraps=8 autonr
```

```
171
172 log outf=eprmex01_4.log master
173 solve init
174 solve vdrain=0.5
175 solve vstep=0.5 vfinal=25 name=cgate comp=5.5e-5 cname=drain
176 # plot new idvg overlaid on old one
177 tonyplot -overlay eprmex01_2.log eprmex01_4.log -set eprmex01_4.set
178 # extract vt and vt shift
179 extract name="final vt" ((xintercept(maxs-
    lope(curve(v."cgate",i."drain"))))-abs(ave(v."drain")))/2.0)
180 extract name="vt shift" ("final vt" - "initial vt")
181
182 ##### This is the Erasing Test #####
183 #####
184
185 go atlas
186
187 # select erasing models
188
189 models cvt srh fnord bbt.std print nearflg
190 impact selb
191
192
193 contact name=fgate n.poly floating
194 contact name=cgate n.poly
195 interface qf=3e10
196
197 method carr=2
198 # get initial zero carrier solution
199 solve init
200
201 # ramp the floating gate charge
202
203 method newton trap maxtraps=8
204
205 solve prev
206 solve q1=-1e-16
207 solve q1=-5e-16
208 solve q1=-1e-15
209 solve q1=-2e-15
210 solve q1=-3.5e-15
211 solve q1=-5e-15
212
```

```
213 # put a resistor on drain
214
215 contact name=drain r=1.e20
216
217 # do Erasing transient
218 method newton trap maxtraps=8 autonr c.tol=1.e-4 p.tol=1.e-4
     tol.time=0.02 quasi
219
220 log    outf=eprmex01_5.log master
221
222 solve vsource=12.5 tstep=1.e-14 tfinal=4.e-3
223
224 tonyplot eprmex01_5.log -set eprmex01_5.set
225 quit
```

6.1.2. eprmex02.in: 3D Flash EPROM Programming

Requires: DEVEDIT3D/DEVICE3D

This examples demonstrates steady-state and transient simulation of an Flash EPROM device in three dimensions.

In this example an EPROM device is constructed using DEVEDIT3D. The structure is then passed to ATLAS for electrical testing. The input file consists of the following 2 main portions:

- construction of the device in DEVEDIT3D
- threshold voltage test before programming
- transient simulation of Flash EPROM programming
- threshold voltage test after programming

The first stage of the input constructs the EPROM geometry, material regions, doping profiles and electrodes in DEVEDIT3D. The structure was created in DEVEDIT3D by drawing the device regions in interactive mode and specifying 3D doping distribution. Finally the mesh was generated automatically by specifying basic mesh constraints and refining in the important areas of the device.

The ATLAS simulation begins from reading in the structure from DEVEDIT3D. The DECKBUILD provides an automatic interface between DEVEDIT and ATLAS so that the structure produced by the DEVEDIT3D is transferred to ATLAS without having to use the mesh statement.

In ATLAS the contact statements are used to assign the work function on the polysilicon gates and to specify the floating gate contact. The interface statement is used to assign a fixed interface charge under the floating gate. The models statement is used to select a set of physical models for programming simulation. The key model for programming is the hot carrier injection model to give the gate current. This is enabled by models hei.

First, the initial solution for zero biases is obtained. Next, Id/Vgs calculations are performed with zero charge on the floating gate(before programming). The drain voltage is set to 0.5V, and the control gate voltage is ramped until the drain current reaches a compliance limit set with the 'compl' parameter. At this stage combined algorithm is specified using method gummel newton. It means that if convergence is not reached in decoupled mode (gummel), the simulator will automatically switch to coupled mode (newton).

Next, the programming process is simulated. First of all, the control gate voltage is ramped to 10V. The combined algorithm is used for this stage, but the coupled Newton method is used for transient

analysis, calculations. In the transient analysis the drain voltage is ramped to 5.5V in 1ns. Vds is kept constant while transient programming is performed until the time set by tfinal is reached. The mechanism for charging only the floating gate is the same as described in the previous example.

The final stage of the file re-simulates the Id/Vgs curve to obtain the threshold voltage after programming. The results of the two Id/Vgs curves can be overlaid using TONYPLOT. The extract statement can be used to measure the threshold according to user-defined rules. Details of the extract syntax for threshold voltage can be found under the MOS threshold voltage example. extract can also be used to measure the threshold voltage shift by subtracting the two previously extracted thresholds.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory. Once loaded into DECKBUILD, select the run button to execute the example.

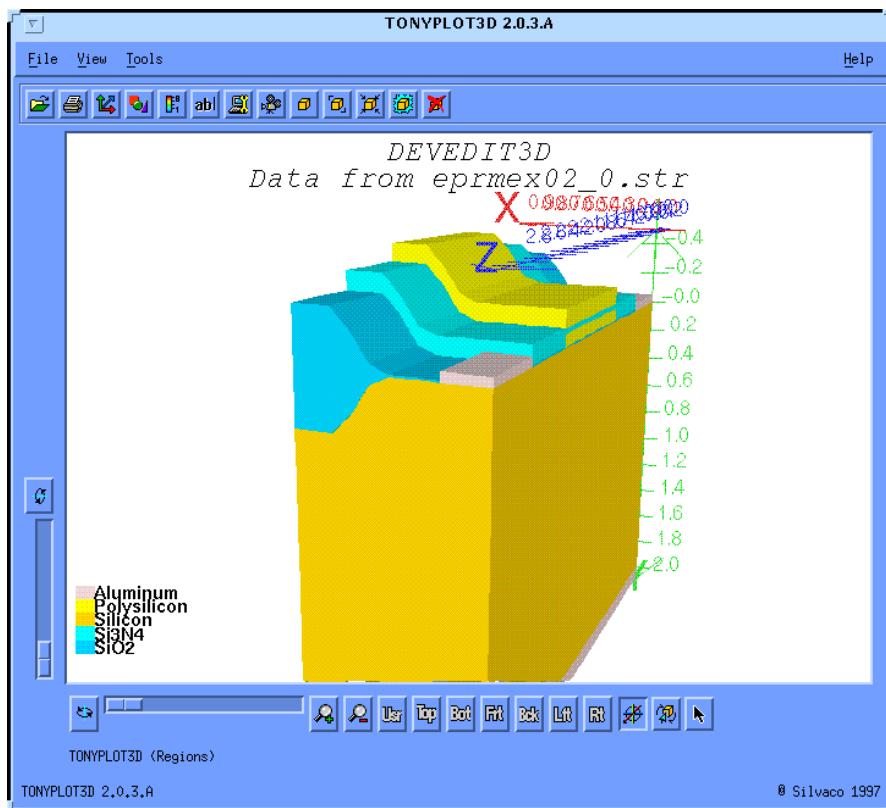


Figure 6.5: 3D EEPROM Structure defined in DevEdit3D

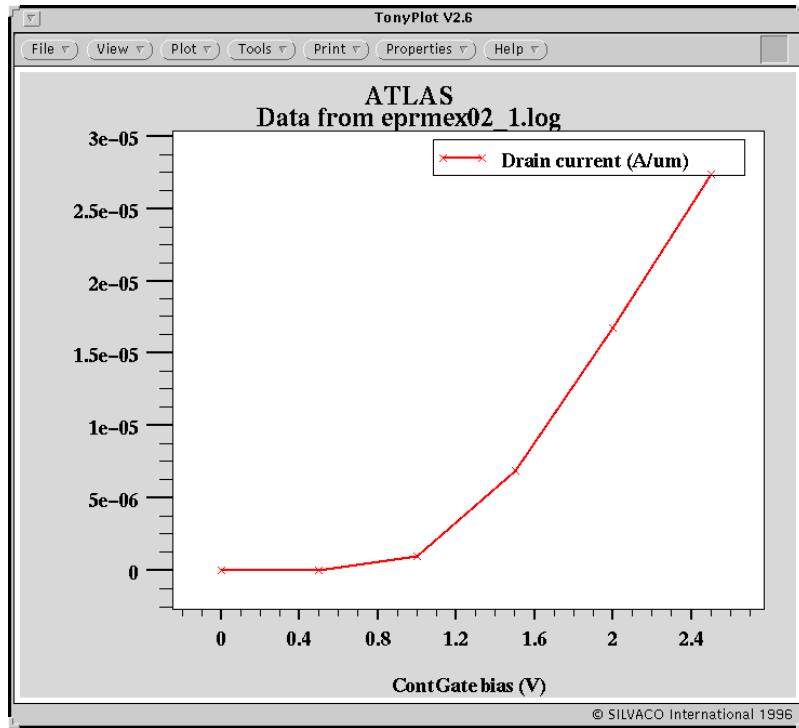


Figure 6.6: Threshold Voltage curve from 3D EEPROM

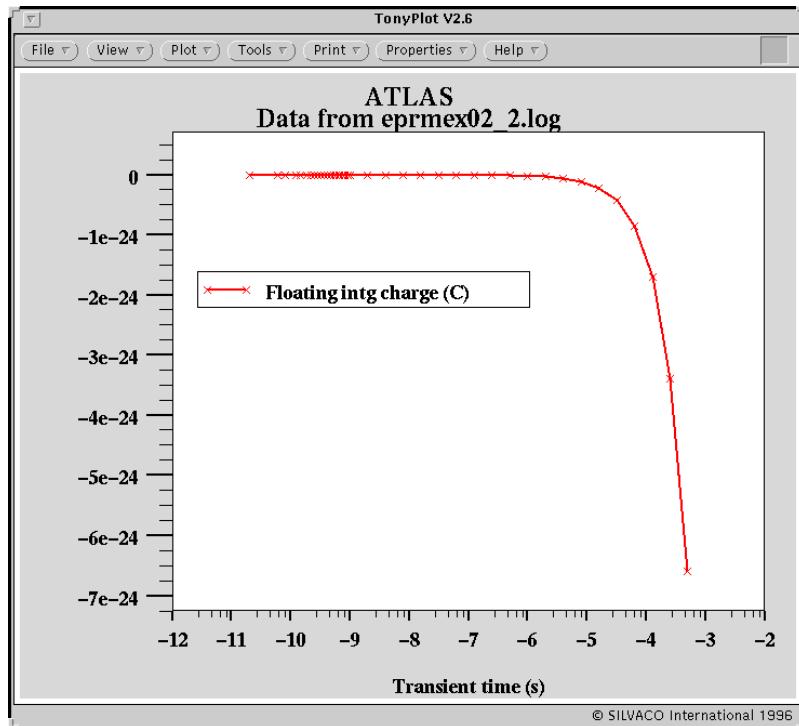


Figure 6.7: Programming curve from 3D EEPROM

Input File eprom/eprmex02.in:

1 go DevEdit

```
2
3  region reg=1 mat=Silicon color=0xffffc000 pattern=0x3 z1=0 z2=3 \
4    points="0,0 0.25,0 0.5,0 0.6,0.05 0.7,0.2 0.8,0.3 1,0.3 1,2 0,2 0,0"
5  #
6  impurity id=1 region.id=1 imp=Boron color=0x906000 \
7    x1=0 x2=0 y1=0 y2=0 \
8    peak.value=2e+16 ref.value=0 z1=0 z2=0 comb.func=Multiply \
9    rolloff.y=both conc.func.y=Constant \
10   rolloff.x=both conc.func.x=Constant \
11   rolloff.z=both conc.func.z=Constant
12
13
14  region reg=2 mat="Silicon Oxide" color=0xff pattern=0x1 z1=0 z2=3 \
15    points="0,-0.01 0.25,-0.01 0.5,-0.01 0.55,-0.03 0.6,-0.05 0.7,-0.2 0.8,-
     0.3 1,-0.3 1,0.3 0.8,0.3 0.7,0.2 0.6,0.05 0.5,0 0.25,0 0,0 0,-0.01"
16
17
18  region reg=3 mat="Silicon Nitride" color=0xffff pattern=0x2 z1=0.5 z2=2.5 \
19    points="0,-0.11 0.5,-0.11 0.6,-0.15 0.7,-0.3 0.8,-0.4 1,-0.4 1,-0.3 0.8,-
     0.3 0.7,-0.2 0.6,-0.05 0.55,-0.03 0.5,-0.01 0.25,-0.01 0,-0.01 0,-0.05
     0,-0.08 0,-0.11"
20
21  region reg=4 name=ContGate mat=PolySilicon elec.id=1 color=0xfffff00 pat-
     tern=0x4 z1=1 z2=2 \
22  points="0,-0.21 0.5,-0.21 0.6,-0.25 0.7,-0.4 0.8,-0.5 1,-0.5 1,-0.4 0.8,-
     0.4 0.7,-0.3 0.6,-0.15 0.5,-0.11 0,-0.11 0,-0.21"
23
24  region reg=5 name=Floating mat=PolySilicon elec.id=2 color=0xfffff00 pat-
     tern=0x4 z1=1 z2=2 \
25  points="0,-0.08 0.5,-0.08 0.55,-0.06 0.55,-0.03 0.5,-0.01 0.25,-0.01 0,-
     0.01 0,-0.05 0,-0.08"
26
27  region reg=6 name=Source mat=Aluminum elec.id=3 color=0xffffc8c8 pat-
     tern=0x6 z1=0 z2=0.5 \
28  points="0,-0.05 0.25,-0.05 0.25,-0.01 0.25,0 0,0 0,-0.01 0,-0.05"
29
30  region reg=7 name=Drain mat=Aluminum elec.id=4 color=0xffffc8c8 pattern=0x6
     z1=2.5 z2=3 \
31  points="0,-0.05 0.25,-0.05 0.25,-0.01 0.25,0 0,0 0,-0.01 0,-0.05"
32
33  region reg=8 name=substrate mat=Aluminum elec.id=5 work.func=0 col-
     or=0xffffc8c8 pattern=0x7 z1=0 z2=3 \
34  points="0,2 1,2 1,2.1 0,2.1 0,2"
35
36
```

```
37 impurity id=1 imp=Boron color=0x906000 \
38 x1=0 x2=0.5 y1=0.05 y2=0.05 \
39 peak.value=1e+17 ref.value=0 z1=0 z2=3 comb.func=Multiply \
40 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
41 rolloff.x=both conc.func.x="Error Function" conc.param.x=0.05 \
42 rolloff.z=both conc.func.z=Gaussian conc.param.z=1
43 impurity id=2 imp=Boron color=0x906000 \
44 x1=0.5 x2=1 y1=0.4 y2=0.4 \
45 peak.value=1e+17 ref.value=0 z1=0 z2=3 comb.func=Multiply \
46 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
47 rolloff.x=both conc.func.x="Error Function" conc.param.x=0.05 \
48 rolloff.z=both conc.func.z=Gaussian conc.param.z=1
49 impurity id=3 imp=Arsenic color=0x906000 \
50 x1=0 x2=0.3 y1=0 y2=0 \
51 peak.value=1e+20 ref.value=0 z1=0 z2=1.2 comb.func=Multiply \
52 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.08 \
53 rolloff.x=both conc.func.x="Error Function" conc.param.x=0.08 \
54 rolloff.z=both conc.func.z="Error Function" conc.param.z=0.08
55 impurity id=4 imp=Arsenic color=0x906000 \
56 x1=0 x2=0.3 y1=0 y2=0 \
57 peak.value=1e+20 ref.value=0 z1=2 z2=3 comb.func=Multiply \
58 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.03 \
59 rolloff.x=both conc.func.x="Error Function" conc.param.x=0.05 \
60 rolloff.z=both conc.func.z="Error Function" conc.param.z=0.05
61
62 # Set Meshing Parameters
63 #
64 base.mesh height=0.5 width=0.5
65 #
66 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
       line.straightening=1 align.points when=automatic
67 #
68 imp.refine imp="Arsenic" sensitivity=1
69 imp.refine min.spacing=0.01 z=0
70 #
71 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
72 max.width=1 min.height=0.0001 min.width=0.0001
73 #
74 # Perform mesh operations
75 #
76 Mesh Mode=MeshBuild
77 Refine Mode=X P1=0.88,0.33 P2=0.89,0.64
78 Refine Mode=Y P1=0.33,-0.46 P2=0.33,-0.46
```

```
79 Refine Mode=X P1=0.07,-0.004 P2=0.30,0.49
80 Refine Mode=X P1=0.07,0.004 P2=0.20,0.52
81 Refine Mode=Both P1=0.27,-0.16 P2=0.27,-0.16
82 Refine Mode=Y P1=0.013,-0.005 P2=0.44,0.012
83 Refine Mode=Y P1=0.012,0.008 P2=0.46,0.01
84 Refine Mode=Y P1=0.02,0.08 P2=0.33,0.09
85
86 imp.refine imp="Arsenic" sensitivity=1
87 imp.refine min.spacing=0.01 z=0
88
89 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
90 max.width=1 min.height=0.0001 min.width=0.0001
91
92
93 z.plane z=0.5 spacing=0.25
94 #
95 z.plane z=1 spacing=0.125
96 #
97 z.plane z=2 spacing=0.1
98 #
99 z.plane z=2.5 spacing=0.25
100 #
101 z.plane max.spacing=1000000 max.ratio=1.5
102
103 base.mesh height=0.5 width=0.5
104
105 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
     line.straightening=1 align.Points when=automatic
106
107 structure outf=eprmex02_0.str
108
109 go atlas
110
111 # Electrode #1 Control gate
112 # Electrode #2 Floating gate
113 # Electrode #3 Source
114 # Electrode #4 Drain
115 # Electrode #5 Substrate
116
117 # Set workfunction for the poly gates,
118
119 contact num=2 n.polysilicon floating
120 contact num=1 n.polysilicon
```

```
121
122 #Define some Qss...
123 interface qf=3e10
124
125 models srh cvt hei
126
127
128 ##### This is the Vt Test before programming #####
129 #####
130 solve init
131 method gummel newton trap maxtraps=8
132
133 log outf=eprmex02_1.log
134 solve v4=0.5
135 solve vstep=0.5 vfinal=25 electr=1 comp=2.e-5 e.compliance=4
136
137 # plot idvg
138
139 tonyplot eprmex02_1.log -set eprmex02_1.set
140 # extract vt
141 extract name="initial vt" ((xintercept(maxslope(curve(v."Cont-Gate",i."Drain"))))-abs(ave(v."Drain")))/2.0)
142
143
144 ##### This is the Programming/Writing Transient #####
145 #####
146
147
148 method gummel newton trap maxtraps=8
149 log off
150
151 #ramp the control gate to 10 V
152
153 solve init
154 solve v1=3
155 solve v1=6
156 solve v1=10
157
158 # ramp up drain voltage
159
160 method newton trap maxtraps=8 quasi
161 log    outf=eprmex02_2.log master
162
```

```

163 solve v4=5.5 ramptime=1e-9 tstep=2e-11 tfinal=1e-9
164
165
166 # keep voltages constant and perform transient programming
167 solve tstep=1e-9 tfinal=5.e-4
168 # plot programming curve
169 tonyplot eprmex02_2.log -set eprmex02_2.set
170
171
172 ##### This is the Vt Test After Programming #####
173 #####
174
175 method gummel newton trap maxtraps=8
176
177 log outf=eprmex02_3.log
178 solve init
179 solve v4=0.5
180 solve vstep=0.5 vfinal=25 electr=1 comp=2.e-5 e.compliance=4
181 # plot new idvg overlaid on old one
182 tonyplot -overlay eprmex02_1.log eprmex02_3.log -set eprmex02_3.set
183 # extract vt and vt shift
184 extract name="final vt" ((xintercept(maxslope(curve(v."Cont-
    Gate",i."Drain"))))-abs(ave(v."Drain")))/2.0)
185 extract name="vt shift" ("final vt" - "initial vt")
186
187 quit
188
189

```

6.1.3. eprmex03.in: Controlling the Capacitative Coupling

Requires: SSUPREM4/DEVEDIT/S-PISCES

This example consists of :

- dual gate EEPROM structure formation in ATHENA
- re-meshing in DEVEDIT
- threshold voltage simulation without a coupling capacitor
- definition of additional coupling capacitance
- threshold voltage simulation with a coupling capacitor
- Plotting two threshold voltage curves for comparison

This example file is based upon that given in exprmex01.in but has an additional modification to account for capacitive coupling. A description of the standard syntax may be found in example eprmex01.in.

In a real device the coupling between the control gate and the floating gate is a three-dimensional problem that depends upon the layout. As a result, any two-dimensional simulation will not be able to accurately simulate coupling capacitance. In most cases it will underestimate this value. Taking this problem into account, ATLAS is capable of connecting electrodes together via some capacitor. This effectively increases the coupling capacitance and can normally allow accurate matching to experimental data without having to make unphysical modifications to the structure.

This example consists of two ATLAS input files. The first is a standard calculation of the threshold voltage from which the coupling ratio may be found. In the second, the syntax has been modified so that on the contact statement a capacitance is specified between the control and floating gates. After plotting the results, it is apparent that the coupling ratio has been increased due to the additional coupling capacitance. This has effectively modified the threshold voltage.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

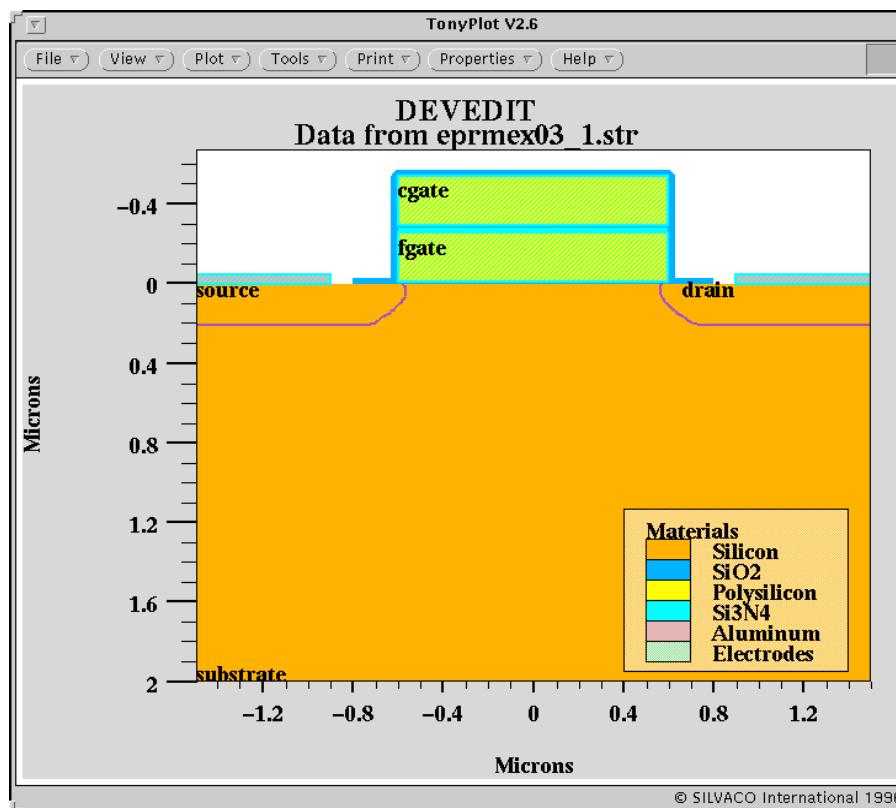


Figure 6.8: Flash Structure defined in ATHENA and remeshed in DevEdit

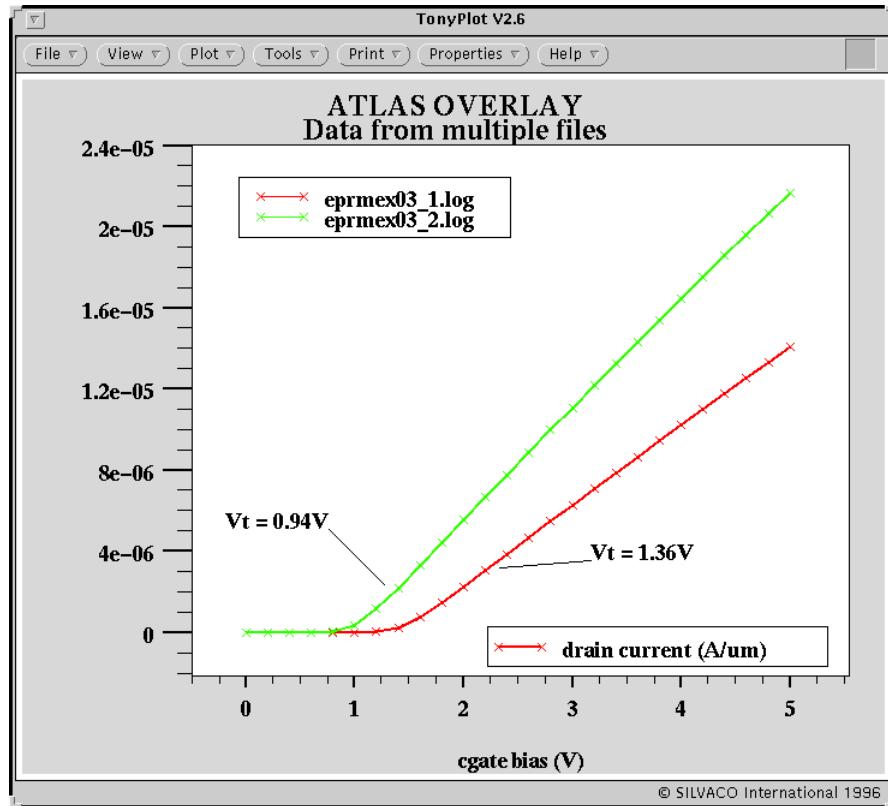


Figure 6.9: Effect of Coupling Capacitance on 3D

Input File eprom/eprmex03.in:

```

1 go athena
2 #TITLE: EEPROM cell formation example
3 #
4
5 line x loc=0.0  spac=0.1
6 line x loc=0.6  spac=0.025
7 line x loc=0.9  spac=0.05
8 line x loc=1.5  spac=0.2
9 #
10 line y loc=0.00 spac=0.01
11 line y loc=0.3  spac=0.03
12 line y loc=2.0  spac=0.25
13
14 #
15 init c.boron=3e16 orientation=100 space.mult=1
16
17 #
18 method compress fermi
19 diffuse time=10 temp=950 dryo2
20 #

```

```
21 extract name="tunnelox" thickness oxide mat.occno=1 x.val=0
22 #
23 implant boron dose=1e12 energy=25
24 #
25 deposit poly thick=.25 div=4
26 #
27 implant phos dose=6e14 energy=30
28 #
29 diffuse time=5 temp=950 dryo2
30 #
31 deposit nitride th=.02
32 #
33 deposit oxide th=.01
34 #
35 deposit poly thick=.25 div=4 phos conc=8e19
36 #
37 etch poly right p1.x=.6
38 #
39 etch oxide right p1.x=.6
40 #
41 etch nitride right p1.x=.6
42 #
43 etch oxide right p1.x=.6
44 #
45 etch poly right p1.x=.6
46 #
47 etch oxide right p1.x=.6
48 #
49 relax y.min=.3 dir.y=f
50 #
51 implant arsenic dose=1e15 energy=40
52 #
53 diff time=50 temp=950
54 deposit oxide thick=.03 div=2
55 #
56 structure mirror left
57 #
58 etch oxide left p1.x=-0.8
59 etch oxide right p1.x=0.8
60 #
61 deposit alum th=.05
62 #
63 etch alum start x=0.9 y=-10.
```

```
64 etch alum cont x=0.9 y=10.
65 etch alum cont x=-.9 y=10.
66 etch alum done x=-.9 y=-10.
67 #
68 # define electrode names
69 electrode name=fgate x=0 y=-0.1
70 electrode name=cgate x=0 y=-0.4
71 electrode name=source x=-1.5
72 electrode name=drain x=1.5
73 electrode name=substrate backside
74 # save the structure
75 structure outfile=eprmex03_0.str
76 #
77 # Switch to DevEdit for remeshing...
78 go DevEdit
79
80 # Set Meshing Parameters
81 #
82 base.mesh height=0.4 width=0.4
83 #
84 # Make sure impurity gradients have enough detail. (i.e. no triangle
85 # spans more than 1 (sensitivity=1) power of 10)
86 imp.refine imp="NetDoping" sensitivity=1
87 imp.refine min.spacing=0.02
88 #
89 # Make sure channel has enough triangles.
90 constr.mesh depth=0.25 under.material="PolySilicon" max.height=0.05 \
91     max.width=0.05
92 constr.mesh depth=0.05 under.material="PolySilicon" max.height=0.015
93 #
94 # Make sure contacts have enough connection points.
95 constr.mesh depth=0.05 under.material="Aluminum" max.width=0.1
96
97 # Create a mesh, using the parameters set above.
98 mesh mode=meshbuild
99
100 # save structure
101 struct outfile=eprmex03_1.str
102 tonyplot eprmex03_1.str -set eprmex03_1.set
103
104
105 # switch to Atlas for the Device Tests....
106
```

```
107 go atlas
108 mesh infile=eprmex03_1.str
109
110 #
111 # Set workfunction for the poly gates,
112 #
113 contact name=fgate n.polysilicon floating
114 contact name=cgate n.polysilicon
115 #
116 #Define some Qss...
117 interface qf=3e10
118 models srh cvt hei fnord print nearflg
119 impact selb
120
121 ##### This is the Vt Test without additional coupling #####
122 #####
123 solve init
124 #
125 method newton trap maxtraps=8 autonr
126 #
127 log outf=eprmex03_1.log
128 solve vdrain=0.1
129 solve vstep=0.2 vfinal=5 name=cgate comp=5.5e-5 cname=drain
130 #
131 # extract vt
132 extract name="initial vt" ((xintercept(maxs-
    llope(curve(v."cgate",i."drain"))))-abs(ave(v."drain")))/2.0)
133 #
134 go atlas
135 mesh infile=eprmex03_1.str
136 #
137 # Set workfunction for the poly gates,
138 #
139 contact name=fgate n.polysilicon floating ele.cap=2 fg.cap=1e-15
140 contact name=cgate n.polysilicon
141 #
142 #Define some Qss...
143 interface qf=3e10
144 models srh cvt hei fnord print nearflg
145 impact selb
146 #
147 ##### This is the Vt Test with additional coupling #####
148 #####
```

```

149 solve      init
150 #
151 method     newton trap maxtraps=8 autonr
152 #
153 log        outf=eprmex03_2.log
154 solve      vdrain=0.1
155 solve      vstep=0.2 vfinal=5 name=cgate comp=5.5e-5 cname=drain
156 # plot idvg
157 #
158 tonyplot -overlay eprmex03_1.log eprmex03_2.log -s eprmex03_2.set
159 # extract vt
160 extract name="second vt" ((xintercept(maxs-
    lope(curve(v."cgate",i."drain"))))-abs(ave(v."drain")))/2.0)
161 #
162 quit

```

6.1.4. eprmex04.in: Hot Carrier Injection and Ionization

Requires: SSUPREM4/DEVEDIT/S-PISCES

This example has been based upon exprmex01.in for the SSUPREM4/DEVEDIT simulations. It demonstrates

- Concannon model for substrate current
- Concannon model for hot carrier injection to the gate
- Plotting of gate current as a function of position on the gate

In practice hot electron injection is normally analysed by measuring the gate current that is injected onto the floating gate contact. The ATLAS input file was therefore created to simulate both the floating gate and substrate currents. To do this the electrode `fgate` was not specified as floating.

The Concannon model for substrate current is implemented on the `impact` statement with the parameters, `n.concannon`, `p.concannon`, to turn on the individual electron and hole components. The Concannon model for hot carrier injection is implemented on the `models` statement with the parameters `n.concannon`, `p.concannon` for the individual components. Both of these models are based upon the carrier energies and therefore will automatically implement the electron and hole energy balance equations.

This example finishes by saving a solution and plotting the structure and the injected current as a function of position across the polysilicon gate - oxide interface.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

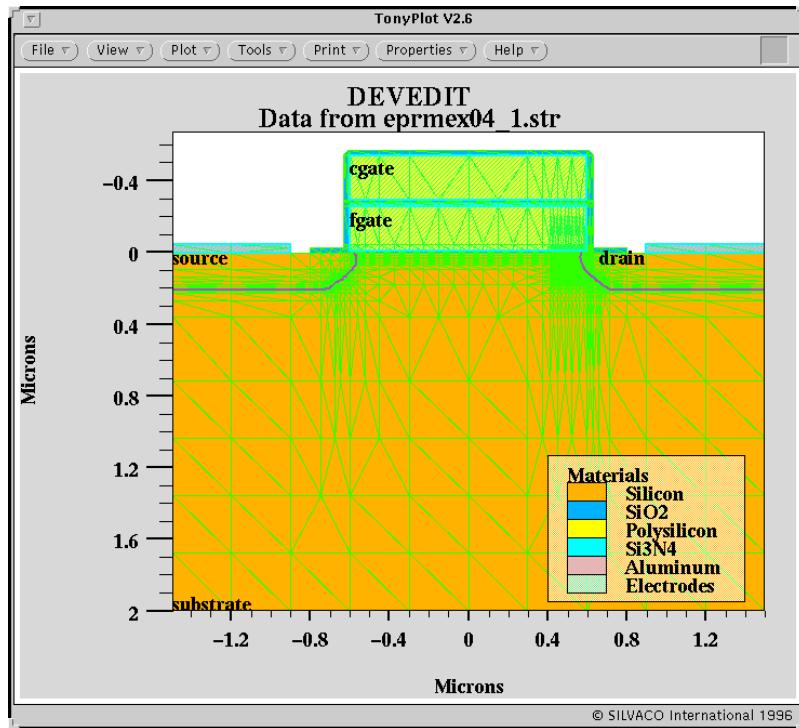


Figure 6.10: Mesh for accurate EEPROM simulations can be created using DevEdit from results of process simulations in ATHENA

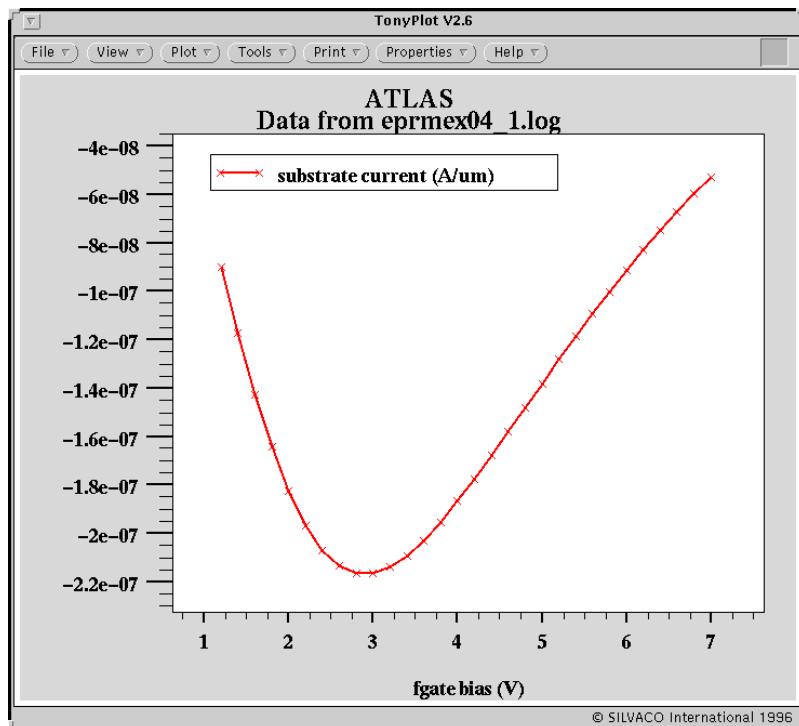


Figure 6.11: Substrate Current Characteristics for the EEPROM using non-local models

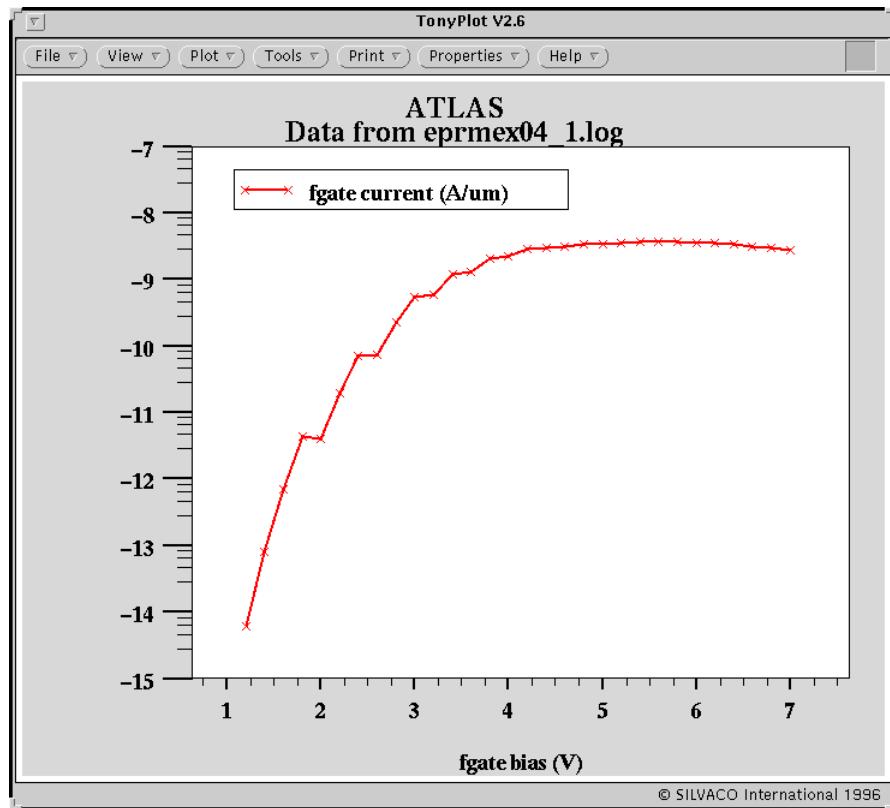


Figure 6.12: Gate Current Characteristics for the EEPROM using non-local models

Input File eprom/eprmex04.in:

```

1 go athena
2 #TITLE: EEPROM cell formation example
3 #
4
5 line x loc=0.0  spac=0.1
6 line x loc=0.6  spac=0.025
7 line x loc=0.9  spac=0.05
8 line x loc=1.5  spac=0.2
9 #
10 line y loc=0.00 spac=0.01
11 line y loc=0.3  spac=0.03
12 line y loc=2.0  spac=0.25
13
14 #
15 init c.boron=3e16 orientation=100 space.mult=1
16
17 #
18 method compress fermi
19 diffuse time=10 temp=950 dryo2
20 #

```

```
21 extract name="tunnelox" thickness oxide mat.occno=1 x.val=0
22 #
23 implant boron dose=1e12 energy=25
24 #
25 deposit poly thick=.25 div=4
26 #
27 implant phos dose=6e14 energy=30
28 #
29 diffuse time=5 temp=950 dryo2
30 #
31 deposit nitride th=.02
32 #
33 deposit oxide th=.01
34 #
35 deposit poly thick=.25 div=4 phos conc=8e19
36 #
37 etch poly right p1.x=.6
38 #
39 etch oxide right p1.x=.6
40 #
41 etch nitride right p1.x=.6
42 #
43 etch oxide right p1.x=.6
44 #
45 etch poly right p1.x=.6
46 #
47 etch oxide right p1.x=.6
48 #
49 relax y.min=.3 dir.y=f
50 #
51 implant arsenic dose=1e15 energy=40
52 #
53 diff time=50 temp=950
54 deposit oxide thick=.03 div=2
55
56
57
58 #
59 structure mirror left
60 #
61 etch oxide left p1.x=-0.8
62 etch oxide right p1.x=0.8
63
```

```
64 deposit alum th=.05
65 #
66 etch alum start x=0.9 y=-10.
67 etch alum cont x=0.9 y=10.
68 etch alum cont x=-.9 y=10.
69 etch alum done x=-.9 y=-10.
70 #
71 # define electrode names
72 electrode name=fgate x=0 y=-0.1
73 electrode name=cgate x=0 y=-0.4
74 electrode name=source x=-1.5
75 electrode name=drain x=1.5
76 electrode name=substrate backside
77 # save the structure
78 structure outfile=eprmex04_0.str
79
80 go DevEdit
81
82 #init infile=eprmex01_0.str
83
84 DevEdit version=2.3.2.A
85
86 work.area x1=-1.5000001 y1=-0.5724238 x2=1.5000001 y2=2
87 # DevEdit 2.3.2.A (Wed Apr 16 13:29:36 PDT 1997)
88 # libsflm 2.0.0.R (Tue Apr  8 20:00:47 PDT 1997)
89 # libDW_Misc 1.20.0.A (Wed Apr 16 01:48:23 PDT 1997)
90 # libCardDeck 1.19.10.A (Wed Apr 16 01:59:26 PDT 1997)
91 # libGeometry 1.19.10.A (Wed Apr 16 02:06:31 PDT 1997)
92 # libDW_Set 1.19.0.R (Wed Apr 16 01:50:04 PDT 1997)
93 # libSVC_Misc 1.19.0.R (Wed Apr 16 02:09:29 PDT 1997)
94 # libSDB 1.0.6.A (Wed Apr 16 02:12:50 PDT 1997)
95 # libSSS 1.19.0.R (Wed Apr 16 02:21:54 PDT 1997)
96 # libMeshBuild 1.20.0.A (Wed Apr 16 13:01:32 PDT 1997)
97 # libDW_Make 1.1.3.R (Mon Apr  7 14:21:50 PDT 1997)
98
99 # Set Meshing Parameters
100 #
101 base.mesh height=0.5 width=0.5
102 #
103 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
line.straightening=1 align.points when=automatic
104 #
105 imp.refine imp="Net Doping" scale=log sensitivity=2 transition=1e+10
```

```
106 imp.refine min.spacing=0.02
107 #
108 constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
109 max.width=10000 min.height=0.0001 min.width=0.0001
110 #
111 constr.mesh type=Semiconductor default
112 #
113 constr.mesh type=Insulator default
114 #
115 constr.mesh type=Metal default
116 #
117 constr.mesh type=Other default
118 #
119 constr.mesh region=1 default
120 #
121 constr.mesh region=2 default
122 #
123 constr.mesh region=3 default
124 #
125 constr.mesh region=4 default
126 #
127 constr.mesh region=5 default
128 #
129 constr.mesh region=6 default
130 #
131 constr.mesh region=7 default
132 constr.mesh id=1 under.mat=PolySilicon depth=0.06 default
    max.height=0.015 max.width=0.1
133 constr.mesh id=2 x1=0.42 y1=0 x2=0.62 y2=0.1 default max.width=0.01
134 Mesh Mode=MeshBuild
135
136
137 base.mesh height=0.5 width=0.5
138
139 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
    line.straightening=1 align.Points when=automatic
140
141 # save structure
142 struct outfile=eprmex04_1.str
143 tonyplot eprmex04_1.str -set eprmex04_1.set
144
145
146 go atlas
147
```

```
148 #mesh infile=eprmex04_1.str
149
150 #
151 # Set workfunction for the poly gates,
152 #
153 contact name=fgate n.polysilicon
154 contact name=cgate n.polysilicon
155 #
156 #Define some Qss...
157 interface qf=3e10
158 models srh cvt print nearflg n.concannon cgate.n=0.0025
159 impact n.concannon csub.n=l1l1
160 #
161 solve init
162 #
163 method block newton trap maxtraps=8 autonr
164 #
165 solve vfinal=1 vstep=0.05 name=drain
166 #
167 # Apply initial gate voltage
168 solve vfinal=1 vstep=0.2 name=fgate
169 #
170 # Ramp the drain voltage to 5V
171 solve vfinal=5 vstep=0.2 name=drain
172 #
173 log outf=eprmex04_1.log
174 solve vfinal=7 vstep=0.2 name=fgate
175 #
176 tonyplot eprmex04_1.log -set eprmex04_2.set
177 tonyplot eprmex04_1.log -set eprmex04_3.set
178 #
179 quit
```

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Chapter 7: LATCHUP: CMOS Latchup Application Examples

7.1. LATCHUP: CMOS Latchup Application Examples

7.1.1. latchex01.in: Transient Simulation of CMOS Latch-Up

Requires: MASKVIEWS/SSUPREM4/S-PISCES

This example demonstrates a latch-up transient in an npnp structure typical of CMOS processes. The stages of this examples are:

- definition of a CMOS layout to include a parasitic npnp structure
- interface of the layout information to ATHENA
- process simulation of the npnp structure
- interface of the structure to ATLAS with automatic electrode specification
- setting of a transient negative voltage pulse on the Vss contact to trigger latch-up.

The process simulation for this example is defined using MASKVIEWS. Users not familiar with the MASKVIEWS/ATHENA interface should read the description under the ATHENA_SSUPREM4 examples section. Along with the input file that can be seen by loading this example in to DECKBUILD is a layout file. The layout is of a CMOS well boundary with n+ and p+ contact layers. An n-p-n-p structure is formed by these layers. By modifying the layers it is possible to misalign the contacts with respect to the well boundary and repeat this latch-up simulation. Using the MASKVIEWS/ATHENA interface avoids having to set etch coordinates manually.

Along with the layout file, a MASKVIEWS cross-section file is copied to the user's current working directory when 'Load example' is selected. For this example, the cross-section information is indicated on the go athena line at the top of the input file. This is a cross section drawn by the user through the layout. In this layout it is drawn through the center of the n+ and p+ contacts.

The key syntax in ATHENA that loads the mask edge coordinates are `mask` statements. A syntax sequence such as:

```
deposit alum thickness=0.05 div=2
mask name="MET"
etch alum dry thickness=0.06
strip
```

will deposit a metal layer, deposit photoresist, set the etch coordinates of the layer defined in the cross section file as 'MET', etches the photoresist pattern, etches the exposed metal with the specified thickness and then finally strips off all photoresist.

In the layout file each area of metal (layer MET) was defined with a name to be used as the name of the electrode associated with that area of metal. Each of the n+ and p+ contacts were defined in this manner. The statement `autoelectrode` at the end of the ATHENA run will automatically define the electrodes for ATLAS.

In ATLAS the material and model parameters are set first as usual. Carrier lifetimes are set in the `material` statement. These lifetimes will affect the gain of the parasitic bipolar devices in this structure. Typical bipolar models are set. Here all models are listed individually, but they could be replaced by the macro `models bip`. For latch-up, impact ionization must also be included. Two DC `solve` statements are required to bias the device into the correct initial voltage with 5V reverse bias between `nwell` and `pwell`.

Latch-up in this example will be caused by a transient pulse on the Vss contact. This is defined by two `solve` statements. The first defines the ramp to the negative voltage and the time at that voltage. The second sets the time for the ramp down and the final simulation time. If no latch-up occurs,

curs, the device should return at the end of this transient to the same state as at the beginning of the transient.

Latch-up is seen in the terminal characteristics as the current rises during the negative pulse, begins to fall, but in the end keeps rising. At the final simulation point, the current is still rising and eventually burn-out of the device would occur. The time taken for this to occur could also be simulated by including lattice heating (using GIGA) into this simulation.

Latch-up can also be seen in the internal distributions of carriers and current density in the solution files generated by this example.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. You cannot run this file until the cross-section file is loaded. To do this go to the DECKBUILD menu **Tools->Mask-Views->Cutlines**. Then select the name of the cross-section file from the list. The name will be <file>.sec where <file> is the name of this example. Then press **Load** on this **Cutline** menu. Once the cross-section file is loaded, select **run** in DECKBUILD to execute the example

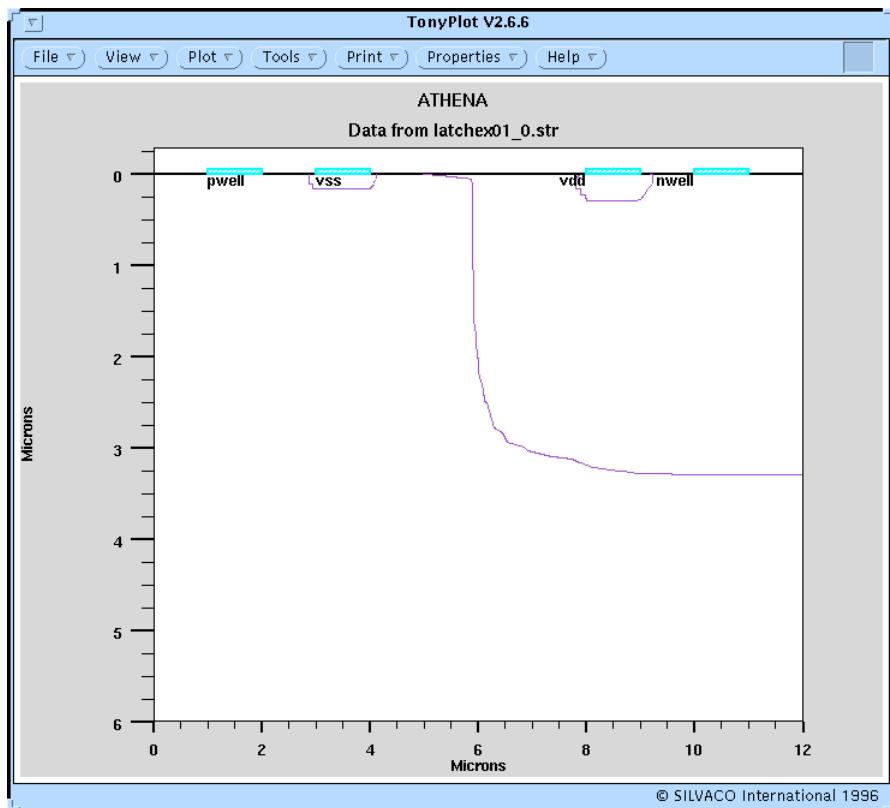


Figure 7.1: Junctions and Electrodes for a CMOS twin-tub well boundary

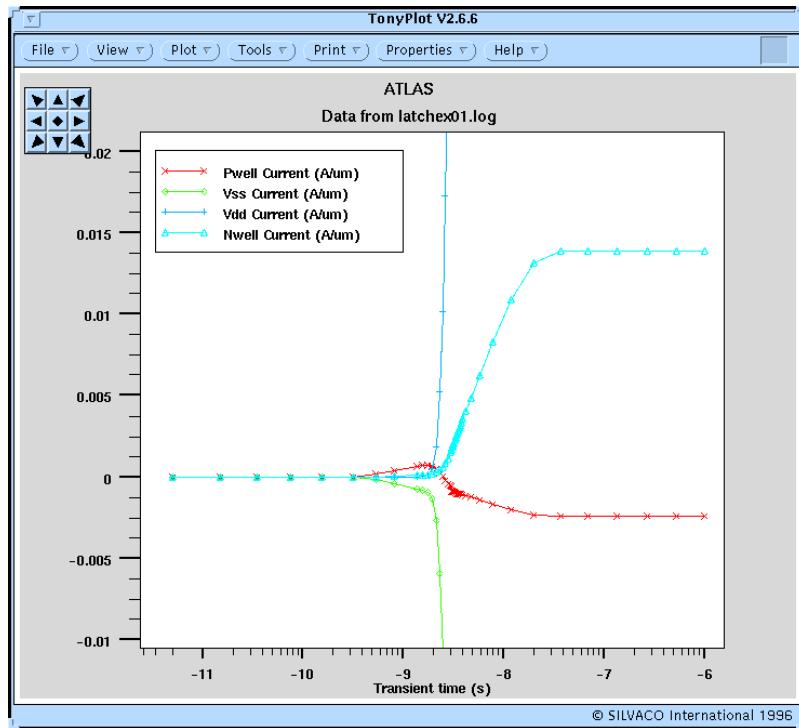


Figure 7.2: Transient Latchup triggered by a negative V_{SS} pulse. Current flows from pwell/vss initially but then switches to direct vdd/vss leakage

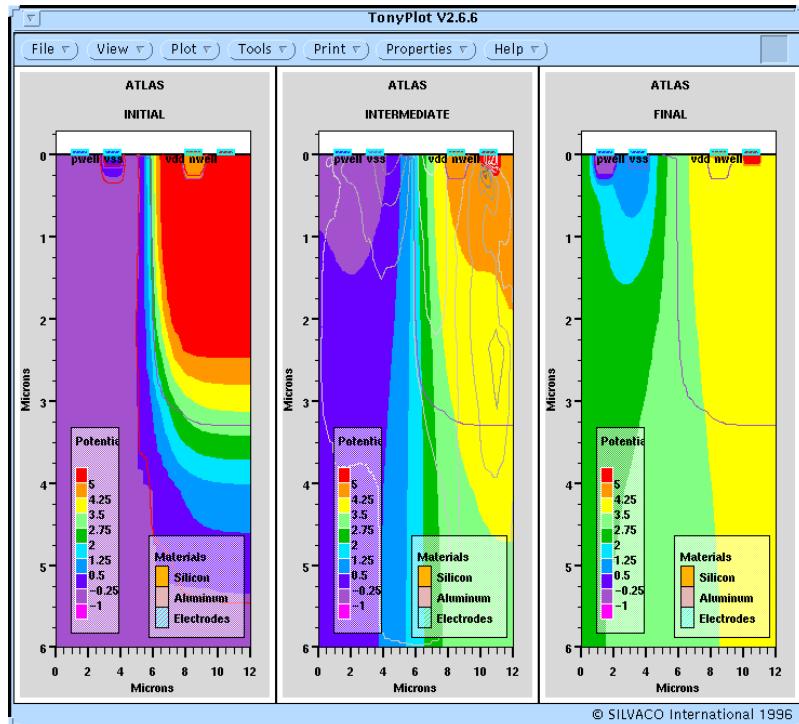


Figure 7.3: Potential contours before, during and after the latchup transient. After latchup the potential is spread evenly across the structure.

Input File latchup/latchex01.in:

```
1 go athena cutfile=latchex01.sec
2
3 # grid and mask information provided by latchex01.sec
4
5 init silicon c.boron=1.0e15 orientation=100
6
7 deposit oxide thickness=0.05
8 mask name="PWE"
9 implant amorphous boron dose=3e12 energy=100
10 strip
11
12 mask name="PWE" reverse
13 implant amorphous phosphorus dose=4e12 energy=180
14 strip
15
16 # relax grid
17 relax y.min=1
18 relax y.min=2
19
20 # well drive
21 diffus time=300 temp=1150
22
23 mask name="N+"
24 implant amorphous arsenic dose=1e15 energy=100
25
26 strip
27
28 mask name="P+"
29 implant amorphous boron dose=1e15 energy=30
30 strip
31
32 # final activation
33 diffuse time=30 temp=900
34
35 etch oxide all
36 deposit alum thickness=0.05 div=2
37 mask name="MET"
38 etch alum dry thickness=0.06
39 strip
40
41 autoelectrode
42
```

```
43 structure outf=latchex01_0.str
44 tonyplot latchex01_0.str -set latchex01_0.set
45
46
47
48
49
50 go atlas
51 # Electrodes #1 - pwell; #2 - vss; #3 - vdd; #4 - nwell;
52 #mesh      inf=latchex01_0.str
53
54 material taup0=1e-6 taun0=1e-6
55 models    bipolar print
56 impact    selb
57 output    flowlines
58
59 method    newton trap
60
61 solve    vnwell=0.25 vstep=0.25 vfinal=5 name=nwell
62 solve    vvdd=0.25 vstep=0.25 vfinal=5 name=vdd
63 save outf=latchex01_1.str
64
65
66 log outf=latchex01.log
67
68
69 solve    v2=-1.0 ramptime=0.5e-9 tstep=5.0e-12 tstop=3.0e-9
70 save outf=latchex01_2.str
71
72 solve    v2=0 ramptime=0.5e-9 tstep=5.0e-11 tstop=1.e-6
73 save outf=latchex01_3.str
74
75 tonyplot latchex01.log -set latchex01_log.set
76 tonyplot latchex01_1.str latchex01_2.str latchex01_3.str -set
    latchex01_1.set
77
78 quit
79
80
```

7.1.2. latchex02.in: CMOS Latch-Up By Positive Voltage on Vdd

Requires: MASKVIEWS/SSUPREM4/S-PISCES

This example demonstrates a latch-up caused by a DC ramp in an npnp structure typical of CMOS processes. The stages of this examples are:

- definition of a CMOS layout to include a parasitic npnp structure
- interface of the layout information to ATHENA
- process simulation of the npnp structure
- interface of the structure to ATLAS with automatic electrode specification
- ramp of Vdd to cause latch-up using curve tracing algorithm.

The parasitic npnp device used is identical to the device in the previous example. The use of MASKVIEWS and ATHENA to create this structure is given in the description of that example. The initial part of the ATLAS run is also identical.

This file differs only in the manner of triggering the latch-up. A DC ramp of the p+ contact in the n-well (named Vdd) is used as the trigger. Once the voltage on Vdd exceeds the 5.0V on the nwell, the p+/n-well junction is forward biased and latch-up may be triggered.

To allow the complete holding voltage and current to be extracted simply, the curve tracing algorithm in ATLAS is used. The key command is the `curvetrace` statement coupled with 'solve curvetrace'. The parameters on the `trace` statement are used to set initial conditions and limits on the curve tracing. A detailed description of the use of this technique in tracing IV curves with turning points can be found in the description of the MOS snapback example.

The latch-up characteristic can be seen in the stored log file. It is important to plot the current versus `vdd int. bias` rather than '`vdd bias`', since the former is the voltage actually applied to the semiconductor and the latter includes the effect of the load line used during the curve trace.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. You cannot run this file until the cross-section file is loaded. To do this go to the DECKBUILD menu **Tools->MaskViews->Cutlines**, then select the name of the cross-section file from the list. The name will be `<file>.sec`, where `<file>` is the name of this example. Then press **Load** on this **Cutline** menu. Once the cross-section file is loaded, select **run** in DECKBUILD to execute the example

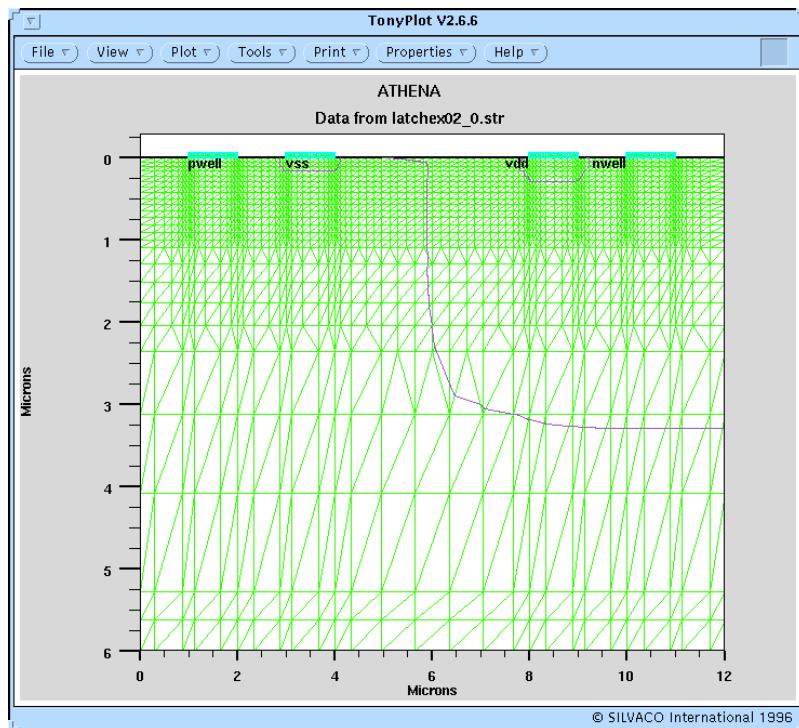


Figure 7.4: Process Simulation Mesh for CMOS Latchup structure

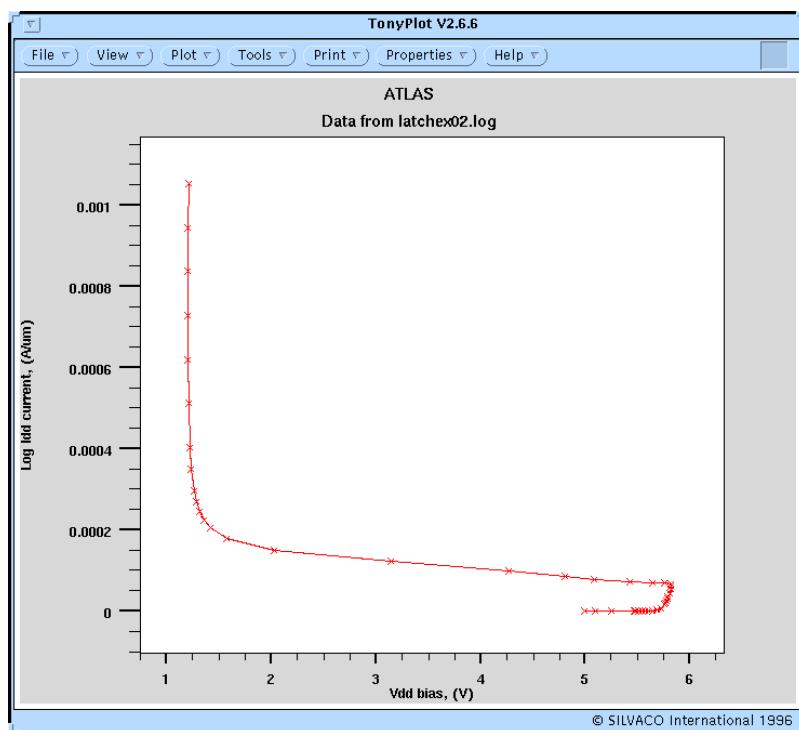


Figure 7.5: DC Latchup via positive pulse on Vdd. The holding voltage and current are clearly seen.

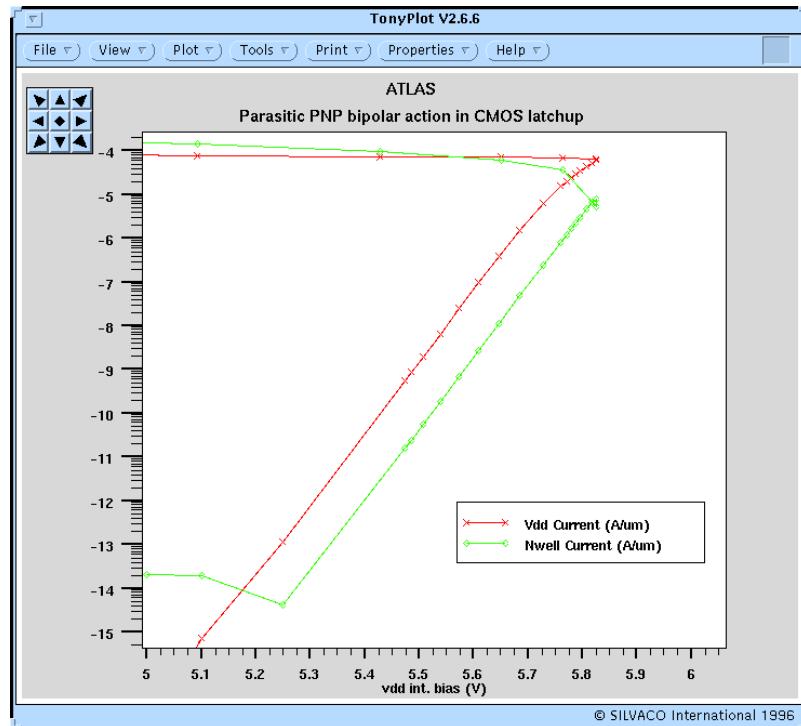


Figure 7.6: Gummel plot of the Vdd/nwell/pwell bipolar transistor. Gain of this parasitic transistor controls latchup when Vdd is pulsed

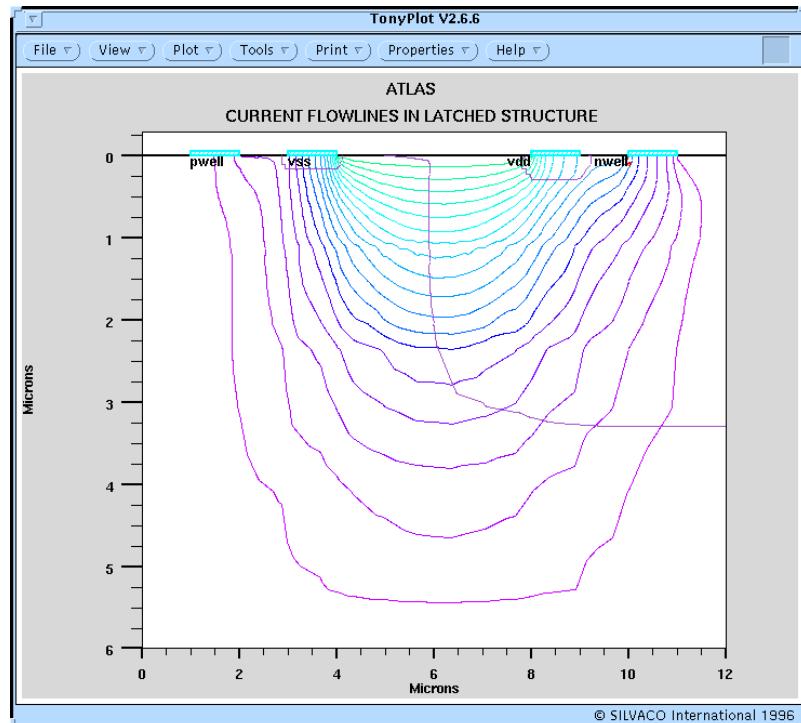


Figure 7.7: Current flowlines after latchup. Most current flows directly from Vdd to Vss. An equal amount of current flows between each pair of lines

Input File latchup/latchex02.in:

```
1 go athena cutfile=latchex02.sec
2
3 # grid and mask information provided by latchex02.sec
4
5 init silicon c.boron=1.0e15 orientation=100
6
7 deposit oxide thickness=0.05
8 mask name="PWE"
9 implant amorphous boron dose=3e12 energy=100
10 strip
11
12 mask name="PWE" reverse
13 implant amorphous phosphorus dose=4e12 energy=180
14 strip
15
16 # relax grid
17 relax y.min=1
18 relax y.min=2
19
20 # well drive
21 diffus time=300 temp=1150
22
23 mask name="N+"
24 implant amorphous arsenic dose=1e15 energy=100
25
26 strip
27
28 mask name="P+"
29 implant amorphous boron dose=1e15 energy=30
30 strip
31
32 # final activation
33 diffuse time=30 temp=900
34
35 etch oxide all
36 deposit alum thickness=0.05 div=2
37 mask name="MET"
38 etch alum dry thickness=0.06
39 strip
40
41 autoelectrode
42 structure outf=latchex02_0.str
```

```
43 tonyplot latchex02_0.str -set latchex02_0.set
44
45 go atlas
46 # Electrodes #1 - pwell; #2 - vss; #3 - vdd; #4 - nwell;
47 # mesh      inf=latchex02_0.str
48 material taup0=1e-6 taun0=1e-6
49 models bipolar print
50 impact selb
51 output flowlines
52
53 method newton trap
54
55 solve vnwell=0.25 vstep=0.25 vfinal=5 name=nwell
56 solve vvdd=0.25 vstep=0.25 vfinal=5 name=vdd
57 save outf=latchex02_1.str
58
59 # syntax for loading solutions.
60 # Can be used on subsequent runs to save time
61 # load inf=latchex02_1.str master
62 # solve prev
63
64 log outf=latchex02.log
65
66 curvetrace end.val=1.e-3 contr.name=vdd curr.cont step.init=0.1 min-
       cur=1e-12 nextst=1.5
67 solve curvetrace
68
69 save outf=latchex02_2.str
70
71 tonyplot latchex02.log -set latchex02_log.set
72 tonyplot latchex02.log -set latchex02_log2.set
73 tonyplot latchex02_2.str -set latchex02_1.set
74
75
76 quit
77
```

7.1.3. latchex03.in: CMOS Latch-Up By Negative Voltage on Vss

Requires: MASKVIEWS/SSUPREM4/S-PISCES

This example demonstrates a latch-up caused by a DC ramp in an npnp structure typical of CMOS processes. The stages of this examples are:

- definition of a CMOS layout to include a parasitic npnp structure
- interface of the layout information to ATHENA

- process simulation of the npnp structure
- interface of the structure to ATLAS with automatic electrode specification
- negative ramp of Vss to cause latch-up using curve tracing algorithm.

The parasitic npnp device used is identical to the device in the previous example. The use of MASK-VIEWS and ATHENA to create this structure is given in the description of that example. The initial part of the ATLAS run is also identical.

This file differs only in the manner of triggering the latch-up. A DC ramp of the n+ contact in the p-well (named Vss) is used as the trigger. Once the voltage on Vss becomes less than the 0.0V on the pwell, the n+/p-well junction is forward biased and latch-up may be triggered.

To allow the complete holding voltage and current to be extracted simply, the curve tracing algorithm in ATLAS is used. The key command is the `curvetrace` statement coupled with '`solve curvetrace`'. The parameters on the trace statement are used to set initial conditions and limits on the curve tracing. In particular, the `step.init` parameter is given as a negative voltage step. This is all that is required to select the polarity of the voltage sweep. A detailed description of the use of this technique in tracing IV curves with turning points can be found in the description of the MOS snapback example.

The latch-up characteristic can be seen in the stored log file. It is important to plot the current versus `vss int. bias` rather than '`vss bias`', since the former is the voltage actually applied to the semiconductor and the latter includes the effect of the load line used during the curve trace.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. You cannot run this file until the cross-section file is loaded. To do this go to the DECKBUILD menu Tools->MaskViews->Cutlines, then select the name of the cross-section file from the list. The name will be `<file>.sec`, where `<file>` is the name of this example. Then press **Load** on this **Cutline** menu. Once the cross-section file is loaded, select **run** in DECKBUILD to execute the example.

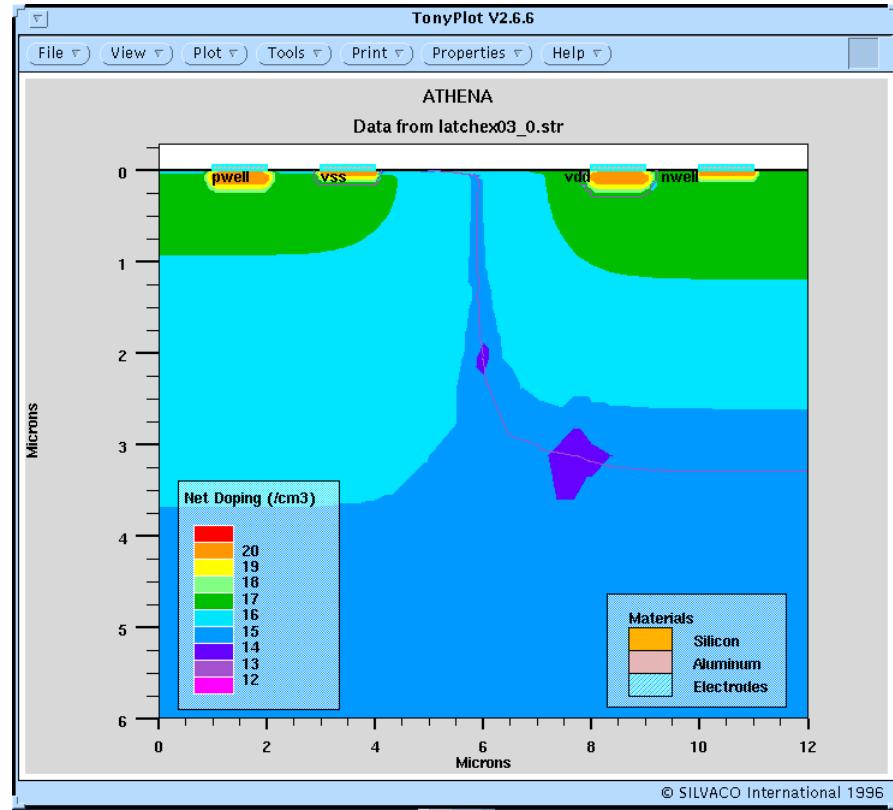


Figure 7.8: Doping profile of CMOS Latchup structure

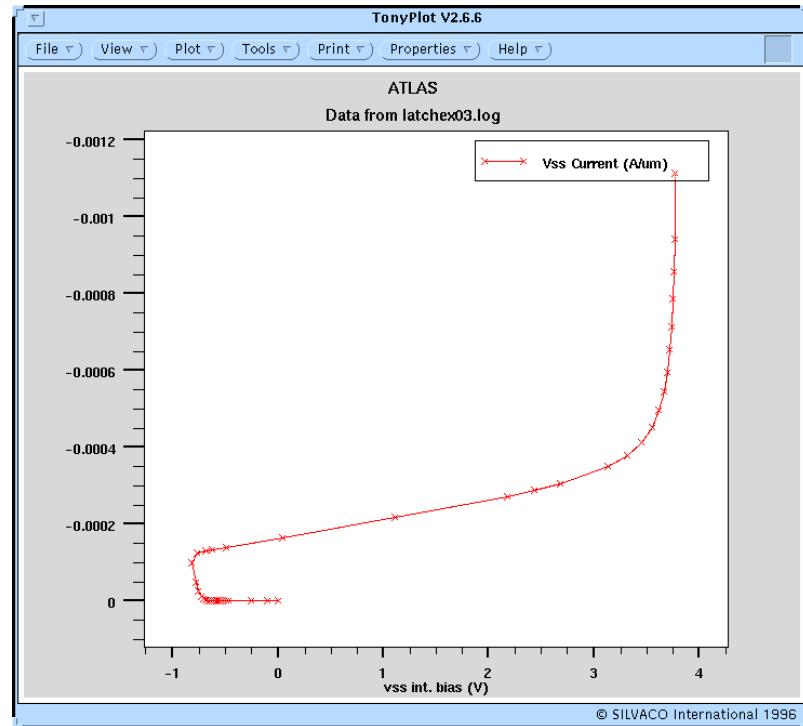


Figure 7.9: DC Latchup via negative pulse on Vss. The holding voltage and current is clearly seen.

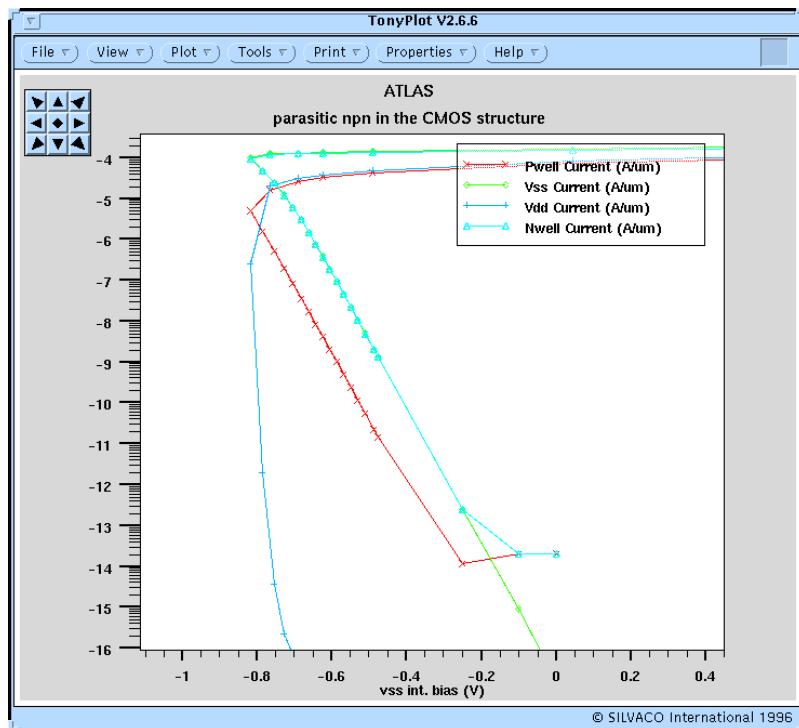


Figure 7.10: Gummel plot of the Vss/pwell/nwell bipolar transistor. Gain of this parasitic transistor controls latchup when Vss is pulsed.

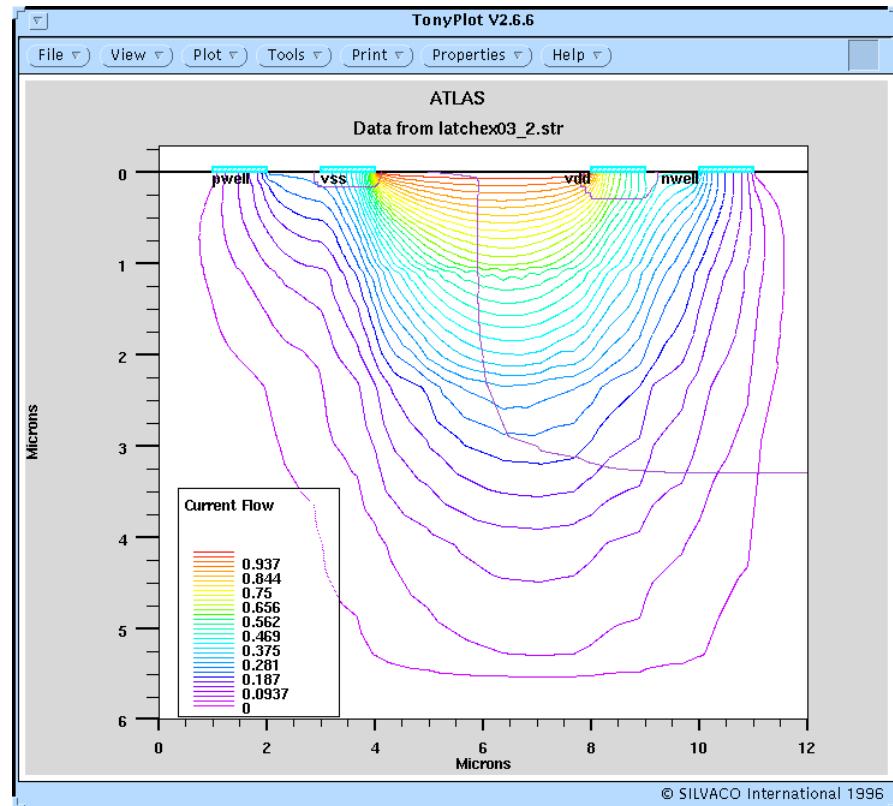


Figure 7.11: Current flowlines after latchup. Most current flows directly from Vdd to Vss. An equal amount of current flows between each pair of lines

Input File latchup/latchex03.in:

```

1 go athena cutfile=latchex03.sec
2
3 # grid and mask information provided by latchex03.sec, latchex03.lay
4
5 init silicon c.boron=1.0e15 orientation=100
6
7 deposit oxide thickness=0.05
8 mask name="PWE"
9 implant amorphous boron dose=3e12 energy=100
10 strip
11
12 mask name="PWE" reverse
13 implant amorphous phosphorus dose=4e12 energy=180
14 strip
15
16 # relax grid
17 relax y.min=1
18 relax y.min=2
19

```

```
20 # well drive
21 diffus time=300 temp=1150
22
23 mask name="N+"
24 implant amorphous arsenic dose=1e15 energy=100
25
26 strip
27
28 mask name="P+"
29 implant amorphous boron dose=1e15 energy=30
30 strip
31
32 # final activation
33 diffuse time=30 temp=900
34
35 etch oxide all
36 deposit alum thickness=0.05 div=2
37 mask name="MET"
38 etch alum dry thickness=0.06
39 strip
40
41 autoelectrode
42 structure outf=latchex03_0.str
43 tonyplot latchex03_0.str -set latchex03_0.set
44
45 go atlas
46 # Electrodes #1 - pwell; #2 - vss; #3 - vdd; #4 - nwell;
47 # mesh inf=latchex03_0.str
48 material taup0=1e-6 taun0=1e-6
49 models bipolar print
50 impact selb
51 output flowlines
52
53 method newton trap
54
55 solve vnwell=0.25 vstep=0.25 vfinal=5 name=nwell
56 solve vvdd=0.25 vstep=0.25 vfinal=5 name=vdd
57 save outf=latchex03_1.str
58
59 # syntax for loading solutions.
60 # Can be used on subsequent runs to save time
61 # load inf=latchex03_1.str master
62 # solve prev
```

```
63
64 log outf=latchex03.log
65
66 curvetrace end.val=1.e-3 contr.name=vss curr.cont step.init=-0.1 min-
    cur=1e-12 nextst=1.5
67 solve curvetrace
68
69 save outf=latchex03_2.str
70
71 tonyplot latchex03.log -set latchex03_log.set
72 tonyplot latchex03.log -set latchex03_log2.set
73 tonyplot latchex03_2.str -set latchex03_1.set
74
75 quit
76
```

7.1.4. latchex04.in: Transient 3D CMOS Latch-Up

Requires: DEVEDIT3D/DEVICE3D

This example demonstrates transient latch-up in a three-dimensional npnp structure typical of CMOS processes. The stages of this examples are:

- definition of npnp structure in DEVEDIT3D
- setting of a transient negative voltage pulse on the Vss contact to trigger latch-up

The npnp structure defined by DEVEDIT3D is a three dimensional one. The n+ and p+ contacts do not fall in one 2D plane as in the previous examples. They are arranged in a rectangle. The DEVICE3D module of ATLAS is required to simulate latch-up in this structure.

The structure is created using DEVEDIT3D either graphically or using the command menus in DECK-BUILD. The most common technique is to form the structure graphically, then save an input file containing all the commands required to reproduce this structure. This input file can be loaded into DECKBUILD and ATLAS runs can be appended to it to create a file similar to this one.

In ATLAS, no special syntax is required to enter the DEVICE3D module as opposed to 2D S-PISCES. On reading a mesh file, ATLAS will automatically detect if it is two or three dimensional. The syntax for specifying bipolar models and setting up the initial bias state are identical to the two-dimensional cases described in the previous examples.

The command, `method halfimpl`, chooses the half-implicit scheme for transient simulation. This scheme significantly reduces the simulation time for many 3D transient problems. In difficult cases more robust but slower methods might be required. The transient pulse applied to the n+ contact in the pwell is similar to the first example in this section.

Results from the log file show latch-up occurs as the device does not return to its initial state after the pulse is over. The current is still increasing at the end of the simulation which will eventually cause device failure. It is possible to repeat this experiment by varying the the parameter, `t.final`, in the statement:

```
solve v4=-2.0 tfinal=4.5e-9 tstep=10.e-12
```

If the voltage is held at -2.0V for shorter times latch-up may not occur.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

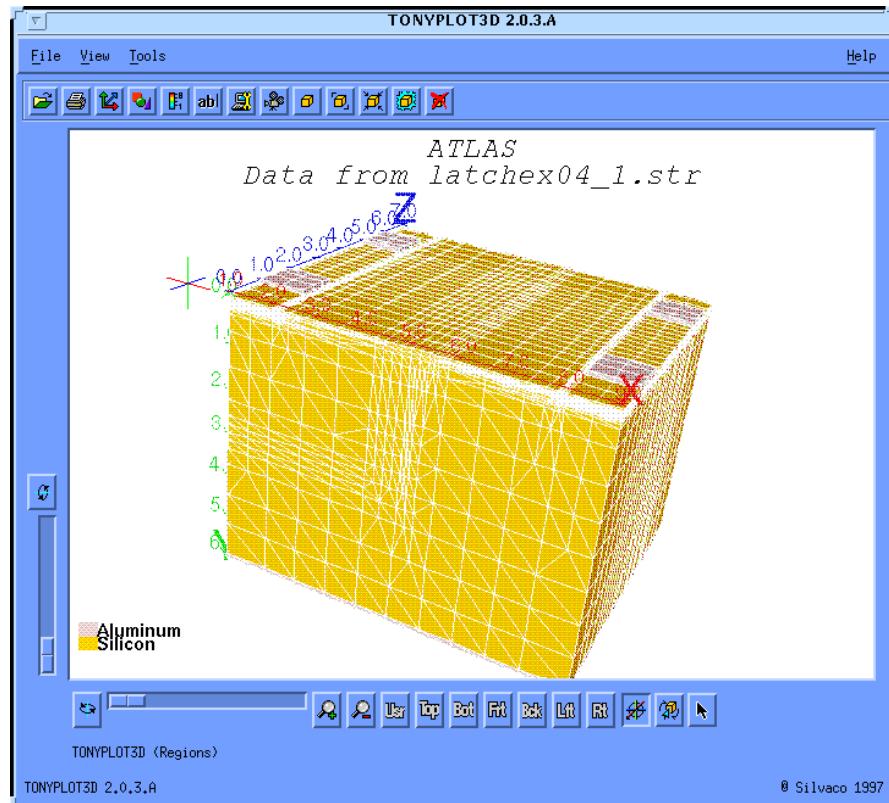


Figure 7.12: 3D CMOS Well Boundary. The Four contacts are not co-planar so 3D device simulation is necessary to show latch-up

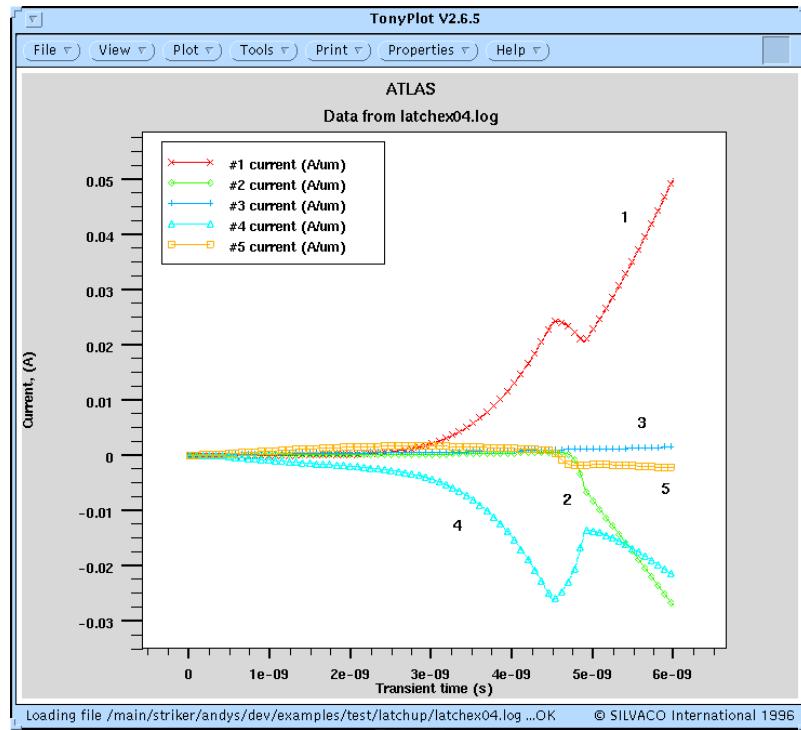


Figure 7.13: Transient waveforms during latchup. 1=vss, 2=vss, 3=nwell 4=backside vss, 5=pwell

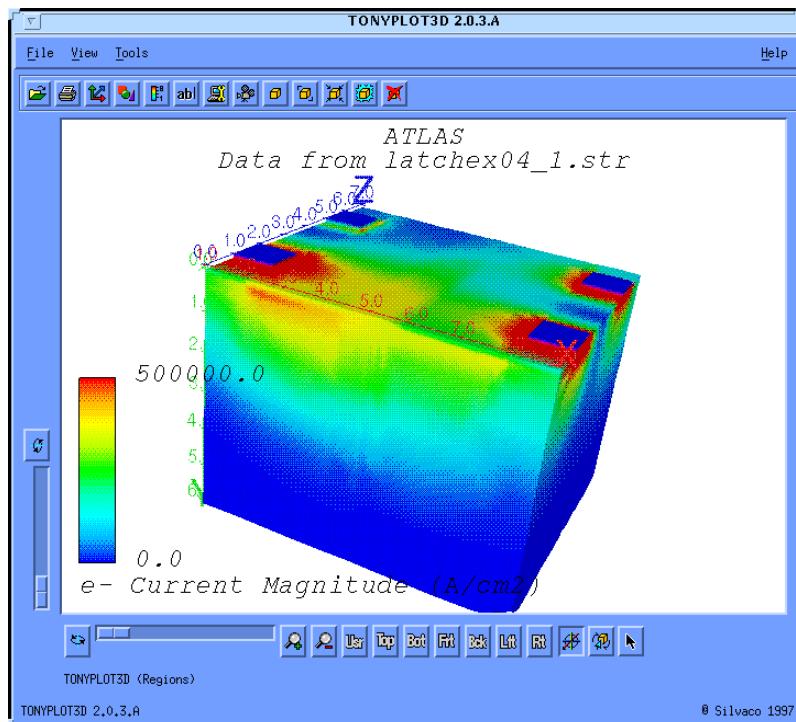


Figure 7.14: Current density in the 3D structure during the latchup transient

Input File latchup/latchex04.in:

1 go DevEdit

```
2
3 DevEdit version="2.1" library="1.15"
4
5 work.area left=0 top=-0.1 right=10 bottom=6.1
6
7 # DevEdit V2.1 L1.15
8
9 region reg=1 mat=Silicon color=0xffffc000 pattern=0x3 z1=0 z2=7 \
10 points="1,0 2,0 8,0 9,0 9,6 1,6 1,0"
11 #
12 impurity id=1 region.id=1 imp=Boron color=0x906000 \
13 x1=0 x2=0 y1=0 y2=0 \
14 peak.value=5e+15 ref.value=0 z1=0 z2=0 comb.func=Multiply \
15 rolloff.y=both conc.func.y=Constant \
16 rolloff.x=both conc.func.x=Constant \
17 rolloff.z=both conc.func.z=Constant
18
19 region reg=2 mat=Aluminum color=0xffffc0c0 pattern=0x6 z1=1 z2=2 \
20 points="1,-0.1 2,-0.1 2,0 1,0 1,-0.1" elec.id=1
21
22 region reg=3 mat=Aluminum color=0xffffc0c0 pattern=0x6 z1=1 z2=2 \
23 points="8,-0.1 9,-0.1 9,0 8,0 8,-0.1" elec.id=2
24
25 region reg=4 mat=Aluminum color=0xffffc0c0 pattern=0x6 z1=5 z2=6 \
26 points="1,-0.1 2,-0.1 2,0 1,0 1,-0.1" elec.id=3
27
28 region reg=5 mat=Aluminum color=0xffffc0c0 pattern=0x6 z1=5 z2=6 \
29 points="8,-0.1 9,-0.1 9,0 8,0 8,-0.1" elec.id=4
30
31 region reg=6 mat=Aluminum color=0xffffc8c8 pattern=0x6 z1=0 z2=7 \
32 points="1,6 9,6 9,6.1 1,6.1 1,6" elec.id=5
33
34
35 impurity id=1 imp=Boron color=0x906000 \
36 x1=1 x2=2 y1=0 y2=0 \
37 peak.value=1e+20 ref.value=0 z1=1 z2=2 comb.func=Multiply \
38 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
39 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.05 \
40 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.05
41 impurity id=2 imp=Arsenic color=0x906000 \
42 x1=8 x2=9 y1=0 y2=0 \
43 peak.value=1e+20 ref.value=0 z1=1 z2=2 comb.func=Multiply \
44 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
```

```
45 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.05 \
46 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.05
47 impurity id=3 imp=Arsenic color=0x906000 \
48 x1=1 x2=2 y1=0 y2=0 \
49 peak.value=1e+20 ref.value=0 z1=5 z2=6 comb.func=Multiply \
50 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
51 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.05 \
52 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.05
53 impurity id=4 imp=Arsenic color=0x906000 \
54 x1=8 x2=9 y1=0 y2=0 \
55 peak.value=1e+20 ref.value=0 z1=5 z2=6 comb.func=Multiply \
56 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
57 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.05 \
58 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.05
59 impurity id=5 imp=Arsenic color=0x906000 \
60 x1=1 x2=4 y1=0 y2=0 \
61 peak.value=1e+16 ref.value=0 z1=0 z2=7 comb.func=Multiply \
62 rolloff.y=both conc.func.y=Gaussian conc.param.y=2.7 \
63 rolloff.x=both conc.func.x=Gaussian conc.param.x=1 \
64 rolloff.z=both conc.func.z=Gaussian conc.param.z=1
65 impurity id=6 imp=Arsenic color=0x906000 \
66 x1=1 x2=4 y1=0 y2=0 \
67 peak.value=1e+17 ref.value=0 z1=0 z2=7 comb.func=Multiply \
68 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
69 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.2 \
70 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.2
71 impurity id=7 imp=Boron color=0x906000 \
72 x1=6 x2=9 y1=0 y2=0 \
73 peak.value=1e+17 ref.value=0 z1=0 z2=7 comb.func=Multiply \
74 rolloff.y=both conc.func.y=Gaussian conc.param.y=0.05 \
75 rolloff.x=both conc.func.x=Gaussian conc.param.x=0.2 \
76 rolloff.z=both conc.func.z=Gaussian conc.param.z=0.2
77
78 # Set Meshing Parameters
79 #
80 base.mesh height=1 width=1
81 #
82 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
     line.straightening=1 align.points when=automatic
83 #
84 imp.refine imp="Total Doping" sensitivity=0.5
85 imp.refine min.spacing=0.01 z=1
86 #
```

```
87 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
88 max.width=1 min.height=0.0001 min.width=0.0001
89 #
90 # Perform mesh operations
91 #
92 Mesh Mode=MeshBuild
93 refine mode=x x1=4.9 y1=0.006 x2=5.52 y2=3.49
94 refine mode=y x1=1.07 y1=3.096 x2=3.97 y2=3.452
95 refine mode=y x1=1.07 y1=2.549 x2=3.98 y2=3.26
96 refine mode=x x1=5.04 y1=0.611 x2=5.19 y2=2.693
97 refine mode=both x1=4.4 y1=2.022 x2=5.07 y2=2.905
98 refine mode=x x1=8.38 y1=0.102 x2=8.57 y2=2.703
99 refine mode=x x1=1.41 y1=0.064 x2=1.54 y2=2.885
100 refine mode=y x1=1.09 y1=2.789 x2=4.01 y2=2.789
101
102 imp.refine imp="Total Doping" sensitivity=0.5
103 imp.refine min.spacing=0.01 z=1
104
105 constr.mesh max.angle=90 max.ratio=300 max.height=1 \
106 max.width=1 min.height=0.0001 min.width=0.0001
107
108 z.plane z=0 spacing=0.5
109 #
110 z.plane z=2 spacing=0.25
111 #
112 z.plane z=5 spacing=0.25
113 #
114 z.plane z=7 spacing=0.5
115 #
116 z.plane max.spacing=1000000 max.ratio=1.5
117
118 base.mesh height=1 width=1
119
120 bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.001
    line.straightening=1 align.Points when=automatic
121
122 structure outf=latchex04_0.str
123
124 go atlas
125
126
127 #
128 # electrode #1 p+ in well
```

```
129 # electrode #2 n+ in p bulk
130 # electrode #3 n+ well
131 # electrode #4 n+ in p bulk backside
132 # electrode #5 substrate
133 #
134 models bgn srh auger conmob fldmob
135
136 #
137 solve init
138
139 method gummel newton carriers=2
140 solve v1=0.1 v3=0.1 local
141 solve v1=0.5 v3=0.5
142 solve v1=1.0 v3=1.0
143 solve v1=3.0 v3=3.0
144
145 method halfimpl dt.min=10.e-12
146 log outf=latchex04.log
147
148 solvev4=-2.0 ramptime=500.e-12 tfinal=500.e-12 tstep=10.e-12
149 solvev4=-2.0 tfinal=4.5e-9 tstep=10.e-12
150 solvev4= 0.0 ramptime=400e-12 tfinal=6.e-9 tstep=10.e-12
    outf=latchex04_1.str onefile
151 tonyplot latchex04.log -set latchex04_log.set
152 quit
153
154
```

8.1. ESD: ESD Application Examples

8.1.1. esdex01.in: Human Body Model in a Diode

Requires: SPICES/GIGA/MIXEDMODE

This simple example demonstrates transient Human Body Model (HBM) ESD simulation in a simple 1D diode. It shows:

- structure formation using ATLAS syntax
- material parameters and model set up for non-isothermal simulation
- transient solution generated by a discharge of a 100pF capacitor through a 1500 Ohm resistor connected to the diode

The input file consists of three separate runs each starting with the statement `go atlas`. The first one uses the ATLAS syntax to construct a 1D diode structure. The mesh, regions and electrodes are specified as coordinates in the syntax. It is compulsory to use electrode names (and not just numbers) when the structure is used in MIXEDMODE. The doping distribution for the device is constructed from Gaussian and uniform analytical functions. The final structure is saved for later use.

The second run calculates the initial operating point of the circuit. The syntax for this run is split into two parts. The first part is a SPICE-like circuit description and control cards. This part is bounded by `.begin` and `.end`. The second is device parameter syntax. The circuit netlist is written using standard SPICE syntax.

After the `.end` statement the device parameter syntax is given. This sets the models, material and contact parameters for the ATLAS device.

The final run uses the `.tran` statement. Note that a time dependent resistor is used which changes value from 1.e6 Ohm to 1500 Ohm during 1ps.

The currents and voltages for each node, and the maximum lattice temperature in the device versus time are stored in the file specified in the `.log` statement.

To load and run this example, select the **Load example** button while this text is displayed. Once loaded into DECKBUILD, select the **run** button to execute the commands. Several support files will also be copied to your home directory at the time of loading.

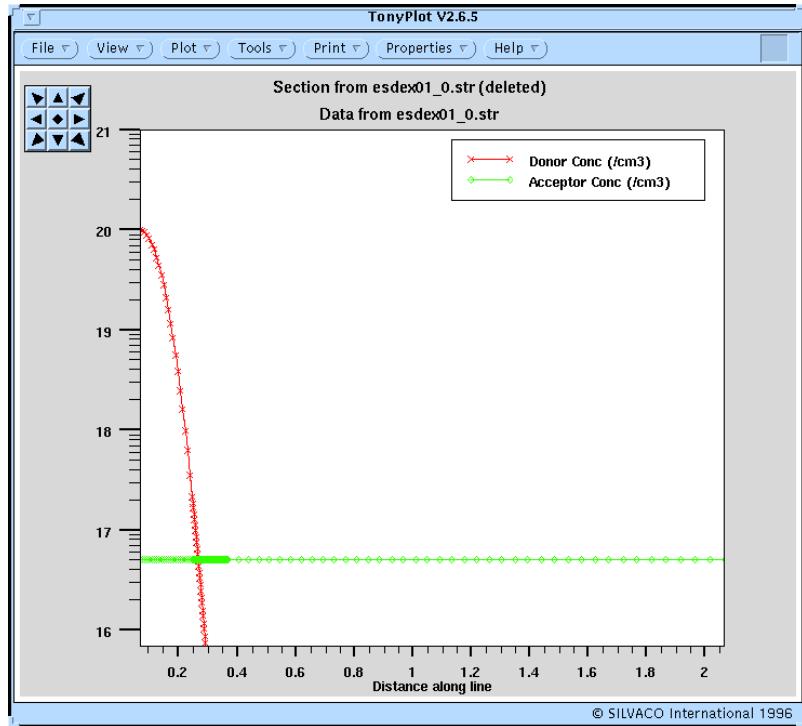


Figure 8.1: Doping profile for 1D diode as an ESD protection device

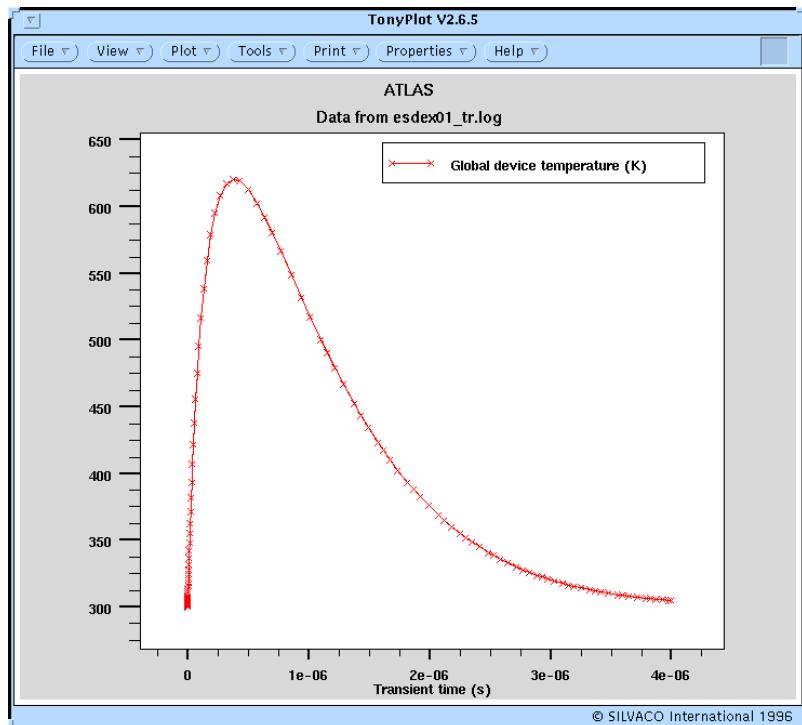


Figure 8.2: Peak Temperature in the diode during the ESD current pulse transient

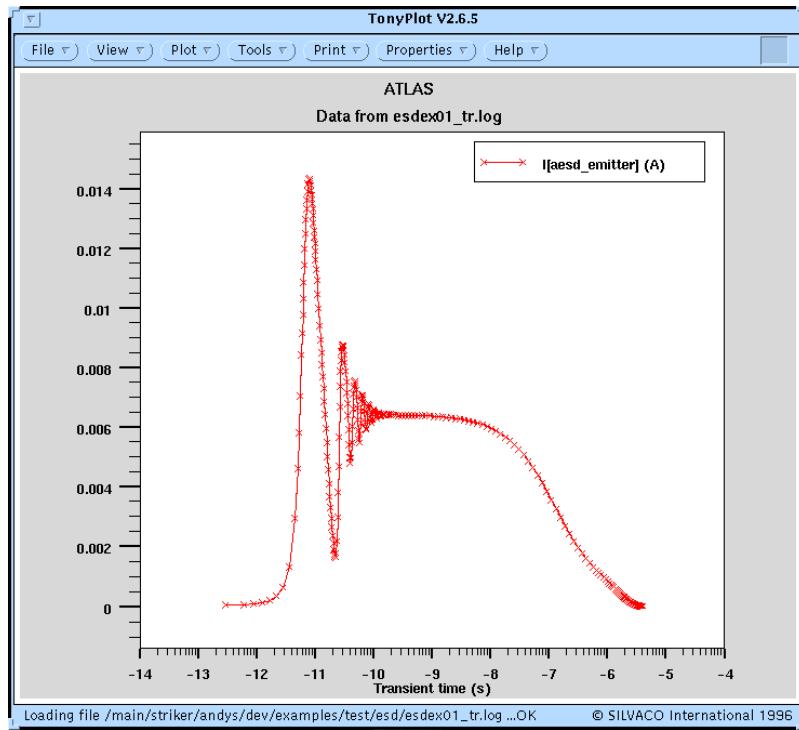


Figure 8.3: Diode current during the ESD current pulse

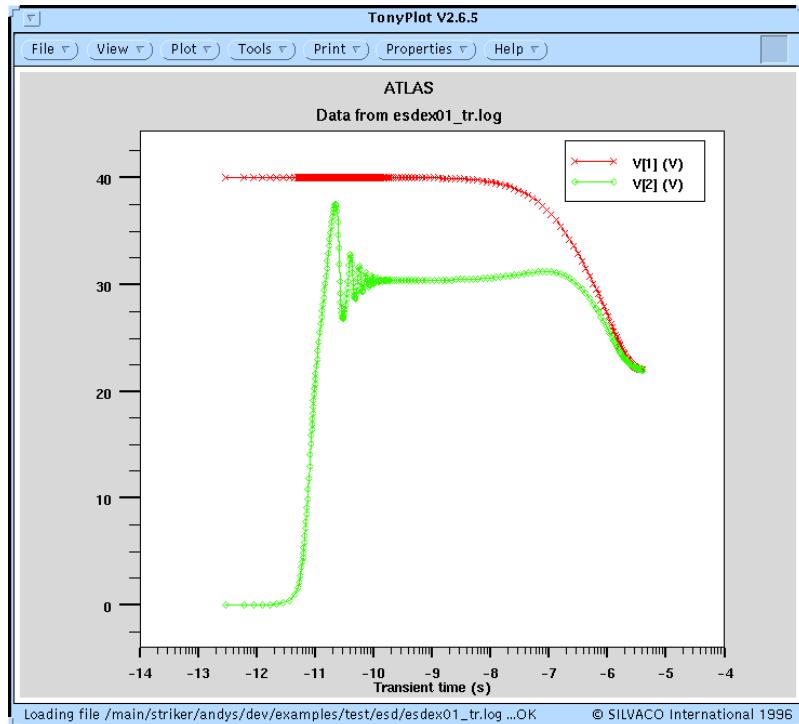


Figure 8.4: Terminal voltages in the diode (o) and circuit (x) during ESD

Input File esd/esdex01.in:

1 go atlas

```
2   TITLE HBM ESD simulation for PN diode
3
4
5   mesh nx=2 ny=65
6   x.m n=1 l=0.0 r=1.0
7   x.m n=2 l=2.0 r=1.0
8
9   y.m n=1 l=0 r=1.0
10  y.m n=12 l=0.18 r=1.0
11  y.m n=45 l=0.3 r=1.0
12  y.m n=65 l=2.0 r=1.02
13
14  region num=1 silicon
15
16  electrode num=1 top name=emitter
17  electrode num=2 bottom name=base
18
19  doping uniform conc=5e16 p.type
20  doping gauss n.type conc=1.e20 dir=y junction=0.2 peak=0
21
22
23  save outf=esdex01_0.str
24  tonyplot esdex01_0.str -set esdex01_0.set
25
26
27  go atlas
28
29  .begin
30  c1 1 0 100p
31  r1 1 2 1500
32  aesd 0=base 2=emitter width=10 infile=esdex01_0.str
33  .nodeset v(1)=40 v(2)=0
34
35  .ic v(1)=40 v(2)=0
36  .numeric toldc=1.e-5 vchange=0.5 imaxdc=999
37  .options m2ln debug print
38  .save outfile=esdex01_dc
39  .end
40
41  thermcontact num=1 device=aesd y.min=2 y.max=2 ext.temp=300 alpha=1000
42  models device=aesd region=1 commob fermi fldmob srh auger bgn lat.temp
43  mater device=aesd region=1 taup0=1e-7 taun0=1e-7
44  impact device=aesd reg=1 selb
```

```

45
46
47 go atlas
48
49 .begin
50 c1 1 0 150p
51 r1 1 2 1.0e6 exp 1.0e6 1500 0. 1ps 10 10
52 aesd 0=base 2=emitter width=10 infile=esdex01_0.str
53 .numeric toltr=1.e-3 vchange=10. lte=0.1 dtmin=0.01ps
54
55 .ic v(1)=40 v(2)=0
56 .options print relpot
57 .tran 0.3ps 4.e-6
58
59 .load infile=esdex01_dc
60 .log outfile=esdex01
61 .end
62
63 thermcontact num=1 device=aesd y.min=2 y.max=2 ext.temp=300 alpha=1000
64 models device=aesd region=1 conmob fldmob fermi srh auger bgn lat.temp
65 mater device=aesd region=1 taup0=1e-7 taun0=1e-7
66 impact device=aesd reg=1 selb
67 method climit=1000
68
69 go atlas
70
71 tonyplot esdex01_tr.log -set esdex01_log.set
72 quit
73

```

8.1.2. esdex02.in: Charge Device Model in a Diode

Requires: S-PISCES/GIGA/MIXEDMODE

This simple example demonstrates transient Charge Device Model (CDM) ESD simulation in a simple 1D diode. It shows:

- structure formation using ATLAS syntax
- material parameters and model set up for non-isothermal simulation
- transient solution generated by a discharge of a 10pF capacitor through a 5nH inductor and 1 Ohm resistor connected to the diode

The input file consists of three separate runs each starting with the statement `go atlas`. The first one uses the ATLAS syntax to construct a 1D diode structure. The mesh, regions and electrodes are specified as coordinates in the syntax. It is compulsory to use electrode names (not just numbers) when the structure is used in MIXEDMODE. The doping distribution for the device is constructed from Gaussian and uniform analytical functions. The final structure is saved for later use.

The second run calculates the initial operating point of the circuit. The syntax for this run is split into two parts. The first part is a SPICE-like circuit description and control cards. This part is bounded by `.begin` and `.end`. The second part is device parameter syntax. The circuit netlist is written using standard SPICE syntax.

After the `.end` statement the device parameter syntax is given. This sets the models, material and contact parameters for the ATLAS device.

The final run uses the `.tran` statement. Note that a time dependent resistor is used which changes value from $1.e6$ Ohm to 1500 Ohm during 1ps.

The currents and voltages for each node, and the maximum lattice temperature in the device versus time are stored in the file specified in the `.log` statement.

To load and run this example, select the **Load example** button while this text is displayed. Once loaded into DECKBUILD, select the **run** button to execute the commands. Several support files will also be copied to your home directory at the time of loading.

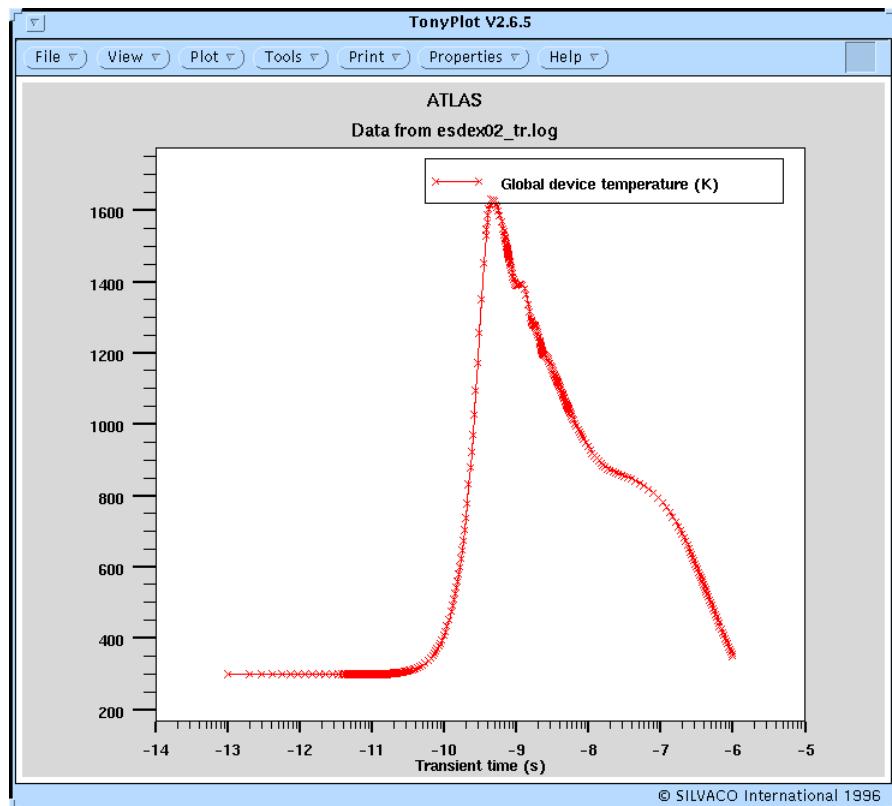


Figure 8.5: Peak Temperature in the diode during the CDM ESD transient

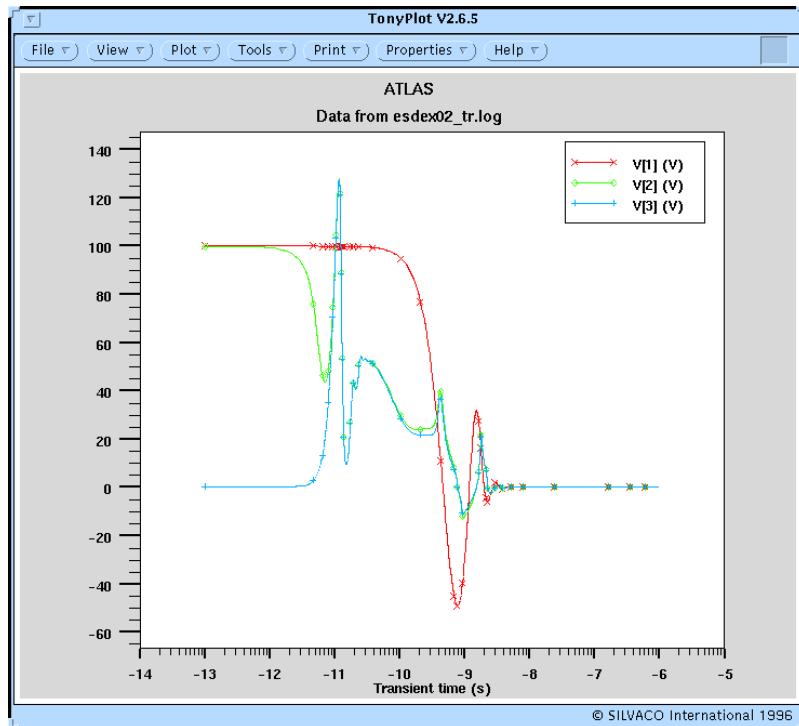


Figure 8.6: Voltages in the circuit during the ESD transient. The presence of an inductor in the CDM Model produces more complex waveforms

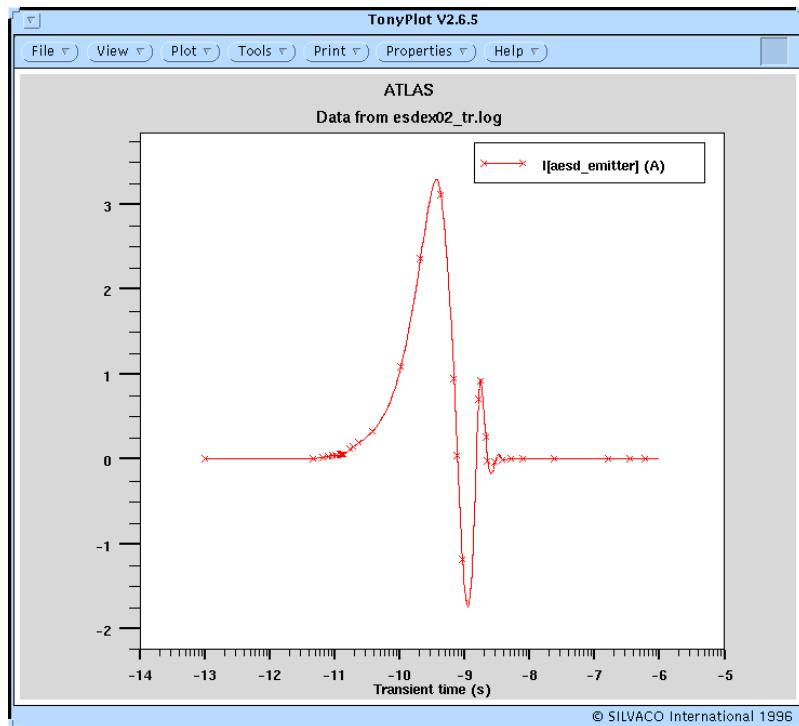


Figure 8.7: Diode Current during the ESD pulse.

Input File esd/esdex02.in:

```
1 go atlas
2 TITLE CDM ESD simulation for PN diode
3
4
5 mesh nx=2 ny=65
6 x.m n=1 l=0.0 r=1.0
7 x.m n=2 l=2.0 r=1.0
8
9 y.m n=1 l=0 r=1.0
10 y.m n=12 l=0.18 r=1.0
11 y.m n=45 l=0.3 r=1.0
12 y.m n=65 l=2.0 r=1.02
13
14 region num=1 silicon
15
16 electrode num=1 top name=emitter
17 electrode num=2 bottom name=base
18
19 doping uniform conc=5e16 p.type
20 doping gauss n.type conc=1.e20 dir=y junction=0.2 peak=0
21
22
23 save outf=esdex02_0.str
24 tonyplot esdex02_0.str -set esdex02_0.set
25
26
27
28
29
30 go atlas
31
32 .begin
33 c1 1 0 10p
34 l1 1 2 5nH
35 r1 2 3 1
36 aasd 0=base 3=emitter width=10 infile=esdex02_0.str
37 .nodeset v(1)=100 v(2)=0 v(3)=0
38
39 .ic v(1)=100 v(2)=0 v(3)=0
40 .numeric toldc=1.e-5 vchange=0.5 imaxdc=999
41 .options m2ln debug print
42 .save outfile=esdex02_dc
```

```

43 .end
44
45 thermcontact num=1 device=aesd y.min=2 y.max=2 ext.temp=300 alpha=1000
46 models device=aesd region=1 commob fldmob srh auger bgn lat.temp
47 mater device=aesd region=1 taup0=1e-7 taun0=1e-7
48 impact device=aesd reg=1 selb
49
50
51 go atlas
52
53 .begin
54 c1 1 0 10p
55 l1 1 2 5nH
56 r1 2 3 1.0e6 exp 1.0e6 1 0. 1ps 10 10
57 aesd 0=base 3=emitter width=10 infile=esdex02_0.str
58 .numeric toltr=1.e-3 vchange=10. lte=0.05 dtmin=0.01ps
59
60 .ic v(1)=100 v(3)=0
61 .options print relpot
62 .tran 0.1ps 1000ns
63
64 .load infile=esdex02_dc
65 .log outfile=esdex02
66 .end
67
68 thermcontact num=1 device=aesd y.min=2 y.max=2 ext.temp=300 alpha=1000
69 models device=aesd region=1 commob fldmob srh auger bgn lat.temp
70 mater device=aesd region=1 taup0=1e-7 taun0=1e-7
71 impact device=aesd reg=1 selb
72 method tol.ltemp=0.01 max.temp=3000 climit=1000
73
74 go atlas
75 tonyplot esdex02_tr.log -set esdex02_log.set
76
77 quit

```

8.1.3. esdex03.in: Human Body Model in a MOSFET

Requires: SSUPREM4/S-PISCES/GIGA

In this example transient simulation of Electrostatic Discharge (ESD) on an NMOS transistor using the Human Body Model (HBM) is performed. During the ESD event significant local heating is produced. The solution of local lattice temperature is included. This example shows:

- formation of a MOS structure in ATHENA
- interface to ATLAS

- selection of lattice heat flow models
- use of current boundary conditions and non-linear transient pulse to simulate a HBM ESD event.
- analysis of both the temperature distribution in the device and non-isothermal IV curve.

The MOS structure is constructed using the ATHENA process simulation. This structure is passed to ATLAS for a HBM test simulation. The NMOS transistor is a 0.8um LDD device using oxide spacers. For a more complete description of the MOS process simulation see the MOS examples.

The ATLAS syntax shows a simple and effective test procedure for HBM ESD simulation that may be used with any initial NMOS structure.

The ATLAS simulation begins with definition of the models and material parameters of the device. The contact statement is used to define the workfunction of the polysilicon electrode. The material statement is used to define the capture times (electron and hole lifetimes) in semiconductor.

The physical models used in this simulation reflect the different physical effects important to ESD device simulation. The mobility model ‘analytic’ accounts for concentration and the temperature dependencies.

The mobility model ‘fldmob’ accounts for the electric field dependency. In addition to the Shockley-Read-Hall recombination model (SRH), the recombination model ‘auger’ is included to take into account the high injection level effects. Band gap narrowing is taken into account by means of the bgn parameter. The continuity equations for both carriers are selected by default. The impact ionization model is turned on using the impact selb statement.

A nonisothermal approach is used, which means that the heat flow equation is solved in addition to the semiconductor equations and all physical parameters become temperature dependent. The syntax, models lat.temp, enables the solution of the heat flow equation.

In all non-isothermal simulations the definition of the thermal boundary conditions is very important. Thermal boundary conditions are defined in the thermcontact statement. A value of the thermal conductance determined from the heat conductivity of the substrate is specified at the thermocontact located along the substrate. Where no thermal contacts are specified, thermal isolation is assumed. Here thermal isolation conditions are assumed on all other surfaces besides the bottom.

To simulate the device interaction with the simplified HBM test circuit, the current pulse is applied to drain of the MOS structure in the reverse direction. The current pulse risetime is 10ns and the exponential decay time is 150ns, which corresponds to the discharge of the 100pF capacitor through the 1500 Ohm resistor into the test device. These values are the definition of the Human Body Model.

The transient current/voltage characteristics are saved in the LOG file. Using TonyPlot, it is possible to observe the maximum temperature in the device versus time. The temperature increases with time and peaks significantly after the peak current. The value of the maximum temperature can be extracted and used as a figure of merit for comparing the ESD protection capability of various device designs.

The probe statement is used to define quantities to be measured at each bias step. The values from these quantities are saved in the log file and can be plotted versus time and bias. The first probe statement saves the *lattice temperature at the drain contact* and the second *electric field across the gate oxide*. The former can be used to determine the likelihood of metal melting and the latter to determine the likelihood of gate dielectric breakdown.

The solution at a time of 10ns and at the final stage are saved. All internal distributions can be observed using TONYPLOT. Most interesting is that the temperature distribution in the MOSFET shows the location and value of the hot spot.

To load and run this example, select the Load example button while this text is displayed. Once loaded into DECKBUILD, select the run button to execute the commands. Several support files will also be copied to your home directory at the time of loading.

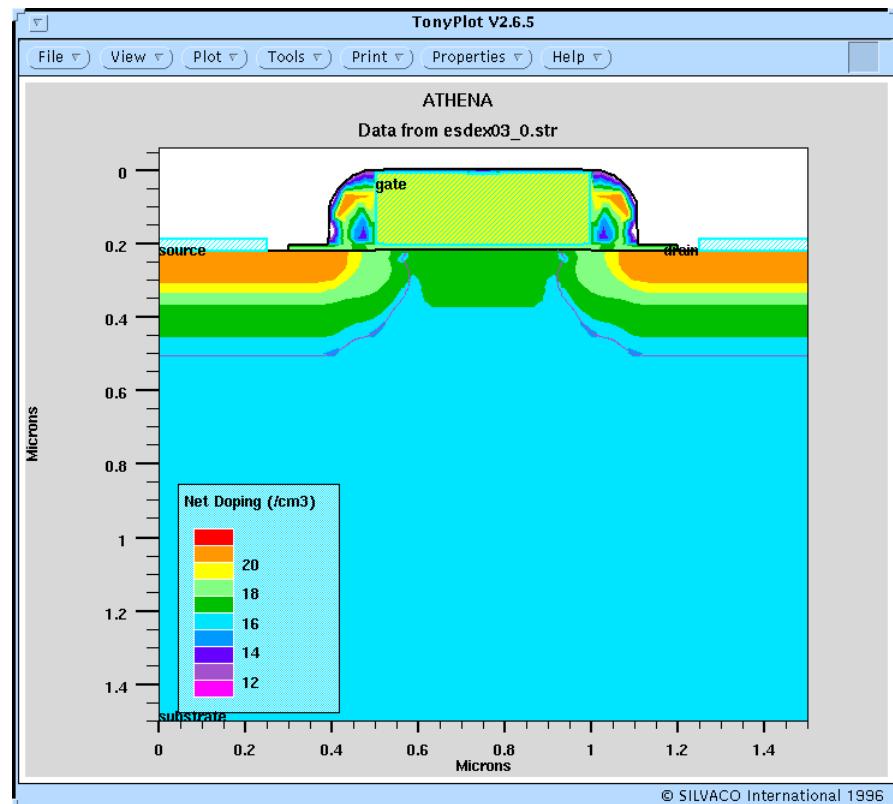


Figure 8.8: Structure and Doping in a MOSFET used for ESD protection

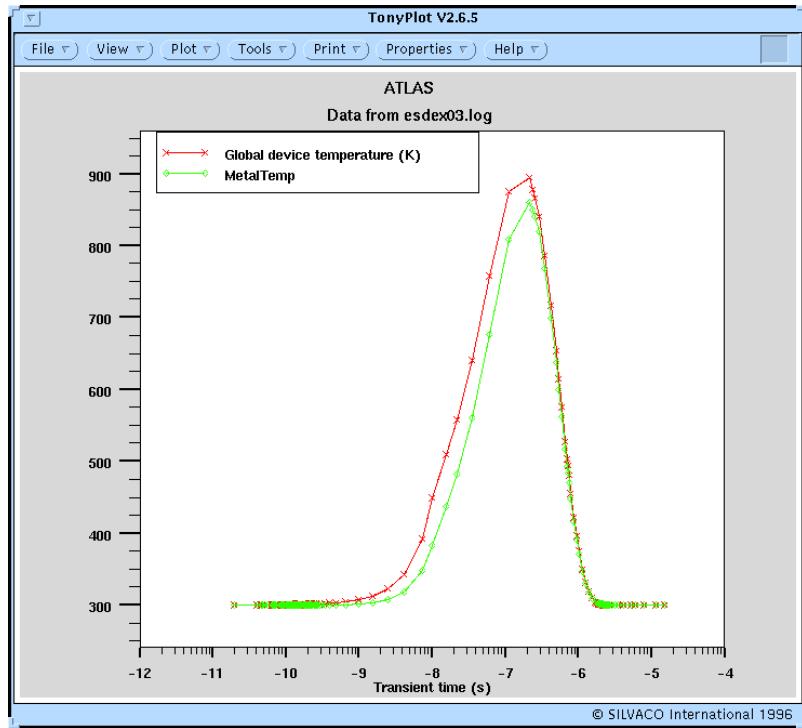


Figure 8.9: Comparison of peak semiconductor temperature and the temperature at the metal/semiconductor contact. The metal contact temperature is the most important of these two for monitoring for ESD protection

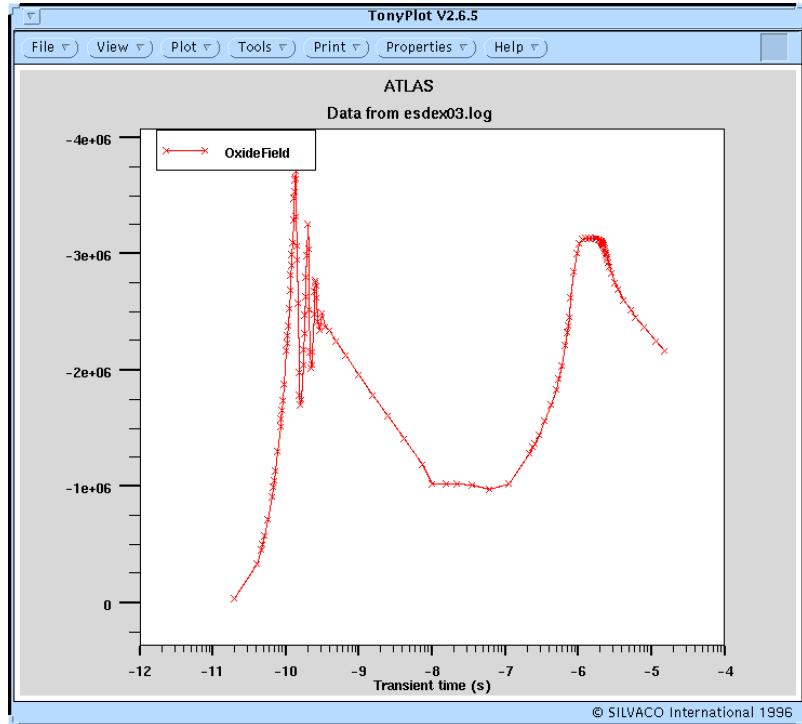


Figure 8.10: Electric Field in the Gate Oxide during the ESD transient. Gate Oxide rupture can be predicted if the field exceeds the critical value

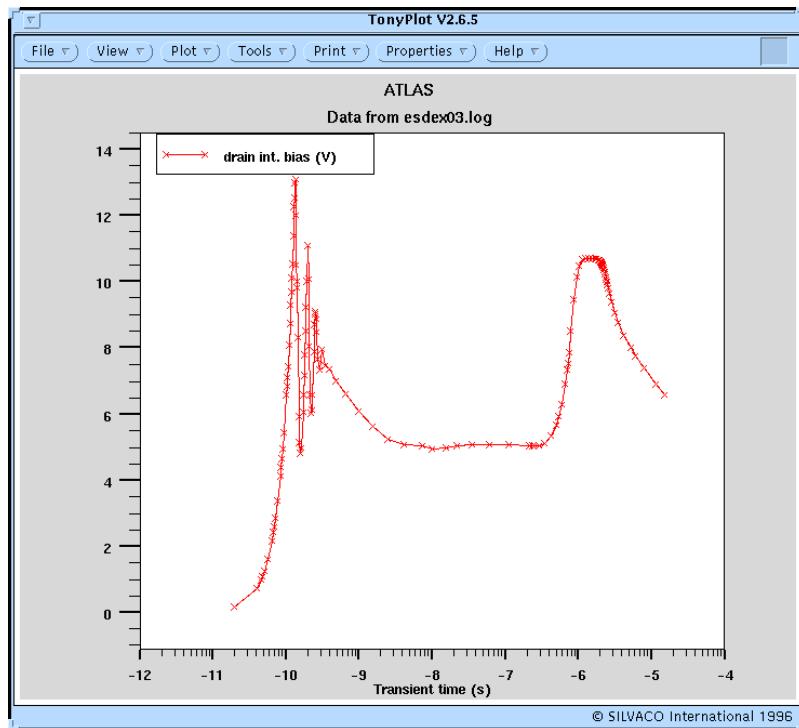


Figure 8.11: MOS Drain bias during the ESD pulse. Complex breakdown behavior is seen due to local heating.

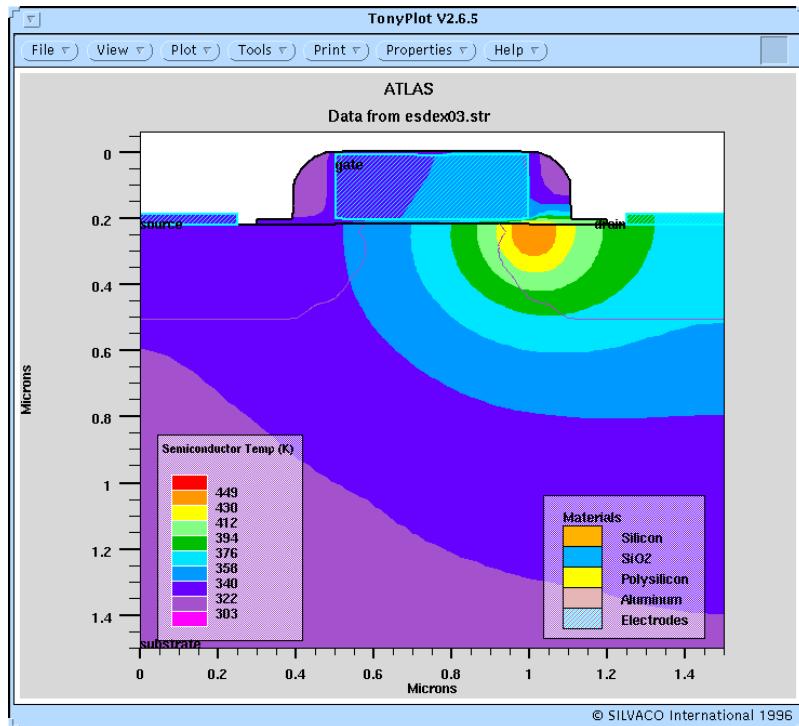


Figure 8.12: 2D temperature distribution in the MOSFET during the ESD transient. A clear hot spot is seen at the gate edge although the metal remains cool.

Input File esd/esdex03.in:

```
1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.5 spac=0.02
5 line x loc=0.75 spac=0.05
6 #
7 line y loc=0.00 spac=0.05
8 line y loc=0.2 spac=0.02
9 line y loc=0.4 spac=0.02
10 line y loc=0.8 spac=0.1
11 line y loc=1.5 spac=0.25
12 #
13 init orientation=100 phos conc=1e14 space.mult=1
14 #
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl%=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=5.0e12 energy=100 pears
24 #
25 diffus temp=950 time=100 weto2 hcl%=3
26 #
27 #N-well implant not shown -
28 #
29 # welldrive
30 diffus time=220 temp=1200 nitro press=1
31 #
32 etch oxide all
33 #
34 #sacrificial "cleaning" oxide
35 diffus time=20 temp=1000 dryo2 press=1 hcl%=3
36 #
37 etch oxide all
38 #
39 #gate oxide grown here:-
40 diffus time=8 temp=950 dryo2 press=1.00 hcl%=3
41 extract name="gate tox" thickness oxide mat.occcno=1 x.val=1
42 #
```

```
43 #vt adjust implant
44 implant bf2 dose=1.5e12 energy=35 pearson
45 #
46 depo poly thick=0.20 div=3
47 #
48 etch poly left p1.x=0.5
49 #
50 relax y.min=0.8
51 method fermi compress
52 diffuse time=5 temp=850 weto2 press=0.8
53 extract name="sidewall tox" thickness oxide mat.occno=1 y.val=0.1
54 #
55 implant phosphor dose=3.0e13 energy=50 pearson
56 #
57 depo oxide thick=0.10 divisions=5
58 #
59 etch oxide dry thick=0.10
60 #
61 implant arsenic dose=5.0e15 energy=50 pearson
62 #
63 #
64 method fermi compress
65 diffuse time=5 temp=950 nitro press=1.0
66 #
67 structure outf=half.str
68
69 # extract final S/D Xj
70 extract name="s/d xj" xj silicon mat.occno=1 x.val=0.05 junc.occno=1
71 extract name="s/d rho" sheet.res silicon mat.occno=1 x.val=0.05 re-
    gion.occno=1
72 extract name="1d vt" ldvt vb=0.0 x.val=0.7
73
74 #
75 etch oxide left p1.x=0.3
76 deposit alumin thick=0.03 div=2
77 etch alumin right p1.x=0.25
78 structure mirror right
79
80 electrode name=gate x=0.75 y=0.1
81 electrode name=source x=0
82 electrode name=drain x=1.4 y=0.2
83 electrode name=substrate backside
84
```

```
85
86 structure outfile=esdex03_0.str
87
88 tonyplot esdex03_0.str -set esdex03_0.set
89
90
91 go atlas
92 # ESD ELECTROTHERMAL TRANSIENT SIMULATION
93 # HBM TEST TRANSIENT characteristics
94
95 material taup0=1e-7 taun0=1e-7
96 contact name=gate n.poly
97 #
98 models cvt srh auger bgn lat.temp
99 impact selb
100 thermcontact num=1 y.min=1.49 y.max=1.51 ext.temp=300 alpha=1000
101
102 # Current boundary conditions
103 contact name=drain current
104
105 method newton
106 output j.tot e.field
107
108 #setup quantities to monitor during simulation
109 #results go into the log file
110
111 # vertical field across gate oxide
112 probe x=0.98 y=0.21 field dir=90 name=OxideField
113 # temperature at drain metal contact
114 probe x=1.25 y=0.22 lat.temp name=MetalTemp
115
116 solve
117
118 log      outf=esdex03.log master
119
120
121 solve    idrain=5.0e-3 ramptime=10.e-9 tstep=2.0e-11 tstop=10.e-9
122 save    outf=esdex03.str
123 solve    idrain=0 decay=150e-9 tstop=15e-6
124
125
126 tonyplot esdex03.log -set esdex03_log.set
127 tonyplot esdex03.str -set esdex03_1.set
```

128

129 quit

8.1.4. esdex04.in: HBM in a MOSFET with Energy Balance Models

Requires: SSUPREM4/S-PISCES/GIGA

In this example, transient simulation of Electrostatic Discharge (ESD) on an NMOS transistor using the Human Body Model (HBM) is performed. During the ESD event, significant local heating is produced. The solution of local lattice temperature is included. Since this is a short channel MOSFET, significant non-local effects are present. The energy balance (EB) models are also used. This example shows:

- formation of a MOS structure in ATHENA
- interface to ATLAS
- selection of lattice heat flow models
- selection of energy balance models
- use of current boundary conditions and non-linear transient pulse to simulate a HBM ESD event.
- analysis of both the temperature distribution in the device and non-isothermal IV curve.

In most respects, except for the use of energy balance models, this example is the same as the previous example. The device structure and grid are slightly different. The parameter, `init spac.mult=2`, is used in ATHENA to reduce the CPU time. For more accurate simulation `spac.mult=1` would be required.

To select the energy balance models for electrons, the parameter, `hcte.el`, is used. In many cases it is necessary to optimize the numerical methods used in combined lattice heating and energy balance simulations. Here, `newton` is used. However, `block newton` is a more robust alternative for difficult cases.

To load and run this example, select the **Load example** button while this text is displayed. Once loaded into DECKBUILD, select the **run** button to execute the commands. Several support files will also be copied to your home directory at the time of loading.

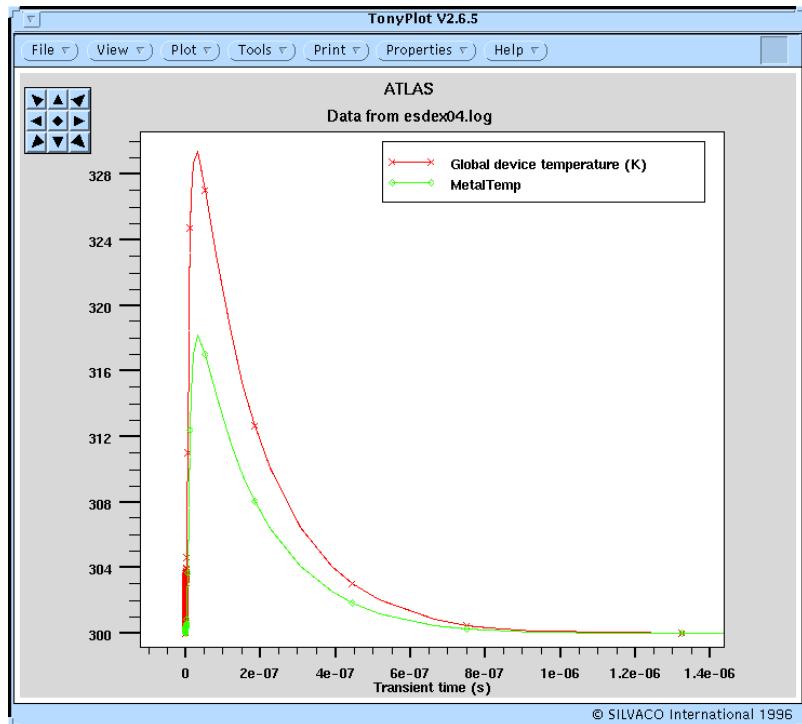


Figure 8.13: Comparison of Peak and Metal temperature during an HBM ESD transient

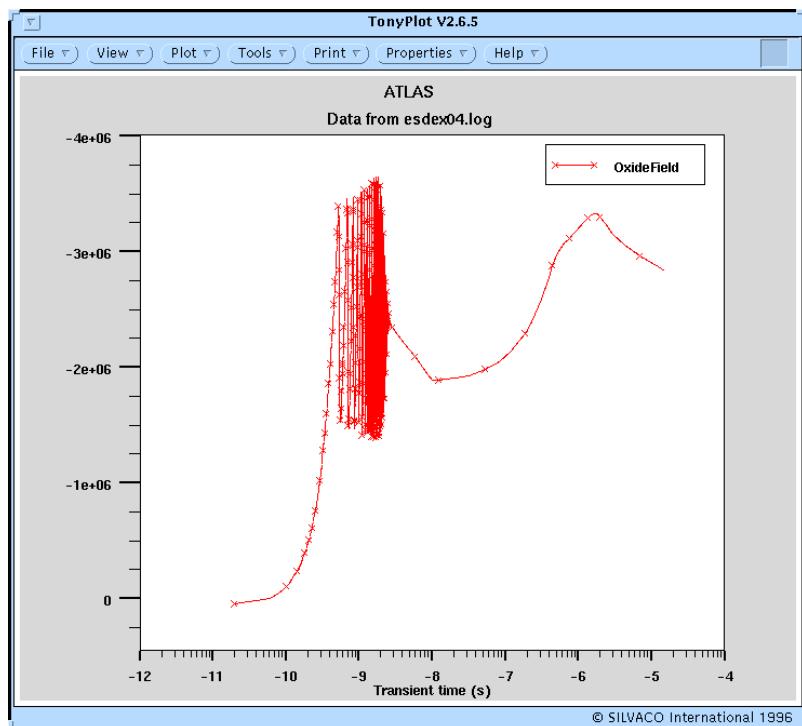


Figure 8.14: Electric field in the gate oxide during the ESD transient. Once a critical value is exceeded, the gate oxide will rupture.

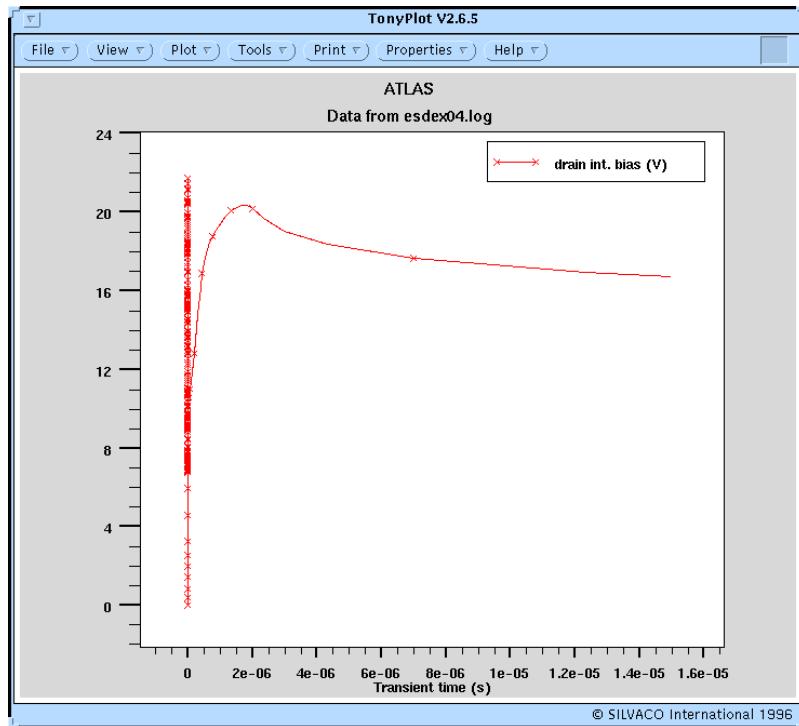


Figure 8.15: Drain bias during the HBM ESD transient

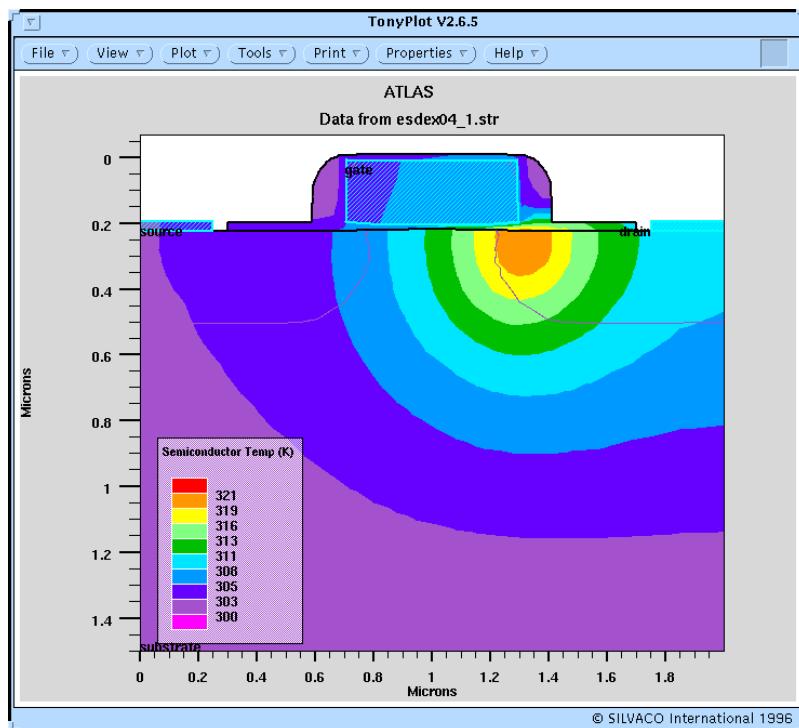


Figure 8.16: Display of Hot Spot in a MOSFET during an ESD transient

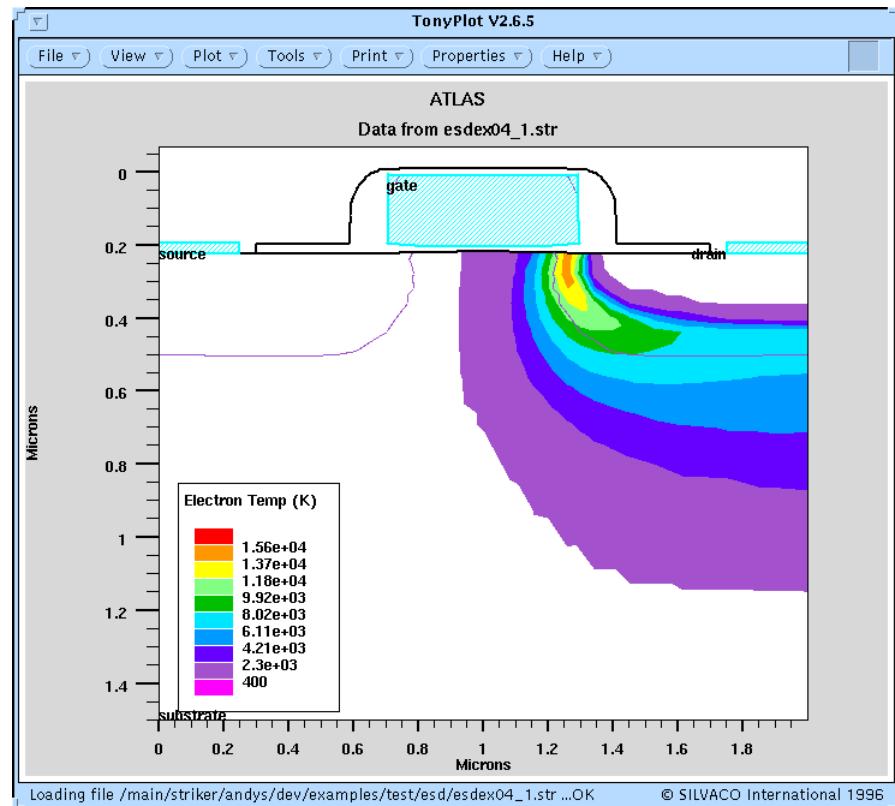


Figure 8.17: Energy Balance Models were used to accurately predict the breakdown behavior of the MOSFET. This plot shows electron temperature (energy) within the device

Input File esd/esdex04.in:

```

1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.7 spac=0.02
5 line x loc=1 spac=0.05
6 #
7 line y loc=0.00 spac=0.05
8 line y loc=0.2 spac=0.02
9 line y loc=0.4 spac=0.02
10 line y loc=0.8 spac=0.1
11 line y loc=1.5 spac=0.25
12 #
13 init orientation=100 phos conc=1e14 space.mult=2
14 #
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #

```

```
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=5.0e12 energy=100 pears
24 #
25 diffus temp=950 time=100 weto2 hcl=3
26 #
27 #N-well implant not shown -
28 #
29 # welldrive
30 diffus time=220 temp=1200 nitro press=1
31 #
32 etch oxide all
33 #
34 #sacrificial "cleaning" oxide
35 diffus time=20 temp=1000 dryo2 press=1 hcl=3
36 #
37 etch oxide all
38 #
39 #gate oxide grown here:-
40 diffus time=13 temp=950 dryo2 press=1.00 hcl=3
41 extract name="gate tox" thickness oxide mat.occno=1 x.val=1
42 #
43 #vt adjust implant
44 implant bf2 dose=1.3e12 energy=35 pearson
45 #
46 depo poly thick=0.20 div=3
47 #
48 etch poly left p1.x=0.7
49 #
50 relax y.min=0.8
51 method fermi compress
52 diffuse time=5 temp=900 weto2 press=0.8
53 extract name="sidewall tox" thickness oxide mat.occno=1 y.val=0.1
54 #
55 implant phosphor dose=3.0e13 energy=50 pearson
56 #
57 depo oxide thick=0.10 divisions=5
58 #
59 etch oxide dry thick=0.10
60 #
61 implant arsenic dose=5.0e15 energy=50 pearson
```

```
62 #
63 #
64 method fermi compress
65 diffuse time=5 temp=950 nitro press=1.0
66 #
67 structure outf=half.str
68
69 # extract final S/D Xj
70 extract name="s/d xj" xj silicon mat.occno=1 x.val=0.05 junc.occno=1
71 extract name="s/d rho" sheet.res silicon mat.occno=1 x.val=0.05 re-
    gion.occno=1
72 extract name="1d vt" 1dvt vb=0.0 x.val=0.95
73
74 #
75 etch oxide left p1.x=0.3
76 deposit alumin thick=0.03 div=2
77 etch alumin right p1.x=0.25
78 structure mirror right
79
80 electrode name=gate x=1 y=0.1
81 electrode name=source x=0
82 electrode name=drain x=2 y=0.2
83 electrode name=substrate backside
84
85
86 structure outfile=esdex04_0.str
87
88 tonyplot esdex04_0.str -set esdex04_0.set
89
90
91 go atlas
92 # ESD ELECTROTHERMAL TRANSIENT SIMULATION
93 # HBM TEST TRANSIENT characteristics
94 # Current pulse 1.0A (1.0/100 micron=1.0e-2 A/um)
95 # Current ramp-time: 10 ns
96 # Electrodes #1 - Gate; #2 - Source; #3 -Drain #4 -Substrate
97
98 mater taup0=1e-7 taun0=1e-7
99 contact name=gate n.poly
100 #
101 models cvt srh auger bgn lat.temp hcte.el
102 impact selb
103 thermcontact num=1 elec=4 ext.temp=300
```

```

104 #
105 solve init
106
107 # Current boundary conditions
108 contact name=drain current
109 method trap newton
110 solve prev
111 output j.tot e.field
112
113 # vertical field across gate oxide
114 probe x=1.25 y=0.21 field dir=90 name=OxideField
115 # temperature at drain metal contact
116 probe x=1.75 y=0.22 lat.temp name=MetalTemp
117
118 log      outf=esdex04.log
119
120
121 solve idrain=5.0e-4 ramptime=10.e-9 tstep=2.0e-11 tstop=10.e-9
122 save outf=esdex04_1.str
123 solve idrain=0 decay=150e-9 tstep=1.e-9 tstop=15e-6
124
125 tonyplot esdex04.log -set esdex04_log.set
126 tonyplot esdex04_1.str -set esdex04_1.set
127 quit

```

8.1.5. esdex05.in: Second Breakdown of a MOSFET

Requires: ATHENA/S-PISCES/GIGA

In this example, the steady state second breakdown simulation of an NMOS transistor was performed. Second breakdown analysis is an important figure of merit in the understanding of the resistance of devices to high current (voltage) stress caused by the ESD events. This example shows:

- formation of a MOS structure in ATHENA
- interface to ATLAS
- selection of lattice heat flow models
- analysis of a non-isothermal IV curve

The MOS structure is constructed using ATHENA process simulation. This structure is passed to ATLAS for HBM test simulation. The NMOS transistor is a 0.8um LDD device using oxide spacers. For a more complete description of the MOS process simulation, see the MOS examples.

The ATLAS syntax shows a simple and effective procedure for the tracing of the complicated S-shape I-V characteristics that could be used with any initial NMOS structure.

The ATLAS simulation begins with the definition of the models and material parameters of the device. The contact statement is used to define the workfunction of the polysilicon electrode. The material statement is used to define the electron and hole lifetimes in semiconductor.

The physical models used in this simulation reflect the different physical effects important to electrothermal device simulation. The mobility model CVT includes the concentration, electric field and temperature dependencies as well as a surface mobility degradation effects. In addition to the Shockley-Read-Hall recombination model(SRH), the recombination model AUGER is included to take into account the high injection level effects. Band gap narrowing is taken into account by means of the BGN parameter. The continuity equations for both carriers are selected by default or by using parameter, `carriers=2` in the `method` statement. Impact ionization is necessary for any breakdown simulation and it is also included here.

A nonisothermal approach is used, which means that the heat flow equation is solved in addition to the semiconductor equations and all physical parameters become temperature dependent. The syntax, `models lat.temp`, enables the solution of the heat flow equation.

In all nonisothermal simulations, the definition of the thermal boundary conditions is very important. Thermal boundary conditions are defined in the `thermcontact` statement. A value of the thermal conductance determined from the heat conductivity of the substrate is specified at the thermoccontact located along the substrate. Where no thermal contacts are specified thermal isolation is assumed. Here thermal isolation conditions are assumed on the all other surfaces besides the bottom.

To simulate the device second breakdown the curve tracing algorithm was used. For more details of this algorithm and its syntax see the snapback example in the Advanced MOS section.

The steady state current/voltage characteristics are saved in a LOG file. Using TONYPLOT, it is possible to observe the maximum temperature in the device versus current/voltage. The sharp decrease of the voltage on the nonisothermal I-V curve shows the onset of second breakdown.

To load and run this example, select the **Load example** button while this text is displayed. Once loaded into DECKBUILD, select the **run** button to execute the commands. Several support files will also be copied to your home directory at the time of loading.

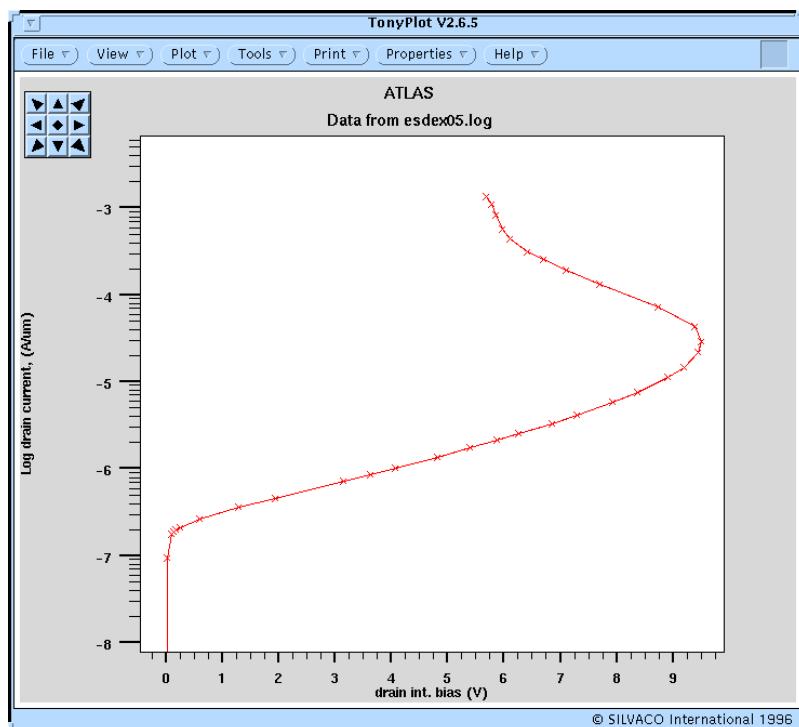


Figure 8.18: MOS snapback and breakdown. These DC tests provide important insight into ESD protection using MOSFETs

Input File esd/esdex05.in:

```
1 go athena
2 #
3 line x loc=0 spac=0.1
4 line x loc=0.7 spac=0.02
5 line x loc=1 spac=0.05
6 #
7 line y loc=0.00 spac=0.05
8 line y loc=0.2 spac=0.02
9 line y loc=0.4 spac=0.02
10 line y loc=0.8 spac=0.1
11 line y loc=1.5 spac=0.25
12 #
13 init orientation=100 phos conc=1e14 space.mult=1
14 #
15 #pwell formation including masking off of the nwell
16 #
17 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
18 #
19 etch oxide thick=0.02
20 #
21 #P-well Implant
22 #
23 implant boron dose=5.0e12 energy=100 pears
24 #
25 diffus temp=950 time=100 weto2 hcl=3
26 #
27 #N-well implant not shown -
28 #
29 # welldrive
30 diffus time=220 temp=1200 nitro press=1
31 #
32 etch oxide all
33 #
34 #sacrificial "cleaning" oxide
35 diffus time=20 temp=1000 dryo2 press=1 hcl=3
36 #
37 etch oxide all
38 #
39 #gate oxide grown here:-
40 diffus time=13 temp=950 dryo2 press=1.00 hcl=3
41 extract name="gate tox" thickness oxide mat.occcno=1 x.val=1
42 #
```

```
43 #vt adjust implant
44 implant bf2 dose=1.3e12 energy=35 pearson
45 #
46 depo poly thick=0.20 div=3
47 #
48 etch poly left p1.x=0.7
49 #
50 relax y.min=0.8
51 method fermi compress
52 diffuse time=5 temp=900 weto2 press=0.8
53 extract name="sidewall tox" thickness oxide mat.occno=1 y.val=0.1
54 #
55 implant phosphor dose=3.0e13 energy=50 pearson
56 #
57 depo oxide thick=0.10 divisions=5
58 #
59 etch oxide dry thick=0.10
60 #
61 implant arsenic dose=5.0e15 energy=50 pearson
62 #
63 #
64 method fermi compress
65 diffuse time=5 temp=950 nitro press=1.0
66 #
67 structure outf=half.str
68
69 # extract final S/D Xj
70 extract name="s/d xj" xj silicon mat.occno=1 x.val=0.05 junc.occno=1
71 extract name="s/d rho" sheet.res silicon mat.occno=1 x.val=0.05 re-
    gion.occno=1
72 extract name="1d vt" ldvt vb=0.0 x.val=0.95
73
74 #
75 etch oxide left p1.x=0.3
76 deposit alumin thick=0.03 div=2
77 etch alumin right p1.x=0.25
78 structure mirror right
79
80 electrode name=gate x=1 y=0.1
81 electrode name=source x=0
82 electrode name=drain x=2 y=0.2
83 electrode name=substrate backside
84
```

```
85
86 structure outfile=esdex05_0.str
87
88 tonyplot esdex05_0.str -set esdex05_0.set
89
90
91
92
93
94 go atlas
95
96 mater region=1 taup0=1e-7 taun0=1e-7
97 contact num=1 n.poly
98 #
99 models cvt srh auger bgn lat.temp
100 impact selb
101 #
102 # Thermal boundary conditions
103 #
104 thermcontact num=1 y.min=1.5 y.max=1.5 ext.temp=300 alpha=1000
105
106 method newton trap
107 curvetrace end.val=1.2e-3 contr.name=drain curr.cont mincur=1e-13 \
108         nextst.ratio=1.5 step.init=0.05
109
110 solve init
111
112 #ramp gate to 0.6V
113 solve vgate=0.2 vstep=0.2 vfinal=0.6 name=gate
114
115 #ramp drain
116
117 log outf=esdex05.log master
118
119 solve curvetrace
120
121 tonyplot esdex05.log -set esdex05_log.set
122
123 quit
```

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9.1. POWER: Power Device Application Examples

9.1.1. powerex01.in: Reverse Recovery of a Power Diode

Requires: S-PISCES, MIXEDMODE

This example demonstrates the reverse recovery of a silicon power diode. It shows:

- Structure definition using ATLAS
- The SPICE-like command syntax for simulating MIXEDMODE circuits
- Steady state and transient analysis of a power diode

The structure consists of a rectangular silicon power diode. ATLAS is used to define the power diode structure including mesh, materials, electrodes, and doping. The `mesh rect` statement defines a rectangular mesh with grid lines at the locations specified by the `x.m` and `y.m` statements. The entire mesh is defined as one silicon region using the `region` statement. Electrodes are defined on top and bottom and the `doping` statement is used to define a uniform background concentration and gaussian n-type and p-type regions. This structure is saved and will be used as a device by MIXEDMODE.

In this simulation, the MIXEDMODE circuit simulator uses ATLAS to calculate the electrical characteristics of the power diode under the specified circuit conditions. First, a steady-state simulation of the power diode circuit is performed.

The `.begin` and `.end` statements indicate the beginning and end of the MIXEDMODE syntax. The MIXEDMODE commands are similar to those used in SMARTSPICE. Circuit components, topology, and analysis are defined within. In general, the circuit component definition consists of three parts: the type of component, the lead or terminal node assignments, and the component value or model name. For example, the first component definition in this simulation is a dc voltage source. `v1` defines the component as voltage source number one, `1` and `0` are the two circuit nodes for this component, and `1000` indicates that the voltage source value is 1000 volts. The remaining circuit components are resistors `r1 r2`, inductor `l1` and independent current source `i1`. The `adiode` statement specifies a device to be analyzed by ATLAS. The `a` part of the `adiode` command specifies that this is a device statement. The `diode` portion simply defines the device name. The option `infile=` indicates which device structure file is to be used. The `.nodeset` statement defines the initial values for node voltages and the `.save outfile=` statement saves the result to the indicated file. Since this is the steady state solution, no output log data file is needed. Additionally, the `.options` command sets the solution method to a modified two-level Newton using the `m2ln` parameter. Other command line options exist. Please refer to the MIXEDMODE section of the ATLAS User's manual for a complete list.

To completely specify the simulation, the physical models used by ATLAS must be specified. The `model` statement is used to turn on the appropriate transport models. This set includes `conmob`: the concentration dependent mobility model, `fldmob`: the lateral electric field-dependent mobility model, `consrh`: Shockley-Read-Hall recombination using concentration dependent lifetimes, `auger`: recombination accounting for high level injection effects, and `bgn`: band gap narrowing. Refer to the ATLAS User's manual for a description of these models. The `material` statement is used to override default material parameters. In this case, the carrier recombination fixed lifetimes are set. Finally, an impact ionization model is enabled using the `impact` statement with the `selb` option. This specifies that the Selberherr impact ionization model is to be used.

The next step is the transient analysis which is specified in a similar manner. The reverse recovery of the diode is simulated by dropping the value of output resistor `r2` over a small increment of time. The `r2` statement contains additional syntax to perform this task. Here, the resistor is treated as a

source whose resistance decreases exponentially from 1 M Ω to 1 m Ω over the specified time step. This action essentially shorts out the parallel current source i1 which is also connected to the base of the diode. The .trans statement is used to specify the time stepping parameters for the transient analysis. In addition, the .log statement saves the diode output characteristics over the time interval specified. TONYPLOT plots the transient reverse recovery of the power diode.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

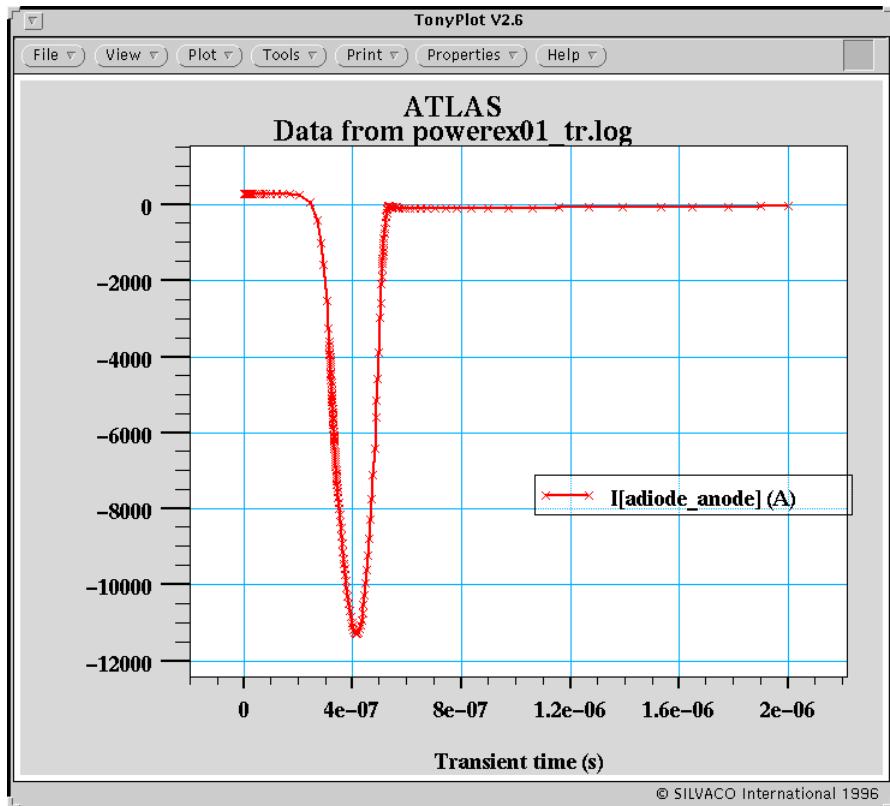


Figure 9.1: Diode current during transient reverse recovery

Input File power/powerex01.in:

```

1 go atlas
2 mesh      nx=2 ny=120 outf=powerex01.str master.out
3 x.m      n=1    l=0.0      r=1.0
4 x.m      n=2    l=10.0     r=1.0
5 y.m      n=1    l= 0.0     r=1.0
6 y.m      n=15   l=35.0     r=1.
7 y.m      n=110  l=350.0    r=1.
8 y.m      n=120  l=370.0    r=1.0
9 #
10 #
11 region   num=1 silicon
12 #

```

```
13 elec      num=1 top name=cathode
14 elec      num=2 bottom name=anode
15 #
16 # Impurity profile
17 #
18 doping uniform conc=1.e14    n.type
19 doping gauss conc=2.e19 n.type char=7
20 doping gauss conc=2.e19 p.type peak=370 junc=350
21
22 go atlas
23 .begin
24 #
25 # Steady-state simulation of circuit with power diode
26 #
27 v1 1 0  1000.
28 r1 1 2  1m
29 l1 2 3  3nH
30 adiode 3=cathode 4=anode width=5.e7 infile=powerex01.str
31 r2 4 0  1mg
32 i1 0 4  300.
33 #
34 .nodeset v(1)=1000. v(2)=1000. v(3)=1000. v(4)=1000.5
35 .numeric toldc=1.e-9 vchange=0.1
36 #
37 .save outfile=powerex01_save
38 .options m2ln print
39 .end
40 #
41 #
42 models device=adiode reg=1 conmob fldmob consrh auger bgn
43 material device=adiode reg=1 taun0=5e-6 taup0=2e-6
44 #
45 impact device=adiode reg=1 selb
46
47 go atlas
48 .begin
49 #
50 # Reverse recovery of power diode
51 #
52 v1 1 0  1000.
53 r1 1 2  1m
54 l1 2 3  3nH
55 adiode 3=cathode 4=anode width=5.e7 infile=powerex01.str
```

```
56 r2 4 0 1mg EXP 1mg 1e-3 0. 20ns 10 200
57 i1 0 4 300
58 #
59 .numeric lte=0.3 toltr=1.e-5 vchange=10.
60 .options print relpot write=10
61 #
62 .log outfile=powerex01
63 .load infile=powerex01_save
64 .save master=powerex01
65 #
66 .tran 0.1ns 2us
67 #
68 .end
69 #
70 #
71 #
72 models device=adiode reg=1 commob fldmob consrh auger bgn
73 material device=adiode reg=1 taun0=5e-6 taup0=2e-6
74 impact device=adiode reg=1 selb
75 #
76
77 #
78
79 go atlas
80 tonyplot powerex01_tr.log -set powerex01.set
81
82 quit
```

9.1.2. powerex02.in: Vertical DMOS Turn-on Characteristics

Requires: SSUPREM4, S-PISCES, GIGA

This example demonstrates fabrication and electrical analysis of a vertical DMOS structure. It shows:

- DMOS process flow to generate the device structure using ATHENA
- Model setup for non-isothermal device simulation using GIGA
- ATLAS methodology for simulating the DMOS device gate characteristics

The structure generated by ATHENA is a silicon vertical DMOS device. A phosphorus doped silicon substrate and underlying mesh are defined. A lightly phosphorus doped silicon epitaxial layer is then grown using the epitaxy command. The gate material is deposited, patterned and etched. Boron is implanted and diffused to form the right edge of channel region under the gate. The source region arsenic implant is performed and diffused to complete the channel definition. Aluminum is deposited and etched to form the source contact. The source, drain and gate electrodes are defined by using the electrode statement and by including the name and location of the contact on the command line. Notice that the drain electrode location is defined by the electrode command line

option backside. Now that the structure has been completed, the ATLAS device test can be performed.

In this simulation, the structure created by ATHENA will be automatically loaded into ATLAS when the command, `go atlas`, is reached. The `contact` statement sets the workfunction for the gate to that of degenerately doped n-type polysilicon. Next, the `models` statement sets the physical transport and associated models to be used, in this case, `conmob`: concentration dependent mobility, `fldmob`: lateral electric field dependent mobility, `srh`: Shockley-Read-Hall recombination, and most importantly for power devices `lat.temp`: non-isothermal transport using GIGA. The thermal boundary condition for the source contact is defined by the `thermcontact` statement.

The gate characteristics of this DMOS device are calculated by solving the transport and thermal equations at the bias specified in the `solve` statements. Here, the drain bias is stepped to 20 volts. Next, an output logfile is opened using the `log` command, and the gate contact is ramped from 0.25 volts to 20 volts in two stages. It is advisable to use smaller bias steps initially. Larger bias steps can then be used for the remaining bias range. TONYPLOT plots the gate characteristics from the log file. To plot the structure and solution at the final bias point, highlight the name, `powerex02_2.str` on the `save` command line and click left 'Tools' at the top right of the DECK-BUILD window.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

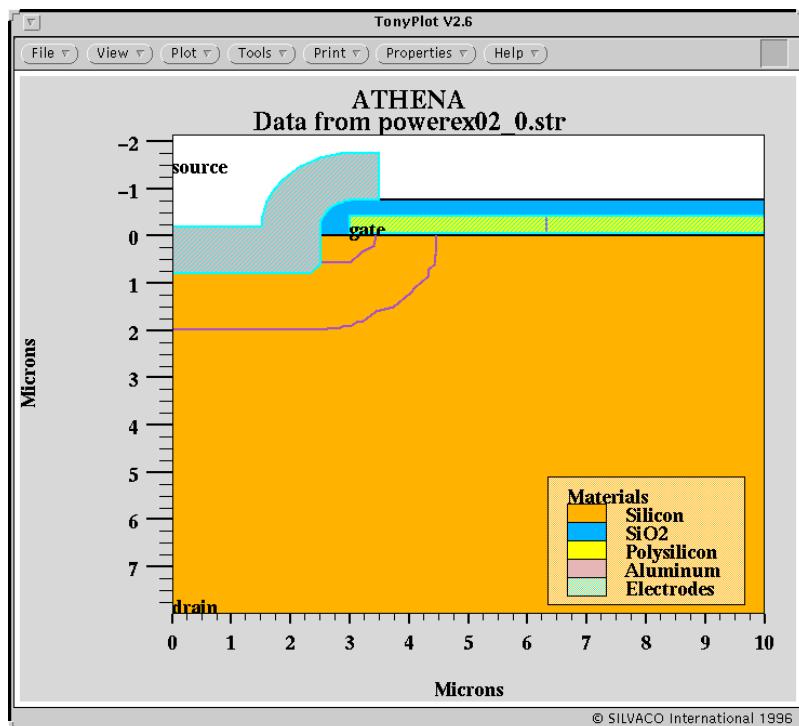


Figure 9.2: DMOS structure simulated using ATHENA

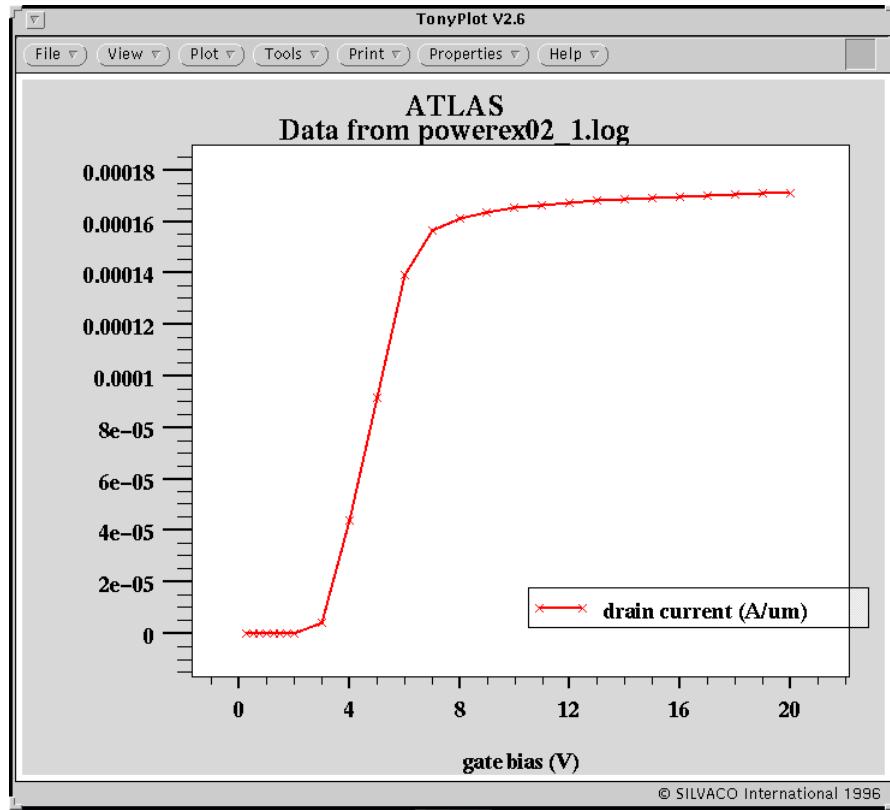


Figure 9.3: threshold Voltage extraction for DMOS power transistor

Input File power/powerex02.in:

```

1 go athena
2 #
3 line x loc=0.00 spac=0.25
4 line x loc=3.00 spac=0.10
5 line x loc=10.00 spac=1.0
6 #
7 line y loc=7.00 spac=0.5
8 line y loc=8.00 spac=0.5
9 #
10 init c.phosphor=1.0e18 orientation=100 space.mult=2
11 #
12 epitaxy time=10 temp=1200 thickness=7 divisions=15 \
13      dy=0.10 ydy=0.00 phosphorus conc=1.0e15
14
15 deposit oxide thickness=0.06
16 deposit poly thickness=0.35 div=3
17 deposit oxide thickness=0.35 div=3
18 deposit photores thickness=1 div=3
19

```

```
20
21 etch photores p1.x=3 left
22 etch oxide p1.x=3 left
23 etch poly p1.x=3 left
24 etch oxide p1.x=3 left
25
26 implant boron dose=1e14 energy=80
27
28 etch photores all
29
30 diffuse time=100 temp=1100
31
32 implant arsenic dose=3e15 energy=100
33 diffuse time=20 temp=1100
34
35
36 deposit oxide thickness=0.5 div=4
37 etch oxide thickness=0.5
38
39 etch start x=0 y=-0.1
40 etch cont x=0 y=0.8
41 etch cont x=2.5 y=0.8
42 etch done x=2.5 y=-0.1
43
44 diffuse time=1 temp=1100
45
46 deposit alum thickness=1 div=8
47 etch alum right p1.x=3.5
48
49 electrode name=source x=0
50 electrode name=gate x=5 y=-0.2
51 electrode name=drain backside
52
53 structure outfile=powerex02_0.str
54
55 tonyplot powerex02_0.str -set powerex02_0.set
56
57 go atlas
58
59 contact name=gate n.poly
60
61 models commob fldmob srh lat.temp
62 output flowlines
```

```
63
64 thermcontact num=1 name=source temp=300
65
66
67 method newton autonr trap
68 solve init
69 solve vdrain=10
70 solve vdrain=20
71 log outf=powerex02_1.log
72 solve vstep=0.25 vfinal=2 name=gate
73 solve vstep=1      vfinal=20 name=gate
74 save outf=powerex02_2.str
75
76 tonyplot powerex02_1.log -set powerex02_1.set
77
78 quit
```

9.1.3. powerex03.in: IGBT Transient Latch-up with Lattice Heating

Requires: S-PISCES, GIGA

The non-isothermal latchup of an IGBT device is simulated. The latchup is produced in the transient or switching mode. The currents during latchup in this device are high and significant local heating occurs. Therefore, the solution of lattice temperature and heat flow must be included. This example shows:

- The definition of the IGBT structure using ATLAS
- How to enable GIGA non-isothermal simulation
- IGBT collector steady state solution at 300V
- transient gate voltage ramp to produce latchup

The ATLAS simulation begins with the definition of the IGBT structure. A fine rectangular mesh is first defined. Once this is done, the `eliminate` statement is used to remove unnecessary grid lines. Next, the materials are assigned to specific regions using the `region` command. The electrodes and doping profiles are then defined. Additionally, specific characteristics of these materials, their electrodes and the charge carriers within can be modified. The `material` statement is used to define the electron and hole recombination lifetimes in the semiconductor. The `contact` statement defines the workfunction of the polysilicon electrode, in this case, that of degenerately doped n-type polysilicon. This completes the IGBT structure definition.

For any ATLAS device simulation, the physical transport models must be enabled using the `models` statement. In this case, they reflect the different physical effects important to the IGBT device.

They are:

- `analytic`: analytic concentration dependent mobility
- `fldmob`: lateral electric field dependent mobility
- `surfmob`: surface mobility degradation

- srh: Shockley-Read-Hall recombination and
- auger: recombination accounting for high level injection effects.

The steady-state characteristics of the IGBT are now solved. As with most ATLAS simulations, an initial solution is performed at zero bias using the statement `solve init`. This gives the ATLAS solvers a good starting point. The subsequent `solve` statements ramp the IGBT collector up to 300V in several stages. Each additional stage uses the previous solution as an initial guess. Other initial guess strategies are available however. Consult the ATLAS User's manual for more details. If an electrode bias is not specified, it remains at its previous value; in this case, zero volts. After the solution is obtained at 300V, the solution is saved. It will be used as the initial solution in the transient mode latchup simulation which follows.

Three additional items are added for the IGBT transient mode simulation: thermal contacts, heat flow, and impact ionization. Thermal boundary conditions are a very important part of any non-isothermal simulation and must be specified. For the IGBT, a constant temperature along the collector contact is specified in the `thermcontact` statement. All other contacts and surfaces are assumed to be in thermal isolation. The `lat.temp` lattice temperature model is added to the `model` statement to include heat flow. This means that the heat flow equation is solved in addition to the semiconductor equations and all physical parameters become temperature dependent. In addition to heat flow, impact ionization plays an important role in IGBT transient mode latchup. The Selberherr impact ionization model is added using the `impact` statement with the `selb` option.

An IGBT gate transient is now simulated. The previous solution at the collector bias of 300V is loaded and used as an initial guess for the latchup simulation. The `output` statement is used to add additional solution quantities to the standard output variables. The gate voltage is ramped from 0 to 10 V in 100 nano seconds to cause the IGBT latchup. The gate will then be held at the 10 V level until the time reaches 1 micro second. These conditions are set on the `solve` statement. The output results are saved in the log file. Using TONYPLOT it is possible to observe the latchup by plotting the collector current and maximum temperature in the device versus time. The structure and solution at the final time point is saved and all output variables can be observed using TONYPLOT.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

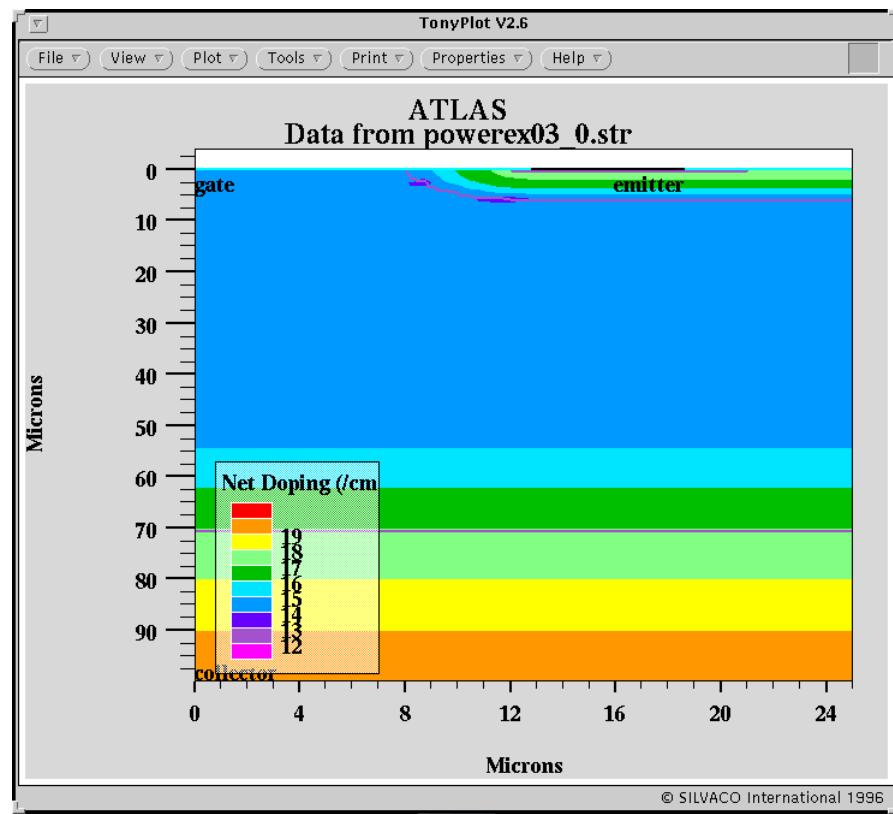


Figure 9.4: Doping and Junctions of an IGBT defined using ATLAS syntax

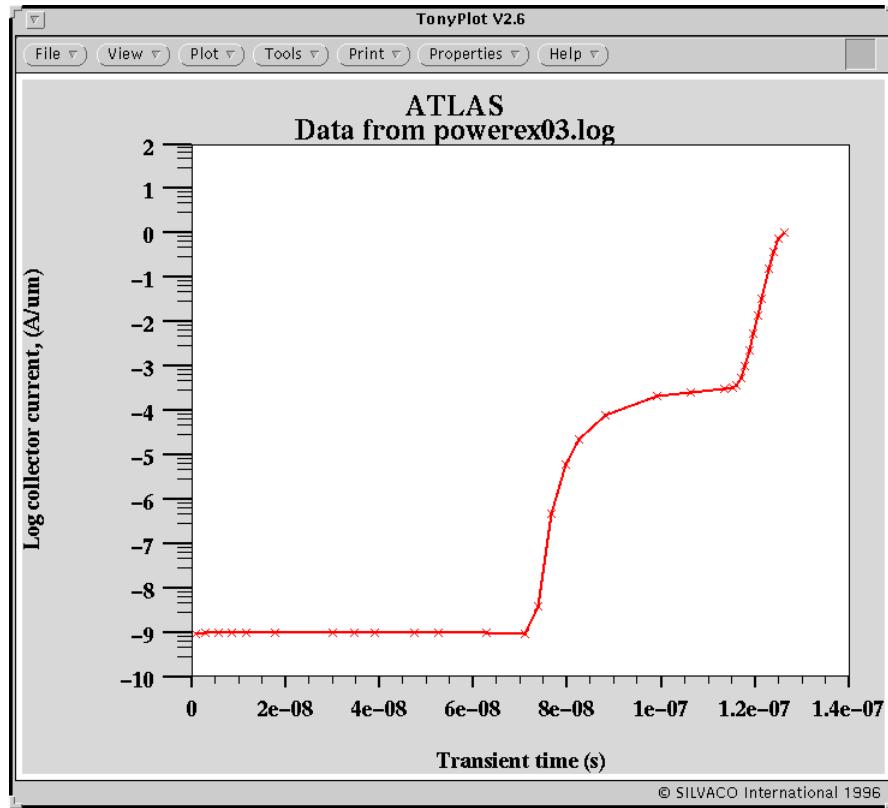


Figure 9.5: Latchup transient for the IGBT. The device latches at 12us due to gate turn-on pulse

Input File power/powerex03.in:

```

1 go atlas
2 TITLE: IGBT LATCHUP SIMULATION
3 # Silvaco International 1992,1993.1994
4 # IGBT steady state output characteristics
5 # Save the solution at Vce=300 V
6
7 mesh      nx=25 ny=49
8 x.m      n=1    l=0.0     r=1.00
9 x.m      n=13   l=12.0    r=0.95
10 x.m     n=25   l=25.0    r=1.05
11 y.m      n=1    l=-0.08   r=1.0
12 y.m      n=3    l=0.0     r=1.0
13 y.m      n=9    l=0.6     r=1.0
14 y.m      n=25   l=8.0     r=1.05
15 y.m      n=27   l=10.0    r=1.0
16 y.m      n=32   l=20.0    r=1.05
17 y.m      n=41   l=60.0    r=1.10
18 y.m      n=45   l=80.0    r=0.95
19 y.m      n=49   l=100     r=0.95

```

```
20 #
21 eliminate rows ix.l=1 ix.h=25 iy.l=4 iy.h=49
22 eliminate rows ix.l=1 ix.h=25 iy.l=25 iy.h=49
23 eliminate columns ix.l=1 ix.h=25 iy.l=31 iy.h=49
24 #
25 region      num=1 y.max=0.0    oxide
26 region      num=2 y.min=0.0    silicon
27
28 #   electrodes #1 - gate; #2 - emitter #3 - collector
29
30 elec        num=1 left  y.min=-0.08  length=13.0 name=gate
31 elec        num=2 right y.min=0.0    y.max=0.0 length=6.8  name=emitter
32 elec        num=3 bottom name=collector
33
34 #   impurity profile
35 doping      uniform conc=1.5e14 n.type
36 doping      uniform conc=1.0e19 p.type    y.t=81.4 y.b=100
37 doping      uniform conc=1.0e17 n.type    y.t=65.0 y.b=81.4
38 doping      gauss conc=2.7e17 p.type junc=5.8 x.l=13   ratio=0.8
39 doping      gauss conc=9.3e19 n.type junc=0.4 x.l=13 x.r=20 ratio=0.8
40
41 save outf=powerex03_0.str
42
43 tonyplot powerex03_0.str -set powerex03_0.set
44
45 mater      region=2 taup0=1e-6 taun0=1e-6
46 contact    num=1 n.poly
47
48 models     analytic srh auger fldmob surfmob
49
50 solve      init
51
52
53 method    newton trap
54
55
56 # Vce increased from 0.
57 solve      vcollector=0.5
58 solve      vcollector=1
59 solve      vcollector=5
60 solve      vcollector=10  vstep=10.0  vfinal=50 name=collector
61 solve      vcollector=75  vstep=25.0  vfinal=300 name=collector
62 save      outf=powerex03_1.str
```

```
63
64 go atlas
65
66 mesh      nx=25 ny=49
67 x.m      n=1   l=0.0    r=1.00
68 x.m      n=13  l=12.0   r=0.95
69 x.m      n=25  l=25.0   r=1.05
70 y.m      n=1   l=-0.08  r=1.0
71 y.m      n=3   l=0.0    r=1.0
72 y.m      n=9   l=0.6    r=1.0
73 y.m      n=25  l=8.0    r=1.05
74 y.m      n=27  l=10.0   r=1.0
75 y.m     n=32  l=20.0   r=1.05
76 y.m     n=41  l=60.0   r=1.10
77 y.m     n=45  l=80.0   r=0.95
78 y.m     n=49  l=100    r=0.95
79 #
80 eliminate rows ix.l=1 ix.h=25 iy.l=4 iy.h=49
81 eliminate rows ix.l=1 ix.h=25 iy.l=25 iy.h=49
82 eliminate columns ix.l=1 ix.h=25 iy.l=31 iy.h=49
83 #
84 region    num=1 y.max=0.0  oxide
85 region    num=2 y.min=0.0  silicon
86
87 # electrodes #1 - gate; #2 - emitter #3 - collector
88
89 elec      num=1 left  y.min=-0.08  length=13.0 name=gate
90 elec      num=2 right y.min=0.0   y.max=0.0  length=6.8  name=emitter
91 elec      num=3 bottom name=collector
92
93 # impurity profile
94 doping    uniform conc=1.5e14 n.type
95 doping    uniform conc=1.0e19 p.type    y.t=81.4 y.b=100
96 doping    uniform conc=1.0e17 n.type    y.t=65.0 y.b=81.4
97 doping    gauss conc=2.7e17 p.type junc=5.8 x.l=13   ratio=0.8
98 doping    gauss conc=9.3e19 n.type junc=0.4 x.l=13 x.r=20 ratio=0.8
99
100
101 mater   region=2 taup0=1e-6 taun0=1e-6
102 contact num=1 n.poly
103
104 thermcontact num=1 elec.num=3 temp=300
105
```

```
106 models analytic srh auger fldmob surfmob lat.temp
107 impact selb
108
109
110 method newton
111
112 # Solution at Vge=0 and Vce= 300.0 V is loaded
113 load    inf=powerex03_1.str master
114
115 solve   prev
116
117 output  flowlines jx.e jy.e jx.h jy.h
118
119 log     outf=powerex03.log
120 solve   v1=10.0 ramptime=100.e-9 tstep=1e-9 tstop=1.e-6 t.compl=1000
121
122 save outf=powerex03_2.str
123
124 tonyplot powerex03.log -set powerex03_log.set
125
126 end
```

9.1.4. powerex04.in: IGBT Ic/Vce Characteristics

Requires: S-PISCES

The Ic/Vce characteristics of an Insulated Gate Bipolar Transistor (IGBT) are simulated. This example shows:

- Creating the IGBT structure using ATLAS
- Ic / Vce test definition
- IGBT Ic versus Vce characteristics

The ATLAS simulation begins with the definition of the IGBT structure. ATLAS is used to define the IGBT structure including mesh, materials, electrodes, and doping. A fine rectangular mesh is first defined. Once this is done, the `eliminate` statement is used to remove unnecessary grid lines. Next the materials are assigned to specific regions using the `region` command. The electrodes and doping profiles are then defined. Additionally, specific characteristics of these materials, their electrodes and the charge carriers within can be modified. The `material` statement is used to define the electron and hole recombination lifetimes in the semiconductor. The `contact` statement defines the workfunction of the polysilicon electrode, in this case, that of degenerately doped n-type polysilicon. This completes the IGBT structure definition.

For any ATLAS device simulation, the physical transport models must be enabled using the `model` statement. In this case, they reflect the different physical effects important to the IGBT device. They are:

- `analytic`: analytic concentration dependent mobility
- `fldmob`: lateral electric field dependent mobility

- surfmob: surface mobility degradation
- srh: Shockley-Read-Hall recombination and
- auger: recombination accounting for high level injection effects.

IGBT output characteristics are simulated by sweeping the collector contact voltage for several discrete values of gate voltage. In this example, the collector voltage will be swept from 0 to 20 V for gate voltages of 5 and 10 V. This is accomplished by first obtaining a solution at each gate bias of interest with all other electrodes set to 0V. Next, each gate solution is used as the initial solution for a collector sweep. Output log files are saved for each gate-collector sweep combination. TONY-PLOT displays the IGBT I_c/V_{ce} family of curves by overlaying all output curves on one plot.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

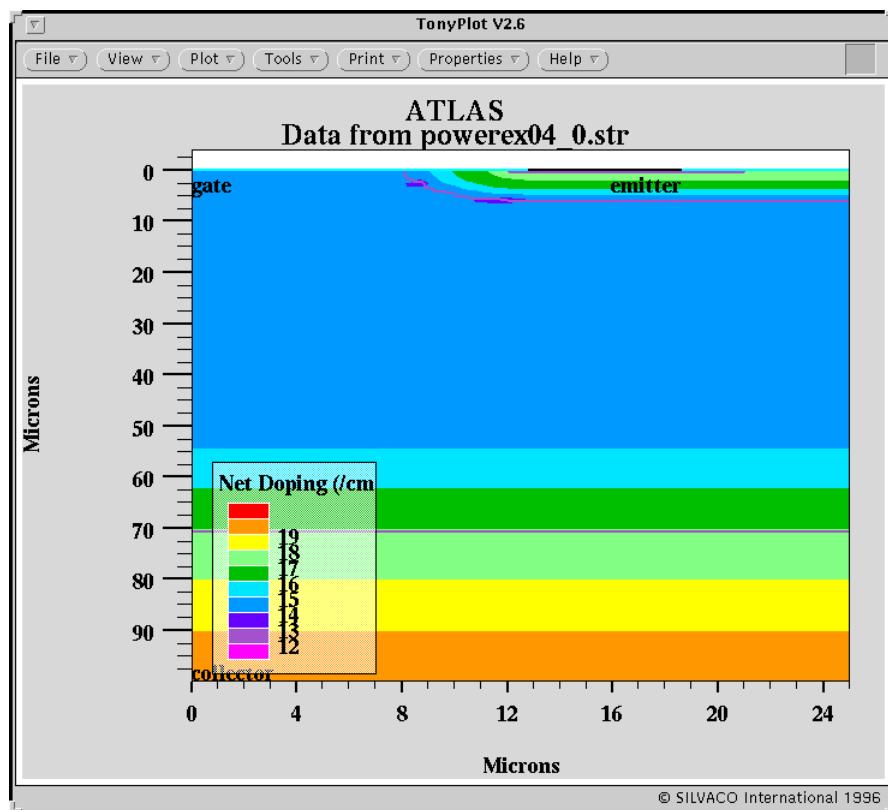
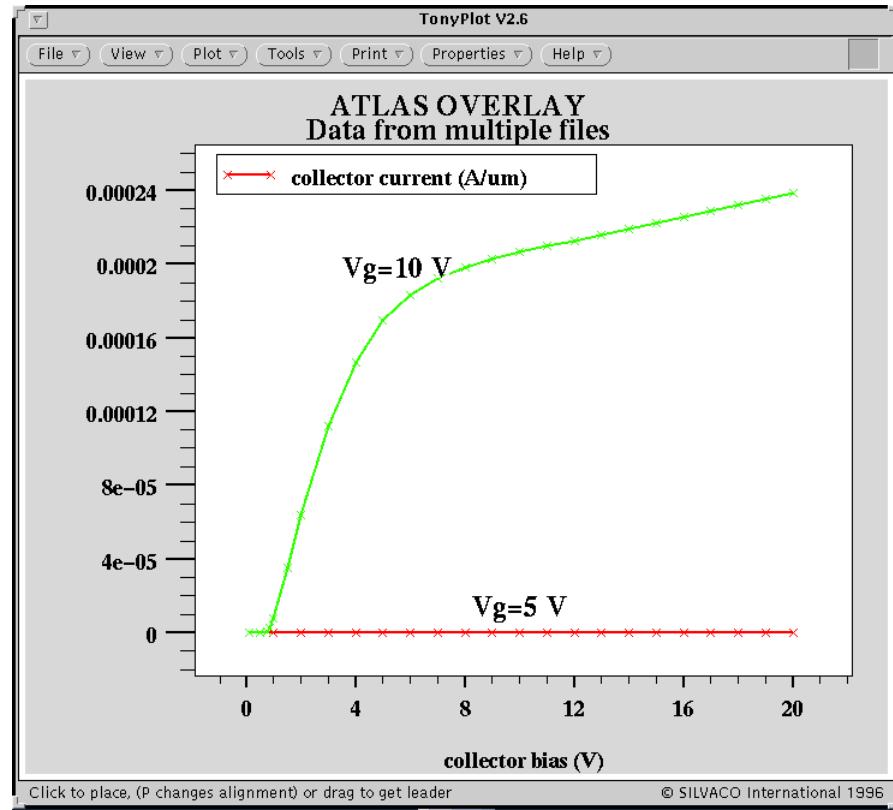


Figure 9.6: Doping and Junctions of an IGBT defined using ATLAS syntax

Figure 9.7: I_c/V_{ce} for an IGBT at two different gate voltages**Input File power/powerex04.in:**

```

1 go atlas
2 TITLE : IGBT steady state output characteristics
3
4 # Silvaco International 1994
5
6 mesh      nx=25 ny=49
7 x.m      n=1    l=0.0     r=1.00
8 x.m      n=13   l=12.0    r=0.95
9 x.m      n=25   l=25.0    r=1.05
10 y.m     n=1    l=-0.08   r=1.0
11 y.m     n=3    l=0.0     r=1.0
12 y.m     n=9    l=0.6     r=1.0
13 y.m     n=25   l=8.0     r=1.05
14 y.m     n=27   l=10.0    r=1.0
15 y.m    n=32   l=20.0    r=1.05
16 y.m    n=41   l=60.0    r=1.10
17 y.m    n=45   l=80.0    r=0.95
18 y.m    n=49   l=100     r=0.95
19 #

```

```
20 eliminate rows ix.l=1 ix.h=25 iy.l=4 iy.h=49
21 eliminate rows ix.l=1 ix.h=25 iy.l=25 iy.h=49
22 eliminate columns ix.l=1 ix.h=25 iy.l=31 iy.h=49
23 #
24 region      num=1 y.max=0.0    oxide
25 region      num=2 y.min=0.0    silicon
26
27 #   electrodes #1 - gate; #2 - emitter #3 - collector
28
29 elec        num=1 left  y.min=-0.08  length=13.0 name=gate
30 elec        num=2 right y.min=0.0   y.max=0.0 length=6.8  name=emitter
31 elec        num=3 bottom name=collector
32
33 #   impurity profile
34 doping      uniform conc=1.5e14 n.type
35 doping      uniform conc=1.0e19 p.type      y.t=81.4 y.b=100
36 doping      uniform conc=1.0e17 n.type      y.t=65.0 y.b=81.4
37 doping      gauss conc=2.7e17 p.type junc=5.8 x.l=13   ratio=0.8
38 doping      gauss conc=9.3e19 n.type junc=0.4 x.l=13 x.r=20 ratio=0.8
39
40
41 save outf=powerex04_0.str
42
43 tonyplot powerex04_0.str -set powerex04_0.set
44
45
46
47 mater      region=2 taup0=1e-6 taun0=1e-6
48 contact    num=1 n.poly
49
50 models     analytic srh auger fldmob surfmob
51 impact     selb
52
53 solve      init
54
55
56 method     newton trap
57 #
58 # Vge increased from 0 up to Vge=10.0 V
59 solve      vgate=0.1  vstep=0.1   nstep=9    name=gate
60 solve      vgate=1.2  vstep=0.2   nstep=18   name=gate
61 solve      vgate=5.0  outf=VG5.str master
62 solve      vgate=5.2  vstep=0.2   nstep=23   name=gate
```

```
63 solve vgate=10.0 outf=VG10.str master
64 #
65 # Vge=5.0 V
66 # Vce increased from 0. up to Vce=20. V
67 log outf=powerex04_1.log master
68
69 load inf=VG5.str master
70 solve vcollector=0.1
71 solve vcollector=0.5
72 solve vcollector=1.0 vstep=1.0 vfinal=20.0 name=collector
73
74 #
75 # Vge=10.0 V
76 # Vce increased from 0. up to Vce=20. V
77 log outf=powerex04_2.log master
78 load inf=VG10.str master
79 solve vcollector=0.1
80 solve vcollector=0.5
81 solve vcollector=1.0 vstep=1.0 vfinal=20.0 name=collector
82 save outf=powerex04_1.str master
83 #
84 tonyplot -overlay powerex04_1.log powerex04_2.log -set powerex04_log.set
85 quit
86
87
88
```

9.1.5. powerex05.in: Guard Ring Breakdown Analysis

Requires: SSUPREM4, S-PISCES

This example demonstrates the fabrication and electrical analysis of a protection structure using guard rings. It shows:

- Protection device with guard rings process simulation using ATHENA
- Proper guard ring contact definition for breakdown analysis using ATLAS
- Transport model definition including impact ionization
- Breakdown test definition

The breakdown structure considered here consists of a series of four guard rings sandwiched between cathode and anode electrodes. The ATHENA simulation begins by defining a phosphorous doped silicon substrate and its associated mesh. Silicon dioxide is then deposited and etched to expose silicon for guard ring and anode implantation. Boron is implanted and diffused to define the guard ring and anode junction depth. Boron doped polysilicon is then deposited and etched to form the guard ring plate electrodes. Aluminum is deposited and etched to create the anode and cathode electrodes. These electrodes are specified using the electrode statement. This includes

the name and position. Notice that a substrate electrode is added by specifying the backside option. The completed structure is saved and plotted using TONYPLOT.

The ATLAS breakdown simulation is now described. In this simulation, the structure created by ATHENA will be automatically loaded into ATLAS when the command, go atlas, is reached. For this breakdown simulation including guard rings, the guard ring contact must be allowed to float. The contact statement specifies that a 1E20 ohm series resistor be added to each contact. This allows each guard ring contact to float and ensures that there is no appreciable current flow. The bipolar option to the models statement selects a default set of transport models for bipolar devices. The default bipolar models are: conmob: concentration dependent mobility, fldmob: lateral electric field dependent mobility, bgn: band gap narrowing effects, consrh: concentration dependent Shockley-Read-Hall recombination lifetimes, and auger: recombination accounting for high level injection effects. Since breakdown in semiconductor devices can occur in the presence of impact ionization, this model should be enabled. In this case, the impact selb statement enables the Selberherr impact ionization model. Please refer to the ATLAS User's manual for a detailed description of these and other models.

When simulating devices with external components like the guard ring plate resistors, the Newton solution method is required. When using large bias steps, or when operating a device near breakdown, it is advised to specify the trap option to the method statement. With this option enabled, ATLAS automatically reduces the applied bias when convergence is not achieved. The simulation then continues at this new bias point. If convergence is achieved, ATLAS tries the original bias point again. If not, the applied bias is reduced again. This will continue until convergence is achieved or until a maximum number of reductions takes place. Once convergence occurs, ATLAS will automatically work its way back to the original bias point where the initial reduction occurred.

The ATLAS solve statement is now used to construct the breakdown test. As in most cases, an initial zero bias solution is performed by selecting the init option of the solve statement. This gives ATLAS an initial guess for subsequent simulations. An output log file is opened and will contain terminal characteristics for each bias point selected for test or until another output log file is opened. For this breakdown test, the anode voltage is stepped from -1V to -900V in three stages: -1V to -5V, -5V to -25V, and -25V to -900V. This arrangement is designed to provide good convergence while minimizing total simulation time.

The solution at the final bias point is saved as a structure file and TonyPlot is invoked to plot the results. Anode, cathode and substrate currents can be plotted to identify the voltage where breakdown occurs. Various contour quantities such as electric field, potential, and impact generation rate can be displayed from the structure plot.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

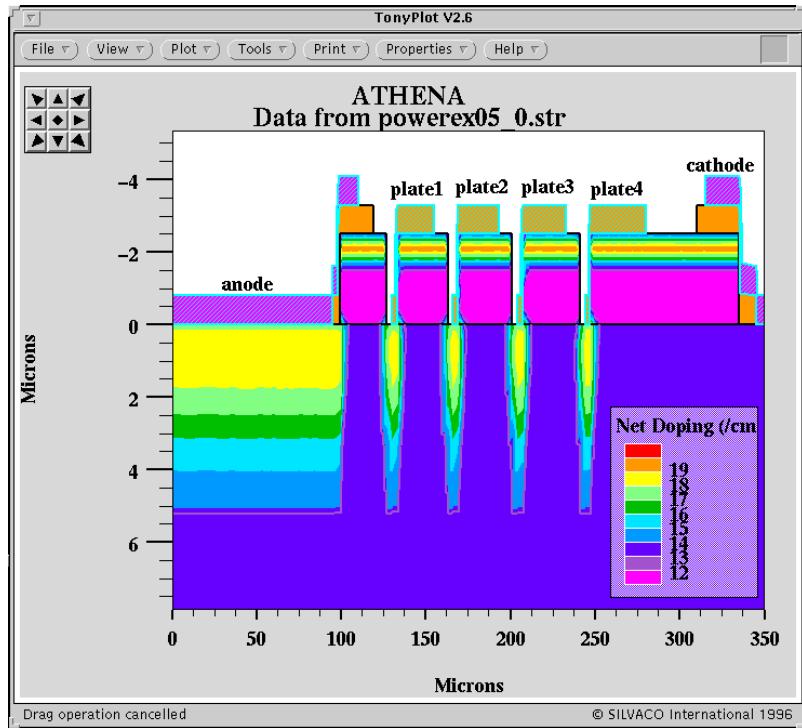


Figure 9.8: Diode structure with four guard rings and field plates defined in ATHENA. Plot is a zoom-in of the active region

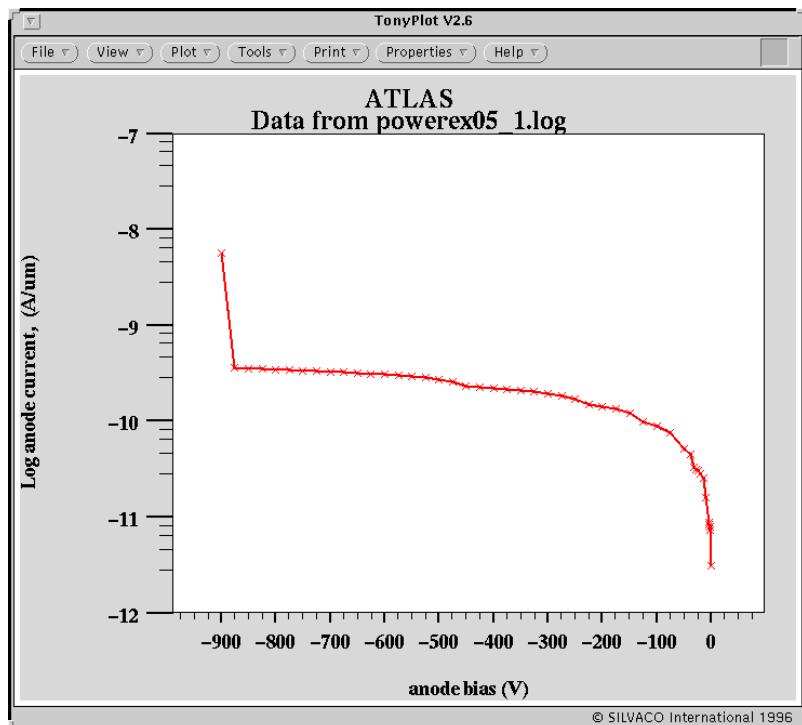


Figure 9.9: Diode breakdown for the four guard ring and field plate structure

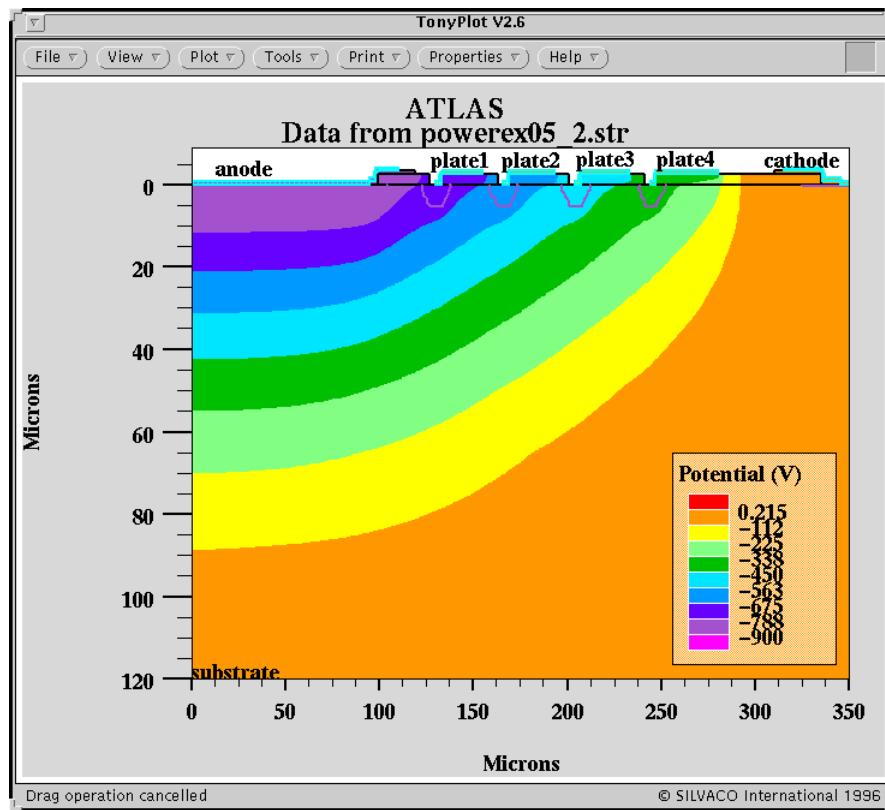


Figure 9.10: Potential Contours within the Guard ring structure. Note how the potential is evenly divided over the four field plates providing the maximum field reduction and hence, breakdown voltage

Input File power/powerex05.in:

```

1 go athena
2 #
3 line x loc=0.00 spac=1.0
4 line x loc=95.0 spac=.5
5 line x loc=96.0 spac=3.0
6 line x loc=99.0 spac=.5
7 line x loc=110.0 spac=.5
8 line x loc=119.0 spac=.5
9 line x loc=127.0 spac=.5
10 line x loc=130.0 spac=3.0
11 line x loc=133.0 spac=.5
12 line x loc=155.0 spac=.5
13 line x loc=163.0 spac=.5
14 line x loc=166.0 spac=3.0
15 line x loc=169.0 spac=.5
16 line x loc=193.0 spac=.5
17 line x loc=201.0 spac=.5
18 line x loc=204.0 spac=3.0

```

```
19 line x loc=207.0 spac=.5
20 line x loc=233.0 spac=.5
21 line x loc=241.0 spac=.5
22 line x loc=244.0 spac=3.0
23 line x loc=247.0 spac=.5
24 line x loc=280.0 spac=.5
25 line x loc=295.0 spac=3.0
26 line x loc=310.0 spac=3.0
27 line x loc=315.0 spac=3.0
28 line x loc=335.0 spac=3.0
29 line x loc=345.0 spac=3.0
30 line x loc=350.0 spac=5.0
31 #
32 line y loc=0.00 spac=0.1
33 line y loc=2.00 spac=0.5
34 line y loc=12.0 spac=2.0
35 line y loc=50.0 spac=5.0
36 line y loc=120.0 spac=10.
37 #
38 init c.phosphor=6e13 orientation=100 space.mult=4
39 #
40 deposit oxide thick=2.50 dy=0.40
41 #
42 etch oxide left p1.x=99
43 #
44 etch oxide start x=127 y=-3
45 etch oxide cont x=127 y=0
46 etch oxide cont x=133 y=0
47 etch oxide done x=133 y=-3
48 #
49 etch oxide start x=163 y=-3
50 etch oxide cont x=163 y=0
51 etch oxide cont x=169 y=0
52 etch oxide done x=169 y=-3
53 #
54 etch oxide start x=201 y=-3
55 etch oxide cont x=201 y=0
56 etch oxide cont x=207 y=0
57 etch oxide done x=207 y=-3
58 #
59 etch oxide start x=241 y=-3
60 etch oxide cont x=241 y=0
61 etch oxide cont x=247 y=0
```

```
62 etch oxide done x=247 y=-3
63 #
64 implant boron dose=1.0e15 energy=100
65 #
66 method fermi compress
67 diffus time=420 temp=1100 nitro
68 #
69 etch oxide right p1.x=335.00
70 #
71 deposit poly thick=.8 dy=0.40 c.boron=1e19
72 #
73 etch poly left p1.x=95.00
74 #
75 etch poly start x=119 y=-4
76 etch poly cont x=119 y=0
77 etch poly cont x=130 y=0
78 etch poly done x=130 y=-4
79 #
80 etch poly start x=155 y=-4
81 etch poly cont x=155 y=0
82 etch poly cont x=166 y=0
83 etch poly done x=166 y=-4
84 #
85 etch poly start x=193 y=-4
86 etch poly cont x=193 y=0
87 etch poly cont x=204 y=0
88 etch poly done x=204 y=-4
89 #
90 etch poly start x=233 y=-4
91 etch poly cont x=233 y=0
92 etch poly cont x=244 y=0
93 etch poly done x=244 y=-4
94 #
95 etch poly start x=280 y=-4
96 etch poly cont x=280 y=0
97 etch poly cont x=310 y=0
98 etch poly done x=310 y=-4
99 #
100 etch poly right p1.x=345.00
101 #
102 deposit alumin thick=.8 dy=0.40
103 #
104 etch aluminum start x=110.0 y=-8.0
```

```
105 etch aluminum cont x=110.0 y=0.0
106 etch aluminum cont x=315.0 y=0.0
107 etch aluminum done x=315.0 y=-8.00
108 #
109 electrode name=anode x=0
110 electrode name=cathode x=350
111 electrode name=plate1 x=150
112 electrode name=plate2 x=180
113 electrode name=plate3 x=220
114 electrode name=plate4 x=260
115 electrode name=substrate backside
116
117 structure outfile=powerex05_0.str
118
119 tonyplot powerex05_0.str -set powerex05_0.set
120 #
121
122 go atlas
123
124 contact name=plate1 res=1e20
125 contact name=plate2 res=1e20
126 contact name=plate3 res=1e20
127 contact name=plate4 res=1e20
128
129 models bipolar print
130 impact selb
131 output e.field
132
133 method newton trap
134 solve init
135
136 log outf=powerex05_1.log
137 solve vanode=-1 vstep=-1 vfinal=-5 name=anode
138 solve vanode=-5 vstep=-5 vfinal=-25 name=anode
139 solve vanode=-25 vstep=-25 vfinal=-900 name=anode
140 save outf=powerex05_2.str
141
142 tonyplot powerex05_1.log -set powerex05_1.set
143 tonyplot powerex05_2.str -set powerex05_2.set
144 quit
```

9.1.6. powerex06.in: GTO Turn-off Transient

Requires: S-PISCES, MIXEDMODE

This example illustrates the simulation of a Gate Turn-Off Thyristor(GTO). The device is embedded in a realistic power device circuit. The interaction between the circuit elements and the active device is important in accurately simulating GTO behavior. The steady state behavior is simulated first. This is used as the initial condition for the transient analysis. This example shows:

- GTO structure definition with ATLAS
- The SPICE-like command syntax for MIXEDMODE circuit simulation
- GTO steady state solution
- GTO transient turn-off process

ATLAS is used to define the GTO structure including mesh, materials, electrodes and doping. The `mesh rect` statement defines a rectangular mesh with grid lines at the locations specified by the `x.m` and `y.m` statements. Using the `region` statement, the mesh is divided into three regions: two, silicon and one insulator. The `electrode` statement defines the cathode, anode and gate electrodes. The doping statements define the doping profiles. Note the definition of implant type, junction position and characteristic length. The net profile is `n+ p n p+` from the cathode on top to anode on the bottom. The gate is contacted to the p region. This structure is saved and will be used as a device by MIXEDMODE.

In this simulation, the MIXEDMODE circuit simulator uses ATLAS to calculate the transient characteristics of a GTO under the specified circuit conditions. First, a steady-state simulation of the GTO circuit is performed. The `.begin` and `.end` statements indicate the beginning and end of the MIXEDMODE syntax. The MIXEDMODE commands are similar to those used in SMARTSPICE. Circuit components, topology, and analysis are defined here. In general, the circuit component definition consists of three parts: the type of component, the lead or terminal node assignments, and the component value or model name. For example, the first component definition in this simulation is a dc current source. Current source, `i1` defines the component as current source number one, `0` and `1` are the two circuit nodes for this component and `400` indicates that the current source value is 400 amps.

This circuit can be divided in two parts: input and output. The input circuit connects to the cathode and anode of the GTO. It includes current source `i1`, voltage source `v1`, resistors `r1 r2 r3`, diodes `d1 d2 d3`, inductors `l1 l2 l3`, and capacitor `c1`. The output or switching circuit connects to the GTO gate and anode and includes voltage sources `v1 v2 v3`, diode `d4`, resistors `r2 r4`, and inductor `l4`. The GTO component itself is specified by the `agto` statement. This statement specifies a device to be analyzed by ATLAS. The `a` part of the `agto` command specifies that this is a device statement. The `gto` portion simply defines the device name. The option `infile=` indicates which device structure file is to be used. Other command line options exist. Please refer to the MIXEDMODE section of the ATLAS User's manual for a complete list.

The `.nodeset` statement defines the initial values for node voltages and the `.save outfile=` statement saves the result to the indicated file. Since this is the steady state solution, no output log data file is needed. Since standard diode parts are used in this circuit, the `.model dd` statement is used to specify additional characteristics. Note that `dd` was the model name given in the diode component definition statement. Additionally, the `.options` command sets the solution method to a modified two-level Newton using the `m2ln` parameter.

To completely specify the simulation, the physical models used by ATLAS must be specified. The `model` statement is used to turn on the appropriate transport models. This set includes: `analytic`: the analytic concentration dependent mobility model, `fldmob`: the lateral electric field-dependent mobility model, `consrh`: Shockley-Read-Hall recombination using concentration dependent lifetimes, `auger`: recombination accounting for high level injection effects, and `bgn`: band gap narrow-

ing. The material statement is used to override default material parameters. In this case, the carrier recombination fixed lifetimes are set and for region three, the permittivity is set to that of air (1). Finally, an impact ionization model is enabled using the impact statement with the selb option. This specifies that the Selberherr impact ionization model is to be used. Note that for each of these commands, the device name and region can be specified.

The final part of this example is the transient simulation of the gate turn-off. The description of the circuit is similar to the steady state part. The gate turn-off is simulated by pulsing the GTO gate output resistance r4 from 1 megohm to 1 micro-ohm over 100 ns. This is defined by the additional command line options on the r4 command line. The result of the essentially shorted resistor r4 is that a negative pulse is applied to the gate which initiates the GTO turn-off process. The .tran statement controls the overall transient simulation time.

Terminal characteristics of the GTO, circuit node voltages and circuit element currents are saved in the .log file and can be observed with TONYPLOT. The turnoff speed is seen by plotting the GTO anode and gate current.

To load and run this example, select the Load example button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the run button to execute the example.

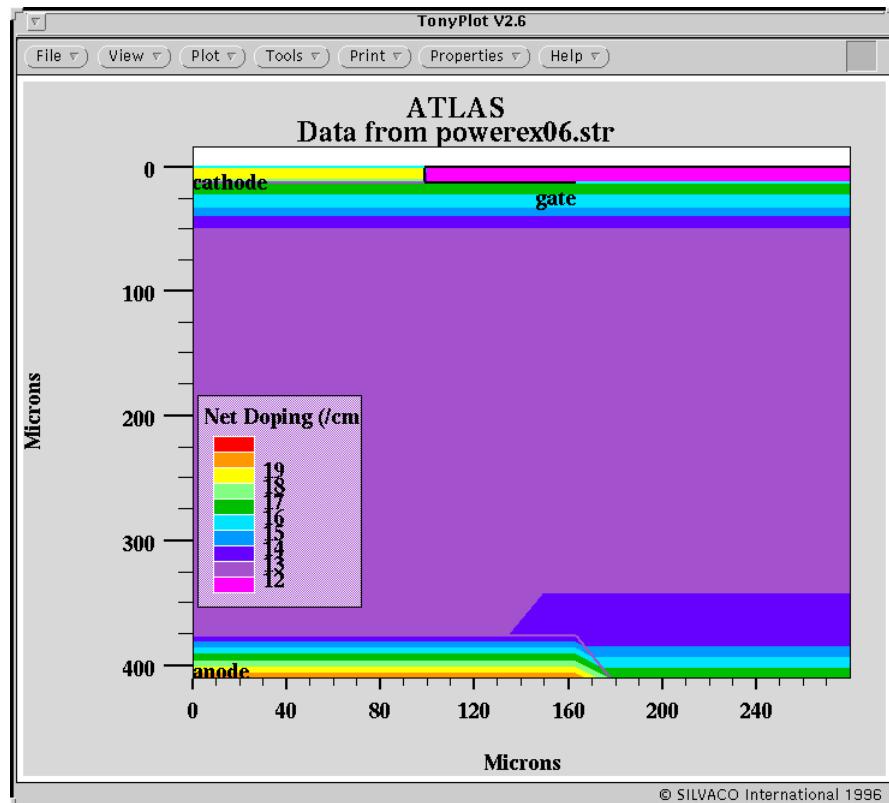


Figure 9.11: GTO Thyristor defined using ATLAS syntax.

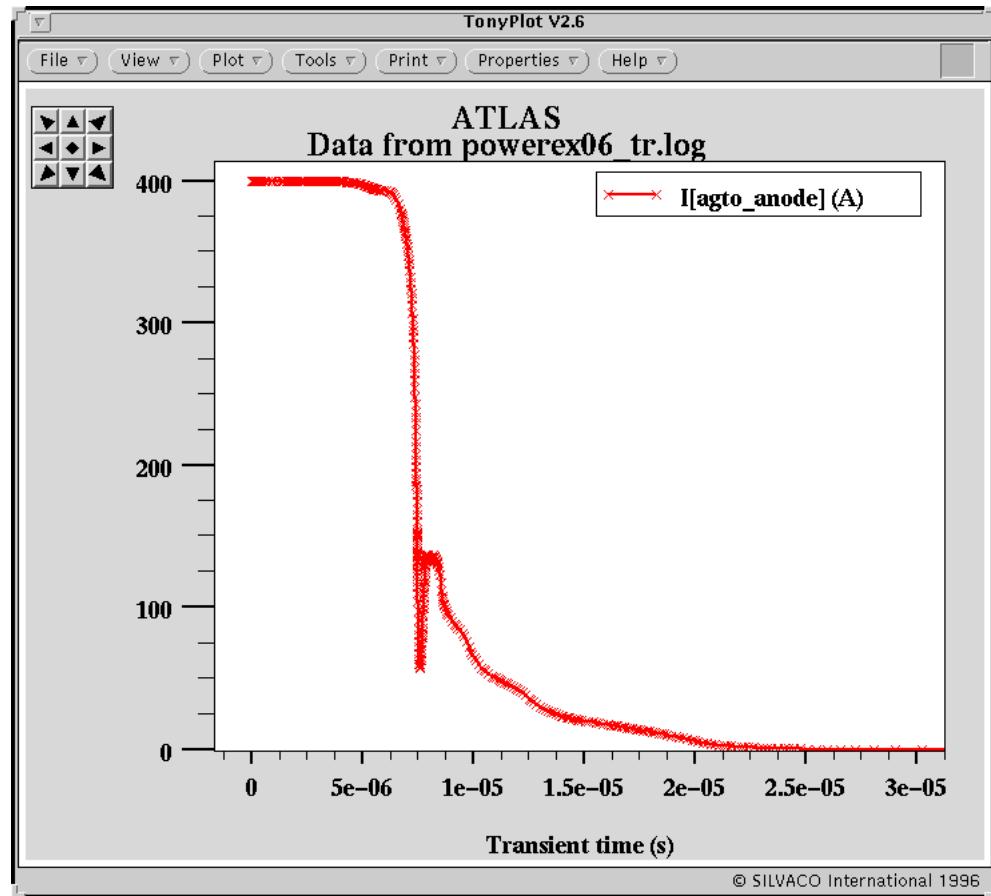


Figure 9.12: Thyristor anode voltage during gate turn off transient

Input File power/powerex06.in:

```

1 go atlas
2 # SILVACO INTERNATIONAL
3 #
4 mesh      nx=26 ny=25
5 x.m      n=1    l=0.0      r=1.0
6 x.m      n=9    l=90.0     r=1.0
7 x.m      n=14   l=105.0    r=1.0
8 x.m      n=26   l=280.0    r=1.0
9 #
10 y.m     n=1    l=0.0      r=1.0
11 y.m     n=5    l=13.0     r=1.0
12 y.m     n=9    l=17.0     r=1.0
13 y.m     n=15   l=70.0     r=1.0
14 y.m     n=25   l=410.0    r=1.0
15 #
16 region   num=1 silicon  x.min=0 x.max=100 y.min=0 y.max=13
17 region   num=2 silicon  x.min=0 x.max=280 y.min=13 y.max=410

```

```
18 region      num=3 insulator x.min=100 x.max=280 y.min=0 y.max=13
19 #
20 # 1- Cathode; 2- Anode; 3-Gate
21 elec        num=1 top left length=100 name=cathode
22 elec        num=2 bottom name=anode
23 elec        num=3 x.min=150 x.max=280 y.min=13 y.max=13. name=gate
24 #
25 # Impurity profile
26 #
27 doping reg=2 uniform conc=1.e13    n.type
28 doping reg=2 gauss conc=1.e17 p.type junc=47
29 doping reg=1 gauss conc=1.e19 n.type junc=16 x.l=0 x.r=100 rat=0.8
30 doping reg=2 gauss conc=1.e20 p.type peak=410 junc=393 x.l=0 x.r=170
               rat=0.1
31 doping reg=2 gauss conc=1.e17 n.type peak=410 char=10 x.l=170 x.r=280
32
33 save outf=powerex06.str
34 tonyplot powerex06.str -set powerex06.set
35 #
36 ##
37 go atlas
38 .begin
39 #
40 # Turn-off of GTO with protection circuitry
41 # SILVACO International
42 #
43 # Part 1: Steady state solution
44 # ISOTHERMAL CASE
45 #
46 i1 0 1  400.
47 d1 1 2  dd
48 v1 2 0  900
49 r1 1 3  1
50 l1 1 4  4uH
51 #
52 d2 5 3  dd
53 l2 4 5  4uH
54 r2 4 6  22
55 #
56 d3 5 6  dd
57 l3 5 7  0.2uH
58 c1 6 0  0.22uF
59 #
```

```
60 agto 0=cathode 7=anode 8=gate width=3.035e6 infile=powerex06.str
61 #
62 d4 12 8 dd
63 l4 8 9 0.5uH
64 r4 9 11 1mg
65 #
66 v2 12 0 -25
67 v3 11 0 -12
68 #
69 r3 9 10 5.4
70 #
71 v4 10 0 12
72 #
73 #
74 .nodeset v(1)=0 v(2)=900 v(3)=0 v(4)=0 v(5)=0 v(6)=0 \
75           v(7)=0. v(8)=0 v(9)=0 v(10)=12 v(11)=-12 v(12)=-25
76 #
77 .numeric toldc=1.e-6 vchange=0.05 imaxdc=100
78 .save outfile=gtosave
79 .model dd d is=1e-7
80 .options m2ln relpot print debug
81 .end
82 #
83 models device=agto reg=1 analytic fldmob consrh auger bgn
84 models device=agto reg=2 analytic fldmob consrh auger bgn
85 material device=agto reg=1 taun0=2.4e-6 taup0=0.6e-6
86 material device=agto reg=2 taun0=2.4e-6 taup0=0.6e-6
87 material device=agto reg=3 PERM=1
88 impact device=agto selb reg=1
89 impact device=agto selb reg=2
90
91 ##
92 go atlas
93 .begin
94 #
95 #      Turn-off of GTO with protection circuitry (tr)
96 #      SILVACO International
97 #
98 #      Part 2: Transient solution
99 #      ISOTHERMAL CASE
100 #
101 i1 0 1 400.
102 d1 1 2 dd
```

```
103 v1 2 0 900
104 r1 1 3 1
105 l1 1 4 4uH
106 #
107 d2 5 3 dd
108 l2 4 5 4uH
109 r2 4 6 22
110 #
111 d3 5 6 dd
112 l3 5 7 0.2uH
113 c1 6 0 0.22uF
114 #
115 agto 0=cathode 7=anode 8=gate width=3.035e6 infile=powerex06.str
116 #
117 d4 12 8 dd
118 l4 8 9 0.5uH
119 r4 9 11 1mg PULSE 1mg 1.e-6 0 100ns 100ns 10 1000
120 #
121 v2 12 0 -25
122 v3 11 0 -12
123 #
124 r3 9 10 5.4
125 #
126 v4 10 0 12
127 #
128 .numeric lte=0.1 toltr=1.e-4 dtmin=0.1ns
129 #
130 .tran 25ns 400us
131 .load infile=gtosave
132 .log outfile=powerex06
133 .model dd d is=1e-7
134 .options relpot print
135 .end
136 #
137 models device=agto reg=1 analytic fldmob consrh auger bgn
138 models device=agto reg=2 analytic fldmob consrh auger bgn
139 material device=agto reg=1 taun0=2.4e-6 taup0=0.6e-6
140 material device=agto reg=2 taun0=2.4e-6 taup0=0.6e-6
141 material device=agto reg=3 PERM=1
142 impact device=agto selb reg=1
143 impact device=agto selb reg=2
144 method climit=1000
145
```

```

146 tonyplot powerex06_tr.log -set powerex06_tr_log.set
147
148 quit

```

9.1.7. powerex07.in: LDMOS Breakdown

Requires: SSUPREM4, S-PISCES

This example simulates the fabrication process and breakdown analysis of a Lateral DMOS device (LDMOS). The example shows:

- Process simulation of the LDMOS structure using ATHENA
- Measurement of layer thickness, 1D V_t and BV_{dss} using EXTRACT
- Auto interface from ATHENA to ATLAS
- ATLAS simulation of the breakdown voltage BV_{dss}

The device simulated is an asymmetric LDMOS power device structure with a 4 micron gate length. ATHENA simulation starts by defining an asymmetric grid with a finer grid in the drift region. In preparation for the gate oxide growth, a sacrificial oxide layer is grown and etched away. A gate oxide of 570 Angstroms is then grown. To insure adequate grid spacing in the growing oxide, the method grid.ox statement sets the grid to 100 Angstroms. After the oxide growth, the extract statement is used to measure the gate oxide thickness. The results of the EXTRACT can be found in the DECKBUILD output window and in the file 'results.final'. Check for this file in the directory in which DECKBUILD was started. The next step is a low-energy and low-dose boron V_t-adjust implant. Poly deposition, poly-gate definition and drift region implant are then performed. The drift region is masked and n+ phosphorus is implanted into the opened source and drain areas.

After the final anneal at 1000 degrees the contact holes are opened, metal is deposited and patterned. The four electrodes are then specified.

A useful parameter to measure at this stage is the threshold voltage of a 1D slice through the center of the gate. This is done via the extract statement. Since the channel length is fairly long and the channel doping is uniform laterally, this is a fairly good approximation to the 2D threshold voltage that ATLAS would give. This ends the LDMOS process simulation. The resultant structure file is saved and plotted.

In this simulation, the structure created by ATHENA will be automatically loaded into ATLAS when the command, go atlas, is reached. The ATLAS portion of this example begins by specifying the physical models to be used. For this example, they are cvt: for transverse field dependent mobility, and srh: Shockley-Read-Hall recombination. carriers=2 indicates that both holes and electrons will be simulated. The Selberherr impact ionization model is enabled using the impact selb statement. The contact statement sets the gate workfunction to that of degenerately doped n-type polysilicon. Additionally, the interface statement sets the silicon-silicon dioxide interface charge to 3E10.

The method statement has many purposes. First, it sets the type of solution methodology, as in this case with the Newton option. The trap option enables the reduction in applied bias when convergence is not achieved. This is an important feature for large bias steps and simulations near breakdown. The option, climit=1e-4, improves convergence for breakdown simulation when the pre-breakdown current is very low. It is recommended for most power device breakdown calculations. Many other options are available. Please consult the ATLAS User's manual for additional information.

The sequence of solve statements ramp the drain voltage from zero to 100V. For this particular device, the breakdown voltage is about 50V. At biases higher than this, the simulation will fail to

converge. With the `trap` option enabled, ATLAS will automatically reduce the applied bias until the convergence criteria is met or until the maximum number of reductions is reached. The final `extract` statement reads the maximum drain voltage solved from the output log file. A plot of the `Id` versus `Vds` curve in TONYPLOT clearly shows the breakdown characteristics. A more sophisticated technique using the curve tracing algorithm in ATLAS is also possible. This technique is demonstrated in the Advanced MOS examples section for simulating snapback. Another technique using compliance limits is described in the MOS examples section under the NMOS breakdown.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

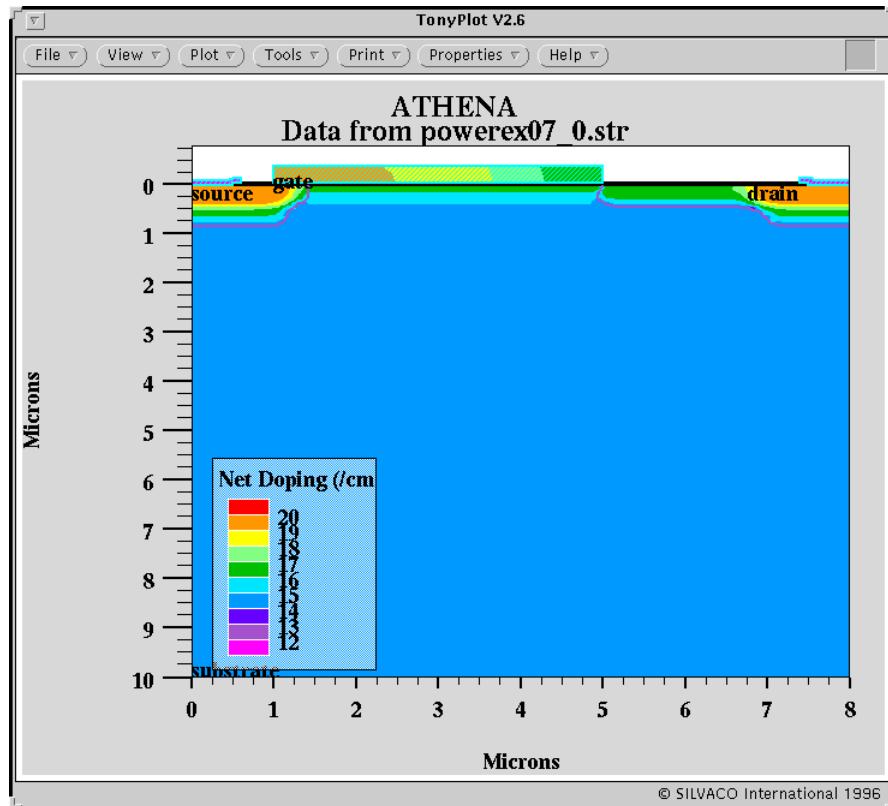


Figure 9.13: Doping and geometry of a lateral DMOS transistor simulated in ATHENA

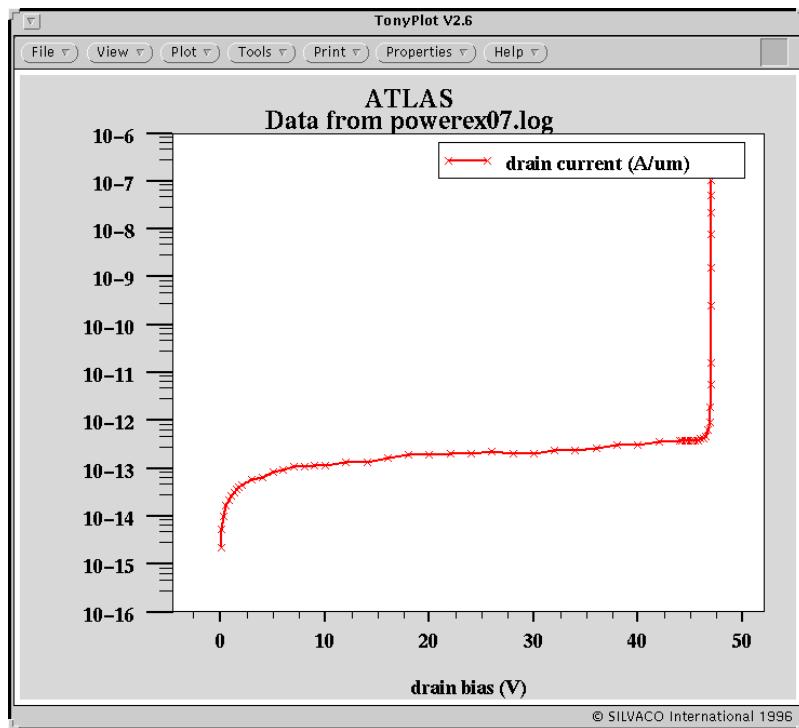


Figure 9.14: Breakdown of the LDMOS power transistor

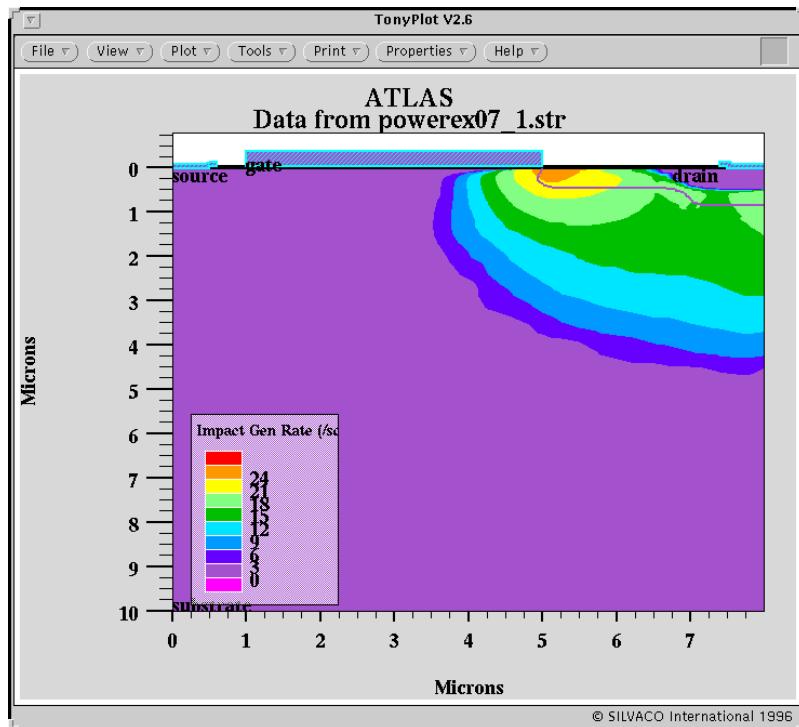


Figure 9.15: Contours of impact ionization in the LDMOS at the breakdown point. Note the impact ionization is spread though the whole drift region

Input File power/powerex07.in:

```
1 go athena
2 #
3 line x loc=0 spac=0.4
4 line x loc=0.5 spac=0.1
5 line x loc=0.6 spac=0.1
6 line x loc=1 spac=0.08
7 line x loc=2 spac=0.3
8
9 line x loc=3 spac=0.5
10 line x loc=5 spac=0.05
11 line x loc=6 spac=0.3
12 line x loc=7 spac=0.1
13 line x loc=7.4 spac=0.1
14 line x loc=7.5 spac=0.1
15 line x loc=8 spac=0.4
16
17 #
18 line y loc=0.00 spac=0.01
19 line y loc=0.2 spac=0.015
20 line y loc=0.5 spac=0.06
21 line y loc=1     spac=0.12
22 line y loc=10.0 spac=2.0
23 #
24 init orientation=100 c.boron=1e15
25 # sacrificial oxide
26 diffus time=30 temp=1000 dryo2
27 #
28 etch oxide all
29 #
30 # gate oxide growth
31 # make sure more than one grid point is included within the gate oxide
   thickness
32 method grid.ox=0.01
33 diffus time=50 temp=1000 dryo2 press=1.00 hcl=3
34 #
35 extract name="gateox" thickness material="SiO~2" mat.occno=1 x.val=-10
36
37 # vt adjust implant
38 implant boron dose=6e11 energy=20 pearson
39
40 # Poly deposition
41 depo poly thick=0.35 divi=10
```

```
42
43 # Poly definition
44 etch poly left p1.x=1
45 etch poly right p1.x=5
46 # slightly relax grid
47 relax y.min=0.4 dir.y=f
48 relax y.min=0.4 dir.y=f
49
50 # Light n+ implant
51 implant phosphor dose=2e12 energy=100 pearson
52 # S/D mask and implant
53 depo barrier thick=0.01
54 etch barrier left p1.x=2
55 etch barrier right p1.x=7
56 implant phos dose=3.0e15 energy=100 pearson
57 strip
58
59 # final anneal
60 method fermi compress
61 phosph poly /oxide trn.0=0.0
62 diffuse time=30 temp=1000 nitro press=1.0
63
64 # contact holes
65 etch oxide left p1.x=0.5
66 etch oxide right p1.x=7.5
67
68 # Contact metal deposition and etching
69 deposit alumin thick=0.1 divi=2
70 etch alumin start x=0.6 y=-10
71 etch cont x=0.6 y=10
72 etch cont x=7.4 y=10
73 etch done x=7.4 y=-10
74
75 # electrode naming
76 electrode name=source x=0.3
77 electrode name=gate x=2 y=0.0
78 electrode name=drain x=7.7
79 electrode name=substrate backside
80
81
82 # estimate threshold voltage
83 extract name="ldvt" ldvt ntype x.val=3.0
84
```

```
85 structure outf=powerex07_0.str
86 tonyplot powerex07_0.str -set powerex07_0.set
87
88
89 go atlas
90
91 models cvt srh print
92 impact selb
93
94
95 contact name=gate n.poly
96 interface qf=3e10
97 #
98 solve init
99 method newton trap maxtraps=10 climit=le-4 ir.tol=le-30 ix.tol=le-30
100
101
102 solve init
103 #
104 log outf=powerex07.log
105 solve vdrain=0.03
106 solve vdrain=0.1
107 solve vdrain=0.25 vstep=0.25 vfinal=2 name=drain
108
109 solve vstep=1 vfinal=10 name=drain
110
111 solve vstep=2.0 vfinal=44 name=drain
112 solve vstep=0.25 vfinal=50 name=drain compl=1.e-7 cname=drain \
113     outf=powerex07_1.str master onefile
114 extract name="bv" max(v."drain")
115
116 tonyplot powerex07.log -set powerex07_log.set
117 tonyplot powerex07_1.str -set powerex07_1.set
118 quit
```

9.1.8. powerex08.in: LDMOS Breakdown using Ionization Integrals

Requires: SSUPREM4, S-PISCES

This examples demonstrates a technique to quickly estimate the breakdown voltage of any device. It uses the same LDMOS power device process simulation and structure as the previous example.

Rather than perform a full breakdown analysis by solving for impact ionization using a two carrier approach, this example uses ionization integrals. Ionization integrals are based solely on the electric field strength so zero carrier solutions can be done. The zero carrier option is specified using

`carriers=0`. Although impact ionization is not solved directly, the impact model is used in the post processing analysis. For this, it is necessary to specify `impact selb`.

The ionization integrals are calculated along electric field lines. Electric field lines are specified during the solution by parameters on the `solve` statement. The parameter `deltav` specifies an offset between the applied voltage and the voltage at which the electric field lines will start. The lines should not start exactly at a contact since the electric field is often zero at the contact. The `lratio` parameter specifies the ratio of spacing between adjacent field lines. A value less than unity means the lines occur more to the left, greater than unity they occur more to the right. In this example the drain is on the right of the structure. So the lines should be more towards the high field area on the left side of the drain. Hence, `lratio` is less than one. The locations of the electric field lines can be saved into the solution files. However, the `output` statement must be used to specify the electric field line parameters as in the `solve` statement. The final plot shows the electric field and the electric field lines at the breakdown point.

The solve sequence in this example uses assigned variables from the `extract` statement to closely define the breakdown. The first solve statement ramps the drain voltage in 5V steps until the ionization integrals exceed one. This means the breakdown is between this voltage and 5V less than this voltage. The extract sequence steps the voltage back 5V. The 1V steps are taken until the breakdown condition is reached and the analysis is repeated. After this 0.1V steps are used to give a breakdown number to within 0.1V.

Users should note that using this method to extract the breakdown voltage is only approximate. The algorithm does not consider any current and hence usually overestimates the actual breakdown voltage. The advantage over the method in the previous example is speed.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

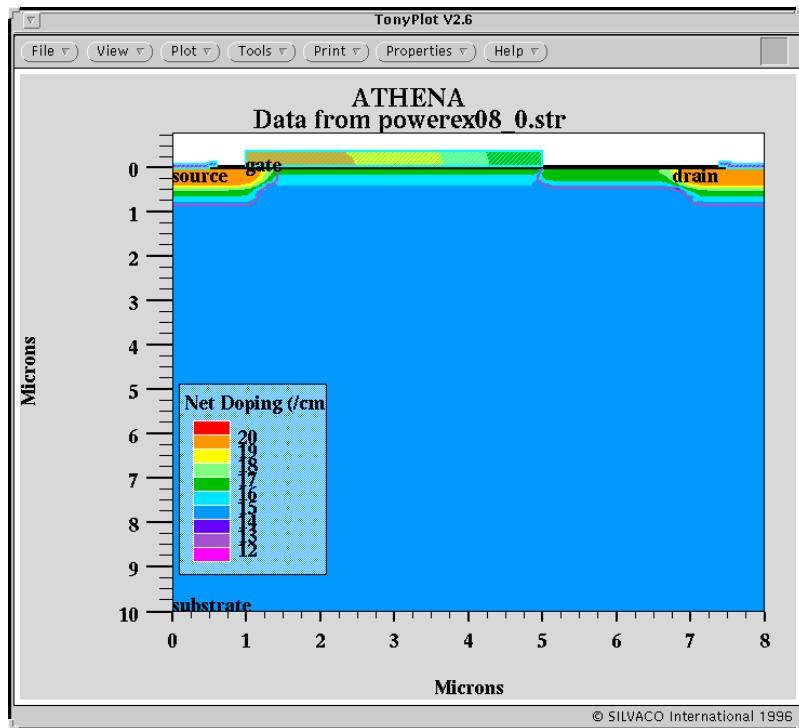


Figure 9.16: Doping and geometry of a lateral DMOS transistor simulated in ATHENA

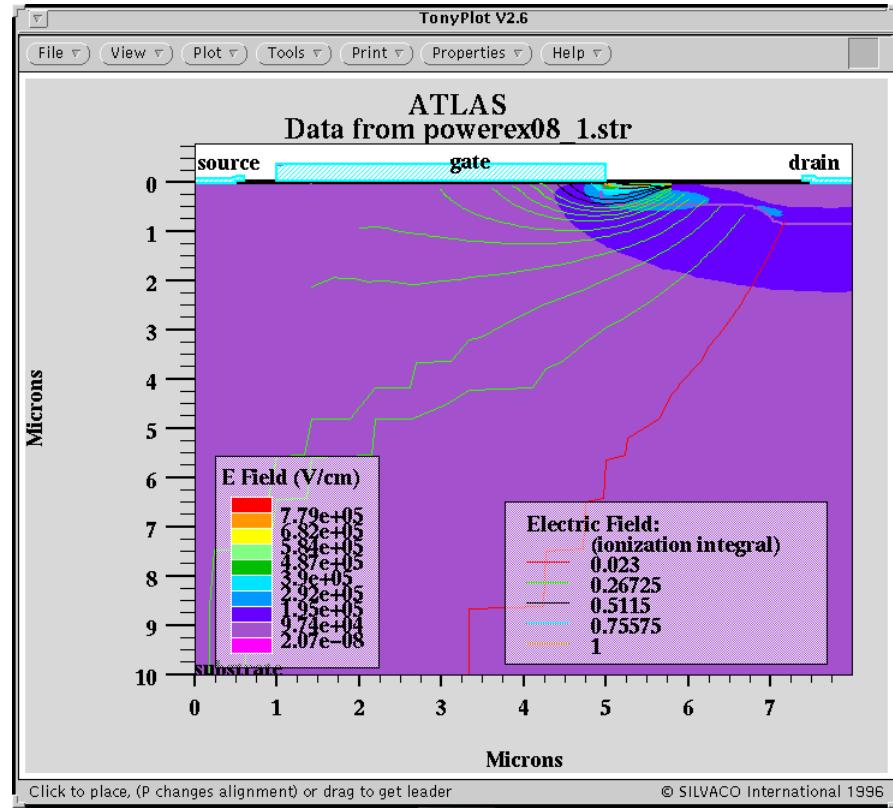


Figure 9.17: Electric field lines displayed over contours of electric field. Integrating the ionization rate along the field lines allows quick breakdown voltage estimation using a zero carrier solution in ATLAS

Input File power/powerex08.in:

```

1 go athena
2 #
3 line x loc=0 spac=0.4
4 line x loc=0.5 spac=0.1
5 line x loc=0.6 spac=0.1
6 line x loc=1 spac=0.08
7 line x loc=2 spac=0.3
8
9 line x loc=3 spac=0.5
10 line x loc=5 spac=0.05
11 line x loc=6 spac=0.3
12 line x loc=7 spac=0.1
13 line x loc=7.4 spac=0.1
14 line x loc=7.5 spac=0.1
15 line x loc=8 spac=0.4
16
17 #
18 line y loc=0.00 spac=0.01

```

```
19 line y loc=0.2 spac=0.015
20 line y loc=0.5 spac=0.06
21 line y loc=1      spac=0.12
22 line y loc=10.0 spac=2.0
23 #
24 init orientation=100 c.boron=1e15
25 # sacrificial oxide
26 diffus time=30 temp=1000 dryo2
27 #
28 etch oxide all
29 #
30 # gate oxide growth
31 # make sure more than one grid point is included within the gate oxide
   thickness
32 method grid.ox=0.01
33 diffus time=50 temp=1000 dryo2 press=1.00 hcl=3
34 #
35 extract name="gateox" thickness material="SiO~2" mat.occno=1 x.val=-10
36
37 # vt adjust implant
38 implant boron dose=6e11 energy=20 pearson
39
40 # Poly deposition
41 depo poly thick=0.35 divi=10
42
43 # Poly definition
44 etch poly left p1.x=1
45 etch poly right p1.x=5
46 # slightly relax grid
47 relax y.min=0.4 dir.y=f
48 relax y.min=0.4 dir.y=f
49
50 # Light n+ implant
51 implant phosphor dose=2e12 energy=100 pearson
52 # S/D mask and implant
53 depo barrier thick=0.01
54 etch barrier left p1.x=2
55 etch barrier right p1.x=7
56 implant phos dose=3.0e15 energy=100 pearson
57 strip
58
59 # final anneal
60 method fermi compress
```

```
61 phosph poly /oxide trn.0=0.0
62 diffuse time=30 temp=1000 nitro press=1.0
63
64 # contact holes
65 etch oxide left p1.x=0.5
66 etch oxide right p1.x=7.5
67
68 # Contact metal deposition and etching
69 deposit alumin thick=0.1 divi=2
70 etch alumin start x=0.6 y=-10
71 etch cont x=0.6 y=10
72 etch cont x=7.4 y=10
73 etch done x=7.4 y=-10
74
75 # electrode naming
76 electrode name=source x=0.3
77 electrode name=gate x=2 y=0.0
78 electrode name=drain x=7.7
79 electrode name=substrate backside
80
81
82 # estimate threshold voltage
83 extract name="ldvt" ldvt ntype x.val=3.0
84
85 structure outf=powerex08_0.str
86 tonyplot powerex08_0.str -set powerex08_0.set
87
88
89 go atlas
90 #mesh inf=powerex08_0.str
91
92 # set material models
93 models cvt srh print
94 impact selb
95 contact name=gate n.poly
96 interface qf=3e10
97 output e.field
98
99 method climit=1e-4 carriers=0
100
101 # Ramp the drain
102 log outf=powerex08_0.log master
```

```

103 solve vdrain=0 vstep=5 vfinal=200.0 name=drain ioniz ionlines=50 lratio=0.7 deltav=5
104 save outf=powerex08_1.str
105
106 extract name="Vd1" max(v."drain")-5.0
107 log outf=powerex08_1.log master
108 solve prev vdrain=$Vd1 vstep=1 vfinal=200 name=drain ioniz ionlines=50 lratio=0.7 deltav=5
109
110 extract name="Vd2" max(v."drain")-1.0
111 log outf=powerex08_2.log master
112 solve prev vdrain=$Vd2 vstep=0.1 vfinal=200 name=drain ioniz ionlines=50 lratio=0.7 deltav=5
113 extract name="bv" max(v."drain")
114
115
116 output e.lines contact=3 n.lines=50 lratio=0.7 deltav=5
117 save outf=powerex08_1.str
118
119 tonyplot powerex08_1.str -set powerex08_1.set
120
121
122

```

9.1.9. powerex09.in : Anisotropic Mobility Characteristics of a SiC T-MOSFET

Requires: DEVEDIT, BLAZE, SiC

This example demonstrates the simulation of the forward characteristics of a trench gated MOS power transistor. Three simulations are performed to show the effect of the crystallographic plane mobility modelling on the device characteristics.

This device is created entirely within DEVEDIT and is composed of SiC, silicon dioxide, aluminum and polysilicon within a simulation domain of 6um x 16um. The MOSFET has been created with a gate oxide of 800A and an N-type polysilicon gate.

The device simulations consist of the ID-VD characteristics at a gate voltage of 20V. Three characteristics were then obtained for different mobility models.

First, the standard isotropic mobility model was used where the SiC mobility coefficients were defined for the <1100> plane which is the high mobility plane.

Secondly, the standard isotropic mobility model was used where the SiC mobility coefficients were defined for the <1000> plane which is the low mobility plane.

Thirdly, an anisotropic mobility model was used where the SiC mobility coefficients were defined for both the <1100> and <1000> planes.

The anisotropic model is applied by specifying a default set of mobility coefficients which apply everywhere. Then on the second mobility statement the n.angle parameter specifies the mobility at 90 degrees to the horizontal. This switches on the anisotropic mobility model.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

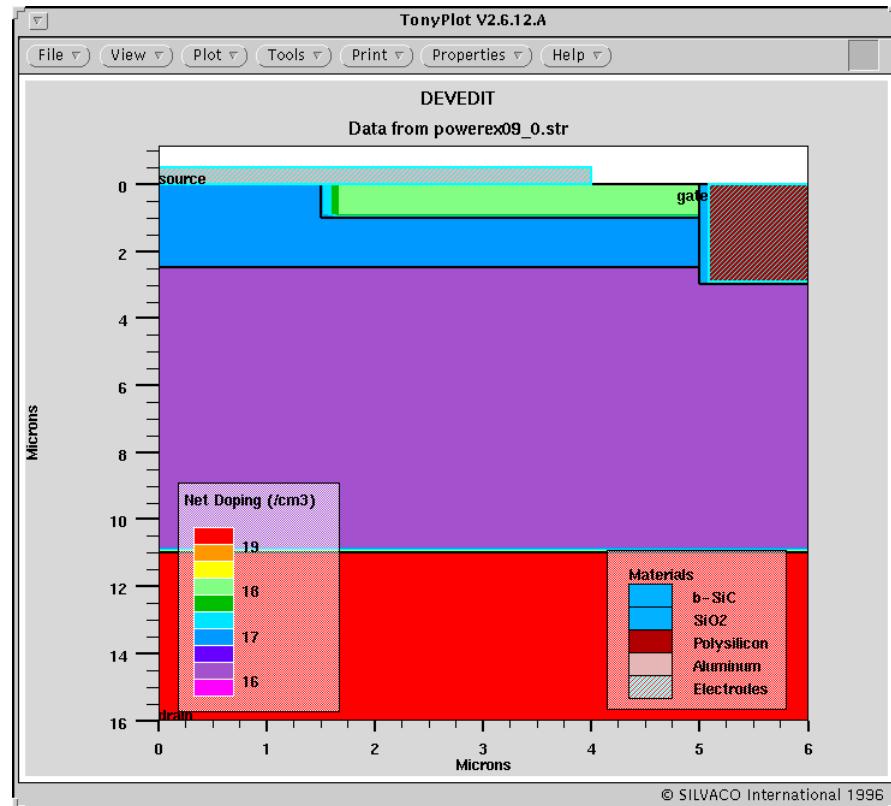


Figure 9.18: Doping and Geometry of a SiC D-MOS Power Transistor

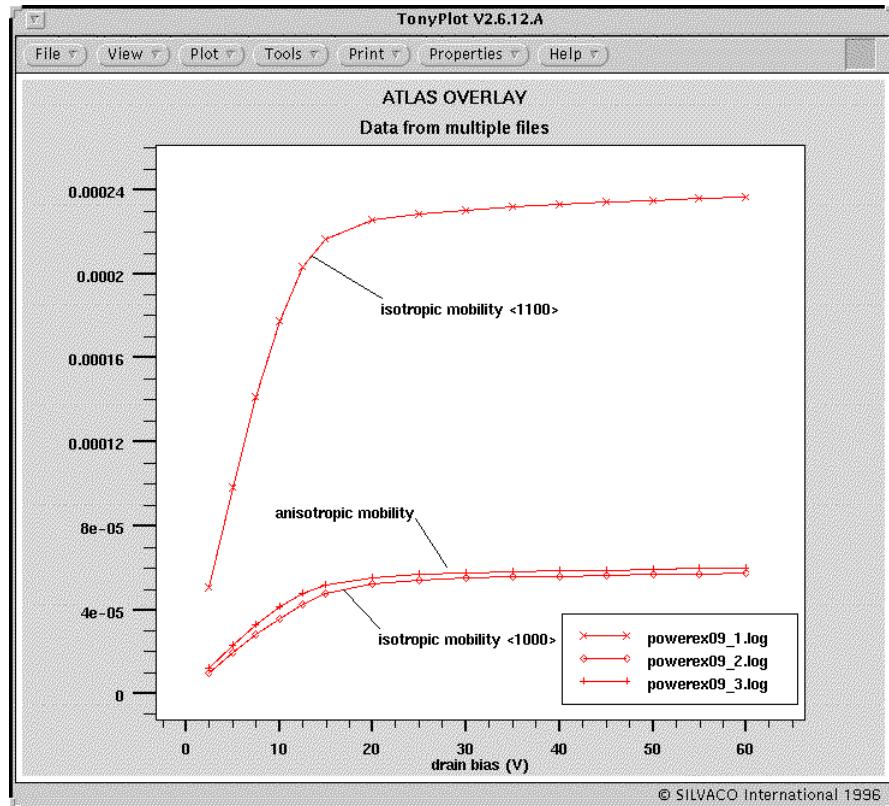


Figure 9.19: Id-Vd characteristics of a SiC T-MOSFET showing the difference between assuming isotropic and anisotropic mobility within the SiC

Input Deck power/powerex09.in :

```

1 go devedit
2
3 DevEdit version=2.4.2.R
4
5 work.area x1=0 y1=-0.5 x2=7 y2=17
6 # devedit 2.4.2.R (Wed Oct 29 20:04:11 PST 1997)
7 # libsflm 2.0.0.R (Thu May 1 18:03:38 PDT 1997)
8 # libDW_Misc 1.20.0.R (Mon Apr 28 17:55:25 PDT 1997)
9 # libCardDeck 1.20.0.R (Tue Apr 29 15:01:54 PDT 1997)
10 # libGeometry 1.20.0.R (Mon Apr 28 18:17:55 PDT 1997)
11 # libDW_Set 1.20.0.R (Mon Apr 28 17:57:52 PDT 1997)
12 # libSVC_Misc 1.20.0.R (Mon Apr 28 18:20:53 PDT 1997)
13 # libSDB 1.0.6.C (Mon May 5 16:28:49 PDT 1997)
14 # libSSS 1.20.0.R (Mon May 5 16:29:45 PDT 1997)
15 # libMeshBuild 1.20.2.R (Wed Oct 15 20:34:28 PDT 1997)
16 # libDW_Make 1.1.3.R (Thu May 1 20:07:31 PDT 1997)
17 region reg=1 name=n+sub mat=b-SiC color=0x7f00ff pattern=0x8 \
18 polygon="6,11 6,16 0,16 0,11"

```

```
19 #
20 impurity id=1 region.id=1 imp=Arsenic \
21 peak.value=1e+19 ref.value=1000000000000 comb.func=Multiply
22 #
23 constr.mesh region=1 default
24
25 region reg=2 name=n-drift mat=b-SiC color=0x7f00ff pattern=0x8 \
26 polygon="5,3 6,3 6,11 0,11 0,2.5 5,2.5"
27 #
28 impurity id=1 region.id=2 imp=Arsenic \
29 peak.value=1e+16 ref.value=1000000000000 comb.func=Multiply
30 #
31 constr.mesh region=2 default
32
33 region reg=3 name=pbase mat=b-SiC color=0x7f00ff pattern=0x8 \
34 polygon="5,2.5 0,2.5 0,0 1.5,0 1.5,1 5,1"
35 #
36 impurity id=1 region.id=3 imp=Boron \
37 peak.value=1e+17 ref.value=1000000000000 comb.func=Multiply
38 #
39 constr.mesh region=3 default max.height=0.25
40
41 region reg=4 name=n+source mat=b-SiC color=0x7f00ff pattern=0x8 \
42 polygon="5,1 1.5,1 1.5,0 4,0 5,0"
43 #
44 impurity id=1 region.id=4 imp=Arsenic \
45 peak.value=1e+18 ref.value=1000000000000 comb.func=Multiply
46 #
47 constr.mesh region=4 default max.height=0.2 max.width=0.25
48
49 region reg=5 name=gateox mat="Silicon Oxide" color=0xff pattern=0x2 \
50 polygon="5.08,2.92 6,2.92 6,3 5,3 5,2.5 5,1 5,0 5.08,0"
51 #
52 constr.mesh region=5 default
53
54 region reg=6 name=gate mat=PolySilicon elec.id=1 work.func=0 col-
      or=0xfffff00 pattern=0x5 \
55 polygon="6,2.92 5.08,2.92 5.08,0 6,0"
56 #
57 constr.mesh region=6 default
58
59 region reg=7 name=source mat=Aluminum elec.id=2 work.func=0 col-
      or=0xfffffc8c8 pattern=0x7 \
60 polygon="0,0 0,-0.5 4,-0.5 4,0 1.5,0"
```

```
61 #
62 constr.mesh region=7 default
63
64 substrate name="drain" electrode=3 workfunction=0
65
66
67 # Set Meshing Parameters
68 #
69 base.mesh height=2 width=0.5
70 #
71 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
    line.straightening=1 align.points when=automatic
72 #
73 imp.refine imp="Net Doping" scale=log transition=1e+10
74 imp.refine min.spacing=0.02
75 #
76 constr.mesh max.angle=90 max.ratio=300 max.height=1000 \
77 max.width=1000 min.height=0.0001 min.width=0.0001
78 #
79 constr.mesh type=Semiconductor default
80 #
81 constr.mesh type=Insulator default
82 #
83 constr.mesh type=Metal default
84 #
85 constr.mesh type=Other default
86 #
87 constr.mesh region=1 default
88 #
89 constr.mesh region=2 default
90 #
91 constr.mesh region=3 default max.height=0.25
92 #
93 constr.mesh region=4 default max.height=0.2 max.width=0.25
94 #
95 constr.mesh region=5 default
96 #
97 constr.mesh region=6 default
98 #
99 constr.mesh region=7 default
100 constr.mesh id=1 under.mat=PolySilicon depth=0.1 default max.height=0.02
    max.width=0.2
101 constr.mesh id=2 x1=4.9 y1=0 x2=5 y2=3.5 default max.width=0.02
102 constr.mesh id=3 x1=0 y1=2 x2=5 y2=3.5 default max.height=0.1
```

```
103 constr.mesh id=4 x1=0 y1=10 x2=6 y2=12 default max.height=0.4
104 constr.mesh id=5 x1=5 y1=0 x2=5.15 y2=3.5 default max.width=0.02
105 Mesh Mode=MeshBuild
106
107
108 base.mesh height=2 width=0.5
109
110 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
    line.straightening=1 align.Points when=automatic
111
112 struct outf=powerex09_0.str
113
114 tonyplot powerex09_0.str -set powerex09_0.set
115
116 go atlas
117
118 TITLE : TRENCH MOSFET POWER DEVICE SIMULATION
119
120 set temp=300
121
122 mesh infile=powerex09_0.str
123
124
125 material material=b-SiC perm=9.66 eg300=2.99 \
126 edb=0.1 gcb=2 eab=0.2 gvb=4 \
127 nsrhn=3e17 nsrhp=3e17 taun0=5e-10 taup0=1e-10 \
128 tc.a=100
129
130 models analytic conmob fldmob srh auger fermi optr bgn print temp="$temp"
131
132 # Standard isotropic mobility in plane <1100>
133 #
134 mobility material=b-SiC vsatn=2e7 vsatp=2e7 betan=2 betap=2 \
135 mu1n.caug=10 mu2n.caug=410 ncritn.caug=13e17 \
136 deltan.caug=0.6 gamman.caug=0.0 \
137 alphan.caug=-3 betan.caug=-3 \
138 mulp.caug=20 mu2p.caug=95 ncritp.caug=1e19 \
139 deltap.caug=0.5 gammap.caug=0.0 \
140 alphap.caug=-3 betap.caug=-3
141 #
142 contact name=gate n.poly
143 #
144
```

```
145 solve    init
146 solve    prev
147
148 method   newton
149 solve prev vfinal=20 name=gate vstep=1
150 save outf=powerex09_1.str
151
152 method   newton trap maxtrap=10
153 log outf=powerex09_1.log
154 solve prev vfinal=15 vstep=2.5 name=drain
155
156 output flowlines e.mobility h.mobility
157 save outf=powerex09_2.str
158
159 solve prev vfinal=60 vstep=5 name=drain
160
161 go atlas
162
163 TITLE : TRENCH MOSFET POWER DEVICE SIMULATION
164
165 set temp=300
166
167 mesh infile=powerex09_0.str
168
169
170 material material=b-SiC perm=9.66 eg300=2.99 \
171 edb=0.1 gcb=2 eab=0.2 gvb=4 \
172 nsrhn=3e17 nsrhp=3e17 taun0=5e-10 taup0=1e-10 \
173 tc.a=100
174
175 models analytic conmob fldmob srh auger fermi optr bgn print temp="$temp"
176
177 # Standard isotropic mobility in plane <1000>
178 #
179 mobility material=b-SiC vsatn=2e7 vsatp=2e7 betan=2 betap=2 \
180 mu1n.caug=5 mu2n.caug=80 ncritn.caug=13e17 \
181 deltan.caug=0.6 gamman.caug=0.0 \
182 alphan.caug=-3 betan.caug=-3 \
183 mu1p.caug=2.5 mu2p.caug=20 ncritp.caug=1e19 \
184 deltap.caug=0.5 gammap.caug=0.0 \
185 alphap.caug=-3 betap.caug=-3
186 #
187 contact name=gate n.poly
```

```
188 #
189
190 solve    init
191 solve    prev
192
193 method   newton
194 solve prev vfinal=20 name=gate vstep=1
195 save outf=powerex09_3.str
196
197 method   newton trap maxtrap=10
198 log outf=powerex09_2.log
199 solve prev vfinal=15 vstep=2.5 name=drain
200
201 output flowlines e.mobility h.mobility
202 save outf=powerex09_4.str
203
204 solve prev vfinal=60 vstep=5 name=drain
205
206 go atlas
207
208 TITLE : TRENCH MOSFET POWER DEVICE SIMULATION
209
210 set temp=300
211
212 mesh infile=powerex09_0.str
213
214
215 material material=b-SiC perm=9.66 eg300=2.99 \
216 edb=0.1 gcb=2 eab=0.2 gvb=4 \
217 nsrhn=3e17 nsrhp=3e17 taun0=5e-10 taup0=1e-10 \
218 tc.a=100
219
220 models analytic conmob fldmob srh auger fermi optr bgn print temp=$"temp"
221
222 # Anisotropic mobility model
223 #
224 # First define mobility in plane <1100>
225 #
226 mobility material=b-SiCvsatn=2e7 vsatp=2e7 betan=2 betap=2 \
227 mu1n.caug=10 mu2n.caug=410 ncritn.caug=13e17 \
228 deltan.caug=0.6 gamman.caug=0.0 \
229 alphan.caug=-3 betan.caug=-3 \
230 mulp.caug=20 mu2p.caug=95 ncritp.caug=1e19 \
```

```

231 deltap.caug=0.5 gammap.caug=0.0 \
232 alphap.caug=-3 betap.caug=-3
233 #
234 # Now define mobility in plane <1000>
235 #
236 mobility material=b-SiCn.angle=90.0 vsatn=2e7 vsatp=2e7 betan=2 betap=2 \
237 mu1n.caug=5 mu2n.caug=80 ncritn.caug=13e17 \
238 deltan.caug=0.6 gamman.caug=0.0 \
239 alphan.caug=-3 betan.caug=-3 \
240 mulp.caug=2.5 mu2p.caug=20 ncritp.caug=1e19 \
241 deltap.caug=0.5 gammap.caug=0.0 \
242 alphap.caug=-3 betap.caug=-3
243 #
244 contact name=gate n.poly
245 #
246
247 solve init
248 solve prev
249
250 method newton
251 solve prev vfinal=20 name=gate vstep=1
252 save outf=powerex09_5.str
253
254 method newton trap maxtrap=10
255 log outf=powerex09_3.log
256 solve prev vfinal=15 vstep=2.5 name=drain
257
258 output flowlines e.mobility h.mobility
259 save outf=powerex09_6.str
260
261 solve prev vfinal=60 vstep=5 name=drain
262
263 # Now plot three Id-Vd curves to compare mobility models
264 tonyplot -overlay powerex09_1.log powerex09_2.log powerex09_3.log -set
      powerex09.set
265
266 quit

```

9.1.10. powerex10.in : Anisotropic Mobility Characteristics of a SiC DMOS Device

Requires: DEVEDIT, BLAZE, SiC

This example demonstrates the simulation of the forward characteristics of a doubly diffused, or implanted, MOS power transistor.

Three simulations are performed to show the effect of the crystallographic plane mobility modelling on the device characteristics.

This device is created entirely within DEVEDIT and is composed of SiC, silicon dioxide and aluminum within a simulation domain of 7.5um x 15um. The MOSFET has been created with a gate oxide of 800A and an aluminum gate.

The device simulations consist of the ID-VD characteristics at a gate voltage of 20V. Three characteristics were then obtained for different mobility models.

First, the standard isotropic mobility model was used where the SiC mobility coefficients were defined for the <1100> plane which is the high mobility plane.

Secondly, the standard isotropic mobility model was used where the SiC mobility coefficients were defined for the <1000> plane which is the low mobility plane.

Thirdly, an anisotropic mobility model was used where the SiC mobility coefficients were defined for both the <1100> and <1000> planes.

The anisotropic model is applied by specifying a default set of mobility coefficients which apply everywhere. Then on the second mobility statement the n.angle parameter specifies the mobility at 90 degrees to the horizontal. This switches on the anisotropic mobility model.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

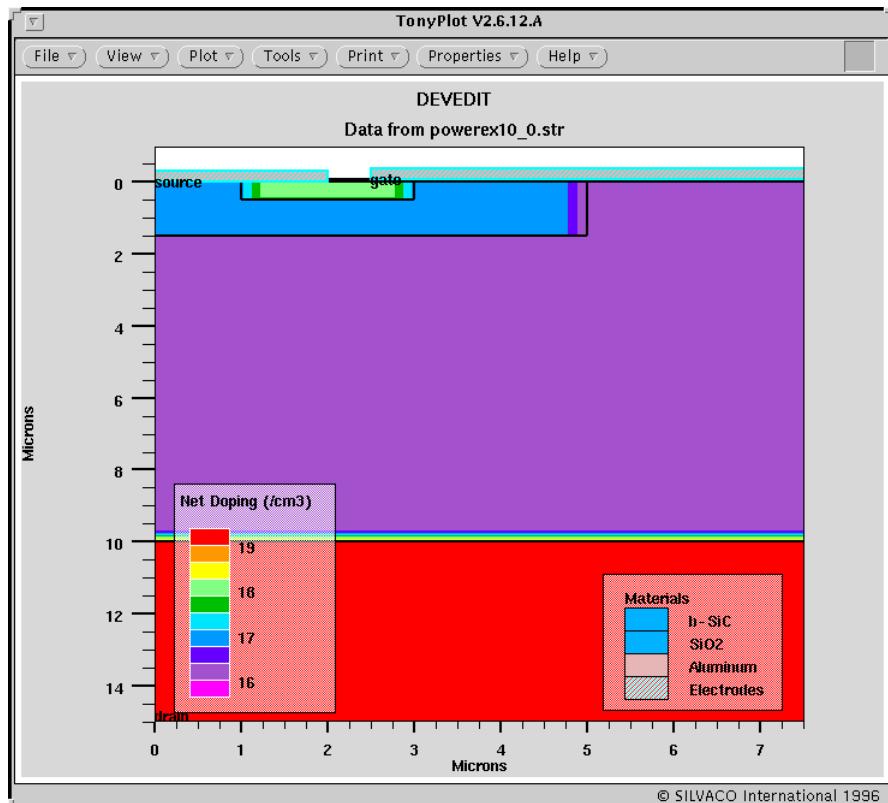


Figure 9.20: Id-Vd characteristics of a SiC D-MOS transistor showing the difference between assuming isotropic and anisotropic mobility within the SiC

Input Deck power/powerex10.in :

```

1 go devedit
2
3 DevEdit version=2.4.0.R
4
5 work.area x1=0 y1=-0.68 x2=10 y2=15
6 # devedit 2.4.0.R (Thu May  8 12:10:27 PDT 1997)
7 # libsflm 2.0.0.R (Thu May  1 18:03:38 PDT 1997)
8 # libDW_Misc 1.20.0.R (Mon Apr 28 17:55:25 PDT 1997)
9 # libCardDeck 1.20.0.R (Tue Apr 29 15:01:54 PDT 1997)
10 # libGeometry 1.20.0.R (Mon Apr 28 18:17:55 PDT 1997)
11 # libDW_Set 1.20.0.R (Mon Apr 28 17:57:52 PDT 1997)
12 # libSVC_Misc 1.20.0.R (Mon Apr 28 18:20:53 PDT 1997)
13 # libSDB 1.0.6.C (Mon May  5 16:28:49 PDT 1997)
14 # libSSS 1.20.0.R (Mon May  5 16:29:45 PDT 1997)
15 # libMeshBuild 1.20.0.R (Wed May  7 23:57:48 PDT 1997)
16 # libDW_Make 1.1.3.R (Thu May  1 20:07:31 PDT 1997)
17 region reg=1 name=n+sub mat=b-SiC color=0x7f00ff pattern=0x8 \
18 polygon="0,15 0,10 7.5,10 7.5,15"
19 #
20 impurity id=1 region.id=1 imp=Arsenic \
21 peak.value=1e+19 ref.value=1000000000000 comb.func=Multiply
22 #
23 constr.mesh region=1 default max.height=2
24
25 region reg=2 name=n-drift mat=b-SiC color=0x7f00ff pattern=0x8 \
26 polygon="5,1.5 5,0 7.5,0 7.5,10 0,10 0,1.5"
27 #
28 impurity id=1 region.id=2 imp=Arsenic \
29 peak.value=1e+16 ref.value=1000000000000 comb.func=Multiply
30 #
31 constr.mesh region=2 default max.height=1.25
32
33 region reg=3 name=pbase mat=b-SiC color=0x7f00ff pattern=0x8 \
34 polygon="1,0.5 3,0.5 3,0 5,0 5,1.5 0,1.5 0,0 1,0"
35 #
36 impurity id=1 region.id=3 imp=Boron \
37 peak.value=1e+17 ref.value=1000000000000 comb.func=Multiply
38 #
39 constr.mesh region=3 default
40
41 region reg=4 name=n+source mat=b-SiC color=0x7f00ff pattern=0x8 \
42 polygon="1,0 2,0 3,0 3,0.5 1,0.5"

```

```
43 #
44 impurity id=1 region.id=4 imp=Arsenic \
45 peak.value=1e+18 ref.value=1000000000000 comb.func=Multiply
46 #
47 constr.mesh region=4 default max.width=0.25
48
49 region reg=5 mat="Silicon Oxide" \
50 polygon="3,0 2,0 2,-0.08 2.5,-0.08 7.5,-0.08 7.5,0 5,0"
51 #
52 constr.mesh region=5 default
53
54 region reg=6 name=source mat=Aluminum elec.id=1 work.func=0 col-
      or=0xffc8c8 pattern=0x7 \
55 polygon="0,0 0,-0.3 2,-0.3 2,-0.08 2,0 1,0"
56 #
57 constr.mesh region=6 default max.width=0.25
58
59 region reg=7 name=gate mat=Aluminum elec.id=2 work.func=0 color=0xffc8c8
      pattern=0x7 \
60 polygon="2.5,-0.08 2.5,-0.38 7.5,-0.38 7.5,-0.08"
61 #
62 constr.mesh region=7 default
63
64 substrate name="drain" electrode=3 workfunction=0
65
66
67 # Set Meshing Parameters
68 #
69 base.mesh height=2.5 width=1
70 #
71 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
      line.straightening=1 align.points when=automatic
72 #
73 imp.refine imp="Net Doping" scale=log transition=1e+10
74 imp.refine min.spacing=0.02
75 #
76 constr.mesh max.angle=90 max.ratio=300 max.height=1000 \
77 max.width=1000 min.height=0.0001 min.width=0.0001
78 #
79 constr.mesh type=Semiconductor default
80 #
81 constr.mesh type=Insulator default
82 #
83 constr.mesh type=Metal default
```

```
84 #
85 constr.mesh type=Other default
86 #
87 constr.mesh region=1 default max.height=2
88 #
89 constr.mesh region=2 default max.height=1.25
90 #
91 constr.mesh region=3 default
92 #
93 constr.mesh region=4 default max.width=0.25
94 #
95 constr.mesh region=5 default
96 #
97 constr.mesh region=6 default max.width=0.25
98 #
99 constr.mesh region=7 default
100 constr.mesh id=1 under.reg=gate depth=0.1 default max.height=0.0125
      max.width=0.5
101 constr.mesh id=2 x1=0 y1=0.25 x2=1e+06 y2=2 default max.height=0.1
102 constr.mesh id=3 under.reg=source depth=0.1 default max.height=0.02
      max.width=0.25
103 constr.mesh id=4 x1=0 y1=8 x2=1e+06 y2=11 default max.height=0.4
104 constr.mesh id=5 x1=0 y1=2 x2=1e+06 y2=4 default max.height=0.6
105 Mesh Mode=MeshBuild
106
107
108 base.mesh height=2.5 width=1
109
110 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
      line.straightening=1 align.Points when=automatic
111
112 struct outf=powerex10_0.str
113
114 go atlas
115
116 #
117 TITLE : DMOS POWER DEVICE SIMULATION
118
119 set temp=300
120
121 mesh infile=powerex10_0.str
122
123
124 material material=b-SiC perm=9.66 eg300=2.99 \
```

```
125 edb=0.1 gcb=2 eab=0.2 gvb=4 \
126 nsrhn=3e17 nsrhp=3e17 taun0=5e-10 taup0=1e-10 \
127 tc.a=100
128
129 models analytic conmob fldmob srh auger fermi optr bgn print temp="$temp"
130
131 # Standard isotropic mobility in plane <1100>
132 #
133 mobility material=b-SiCvsatn=2e7 vsatp=2e7 betan=2 betap=2 \
134 muln.caug=10 mu2n.caug=410 ncritn.caug=13e17 \
135 deltan.caug=0.6 gamman.caug=0.0 \
136 alphan.caug=-3 betan.caug=-3 \
137 mulp.caug=20 mu2p.caug=95 ncritp.caug=1e19 \
138 deltap.caug=0.5 gammap.caug=0.0 \
139 alphap.caug=-3 betap.caug=-3
140 #
141 contact name=gate n.poly
142 #
143 tonyplot powerex10_0.str -set powerex10_0.set
144 #
145 solve init
146 solve prev
147
148 method newton
149 solve prev vfinal=20 name=gate vstep=1
150 save outf=powerex10_1.str
151
152 method newton trap maxtrap=10
153 log outf=powerex10_1.log
154 solve prev vfinal=15 vstep=2.5 name=drain
155
156 output flowlines e.mobility h.mobility
157 save outf=powerex10_2.str
158
159 solve prev vfinal=60 vstep=5 name=drain
160
161 go atlas
162
163 #
164 TITLE : DMOS POWER DEVICE SIMULATION
165
166 set temp=300
167
```

```
168 mesh infile=powerex10_0.str
169
170
171 material material=b-SiC perm=9.66 eg300=2.99 \
172 edb=0.1 gcb=2 eab=0.2 gvb=4 \
173 nsrhn=3e17 nsrhp=3e17 taun0=5e-10 taup0=1e-10 \
174 tc.a=100
175
176 models analytic conmob fldmob srh auger fermi optr bgn print temp="$temp"
177
178 # Standard isotropic mobility in plane <1000>
179 #
180 mobility material=b-SiC vsatn=2e7 vsatp=2e7 betan=2 betap=2 \
181 mu1n.caug=5 mu2n.caug=80 ncritn.caug=13e17 \
182 deltan.caug=0.6 gamman.caug=0.0 \
183 alphan.caug=-3 betan.caug=-3 \
184 mu1p.caug=2.5 mu2p.caug=20 ncritp.caug=1e19 \
185 deltap.caug=0.5 gammap.caug=0.0 \
186 alphap.caug=-3 betap.caug=-3
187 #
188 contact name=gate n.poly
189 #
190
191 solve init
192 solve prev
193
194 method newton
195 solve prev vfinal=20 name=gate vstep=1
196 save outf=powerex10_3.str
197
198 method newton trap maxtrap=10
199 log outf=powerex10_2.log
200 solve prev vfinal=15 vstep=2.5 name=drain
201
202 output flowlines e.mobility h.mobility
203 save outf=powerex10_4.str
204
205 solve prev vfinal=60 vstep=5 name=drain
206
207 go atlas
208
209 #
210 TITLE : DMOS POWER DEVICE SIMULATION
```

```
211
212 set temp=300
213
214 mesh infile=powerex10_0.str
215
216
217 material material=b-SiC perm=9.66 eg300=2.99 \
218 edb=0.1 gcb=2 eab=0.2 gvb=4 \
219 nsrhn=3e17 nsrhp=3e17 taun0=5e-10 taup0=1e-10 \
220 tc.a=100
221
222 models analytic conmob fldmob srh auger fermi optr bgn print temp="$temp"
223
224 # Anisotropic mobility model
225 #
226 # First define mobility in plane <1100>
227 #
228 mobility material=b-SiCvsatn=2e7 vsatp=2e7 betan=2 betap=2 \
229 mu1n.caug=10 mu2n.caug=410 ncritn.caug=13e17 \
230 deltan.caug=0.6 gamman.caug=0.0 \
231 alphan.caug=-3 betan.caug=-3 \
232 mulp.caug=20 mu2p.caug=95 ncritp.caug=1e19 \
233 deltap.caug=0.5 gammap.caug=0.0 \
234 alphap.caug=-3 betap.caug=-3
235 #
236 # Now define mobility in plane <1000>
237 #
238 mobility material=b-SiCn.angle=90.0 vsatn=2e7 vsatp=2e7 betan=2 betap=2 \
239 mu1n.caug=5 mu2n.caug=80 ncritn.caug=13e17 \
240 deltan.caug=0.6 gamman.caug=0.0 \
241 alphan.caug=-3 betan.caug=-3 \
242 mulp.caug=2.5 mu2p.caug=20 ncritp.caug=1e19 \
243 deltap.caug=0.5 gammap.caug=0.0 \
244 alphap.caug=-3 betap.caug=-3
245
246 contact name=gate n.poly
247 #
248
249 solve init
250 solve prev
251
252 method newton
253 solve prev vfinal=20 name=gate vstep=1
```

```

254 save outf=powerex10_5.str
255
256 method newton trap maxtrap=10
257 log outf=powerex10_3.log
258 solve prev vfinal=15 vstep=2.5 name=drain
259
260 output flowlines e.mobility h.mobility
261 save outf=powerex10_6.str
262
263 solve prev vfinal=60 vstep=5 name=drain
264
265
266 # Now plot three Id-Vd curves to compare mobility models
267 tonyplot -overlay powerex10_1.log powerex10_2.log powerex10_3.log -set
      powerex10_1.set
268
269 quit

```

9.1.11. powerex11.in : Vertical DMOS Gate Charging Simulation

Requires: SSUPREM4, DEVEDIT, MIXEDMODE

In modern power devices the total power loss comprises both a conductance power loss component and a capacitive loss component. As the cell pitch decreases the conduction loss will decrease whilst the capacitive loss will increase. Therefore for small cell pitch the capacitive power loss may be the dominant component in the total power loss in the device. The need is now clear for a method that will allow analysis of the capacitive component of the power loss. One technique to do this in a DMOS device is to analyse the gate charging time. This example illustrates a technique whereby the gate charging time for a vertical DMOS structure may be simulated.

The example contains the following parts:

- Process simulation to create the vertical DMOS
- The SPICE-like command syntax for simulating MIXEDMODE circuits
- Steady state analysis that defines the DC operating point
- Time domain analysis that illustrates gate charging

The first section uses ATHENA/SSUPREM4 to build a vertical DMOS power device. This section is identical to that used in the example powerex02.in which is described earlier in this power device section. For information on the process description please refer to this prior example.

After the process simulation, the structure is remeshed with DEVEDIT using the command: go devedit

At this point the solution only contains quantities from the process simulator, so only impurity values are available as remeshing criteria. These are selected with the commands:

```

imp.refine imp="Net Doping" scale=log transition=1e+10 sensitivity=2
imp.refine min.spacing=0.2

```

In addition to the doping profile devedit is used to obtain a denser mesh within the channel region underneath the gate. This is performed in two stages with the commands:

```
constr.mesh id=1 x1=2.5 y1=0 x2=1e+06 y2=0.5 default max.height=0.1  
max.width=2  
constr.mesh id=2 x1=2 y1=0 x2=4.5 y2=0.5 default max.height=0.1  
max.width=0.2
```

The mesh is then created using the devedit command

```
Mesh Mode=MeshBuild
```

Once the mesh has been designed for the electrical analysis it is passed on to the device simulator. This analysis is conducted using the mixed device and circuit simulator ATLAS/MIXEDMODE. First, a steady-state simulation of the power circuit is performed.

The .begin and .end statements indicate the beginning and end of the MIXEDMODE syntax. The MIXEDMODE commands are similar to those used in SmartSpice. Circuit components, topology, and analysis are defined within these statements. In general, the circuit component definition consists of three parts: the type of component, the lead or terminal node assignments, and the component value or model name.

For example, the first component definition in this simulation is an independent current source defined by iin between the circuit nodes 0 and 1. The final value of 0 indicates that the initial current source value is 0 Amps. The remaining circuit components are a resistor r1, another independent current source iout a compact diode model dum and a voltage source vin.

The amos statement specifies a device to be analyzed by ATLAS. The a part of the amos command specifies that this is a device statement. The mos portion simply defines the device name. The option infile= indicates which device structure file is to be used. The.nodeset statement defines the initial values for node voltages. The .dc statement indicates that a dc ramp is applied to the device iout. Additionally, the .options command specifies that a full Newton method is applied using the fulln parameter. Once the current ramp is complete the .save outfile= statement saves the final solution to the indicated file.

Other command line options exist. Please refer to the MIXEDMODE section of the ATLAS USER'S MANUAL for a complete list.

To completely specify the simulation, the physical models used by ATLAS must be specified. The model statement is used to turn on the appropriate transport models. This set includes commob: the concentration dependent mobility model, fldmob: the lateral electric field-dependent mobility model, surfmob: the surface degradation component of mobility, srh: Shockley-Read-Hall recombination, auger: recombination accounting for high level injection effects, and bgn: band gap narrowing. Refer to the ATLAS USER'S MANUAL for a description of these models. Finally, an impact ionization model is enabled using the impact statement with the selb option. This specifies that the Selber-herr impact ionization model is to be used.

The next step is the transient analysis which is specified in a similar manner. The charging effect of the gate is simulated by applying a current pulse to the independent current source iin. The .trans statement is used to specify the time stepping parameters for the transient analysis. In addition, the .log statement saves the diode output characteristics over the time interval specified. TONYPLOT plots the transient response of the circuit.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time. Once loaded into DECKBUILD, select the **run** button to execute the example.

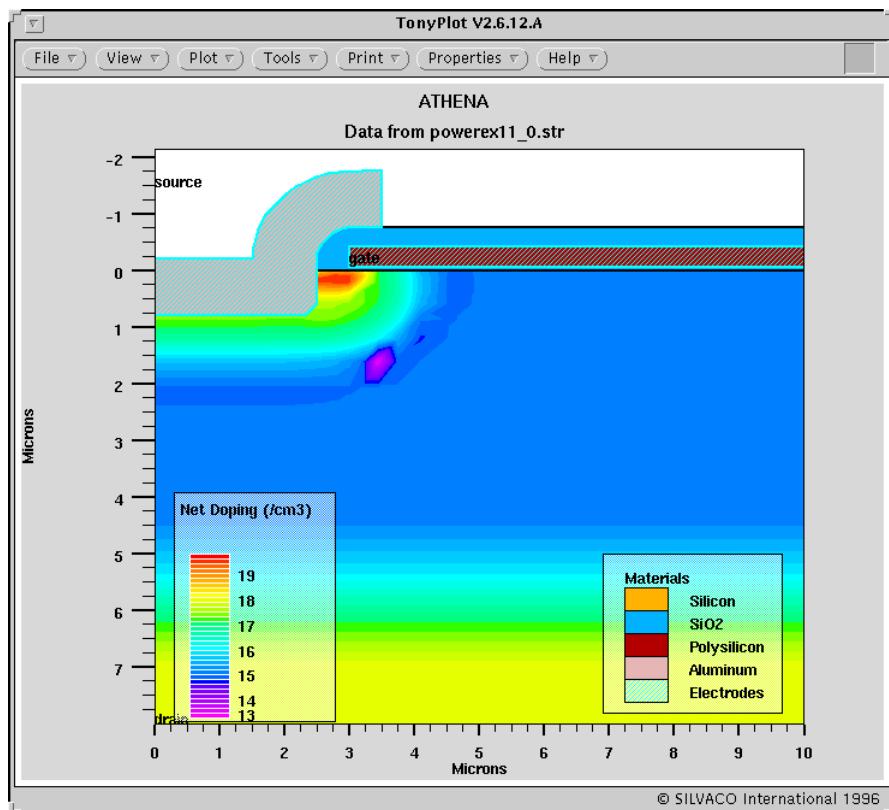


Figure 9.21: Geometry and Doping profile of a LDMOS power transistor

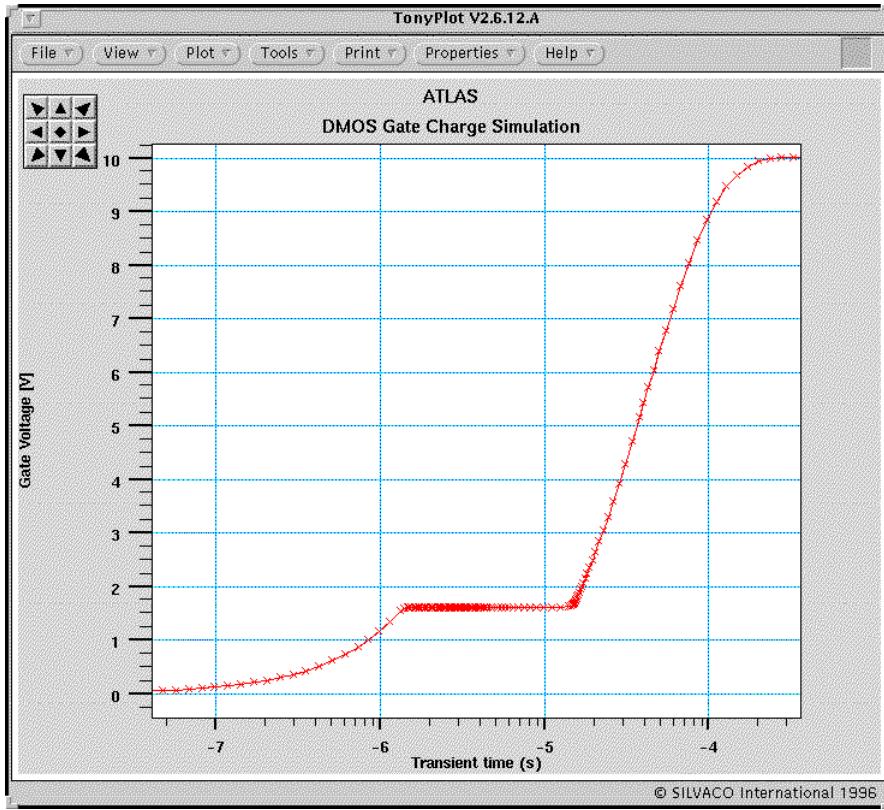


Figure 9.22: : Gate voltage versus time characteristic showing the change in gate charge

Input Deck power/powerex11.in :

```

1 go athena
2 #
3 line x loc=0.00 spac=0.25
4 line x loc=3.00 spac=0.10
5 line x loc=10.00 spac=1.0
6 #
7 line y loc=7.00 spac=0.5
8 line y loc=8.00 spac=0.5
9 #
10 init c.phosphor=1.0e18 orientation=100 space.mult=2
11 #
12 epitaxy time=10 temp=1200 thickness=7 divisions=15 \
13      dy=0.10 ydy=0.00 phosphorus conc=1.0e15
14
15 deposit oxide thickness=0.06
16 deposit poly thickness=0.35 div=3
17 deposit oxide thickness=0.35 div=3
18 deposit photores thickness=1 div=3
19

```

```
20
21 etch photores p1.x=3 left
22 etch oxide p1.x=3 left
23 etch poly p1.x=3 left
24 etch oxide p1.x=3 left
25
26 implant boron dose=1e14 energy=80
27
28 etch photores all
29
30 diffuse time=100 temp=1100
31
32 implant arsenic dose=3e15 energy=100
33 diffuse time=20 temp=1100
34
35
36 deposit oxide thickness=0.5 div=4
37 etch oxide thickness=0.5
38
39 etch start x=0 y=-0.1
40 etch cont x=0 y=0.8
41 etch cont x=2.5 y=0.8
42 etch done x=2.5 y=-0.1
43
44 diffuse time=1 temp=1100
45
46 deposit alum thickness=1 div=8
47 etch alum right p1.x=3.5
48
49 electrode name=source x=0
50 electrode name=gate x=5 y=-0.2
51 electrode name=drain backside
52
53 structure outfile=powerex11_0.str
54
55 tonyplot powerex11_0.str -set powerex11_0.set
56
57 go devedit
58 DevEdit version=2.4.0.R
59 #
60 init infile=powerex11_0.str
61
62 work.area x1=0 y1=-1.76 x2=10 y2=8
```

```
63 # devedit 2.4.0.R (Thu May  8 12:10:27 PDT 1997)
64 # libSFLM 2.0.0.R (Thu May  1 18:03:38 PDT 1997)
65 # libDW_Misc 1.20.0.R (Mon Apr 28 17:55:25 PDT 1997)
66 # libCardDeck 1.20.0.R (Tue Apr 29 15:01:54 PDT 1997)
67 # libGeometry 1.20.0.R (Mon Apr 28 18:17:55 PDT 1997)
68 # libDW_Set 1.20.0.R (Mon Apr 28 17:57:52 PDT 1997)
69 # libSVC_Misc 1.20.0.R (Mon Apr 28 18:20:53 PDT 1997)
70 # libSDB 1.0.6.C (Mon May  5 16:28:49 PDT 1997)
71 # libSSS 1.20.0.R (Mon May  5 16:29:45 PDT 1997)
72 # libMeshBuild 1.20.0.R (Wed May  7 23:57:48 PDT 1997)
73 # libDW_Make 1.1.3.R (Thu May  1 20:07:31 PDT 1997)
74 #
75 # Set Meshing Parameters
76 #
77 base.mesh height=1 width=2
78 #
79 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
    line.straightening=1 align.points when=automatic
80 #
81 imp.refine imp="Net Doping" scale=log transition=1e+10 sensitivity=2
82 imp.refine min.spacing=0.2
83 #
84 constr.mesh max.angle=90 max.ratio=300 max.height=10000 \
85 max.width=10000 min.height=0.0001 min.width=0.0001
86 #
87 constr.mesh type=Semiconductor default
88 #
89 constr.mesh type=Insulator default
90 #
91 constr.mesh type=Metal default
92 #
93 constr.mesh type=Other default
94 #
95 constr.mesh region=1 default
96 #
97 constr.mesh region=2 default
98 #
99 constr.mesh region=3 default
100#
101 constr.mesh region=4 default
102 constr.mesh id=1 x1=2.5 y1=0 x2=1e+06 y2=0.5 default max.height=0.1
    max.width=2
103 constr.mesh id=2 x1=2 y1=0 x2=4.5 y2=0.5 default max.height=0.1
    max.width=0.2
```

```
104 Mesh Mode=MeshBuild
105 refine mode=y x1=0.15 y1=5.98 x2=9.82 y2=7.53
106
107
108 base.mesh height=1 width=1
109
110 bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001
    line.straightening=1 align.Points when=automatic
111
112 structure outf=powerex11_1.str
113
114 go atlas
115 #
116 # This example demonstrates gate charge characteristics of a DMOS struc-
    ture.
117 #
118 # SPISCES, MIXEDMODE was used
119 #
120 # Part 1: Steady state solution
121 # Circuit descriptions
122 #
123 .begin
124 #
125 iin 0 1 0
126 r1 1 0 1e6
127 amos 1=gate 2=drain 0=source infile=powerex11_1.str width=1e4
128 iout 0 2 0
129 ddum 2 3 ideal
130 vin 3 0 0
131 #
132 # End of circuit description
133 #
134 .model ideal d()
135 #
136 .nodeset v(1)=0 v(2)=0 v(3)=0
137 #
138 .numeric lte=0.05
139 #
140 .options fulln print
141 #
142 .save outfile=powerex11
143 #
144 .log outfile=powerex11
145 #
```

```
146 .dc iout 0 1e-9 0.1e-9
147 .dc iout 1e-9 1e-8 1e-9
148 .dc iout 1e-8 1e-7 1e-8
149 .dc iout 1e-7 1e-6 1e-7
150 .dc iout 1e-6 1e-5 1e-6
151 .dc iout 1e-5 1e-4 1e-5
152 .dc vin 0 20 0.2
153 #
154 .end
155 #
156 contact device=amos name=gate n.poly
157 interface device=amos qf=2e11
158
159 models device=amos conmob fldmob surfmob srh auger bgn print
160 impact device=amos selb
161
162 method newton autonr trap
163
164
165
166 go atlas
167 # Part 2: Transient Solution
168 # Circuit descriptions
169 #
170 .begin
171 #
172 iin 0 1 0 pulse 0 1e-5 1e-10 1e-10 1e-10 100e-1 200e-1
173 r1 1 0 1e6
174 amos 1=gate 2=drain 0=source infile=powerex11_1.str width=1e4
175 iout 0 2 1e-4
176 ddum 2 3 ideal
177 vin 3 0 20
178 #
179 # End of circuit description
180 #
181 .model ideal d()
182 #
183 .numeric vchange=0.01 imaxtr=50
184 #
185 .load infile=powerex11
186 .save outfile=powerex11_tr
187 #
188 .options fulln print
```

```
189 #
190 .log outfile=powerex11
191 #
192 .tran 100ps 30e-1
193 #
194 .end
195 #
196 contact device=amos name=gate n.poly
197 interface device=amos qf=2e11
198
199 models device=amos conmob fldmob surfmob srh auger bgn print
200 impact device=amos selb
201
202 method newton autonr trap
203
204
205 go atlas
206
207 tonyplot powerex11_tr.log -set powerex11_1.set
208
209 quit
```

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10.1. ISOLATION : ISOLATION Applications Examples

10.1.1 isolationex01.in : Local Oxidation Isolation Punchthrough

Requires: SSUPREM4/DEVEDIT/SPICES

This example simulates the punchthrough between two n+ areas separated by an oxide isolation structure. The isolation structure is a local oxidation using Sealed Interface Local Oxidation (SILO) combined with a p-type field stop implant.

This example demonstrates the following features:

- processing of a local oxidation structure
- remeshing at the process to device simulation interface
- remeshing within device simulation
- ramping iv curves to a compliance limit

This examples starts with process simulation using ATHENA. Then, it's remeshes using DEVEDIT. And finally it's interfaced to ATLAS. ATLAS then ramps the voltage to 10V and a further remesh in DEVEDIT is performed. ATLAS then ramps to the punchthrough target current.

For details on local oxidation (bird's beak) process simulations, see the ATHENA_SSUPREM4 examples section.

The electrodes are placed at the end of the process flow and then subsequently named with electrode statements. Only the x coordinate needs to be specified, in this case, as the electrodes are on the surface of the structure. If they are buried, then both x and y coordinates need to be specified. Both polysilicon and metal regions are treated as possible electrodes.

The electrode name=substrate backside statement will automatically place an electrode on the bottom of the structure. This is the best and most efficient way of approximating a well contact.

After the process simulation, the structure is remeshed with DEVEDIT with the command:

```
go devedit
```

At this point the solution only contains solution quantities from the process simulator, so that only impurity values are available as remeshing criteria. These are selected with the commands:

- imp.refine imp="Arsenic" sensitivity=0.5
- imp.refine imp="Boron" sensitivity=0.4
- imp.refine imp="Phosphorus" sensitivity=0.5

Boron is weighted so that the mesh will be more sensitive to boron concentration gradients. This means, the smaller the value for sensitivity, the more sensitive the mesh will be to concentration gradients, which makes the mesh denser.

In this example, the constr.mesh command controls the maximum allowed angle within a triangle, specific to a material type. For example:

```
constr.mesh type=Insulator default max.angle=178
```

states that very obtuse triangles are allowed in all insulator (oxide) regions.

This is acceptable, because obtuse triangles are only a problem in semiconductor regions, when solving carrier transport equations. The reason for doing this, is because by lowering the criteria for maintaining zero obtuse triangles, the mesh will be more relaxed, which makes the simulation run faster.

Next, the structure is passed into the device simulator, ATLAS, for biasing and design parameter extraction. This is accomplished with the `go atlas` command.

As the device is punching through, the current is governed almost completely by the potential barrier and drain induced barrier lowering effects. Thus, a mobility model is not selected to speed to calculation.

An interface charge of `1e11` is selected arbitrarily and can be adjusted as a primary calibration parameter to match experimental results.

A sequence of `solve` commands ramps the drain contact up to 10 volts, using a current compliance of `0.1uA`. The simulation stops when either of these are exceeded. It is assumed that the breakdown will not occur during this ramp. After each bias point, a single structure file, containing both the mesh and the solution, is saved.

After a biasing of 10 volts, use DEVEDIT to remesh the structure. But this time, use it as a function of potential gradient, doping gradient, and electron concentration gradient. A more accurate mesh will result. 10 volts is chosen as a value, which will always be lower than the punchthrough voltage, but high enough to offer a closer solution to the final IV area of interest.

Another log file is opened for the final punchthrough IV curve to be held. The solution is reloaded with the new mesh created by DEVEDIT and the drain bias is increased up to 30 volts or `0.1um/W/L`, which ever is reached sooner.

Finally, a design parameter, relating to the punchthrough voltage is extracted.

The command:

```
extractname="n_isolation_vpt" x.valfrom  
curve(abs(v."drain"),abs(i."drain"))where y.val = 1.0e-7
```

should be allowed to run over two lines. Don't use a line continuation character in any extract statement. It defines the measure of punchthrough at that drain voltage, where the drain current is `0.1uA/um`.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will then be copied to your current working directory. Once loaded into DeckBuild, select the **run** button to execute the example.

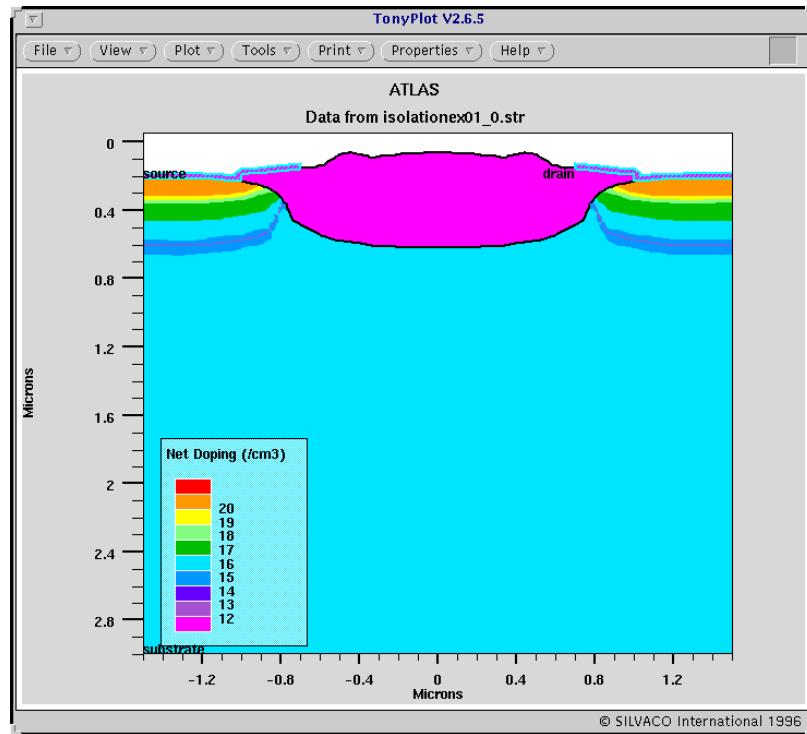


Figure 10.1: LOCOS isolation structure defined in ATHENA. This test ramps the drain electrode

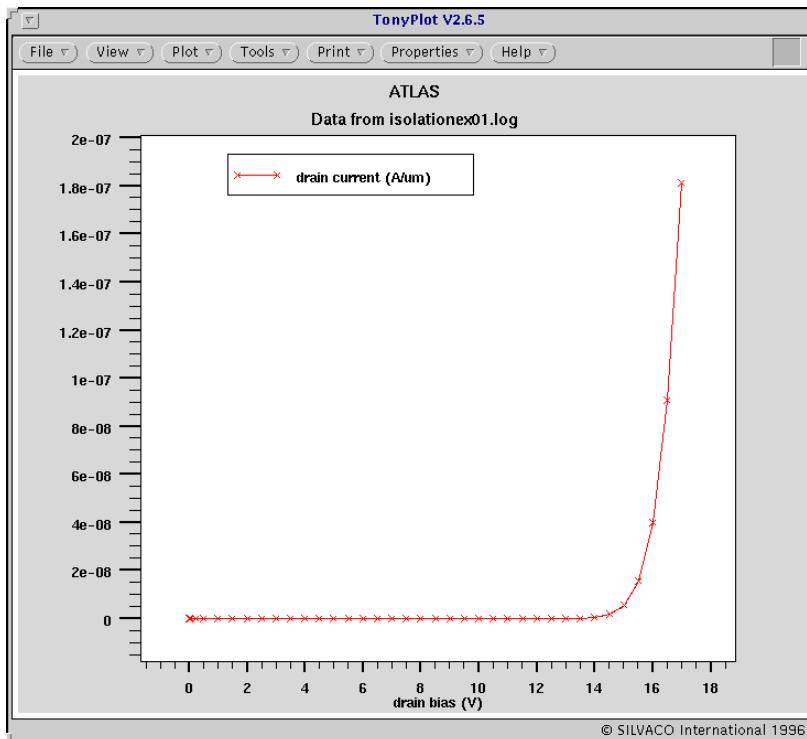


Figure 10.2: Curve of leakage from source to drain across the LOCOS isolation

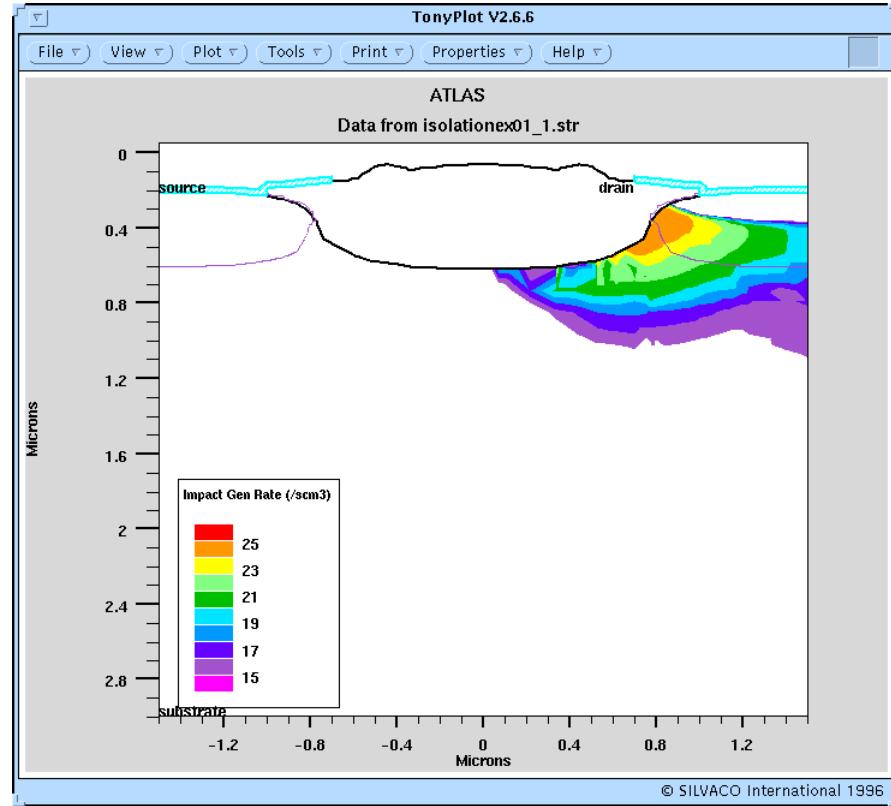


Figure 10.3: Impact ionization under the LOCOS showing a peak at the drain edge

Input File **isolation/isolationex01.in:**

```

1 go athena
2 # Active Area Isolation Structure Punchthrough Extraction Test
3 #
4 line x loc=0 spac=0.1 tag=left
5 line x loc=0.5 spac=0.04
6 line x loc=0.7 spac=0.04
7 line x loc=1.5 spac=0.1 tag=right
8 #
9 line y loc=0.00 spac=0.01 tag=top
10 line y loc=0.2 spac=0.01
11 line y loc=0.35 spac=0.04
12 line y loc=0.5 spac=0.04
13 line y loc=3 spac=0.3 tag=bottom
14 #
15 init orientation=100 c.phos=1e12 space.m=1
16
17 #pwell formation including masking off of the nwell
18 #

```

```
19 diffus time=30 temp=1000 dryo2 press=1.00 hcl=3
20 #
21 etch oxide thick=0.02
22 #
23 #P-well Implant
24 #
25 implant boron dose=1e12 energy=100 pears
26 #
27 diffus temp=950 time=100 weto2 hcl=3
28 #
29 #N-well implant not shown -
30 #
31 # welldrive starts here
32 diffus time=50 temp=1000 t.rate=4.000 dryo2 press=0.10 hcl=3
33 #
34 diffus time=220 temp=1200 nitro press=1
35 #
36 diffus time=90 temp=1200 t.rate=-4.444 nitro press=1
37 #
38 etch oxide all
39 #
40 #Create Active..
41 deposit oxide thick=0.01 divi=1
42 deposit nitride thick=0.3 divi=6
43
44 deposit barrier thick=.1 divi=1
45 #
46 etch barrier left p1.x=0.5
47 etch nitride thick=.35
48 etch oxide thick=.02
49 etch silicon dry thick=0.15
50 #
51 #Field Implant
52 implant boron dose=1e12 energy=50
53 #
54 strip
55 relax y.min=1
56 relax y.min=1.5
57 #
58 #Fieldox
59 method grid.ox=0.1
60 diffuse temp=950 time=180 weto2 hcl.pc=3
61
```

```
62 etch nitride all
63 #
64 etch oxide thick=0.02 dry
65 #
66 #sacrificial "cleaning" oxide
67 diffus time=20 temp=1000 dryo2 press=1 hcl=3
68 #
69 etch oxide dry thick=0.02
70 #
71 #gate oxide grown here:-
72 diffus time=11 temp=925 dryo2 press=1.00 hcl=3
73 #
74 # Extract the gate oxide thickness...
75 extract name="gate ox" thickness oxide mat.occno=1
76
77 # Implant the VT adjust....
78 #vt adjust implant
79 implant boron dose=1e12 energy=25 pearson
80 #
81 #LDD Spacer formation
82 depo oxide thick=0.120 divisions=8
83 #
84 etch oxide dry thick=0.120
85 #
86 implant arsenic dose=5.0e15 energy=50 pearson
87 #
88 method fermi compress
89 diffuse time=30 temp=900 nitro press=1.0
90 #
91
92 # Make the metal contacts to be used as electrodes in Atlas...
93 etch oxide right p1.x=1
94 deposit alumin thick=0.03 divi=2
95 etch alumin left p1.x=0.7
96 structure mirror left
97 # Name the electrodes....
98 electrode name=source x=-1.2
99 electrode name=drain x=1.2
100 electrode name=substrate backside
101
102
103 # Remesh the structure for Device simulation.....
104 # Use the Sensitivity & Minspacing parameters to adjust the mesh densi-
```

```
ty....  
105 # .. the smaller the Sensitivity, the denser the mesh...  
106  
107 go devedit  
108  
109 base.mesh height=0.25 width=0.25  
110 bound.cond apply=false max.ratio=300  
111 constr.mesh max.angle=90 max.ratio=300 max.height=1 max.width=1 \  
112         min.height=0.0001 min.width=0.0001  
113 constr.mesh type=Semiconductor default  
114 constr.mesh type=Insulator default max.angle=178  
115 constr.mesh type=Metal default max.angle=179  
116  
117 # Define the minimum mesh spacing globally...  
118 imp.refine min.spacing=0.025  
119  
120 # Select a list of solution (impurity) gradients to refine upon....  
121 imp.refine imp="Arsenic" sensitivity=0.5  
122 imp.refine imp="Boron" sensitivity=0.4  
123 imp.refine imp="Phosphorus" sensitivity=0.5  
124  
125 # now mesh the structure....  
126 mesh  
127 #  
128  
129  
130  
131  
132 go atlas  
133  
134 # restate the models then load the last devedit structure and solve  
     again....  
135 models cvt print srh  
136 interface qf=1e11  
137  
138  
139 impact selb  
140  
141 solve init  
142  
143 save outfile=isolationex01_0.str  
144  
145 # plot structure
```

```
146 tonyplot isolationex01_0.str -set isolationex01_0.set
147
148 method newton
149 log outf=isolationex01.log
150 # Now ramp up to the punchthrough point....
151
152 solve vdrain=0.025
153 solve vdrain=0.05
154 solve vdrain=0.25
155
156 solve vdrain=0.5 vstep=0.5 vfinal=30.0 name=drain comp=1.0le-07
      cname=drain
157
158 save outf=isolationex01_1.str
159
160
161
162 # Save a final structure file with all solution quantities inside it...
163
164
165 extract init infile="isolationex01.log"
166 # extract the punchthrough voltage....
167 extract name="n_isolation_vpt" x.val from
      curve(abs(v."drain"),abs(i."drain")) where y.val = 1.0e-7
168
169 # plot the IV curve...
170 tonyplot isolationex01.log -set isolationex01_log.set
171 # plot the last structure for looking at the internals of the device....
172 tonyplot isolationex01_1.str -set isolationex01_1.set
173 #
174 quit
```

10.1.2 {subsection} isolationex02.in : Trench Isolation Punchthrough

Requires: SSUPREM4/ELITE/SPISCES

This examples demonstrates punchthrough between unrelated n+ regions separated by trench isolation. It shows:

- trench formation by ELITE physical etch models
- trench doping using SSUPREM4 implant models
- trench fill by ELITE physical deposition models
- punchthrough test across the trench using ATLAS

The example file consists of two parts. The first uses ATHENA to construct the geometry and doping of two n+ areas separated by trench isolation. The second uses ATLAS to simulate punchthrough between these two regions.

Details of ELITE and SSUPREM4 syntax for trench formation and refill can be found in the appropriate ATHENA example sections.

The trench is formed by Reactive Ion Etching (RIE), with different isotropic and anisotropic etch rates for each material present. A field implant is performed directly into the trench.

The device is interfaced automatically into ATLAS. The two carrier mode is selected along with impact ionization. The contact named drain is ramped to 20 volts.

The final drain current contours are plotted at the end of the simulation, where the current density can be seen to avoid the field implant doping peak.

A design parameter is measured at the end of the ATLAS simulation using the `extract` statement. The parameter is defined as the voltage required on the drain to get $2e-12$ A/ μm of drain current.

To load and run this example, select the **Load example** button while this text is displayed. The input file and several support files will be copied to your current working directory at this time.

Once loaded into DeckBuild, select the **run** button to execute the example.

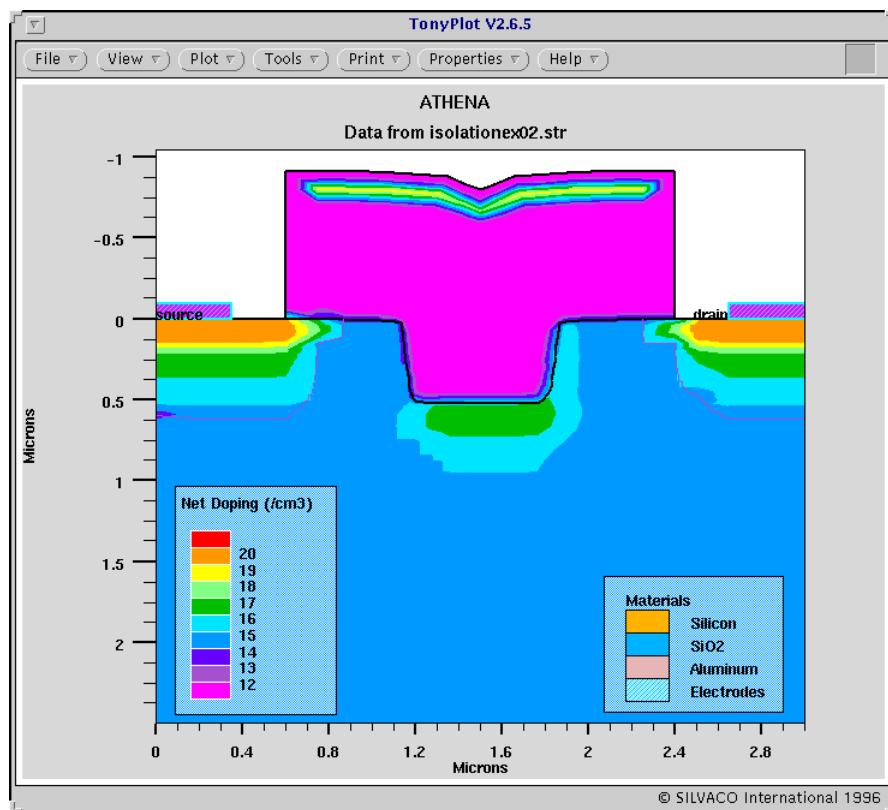


Figure 10.4: Shallow trench isolation structure defined in ATHENA. This test ramps the drain electrode

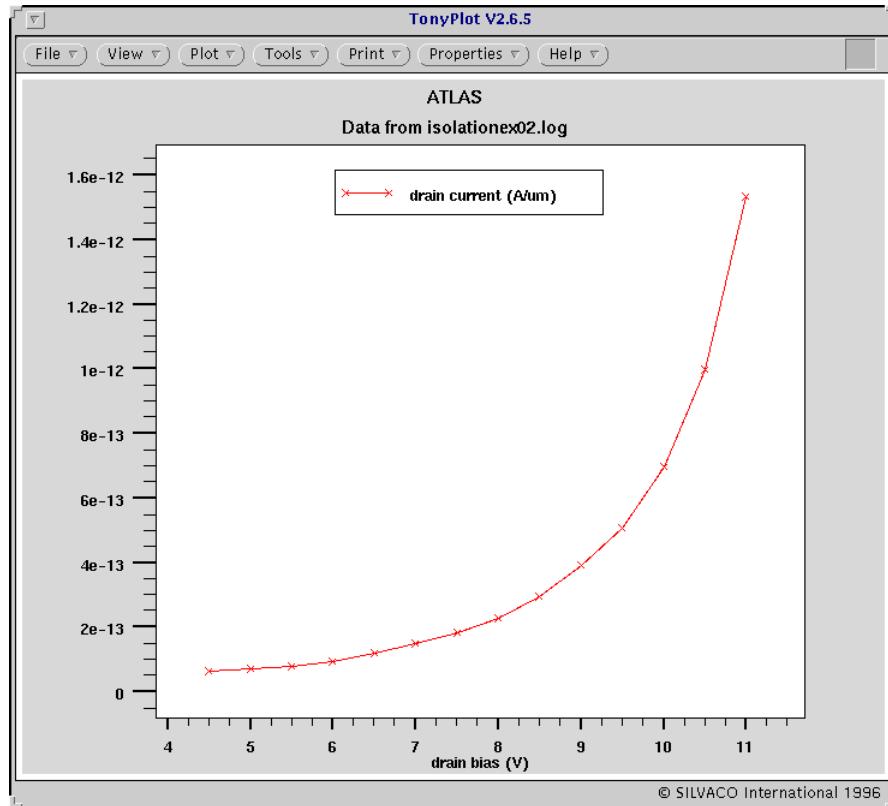


Figure 10.5: Curve of leakage from source to drain across the trench isolation

Input File isolation/isolationex02.in:

```

1 go athena
2 #TITLE: Trench isolation
3 #
4 set trench_bottom=0.5
5 line x loc=0.00 spac=0.20
6 line x loc=0.35 spac=0.1
7 line x loc=0.6 spac=0.1
8 line x loc=1.2 spac=0.02
9 line x loc=1.8 spac=0.02
10 line x loc=2.4 spac=0.1
11 line x loc=2.65 spac=0.1
12 line x loc=3.0 spac=0.20
13 #
14 line y loc=0.00 spac=0.02
15 line y loc=$trench_bottom spac=0.02
16 line y loc=2.5 spac=0.4
17 init silicon c.boron=1.0e15 orientation=100 spac=2

```

```
18  #
19  diffuse temp=900 time=25 dryo2 %hcl=3
20  #
21  deposit nitride thick=0.4
22
23  deposit photo thick=1. div=10
24  #
25  etch    photo    start x=1.2 y=-10
26  etch    photo      cont  x=1.2 y=10
27  etch    photo      cont  x=1.8 y=10
28  etch    photo      done   x=1.8 y=-10
29
30
31  relax y.min=0.4 dir.y=f
32  relax y.min=1.0 dir.y=f
33
34  etch nitride thick=0.5
35
36  strip photo
37
38  etch oxide thick=0.1
39
40
41  # Setup a silicon trench etching machine.....
42  rate.etch machine=trench_etch rie silicon iso=0.1 dir=0.9 u.m
43  rate.etch machine=trench_etch rie oxide iso=0.1 dir=0.9 u.m
44
45
46  etch machine=trench_etch time=0.5 minute dx.mult=0.5
47
48
49  # Oxidize the trench....
50  diffuse temp=925 time=10 weto2
51
52  # Implant the trench
53  implant boron energy=35 dose=1.2e12
54
55
56  # Strip off all the nitride
57  strip nitride
58
59  # Dip off the oxide
60  etch oxide all
```

```
61
62 # deposit a new oxide layer to fill the trench
63
64 deposit oxide thick=0.8 div=10
65
66 etch oxide left p1.x=0.6
67 etch oxide right p1.x=2.4
68
69 # S/D Implant....
70 implant arsenic energy=85 dose=2e15
71
72 # Final anneal...
73 diffuse temp=925 time=25 nitrogen
74
75
76 # now make electrode contacts and move it into device simulation.....
77 deposit alumin thick=0.1
78 etch alumin start x=0.35 y=-10
79 etch alumin cont x=0.35 y=10
80 etch alumin cont x=2.65 y=10
81 etch alumin done x=2.65 y=-10
82
83 electrode name=source x=0.1
84 electrode name=drain x=2.9
85
86
87 structure outf=isolationex02.str
88
89 tonyplot isolationex02.str -set isolationex02_0.set
90
91
92
93 # now switch to Device Simulation.....
94 go atlas
95 model cvt srh
96 impact selb
97
98 output flowlines
99
100 solve init
101
102
103 method newton
```

```
104 solve prev
105
106
107 solve vdrain=0.1
108 solve vdrain=0.2 vstep=0.2 vfinal=4 name=drain
109
110 log outf=isolationex02.log master
111
112 solve vdrain=4.5 vstep=0.5 vfinal=15 name=drain compl=1.3e-12 cname=drain
113
114 save outf=isolationex02_2.str
115
116 # Extract the design parameters.....
117 extract init inf="isolationex02.log"
118 extract name="isolation_vpt" x.val from
    curve(abs(v."drain"),abs(i."drain")) where y.val=1.3e-12
119
120 tonyplot isolationex02.log -set isolationex02_log.set
121
122
123 quit
```

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