

# Integrated Circuits Design for 5 GHz Wi-Fi: Radio Frequency Receiver Front-end *Senior Project Report*

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## Problem Statement

In the current state of integrated circuit (IC) technology, advances have made it such that fabrication technology has reached sizes below 15 nm. This has caused the focus to shift away from designing using outdated technologies and Process Design Kits (PDK). However, the latest processes are costly and acquiring the license for such technology is a lengthy process. This has led to research on how older processes can be used to generate similar or better results when implemented on current technologies, and if this is a practical solution for improving upon efficiency in the future. The selected area of interest is in improving upon Radio Frequency (RF) receiver front-end technology. Our front-end is intended for 5 GHz WiFi signal reception and is expected to be more cost-effective than existing front-ends, making it suitable for communication devices operating in the 5 GHz band. The results of our experimentation will prove whether the proposed solution of using older processes is viable.

Our team is working with Efabless, a New York based fabrication company, that offers affordable chip manufacturing and an open-source PDK called SKY130 that uses the 130 nm technology developed in 2000-2001. The design is challenging due to the constraints posed by this technology. For instance, some design metrics in 130 nm technology will not match up to those of modern chips. However, we will focus on prioritizing certain performance metrics (See 0.2 for targeted parameters) such that usage of the older technology exhibits a greater net positive in comparison. This will be done by manufacturing the desired chip technology and testing its real world performance on a printed circuit board (PCB) and RF test equipment.

## Background

### 0.1 Significance

The RF front-end in a receiver circuit is designed to process incoming radio frequency signals into the intermediate frequency (IF) signal for easier handling. Our design will only include the basic components of the front-end; consisting of a low-noise amplifier (LNA), a mixer, and a local oscillator (LO). The LNA amplifies the RF signal while minimizing noise. The mixer combines the RF signal with the LO signal, resulting in the IF signal, which is then sent to the rest of the receiver. We are designing a front-end to operate in the 5 GHz band to be used as a part of a WiFi receiver.

Figure 1 depicts a whole receiver chip. Our design will only include the LNA, Mixer, and LO.

The 2.4 GHz band is the most commonly used frequency band for WiFi. It falls within the ISM (industrial, scientific, and medical) band, which is a portion of the radio spectrum reserved for non-communication purposes. The 5 GHz band is also part of the ISM band, and while it is less commonly used than the 2.4

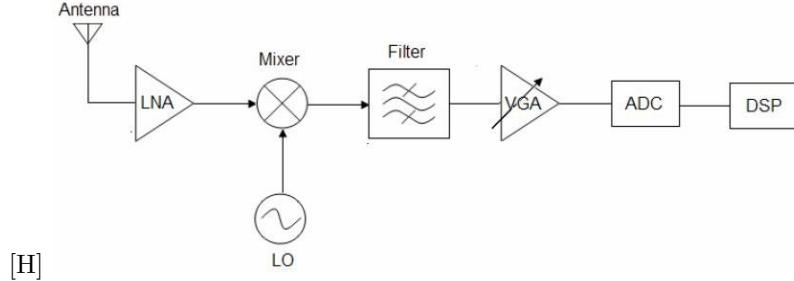


Figure 1: Block diagram of the whole receiver chip

GHz band, it has some advantages. For one, it is less prone to overcrowding, since most devices operate in the 2.4 GHz band. In addition, the 5 GHz band has more available channels (23 channels compared to 11 in the 2.4 GHz band), and it can offer faster speeds, though at the cost of shorter range.

This project aims to design a front-end that takes advantage of the 5 GHz band while accounting for the disadvantages of existing receivers. There already exists designs for a 5 GHz front-end but we are aiming to design a 5 GHz receiver using 130 nm technology, with a focus on improving the linearity. 130 nm technology refers to the sizing of the devices in the circuit. Older technologies have larger transistor sizes, which limits their design space, but they are more accessible than newer technologies. This project serves as a test of the ongoing usefulness of older technologies, such as 130 nm technology. While VLSI design techniques are constantly evolving, it is important to recognize that older technologies can still have value and should not be discarded without consideration. By designing a front-end using older technology, we can validate the use of older technologies. In addition, our design can be used towards advancing WiFi technologies. Either our design techniques can be used towards modern VLSI technologies or our chip itself could be added to existing devices.

## 0.2 Targeted Parameters

Among several parameters we are targeting, one of the most important is linearity. In general, linearity is the ability to provide an output signal that is directly proportional to the input signal. While some electronics components are linear (resistors, capacitors, inductors), all wireless receivers have some degree of non-linearity that can negatively impact performance. The two major effects from non-linearity are power compression and desensitization. Power compression is not desired because it can lead to amplitude and phase distortions in the received signal, and desensitization does not allow for the detection of input signals with low power. Improving the linearity is especially important if preservation of the input signal is crucial.

The dynamic range and the 1dB compression point are two quantifiable parameters that indicate the linearity of a receiver. The dynamic range measures the receiver's ability to process a range of input powers from the antenna. When the input power is too high due to a strong signal, gain compression occurs and this can decrease energy efficiency because the output power is no longer directly proportional to the input power. This is seen in the figure below. The range of output powers for which the relationship between the input and output power is linear is known as the blocking dynamic range (BDR) of the receiver. Formally, it is defined as the difference in dB between the minimum detectable signal (can be calculated through the noise figure and instantaneous bandwidth) and the maximum signal that causes a 1 dB compression. Therefore, the higher the 1 dB compression point, the better the receiver is at handling strong signals.

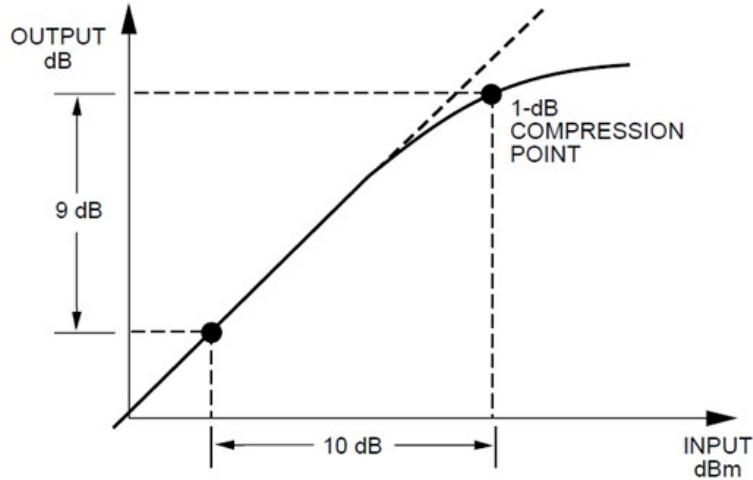


Figure 2: Blocking dynamic range of a receiver

Another way to assess the linearity of a receiver is to determine the spurious-free dynamic range (SFDR). It is defined as  $2/3$  of the difference between the third-order intercept point ( $IP_3$ ) and the noise floor (level of background noise that is present before signals are received), as seen in the figure below.

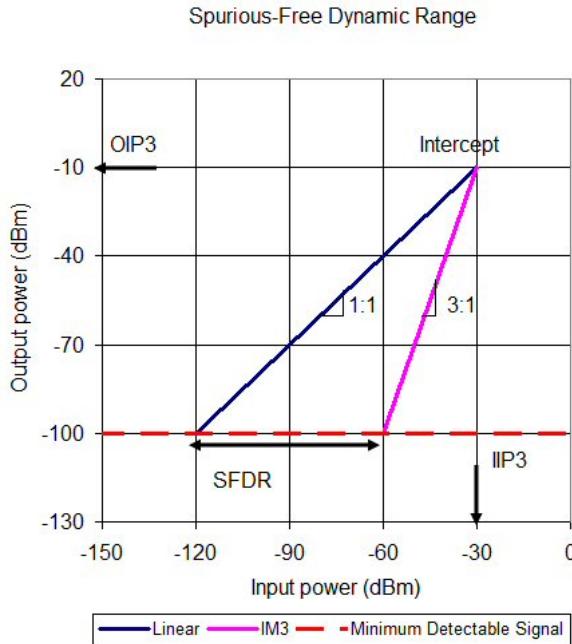


Figure 3: Illustration of the spurious-free dynamic range

The third-order intercept point is another figure of merit that specifies good or bad linearity for a receiver. It is associated with intermodulation distortion, which occurs when two or more signals are mixed. The frequency spectrum of the output of such a combination not only contains the original signals but also the sum and difference of the input signals along with their harmonics (integer multiples of the fundamental signal). The third order products, which we are most concerned about, are a result of the mixing between the second order products and the original frequencies. They are most concerning because they are difficult to filter out due to their proximity to the fundamental frequencies, as seen in the figure below.

## Harmonics & Intermodulation Products

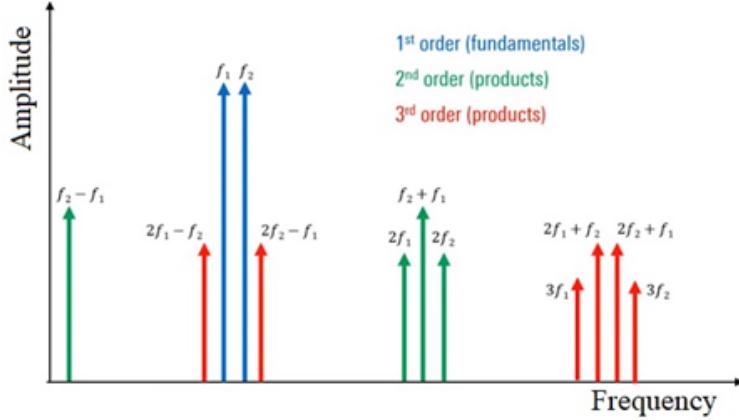


Figure 4: Frequency spectrum of two input signals

It can be extrapolated from a graph similar to the one below by extending the linear parts of the input tones (first order) and the nonlinear product (3rd order) curves for the input power versus the output power. The point at which they intersect is the third-order intercept point. The higher it is, the more linear the receiver is, and the less intermodulation distortion there is, making it easier to filter out higher order products.

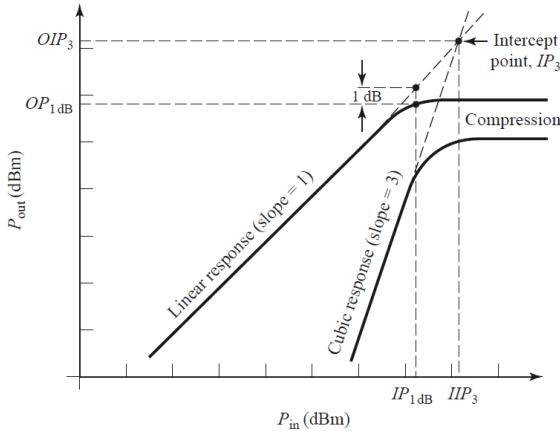


Figure 5: Illustration of third order intercept point

Besides linearity, the VSWR (voltage standing wave ratio) of a receiver is another useful parameter to take into consideration. It is a measure of how efficiently power is transmitted. The VSWR is also known to be a function of the reflection coefficient, which determines how much power is reflected. It is caused by any difference between the impedance of receiver and its surrounding network. The smaller VSWR is (minimum value is 1.0), the more power is transmitted to the antenna because less power is reflected. Improving this parameter is good when designing for a sensitive system that needs to pick up signals of low power.

Other parameters include noise figure and bandwidth. The noise figure is a measure of how much the receiver degrades the signal-to-noise ratio (SNR) of the incoming signal. As the signal passes through the multiple stages of a receiver, noise such as thermal noise (due to temperature increase) can add onto the total noise in the system and causes distortion in the output signal. By increasing the gain of the stages in the cascade through topological improvements, the noise figure can be increased. Likewise, the other parameters

mentioned in this section, and bandwidth, can be improved by increasing or decreasing one another. In the sections that follow, we will describe our design methodology and trade-off study for the low noise amplifier, mixer and oscillator with a focus on improving linearity.

### 0.3 State of the Art

As previously mentioned, we will compare our chip design it to other existing designs. However, there may not be an identical experiment for direct comparison. For example, we will consider a RF Front-End design that uses 180 nm technology [RWI05], which is similar to our design in concept but uses an older technology. This chip has a noise figure of 4.7 dB/5.1 dB, a dual gain mode of 5 dB/30 dB with an IIP3 of -1 dBm for low gain mode, and draws 25 mA/27 mA from a 1.8-V supply for the 2.4 GHz/5 GHz bands.

Another example is a 30 GHz Self-Oscillator Mixer that uses 130 nm technology [KC10]. While this chip is not as similar to our design as the RF Front-End, it still utilizes 130 nm technology, so we can compare some related parameters. Its specs include a down-conversion loss of 30 dB and a minimum LO injection power of -32 dBm.

See the the upcoming sections on individual block results and comparisons to existing designs.

## 1 Methodology

Our design will focus on improving linearity, although we will also consider other performance metrics. Power consumption is not a high priority as linearity is more important in the context of our 130 nm technology.

We will use the RF Microelectronics textbook [Raz11] as a reference for researching our individual blocks. Based on this research, we will decide on the topologies for our blocks that will help us meet our performance goals. We may also make adjustments to our block designs based on the requirements of the other blocks in the circuit. By carefully considering the design of each block, we can ensure that the RF front-end is optimized for the desired performance parameters. Each individual block has its own ways of optimizing linearity, so their design process will review how linearity can be improved. We are using the SKY130 PDK to design our blocks. Initially, we intended to utilize the efabless Docker environment, which includes XSchem for circuit design and NGSpice for simulation. However, after reconsidering these tools, we have decided to import the SKY130 PDK into our Cadence environment and use ADE L for simulation of our circuit instead.

## 2 LNA

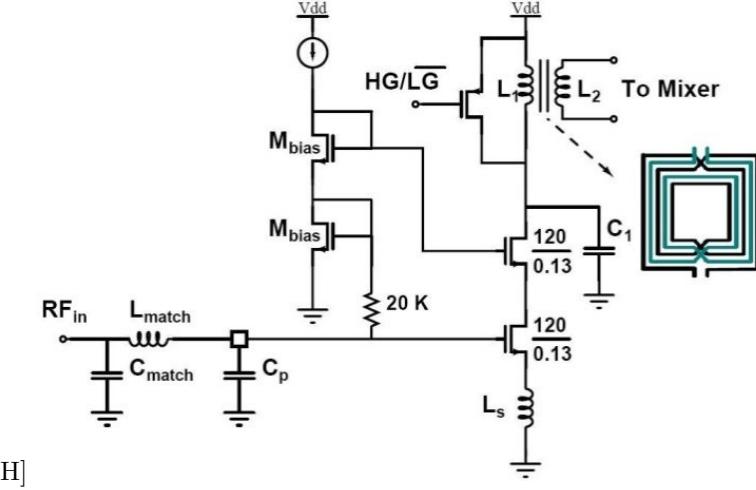


Figure 6: Example of an LNA design

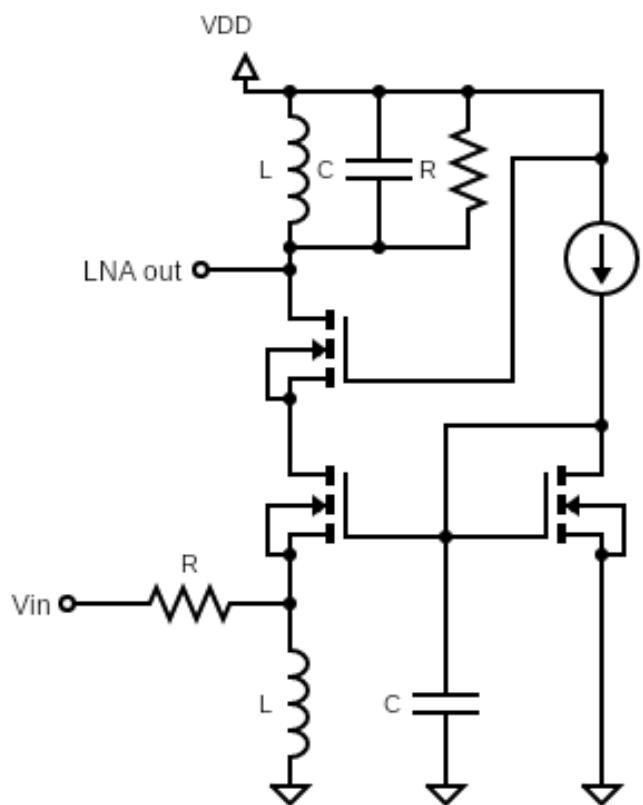
Like most amplifiers, a LNA is designed to amplify input signals. A low-noise amplifier (LNA) is a type of amplifier that is designed to amplify weak signals, usually received from an antenna, while minimizing any additional noise. LNAs are useful in radio frequency (RF) circuits, where they can amplify signals with a low signal-to-noise ratio (SNR). LNAs are typically characterized by their low noise figure, which measures the amount of noise added to the output signal. LNAs with a low noise figure are able to amplify weak signals without significantly degrading the signal-to-noise ratio. In addition to the noise figure, LNAs may also be characterized by their gain, linearity, and power consumption. The gain of an LNA is a measure of the amount by which the signal is amplified, and linearity refers to the LNA's ability to accurately amplify signals over a range of input levels. Power consumption is also an important factor, as LNAs are often used in battery-powered devices where low power consumption is a key concern.

LNAs consume a small fraction of the overall power for a front end, meaning this design should focus on improving the noise figure. However, there are challenges associated with designing LNAs, such as parasitic effects that can introduce noise and produce a high return loss (S11).

LNA designers must decide between two primary topologies: common gate (CG) or common source (CS). CG LNAs offer a more robust input resistance but may have a higher noise figure, while CS LNAs have a lower noise figure but may have a lower input resistance. Since this design requires a higher linearity, a CG LNA design with cascode is used.

There are also other topologies with different features to consider:

1. Voltage-voltage feedback:
  - (a) Input resistance can be substantially higher than  $1/g_m$
  - (b) NF can be lowered by raising  $g_m$
2. Feedforward:
  - (a) Avoids the tight relationship between input resistance and noise figure
  - (b) Difficult to realize feedback with an active circuit
3. Reactance-cancelling:
  - (a) Inductive input impedance of a negative-feedback amplifier cancels input capacitance
  - (b) Input matching only holds up to  $\omega_0$
4. Gain switching:



[H]

Figure 7: CG Cascode LNA Schematic

- (a) Switch gain modes
- 5. Band switching:
  - (a) Operates across a wide bandwidth or in different bands
- 6. Differential:
  - (a) Achieve high  $IP_2$ 's
  - (b) Needs a balun circuit to convert single-ended input to a differential input

In case the parameters of the cascode common gate structure are inadequate or depending on the performance of other blocks, these alternate configurations or topologies can be utilized.

## 2.1 Calculations

The following equations are used to calculate the parameters of the cascode CG LNA. The LNA design will be tweaked based on these equations to meet specifications.

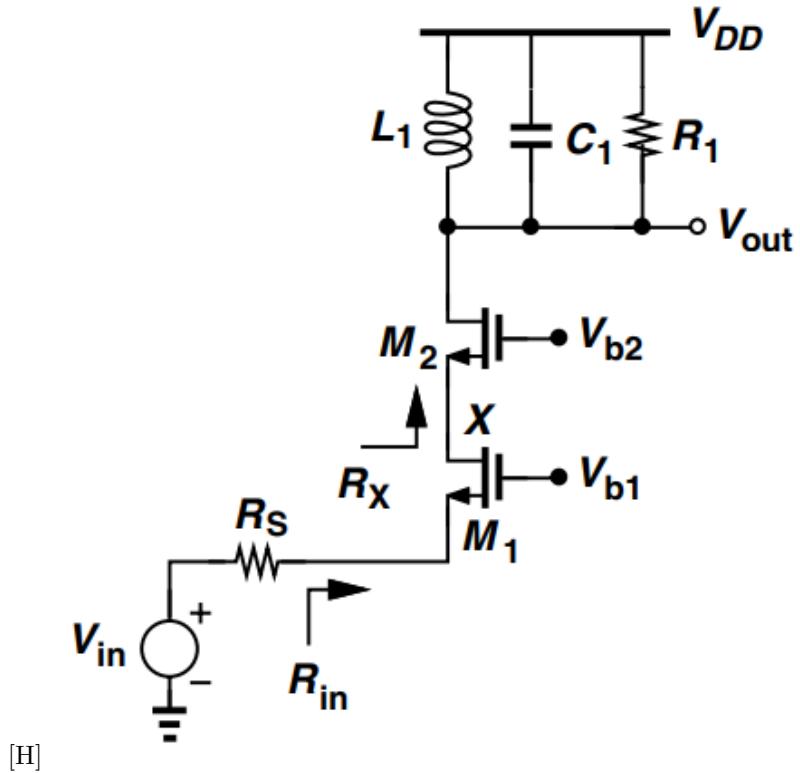


Figure 8: CG Cascode LNA Calculations

**Input impedance** Input impedance refers to the impedance that a source will see looking into the LNA.

$$R_{in} = \left( \frac{R_1 + r_{O1}}{1 + g_{m2}r_{O2}} + r_{O1} \right) / (1 + g_{m1}r_{O1}) \quad (1)$$

$$\approx \frac{1}{g_{m1}} + \frac{R_1}{g_{m1}r_{O1}g_{m2}r_{O2}} + \frac{1}{g_{m1}r_{O1}g_{m2}} \quad (2)$$

$$\approx 1/g_{m1} \quad (3)$$

Thus choose  $R_s$  equal to  $1/g_{m1}$

**Gain** Gain refers to how much the input will be amplified by the circuit.

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m2}R_1C_Xs}{(C_{GS2} + C_X)s + g_{m2}} \quad (4)$$

As seen in the indicators of high linearity, gain corresponds to good linearity. Thus, we will design the LNA to optimize gain while also preserving input matching.

## 2.2 Design Process

The design procedure for a circuit begins by determining the dimensions and bias current for a transistor in order to achieve a specific transconductance. Circuit simulations can be used to plot the transconductance and FT of a transistor as a function of drain current, and the combination of width and current that provides the optimal balance between speed and power consumption can be selected. The required transconductance can then be achieved by scaling the width and current proportionally. The next step involves determining the necessary value of an inductor in the circuit based on the pad capacitance and the frequency of operation, potentially requiring some iteration. The bias of another transistor in the circuit is then defined, and the width of a third transistor is chosen to optimize its performance while minimizing the capacitance at a particular node. The layout of the transistors can also be modified to further minimize the capacitance at the node. Finally, the performance of the overall circuit is simulated to confirm that it meets the desired specifications.

## 2.3 Simulation Results

Cadence Virtuoso was used to simulate the cascode common gate LNA. The schematic and testbench utilized in the simulation are illustrated in the following images. Two testbenches were employed - one for measuring the 1 dB compression point and gain, and the other for measuring S11, IIP3, and Noise Figure.

To optimize the gain of the LNA, the input NMOS was configured with a W/L ratio of 50\*1/0.15 um, while the cascode NMOS had a W/L ratio of 4\*100\*2/0.15 um. The LC tank was designed to have the gain peak at 5.965 GHz. An input resistor was also included for impedance matching at 50 Ohms. The bottom inductors and capacitors were sized to the minimum requirements for AC biasing.

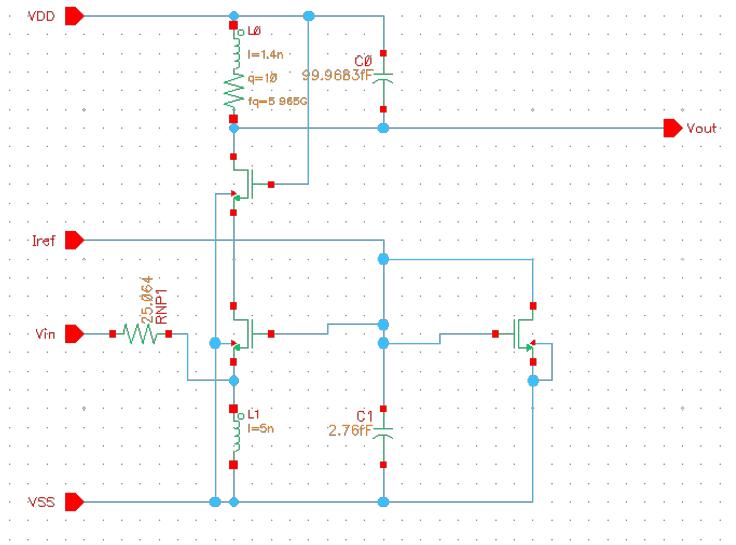


Figure 9: LNA Schematic in Cadence

To evaluate the LNA, a port component was utilized. Ports are capable of generating a variety of signals and harmonics, and can also be used to measure 1 dB compression points, IIP3s, and S parameters. A second setup was used in the second test bench in order to measure the gain of the circuit.

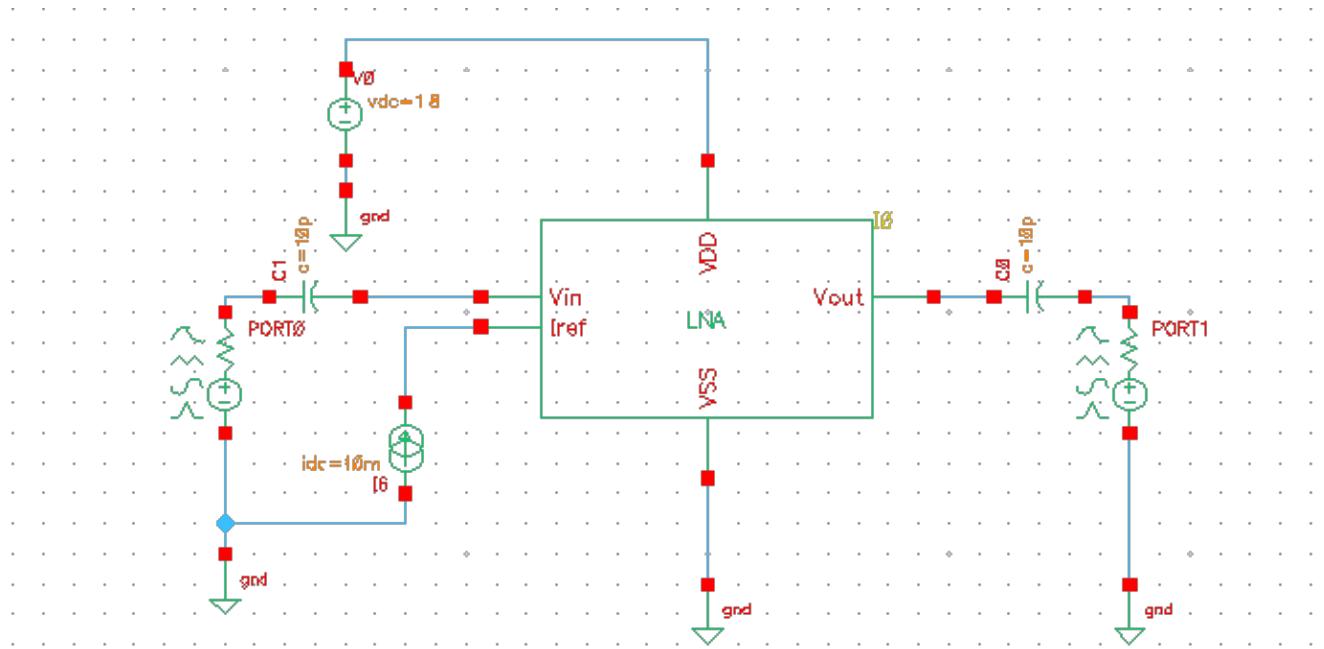


Figure 10: LNA TB Setup

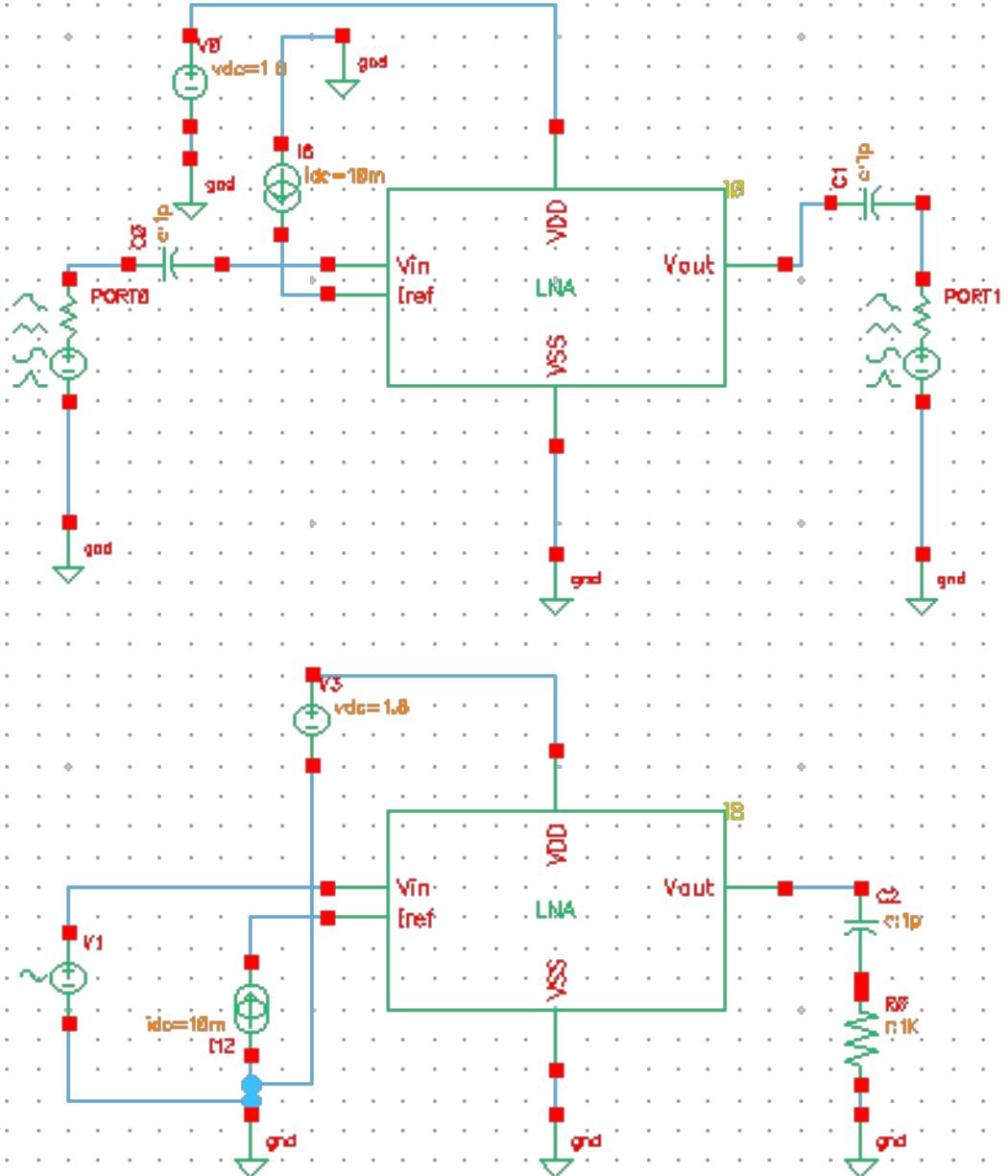


Figure 11: LNA Second TB Setup

Displayed below is the table of the parameters compared to the target specifications.

	Reference Specifications	Our Specifications
Gain	15 dB	12.59 dB
1 dB Compression Point	-29.2 dBm	14.05 dBm
IIP3	-19 dBm	20.01 dBm
Noise Figure	2 dB	10.58 dB
Power Consumption	30 mW	16.88 mW

Compared to the reference sources, our specifications were performed better in every regard except for gain and noise figure. Nevertheless, the linearity of our design surpassed that of the reference specification, which was the primary objective of this design.

Displayed below are the simulated plots for the parameters of the LNA.

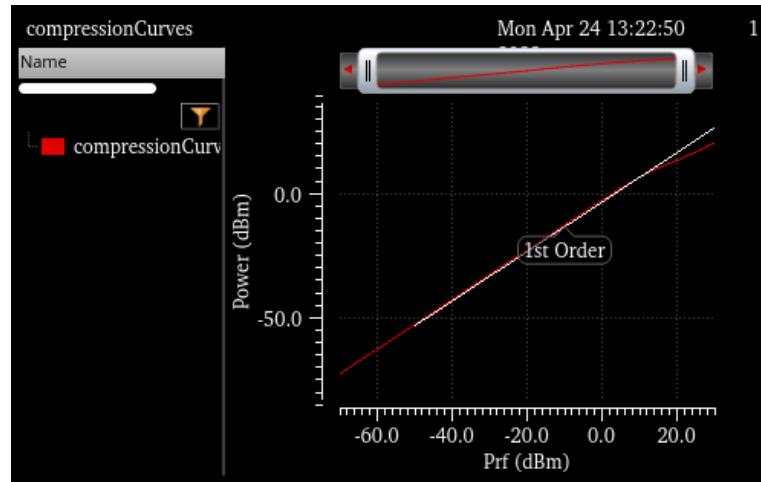


Figure 12: LNA 1dB Compression Result

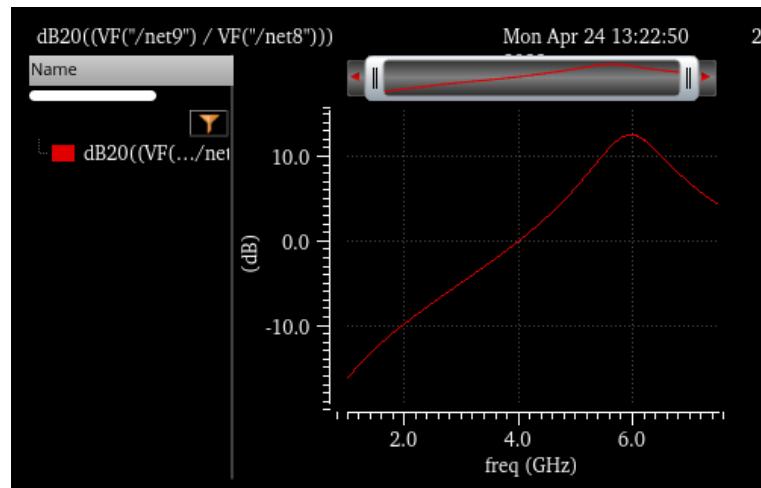


Figure 13: LNA Gain

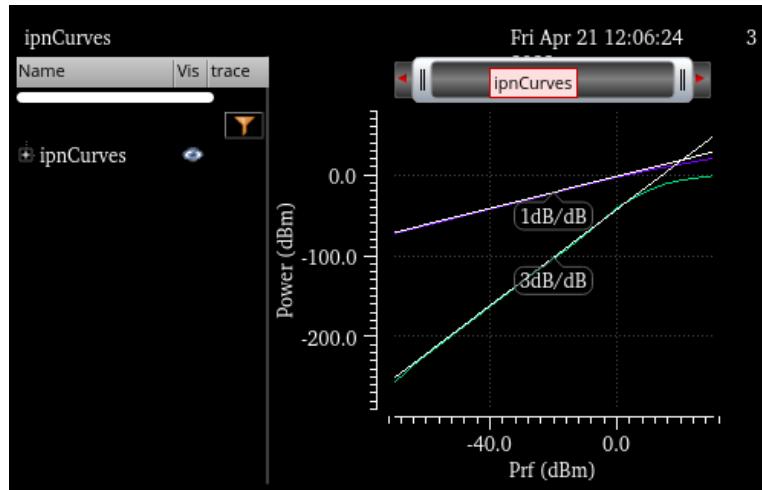


Figure 14: LNA Input Referred 3dB Compression

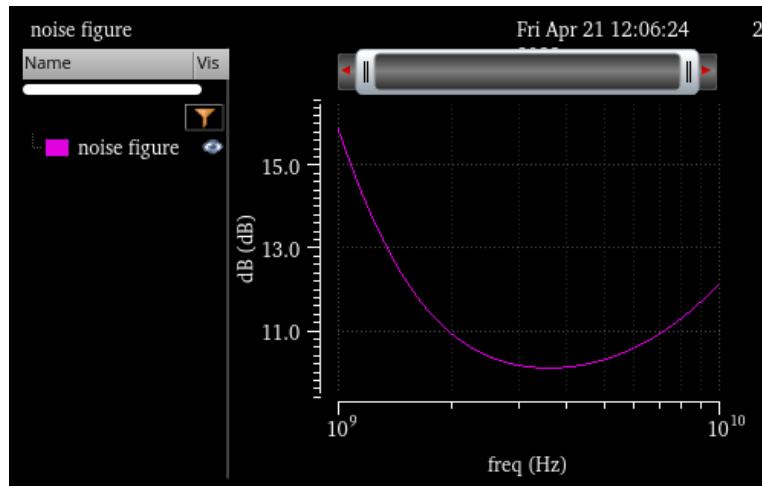


Figure 15: LNA Noise Figure

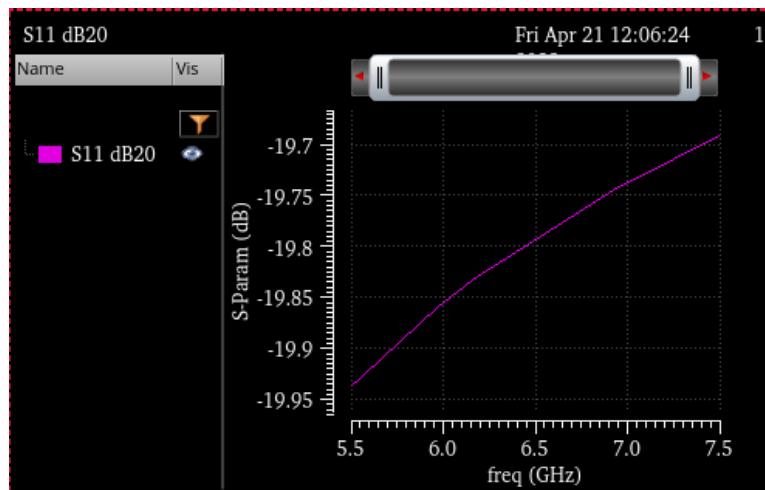


Figure 16: LNA S11 Parameter

### 3 Mixer

Receiver mixers are three-port devices that perform down-conversion by multiplying the RF signal, the LO waveform, and possibly their harmonics. The main purpose of a mixer is to change the frequency while still maintaining the other characteristics of the signal, such as phase and amplitude. The main performance parameters include noise, linearity, gain, port-to-port feedthrough, voltage headroom, and input impedance.

First, the design entails a compromise between the noise figure and the linearity (IP3: third order intercept point) of the mixer. The mixer must provide sufficient gain to suppress noise coming from subsequent stages, but it is difficult to achieve a gain of more than 10 dB while maintaining linearity due to low supply voltage levels. It ultimately becomes a trade off between power consumption and noise levels of the other stages.

Due to device capacitances, mixers also suffer from port-to-port feedthrough (coupling). This effect depends on the architecture (symmetry of the circuit) and the LO waveforms. In this project, a crucial part of the design process is choosing the appropriate architecture (for instance, heterodyne vs. direct-conversion, single-balanced vs. double-balanced) to meet the desired parameter specifications. There are also different mixer typologies that can be studied and fine tuned, such as active mixers with current-source helpers and enhanced transconductance. See the upcoming subsection.

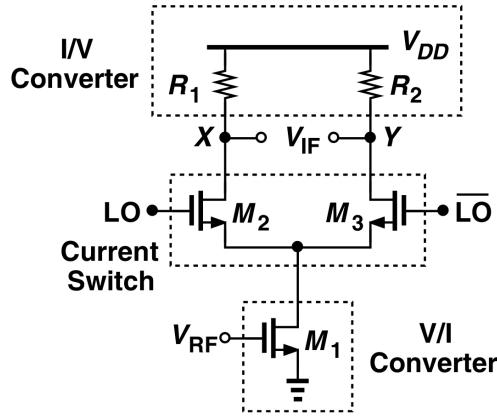


Figure 17: Single-balanced active mixer

#### 3.1 Mixer Topologies

##### 3.1.1 Active Mixers with Current-Source Helpers

The main difficulty in the design of active mixers comes from the conflicting requirements between the input transistor current (needs to be high to meet noise and linearity specifications) and the load resistor current (which has to be low enough to allow large resistors and hence a high gain). Therefore, adding current sources in parallel with the load resistors would help by allowing larger resistor values. A higher load resistor also reduces its input-referred noise contribution.

However, the addition of the current source helpers degrades the linearity because it is assumed that they operate at the edge of saturation so to minimize their noise current, but this condition drives them into the triode region when signals are present. This would be a good topology if achieving high gain is prioritized over linearity, but this is not the case for our project. If we had more time, we could have implemented this and tried it out.

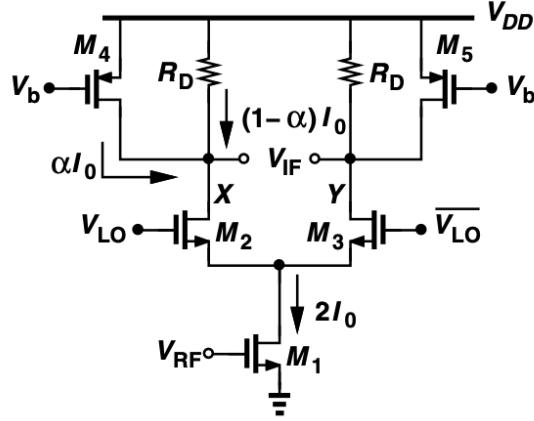


Figure 18: Addition of load current sources to relax headroom constraints

### 3.1.2 Active Mixers with Enhanced Transconductance

Instead of inserting the current source helper in the IF path (shown in the previous topology), it can be inserted in the RF path. This is to provide most of the bias current of M1 (see figure below) by M4. This would reduce the current flowing through the load resistors and the switching transistors. Lower bias current switched by M2 and M3 also translate to a lower overdrive voltage and more abrupt switching.

There are two issues with this topology: first, the additional current source contributes to the parasitic capacitance at node P, reducing the gain. Second, the noise current of the current source adds to the total noise currents. This capacitance and noise contribution can be suppressed with an inductor placed in series with the drain of M4. However, inductor parasitics must be managed carefully.

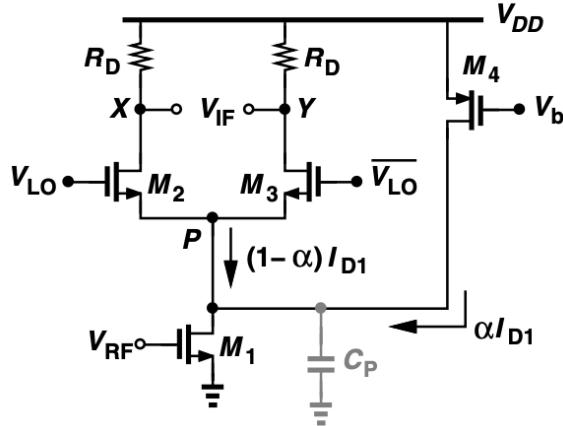


Figure 19: Addition of current source to tail of switching pair

The figure below shows another topology that can lead to lower flicker noise at the output due to the presence of capacitive coupling. Once again, this topology was a possible choice, but it involves the usage of an inductor, and this can be time-consuming on our end as we would have to design the inductor during the layout process of the design.

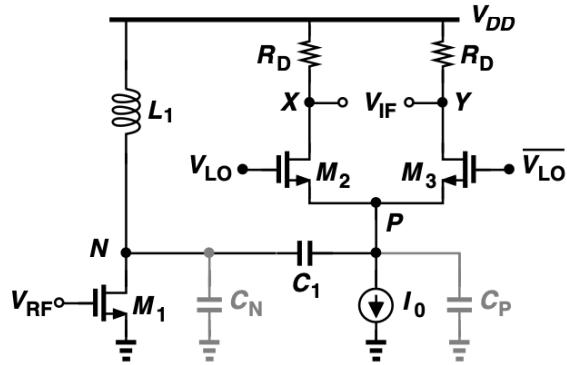


Figure 20: Active mixer using capacitive coupling with resonance

There are additional mixer topologies as suggested by [Raz11], but they are preferred topologies for direct-conversion rather than heterodyne mixers.

### 3.2 Design Considerations

Double-balanced mixers require an additional balun to convert a single-ended output to a differential one. However, they are better for linearity, and because that is the specification we are focusing on, we were considering using them. However, we would have to use a balun to feed the LNA output into the mixer (a double-balanced mixer) and this makes the layout more complicated. We could also change the design of the LNA to have differential outputs, but this could create further complications in design. Due to our time constraint, we decided not to go with the double-balanced mixer for our design.

The single-balanced active mixer consists of three main parts, as shown in the figure below: the I/V converter, current switch, and the V/I converter. Here, the  $M_1$  transistor converts the input RF voltage to a current. The other two transistors  $M_2$  and  $M_3$  (switching pair) steers this current to the left or to the right. Finally, the resistors convert the output currents to voltage.

One of the parameters that we are using to measure the mixer's performance is conversion gain. It can be shown [Raz11] that the voltage conversion gain of the single-balanced active mixer is

$$\frac{V_{IF,p}}{V_{RF,p}} = \frac{2}{\pi} g_{m1} R D \quad (5)$$

From this expression, we see that in order to increase the conversion gain of the mixer, we increase the transconductance  $g_{m1}$  of the driving MOSFET or the value of the resistors. However, increasing the resistance decreases the DC voltage at the output, driving the transistors into the triode region. On the other hand, increasing  $g_{m1}$  increases the current, which can also drive the transistors into the triode region. A careful balance between the two will yield a reasonable conversion gain.

In addition, while the transconductance of the other two transistors are not in the expression, it does impact the amount of drain current that goes through both branches and the DC biasing, and vice versa. This is reflected in the expressions for transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \quad (6)$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (7)$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \quad (8)$$

Depending on which variable is fixed, the DC biasing and the sizes of the transistors can be adjusted to achieve the desired transconductance and drain current.

From the topology of the single balanced mixer, the driving transistor is in common source configuration so that the source of the transistor is connected to  $V_{SS}$  or ground. Given  $V_{TH}$  and a DC bias voltage, the quantity  $(V_{GS} - V_{TH})$  will remain constant. The size of the transistor should be adjusted to achieve the appropriate transconductance and total drain current  $I_{RF} = I_1 + I_2$ , where  $I_1$  and  $I_2$  are the drain currents running through the two branches.

To target the drain current, one can refer to its expression (for an NMOS transistor in saturation while neglecting channel modulation):

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (9)$$

See the next section on the specifics of the design process pertaining to the mixer that is designed for this project.

### 3.3 Simulation Setup and Results

The single balanced mixer design was simulated in Cadence Virtuoso. The schematic and the testbench are shown below.

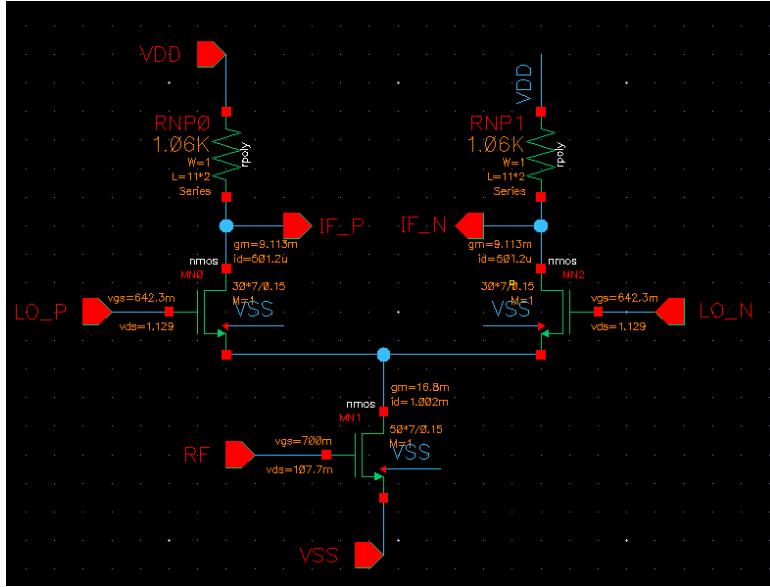


Figure 21: Mixer Schematic

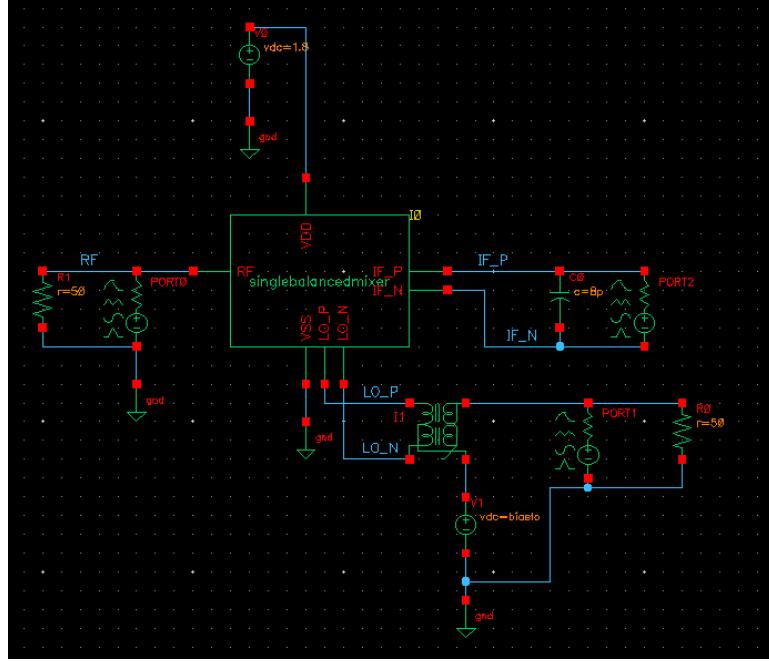


Figure 22: Mixer Testbench

In the testbench, the RF pin of the mixer is connected to a port that simulates the input from the LNA. Likewise, the negative and positive LO pins are connected to a port using a balun. This balun is only used in the individual mixer simulation and will not actually be in the design.

The DC bias of the LO port is set to 700 mV and the bias of the RF port is set to 800 mV. These bias values are determined so that the transistors are in saturation. To be in saturation,  $V_{DS} \geq V_{GS} - V_{th}$ . The  $V_{th}$  for the NMOS devices in this design is 690 mV, so the bias voltages were chosen to be close in value so that the transistors would most likely be in saturation.

Without the appropriate sizing, the transistors cannot operate in saturation either. The maximum W/L ratio that was allowed was 7 um / 0.15 um, so to change the overall size of the individual transistors, the number of fingers was increased. For the RF transistor, the number of fingers was set to 50, and for the LO transistors, the number of fingers was set to 30. This is enough for reasonable transconductance values for all three transistors.

The resistance was chosen so that the DC voltage at the outputs is close to 1 V (so that there is only a 0.8V drop across each of the resistors).

With this configuration, we were able to achieve the following results. The specifications achieved by this mixer design is on the right column of the table, and the reference specifications from a paper [Rad+20] on a 180 nm double-balanced mixer are listed on the left column.

	Reference Specifications	Our Specifications
Conversion Gain	12 dB	5.82 dB @ 10 dBm LO Power
1 dB Compression Point	n/a	-6.014 dBm
IIP3	-4.5 dBm	-3.029 dBm
Noise Figure	12 dB	15.11 dB @ 10 dBm LO Power
Power Consumption	3.4 mW	2.96 mW

Compared to the reference specifications taken from a paper on a double balanced mixer using 180 nm technology, our conversion gain of 5.82 dB is less than 12 dB. However, the other specifications, such as the IIP3, noise figure and power consumption are better. Our mixer is more linear, despite having the disadvantage of being single-balanced instead of double-balanced.

Here are the comprehensive results from the simulation.

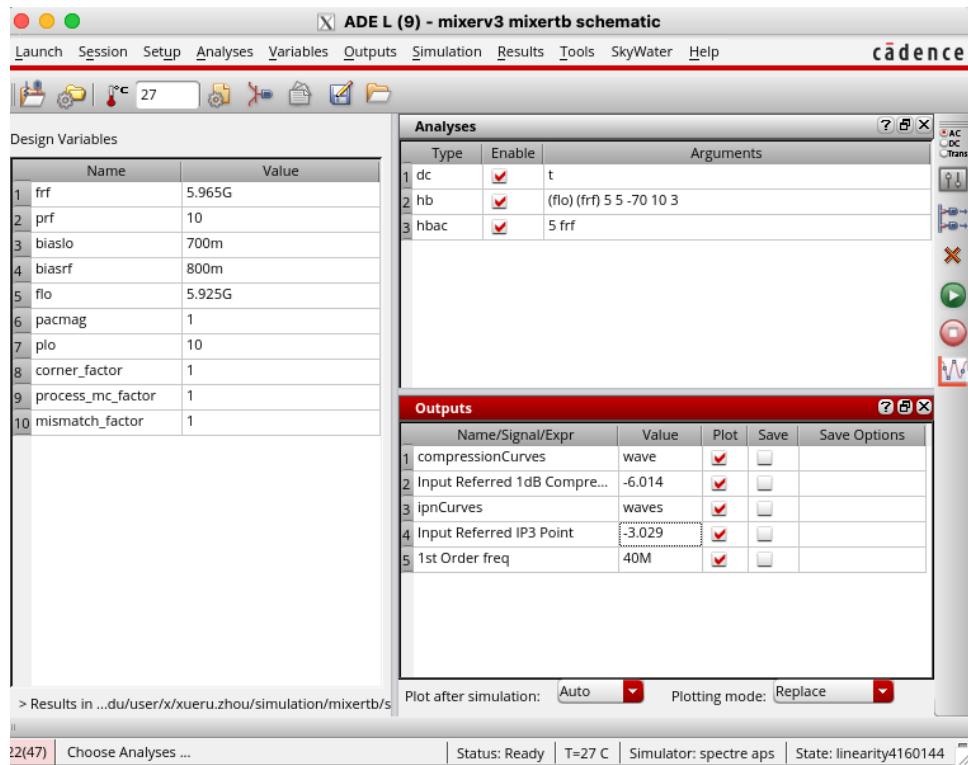


Figure 23: Values shown in ADE L

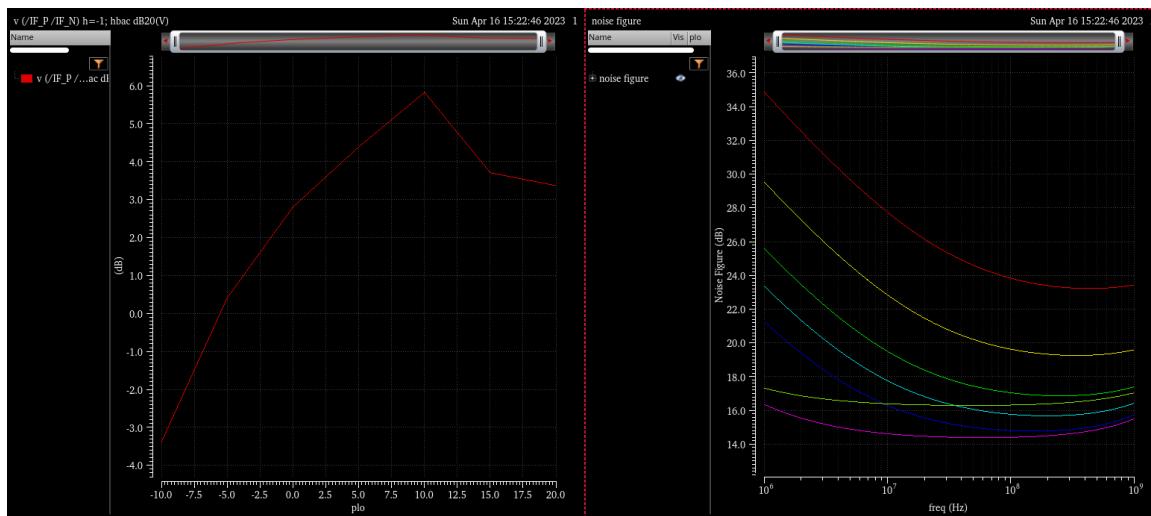


Figure 24: Mixer Conversation Gain and Noise Figure

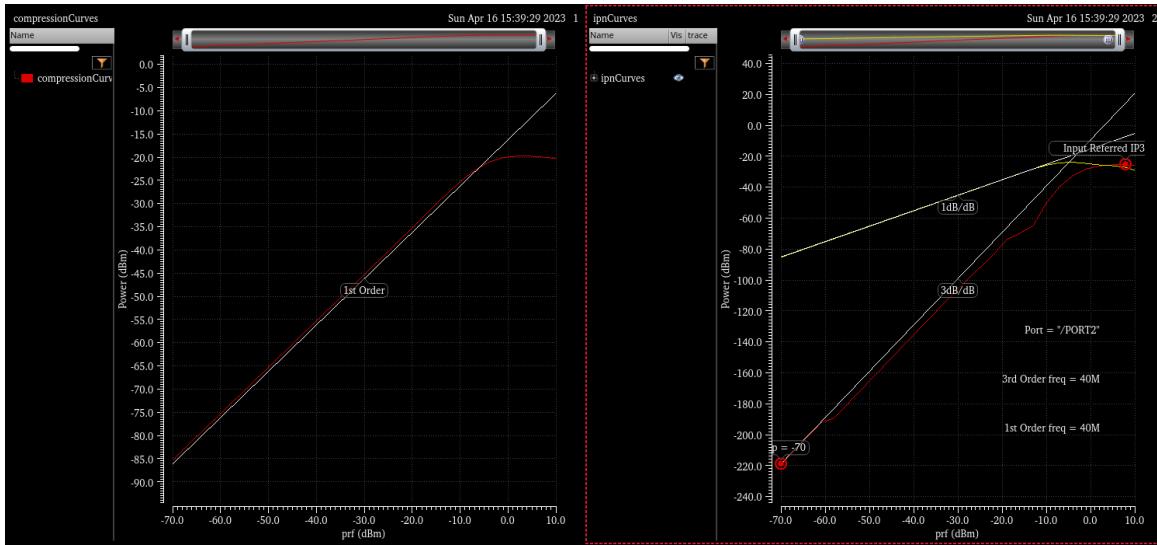


Figure 25: Mixer linearity graphs: compression curves (left) and IPn curves (right)

## 4 Local Oscillator

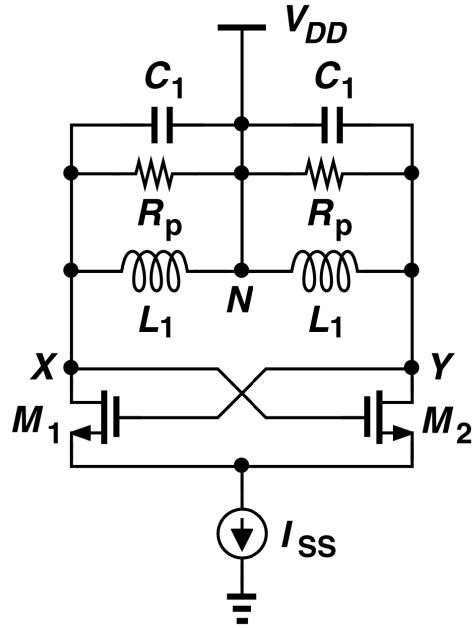


Figure 26: Cross-Coupled Oscillator

The local oscillator generates a stable frequency signal, which is mixed with the incoming RF signal in a process known as heterodyning. This mixing results in the production of sum and difference frequencies, one of which is the desired intermediate frequency (IF) signal. The IF signal, being at a lower frequency, is easier to process and demodulate, allowing for the efficient extraction of the embedded information. Therefore, the local oscillator's performance directly impacts the heterodyne receiver's sensitivity, selectivity, and overall system performance. A well-designed local oscillator must meet several critical requirements, including frequency stability and low phase noise. Frequency stability ensures that the generated LO signal does not drift, which could result in inaccurate frequency conversions and potential signal loss. Low phase noise is crucial for maintaining a high signal-to-noise ratio (SNR) in the receiver, as excessive phase noise can lead to signal degradation and reduced receiver sensitivity.

## 4.1 Design Process

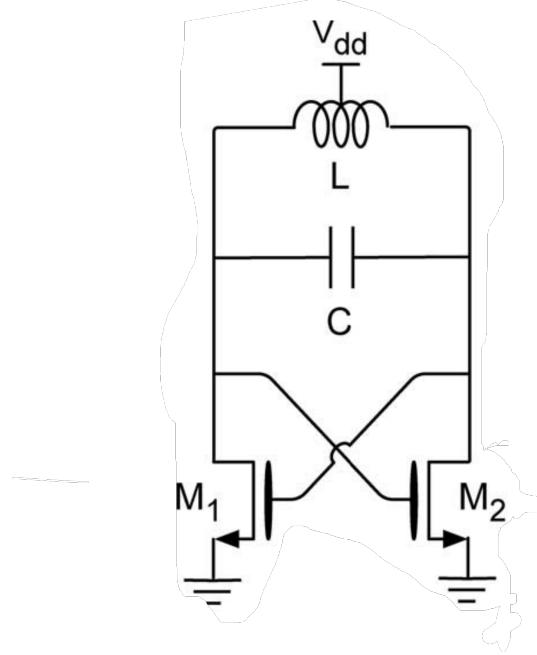


Figure 27: Class-D Oscillator

The topology selected is the Class-D differential oscillator [FA13]. Overall, Class-D oscillators offer a combination of high efficiency, small size, high frequency operation, and low noise, which makes them attractive for a wide range of applications. Additionally, they operate in a switching mode that allows them to only consume power when switching between states, rather than constantly consuming power like other types of oscillators. The Class-D Oscillator generally produces less phase noise when compared to its B/C counterparts with the same amount of power consumption, which increases its appeal when considering for our purposes performance is of the utmost importance. It also offers an oscillation amplitude approximately three times greater than its Vdd input due to the absence of the tail impedance, leading to further improvement of the phase noise. Lastly, this design offers a much lower complexity when compared to its B/C architectures, as it does not necessitate the current bias circuitry that is typically needed in Class-B/C Oscillators that could lead to potential phase noise issues.

There are certain trade-offs to take into account with our design. The transistors of the oscillator must be designed such that they behave as excellent switches, which aids in higher efficiency, lower noise, and improved linearity. To do this, the dimensions of the device is selected such that the width is very large because of the inverse relationship between the width and the on resistance of the MOSFET. Due to the 130nm technology, this has the added effect of increasing the power consumption and decreasing the switching speed because of a large parasitic gate capacitance. However, because of the increased transconductance and the reduced flicker noise, there may be incentive to increase the transistor width and sacrifice some specifications to prioritize others.

## 4.2 Simulation Setup

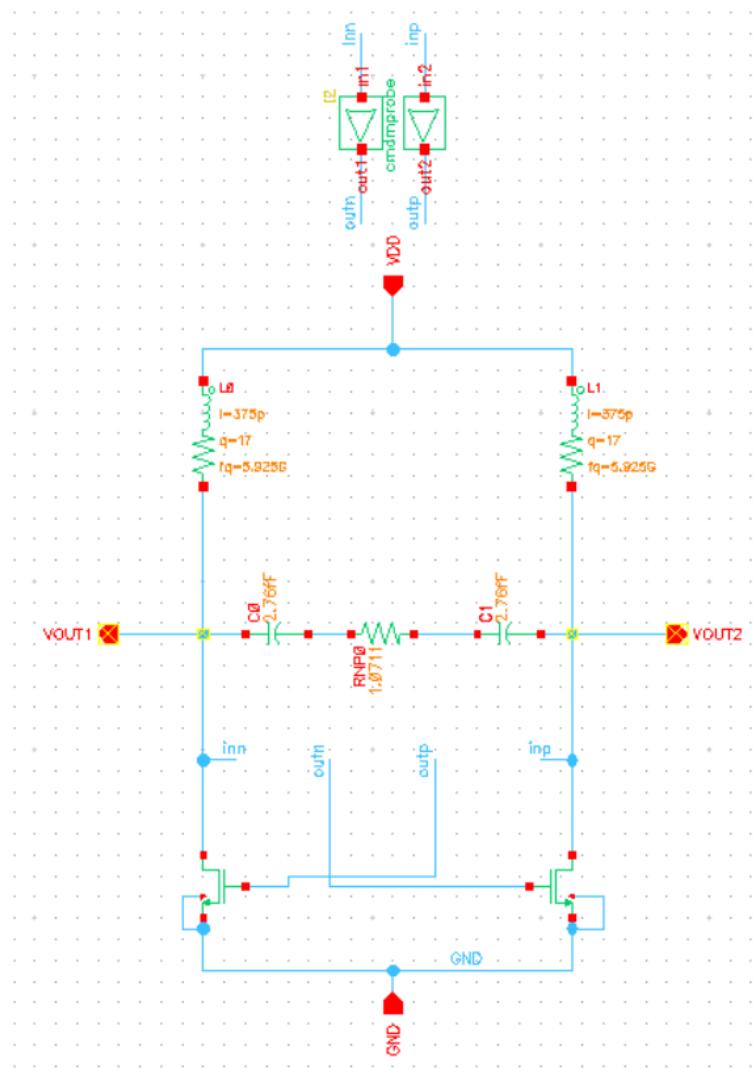


Figure 28: Class-D Oscillator Schematic

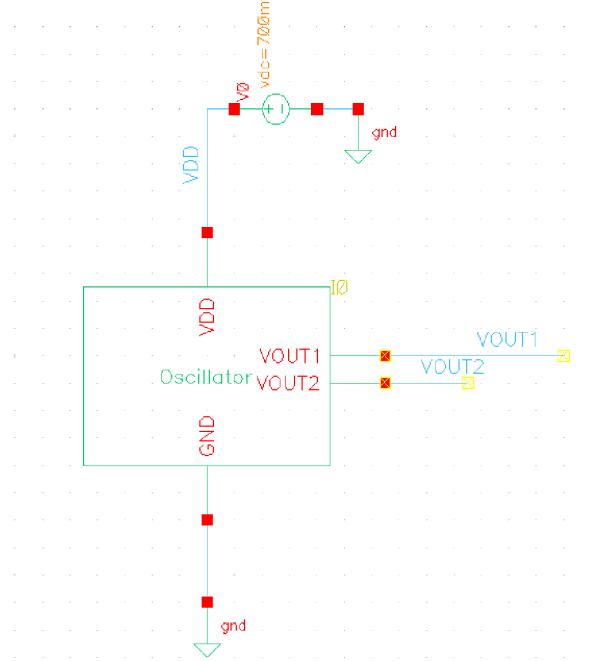


Figure 29: Oscillator Testbench

The schematic and testbench for the Class-D oscillator are presented above. It should be noted that the additional probes in the schematic are for analysis of the loop gain of the device. The W/L ratio for both transistors in the oscillator is set at (700  $\mu\text{m}$ /150 nm), which is relatively high. This high W/L ratio has been chosen in order to improve phase noise performance, as previously discussed.

To compensate for the potential drawbacks of the increased MOSFET width, such as slower switching speeds due to higher parasitic capacitances, inductor values have been carefully selected. These inductors serve to enhance the switching speed of the device and maintain optimal oscillator performance based on:

$$\omega = \frac{\sqrt{2}}{\alpha} \sqrt{\frac{1}{LC}} \quad (10)$$

where alpha is an attenuation term based on the periodic nature of the LC tank designed. It is important to note that the inductors used in the simulation setup will be implemented on a printed circuit board (PCB) during the actual testing of the complete device. This is due to the fact that the SkyWater software utilized for this design does not support on-chip inductor design.

While designing and simulating the circuit, there were specifications that were being used for performance comparison. It should be noted that there is no direct study to use for comparison of using the Class-D Oscillator in an RF front-end for Wifi 6, so the metrics being compared are for lower frequency purposes. However, the studies [FA13] [Koo+19] use more advanced technology that make them valid for comparison use. Also, in the case of [Koo+19], the study uses an FBAR resonator specifically to cater towards low phase noise specifications at differing offset frequencies, making it useful as a comparison with my own design.

Also, as previously mentioned, loop gain is measured, but it is not a metric that is comparatively used. However, it is important to ensure that the Barkhausen criteria is met for the oscillator, which is shown below:

1. The magnitude of the loop gain must be equal to or greater than 1:

$$|A\beta| \geq 1 \quad (11)$$

2. The total phase shift around the loop must be an integer multiple of  $360^\circ$  at the oscillation frequency:

$$\angle(A\beta) = 2n\pi \quad (12)$$

where  $n$  is an integer.

A high loop gain at zero phase ensures that the Barkhausen criterion is satisfied. By meeting these conditions, the oscillator can produce a stable and consistent output signal with minimal distortion and noise. Furthermore, a high loop gain improves the oscillator's start-up time, ensuring that the oscillations begin quickly and reliably when the oscillator is powered on.

### 4.3 Results

As previously mentioned, there are specifications from previous research that were used as comparison, as seen below, along with graphics depicting the results from simulations.

	Reference Specifications	Our Specifications
Phase Noise @ 1kHz:	-68.6 dBc/Hz [Koo+19]	-51 dBc/Hz
Phase Noise @ 10kHz:	-96.4 dBc/Hz [Koo+19]	-81 dBc/Hz
Phase Noise @ 100kHz:	-127 dBc/Hz [Koo+19]	-104.5 dBc/Hz
Phase Noise @ 1MHz:	-125 dBc/Hz [FA13]	-125 dBc/Hz
Phase Noise @ 10MHz:	-146.5 dBc/Hz [FA13]	-145 dBc/Hz
Power Consumption:	n/a	18.6 mW
FoM @ 10MHz:	217 dB [Koo+19]	217.8 dB

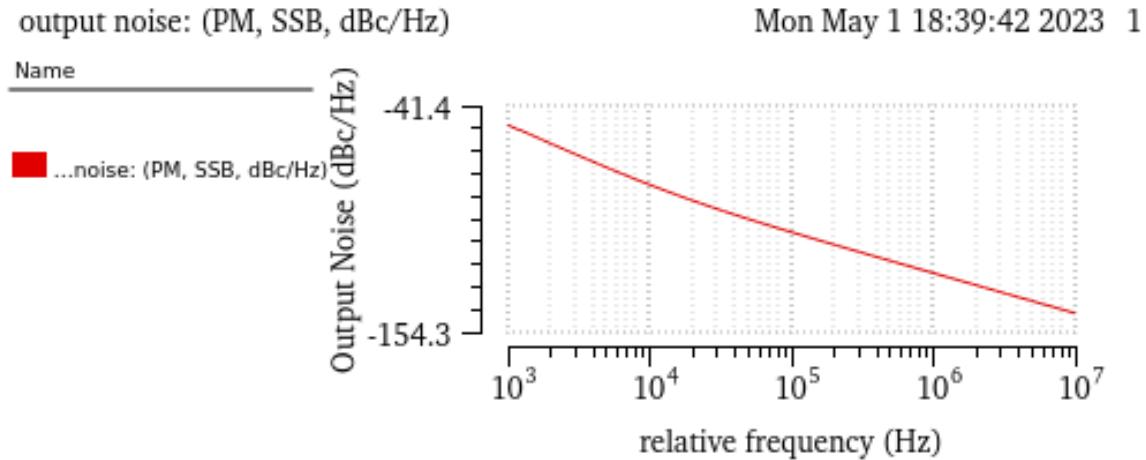


Figure 30: Phase Noise at Offset Frequencies

### Loop Gain Phase:Loop Gain dB20

Mon May 1 18:39:42 2023 3

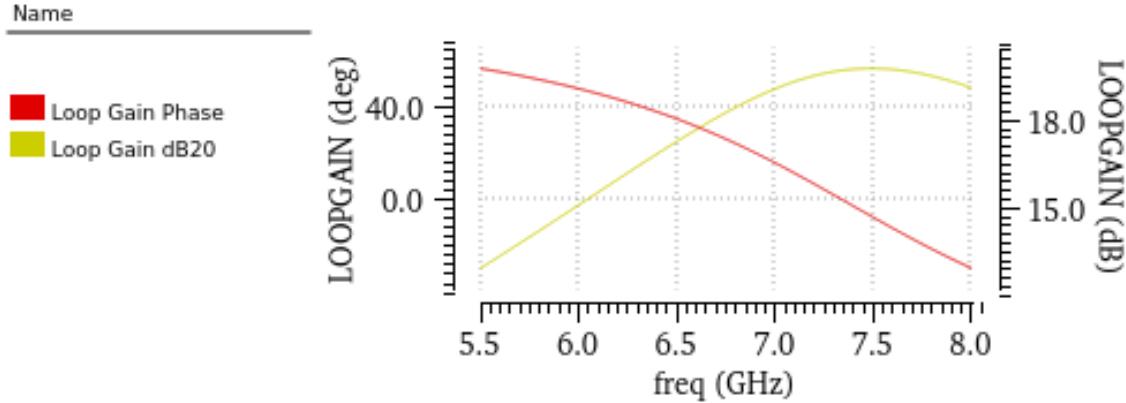


Figure 31: Loop Gain

v /VOUT2; tran (V):v /VOUT1 - vtime('tran "/VOUT2")

Sun May 7 17:59:51 2023 2

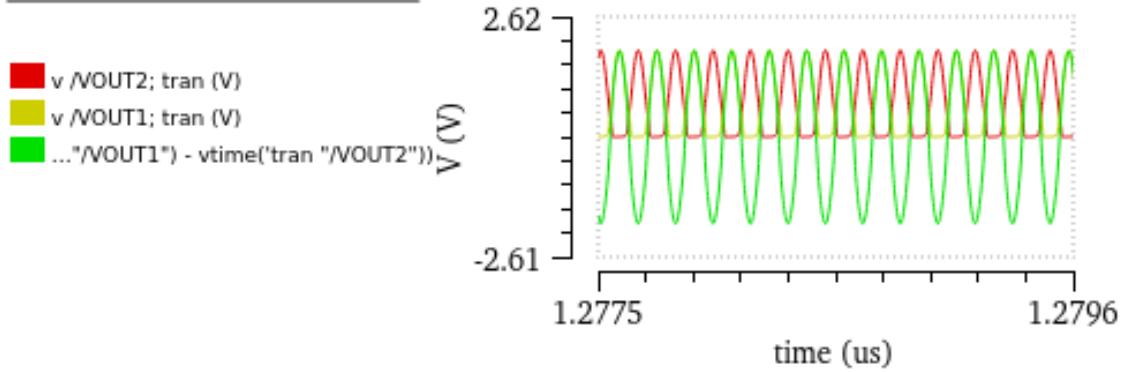


Figure 32: Output Waveform

As seen, a smooth output waveform operating at 5.925 GHz is produced. An essential metric is the Figure of Merit (FoM), which takes into account the phase noise at an offset frequency and power consumption of the oscillator and generates a value to represent the overall performance, given by the following equation:

$$\text{FoM} = -\text{PN} + 20 \log \left( \frac{\text{Operating Freq.}}{\text{Offset Freq.}} \right) - 10 \log (\text{Power Consumption}) \quad (13)$$

Because the phase noise at the offset frequencies is comparable to those in the reference specifications, the FoM value produced shows that this oscillator is well-performing. It should be noted that there is no reference specification for power consumption, as given the older technology there is not a way to have a valid comparison to other studies. However, it can be said that given more time a better LC tank design could be realized, leading to a more efficient oscillator given by LC tank current design in [FA13].

## 5 Overall

High-pass filters (HPF) were incorporated between the components to separate the DC outputs that are linked to the voltage bias pins. Figure 34 illustrates the complete chip along with the interconnections. Capacitors and resistors were carefully chosen to create an HPF that has a cutoff frequency below 40 MHz while not causing any interference to the rest of the circuit. Due to the unavailability of inductors in the SKY130 PDK, off-chip inductors were utilized, and each block was modified to include pins for connecting the off-chip inductors during the testing process.

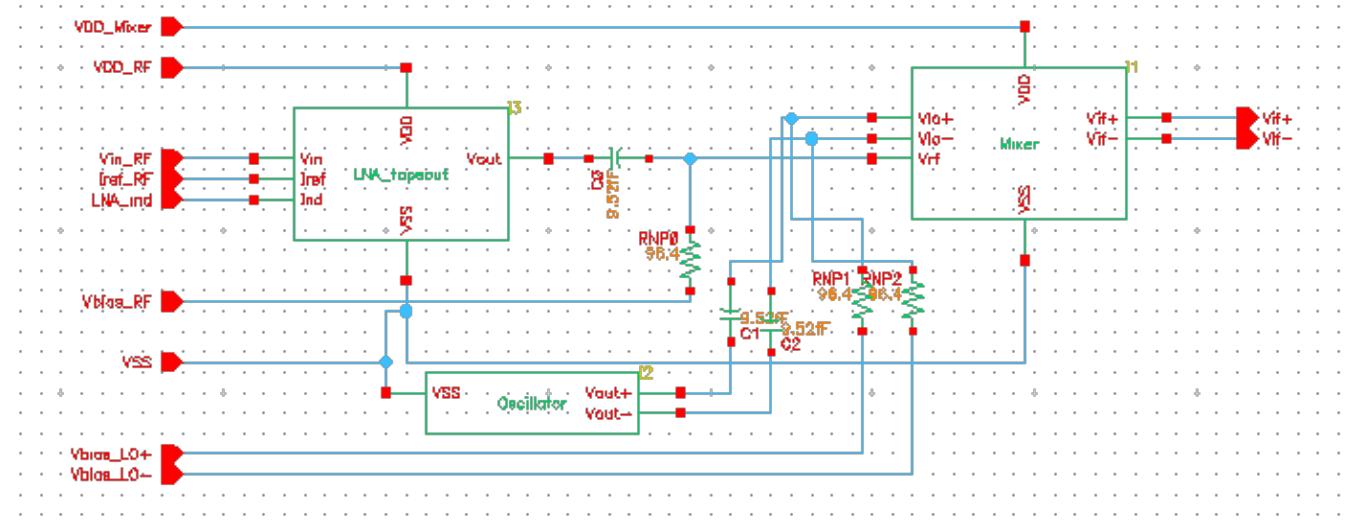


Figure 33: Full Chip Schematic

The test bench illustrated below was employed to evaluate the complete chip. To measure the conversion gain, a testing port connected to a balun which replaced the local oscillator. Additional ports were added at the input of the LNA and the output of the Mixer. Voltage sources were utilized to bias the circuit during the testing process.

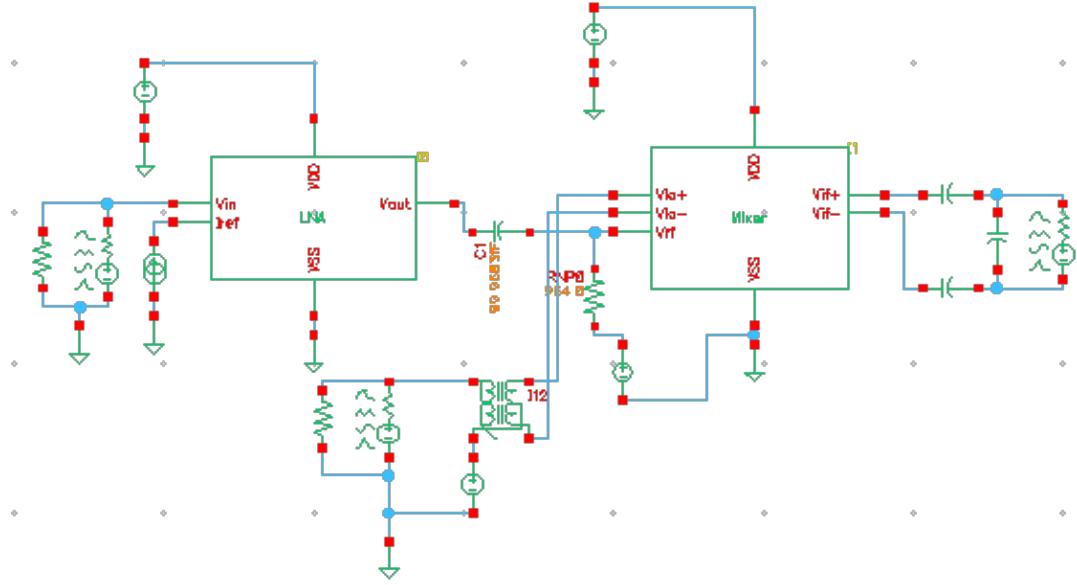


Figure 34: Full Chip Test bench

The conversion gain of the complete chip, swept over LO power, is depicted in Figure 35. The peak conversion gain is 1.121 dB at 10 dB LO power.

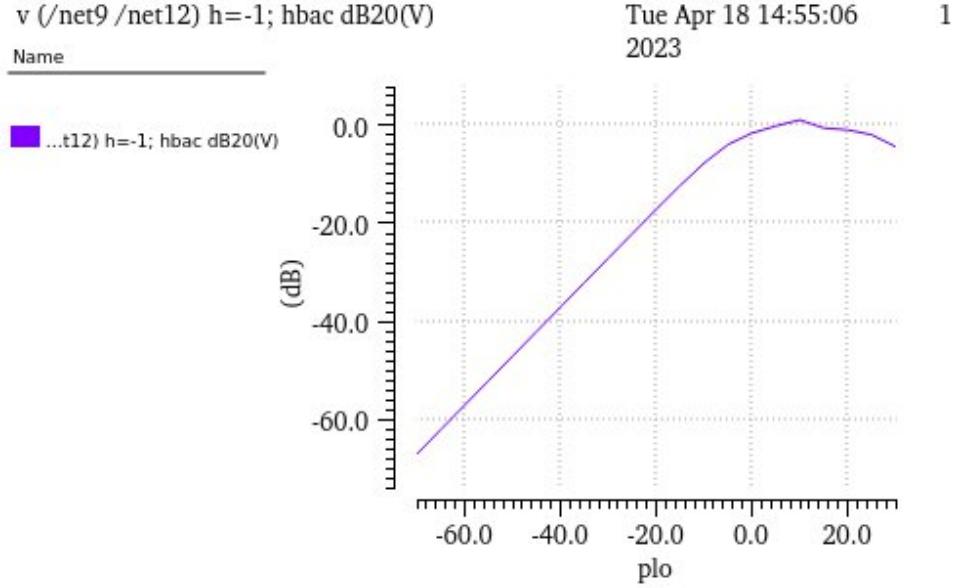


Figure 35: Conversion Gain of the Entire Chip

## 6 Layout

The layout of the complete chip is illustrated in Figure 36, with pins and pads situated on the left and top of the chip, and outputs on the right side. The left section comprises MOSFETs for the LNA, the bottom

section contains MOSFETs for the LO, and the right section comprises MOSFETs for the Mixer. To reduce parasitic resistances and capacitances, wider paths were employed for the current supply, and overlapping paths were minimized. Additionally, the supply voltage and ground pins were designed to cover larger areas to further decrease parasitic resistances.

To pass DRC checks and minimize path length, the components were arranged with appropriate spacing. Guard rings were added to the bottom of each MOSFET, and vias were placed as abundantly as possible to the sources to reduce resistances caused by vias.

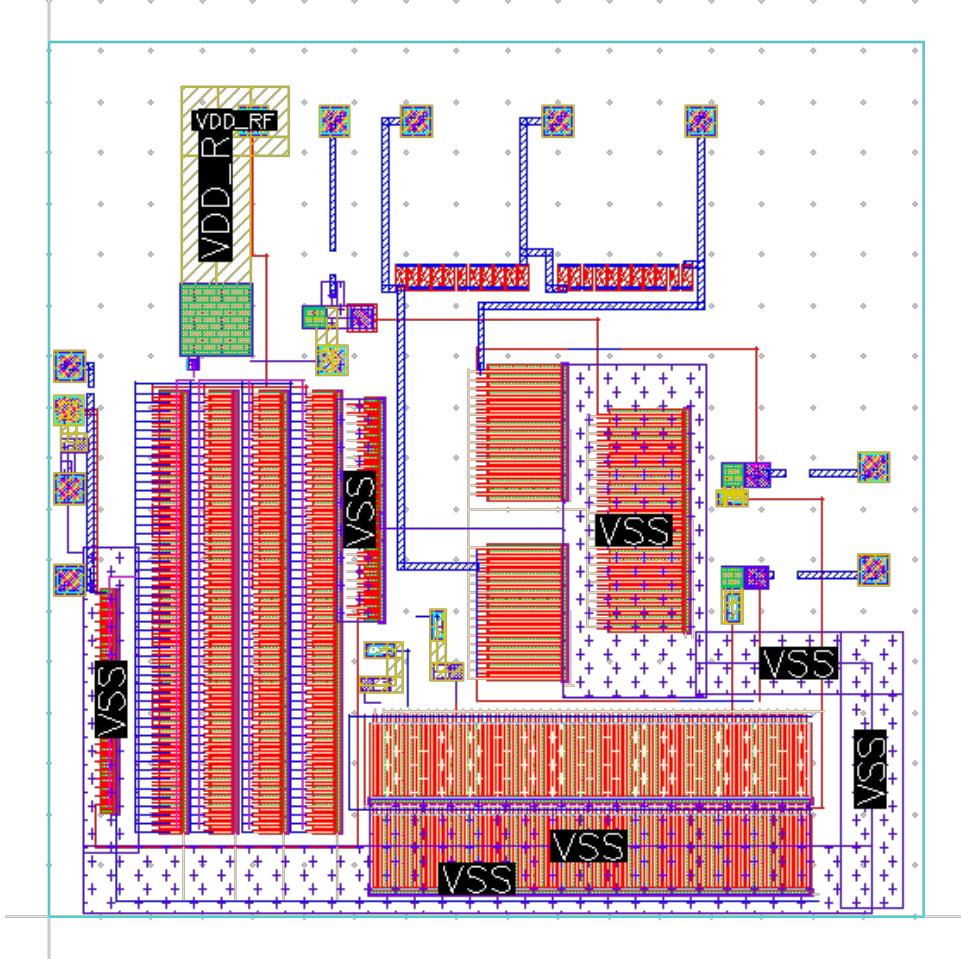


Figure 36: Layout of the Circuit

## 7 Ethics

It is difficult to consider the impact that our project would have considering that it is on such a small scale relative to other existing RF designs, some of which are in use. Thus, we will talk about ethical considerations in general RF design.

First, RF designers must ensure that their designs adhere to applicable regulations and standards, such as spectrum allocation, transmission power limits and electromagnetic interference (EMI). Second, while Wi-Fi operates within regulated power limits, designers should still consider potential health effects. Concerns around this topic should be addressed by designing efficient and well-shielded systems that do not consume more power than necessary. Finally, the environmental impact of RF design must be accommodated for by responsibly sourcing materials, designing for lower power consumption and respectability. Minimizing the carbon footprint and considering end-of-life disposal of devices are important ethical considerations in many

areas of engineering, and RF design is not an exception.

Although we do not focus on materials in this project, one of the parameters we target is power consumption. As seen in the previous sections, the power consumed by the individual stages are less than that of reference designs with similar technology.

## 8 Discussion

The results of the individual components showed improved performance compared to existing standards, achieving the target of improved linearity. However, due to time limitations, the entire chip was not properly tested and did not outperform the standards. Post-layout testing, which would include any parasitic impedances, was also not performed. To verify the chip's performance in real-life, PCBs will be designed to probe individual components and measure the output signal.

For future implementations of this project, it may be beneficial to use a more standard technology such as TSMC65, which provides a richer library of components and testing software. Although it is more expensive to implement, it may be worth the investment in the long run. Moreover, if more time was available, other topologies could be considered to compensate for the areas where the individual blocks were lacking. For instance, a double balanced mixer could be used to improve the output signal, but the LNA block would need to be modified to produce a differential signal. Alternatively, a noise cancelling topology could have been employed to improve the noise figure of the LNA. Also, with the design of the LC tank of the Class-D Oscillator, perhaps a more efficient design could be produced to reduce power consumption and increase FOM further.

Finally, it is important to note that post-layout testing could have been performed to account for parasitic components. However, this was not done due to time constraints. Despite the challenges faced during the design and testing of the integrated circuit, the process has been a valuable learning experience for the individuals involved. Through this project, they gained knowledge and hands-on experience in designing and testing RF circuits, which will prove to be useful in future projects. Chip manufacturing is a lengthy process. More often than not, designs go through several iterations of design, fabrication, and testing. However, since this is a one-time tape-out opportunity, the chip is not necessarily guaranteed to succeed in the first attempt.

## 9 Poster Presentation

### Integrated Circuits Design for 5 GHz Wi-Fi : Radio Frequency Front-End

Franklin Cevallos-Lozano (EE'23), David Yang (EE'23), Sue (Xue Ru) Zhou (EE'23)

ECE395 Senior Design Projects

**Abstract**

The objective of this project is to design and tape-out a working radio frequency (RF) front-end of a 5 GHz Wi-Fi receiver chip with a focus on linearity. Due to the significance of signal integrity, the receiver must be designed to operate at 10 dBm LO power. The receiver is based on the SKY130 180 nm PDK. In collaboration with NYDesign's I.C. program, Efabless, the blocks of the front-end (low-noise amplifier, mixer, oscillator) were simulated individually and as an overall system. While the simulation results for the overall system were not very promising, the individual blocks show comparable results (to existing designs) across parameters such as gain, linearity, noise and power. For next steps, we plan on designing a PCB to test the chips when they arrive.

**Low Noise Amplifier (LNA)**

**Schematic**

**Testbench**

**Specifications:**

- Gain: 17.59 dB
- P1dB: -1.05 dBm
- IP3: -0.14 dBm input/RF power
- Noise Figure: 10.58 dB
- S11: -19.86 dB
- Power: 16.77 mW

**Reference Specs:**

- Gain: 15.68 dB
- P1dB: -2.9 dBm
- IP3: -0.14 dBm input/RF power
- Noise Figure: 2 dB
- S11: -10 dB
- Power: 30 mW

**Layout**

**Introduction**

Wi-Fi 6 (802.11ax) is the latest wireless standard that provides several improvements over its predecessor, including increased speed, capacity, and efficiency. One of the key components of a Wi-Fi 6 network is the 5 GHz Wi-Fi receiver chip, which provides faster and more stable connections than the traditional 2.4 GHz band. The 5 GHz band offers more available channels and less interference, making it ideal for high-density environments such as offices, schools, and public spaces.

Improving the performance of 5 GHz Wi-Fi receiver chips is crucial for realizing the full potential of Wi-Fi 6 networks. Higher performance leads to faster and more reliable connections, increased productivity, and better user experiences.

Our project focuses on the design of the front-end of the receiver chip, which consists of the low-noise amplifier, mixer, and oscillator. There are several parameters that characterize the performance: gain, linearity, noise, and power. By improving these parameters, the receiver will have enhanced sensitivity, better signal-to-noise ratio, reduced interference, less power consumption (longer battery life), and better performance in high-density environments.

**Method**

We are designing an RF RX front-end chip for the 5 GHz band in collaboration with NYDesign's I.C. Program, Efabless. Our design uses SKY130, an open-source I.C. PDK with 130 nm technology. We designed, simulated, and laid out our project in Cadence Virtuoso. We will evaluate the physical chips with RF testing on a PCB.

**Block Diagram\***

\*Theory is from Razavi's book on RF Microelectronics [1]

**Low-Noise Amplifier (LNA):** amplifies the incoming low-signal from the antenna without degrading its signal-to-noise ratio. Typical amplifiers often introduce additional noise, but LNA's are designed to minimize this.

**Mixer:** performs downconversion by multiplying the RF signal and the LO waveform while still maintaining the other characteristics of the signal, such as phase and amplitude.

**Local Oscillator (LO):** generates a frequency that is mixed with the incoming radio signal to convert it to a lower, more easily processed frequency. This allows the receiver to amplify and process the incoming signal more effectively. The local oscillator typically generates a frequency that is close to, but slightly different from, the incoming signal. This difference, or "beat" frequency, is used to process the signal.

**Results**

**Overall**

**Peak Conversion Gain: 1.121 dB at 10 dB LO Power**

**Conversion Gain:** A graph showing conversion gain versus frequency from 400 MHz to 2 GHz.

**Local Oscillator (LO)**

**Schematic**

**Testbench**

**Specifications:**

- Phase Noise @ 1MHz: -51 dBc/Hz
- Phase Noise @ 10MHz: 104.5 dBc/Hz
- Phase Noise @ 100MHz: 125 dBc/Hz
- Phase Noise @ 1GHz: 145.5 dBc/Hz
- Power Consumption: 18.6 mW
- FoM @ 10MHz: 217.8 dB

**Reference Specifications:**

- Phase Noise @ 1MHz: -68.4 dBc/Hz
- Phase Noise @ 10MHz: 104.5 dBc/Hz
- Phase Noise @ 100MHz: 127 dBc/Hz
- Phase Noise @ 1GHz: 146.5 dBc/Hz
- FoM @ 10MHz: 217 dB

**Layout**

**Low Noise Amplifier (LNA)**

**Schematic**

**Testbench**

**Specifications:**

- Gain: 17.59 dB
- P1dB: -1.05 dBm
- IP3: -0.14 dBm input/RF power
- Noise Figure: 10.58 dB
- S11: -19.86 dB
- Power: 16.77 mW

**Reference Specs:**

- Gain: 15.68 dB
- P1dB: -2.9 dBm
- IP3: -0.14 dBm input/RF power
- Noise Figure: 2 dB
- S11: -10 dB
- Power: 30 mW

**Layout**

**Discussion**

LNA: Compared to the reference specifications, this LNA design exhibited enhanced linearity, power consumption, and input reflection, but at the expense of increased noise figure and reduced gain and S11 parameter. Notably, the design yielded a higher P1dB and IP3, indicating an improvement in linearity while also consuming less power. However, this was achieved at the cost of degraded noise performance.

Mixer: Compared to the specifications taken from a paper on a double balanced mixer using 180 nm technology, our conversion gain of 5.82 dB is less than 12 dB. However, the other specifications, such as the IP3, noise figure and power consumption are better. Our mixer is more linear, despite having the disadvantage of being single-balanced instead of double-balanced.

LO: Compared to the specifications taken from a 65nm paper for a Colpitts Oscillator, the phase noise performance does not meet the specifications; however, when comparing the Class D VCO for phase noise at 10 MHz, we are close to the specification. The FoM here is also satisfactory, despite the disadvantage with such a large Power Consumption.

Overall: The overall design has been thoroughly evaluated for performance. Only the system's conversion gain was simulated. The overall conversion gain was measured to be 1.121 dB at 10 dB LO power. To improve this further, we could improve the gain of individual stages, or impedance match the stages better.

Next Steps: Our next steps is to design a PCB for testing. The board will have SMA connectors for connecting the RF LO, IF signals to external test equipment, as well as connections for other off-chip capacitive and inductive components. The board will also include ports to connect to off-chip DC voltages for biasing and power.

Note: That the simulated results are pre-layout. In addition, the simulated results may not reflect experimental results due to the negligence of parasitic capacitances and resistances.

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Collaborators: efabless NYDesign  
Writing Center: Janice Ma, Karen Holmgren

Figure 37: Final Poster for Senior Projects Showcase

## 10 Timeline

This is the final timeline of our project, including what may happen in the future\*.

September	• Introduction to the components of the RF Receiver
October	• Learn more theory through Professor Koo's seminars
November	• Research individual blocks and give presentations to one another
December	• Attempted to create design on the virtual environment provided by eFabless • Midterm project showcase
January	• Winter break
	• PDK is installed onto the school server
February	• Start designing individual blocks on Cadence
March	• Finish individual block designs and simulations
April	• Putting the blocks together • Layout • Tapeout deadline: 4/24
May	• Final senior project showcase
June*	• Design PCB for testing
July*	• Receive chips and conduct tests

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