CSEE W4823x

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**HW5 Designing a Slave Controller for the Philips I2C Bus Protocol**

We assign code as following,



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MSB LSB

{ SDA\_in, SCL\_in, Byte\_done, addr\_match/bit\_send }

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MSB LSB

{ SDA\_out, SDA\_enable, data\_out, addr\_out }

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(i) The symbolic state diagram of the Moore FSM is attached to this file.

The way we implement this FSM as we firstly draw the state signal diagram out separately using master to slave and slave to master protocols.

It could be easily find out the state of none matched device. So we are not include it in diagram.

We attach these diagram alone with this file.

When slave receive bits from master, we send out the address and data in the low clock cycle to make sure it is stable to local comparator and data device. The reason why we do this, is because there will be a state that could give a new number to comparator just before stop signal.

And our design could handle unexpected exit when master send stop signal to slave when sending data.