

## 20 路可编程 LED 呼吸灯驱动芯片

### 特性

- 20 路 LED，每路最大 24.5mA，8 级电流选择
- 内置智能灯效处理器，程序空间 256 条指令
- 用户可编程实现自定义灯效
- 9 bits PWM 分辨率，256 级线性/对数调光
- 支持 I<sup>2</sup>C 兼容接口，接口电压范围 1.8V ~ 2.8V
- 单电源供电，电压范围 3.0V ~ 4.5V
- QFN4mmx4mm\_28L 封装

### 应用

移动电话  
便携式多媒体播放设备  
家电

### 典型应用图

### 概要

AW9120 内置专用可编程灯效处理器，最大可驱动 20 路 LED。LED 驱动采用共阳极恒流源驱动和 PWM 调光方式，专用的灯效控制处理器 ASP 支持高效的灯效控制和等待、分支、跳转指令，一次可加载 256 条指令，编程灵活，可轻松实现复杂的灯效。

AW9120 支持 400kHz I<sup>2</sup>C 兼容接口，采用 QFN4mmx4mm\_28L 封装，工作电压范围是 3.0V~4.5V。

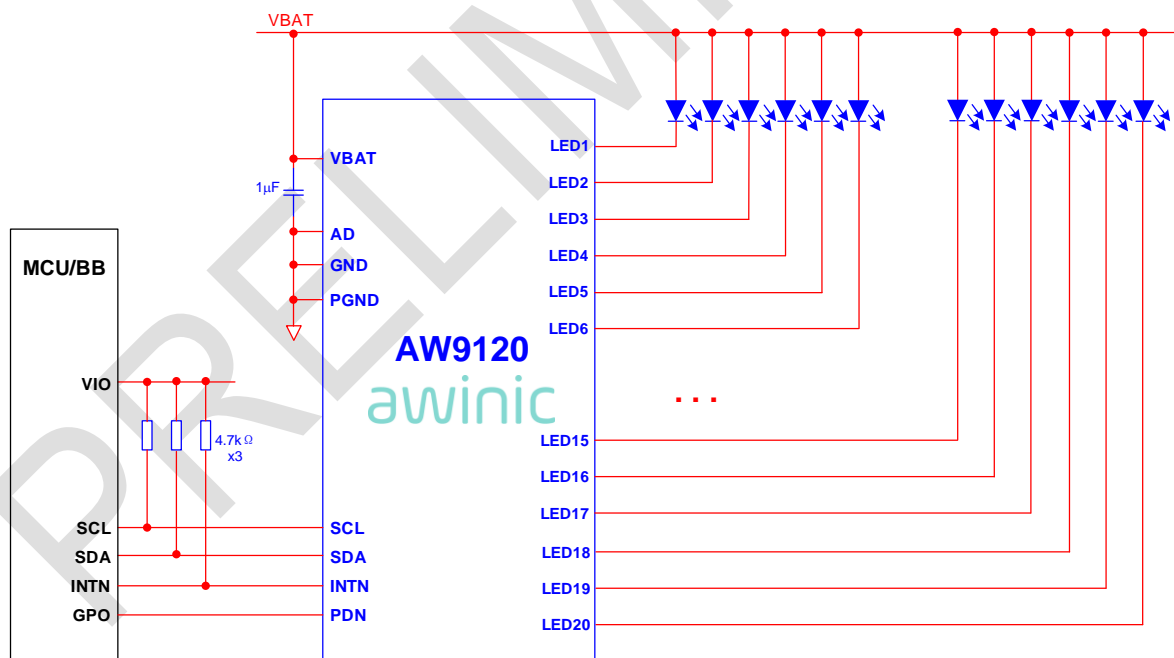


图1 AW9120 典型应用图

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## 20 Programmable LED Driver

### FEATURES

- 8-level LED Maximum Current for each LED, max 24.5mA
- Internal ASP with 256\*16bit SRAM
- Programmable to Achieve Custom Light Effect
- 256-level Linear/Logarithmic PWM Dimming, 12 bits PWM resolution
- Compatible I<sup>2</sup>C Interface, V<sub>IO</sub>: 1.8V ~ 2.8V
- Single Power Supply, Voltage Range: 3.0V ~ 4.5V
- 4mm×4mm QFN28L Package

### GENERAL DESCRIPTION

AW9120 integrates a SRAM program-controlled 20 LED driver. 20 LED driver uses common anode current source and PWM dimming. Each LED is 8-level driver current selectable with dimming independently controlled by external MCU or internal 256word\*16bit SRAM program.

Compatible I<sup>2</sup>C interface of 400kHz fast mode is provided, the package is 4mm×4mm QFN28L. It requires only 3.0V-4.5V single power supply.

### APPLICATIONS

Mobile Phones, MID  
Portable Media Player  
Home Appliances

### TYPICAL APPLICATION CIRCUIT

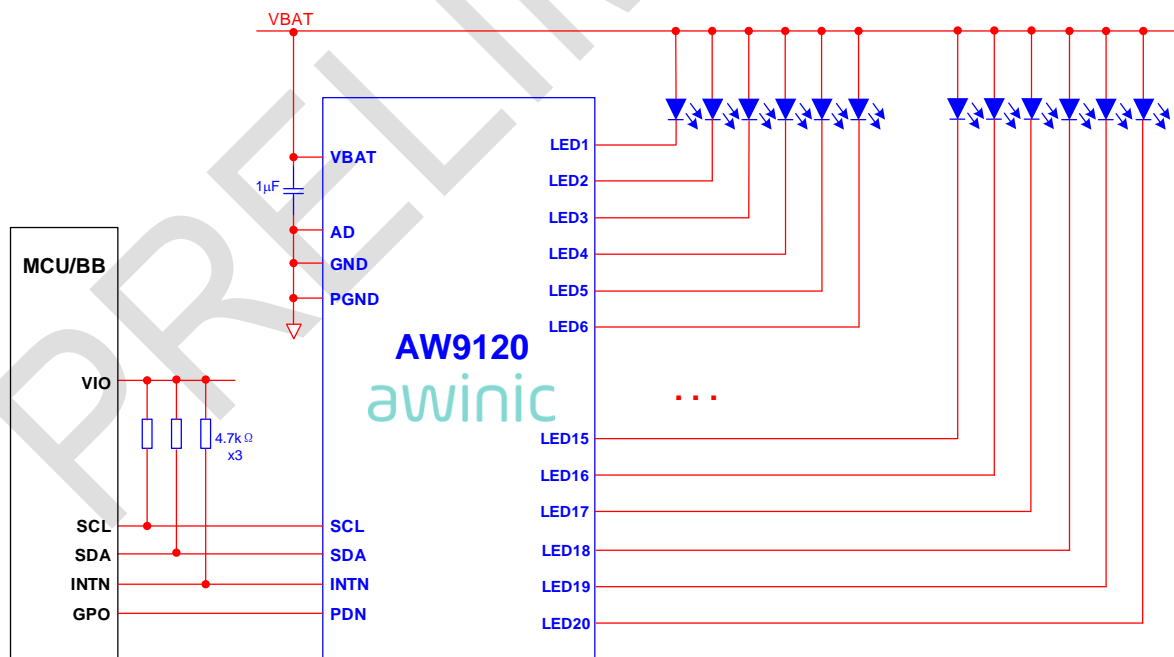


Figure 1 AW9120 Typical Application Circuit

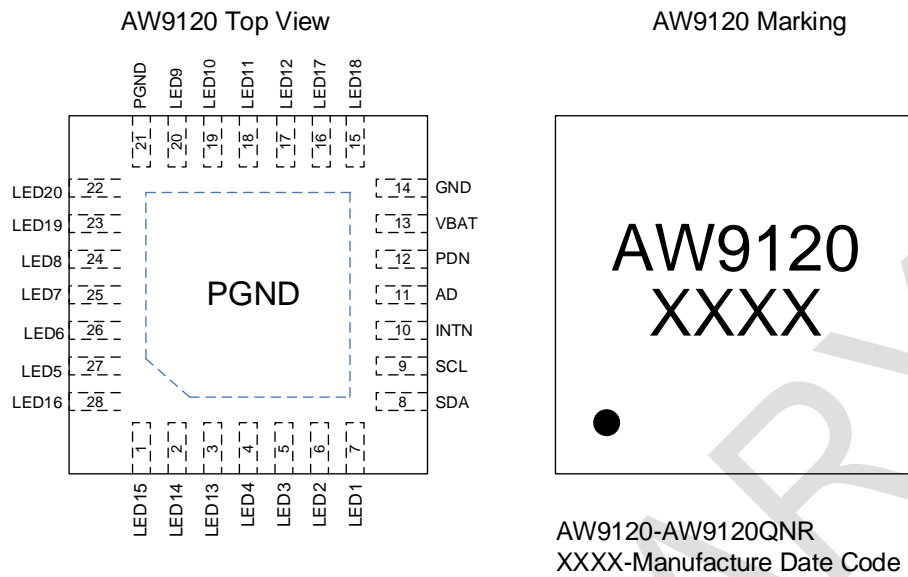
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## 1 PIN CONFIGURATION AND TOP MARK



## 2 PIN DEFINITION

No.	NAME	DESCRIPTION
1	LED15	LED15 cathode driver, anode connected to VBAT
2	LED14	LED14 cathode driver, anode connected to VBAT
3	LED13	LED13 cathode driver, anode connected to VBAT
4	LED4	LED4 cathode driver, anode connected to VBAT
5	LED3	LED3 cathode driver, anode connected to VBAT
6	LED2	LED2 cathode driver, anode connected to VBAT
7	LED1	LED1 cathode driver, anode connected to VBAT
8	SDA	Data I/O of I <sup>2</sup> C Interface
9	SCL	Clock input of I <sup>2</sup> C Interface
10	INTN	Open-drain Interrupt output, low active. Typically connected to VIO via a 4.7kΩ resistor.
11	AD	I <sup>2</sup> C Address Select, internal pull-down resistor
12	PDN	Power-down input, low active, internal 1MΩ pull-down resistor
13	VBAT	Power supply (3.0V to 4.5V)
14	GND	Ground
15	LED18	LED18 cathode driver, anode connected to VBAT
16	LED17	LED17 cathode driver, anode connected to VBAT
17	LED12	LED12 cathode driver, anode connected to VBAT
18	LED11	LED11 cathode driver, anode connected to VBAT
19	LED10	LED10 cathode driver, anode connected to VBAT
20	LED9	LED9 cathode driver, anode connected to VBAT

21	PGND	Ground
22	LED20	LED20 cathode driver, anode connected to VBAT
23	LED19	LED19 cathode driver, anode connected to VBAT
24	LED8	LED8 cathode driver, anode connected to VBAT
25	LED7	LED7 cathode driver, anode connected to VBAT
26	LED6	LED6 cathode driver, anode connected to VBAT
27	LED5	LED5 cathode driver, anode connected to VBAT
28	LED16	LED16 cathode driver, anode connected to VBAT

PRELIMINARY

### 3 FUNCTIONAL BLOCK DIAGRAM

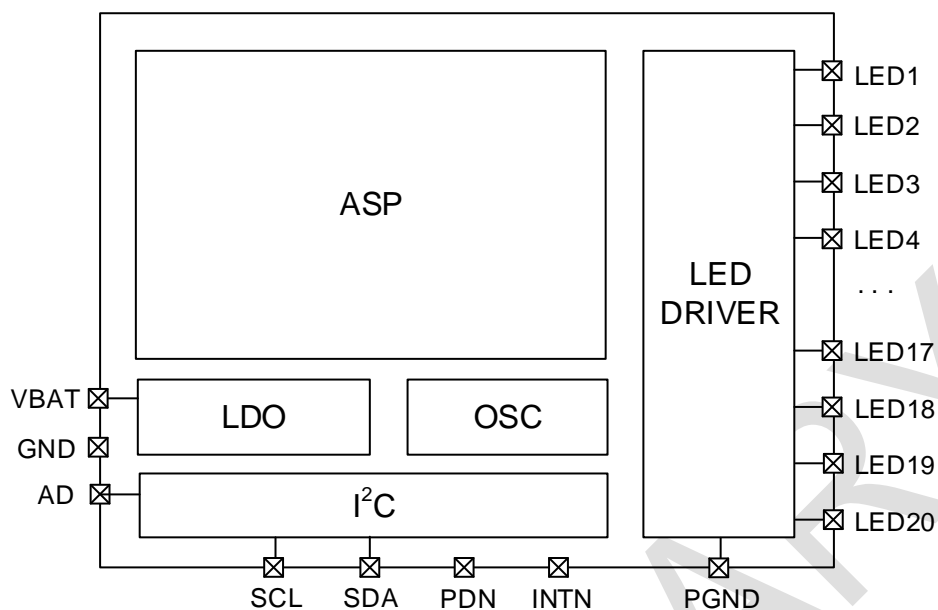


Figure 2 FUNCTIONAL BLOCK DIAGRAM

### 4 TYPICAL APPLICATION CIRCUITS

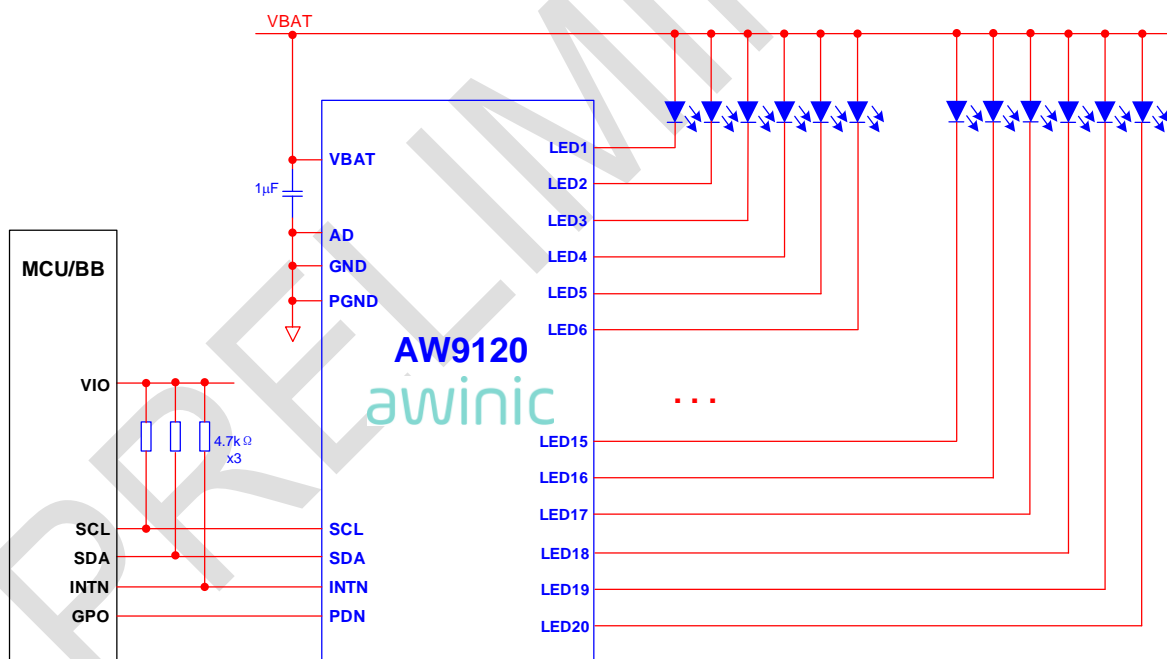
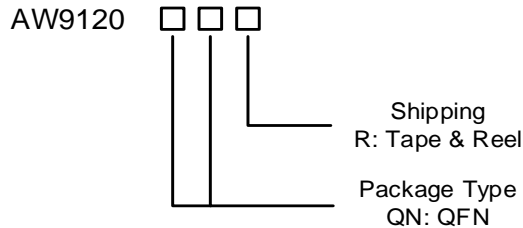


Figure 3 AW9120 Typical Application Circuit

## 5 ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Delivery Form
AW9120QNR	-40°C~85°C	4mm×4mm×0.75mm QFN4mm×4mm-28L	AW9120	6000 unit/ Tape and Reel



## 6 ABSOLUTE MAXIMUM RATINGS<sup>(NOTE 3)</sup>

PARAMETERS		RANGE
Supply voltage range VBAT		-0.3V to 5V
Input voltage range	SCL, SDA	-0.3V to 3.6V
	PDN, LED1~LED20	-0.3V to 4.5V
Output voltage range	SDA, INTN	-0.3V to 3.6V
Junction-to-ambient thermal resistance $\theta_{JA}$		45°C/W
Operating free-air temperature range		-40°C to 85°C
Maximum Junction temperature $T_{JMAX}$		150°C
Storage temperature $T_{STG}$		-55°C to 125°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD <sup>(NOTE 4)</sup>		
HBM (human body model)		±4000V
MM (machine mode)		±300V
CDM (charge device mode)		±2000V
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		+IT: 450mA
		-IT: -450mA

NOTE3: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7



## 7 ELECTRICAL CHARACTERISTICS

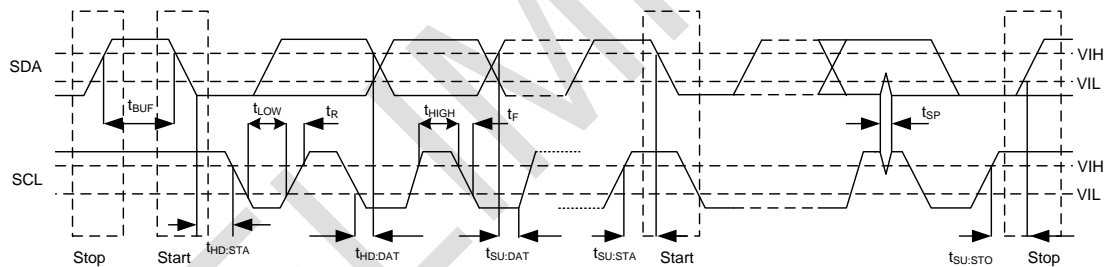
$V_{BAT}=3.8V$ ,  $T_A=25^{\circ}C$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{BAT}$	Power supply	-	3.0		4.5	V
$I_{SHUTDOWN}$	Current in Shutdown mode	PDN=GND		8	15	$\mu A$
$I_{STANDBY}$	Current in Standby mode	PDN= $V_{IO}$		130	160	$\mu A$
$I_{ACTIVE}$	Current in Active mode	PDN= $V_{IO}$ , GCR=0x01		0.55	0.8	mA
$F_{OSC}$	Internal oscillator Frequency accuracy (16MHz)		14.8	16	17.2	MHz
<b>Digital Logical Interface</b>						
$V_{IL}$	Logic input high level	SDA,SCL,PDN	-0.3		0.45	V
$V_{IH}$	Logic input low level	SDA,SCL,PDN	0.9			V
$I_{IL}$	Low level input current	SDA,SCL,PDN		5		nA
$I_{IH}$	High level input current	SDA,SCL,PDN		5		nA
$V_{OL}$	Logic output low level	SDA, INTN $I_{OUT}=3mA$			0.4	V
$I_{OL}$	Maximum output current	SDA, INTN			10	mA
$I_L$	Output leakage current	SDA,INTN open drain			1	$\mu A$
<b>I<sup>2</sup>C Interface</b>						
$F_{SCL}$	I <sup>2</sup> C-BUS clock frequency				400	kHz
$T_{Deglitch}$	SCL deglitch time			200		ns
	SDA deglitch time			250		ns
<b>LED Driver</b>						
$I_{ACC}$	Current accuracy	$I_{LED}=24.5mA$		24.5		mA
$I_{MATCH}$	Matching accuracy	$I_{LED}=24.5mA$			10	%
$V_{SAT}$	Current saturation voltage	$I_{LED}=24.5mA$			300	mV
$F_{PWM}$	PWM frequency	LCR.FREQ=1	110	122	135	Hz
		LCR.FREQ =0	220	244	270	Hz

NOTE5: the value is tested in default configuration.

## 8 I<sup>2</sup>C INTERFACE TIMING

Parameter Name		MIN	TYP	MAX	UNIT
F <sub>SCL</sub>	Interface Clock frequency			400	kHz
T <sub>DEGLITCH</sub>	Deglitch time	SCL	200		ns
		SDA	250		ns
T <sub>HD:STA</sub>	(Repeat-start) Start condition hold time	0.6			μs
T <sub>LOW</sub>	Low level width of SCL	1.3			μs
T <sub>HIGH</sub>	High level width of SCL	0.6			μs
T <sub>SU:STA</sub>	(Repeat-start) Start condition setup time	0.6			μs
T <sub>HD:DAT</sub>	Data hold time	0			μs
T <sub>SU:DAT</sub>	Data setup time	0.1			μs
T <sub>R</sub>	Rising time of SDA and SCL			0.3	μs
T <sub>F</sub>	Falling time of SDA and SCL			0.3	μs
T <sub>SU:STO</sub>	Stop condition setup time	0.6			μs
T <sub>BUF</sub>	Time between start and stop condition	1.3			μs



## 9 FUNCTIONAL DESCRIPTION

### 9.1 WORK MODE

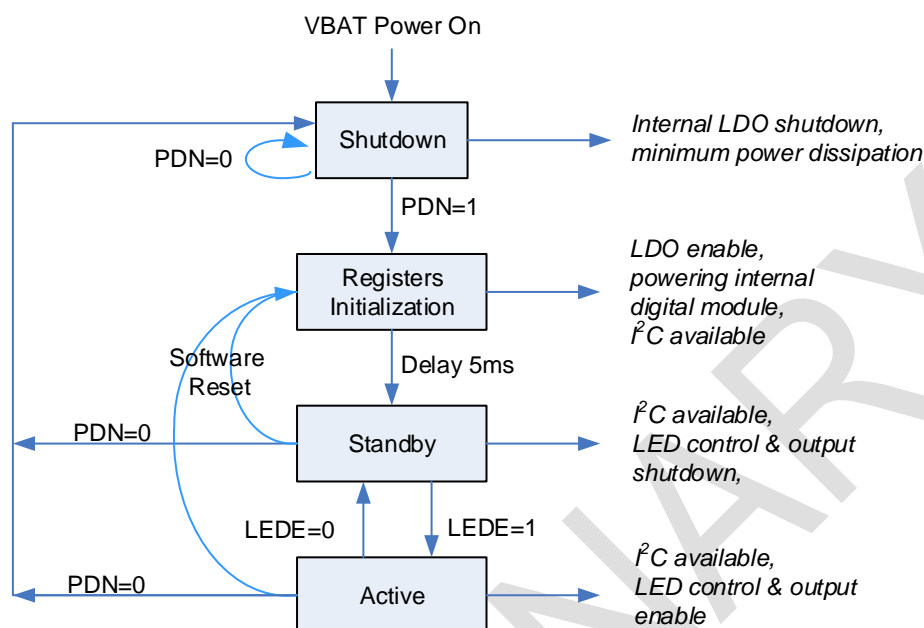


Figure 4 AW9120 Work Mode

After VBAT powered on, if PDN pin is low, the AW9120 is in shut-down mode, the current consumption is less than 15 $\mu$ A. When PDN pin becomes high, the internal LDO is activated, and a power-on reset (POR) signal is generated to initialize all internal registers, the device enters standby mode, this is a low power consumption mode, when all circuit functions are disabled. In standby mode, I<sup>2</sup>C interface is active, all internal configuration register can be written. If control bit GCR.LEDE is written high, the device enters the active mode.

### 9.2 RESET

#### 9.2.1 Hardware Reset

When PDN pin changes from low to high, the power-up reset (POR) signal is generated, all internal registers are reset.

#### 9.2.2 Software Reset

Writing 0x55AA to register RSTR via I<sup>2</sup>C interface will activate a software reset to reset all internal registers.

### 9.3 I<sup>2</sup>C INTERFACE

AW9120 supports the I<sup>2</sup>C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I<sup>2</sup>C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10k $\Omega$  and the typical value is 4.7k $\Omega$ . AW9120 can support different high level (1.8V~3.3V) of this I<sup>2</sup>C interface.

#### 9.3.1 Device Address

The I<sup>2</sup>C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW9120 is 0x2C/0x2D.

把RW当做第8位地址：0X58 59

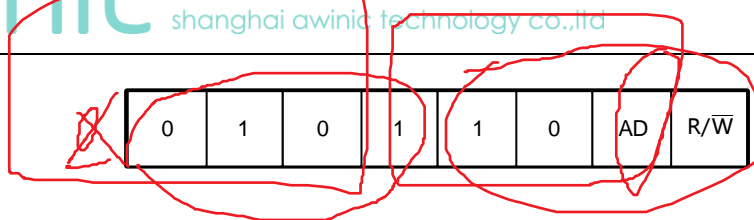


Figure 5 Device Address Configuration

### 9.3.2 Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

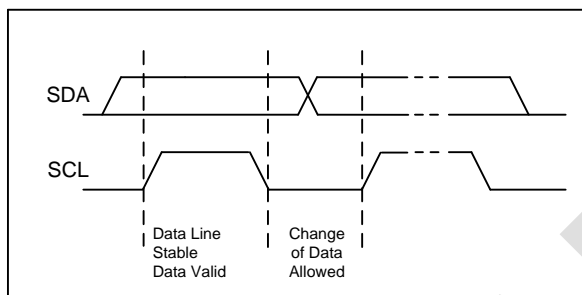


Figure 6 Data Validation Diagram

### 9.3.3 ACK(Acknowledgement)

ACK means the successful transfer of I2C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, AW9120 sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I<sup>2</sup>C stop is not send by master, AW9120 sends the next data. If ACK is not send by master, AW9120 stops to send data and waits for I<sup>2</sup>C stop.

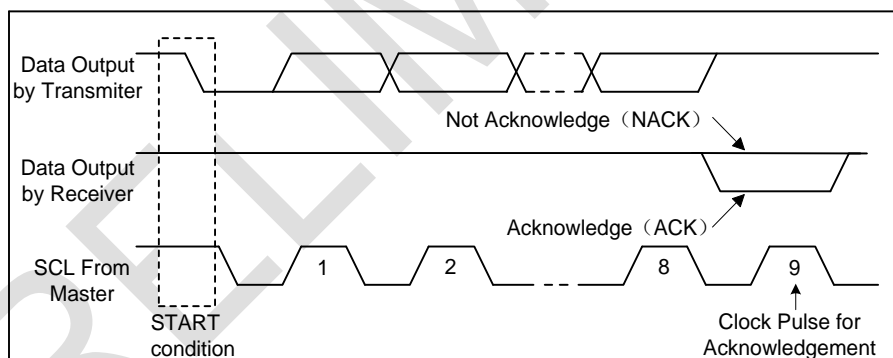


Figure 7 I<sup>2</sup>C ACK Timing

### 9.3.4 I<sup>2</sup>C Start/Stop

I2C start: SDA changes form high level to low level when SCL is high level.

I2C stop: SDA changes form low level to high level when SCL is high level.

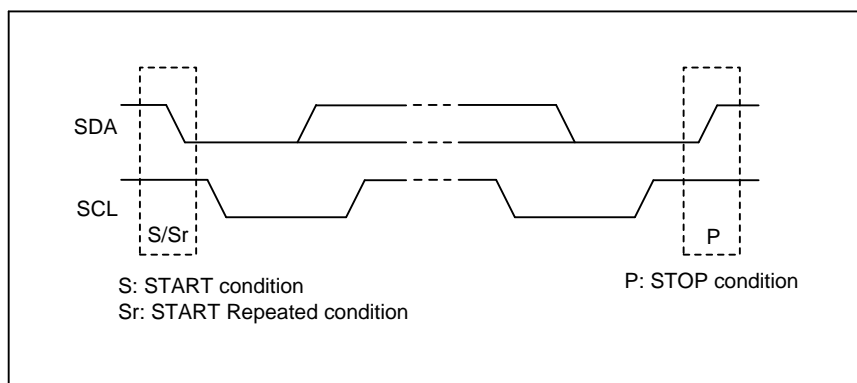


Figure 8 I²C Start/Stop Condition Timing

### 9.3.5 Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

- Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
- Master device sends slave address (7-bit) and the data direction bit ( $w = 0$ ).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8-bit)
- Slave sends acknowledge signal
- Master sends data high 8Bit to be written to the addressed register
- Slave sends acknowledge signal
- Master sends data low 8Bit to be written to the addressed register
- Slave sends acknowledge signal
- Master generates STOP condition to indicate write cycle end

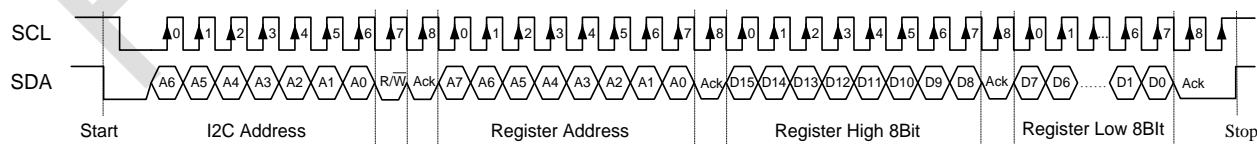


Figure 9 AW9120 I²C Write Timing

### 9.3.6 Read Cycle

In a read cycle, the following steps should be followed:

- Master device generates START condition

- b) Master device sends slave address (7-bit) and the data direction bit ( $w = 0$ ).
- c) Slave device sends acknowledge signal if the slave address is correct.
- d) Master sends control register address (8-bit)
- e) Slave sends acknowledge signal
- f) Master generates STOP condition followed with START condition or REPEAT START condition
- g) Master device sends slave address (7-bit) and the data direction bit ( $r = 1$ ).
- h) Slave device sends acknowledge signal if the slave address is correct.
- i) Slave sends data high 8Bit from addressed register.
- j) Master sends acknowledge signal
- k) Slave sends data low 8Bit from addressed register.
- l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.
- m) If the master device generates STOP condition, the read cycle is ended.

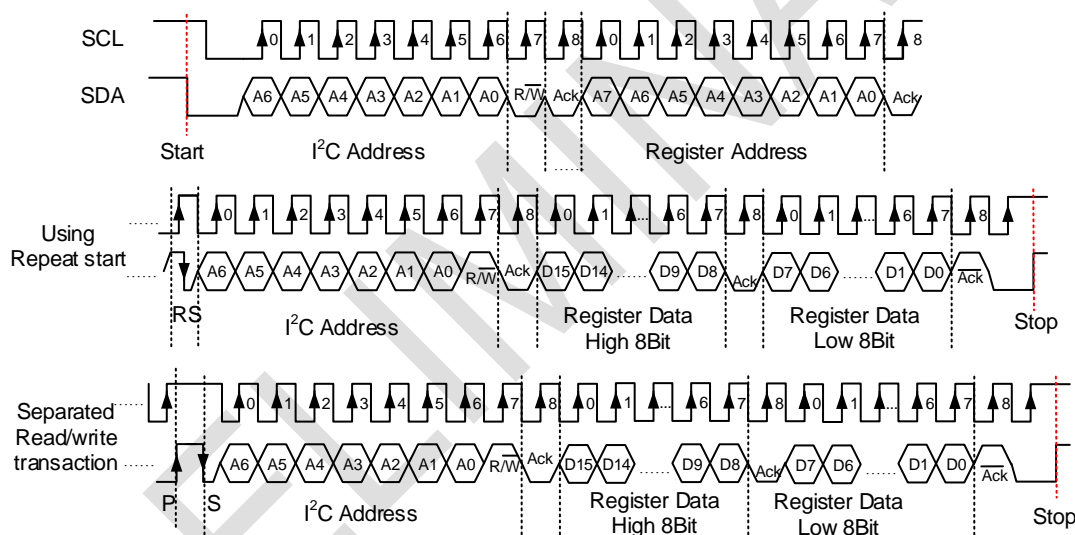


Figure 10 AW9120 I<sup>2</sup>C Read Timing

## 9.4 OSCILLATOR

An internal oscillator provides clock for both capacitive touch detecting and LED controlling circuit. If register bit GCR.LEDE is high, the OSC starts to work, the start-up time is about 5 us. When the register bit GCR.LEDE are low, the internal OSC stops.

## 9.5 LED DRIVER

LED driver provide 20 current sources to drive LEDs, a dedicated Application-Specific-Processor (ASP) is designed to produce versatile lighting effect for mobile devices.

If the control bit GCR.LEDE is 0, LED driver circuit is in reset state, all 20 LED outputs are disabled. If control bit GCR.LEDE is 1, the LED driver circuit is enabled, the control bit LER.LENx ( $x=1$  to 20) configure the corresponding LED channel is active or not.

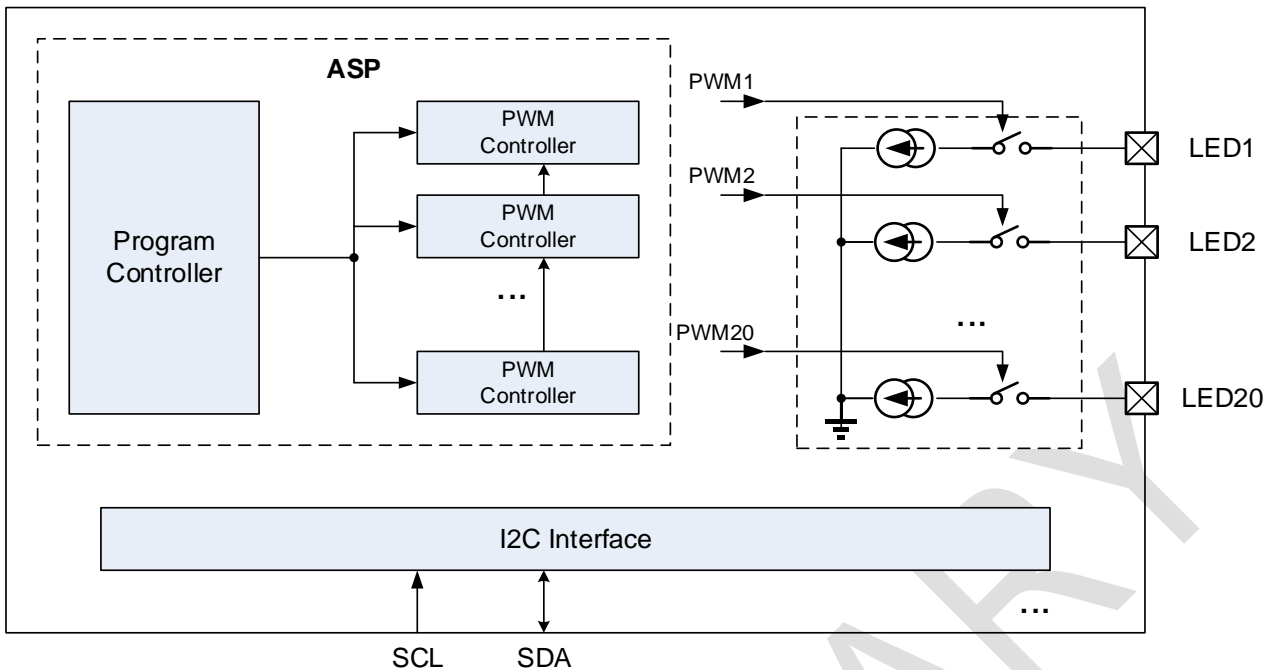


Figure 11 AW9120 LED Dimming Control Module Diagram

### 9.5.1 LED brightness controller

Pulse Width Modulation (PWM) is used to adjust the brightness of LED, 256 level brightness with 9bit resolution is adapted. The PWM frequency can be configured between 122Hz or 245Hz by control bit LCR.FREQ.

The ASP generates the PWM signal with dedicated and highly efficient dimming control instruction for all 9 independent LED constant current source. By programming, user-defined complicated lighting effect could be produced.

The LED control instruction executed by ASP could come from LED SRAM or external I<sup>2</sup>C register. The register CTRS can choose every LED channel to be controlled by SRAM program or by I<sup>2</sup>C register.

- CTRS[n] = 0, LED n controller is controlled by the internal SRAM instruction;
- CTRS[n] = 1, LED n controller is controlled by the external I<sup>2</sup>C register.

### 9.5.2 LED Constant current driver

For each LED, the maximum output constant current is 24.5mA, with 8 level adjustable by register IMAXn (n=1~20).

### 9.5.3 ASP

ASP module is consist of one program controller and 20 PWM controllers.

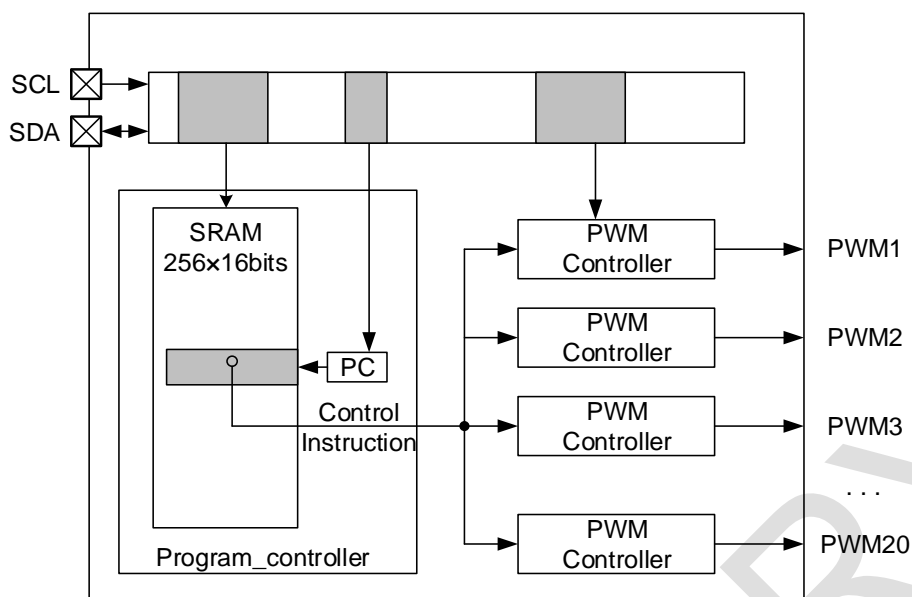


Figure 12 ASP Structure Diagram

### 9.6.3.1 Program Controller

The program controller is clocked by 32kHz internal clock, each instruction is executed in one clock cycle. The program controller is consist of a program SRAM, an algorithmic logic unit ( ALU) and other internal registers. The 256x16bit internal SRAM is used to store LED lighting effect program loaded through I<sup>2</sup>C interface, the I<sup>2</sup>C interface also can start or stop the program execution. There are 4 internal registers RA/RB/RC/RD participating ALU operation so as to generate complicated program control such as repeating and looping. Except for that, there are 8 8bit temporary data registers(R1~R8) and 5 special function registers. Their internal address and function description is shown in the table below.

Table 1 Address allocation of internal data register in ASP

Register	Address(HEX)	Description
R1	00	R1 data temporary register, 8bit, I <sup>2</sup> C readable
R2	01	R2 data temporary register, 8bit, I <sup>2</sup> C readable
R3	02	R3 data temporary register, 8bit, I <sup>2</sup> C readable
R4	03	R4 data temporary register, 8bit, I <sup>2</sup> C readable
R5	04	R5 data temporary register, 8bit, I <sup>2</sup> C readable
R6	05	R6 data temporary register, 8bit, I <sup>2</sup> C readable
R7	06	R7 data temporary register, 8bit, I <sup>2</sup> C readable
R8	07	R8 data temporary register, 8bit, I <sup>2</sup> C reading
GMSK1	0d	Global control mask register(M8~M1)
GMSK2	0e	Global control mask register(M12~M9)
GMSK3	0f	Global control mask register(M20~M13)

Table 2 Special function registers definition

Register	B7	B6	B5	B4	B3	B2	B1	B0	Description
GMSK1	M8	M7	M6	M5	M4	M3	M2	M1	Mask control for global control instruction. When Mn=1, LEDn will not be affected by global
GMSK2					M12	M11	M10	M9	



GMSK3	M20	M19	M18	M17	M16	M15	M16	M13	control instruction.
-------	-----	-----	-----	-----	-----	-----	-----	-----	----------------------

### 9.6.3.2 PWM Controller

The PWM controller is execution unit of LED control instruction. There are 9 PWM controllers receiving the LED effect instruction from SRAM, and generate 8bit PWM code, which will be convert to 9bit duty cycle control code by logarithmic transformation. If LCR.LOGLN=00, the transformation is natural logarithm(  $\log_e$  ). If LCR.LOGLN=01, the transformation is logarithm of 10 (  $\log_{10}$  ), otherwise the 8b-to-9b transformation of PWM code is linear.

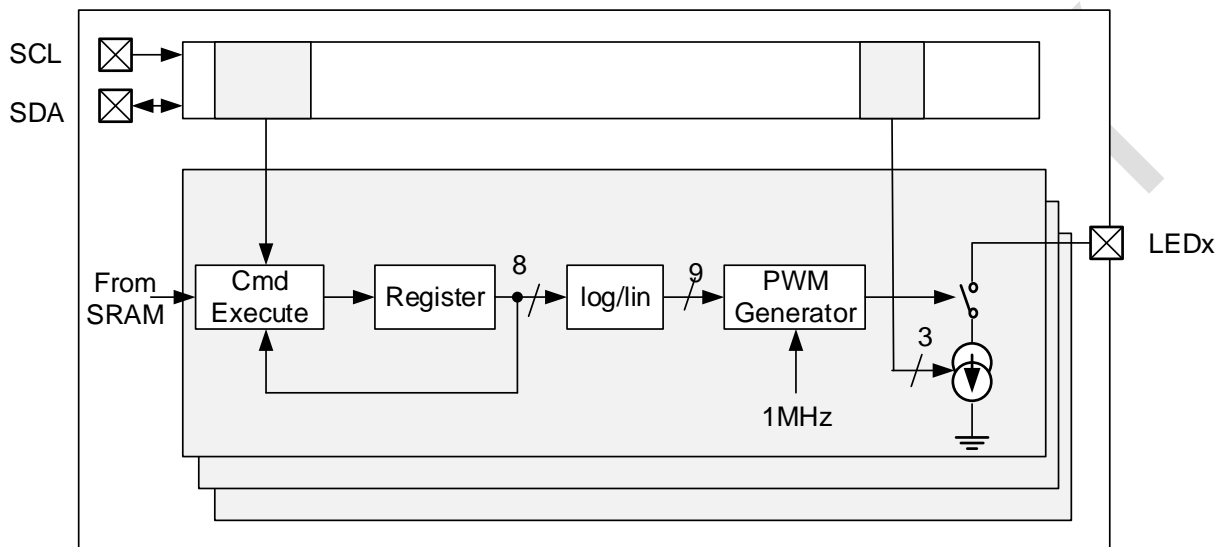


Figure 13 PWM Controller Schematic Diagram

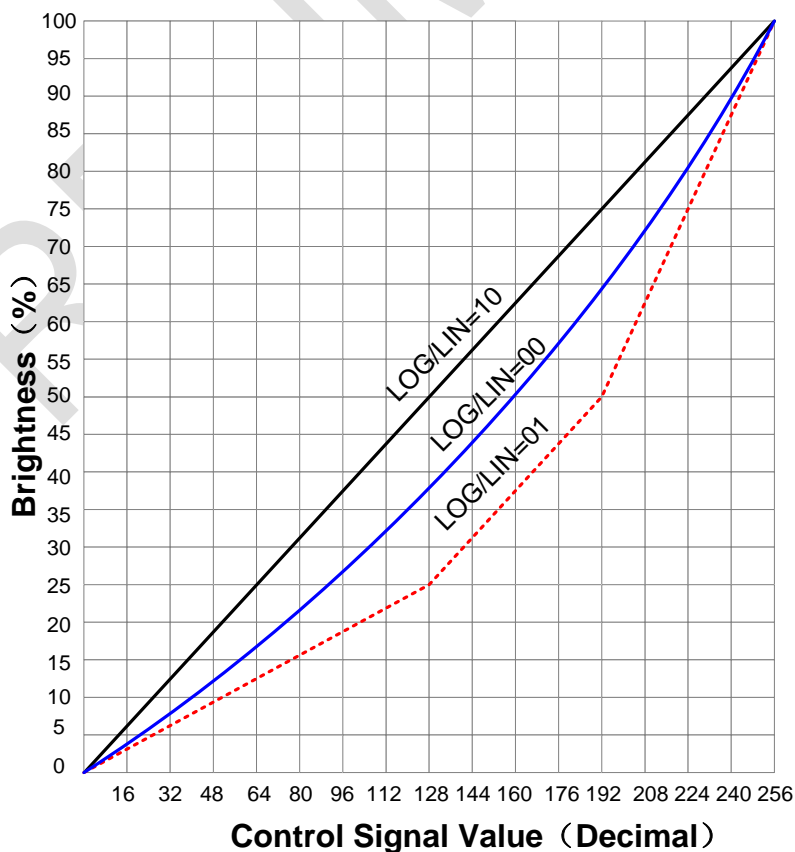


Figure 14 8b-to-9 PWM code transformation curve

### 9.6.3.3 Program Loading and execution

#### a) Program loading

It is recommended to load SRAM program only when control bit PMD.PROGMD is 00. In this state, the internal program can be read/write through I<sup>2</sup>C interface. When loading program, please write the SRAM loading address in register WADDR(0x7E) at first, and then write the 16bit LED effect instruction to register WDATA(0x7F). Continuously loading program is supported, after a 16b instruction is written through register WDATA, the value of WADDR will automatically plus by 1.

#### b) Program execution

Register bit PMD.PROGMD[1:0] controls the loading and execution mode of SRAM program.

When register bit IPMD.PROGMD[1:0]=00, program execution is shut down, SRAM program and program pointer(PC) are permitted to be loaded.

When IPMD.PROGMD[1:0] is written to be 01 from another value, current program will stop, and PC will be reload by register SADDR, and then executes the SRAM program starting from the address of PC

When Register bit PMD.PROGMD[1:0] =10, the SRAM program will be executed by the mode defined by register bit RMD.RUNMD[1:0]

Table 3 Program running mode control register

RMD.RUNMD	Function Description
0 0	Hold mode. program stop and PC hold after one instruction is finished.
0 1	Single step mode, only used for debugging. Once writing 01 to RUNMD, only one instruction will be executed with PC+1, and then RMD.RUNMD is cleared (return to hold mode)
1 0	Continuously running mode, program starts from the address of PC.
1 1	Repeating mode, only used for debugging. Once writing 11 to RUNMD, current instruction will be executed without PC+1, and then RMD.RUNMD is cleared (return to hold mode)

### 9.6.3.4 SRAM program Instruction

There are 27 commands in ASP instruction set, including LED control command, data operation and transfer command, wait and branch control command. The Rx,Ry and Rz in instruction list means the internal register RA, RB, RC and RD, each of them can participate the ALU operation as source or destination register.

Table 4 LED Effect Instruction

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JP	0	0	0	0	0	0	0	0	ADDR[7:0]							
NOP	0	0	0	0	0	0	0	1	-	-	-	-	-	-	-	-
-----	0	0	0	0	0	0	1	X								
JPZ Addr	0	0	0	0	0	1	0	0	ADDR[7:0]							
JPNZ Addr	0	0	0	0	0	1	0	1	ADDR[7:0]							
JPS Addr	0	0	0	0	0	1	1	0	ADDR[7:0]							
JPNS Addr	0	0	0	0	0	1	1	1	ADDR[7:0]							

LD Rz Im	0	0	0	0	1	0	Rz	Im[7:0]							
CMPI Rz Im	0	0	0	0	1	1	Rz	Im[7:0]							
ANDR Rz Im	0	0	0	1	0	0	Rz	Im[7:0]							
ORR Rz Im	0	0	0	1	0	1	Rz	Im[7:0]							
RDR Rz Addr	0	0	0	1	1	0	Rz	ADDR[7:0]							
WDR Rz Addr	0	0	0	1	1	1	Rz	ADDR[7:0]							
ADDI Rz Im	0	0	1	0	0	0	Rz	Im[7:0]							
AUBI Rz Im	0	0	1	0	0	1	Rz	Im[7:0]							
ADDR Rx Ry	0	0	1	0	1	0	Rz	-	-	-	-	Rx	Ry		
SUBR Rx Ry	0	0	1	0	1	1	Rz	-	-	-	-	Rx	Ry		
CMPR Rx Ry	0	0	1	1	0	0	0	0	-	-	-	-	Rx	Ry	
----	0	0	1	1	0	0	X	X							
END Int Rst	0	0	1	1	0	1	0	0	-	-	-	-	-	Int	Rst
INTN_MASKOFF	0	0	1	1	0	1	1	0	-	-	-	-	-	-	-
INTN_MASKON	0	0	1	1	0	1	1	1	-	-	-	-	-	-	-
WAITI Pre Time	0	0	1	1	1	Pre	T[9:0]								
SETPWMR Rx Ry	0	1	0	0	0	0	0	-	-	0	0	0	Rx	Ry	
RAMPR Dir Rx Ry	0	1	0	0	0	0	1	Dir	-	0	0	0	Rx	Ry	
SETSTEPTMRR Pre Rx Ry	0	1	0	0	0	1	0	-	Pre	0	0	0	Rx	Ry	
SETSTEPTMRI Pre Ch Im	1	0	0	Ch[4:0]				Pre	-	Im[5:0]					
SETPWMI Ch Im	1	0	1	Ch[4:0]				Im[7:0]							
RAMPI Dir Ch Im	1	1	Dir	Ch[4:0]				Im[7:0]							

a) Special LED Control Command

There are 3 types of LED control command.

- **SETPWM:** set the brightness level (0~255)for specified LED channel;
- **RAMP:** set the specified LED channel fade in or fade out for expected step( 0~255)
- **SETSTEP:** set the fading slope for specified LED channel;

All control parameter in above commands can either come from specified register (RA~RD), or from immediate data contained in command..

All LED control command supports broadcast mode, one instruction may send to multiple or all LEDs

When SRAM program running, if Ch field or value of Rx in LED control command is '11111', the current command is active for all LED with setting of CTRSR.bitn=0. If Ch field or value of Rx in LED control command is '11110', the current command is only active for those channel with setting of GMSKx=0.

When LED instruction is come from I<sup>2</sup>C interface directly, it is recommended to use only the command with immediate data. If the Ch field in command is "11111", the current command is only active for those LED with STRSR.bitn=1..

Table 5 LED Control Instruction explanation

Instruction	Description
-------------	-------------

Register Parameter	
<b>SETPWMR</b> Rx Ry	<b>Set the PWM brightness level with parameter in register</b> Rx: LED channel number, 0~19 for LED 1~ LED 20 respectively Ry: Brightness level, 0~255
<b>RAMPR</b> Dir Rx Ry	<b>Set the Fade-in/Fade-out for specified step with parameter in register</b> Dir: 1: Fade-in; 0: Fade-out Rx: LED channel number, 0~19 for LED 1~ LED 20 respectively Ry: the step number of Fade-in/Fade-out
<b>SETSTEPTMRR</b> Pre Rx Ry	<b>Set the RAMP slope with parameter in register</b> Pre: basic time unit, 0: 0.5ms; 1: 16ms Rx: LED channel number, 0~19 for LED 1~ LED 20 respectively Ry: RAMP step time = (Ry+1)*Pre, 0~255
Immediate Data	
<b>SETPWMI</b> Ch Im	<b>Set the PWM brightness level with immediate parameter</b> Ch: LED channel number, 0~19 for LED 1~ LED 20 respectively Im: Brightness level, 0~255
<b>RAMPI</b> Dir Ch Im	<b>Set the Fade-in/Fade-out for specified steps with immediate parameter</b> Dir: 1: Fade-in; 0: Fade-out Ch: LED channel number, 0~19 for LED 1~ LED 20 respectively Im: the steps of Fade-in/Fade-out
<b>SETSTEPTMRI</b> Pre Ch Im	<b>Set the RAMP step time with immediate parameter</b> Pre: basic unit of time, 0: 0.5ms; 1: 16ms Ch: LED channel number, 0~19 for LED 1~ LED 20 respectively Im: RAMP step time = (Im +1)*Pre, 0~255

Table 6 Program Control and operation Instruction

Instruction	Encoding	Description
<b>branch Instruction</b>		
<b>JP</b> Addr	0x00xx	Immediate Jump, jump to PC = Addr
<b>JPZ</b> Addr	0x04xx	Conditional Jump, If Rz is 0, jump to PC = Addr
<b>JPNZ</b> Addr	0x05xx	Conditional Jump, If Rz is not 0, jump to PC = Addr
<b>JPS</b> Addr	0x06xx	Conditional Jump, If Rz < 0, jump to PC = Addr
<b>JPNS</b> Addr	0x07xx	Conditional Jump, If Rz >= 0, jump to PC = Addr
<b>Data Transfer Instruction</b>		
<b>LD</b> Rz Im	0x08xx - 0x0bxx	Rz = Im
<b>RDR</b> Rz Addr	0x18xx - 0x1bxx	Rz = *Addr
<b>WDR</b> Rz Addr	0x1cxx - 0x1fxx	*Addr = Rz
<b>Computation Instruction</b>		
<b>CMPI</b> Rz Im	0x0cxx - 0x0fxx	Rz – Im, only change S/Z flag
<b>CMPR</b> Rx Ry	0x30xx	Rx – Ry, only change S/Z flag
<b>ANDR</b> Rz Im	0x10xx - 0x13xx	Rz = Rz & Im, affect S/Z flag
<b>ORR</b> Rz Im	0x14xx - 0x17xx	Rz = Rz   Im, affect S/Z flag
<b>ADDI</b> Rz Im	0x20xx - 0x23xx	Rz = Rz + Im, affect S/Z flag
<b>SUBI</b> Rz Im	0x24xx - 0x27xx	Rz = Rz - Im, affect S/Z flag
<b>ADDR</b> Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rz + Ry, affect S/Z flag
<b>SUBR</b> Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rz - Ry, affect S/Z flag
<b>Control Instruction</b>		
<b>END</b> Int Rst	0x34xx	Program end with optionally reset register RMD and generate interrupt

		Int= 0: no interrupt after instruction executed; Int= 1: generate interrupt after instruction executed Rst=0: PC add 1 after instruction executed; Rst=1: Reload PC with SADDR after instruction executed
INTN_MASKOFF	0x36xx	Unmask internal interrupt
INTN_MASKON	0x37xx	Mask internal interrupt
WAITI Pre Time	0x38xx - 0x3fxx	Wait for specified time Pre: time of basic waiting cycle, 0: 0.5ms; 1: 16ms Time: number of waiting cycle, max value is 1023, wait time=Pre*Time

### 9.6.3.5 Example

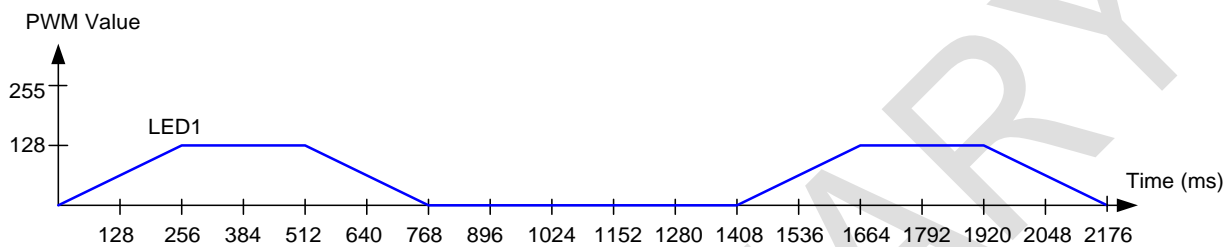


Figure 15 LED Effect Programming Diagram

Table 7 Reference Instruction of LED Effect Programming

PC	Assemble Instruction	Machine Code	explanation
0	SETSTEPTMRI 0x00 0x1F 0x03	0x9F03	RAMPI step time: 2ms
1	SETPWMI 0x1F 0x00	0xBF00	ALL LED turn off
	START:		Address Label "START" (02H)
2	RAMPI 0x01 0x00 0x80	0xE080	LED1 fade in, 128 steps breath
3	WAITI 0x01 0x20	0x3C20	Wait 512ms
4	RAMPI 0x00 0x00 0x80	0xC080	LED1 fade out, 128 steps breath
5	WAITI 0x01 0x38	0x3C38	Wait 896ms
6	JP START	0x0002	Jump to START, PC=2

Step1: Power On, configure register

- VBAT power on, 4.2V
- Pull PDN to 3V
- Wait 5ms
- GCR = 0x0001 // enable LED module
- LER = 0x0001 // enable LED1
- PMD.PROGRMD = 00 //hold mode
- RMD.RUNMD = 00 //hold mode

Step2: Load Instruction to SRAM

- WADDR = 0x0000 // load program starting at address =0x0000
- WDATA = 0x9F03
- WDATA = 0xBF00
- WDATA = 0xE080
- WDATA = 0x3C20
- WDATA = 0xC080

- WDATA = 0x3C38
- WDATA = 0x0002

Step3: Run

- SADDR = 0x0000
- RMD.RUNMD = 10 // execution mode change to run mode,
- PMD.PROGMD = 01 // start program from 0x0000

PRELIMINARY

## 10 REGISTER DESCRIPTION

### 10.1 REGISTER CONFIGURATION

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IDRST	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	GCR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEDE
0x02~0x4F	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
0x50	LER1	0	0	0	0	LE12	LE11	LE10	LE9	LE8	LE7	LE6	LE5	LE4	LE3	LE2	LE1
0x51	LER2	0	0	0	0	0	0	0	0	LE20	LE19	LE18	LE17	LE16	LE15	LE14	LE13
0x52	LCR	0	0	0	0	0	0	0	SRMINI	LIRMD		-		LIE	FREQ	LOG/LIN	
0x53	PROGMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	
0x54	RUNMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMOD	
0x55	CTRS1	0	0	0	0	CS12	CS11	CS10	CS9	CS8	CS7	CS6	CS5	CS4	CS3	CS2	CS1
0x56	CTRS2	0	0	0	0	0	0	0	0	CS20	CS19	CS18	CS17	CS16	CS15	CS14	CS13
0x57	IMAX1	0	IMAX4			0	IMAX3			0	IMAX2			0	IMAX1		
0x58	IMAX2	0	IMAX8			0	IMAX7			0	IMAX6			0	IMAX5		
0x59	IMAX3	0	IMAX12			0	IMAX11			0	IMAX10			0	IMAX9		
0x5A	IMAX4	0	IMAX16			0	IMAX15			0	IMAX14			0	IMAX13		
0x5B	IMAX5	0	IMAX20			0	IMAX19			0	IMAX18			0	IMAX17		
0x5C~0x5D	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x5E	ISR2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS
0x5F	SADDR	0	0	0	0	0	0	0	0	SADDR							
0x60	PCR	0	0	0	0	0	0	0	0	PC							
0x61	CMDR	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x62	RA	0	0	0	0	0	0	0	0	RA							
0x63	RB	0	0	0	0	0	0	0	0	RB							
0x64	RC	0	0	0	0	0	0	0	0	RC							
0x65	RD	0	0	0	0	0	0	0	0	RD							
0x66 ~ 0x6D	R1 ~ R8	0								R1 ~ R8							
6E	GRPR	0	0	0	0	0	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	D1	D0
7D	WP	WPW								0	0	0	0	0	0	0	
7E	WADDR	0	0	0	0	0	0	0	0	ADDR							
7F	WDATA	CODE															



## 10.2 GLOBAL REGISTER DESCRIPTION

### 10.2.1 IDRST, Chip ID and Software Reset

Address: 0x00, R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit	Symbol		Description												
15:0	IDRST		Chip ID: 0xB223 Software Reset: write 0x55AA to IDRST, reset the whole device.												

### 10.2.2 GCR, Global Control Register

Address: 0x01, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEDE
Bit	Symbol		Description												
0	LEDE		LED driver function 0: disable LED driver (default) 1: enable LED driver												

## 10.3 LED Effect Control Register

### 10.3.1 LER1, LED Driver Enable Register

Address: 0x50, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	LE12	LE11	LE10	LE9	LE8	LE7	LE6	LE5	LE4	LE3	LE2	LE1
Bit	Symbol		Description												
11:0	LEx		LED output enable 0: disable 1: enable												
15:12	-		Reserved, must be 0												

### 10.3.2 LER2, LED Driver Enable Register

Address: 0x51, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	LE20	LE19	LE18	LE17	LE16	LE15	LE14	LE13
Bit	Symbol		Description												
7:0	LEx		LED output enable 0: disable 1: enable												
15:8	-		Reserved, must be 0												

### 10.3.3 LCR, LED Effect Configuration Register

Address: 0x52, R/W, default: 0x0080															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SRMINI	LIRMD	-	-	-	LIE	FREQ	LOGLIN	
Bit	Symbol		Description												
1:0	Log/Lin		Log/Linear dimming mode selection 00: log dimming 1, log(e) (default) 01: log dimming 2, log10 1x: linear dimming												
2	FREQ		PWM frequency selection 0: 245Hz (default) 1: 122Hz												
3	LIE		LED program end interrupt enable 0: disable interrupt (default) 1: enable interrupt												
5:4	-		-												

7:6	LIRMD	LED effect code run mode after responding to interrupt request 00: hold mode, PC point can be changed, program hold and wait for RMD.RUNMD 01: step mode 10: run mode (default)
8	SRMINI	SRAM reset bit, write 1, reset SRAM; read SRAM status, default is 0.

### 10.3.4 PMD, Program Mode Register

Address: 0x53, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD
Bit	Symbol		Description												
1:0	PROGMD		Program control mode 00: load program via I <sup>2</sup> C interface (default) 01: re-load program and execute. When write 01 to PROGMD[1:0], set PC pointer will be updated with SADDR, then start to run program, and finally PROGMD[1:0] is changed to 10 automatically 10: run program. Under this mode, the control bit RUNMD in register RMD can configure different program running mode for normal operation or debug. 11: undefined												

### 10.3.5 RMD, Program Run Mode Register

Address: 0x54, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMD
Bit	Symbol		Description												
1:0	RUNMD		SRAM program run mode, only active for these LED set with CTRSR.CSx=0 00: hold mode, program stop and hold PC pointer (default) 01: step mode, RUNMD reset, PC+1 after the current program executed 10: run mode, normal program run 11: repeat mode, RUNMD reset, PC hold after the current program executed												

### 10.3.6 CTRSR1, LED Control Source Selection Register

Address: 0x55, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	CS12	CS11	CS10	CS9	CS8	CS7	CS6	CS5	CS4	CS3	CS2	CS1
Bit	Symbol		Description												
11:0	CSx		LED control source 0: LEDx controlled by SRAM program 1: LEDx controlled by external MCU via I <sup>2</sup> C interface												

### 10.3.7 CTRSR2, LED Control Source Selection Register

Address: 0x56, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	CS20	CS19	CS18	CS17	CS16	CS15	CS14	CS13
Bit	Symbol		Description												
7:0	CSx		LED control source 0: LEDx controlled by SRAM program 1: LEDx controlled by external MCU via I <sup>2</sup> C interface												

### 10.3.8 IMAX1~IMAX20, LEDx Maximum Output Current Register

Address: 0x57~0x5B, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IMAX4				0	IMAX3				0	IMAX2				IMAX1
0	IMAX8				0	IMAX7				0	IMAX6				IMAX5
0	IMAX12				0	IMAX11				0	IMAX10				IMAX9
0	IMAX16				0	IMAX15				0	IMAX14				IMAX13
0	IMAX20				0	IMAX19				0	IMAX18				IMAX17

Bit	Symbol	Description
14:12 10:8 6:4 2:0	IMAXx	LEDx maximum output current selection 000: 0mA (default) 001: 3.5mA 010: 7.0mA 011: 10.5mA 100: 14.0mA 101: 17.5mA 110: 21.0mA 111: 24.5mA

### 10.3.9 LISR, LED Interrupt Status Register

Address: 0x5E, R(clear by reading), default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS
Bit	Symbol		Description												
1	LIS		LED program end interrupt status, set by END instruction with parameter int=1, used for inform external MCU that program has finished. LCR.LIE is the enable bit for LIS. 0: no interrupt 1: interrupt request												

### 10.3.10 SADDR, Program Start Address Register

Address: 0x5F, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								SADDR
Bit	Symbol		Description												
7:0	SADDR		SRAM program starting address. For reload and run mode, if setting PMD.PROGMD=10, program will jump to PC=SADDR and run again.												

### 10.3.11 PCR, LED Program Control Pointer Register

Address: 0x60, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PC							
Bit	Symbol		Description												
7:0	PC		SRAM program pointer(PC), can be written by I <sup>2</sup> C interface. For normal program execution, set the PC pointer at PMD.PROGMD= 00 mode at first, and then write PMD.PROGMD with 10.												

### 10.3.12 CMDR, LED Command Register

Address: 0x61, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD															
Bit	Symbol		Description												
15:0	CMD		External controlled Command. used to send external LED command which is only active for those LED configured with control bit CTRSR.CSx=1. The external controlled command adapted the same instruction with internal ASP.												

### 10.3.13 RA/RB/RC/RD, LED Internal Program Register

Address: 0x62~0x65, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	RA							
0	0	0	0	0	0	0	0	RB							
0	0	0	0	0	0	0	0	RC							
0	0	0	0	0	0	0	0	RD							
Bit	Symbol		Description												
7:0	RA/RB/RC/RD		LED internal program register, read only, for debug usage.												

#### 10.3.14 R1~R8, LED Internal Data Register

Address: 0x66~0x6D, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								R1
0	0	0	0	0	0	0	0								R2
0	0	0	0	0	0	0	0								R3
0	0	0	0	0	0	0	0								R4
0	0	0	0	0	0	0	0								R5
0	0	0	0	0	0	0	0								R6
0	0	0	0	0	0	0	0								R7
0	0	0	0	0	0	0	0								R8
Bit	Symbol		Description												
7:0	R1~R8		LED internal data register, for debug usage.												

#### 10.3.15 GRP, LED Group Operation Register

Address: 0x6E, R, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1		
Bit	Symbol		Description												
10:2	GS[8:0]		LED channel selection for external group control command. GS[n]=0, LED <sub>n</sub> is not included in external LED command with chan=0x1E; GS[n]=1, LED <sub>n</sub> is included in external LED command with chan=0x1E;												

#### 10.3.16 WADDR, LED Program Loading Address Register

Address: 0x7E, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								ADDR
Bit	Symbol		Description												
7:0	ADDR		SRAM address for program access via I <sup>2</sup> C interface												

#### 10.3.17 WDATA, LED Program Loading Data Register

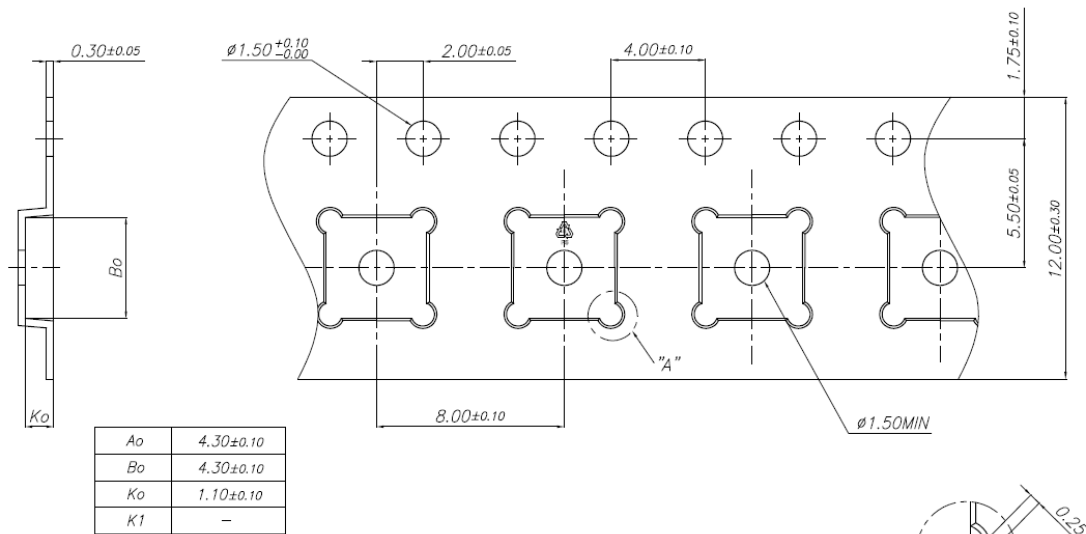
Address: 0x7F, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE															
Bit	Symbol		Description												
15:0	CODE		SARM data for program access via I <sup>2</sup> C interface												

#### 10.3.18 WPR, Writing Protection Register

Address: 0x7D, R/W, default: 0x5500															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPW								0	0	0	0	0	0	0	0
Bit	Symbol		Description												
15:8	WPW		writing protection control, If WPW=0x55, all register is writable, otherwise all register except for WPR is not allowed to be written.												

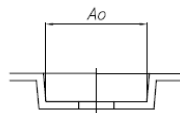
## 11 TAPE AND REEL INFORMATION

### 11.1 Carrier Tape

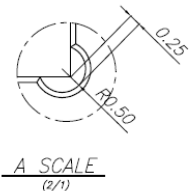


#### NOTES:

1. 10 sprocket hole pitch cumulative tolerance  $0.2/-0.2$
2. Camber not to exceed 1mm in 250mm
3. Material: Black conductive Polystyrene
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket center position relative to sprocket hole center measured as true position center of pocket, not pocket hole center.
7. Pocket center and pocket hole center must be same position.

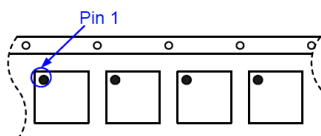


P/N: 433062

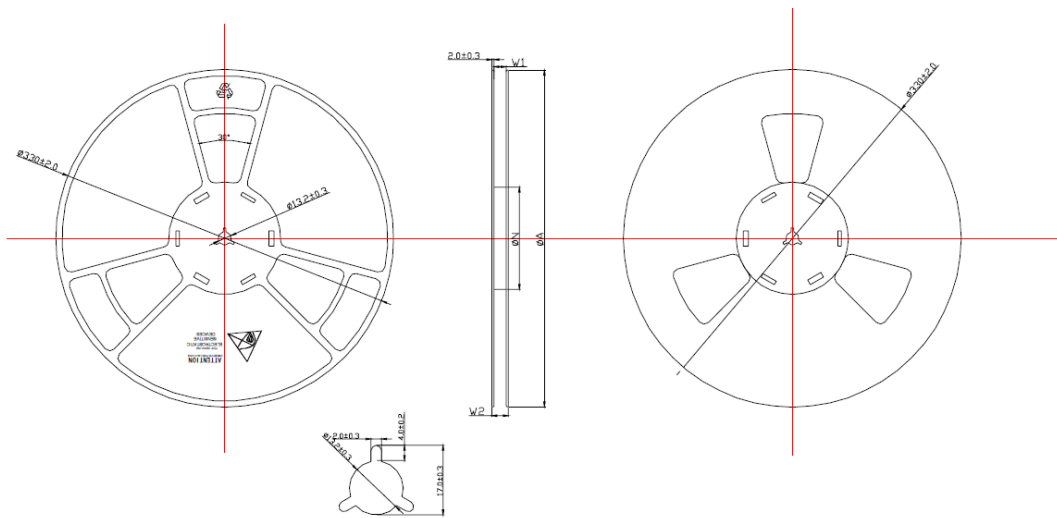


UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS		THIRD ANGLE PROJECTION		Kostat, Inc.	
TOLERANCE		DESIGN		TITLE	
DECIMALS	ANGULAR	M.H.KANG		CARRIER TAPE	
X.X ±0.13	± 1°	CHECK		QFN 4x4	
X.XX ±0.10		APPROVED		SIZE	AW
DO NOT SCALE DRAWING				DWG NO.	KS-1208-176
UNIT	mm			REV NO.	00
				SCALE	5/1
				RELEASE DATE	MAR.26.2004
				SHEET	1 of 1

### 11.2 PIN1 Direction



### 11.3 Reel

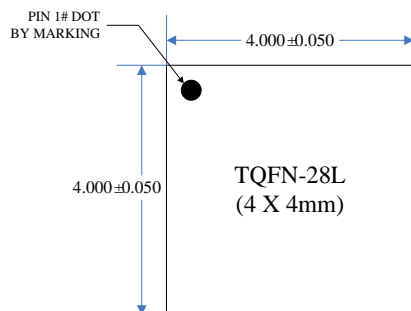


PRODUCT SPECIFICATIONS					DRN. : ZHD	2005. 06. 25	TITLE:Platic Reel
TYPE	WIDTH	$\phi A$	$\phi N$	$W1$ (Min)	$W2$ (Max)		
12MM		$330 \pm 2.0$	$100 \pm 1.0$	12.4	19.4	CHK. : RPP	13'' Inch< Dia> * 4'' Inch< HUB>
16mm		$330 \pm 2.0$	$100 \pm 1.0$	16.4	23.4		
24MM		$330 \pm 2.0$	$100 \pm 1.0$	24.4	31.4		
32MM		$330 \pm 2.0$	$100 \pm 1.0$	32.4	39.4	RPP. : XGM	2005. 06. 30
44MM		$330 \pm 2.0$	$100 \pm 1.0$	44.4	51.4		
							Dwg NO.:CM-REEL-03

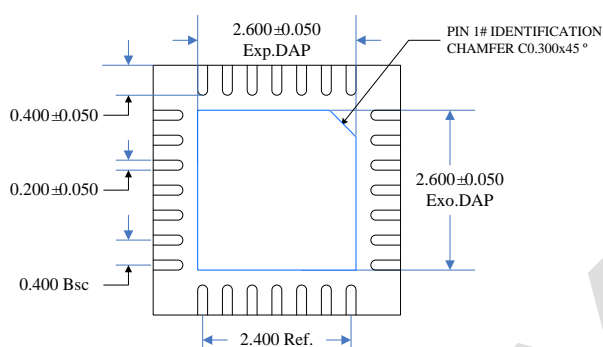
Notes:

1. Material: polystyrene
2. Flatness: maximum permissible 3mm
3. All dimensions are in millimeters
4. Surface resistivity:  $10^5$  to  $10^{11}$  ohms/sq or less
5. All unmarked tolerance:  $\pm 0.5$

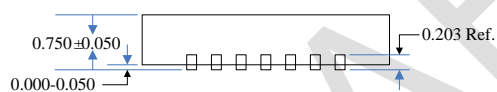
## 12 PACKAGE DESCRIPTION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

## 13 REVISION HISTORY

Vision	Date	Change Record
V1.0	Feb 2017	Officially Released

## 14 DISCLAIMER

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