Sil9533 Port Processor

Data Sheet

SiI-DS-1128-C

July 2014

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1. General Description

The Silicon Image SiI9533 Port Processor is the latest HDMI® port processor targeted at Home Theater in a Box (HTiB), and Soundbar applications. The port processor features InstaPort™ S and InstaPrevue™ technologies, Mobile High-Definition Link 2.1 (MHL®), 300 MHz HDMI, and Audio Return Channel (ARC).

MHL allows the user to attach a device to the HTiB or soundbar and view high-definition content while the mobile device battery is charging. MHL 2.1 supports 3D and PackedPixel Mode (PPM) in SiI9533 port processor and is supported on two input ports.

The SiI9533 port processor offers an extensive set of audio features, including audio extraction and insertion. Multi-channel audio from the active HDMI input can be extracted and sent to the audio output port. Additionally, a 2-channel PCM or bitstream audio from an audio DSP or an SoC can be inserted and sent to the HDMI output.

The SiI9533 device supports an ARC transceiver. ARC transceivers is configurable as either ARC receiver or ARC transmitter. As an ARC receiver in an AVR or HTiB design, the transmitter HDMI output can receive an ARC signal from a Digital Television (DTV). The ARC channel is configurable as an ARC transmitter and data from an S/PDIF output can be routed to the ARC transmitter.

1.1. HDMI Inputs and Outputs

- Three 300 MHz HDMI input ports and one output port
- 3.0 Gb/s TMDS™ cores
- HDMI, MHL, HDCP 1.4, and DVI compatible
- Supports video resolutions up to 8-bit 4K @ 30 Hz, 12-bit 1080p @ 60 Hz, or 12-bit 720p/1080i @ 120 Hz
- HDMI 2.0 Specification format supports 4K @ 50/60 Hz (when Pixel Encoding method is YCbCr 4:2:0 and InstaPrevue is disabled).
- Supports all mandatory and some optional 3D formats up to 300 MHz
- Supports up to1080p @ 60 Hz on two MHL input ports
- Supports 3D video in MHL mode
- Preprogrammed with HDCP keys
- Repeater function supports up to 127 devices

1.2. Performance Improvement Features

- InstaPort S viewing technology reduces port switching time to less than one second
- InstaPrevue technology provides a Picture-in-Picture (PIP) preview of connected source devices
- AVI, Audio InfoFrame, and video input resolution detection for all input ports, accessible port-by-port
- Hardware-based HDCP error detection and recovery minimizes firmware intervention
- Automatic output mute and unmute based on link stability, such as cable connect/detach

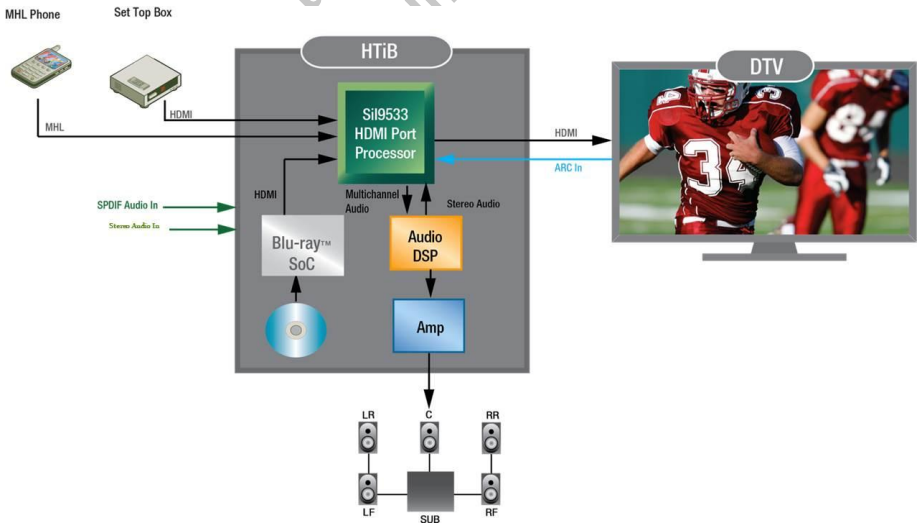


Figure 1.1. Typical HTiB Application

1.3. Audio Inputs and Outputs

- S/PDIF input and output support PCM and compressed audio formats up to 192 kHz, such as Dolby® Digital, DTS and AC-3
- DSD output supports Super Audio CD applications, up to six channels
- I^2S output supports PCM and DVD-audio output, up to eight channels at 192 kHz
- I^2S inputs support PCM and DVD-audio input, up to two channels at 192 kHz
- High bitrate audio output support, such as DTS-HD Master Audio™ and Dolby TrueHD
- Sample Rate Converter (SRC) support for downsampling 2:1 and 4:1
- One ARC input or output support

1.4. ESD and Latch-up

Conforming to JEDEC standards

1.5. Control Capability

- One Consumer Electronics Control (CEC) interface with CEC I/O to support an HDMI device
- Individual control of Hot Plug Detect (HPD) for every input port
- Achieved through the local I^2C bus

1.6. Packaging

88-pin, 10 mm × 10 mm, 0.4 mm pitch QFN package with an ePad

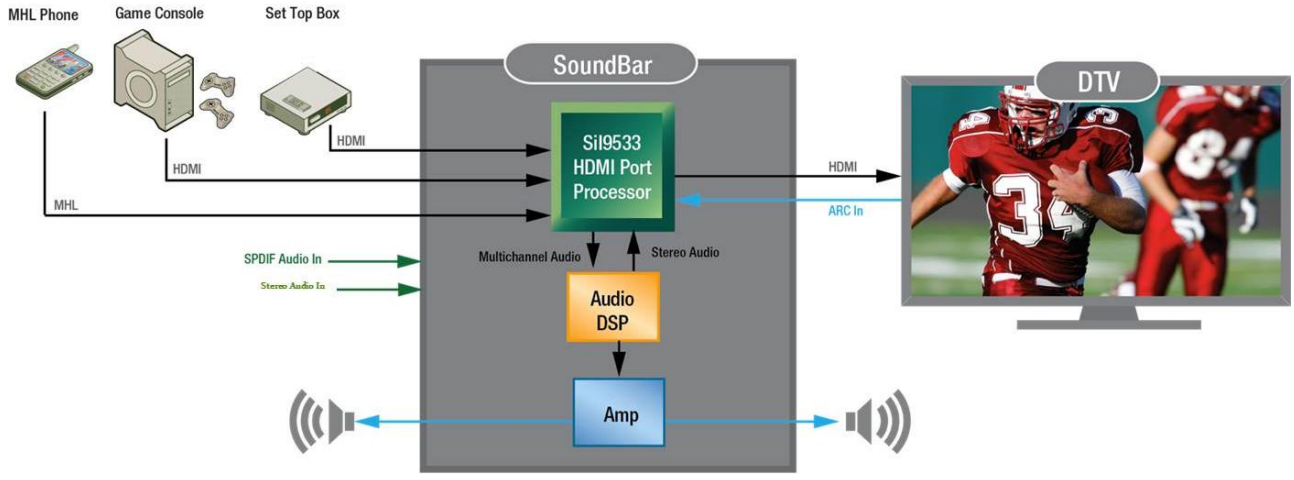


Figure 1.2. Typical SoundBar Application

2. Pin Diagram

Figure 2.1 shows the pin assignments of the SiI9533 port processor. The Pin Descriptions section beginning on page 25 describes the pin functions. The package is a 10 mm × 10 mm, 0.4 mm pitch, 88-pin QFN with ePad, which ***must*** be connected to ground.

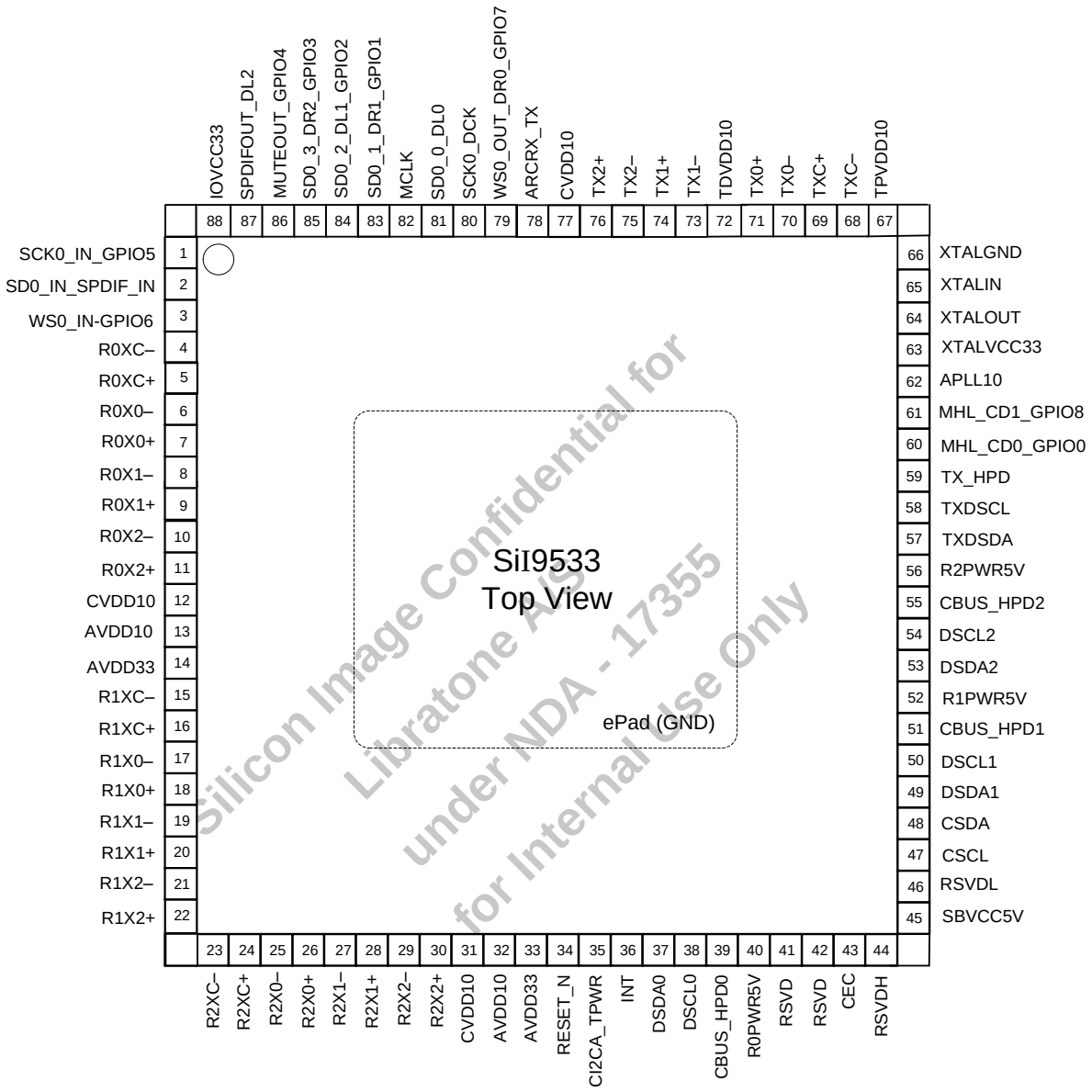


Figure 2.1. Pin Diagram

3. Functional Description

Figure 3.1 shows the block diagram of the SiI9533 port processor.

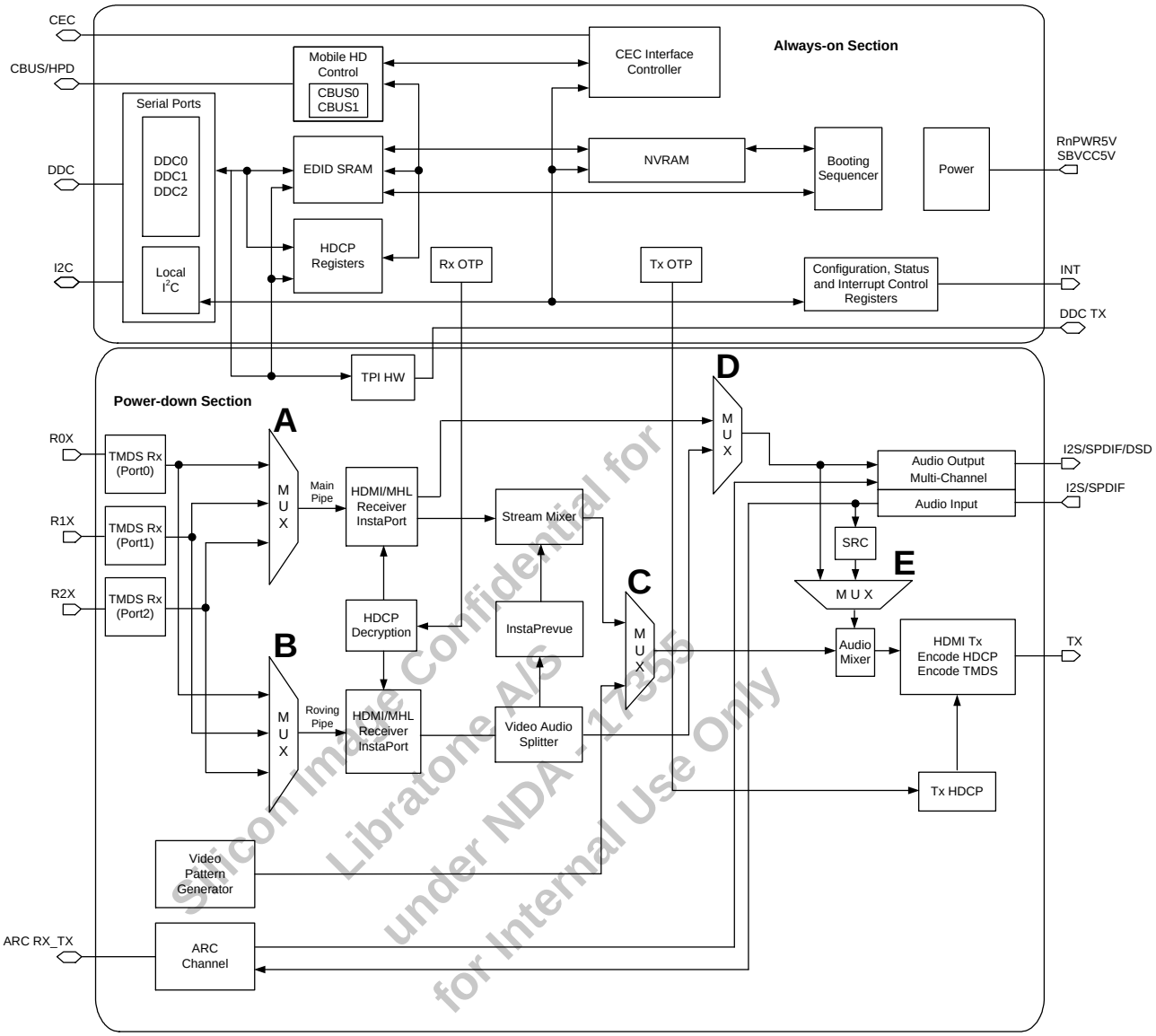


Figure 3.1. Functional Block Diagram

3.1. Always-on Section

The Always-on section contains the low-speed control circuits of the HDMI connection, the I^2C interfaces, internal memory blocks, and the registers that control the blocks of the Always-on section.

3.1.1. Serial Ports Block

The Serial Ports block provides four I²C serial interfaces: three DDC ports to communicate with the HDMI or DVI hosts, and one local I²C port for initialization and control by a local microcontroller in the HTiB, soundbar or display. Each interface is 5 V tolerant. Figure 3.2 shows the connection of the local I²C port to the system microcontroller.

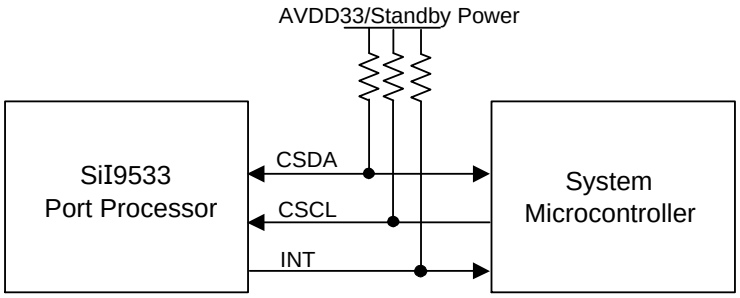


Figure 3.2. I²C Control Mode Configuration

The three DDC interfaces (DDC 0–2) on the SiI9533 port processor are slave interfaces that can run up to 400 kHz. Each interface connects to one E-DDC bus and is used to read the integrated EDID and HDCP authentication information. The port is accessible on the E-DDC bus at device addresses 0xA0, for EDID and 0x74, for HDCP control. The transmitter DDC master controller supports accessing HDCP and EDID up to 100 kHz. Local I²C can also access the transmitter DDC bus in bypass mode in which case the local I²C clock becomes the clock source.

3.1.2. Static RAM Block

The Static RAM (SRAM) block contains 1792 bytes of RAM. Each port is allocated a 256-byte block for DDC; this allows all ports to be read simultaneously from three different sources connected to the SiI9533 device. 640 bytes are available for the Key Selection Vectors (KSVs), while 128 bytes are used for auto-boot feature. The remaining bytes are unused. Every EDID and SHA KSV has an offset location. The SRAM is written to and read from using the local I²C interface and can also be read through the DDC interface. The memory is read through the DDC interface using only 5 V power from the HDMI connector.

3.1.3. NVRAM Block

The port processor contains 512 bytes of NVRAM. Of these, 256 bytes are used to store common EDID data used by each of the ports, 128 bytes are used by the auto-boot feature, and 128 bytes are unused. Both the NVRAM EDID data and NVRAM auto-boot data should be initialized by software using the local I²C bus at least once during manufacture.

3.1.4. HDCP Registers Block

The HDCP Registers block controls the necessary logic to decrypt the incoming audio and video data. The decryption process is controlled entirely by the host-side microcontroller, using a set sequence of register reads and writes through the local I²C channel. The decryption process uses preprogrammed HDCP keys and a Key Selection Vector (KSV) stored in the on-chip nonvolatile memory.

3.1.5. OTP ROM Block

The One-time Programmable (OTP) ROM block of the receiver is programmed at the factory, and contains the preprogrammed HDCP keys. System manufacturers do not need to purchase key sets from Digital Content Protection, LLC. Silicon Image handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security possible, as keys cannot be read out of the device after they are programmed.

3.1.6. Booting Sequencer

The booting sequencer boots the required data, such as EDID, initial HPD status, and MHL port selection from NVRAM during power on.

3.1.7. Configuration, Status, and Interrupt Control Block

The Configuration, Status, and Interrupt Control Registers block contains registers required for configuring and managing the SiI9533 device features. The registers are used to perform audio, video, and auxiliary format processing. The registers are also used for HDMI InfoFrame packet format and power-down control. The registers are accessible from the local I^2C port. This block also handles interrupt operation.

3.1.8. Mobile HD Control Block

The Mobile HD Control block handles MHL DDC control. This block handles CBUS conversion to DDC signals for accessing the EDID and HDCP interface blocks.

3.1.9. CEC Interface Controller

The Consumer Electronics Control (CEC) Interface Controller provides a CEC-compliant signal, and has a high-level register interface accessible through the I^2C interface. Programming is done through the Silicon Image CEC Programming Interface (CPI). This controller makes CEC control easy and straightforward as the host processor is not required to perform these low-level transactions on the CEC bus. CEC pass-through mode is therefore neither required nor supported.

3.1.10. Power Block

The Power block features an analog power multiplexer with inputs from the +5 V power from the R[0-2]PWR5V and the SBVCC5V sources. The output of the analog power multiplexer supplies power to the Always-on section.

3.2. Power-down Section

The Power-down section contains the HDMI high-speed data paths, the analog TMDS input and output blocks, and the digital logic for HDMI data and HDCP processing.

3.2.1. TMDS Receiver Blocks

The TMDS Receiver blocks, defined as Port 0, Port 1, and Port 2, are terminated separately, equalized under the control of the receiver digital block, and controlled by the local I^2C bus. Input data is oversampled by five to enable the downstream DPLL block to capture the most stable signal.

3.2.2. Input Multiplexer Blocks A, B, C, D, and E

There are three 3:1 Input Multiplexer blocks (A, B, and C) and two 2:1 Input Multiplexer blocks (D and E) in the SiI9533 port processor.

Input Multiplexer Block A selects one of the three TMDS inputs and sends it to the main pipe. Input Multiplexer Block B selects one of the three TMDS inputs and sends it to the roving pipe. Input Multiplexer Block C selects either main pipe or video pattern generator source and sends it to HDMI transmitter.

The specific function of the multiplexers is determined by whether InstaPort S or InstaPrevue is enabled. In InstaPort S or InstaPrevue modes, Multiplexer Block A selects the active input and sends it to the main pipe for processing. Multiplexer Block B sequentially selects one of the two inactive input signals and sends it to the InstaPort S or InstaPrevue blocks for processing.

Input Multiplexer Block D selects the decoded audio stream from the TMDS input of main pipe or the roving pipe, and sends it to Audio Output block.

Input Multiplexer Block E selects either the inserted audio, or the audio coming from the Multiplexer Block D, and sends it to the transmitter.

3.2.3. HDMI, MHL, and InstaPort S Receiver Blocks

The HDMI, MHL, and InstaPort S receiver blocks perform:

- Deskewing
- Analyzing packets
- Processing the main and roving pipes
- Multiplexing
- Repeater functions
- HDCP authentication

The SiI9533 device supports three 300 MHz HDMI input ports. MHL can be enabled on any two input ports, selected at the time of manufacture, by programming a register in the NVRAM.

3.2.4. Video/Audio Splitter Block

The Video/Audio Splitter block separates the video and audio data from the TMDS stream for the roving pipe. The video is sent to the InstaPrevue Block and the audio is sent to Multiplexer Block D. This can be used in the InstaPrevue Picture-in-Picture (PIP) mode, in which a single subwindow is displayed on the main video. The audio from the subwindow replaces the audio from the main video before it is sent to the transmitter.

3.2.5. InstaPrevue Block

The InstaPrevue block captures and processes all of the preauthenticated HDMI/DVI/MHL subframe images from the roving pipe. The operating preview mode is configured in this block.

3.2.6. Stream Mixer Block

The Stream Mixer block replaces a region of the main port video with a subframe image from the InstaPrevue block. It merges subframes with the main video input at the proper screen locations specified by external software register settings.

3.2.7. Video Pattern Generator Block

The Video Pattern Generator (VPG) block supplies one of eight predefined video patterns to the HDMI transmitter. The predefined video patterns include:

- Solid red
- Solid green
- Solid blue
- Solid black
- Solid white
- Ramp
- 8 × 6 chessboard
- Color bars

The resolutions of the video patterns in the RGB color space are: 480p, 576p, 720p @ 50/60 Hz, and 1080p @ 50 Hz video resolutions.

An example use of the VPG is to combine the predefined video pattern with an external audio input to create a complete HDMI stream, which can then be sent from the HDMI transmitter to a soundbar. The VPG can be used for test purposes during product development.

The VPG requires a pixel clock for its operation. The crystal oscillator (XCLK) or audio VCO clock, HDMI input clock or roving pipe clock can be used to generate the pixel clock for the VPG. If the crystal oscillator (XCLK) or the audio VCO clock is used as the clock source for the VPG, the frequency of the external audio crystal must be 27 MHz to generate the correct pixel clock frequencies for the VPG. Incorrect pixel clock frequencies are generated if the external audio crystal used is not 27 MHz. The XCLK is generated from the external audio crystal.

Table 3.1 shows the pixel clock source and frequency for the VPG at 480p, 576p, 720p, and 1080p video resolutions.

Refer to the *SiI9533 and SiI9535 Port Processor Programmer Reference* document (References section on page38) for details about configuring the VPG.

Table 3.1. Pixel Clock Source and Frequency

Video Resolution	Pixel Clock Source	Pixel Clock Frequency
480p, 576p	XCLK/Main/Roving Pipe	27 MHz
720p @ 50/60 Hz	Audio VCO Clock/Main/Roving Pipe	(27 MHz) • (11/4) = 74.25 MHz
1080p @ 50/60 Hz	Main Pipe/Roving Pipe	148.5 MHz

The audio VCO clock PLL is shared with the audio extraction logic. Therefore, if the audio VCO clock is used for the VPG, the audio extraction mode must be disabled.

3.2.8. Audio Sampling Rate Converter Block

The Audio Sampling Rate Converter (SRC) block allows the inserted 2-channel PCM audio from the audio port to be down-sampled before combining with the HDMI stream from the main pipe and sent to the transmitter. The audio data can be down-sampled by a factor of two or four using register control. Conversions from the following frequencies are supported:

- 192 kHz to 48 kHz
- 176.4 kHz to 44.1 kHz
- 96 kHz to 48 kHz
- 88.2 kHz to 44.1 kHz

3.2.9. Audio Input Block

The Audio Input block supports the insertion of external audio into the HDMI transmitter streams. The inserted audio can be 2-channel I^2S or S/PDIF.

Audio port insertion supports the following formats:

- I^2S, two channels: PCM, two channels
- S/PDIF, IEC 60958
  - PCM, two channels
  - Compressed bitstream: Dolby Digital, Dolby Digital Plus, Dolby Digital EX, Dolby Digital Surround EX DTS, DTS ES

The SiI9533 I^2S audio port insertion requires SCK, WS, and SD0 signals for 2-channel I^2S. The SiI9533 device supports CTS and N value generation without requiring an MCLK input.

The SiI9533 S/PDIF audio port insertion shares the SD0 pin with I^2S insertion. The functions of these pins are configured by software.

The audio inserted into the audio port can be combined with the audio dropped HDMI stream from the main pipe and sent to the transmitter.

3.2.10. Audio Output Block

The Audio Output block supports audio extraction from the received HDMI/MHL streams. The extracted audio is 8-channel I^2S, 6-channel DSD, or S/PDIF audio. The audio port extraction includes:

- I^2S, eight channels
  - PCM, up to eight channels
  - HBR, such as Dolby TrueHD, DTS-HD Master Audio
- DSD, six channels
- S/PDIF, IEC 60958
  - PCM, two channels
  - Compressed bitstream: Dolby Digital, Dolby Digital Plus, Dolby Digital EX, Dolby Digital Surround EX DTS, DTS ES

By default, the audio port is configured for 8-channel I^2S audio extraction from the main pipe.

The SiI9533 port processor I^2S audio extraction provides MUTEOUT, MCLK, SCK, WS, SD0, SD1, SD2, and SD3 signals for 8-channel I^2S from the audio port. The SiI9533 port processor audio port I^2S, DSD, and S/PDIF audio extraction pins are shared. The functions of these pins are configured by software.

3.2.11. Audio Return Channel Input and Output

The Audio Return Channel (ARC) feature eliminates an extra cable when it sends audio from an HDMI sink device to an adjacent HDMI source or repeater device. This is done by allowing a single IEC60958-1 audio stream to travel in the opposite direction of the TMDS signal on its own conductor in the HDMI cable. The HDMI sink device implements the ARC transmitter, and the HDMI source or repeater device implements the ARC receiver.

The SiI9533 device provides an ARC transceiver channel. The pin can be configured to operate as an ARC transmitter or an ARC receiver. For an ARC transmitter, the ARC transceiver pin is connected to the ARC pin of the connector for the HDMI receiver port that is designated as ARC-capable. For an ARC receiver, the ARC transceiver pin is connected to the ARC pin of the HDMI connector for the transmitter port that is designated as ARC-capable. The SiI9533 device supports only single-mode ARC.

3.2.12. TMDS Transmitter Block

The TMDS Transmitter block performs HDCP encryption and 8- to-10-bit TMDS encoding on the data to be transmitted over the HDMI link. The encoded data is sent to the three TMDS differential data lines, along with a TMDS differential clock line. Internal source termination eliminates the use of external RC components for signal shaping. The internal source termination can be disabled by register settings.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
AVDD33	TMDS Core Supply Voltage	−0.3	—	4.0	V	1, 2
IOVCC33	I/O Supply Voltage	−0.3	—	4.0	V	1, 2
SBVCC5V	5 V Standby Power Supply Voltage	−0.3	—	5.7	V	1, 2
R[0–2]PWR5V	5 V Input from Power Pin of HDMI Connector	−0.3	—	5.7	V	1, 2
XTALVCC33	PLL Crystal Oscillator Power	−0.3	—	4.0	V	1, 2
AVDD10	TMDS Receiver Core Supply Voltage	−0.3	—	1.5	V	1, 2
APLL10	PLL Analog VCC	−0.3	—	1.5	V	1, 2
CVDD10	Digital Core Supply Voltage	−0.3	—	1.5	V	1, 2
TDVDD10	TMDS Transmitter Core Supply Voltage	−0.3	—	1.5	V	1, 2
TPVDD10	TMDS Transmitter Core Supply Voltage	−0.3	—	1.5	V	1, 2
V_I	Input Voltage	−0.3	—	IOVCC33 + 0.3	V	1, 2
V_O	Output Voltage	−0.3	—	IOVCC33 + 0.3	V	1, 2
T_J	Junction Temperature	0	—	125	°C	—
T_{STG}	Storage Temperature	−65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section below.

4.2. Normal Operating Conditions

The supply voltage noise is measured at test point VDDTP shown in Figure 4.1 on the next page. The ferrite bead provides filtering of power supply noise. The figure also applies to other VDD pins.

Table 4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVDD33	TMDS Core Supply Voltage	3.14	3.3	3.46	V
IOVCC33	I/O Supply Voltage	3.14	3.3	3.46	V
SBVCC5V	5 V Standby Power Supply Voltage	4.5	5.0	5.5	V
R[0–2]PWR5V	5 V Input from Power Pin of HDMI Connector	4.5	5.0	5.5	V
XTALVCC33	PLL Crystal Oscillator Power	3.14	3.3	3.46	V
AVDD10	TMDS Receiver Core Supply Voltage	0.95	1.0	1.05	V
APLL10	PLL Analog VCC	0.95	1.0	1.05	V
CVDD10	Digital Core Supply Voltage	0.95	1.0	1.05	V
TDVDD10	TMDS Transmitter Core Supply Voltage	0.95	1.0	1.05	V
TPVDD10	TMDS Transmitter Core Supply Voltage	0.95	1.0	1.05	V
V_{DDN}	Supply Voltage Noise	—	—	100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	+25	+70	°C
Θ_{ja}	Ambient Thermal Resistance (Theta JA)*	—	26.4	—	°C/W
Θ_{jc}	Junction to Case Resistance (Theta JC)*	—	—	12.9	°C/W

Note: 16 Vias on 4-Layer PCB

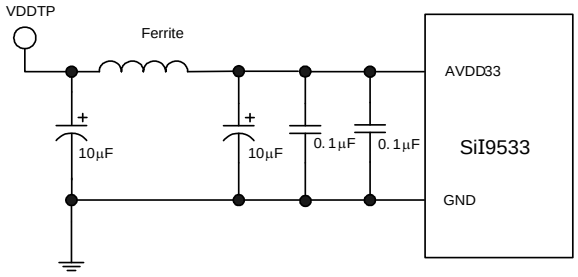


Figure 4.1. Test Point VDDTP for AVDD33 Noise Tolerance Specification

4.3. DC Specifications

Table 4.3. Digital I/O DC Specifications

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V
V_{TH+DDC}	LOW-to-HIGH Threshold, DDC Buses	Schmitt	—	3.0	—	—	V
V_{TH-DDC}	HIGH-to-LOW Threshold, DDC Buses	Schmitt	—	—	—	1.5	V
V_{TH+I2C}	LOW-to-HIGH Threshold, I^2C Buses	Schmitt	—	2.0	—	—	V
V_{TH-I2C}	HIGH-to-LOW Threshold, I^2C Buses	Schmitt	—	—	—	0.8	V
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V
V_{OL}	LOW-level Output Voltage	LVTTL	—	—	—	0.4	V
I_{OL}	Output Leakage Current	—	High-impedance	−10	—	10	µA
I_{OD4}	4 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	4	—	—	mA
			V_{OUT} = 0.4 V	4	—	—	mA
$V_{TH+RESET}$	LOW-to-HIGH Threshold, Reset	Schmitt	—	2.0	—	—	V
$V_{TH-RESET}$	HIGH-to-LOW Threshold, Reset	Schmitt	—	—	—	0.8	V

Table 4.4. TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ID}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	AVDD33 –400	—	AVDD33–37.5	mV

Table 4.5. TMDS Input DC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IDC}	Single-ended Input DC Voltage	—	AVDD33 –1200	—	AVDD33 –300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	The smaller of 720 and 0.85 V_{IDF}	mV

Table 4.6. TMDS Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SWING}	Single-ended Output Swing Voltage	R_{LOAD}: 50 Ω	400	—	600	mV
V_H	Single-ended High-level Output Voltage	—	AVDD33 –200	—	AVDD33 +10	mV
V_L	Single-ended Low-level Output Voltage	—	AVDD33 –700	—	AVDD33 –400	mV

Table 4.7. Single Mode Audio Return Channel DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{el}	Operating DC Voltage	—	0	—	5	V
$V_{el\ swing}$	Swing Amplitude	—	400	—	600	mV

Table 4.8. S/PDIF Input Port DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
Z_{I_SPDIF}	Termination Impedance	—	—	75	—	Ω	1
		—	—	4	—	kΩ	2
V_{I_SPDIF}	Input Voltage	75 Ω termination, AC-coupled	400	—	600	mV_{PP}	3

Notes:

1. This impedance is implemented with an external 75 Ω resistor to ground and is used when the interconnection is over a 75 Ω COAX cable.
2. This is the internal impedance of the S/PDIF input.
3. The S/PDIF input can also be safely driven at LVTTL voltage levels without AC-coupling. The 75 Ω termination is not required in this case.

Table 4.9. CEC DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TH+CEC}	LOW-to-HIGH Threshold	—	2.0	—	—	V
V_{TH-CEC}	HIGH-to-LOW Threshold	—	—	—	0.8	V
V_{OH_CEC}	HIGH-level Output Voltage	—	2.5	—	—	V
V_{OL_CEC}	LOW-level Output Voltage	—	—	—	0.6	V
I_{IL_CEC}	Input Leakage Current	Power Off; R*n*PWR5V: 0 V	—	—	1.8	µA

Table 4.10. CBUS DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH_CBUS}	HIGH-level Input Voltage	—	1.0	—	—	V
V_{IL_CBUS}	LOW-level Input Voltage	—	—	—	0.6	V
V_{OH_CBUS}	HIGH-level Output Voltage	I_{OH} = −100 µA	1.5	—	—	V
V_{OL_CBUS}	LOW-level Output Voltage	I_{OL} = 100 µA	—	—	0.2	V
Z_{DSC_CBUS}	Pull-down Resistance: Discovery	—	800	1000	1200	Ω
Z_{ON_CBUS}	Pull-down Resistance: Active	—	90	100	110	kΩ
I_{IL_CBUS}	Input Leakage Current	High-impedance	—	—	1	µA
C_{CBUS}	Capacitance	Power Off	—	—	30	pF

Table 4.11. Power Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{APLL10}	Supply Current for APLL10	—	—	2	mA	1
I_{AVDD10}	Supply Current for AVDD10	—	—	143	mA	1
I_{AVDD33}	Supply Current for AVDD33	—	—	179	mA	1
$I_{IOVCC33}$	Supply Current for IOVCC33	—	—	6	mA	1
$I_{XTALVCC33}$	Supply Current for XTALVCC33	—	—	6	mA	1
I_{CVDD10}	Supply Current for CVDD10	—	—	230	mA	1
$I_{SBVCC5STBY}$	Supply Current for SBVCC5V in Standby Mode	—	—	12	mA	2
$I_{SBVCC5ACT}$	Supply Current for SBVCC5V in Active Mode	—	—	15	mA	1
$I_{TDVDD10}$	Supply Current for TDVDD10	—	—	28	mA	1
$I_{TPVDD10}$	Supply Current for TPVDD10	—	—	7	mA	1
Total	Total Power	—	—	1.22	W	1

Notes:

1. With all 300 MHz HDMI receiver inputs, InstaPort S, InstaPrevue, audio outputs, and 300 MHz transmitter output.
2. With no active AV sources connected to the HDMI receiver inputs.

4.4. AC Specifications

Table 4.12. TMDS Input Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{RXDPS}	Intrapair Differential Input Skew	—	—	—	0.4	T_{BIT}
T_{RXCCS}	Channel-to-Channel Differential Input Skew	—	—	—	0.2 T_{PIXEL} + 1.78	ns
F_{RXC}	Differential Input Clock Frequency	—	25	—	300	MHz
T_{RXC}	Differential Input Clock Period	—	3.33	—	40	ns
T_{IJIT}	Differential Input Clock Jitter Tolerance (0.3 T_{BIT})	300 MHz	—	—	100	ps

Table 4.13. TMDS Input Timing AC Specifications – MHL Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{SKEW_DF}	Input Differential Intrapair Skew	—	—	—	93	ps
T_{SKEW_CM}	Input Common-mode Intrapair Skew	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.33	—	40	ns
T_{CLOCK_JIT}	Common-mode Clock Jitter Tolerance	—	—	—	0.9 T_{BIT}	ps
T_{DATA_JIT}	Differential Data Jitter Tolerance	—	—	—	0.6 T_{BIT}	ps

Table 4.14. TMDS Output Timing AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{TXDPS}	Intrapair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRT}	Data/Clock Rise Time	20%–80%	75	—	—	ps
T_{TXFT}	Data/Clock Fall Time	80%–20%	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.25	T_{BIT}

Table 4.15. Single Mode Audio Return Channel AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{ASMRT}	Rise Time	10%–90%	—	—	60	ns
T_{ASMFT}	Fall Time	90%–10%	—	—	60	ns
T_{ASMJIT}	Jitter Max	—	—	—	0.05	UI*
F_{ASMDEV}	Clock Frequency Deviation	—	–1000	—	1000	ppm

***Note:** Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF Specification.

Table 4.16. CEC AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{R_CEC}	Rise Time	10%–90%	—	—	250	µs
T_{F_CEC}	Fall Time	90%–10%	—	—	50	µs

Table 4.17. CBUS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{BIT_CBUS}	Bit Time	1 MHz clock	0.8	—	1.2	µs
T_{BJIT_CBUS}	Bit-to-Bit Jitter	—	–1%	—	+1%	T_{BIT_CBUS}
T_{DUTY_CBUS}	Duty Cycle of 1 Bit	—	40%	—	60%	T_{BIT_CBUS}
T_{R_CBUS}	Rise Time	0.2 V–1.5 V	5	—	200	ns
T_{F_CBUS}	Fall Time	0.2 V–1.5 V	5	—	200	ns
ΔT_{RF}	Rise-to-Fall Time Difference	—	—	—	100	ns

4.4.1. Control Signal Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.18. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
T_{RESET}	RESET_N signal LOW time required for reset.	—	50	—	—	µs	1
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command.	C_L = 400pF	—	—	700	ns	2, 5
T_{HDDAT}	I^2C data hold time.	0–400 kHz	0	—	—	ns	3, 5, 6
T_{INT}	Response time for INT output pin from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET_N = HIGH	—	—	100	µs	—
F_{SCL}	Frequency on master DDC SCL signal.	—	40	70	100	kHz	4
F_{CSCL}	Frequency on master CSCL signal.	—	40	—	400	kHz	—

Notes:

1. Reset on RESET_N signal can be LOW as the supply becomes stable (shown in Figure 4.2 on the next page), or pulled LOW for at least T_{RESET} (shown in Figure 5.2 on page 22).
2. All standard mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (pins CSDA and CSCL) and to the master I^2C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA signals as an I^2C slave. The device does not include the 300 ns internal delay required by the I^2C Specification (Version 2.1, Table 5, note 2).
4. The master DDC block provides an SCL signal for the E-DDC bus. The HDMI Specification limits this to I^2C standard mode or 100 kHz.
5. Operation of I^2C pins above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL}. For these levels, I^2C speed up to 400 kHz (fast mode) is supported.
6. All I^2C timings for 400 kHz operation follow those defined for Fast-Mode I^2C

Table 4.19. Audio Crystal Frequency

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{XTAL}	External Crystal Frequency	—	26	27	28.5	MHz

Note: F_{XTAL} must be 27 MHz if the crystal oscillator (XCLK) is used as the clock source for the video pattern generator.

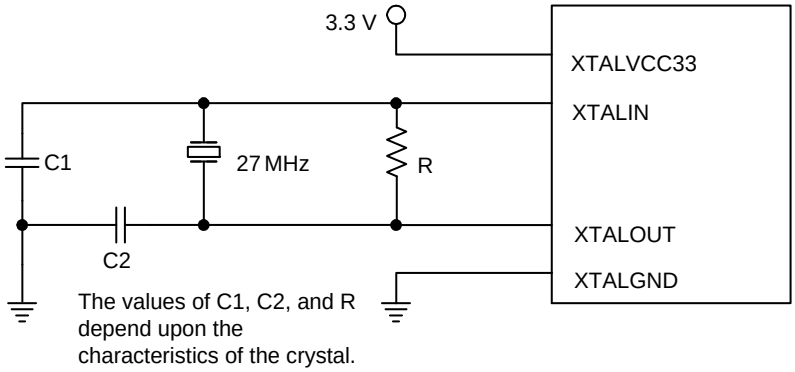


Figure 4.2. Audio Crystal Schematic

Note: The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

4.4.2. Audio Input Timing

Table 4.20. S/PDIF Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure	Note
F_{S_SPDIF}	Sample Rate	2-Channel	32	—	192	kHz	—	—
T_{SPCYC}	S/PDIF Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 5.5	*
T_{SPDUTY}	S/PDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 5.5	*

*** Note:** Proportional to unit time (UI) according to sample rate. Refer to the I^2S or S/PDIF Specifications.

Table 4.21. I^2S Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I^2S Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 5.4	1
$T_{SCKDUTY}$	I^2S Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 5.4	—
T_{I2SSU}	I^2S Setup Time	C_L = 10 pF	15	—	—	ns	Figure 5.4	2
T_{I2SHD}	I^2S Hold Time	C_L = 10 pF	0	—	—	ns	Figure 5.4	2

Notes:

1. Proportional to unit time (UI) according to sample rate. Refer to the I^2S or S/PDIF Specifications.
2. Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I^2S Specification.

4.4.3. Audio Output Timing

Table 4.22. I²S Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{TR}	SCK Clock Period (Tx)	C_L = 10 pF	1.0	—	—	T_{TR}
T_{HC}	SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{TR}
T_{LC}	SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{TR}
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40	—	60	% T_{TR}
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5.0	—	5.0	ns

Note: Refer to Figure 5.6 on page 24.

Table 4.23. S/PDIF Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI[1]
F_{SPDIF}	SPDIF Frequency	—	4.0	—	24.0	MHz
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90.0	—	110.0	% T_{SPCYC}
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20.0	—	250	ns
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4.0	—	50.0	MHz
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	45	—	65	% $T_{MCLKCYC}$

Notes:

1. Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF Specification.
2. Refer to Figure 5.7 and Figure 5.8 on page 24.

5. Timing Diagrams

5.1. Reset Timing Diagrams

VCC must be stable between the limits shown in the Normal Operating Conditions section on page 15 for $T_{RESET,}$ before RESET_N goes HIGH, as shown in Figure 5.1. Before accessing registers, RESET_N must be pulled LOW for T_{RESET}. This can be done by holding RESET_N LOW until T_{RESET} after stable power, or by pulling RESET_N LOW from a HIGH state for at least T_{RESET}, as shown in Figure 5.2.

Note: VCC can be one of R*n*PPWR5V or SBVCC5V.

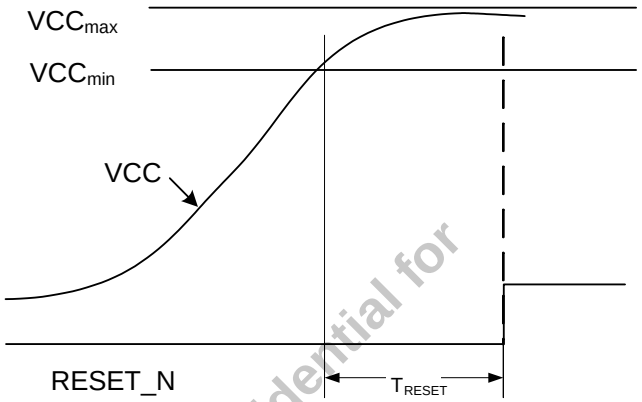


Figure 5.1. Conditions for Use of RESET_N

Figure 5.2. RESET_N Minimum Timing

5.2. I²C Timing Diagram

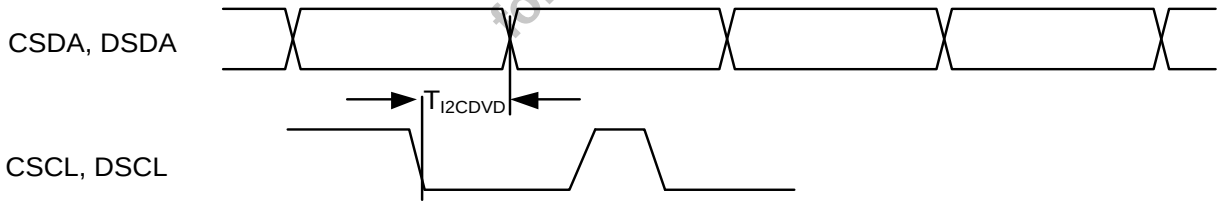


Figure 5.3. I²C Data Valid Delay, Driving Read Cycle Data

5.3. Digital Audio Input Timing

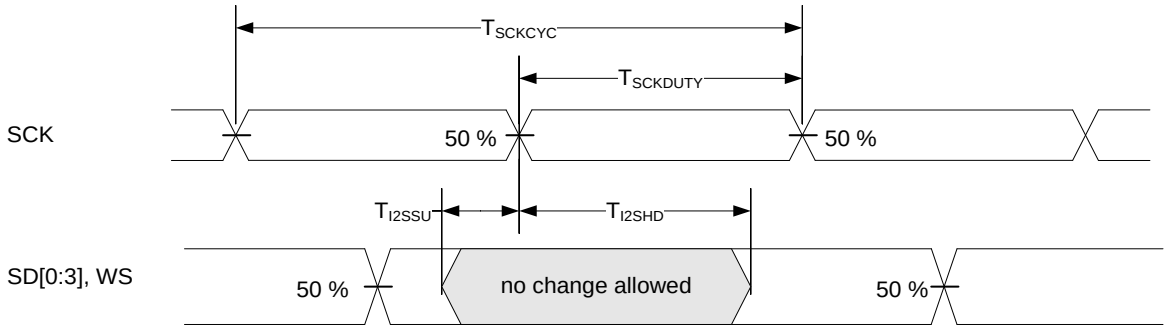


Figure 5.4. I²S Input Timing

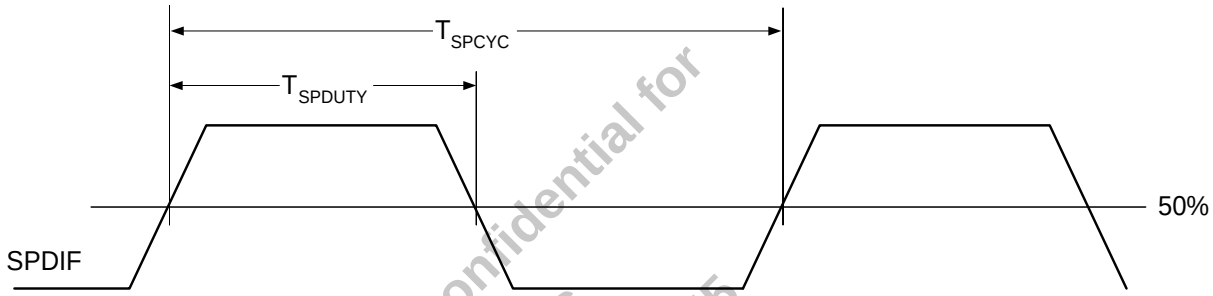


Figure 5.5. S/PDIF Input Timing

5.4. Digital Audio Output Timing

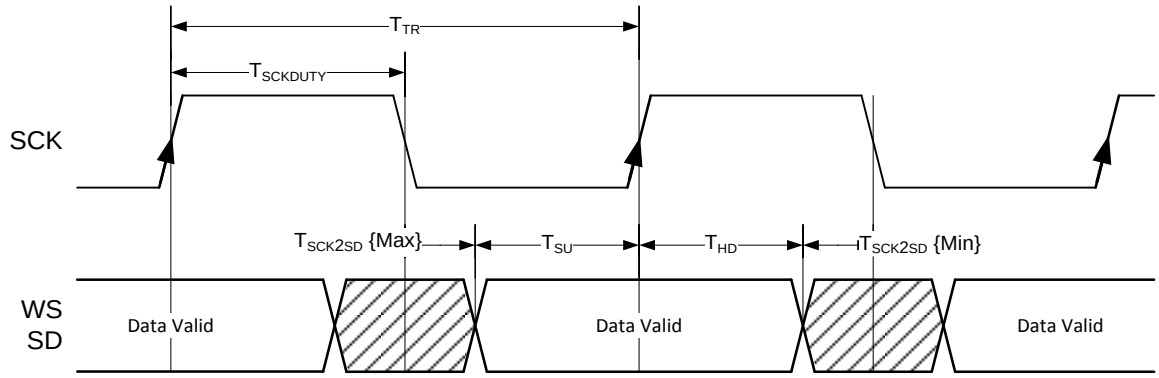


Figure 5.6. I²S Output Timing

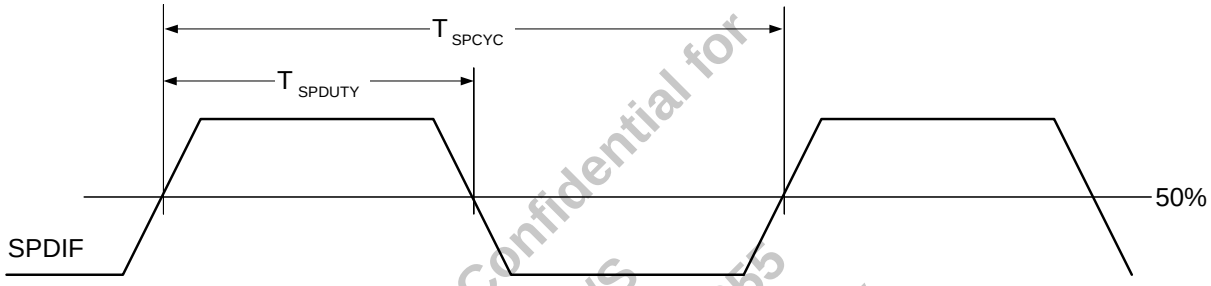


Figure 5.7. S/PDIF Output Timing

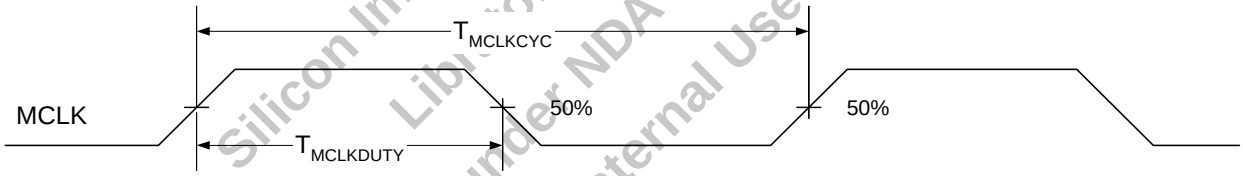


Figure 5.8. MCLK Timing

6. Pin Descriptions

6.1. HDMI Receiver and MHL Port Pins

Name	Pin	Type	Dir	Description
R0X0+	7	TMDS Analog	Input	HDMI Receiver Port 0 TMDS Input Data Pairs.
R0X0–	6			
R0X1+	9			
R0X1–	8			
R0X2+	11			
R0X2–	10			
R0XC+	5	TMDS Analog	Input	HDMI Receiver Port 0 TMDS Input Clock Pair.
R0XC–	4			
R1X0+	18	TMDS Analog	Input	HDMI Receiver Port 1TMDS Input Data Pairs.
R1X0–	17			
R1X1+	20			
R1X1–	19			
R1X2+	22			
R1X2–	21			
R1XC+	16	TMDS Analog	Input	HDMI Receiver Port 1 TMDS Input Clock Pair.
R1XC–	15			
R2X0+	26	TMDS Analog	Input	HDMI Receiver Port 2 TMDS Input Data Pairs.
R2X0–	25			
R2X1+	28			
R2X1–	27			
R2X2+	30			
R2X2–	29			
R2XC+	24	TMDS Analog	Input	HDMI Receiver Port 2 TMDS Input Clock Pair.
R2XC–	23			

Note: For any two ports, such as Port *n* and Port *m* that have been configured as MHL inputs, the R*n*X0+ and R*n*X0– pin pair and the R*m*X0+ and R*m*X0– pin pair carry the respective MHL signals.

6.2. HDMI Transmitter Port Pins

Name	Pin	Type	Dir	Description
TX0+	71	TMDS Analog	Output	HDMI Transmitter TMDS Output Data Pairs.
TX0–	70			Main HDMI transmitter output port TMDS data pairs.
TX1+	74			
TX1–	73			
TX2+	76			
TX2–	75			
TXC+	69	TMDS Analog	Output	HDMI Transmitter TMDS Output Clock Pair.
TXC–	68			Main HDMI transmitter output port TMDS clock pair.

6.3. Audio Pins

Name	Pin	Type	Dir	Description	Default State
MCLK	82	LVTTL 8 mA	Output	Master Clock Output.	—
SCK0_DCK	80	LVTTL 4 mA	Output	I^2S Serial Clock Output/DSD Clock Output.	SCK0
WS0_OUT_DR0_ GPIO7	79	LVTTL 4 mA	Output	I^2S Word Select Output/DSD Data Right Bit 0/ GPIO 7.	GPIO7
SD0_0_DL0	81	LVTTL 4 mA	Input/ Output	I^2S Serial Data 0 Output/DSD Data Left Bit 0 Output.	SD0_0
SD0_1_DR1_ GPIO1	83	LVTTL 4 mA	Input/ Output	I^2S Serial Data 1 Output/DSD Data Right Bit 1 Output/ Programmable GPIO 1.	GPIO1
SD0_2_DL1_ GPIO2	84	LVTTL 4 mA	Input/ Output	I^2S Serial Data 2 Output/DSD Data Left Bit 1 Output/ Programmable GPIO 2.	GPIO2
SD0_3_DR2_ GPIO3	85	LVTTL 4 mA	Input/ Output	I^2S Serial Data 3 Output/DSD Data Right Bit 2/ Programmable GPIO 3.	GPIO3
SPDIFOUT/DL2	87	LVTTL 4 mA	Output	S/PDIF Output/DSD Data Left Bit 2.	SPDIFOUT
SCK0_IN_GPIO5	1	LVTTL 4 mA	Input/ Output	I^2S Serial Clock Input/Programmable GPIO 5.	GPIO5
WS0_IN_GPIO6	3	LVTTL 4 mA	Input/ Output	I^2S Word Select Input/Programmable GPIO 6.	GPIO6
SD0_IN_ SPDIF_IN	2	LVTTL 4 mA	Input	I^2S Serial Data Input/S/PDIF Input.	See Table Note
MUTEOUT_ GPIO4	86	LVTTL 4 mA	Input/ Output	Mute Audio Output/Programmable GPIO 4.	GPIO4
ARCRX_TX	78	Analog	Input/ Output	Audio Return Channel. This pin transmits or receives an IEC60958-1 audio stream. In ARC transmitter mode, received on the SPDIF_IN input pin, this pin transmits an S/PDIF signal to an ARC receiver-capable source device (such as HTiB) or a repeater device (such as AVR), using single-mode ARC. In ARC receiver mode, transmitted through the SPDIF_OUT pin, this pin receives a S/PDIF signal from an ARC transmitter-capable sink device (such as DTV), using single-mode ARC. The channel can either be an ARC input or an ARC output at a time.	—

Note: Since audio insertion is not enabled by default, either SD0_IN or SPDIF_IN is configured based on programming.

6.4. CEC Pin

Name	Pin	Type	Dir	Description
CEC	43	CEC Compliant 5 V tolerant, Schmitt, LVTTL	Input/ Output	CEC I/O is used for interfacing to CEC devices. This signal is electrically compliant with CEC Specification. As an input, this pin acts as an LVTTL Schmitt input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor. This signal should be connected to the CEC signal of all HDMI input and output ports, if the system supports just one CEC line. ***OR*** In a system designed to have separate CEC connectivity for the HDMI input and output ports, this signal should be connected to the CEC signal of all the input ports supported in the system. This signal and CEC each connect to a separate CEC controller within the port processor and are independent of each other.

6.5. Configuration Pins

Name	Pin	Type	Dir	Description
CI2CA_TPWR	35	LVTTL 5 V tolerant	Input/ Output	I^2C Slave Address Input/Transmit Power Sense Output. During Power-on-Reset (POR), this pin is used as an input to latch the I^2C subaddress. The level on this pin is latched when the POR transitions from the asserted state to the deasserted state. After completion of POR, this pin is used as the TPWR output. Register setting can change this pin to show if the active port is receiving a TMDS clock.
INT	36	Schmitt Open-drain 8 mA 3.3 V tolerant	Output	Interrupt Output. This is an open-drain output and requires an external pull-up resistor.

6.6. Control Pins

Name	Pin	Type	Dir	Description
CSCL	47	LVTTL Schmitt Open-drain 5 V tolerant	Input	Local Configuration/Status I^2C Clock. Chip configuration/status is accessed using this I^2C port. This pin is true open-drain, so it does not pull to ground if power is not applied. See Figure 3.2 on page 10.
CSDA	48	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local Configuration/Status I^2C Data. Chip configuration/status is accessed using this I^2C port. This pin is true open-drain, so it does not pull to ground if power is not applied. See Figure 3.2 on page 10.
RESET_N	34	LVTTL Schmitt 5 V tolerant	Input	External Reset. Active LOW. Should be pulled to 3.3 V supply.

6.7. Crystal Pins

Name	Pin	Type	Dir	Description
XTALOUT	64	LVTTL 4 mA	Output	Crystal Clock Output.
XTALIN	65	LVTTL 5 V tolerant	Input	Crystal Clock Input.

6.8. DDC I²C Pins

Name	Pin	Type	Dir	Description
DSDA0	37	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I²C Data for respective HDMI receiver port. These signals are true open-drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSDA1	49			
DSDA2	53			
DSCL0	38	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC I²C Clock for respective HDMI receiver port. These signals are true open-drain, and do not pull to ground when power is not applied to the device. These pins require an external pull-up resistor.
DSCL1	50			
DSCL2	54			
TXDSDA	57	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Master I²C Data for HDMI transmitter port. This signal is true open-drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.
TXDSCL	58	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	DDC Master I²C Clock for HDMI transmitter port. This signal is true open-drain, and does not pull to ground when power is not applied to the device. This pin requires an external pull-up resistor.

6.9. System Switching Pins

Name	Pin	Type	Dir	Description	Default State
R0PWR5V	40	LVTTL 5 V tolerant	Input	5 V Port Detection Input for respective HDMI receiver port. Connect to 5 V signal from HDMI input connector. These pins require a 10 Ω series resistor, a 5.1 kΩ pull-down resistor, and at least a 1 µF capacitor to ground.	—
R1PWR5V	52				—
R2PWR5V	56				—
CBUS_HPD0	39	LVTTL 1.5 mA 5 V tolerant Analog	Input/ Output	Hot Plug Detect Output for the respective HDMI receiver port. In MHL mode, these pins serve as the respective CTRL BUS.	—
CBUS_HPD1	51				—
CBUS_HPD2	55				—
TX_HPD	59	LVTTL, Schmitt 5V tolerant	Input	Hot Plug Detect Input for HDMI transmitter port.	—
MHL_CD1_ GPIO8	61	LVTTL Schmitt Open drain 5 V tolerant	Input/ Output	MHL Cable Detect 0/Programmable GPIO 8.	MHL_CD1_GPIO8*
MHL_CD0_ GPIO0	60	LVTTL Schmitt Open drain 5 V tolerant	Input/ Output	MHL Cable Detect 1/Programmable GPIO 0.	MHL_CD0_GPIO0*

***Note:** MHL_CD1_GPIO8 & MHL_CD0_GPIO0 pads are in input mode by default.

6.10. Power and Ground Pins

Name	Pin	Type	Description	Supply
AVDD33	14, 33	Power	TMDS Core VDD. AVDD33 should be isolated from other system supplies to prevent leakage from the source device through the TMDS input pins. AVDD33 should not be used to power other system components that can be adversely affected by such leakage.	3.3 V
IOVCC33	88	Power	I/O VCC.	3.3 V
SBVCC5	45	Power	Local Power from system. This pin requires a 10 Ω series resistor.	5.0 V
AVDD10	13, 32	Power	TMDS Receiver Core VDD.	1.0 V
CVDD10	12, 31, 77	Power	Digital Core Potential.	1.0 V
APLL10	62	Power	PLL Analog VCC.	1.0 V
TPVDD10	67	Power	Analog Power for TMDS Transmitter Core.	1.0 V
TDVDD10	72	Power	Digital Power for TMDS Transmitter Core.	1.0 V
XTALVCC33	63	Power	PLL Crystal Oscillator Power.	3.3 V
XTALGND	66	Ground	PLL Crystal Oscillator Ground.	GND
GND	ePad	Ground	The ePad ***must*** be soldered to ground, as this is the only ground connection for the device.	GND

6.11. Reserved

Name	Pin	Type	Description	Supply
RSVDL	46	—	Reserved Low	—
RSVD	41, 42	—	Do not connect	—
RSVDH	44	—	Reserved High	3.3 V

7. Feature Information

7.1. Standby and HDMI Port Power Supplies

The SBVCC5V port processor 5 V standby power supply pin can be used to supply power to the EDID and CEC portions of the device when all other power supplies are turned off. This arrangement results in a low-power mode, but allows the EDID to be readable and the CEC controllers to be operational. Table 7.1 summarizes the power modes available in the SiI9533 port processor. Figure 7.1 shows a block diagram of the standby power supply sources and the Always-on power island.

Table 7.1. Description of Power Modes

Power Mode	Description	SBVCC5	RnPWR5V	AVDD33	AVDD10
Power-on mode	All power supplies to the SiI9533 chip are On. All functions are available. The standby power supply is 5 V.	5 V	NA	3.3 V	1.0 V
Standby power mode	The Always-on power domain is On, supplied from the internal power MUX. All other supplies are Off. The standby power supply is 5 V. In this mode, EDID and CEC are functional, but video and audio processing is not performed, and all outputs are Off.	5 V	NA	Off	Off
HDMI Port only power	Power is Off to the device. HDMI +5 V from the HDMI cable is the only power source. For example, if the TV is unplugged from the AC wall outlet, the EDID and CEC are functional in this mode.	Off	5 V on any input	Off	Off

Note: All other supplies are on in the power-on mode and off in all other modes.

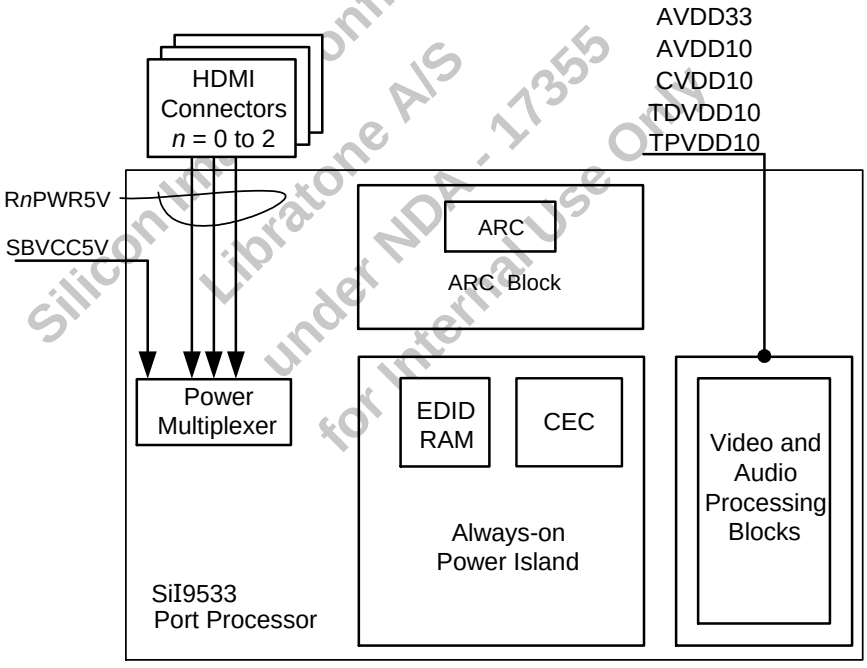


Figure 7.1. Standby Power Supply Diagram

If all power is off to the device, the EDID can still be read from the source by using power from the HDMI connector +5 V signal. In this case, the internal power MUX automatically switches to the HDMI connector power for powering the always-on logic. In this mode, only the EDID and CEC blocks are functional; all other functions of the device are in power-off mode. No damage occurs to the device in this mode.

7.2. InstaPort S

The SiI9533 port processor supports InstaPort S HDCP preauthentication feature, which reduces the HDCP authentication time. HDCP authentication is started on an upstream (input) port immediately after a source device is connected, regardless of whether the port is currently selected for output to the downstream sink device. All nonselected ports are HDCP authenticated in this manner. As soon as HDCP is authenticated, it is maintained in the background. When a nonselected port is selected, the authenticated content is immediately available. This feature reduces port switching time to less than one second.

7.3. InstaPrevue

The SiI9533 device incorporates the InstaPrevue feature, which periodically provides updated Picture-in-Picture previews, of each connected source device. The contents of each preauthenticated TMDS source device that is not being viewed can be displayed as a small subwindow overlaid onto the main video that is currently being viewed. With this feature, DTV and AVR manufacturers can provide end-users with a content-based, rather than a text-based user interface for changing or selecting among Blu-ray disc players, set-top boxes, DVD players, game consoles, or other HDMI/DVI/MHL connected sources.

InstaPrevue operates in one of three modes:

- The *All Preview* mode displays one to two subwindows, selected by the user, regardless of whether a source device is connected or not. A subwindow with a manufacturer- defined color is displayed for an unconnected source device.
- The *Active* mode displays only the subwindow of a connected, active, and authenticated source device.
- The *Selected* mode displays a single subwindow of a connected source device selected by the user and is intended as a Picture-in-Picture preview.

The supported combinations of main video display and InstaPrevue window formats are shown in Table 7.2. InstaPrevue is compatible with RGB, YC4:4:4, and YC4:2:2 color formats.

Table 7.2. Supported Combinations of Main Video and InstaPreview Displays

Main Video Display Format	InstaPrevue Window Format	Supported?
All supported 2D Resolutions	All supported 2D Resolutions except 4K x 2K	Yes
	720p and 1080p 3D Frame Packing	Yes
	480p and 1080i 3D Frame Packing	No
	3D Side-by-Side (Half)	No
	3D Side-by-Side (Full)	No
	3D Top-and-Bottom	No
720p and 1080p 3D Frame Packing	All supported 2D Resolutions except 4K x 2K	Yes
	720p and 1080p 3D Frame Packing	Yes
	480p and 1080i 3D Frame Packing	No
	3D Side-by-Side (Half)	No
	3D Top-and-Bottom	No
480p and 1080i 3D Frame Packing	All Formats	No
3D Top-and-Bottom		
3D Side-by-Side (Half)		
3D Side-by-Side (Full)		

7.4. MHL Receiver

The SiI9533 port processor supports the Mobile High-Definition Link (MHL) as a sink device on two of the three receiver ports (selected at the time of manufacture). MHL is a high-speed multimedia data transfer protocol intended for use between mobile and display devices. The SiI9533 device supports HDMI and MHL modes simultaneously on the two selected receiver ports. When an HDMI source is connected, the receiver port is configured as an HDMI port. When an MHL source is connected, an MHL cable detect sense signal is asserted and sent to the SiI9533 device. A signal is also sent to the host microcontroller as an interrupt to configure the receiver port as an MHL port, and to initiate the CBUS discovery process.

MHL carries video, audio, auxiliary, control data, and power across a cable consisting of five conductors.

One connection is for a dedicated ground that is used as the 0 V reference for the signals on the remaining four connections. Two other conductors form a single-channel TMDS differential signal pair to send video, audio and auxiliary data from the source device to the sink device. On the SiI9533 device, the MHL TMDS channel differential signal pair pins are shared with the RX0+ and RX0– pins of the HDMI TMDS channel differential signal pair.

Another connection is for the MHL Control Bus (CBUS). The CBUS carries control information that provides configuration and status exchanges between the source and the sink devices. CBUS is a software/hardware protocol that supports four types of packet transfers: Display Data Control (DDC), Vendor-specific, MHL Sideband Channel (MSC) and a reserved type.

EDID data can be transferred between the source and sink devices using the CBUS. On the SiI9533 device, the CBUS signal pin is shared with the HPD signal pin. Another connection is used as the VBUS and provides +5 V power to charge the connected MHL source device. An external power switch is used on the system board to supply the +5 V power to the VBUS. Enabling the switch provides the +5 V of power on the VBUS when the MHL source is connected, and the MHL cable detect signal is asserted. The sink device can also supply power to the MHL source after MHL discovery and cable detect signal is done.

7.5. 3D Video Formats

The SiI9533 port processor supports the pass-through of 3D video modes described in the HDMI Specification. All modes support the following color formats:

- RGB 4:4:4
- YCbCr 4:4:4
- YCbCr 4:2:2 color formats

The modes also support 8-, 10-, and 12-bit data-width per color component. Table 7.3 on the next page shows only the maximum possible resolution with a given frame rate. For example, Side-by-Side (Half) mode is defined for 1080p @ 60 Hz, which infers that 720p @ 60 Hz and 480p @ 60 Hz are also supported. Further, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz means that a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

The SiI9533 device supports pass through of the HDMI Vendor-specific InfoFrame that carries 3D information to the receiver. It also supports extraction of the HDMI Vendor-specific InfoFrame, which allows the 3D information contained in the InfoFrame to be passed to the host system over the I^2C port.

Table 7.3. Supported 3D Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	50/60	297
Side-by-Side	full			
Line Alternative	—			
L+ Depth	—			
Frame Packing	—	1080p	24/30	148.35
		720p/1080i	50/60	
Side-by-Side	full	1080p	24/30	
		720p/1080i	30/50/60	
	half	1080p	50/60	
Top-and-Bottom	—	1080p	50/60	
		1080p	24/30	74.25
		720p/1080i	50/60	
Line Alternative	—	1080p	24/30	148.5
		720p/1080i	50/60	
Field Alternative	—	1080i	50/60	
L+ depth	—	1080p	24/30	
Frame Packing	—	720p	30	148.5
		480p/480i	60	54
		576p/576i	50	
		VGAp (640 x 1005)	60	50.35
Side-by-Side	full	480p	60	54
		576p/576i	50	
		2560 x 720p	24	118.6
		VGAp (1280 x 480)	60	50.35
	half	1080i/720p	50	74.25
		720p	60	
		1080p	24/30	74.17
		1080i	60	
		720p	30	
		480p/480i	60	27
		576p/576i	50	
		VGAp (640 x 480)	60	25.17
Top-and-Bottom	—	480p/480i	60	27
		576p/576i	50	
		720p	30	74.17
		720p	24	59.34
		VGAp (640 x 480)	60	25.17

8. Design Recommendations

8.1. Power Supply Decoupling

Designers should include decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 8.1. Connections in one group, such as AVDD33 can share C2, C3, and the ferrite, with each pin having a separate C1 placed as close to the pin as possible. Figure 8.2 is representative of the various types of power connections on the port processor.

The recommended impedance of the ferrite is 10 Ω or more in the frequency range of 1 MHz to 2 MHz.

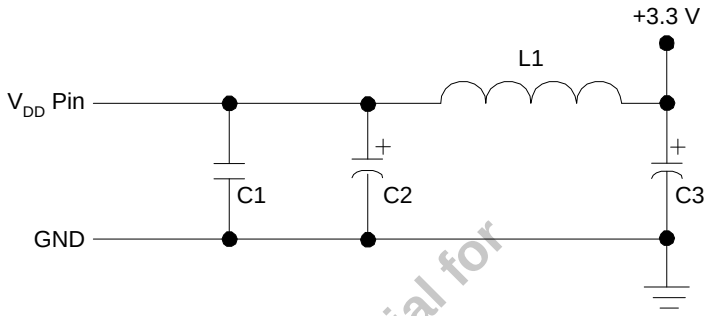


Figure 8.1. Decoupling and Bypass Schematic Diagram

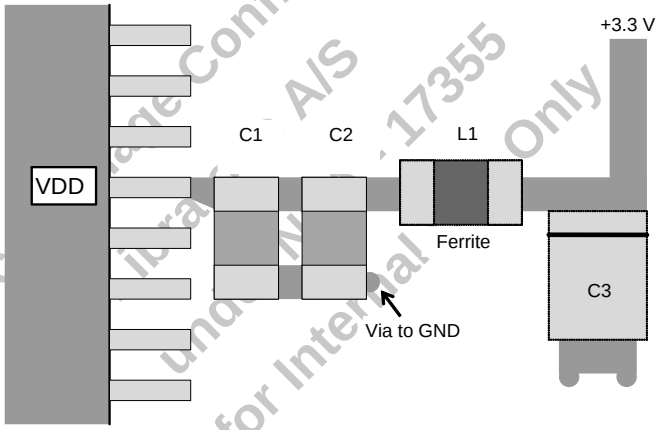


Figure 8.2. Decoupling and Bypass Capacitor Placement

8.2. Power Supply Control Timing and Sequencing

All power supplies in the SiI9533 port processor are independent. However, identical supplies must be provided at the same time. For example, both AVDD33 supplies must be turned on at the same time.

9. Package Information

9.1. ePad Requirements

The SiI9533 chip is packaged in an 88-pin, 10 mm × 10mm QFN package with an ePad that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 4.29 mm × 4.29 mm. Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full-speed operation, and to correctly connect the chip circuitry to electrical ground. A clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical short circuit.

The thermal land area on the PCB may use thermal vias to improve heat removal from the package. These thermal vias also double as the ground connections of the chip and must attach internally in the PCB to the ground plane. An array of vias should be designed into the PCB beneath the package. For optimum thermal performance, the via diameter should be 12 mils to 13 mils (0.30 mm to 0.33 mm) and the via barrel should be plated with 1-ounce copper to plug the via. This design helps avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be tented with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

Package stand-off when mounting the device also needs to be considered. For a nominal stand-off of approximately 0.1 mm, the stencil thickness of 5 mils to 8 mils should provide a good solder joint between the ePad and the thermal land.

Figure 9.1 on the next page shows the package dimensions of the SiI9533 port processor.

9.2. Package Dimensions

These drawings are not to scale. All dimensions are in millimeters.

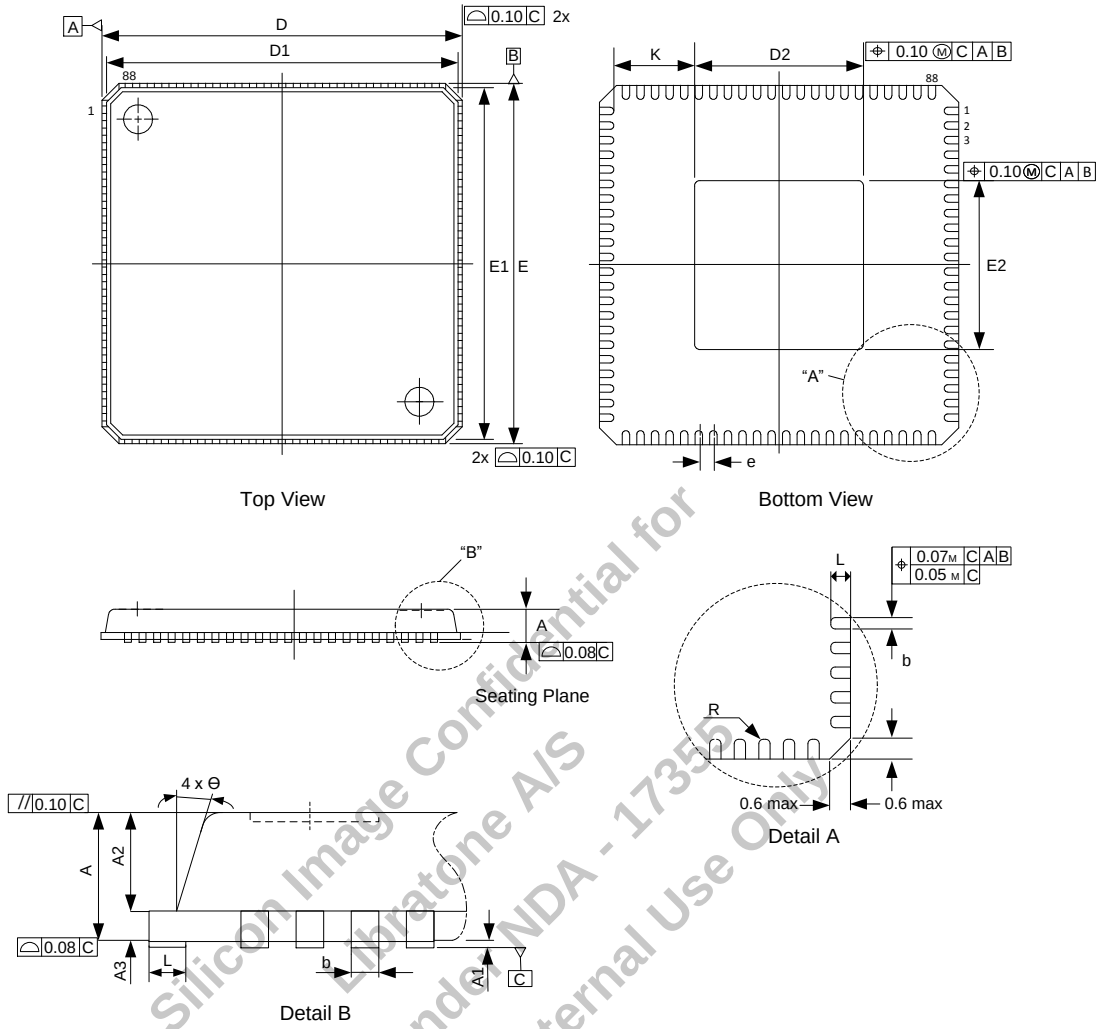


Figure 9.1. Package Diagram

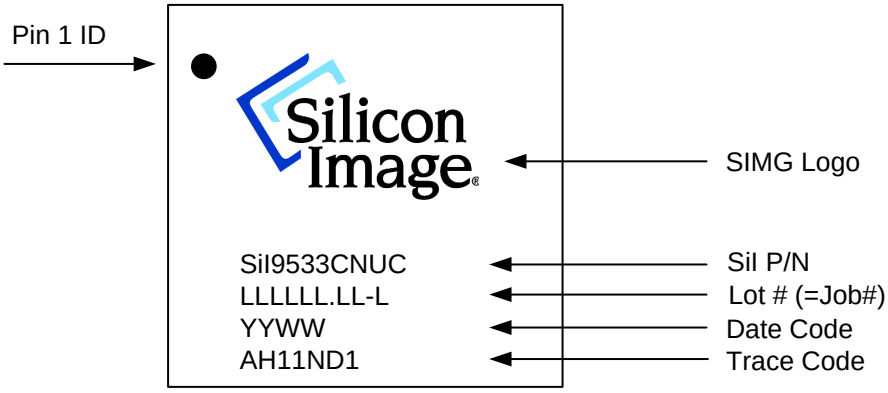
JEDEC Package Code M0-220

Item	Description	Min	Typ	Max
A	Thickness	0.80	0.85	0.90
A1	Stand-off	0.00	0.02	0.05
A2	Body thickness	0.60	0.65	0.70
A3	—		0.20 REF	
b	Lead width (with plating)	0.15	0.20	0.25
D/E	Footprint	9.90	10.00	10.10
D1/E1	Body size		9.75 BSC	
D2	—	4.14	4.29	4.44
E2	—	4.14	4.29	4.44
e	Lead pitch		0.40 BSC	

Item	Description	Min	Typ	Max
L	Lead foot length	0.30	0.40	0.50
Θ	—	0°	—	14°
R	—	0.075	—	—
K	—	0.20	—	—
aaa	—		0.10	
bbb	—		0.07	
ccc	—		0.10	
ddd	—		0.05	
eee	—		0.08	
fff	—		0.10	

9.3. Marking Specification

Figure 9.2 shows the markings of the SiI9533 package. This drawing is not to scale.



Trace code letter 'N' = SPIL Assembly site and copper wire

Figure 9.2. Marking Diagram

9.4. Ordering Information

Production Part Numbers:

Device	Part Number
Port Processor with InstaPort S, InstaPrevue, ARC, 300 MHz	SiI9533CNUC

References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards publication, organization, and date
HDMI	*High Definition Multimedia Interface*, Revision 2.0, HDMI Consortium; September 2013 *High Definition Multimedia Interface*, Revision 1.4b, HDMI Consortium; October 2011
HCTS	*HDMI Compliance Test Specification,* Revision 1.4b, HDMI Consortium; October 2011
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.4, Digital Content Protection, LLC; July 2009
DVI	*Digital Visual Interface,* Revision 1.0, Digital Display Working Group; April 1999
E-EDID	*Enhanced Extended Display Identification Data Standard,* Release A Revision 1, VESA; February 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
CEA-861-E	*A DTV Profile for Uncompressed High Speed Digital Interfaces,* EIA/CEA, March 2008
EDDC	*Enhanced Display Data Channel Standard,* Version 1.1, VESA; March 2004
MHL	*MHL (Mobile High-definition Link) Specification*, Version 2.0, MHL, LLC, February 2012

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—
MHL	http://www.mhlconsortium.org	customerservice@mhlconsortium.org	408-962-4269

Silicon Image Documents

This is a list of the related documents that are available from your Silicon Image sales representative.

Document	Title
SiI-PR-1074	*SiI9533 and SiI9535 Port Processor Programmer Reference*
SiI-UG-1118	*SiI9533 Port Processor Starter Kit User Guide*
SiI-QS-1118	*SiI9533 Port Processor Starter Kit Quick Start Guide*
SiI-AN-1079	*SiI9575-SiI9535 Firmware Comparison Application Note*

Revision History

Revision C, July 2014

Updated Audio Inputs and Outputs section.

Revision B, October 2013

Support for 4K @ 50/60 Hz added.

Revision A, September 2013

First production release.

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