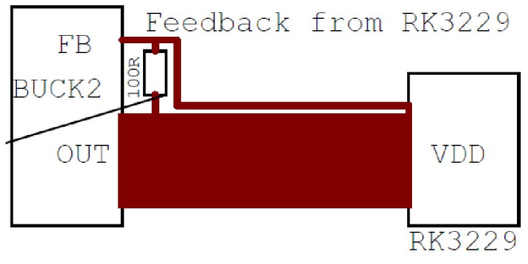
Feedback from RK3229

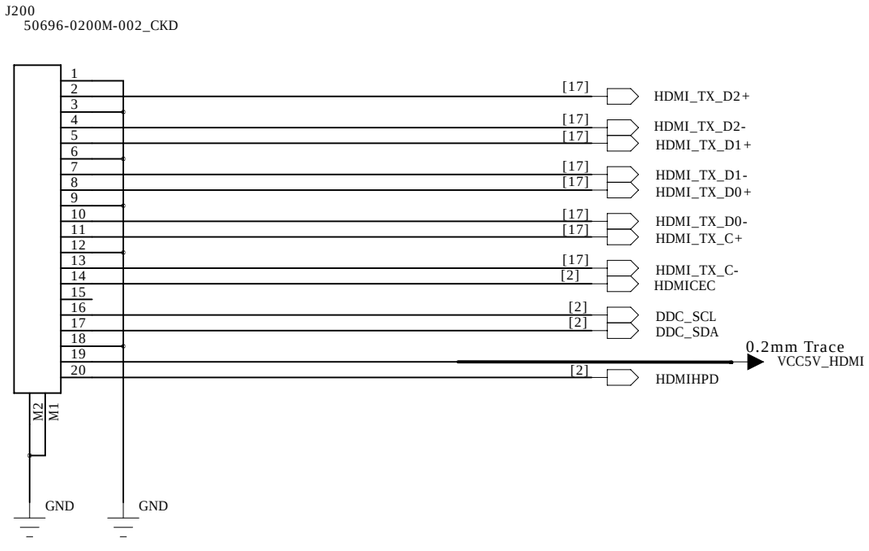
Power Input

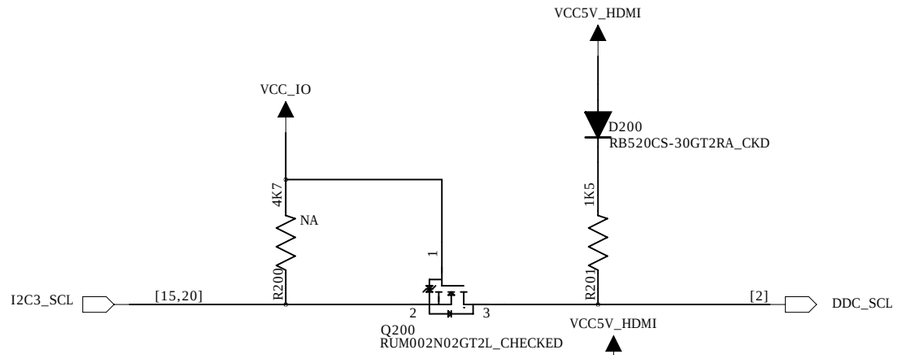
U101
RK805-1_CKD

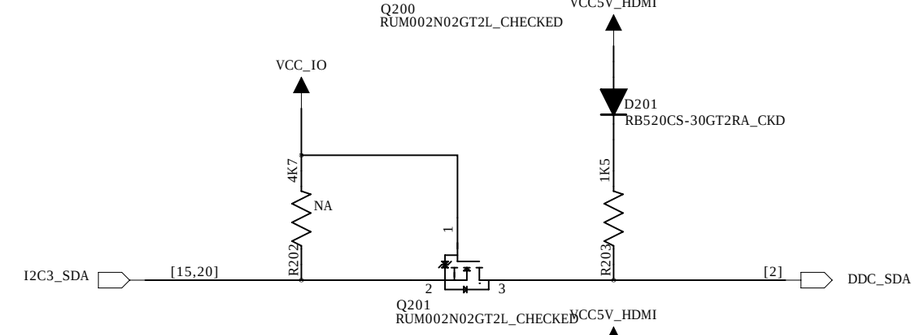
Feedback from RK3229

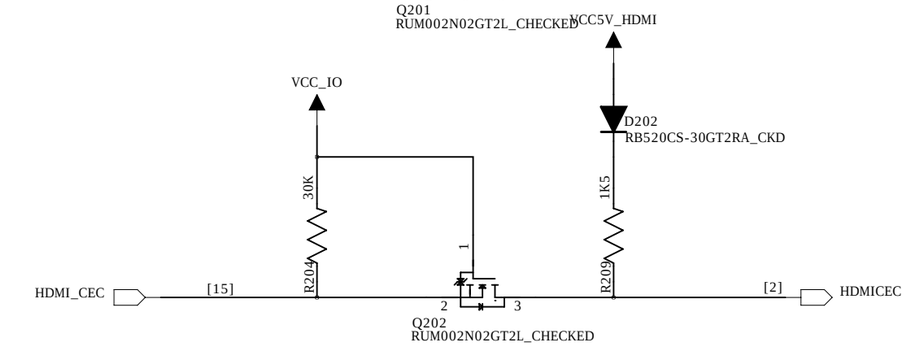


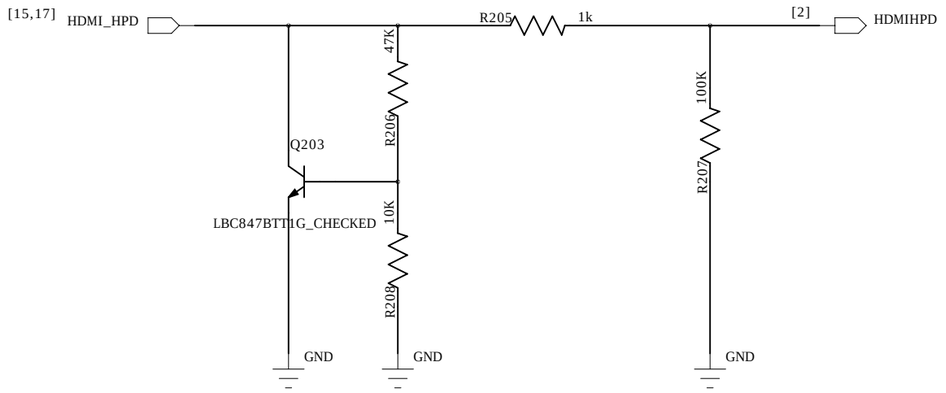
Libratone A/S	PROJECT NAME	Delta_N	
	DRAW NO	ES1	
	DESCRIPTION	WiFi/BT Module	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. R0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 1 OF 22











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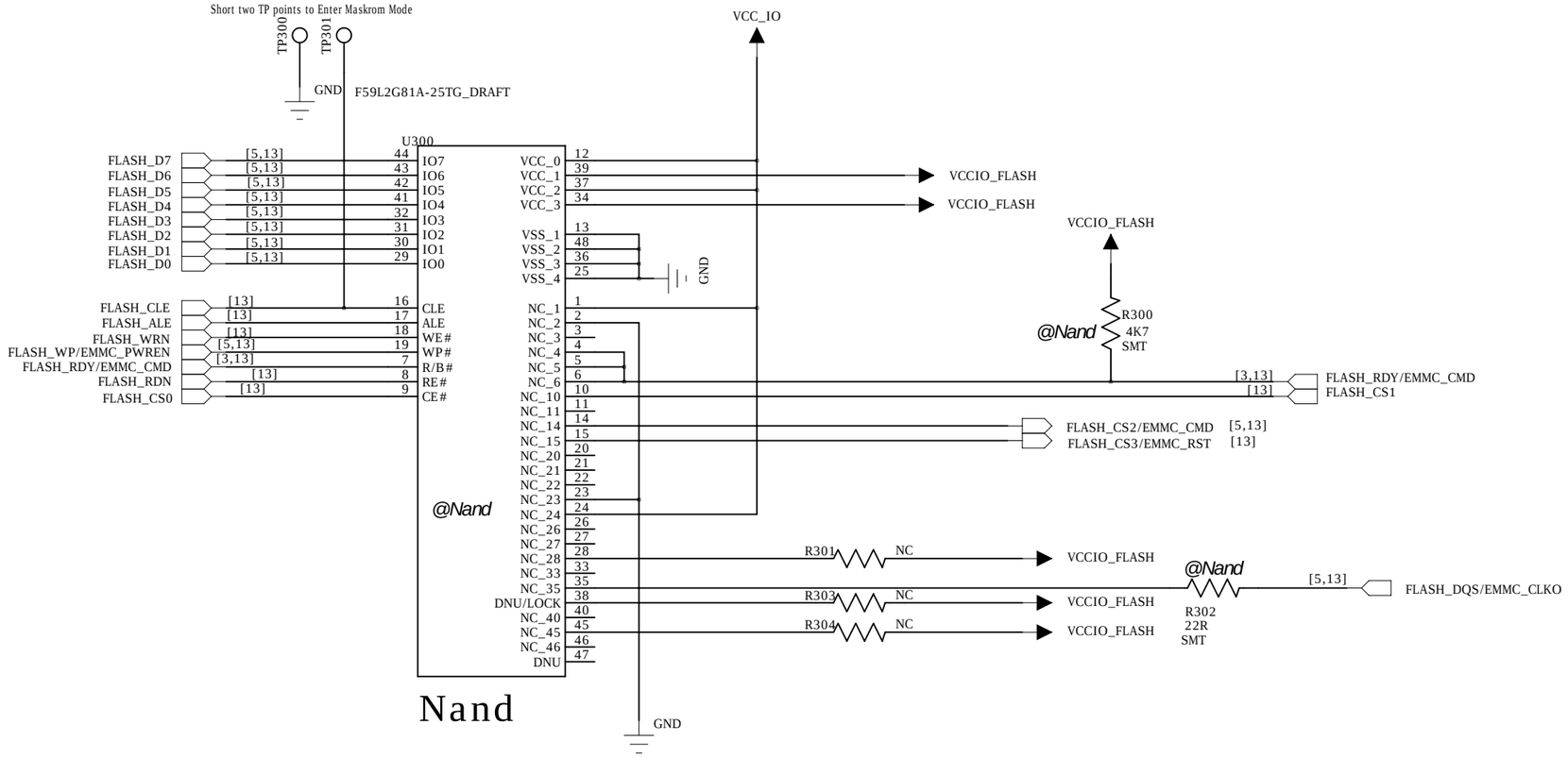
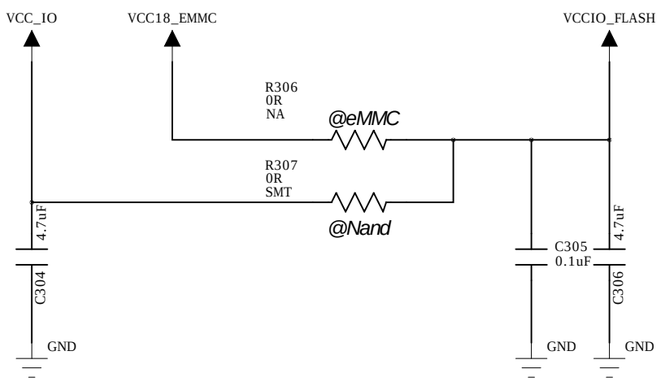
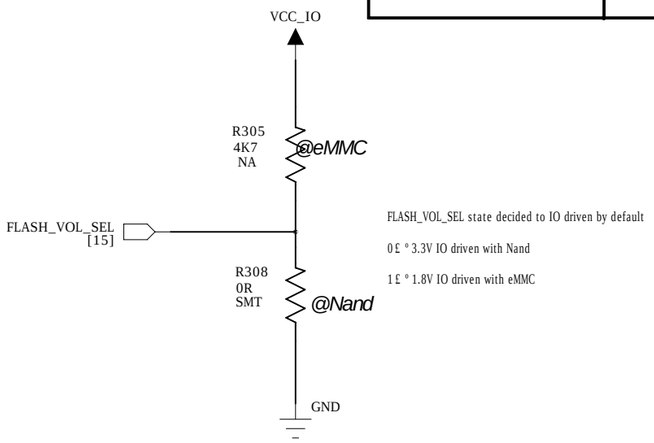


For Nand Flash + eMMC dual layout:The D0-D7 traces should pass through the pads of Nand Flash first,and then connect to eMMC.

Nand/eMMC Version SMT Option

eMMC Version	U500 R500-R502 C500-C505 R305 R306
Nand Version	U300 R300 R302 C300-C303 R307 R308





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APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. R0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 3 OF 22

U400

NT5CB64M16GP-EK_DRAFT

For 2 Die stack

U401

NT5CB64M16GP-EK_DRAFT

For 2 Die stack

VCC_DDR

C400 10uF, C401 0.1uF, C402 0.1uF, C403 0.1uF, C404 0.1uF, C405 0.1uF, C406 0.1uF, C407 0.1uF

GND

1 cap for 1 pin

C409 10uF, C410 0.1uF, C411 0.1uF, C412 0.1uF, C413 0.1uF, C414 0.1uF, C415 0.1uF, C416 0.1uF

1 chip for 1 pin

DDR_RST [4,12]

C408 47pF

C417 47pF

MDDR3_VREF0

Short,Wide 1mm,GND Shielded

R401 240R

R400 240R

R407 240R

R404 240R

DDR_CS0N, DDR_RASN, DDR_CASN, DDR_WEN, DDR_ODT0, DDR_CLKN, DDR_CLK, DDR_CKE0, DDR_BA0, DDR_BA1, DDR_BA2

DDR_A0 … DDR_A15

DQU7 … DQU0, DMU, DQSU, DQSU

DDR_D23, DDR_D18, DDR_D19, DDR_D17, DDR_D22, DDR_D21, DDR_D20, DDR_D16, DDR_DM2, DDR_DQS2M, DDR_DQS2P

Diff,100Ohm

DQL7 … DQL0, DML, DQSL, DQSL

DDR_D2, DDR_D7, DDR_D1, DDR_D5, DDR_D3, DDR_D0, DDR_D4, DDR_D6, DDR_DM0, DDR_DQS0M, DDR_DQS0P

Diff,100Ohm

NC/CS1, NC/CKE1, NC/ODT1, NC/ZQ1

DDR_CS1N, DDR_CKE0, DDR_ODT1

DDR_D29, DDR_D30, DDR_D27, DDR_D28, DDR_D31, DDR_D26, DDR_D25, DDR_D24, DDR_DM3, DDR_DQS3M, DDR_DQS3P

Diff,100Ohm

DDR_D8, DDR_D14, DDR_D10, DDR_D12, DDR_D9, DDR_D15, DDR_D13, DDR_D11, DDR_DM1, DDR_DQS1M, DDR_DQS1P

Diff,100Ohm

DDR_CLKN [4,12] 49R9 R405

DDR_CLK [4,12] 49R9 R406

C423 100pF

VCC_DDR

MDDR3_VREF0

1K R402

1K R403

C418 1000pF, C419 1000pF, C420 1000pF, C421 1000pF, C422 1000pF

SE Trace: 0.1mm width/0.15mm space,50 ohm SE
DIFF Trace: 0.1mm width/0.2mm space,100 ohm DIFF

Data Group
1.DQS diff pair < 0.2mm
2.DQx and DQMx < DQS +/- 2mm

Address/Cmd Group
1.CK diff pair < 0.2mm,GND shielded
2.DQSx < CK - 20mm
3.Addr/Cmd < CK +/- 7.5mm, short branch, match branch < 7.5mm

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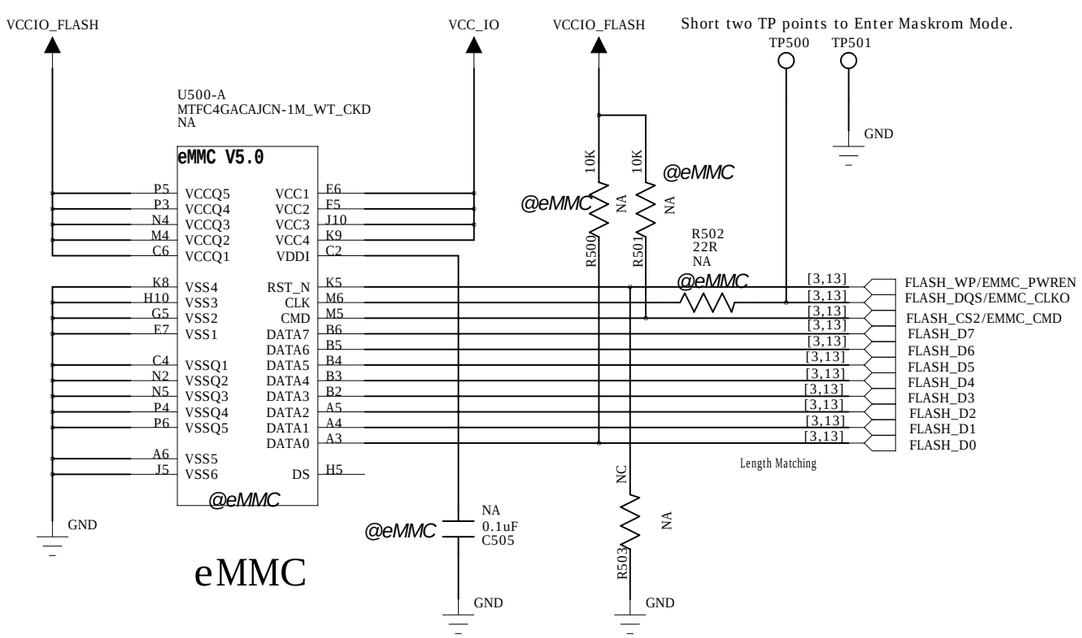
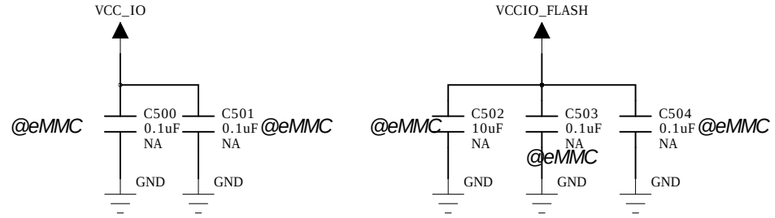
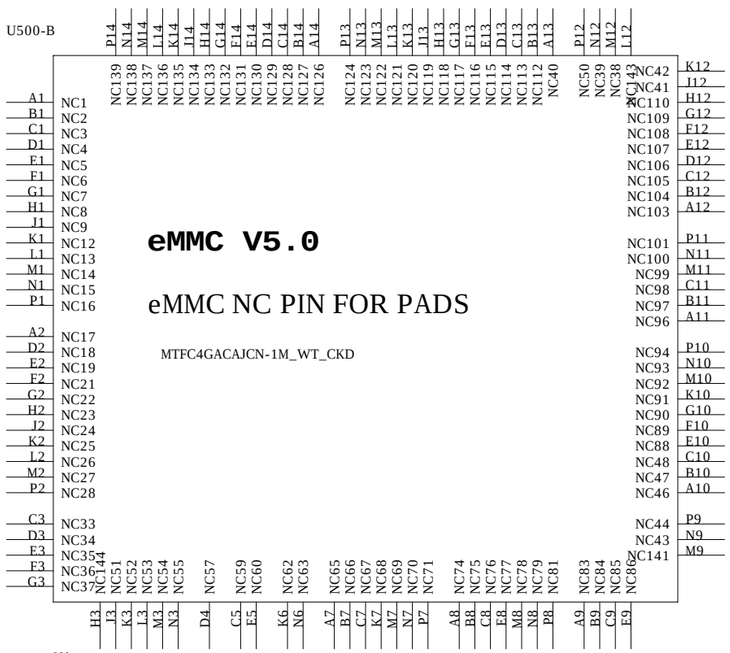
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 4 OF 22







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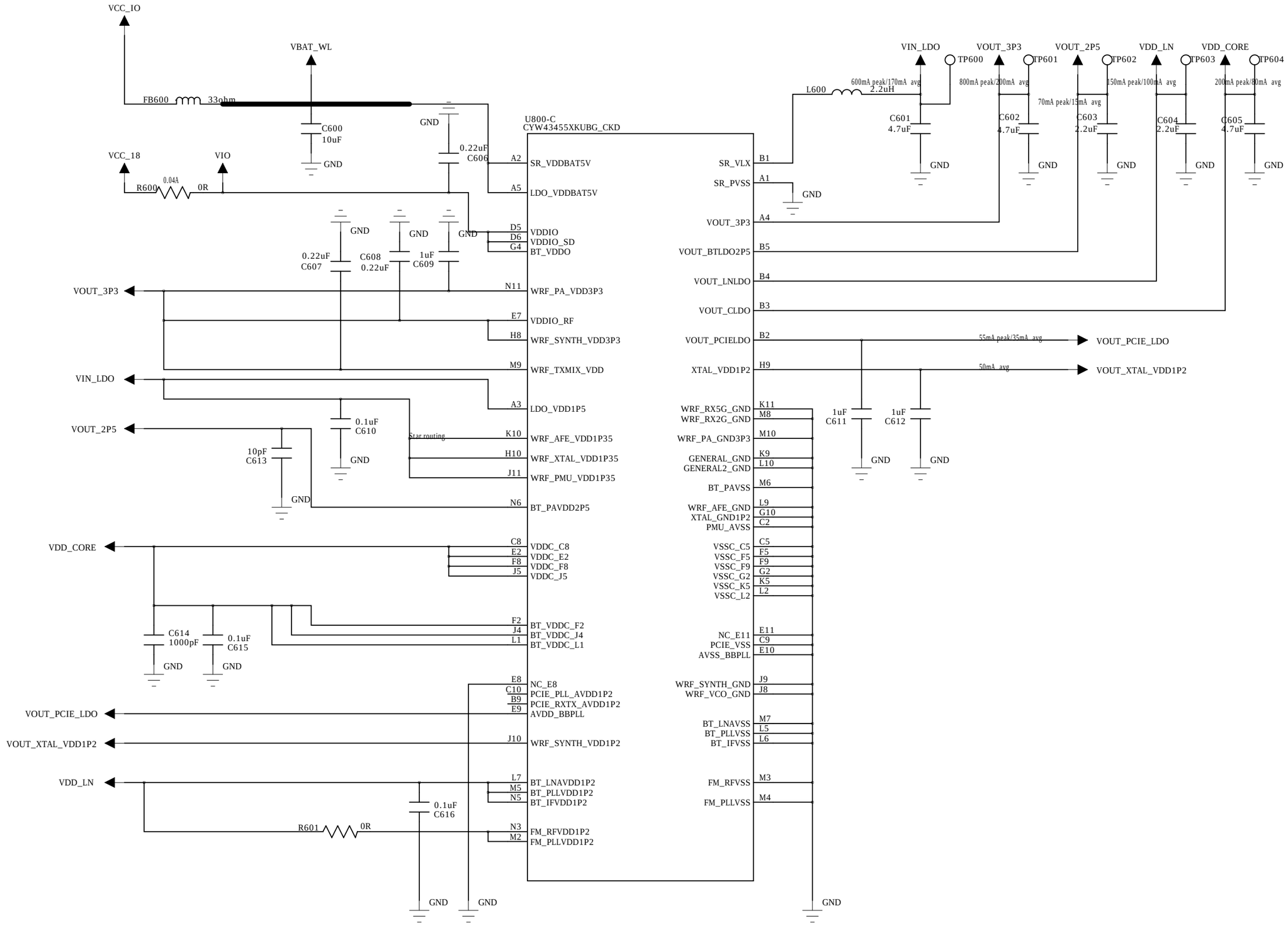

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		DESCRIPTION	WiFi/BT Module
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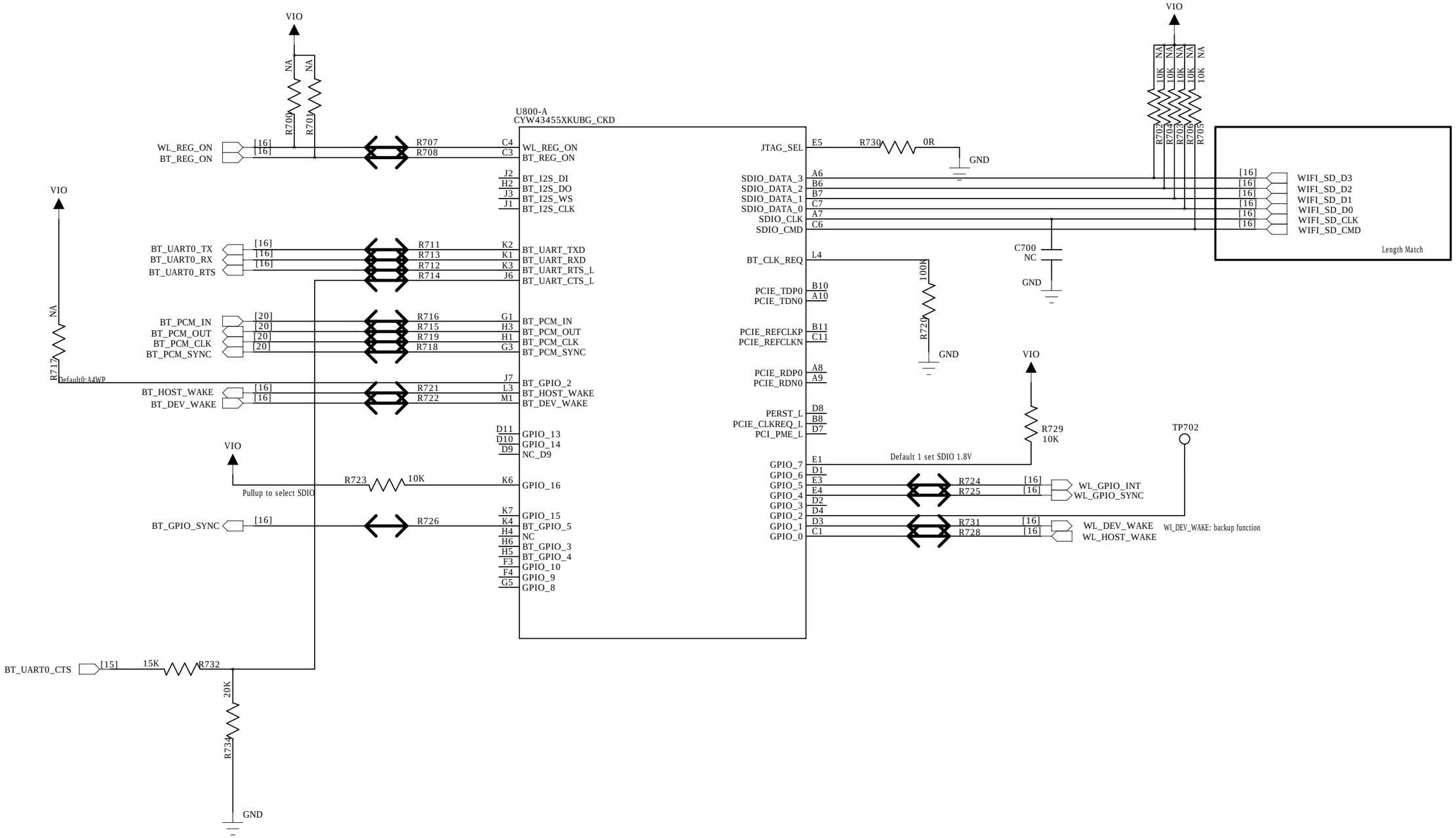
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 6 OF 22



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	DESCRIPTION	WiFi/BT Module	
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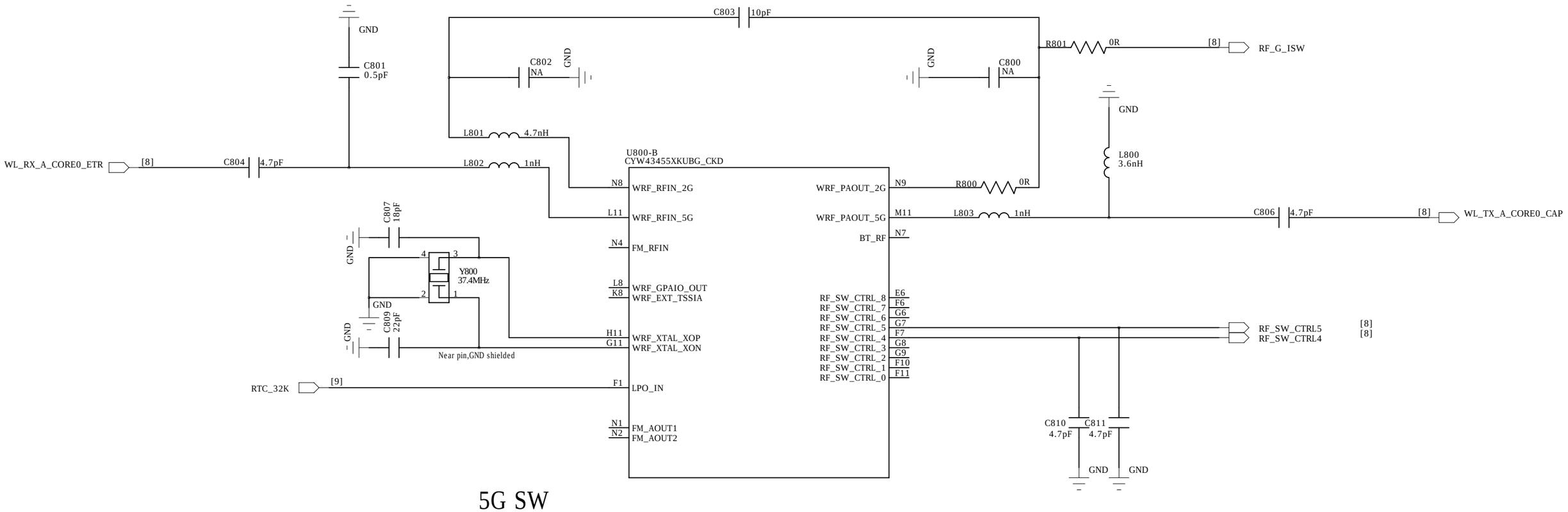
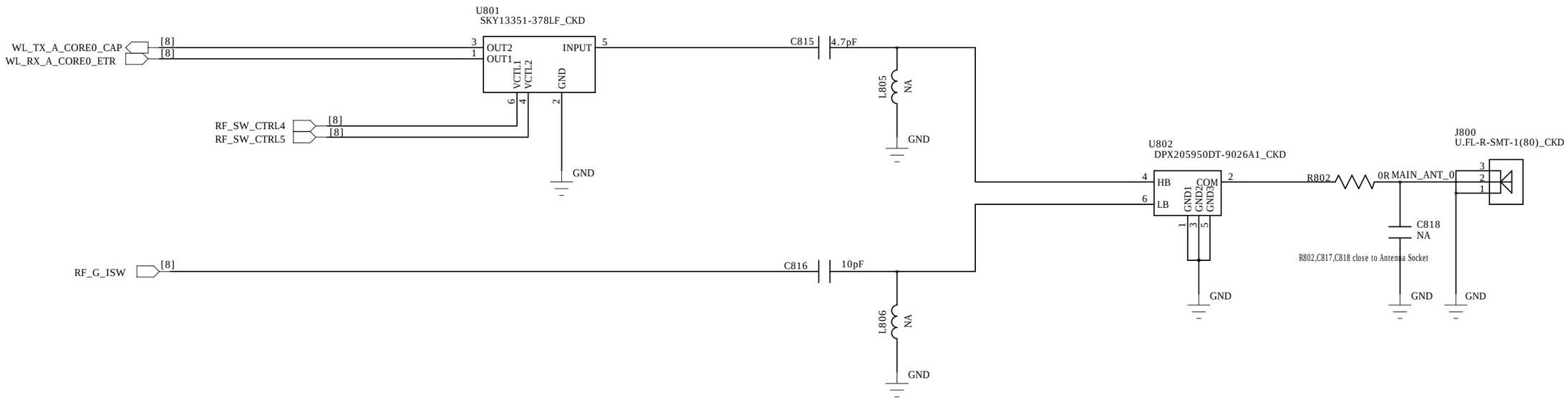


5G SW



A-Band RF T/R Switch Truth Table

	RF_SW_CTRL4	RF_SW_CTRL5
WLAN_TX	H	L
WLAN_RX	L	H

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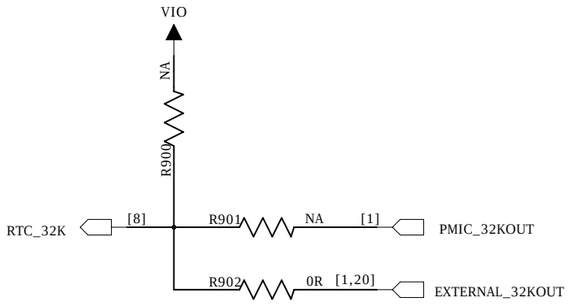

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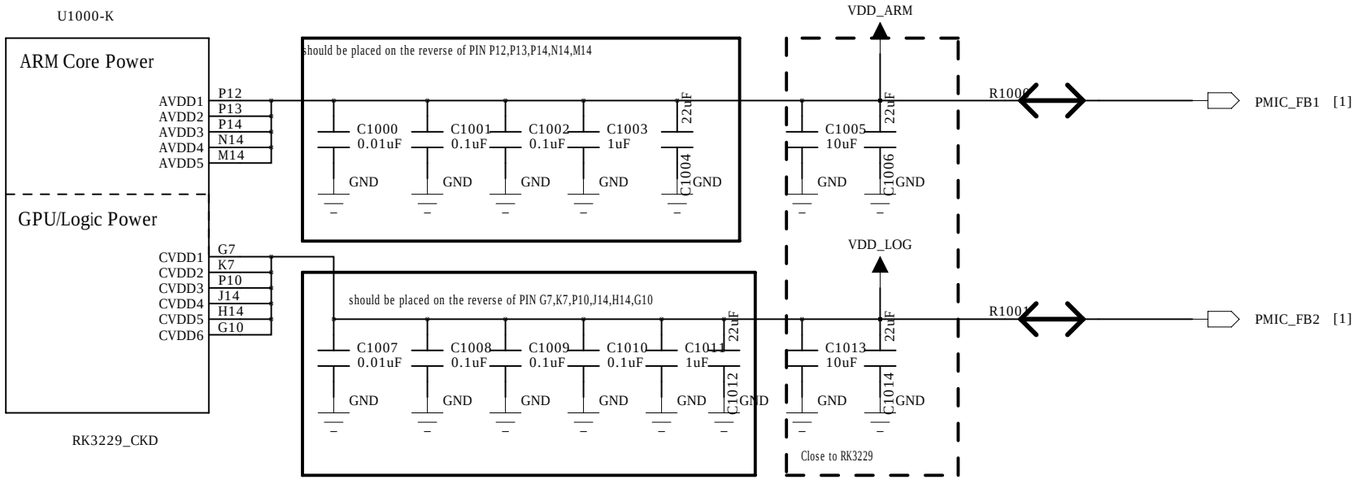

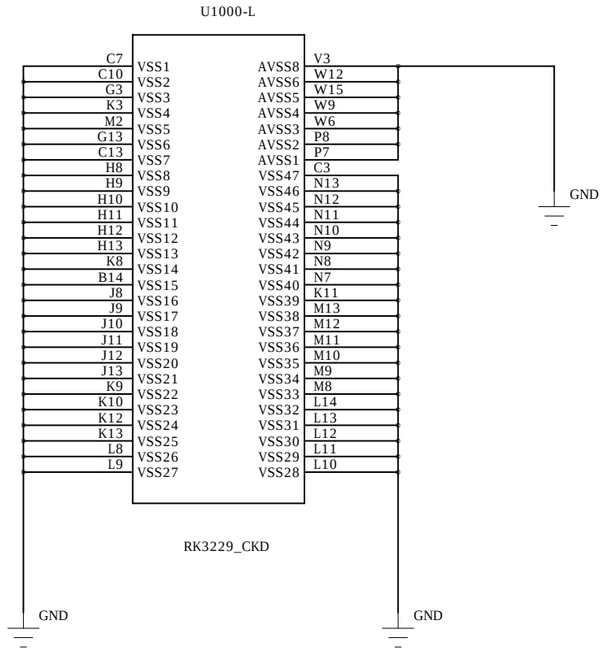

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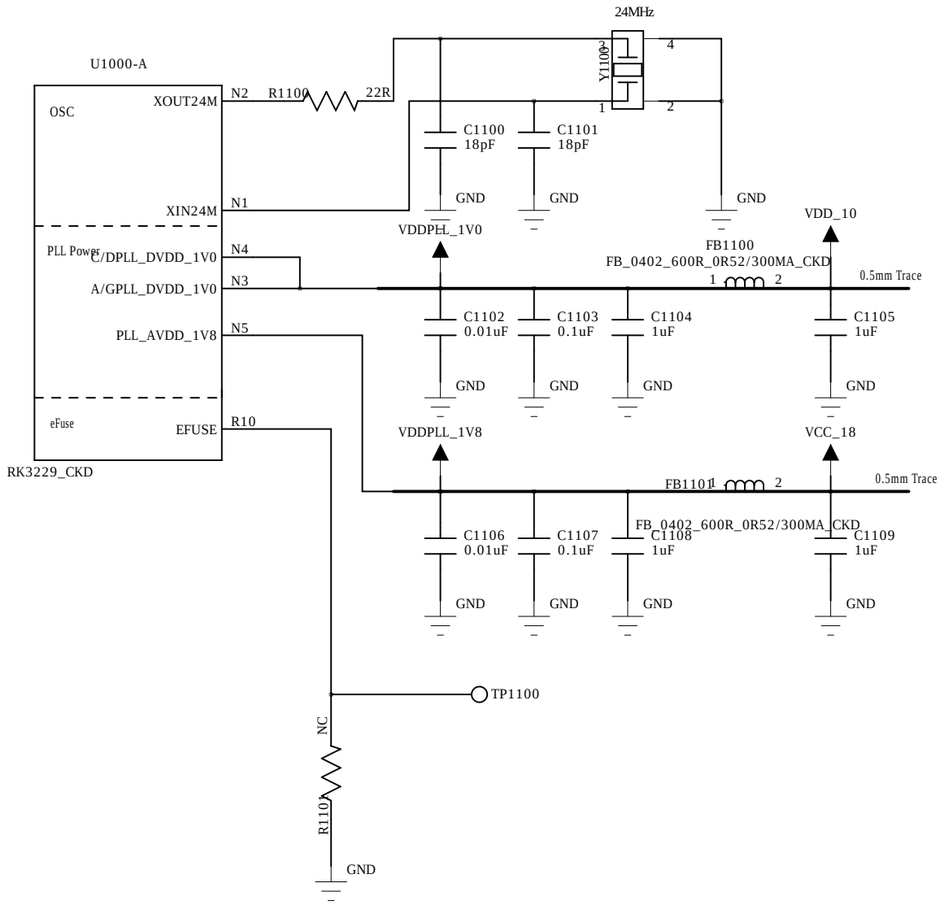

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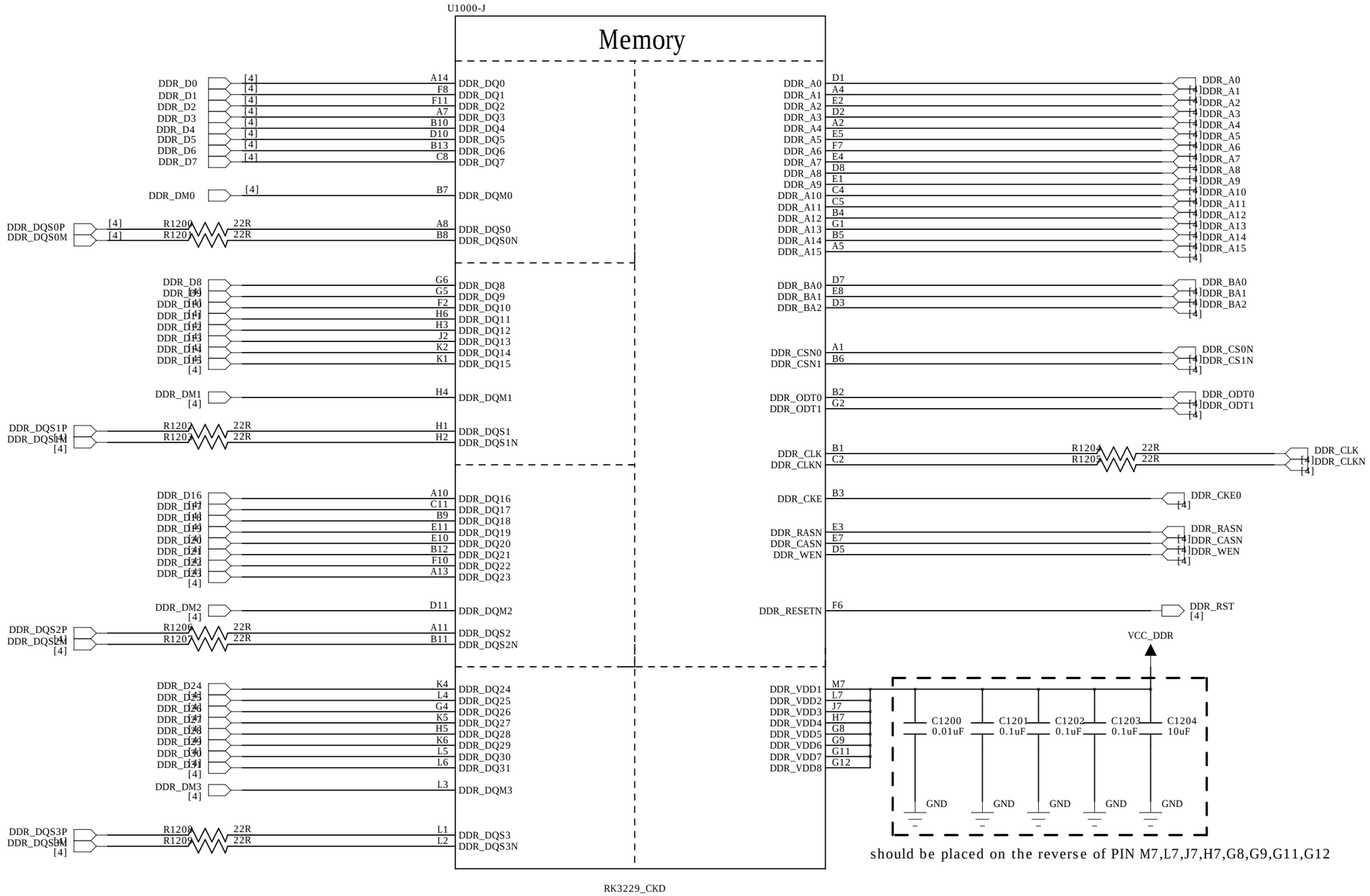

RK3229_CKD

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DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 12 OF 22

U1000-D

Nand Flash/eMMC/SPI

GPIO2_A5/FLASH_WP/EMMC_PWR_D	V19	FLASH_WP/EMMC_PWREN	[3,5]
GPIO1_C6/FLASH_CS2/EMMC_CMD_U	U19	FLASH_CS2/EMMC_CMD	[3,5]
GPIO1_C7/FLASH_CS3/EMMC_RST_U	P19	FLASH_CS3/EMMC_RST	[3]
GPIO1_D0/FLASH_D0/EMMC_D0_U	P16	FLASH_D0	[3,5]
GPIO1_D1/FLASH_D1/EMMC_D1_U	U20	FLASH_D1	[3,5]
GPIO1_D2/FLASH_D2/EMMC_D2_U	T19	FLASH_D2	[3,5]
GPIO1_D3/FLASH_D3/EMMC_D3_U	T20	FLASH_D3	[3,5]
GPIO1_D4/FLASH_D4/EMMC_D4_U	P18	FLASH_D4	[3,5]
GPIO1_D5/FLASH_D5/EMMC_D5_U	R19	FLASH_D5	[3,5]
GPIO1_D6/FLASH_D6/EMMC_D6_U	N15	FLASH_D6	[3,5]
GPIO1_D7/FLASH_D7/EMMC_D7_U	P17	FLASH_D7	[3,5]
GPIO2_A0/FLASH_ALE/SPI_RXD_D	N16	FLASH_ALE	[3]
GPIO2_A1/FLASH_CLE/SPI_TXD_D	N17	FLASH_CLE	[3]
GPIO2_A2/FLASH_WRN/SPI_CSN0_U	P20	FLASH_WRN	[3]
GPIO2_A3/FLASH_RDN/SPI_CSN1_U	L15	FLASH_RDN	[3]
GPIO2_A4/FLASH_RDY/EMMC_CMD_U	K17	FLASH_RDY/EMMC_CMD	[3]
GPIO2_A6/FLASH_CS0_U	L16	FLASH_CS0	[3]
GPIO2_A7/FLASH_DQS/EMMC_CLKO_U	N19	FLASH_DQS/EMMC_CLKO	[3,5]
GPIO0_C7/FLASH_CS1/SPI_CLK_U	L17	FLASH_CS1	[3]
VCCIO3	K14		

RK3229_CKD

VCCIO_FLASH

C1300
0.1uF

GND

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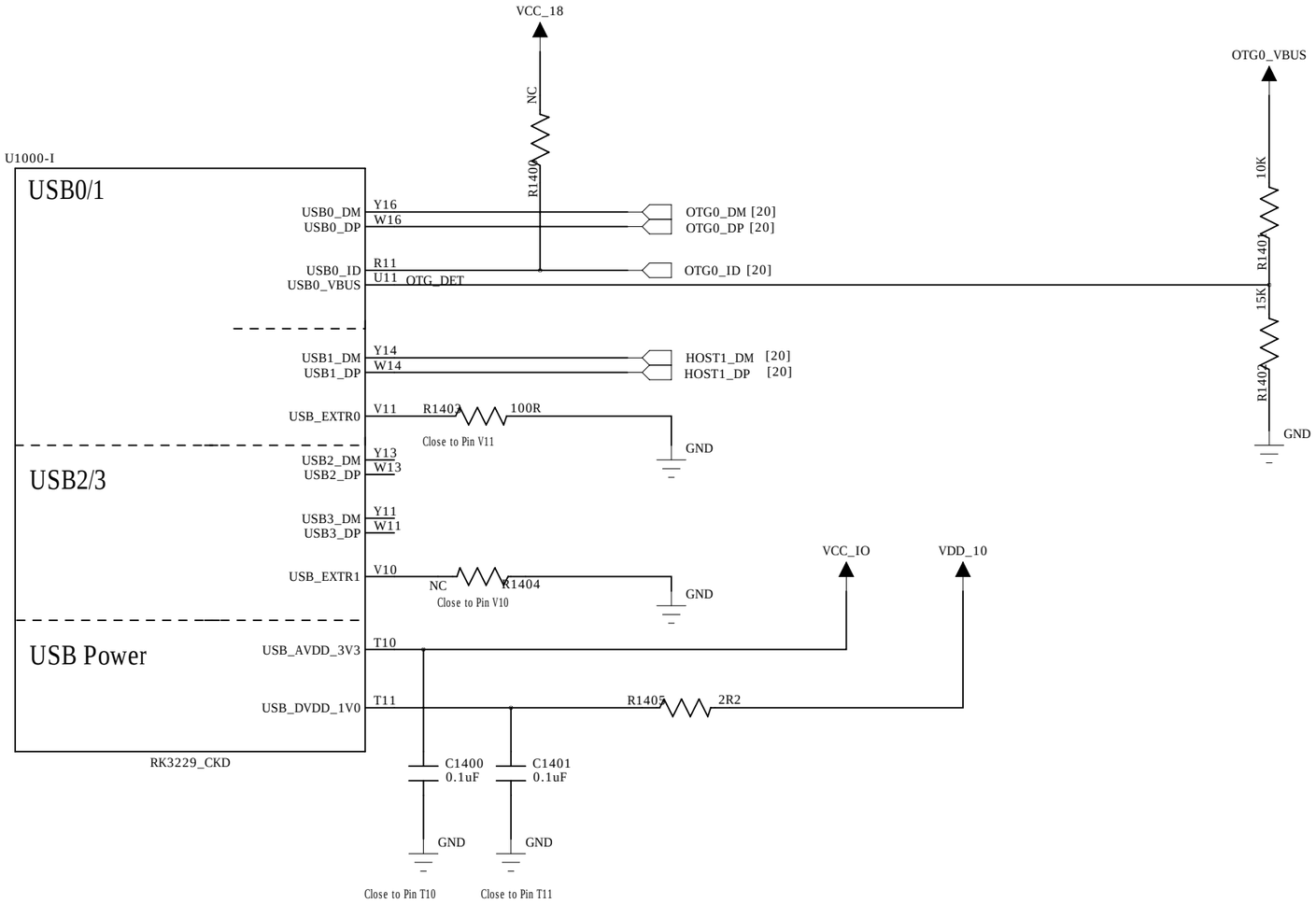

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DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 14 OF 22

U1000-E

TP1501: pull down to GND to into u-boot mode

SDMMC0/I2S/I2C/SPI/UART/GPIO

TP1500 TP1501

H15 TEST_D — GND

SOC_RST [1,20] — N20 NPOR_U — Close to Pin N20 — C1500 0.1uF — GND

P9 NC9

FLASH_VOL_SEL [3] — P11 GPIO3_D4_D

GPIO3_D1/SYS_RECOVERY [20] — U10 GPIO3_D1_U — Close to Pin U10 — C1501 0.1uF — GND

GPIO1_B6/SDMMC0_PWR_D — N18 — GPIO1_B6/SD_PWR

GPIO1_C5/SDMMC0_D3/JTAG_TMS_U — M19 — SD_D3 [20]
GPIO1_C4/SDMMC0_D2/JTAG_TCK_U — K16 — SD_D2 [20]

Pin function change,2017/12/08

GPIO1_C3/SDMMC0_D1/UART2_RX_U — K15 — [20]
GPIO1_C2/SDMMC0_D0/UART2_TX_U — L18 — [20]

UART2_DEBUG_RX
UART2_DEBUG_TX

Sys Debug

GPIO0_B6/I2S0_SDI/SPI_CSN0_U — K19 — I2S0_SDI [20]
GPIO0_B5/I2S0_SDO/SPI_RXD_U — L20 — I2S0_SDO [20]
GPIO0_B4/I2S0_LRCK_TX_U — H16 — I2S0_LRCK [20]
GPIO0_B3/I2S0_LRCK_RX/SPI_TXD_U — J19 R1500 0R
GPIO0_B1/I2S0_SCLK/SPI_CLK_U — K20 — I2S0_BCLK [20]
GPIO0_B0/I2S0_MCLK_U — H17 — I2S0_MCLK [20]

GPIO1_A7/SDMMC0_WP_D — L19 R1501 — LEVEL_CTRL [16]

GPIO0_D6/SDMMC1_PWR/PWM1_D — A20 — SOC_SLEEP [1]

GPIO1_C0/SDMMC0_CLKO_D — H20 — SD_CLK [20]
GPIO1_B7/SDMMC0_CMD_U — D18 — SD_CMD [20]

GPIO1_B3/UART1_RTSN/IR_U — G18 — IR_RX [20]

Pin function change,2017/12/08

GPIO1_B2/UART1_RX/UART2_RX_U — H19 — UART1_SOC_RX [20]
GPIO1_B1/UART1_TX/UART2_TX_U — H18 — UART1_SOC_TX [20]

For MCU

GPIO1_B0/UART1_CTSN/32K_OUT_U — G19 — GPIO1_B0 [20]

GPIO1_A5/SDMMC1_D3/I2S0_SDIO3_U — G17 — I2S0_SDIO3 [20]
GPIO1_A4/SDMMC1_D2/I2S0_SDIO2_U — G16 — I2S0_SDIO2 [20]

GPIO1_A3_D — G15 — GPIO1_A3 [20]

GPIO1_A2/SDMMC1_D1/I2S0_SDIO1_U — E19 — I2S0_SDIO1 [20]

GPIO1_A1/SDMMC1_D0_U — E18
GPIO1_A0/SDMMC1_CLKO_D — E20

Pin function change,2017/12/08

GPIO0_C1/UART0_RTSN/CLK_OUT1_U — P15 — BT_UART0_CTS [7]

GPIO0_A3/I2C1_SDA/SDMMC1_CMD_U — D17 — I2C1_SDA [20]
GPIO0_A2/I2C1_SCL_U — F19 — I2C1_SCL [20]

GPIO0_A1/I2C0_SDA_U — E17 — I2C0_SDA [1,20]
GPIO0_A0/I2C0_SCL_U — D20 — I2C0_SCL [1,20]

GPIO1_B4/SPI_CSN1/PWM2_U — B19 — PMIC_INT_SOC [1]

GPIO0_D1/UART2_CTSN/EFUSE_PWREN_U — A19 — HDMI_PWR_EN [17]

GPIO0_D0/UART2_RTSN/OTP_U — C17 — GPIO0_D0_OTP [20]

GPIO0_C4/HDMI_CEC_U — C19 — HDMI_CEC [2]

GPIO0_A7/HDMI_SDA/I2C3_SDA_U — F14 — I2C3_SDA [2,20]
GPIO0_A6/HDMI_SCL/I2C3_SCL_U — B20 — I2C3_SCL [2,20]
GPIO0_B7/HDMI_HPD_D — E13 — HDMI_HPD [2,17]

GPIO3_D7/TEST_CLKO/SPDIF_D — K18 R1503 0R — SOC_SPDIF_OUT [20]

GPIO3_C7_U — G20 — GPIO3_C7 [20]
GPIO3_C6/DRIVE_VBUS_D — C18
GPIO3_C5/PWM0_D — F13 — PWM0_D [20]
GPIO3_C4_D — D19

VCC_IO

VCCIO4 — G14 — Close to Pin G14 — C1502 0.1uF — GND

RK3229_CKD

Libratone A/S	PROJECT NAME	Delta_N	
LIBRATONE	DRAW NO	ES1	
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DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 15 OF 22

U1000-C

SDMMC1/UART1/PCM/GPIO

GPIO3_A0/SDMMC1_CLKO_D	U17	WIFI_SD_CLK [7]
GPIO3_A1/SDMMC1_CMD_U	V17	WIFI_SD_CMD [7]
GPIO3_A2/SDMMC1_D0_U	W17	WIFI_SD_D0 [7]
GPIO3_A3/SDMMC1_D1_U	V16	WIFI_SD_D1 [7]
GPIO3_A4/SDMMC1_D2_U	T13	WIFI_SD_D2 [7]
GPIO3_A5/SDMMC1_D3_U	R13	WIFI_SD_D3 [7]
GPIO3_A6/UART1_RTSN_D	R14	BT_REG_ON [7]
GPIO3_A7/UART1_CTSN_D	T16	WL_REG_ON [7]
GPIO3_B4/PCM_SYNC_D	U13	I2S_LRCK [16]
GPIO3_B5/UART1_RX_D	V18	BT_GPIO_SYNC [7]
GPIO3_B6/UART1_TX_D	U16	
GPIO3_B7/CLK_OUT0_D	V13	WL_GPIO_INT [7]
GPIO3_B3/PCM_CLK_D	Y20	I2S_BCLK [16]
GPIO3_C1/DRIVE_VBUS_D	U14	WL_GPIO_SYNC [7]
GPIO0_D2/PWM0/PCM_RX_D	U18	I2S_SDI [16]
GPIO0_D3/PWM1/PCM_TX_D	T17	I2S_SDO [16]
GPIO0_D4/PWM2_U	V14	WL_HOST_WAKE [7]
GPIO1_C1/SDMMC0_DET_U	W19	WL_DEV_WAKE [7]
GPIO2_D5/UART0_CTSN_D	W20	BT_UART0_RTS [7]
GPIO2_D3/UART0_RX_D	Y17	BT_UART0_TX [7]
GPIO2_D2/UART0_TX_D	T18	BT_UART0_RX [7]
GPIO3_D3/SPDIF_U	Y19	BT_DEV_WAKE [7]
GPIO3_D2/IR_U	W18	BT_HOST_WAKE [7]
VCCIO2	T14	

R1600 0R

Pin function change,2017/12/08

Pin function change,2017/12/08

To WIFI

Pin function change,2017/12/08

Close to Pin T14

C1602 0.1uF

GND

VCCIO_WL

RK3229_CKD

VCC_18

VCCIO_WL

R1609 0R

VCCIO_WL

VCC_IO

C1600 0.1uF

GND

C1601 0.1uF

GND

U1601

[15]	LEVEL_CTRL	8	OE		
[16]	I2S_BCLK	R1606 0R	2	A1	B1 13 [20] I2S2_BCLK
[16]	I2S_LRCK	R1607 0R	3	A2	B2 12 [20] I2S2_LRCK
[16]	I2S_SDI	R1608 0R	4	A3	B3 11 [20] I2S2_SDI
[16]	I2S_SDO	R1609 0R	5	A4	B4 10 [20] I2S2_SDO
			1	VCCA	
			14	VCCB	
			6	NC0	
			9	NC1	
			7	GND	
			15	THERMAL	

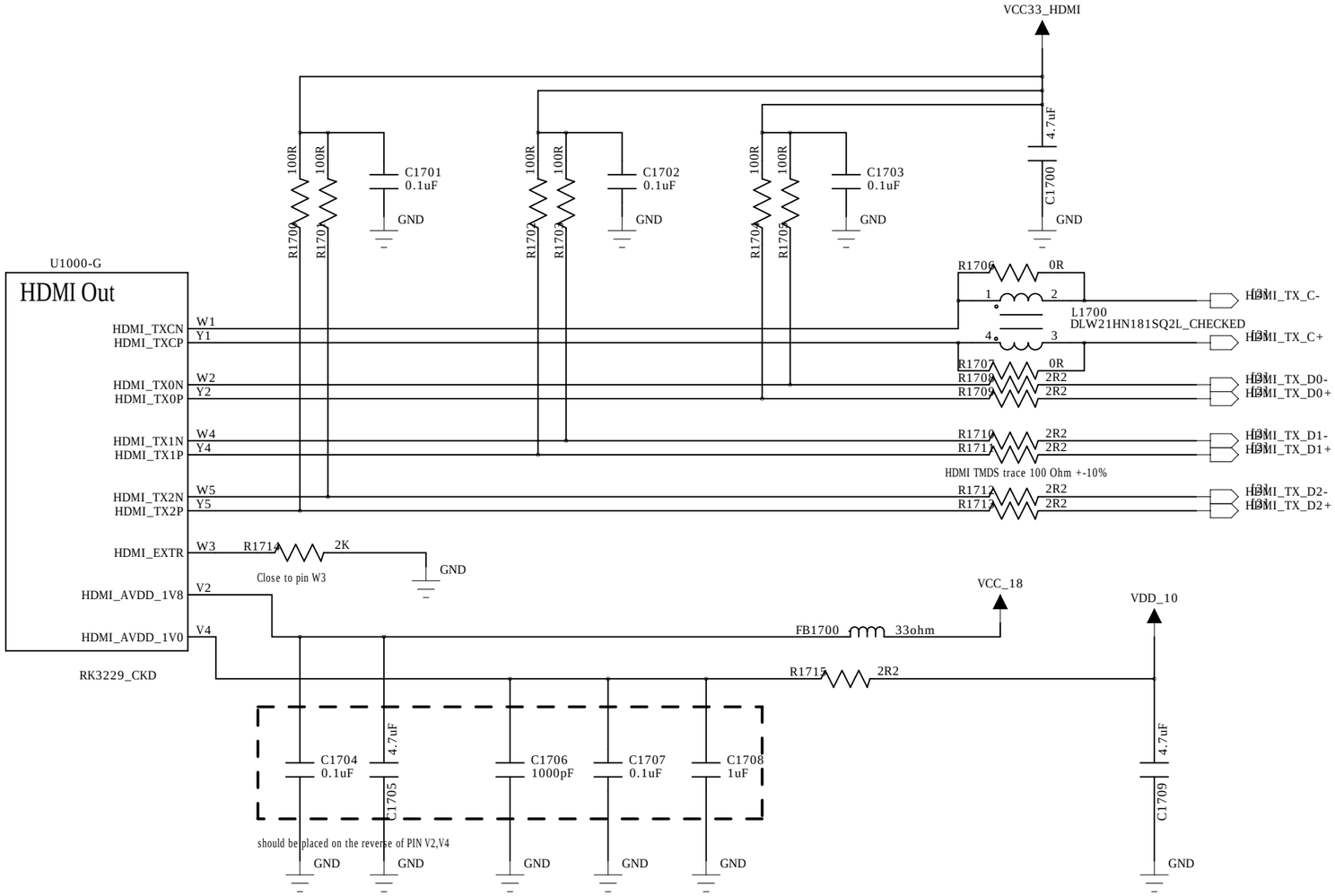
TXB0104RGYR_CKD

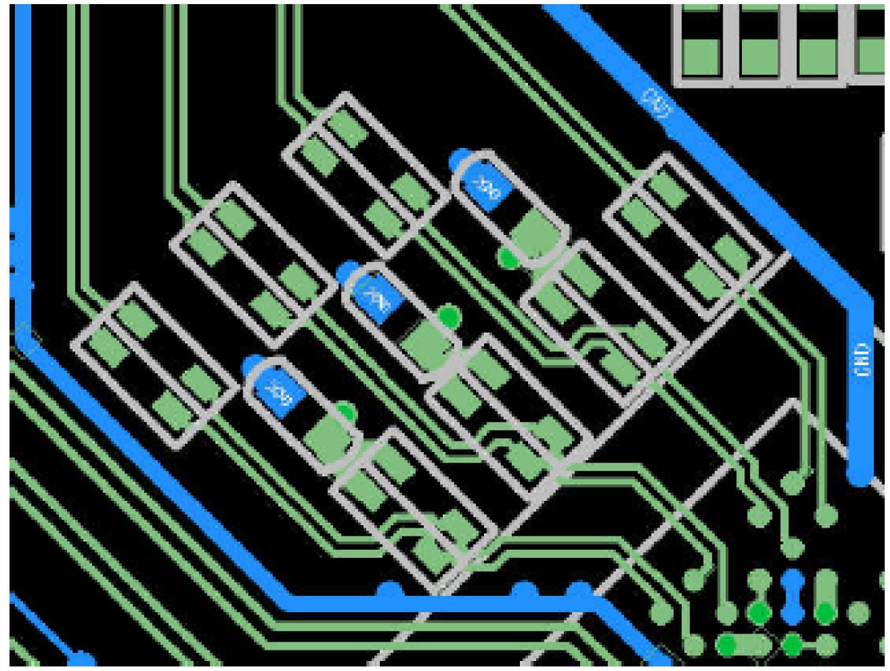
47K R1610

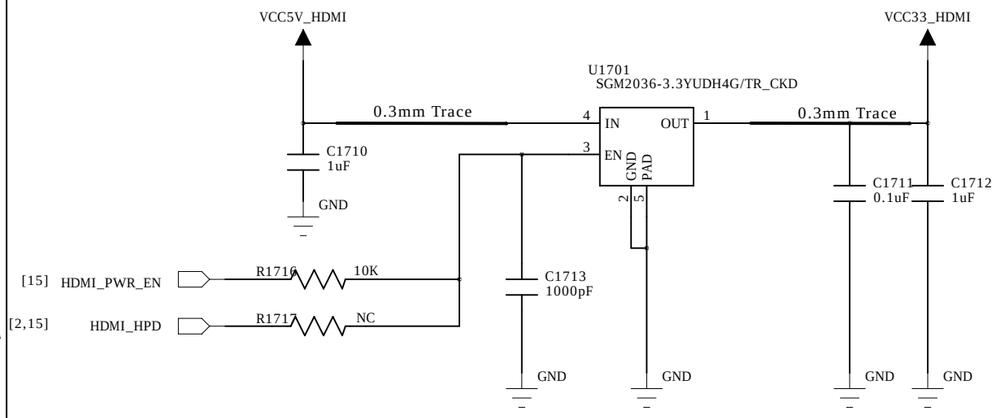
GND

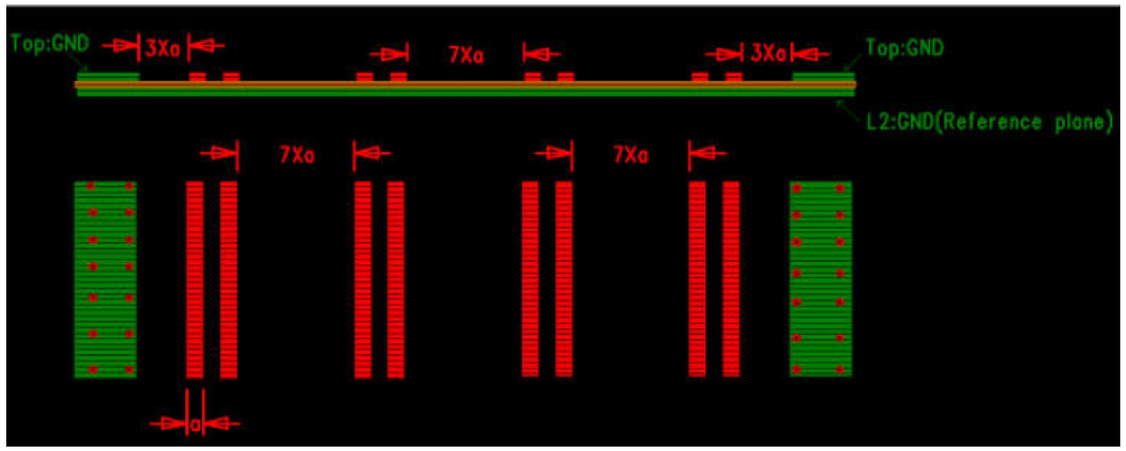
GND

Libratone A/S	PROJECT NAME	Delta_N	
	DRAW NO	ES1	
LIBRATONE	DESCRIPTION	WiFi/BT Module	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. R0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 16 OF 22









Libratone A/S		PROJECT NAME	Delta_N
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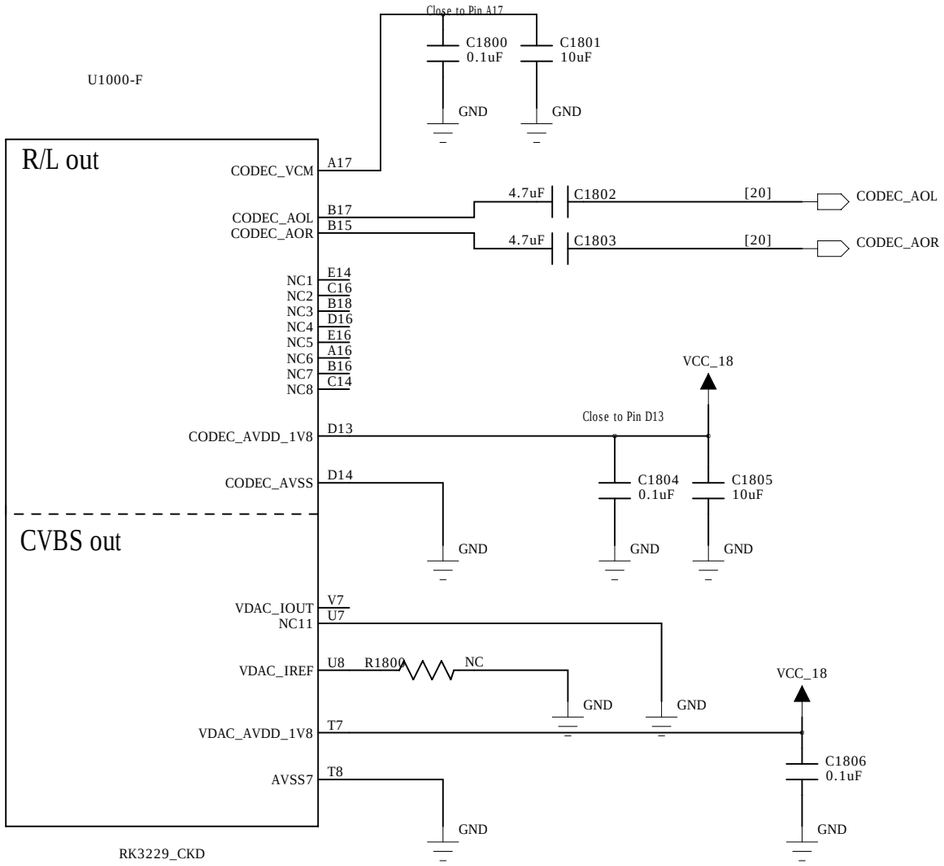

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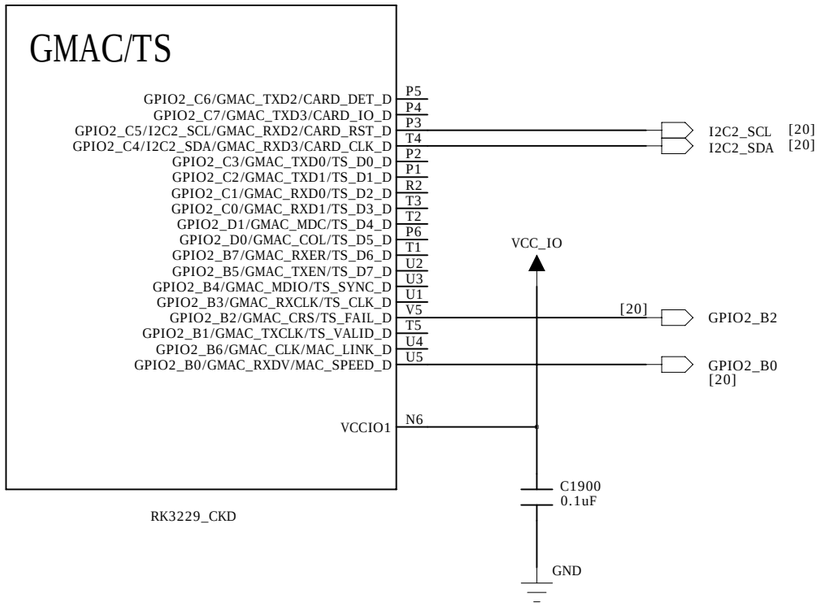
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 18 OF 22

U1000-B



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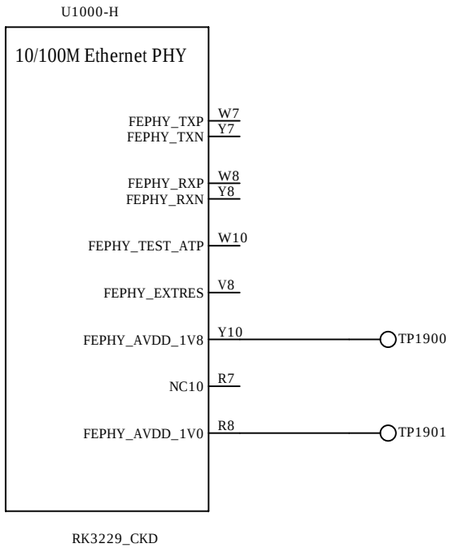

Libratone A/S		PROJECT NAME	Delta_N
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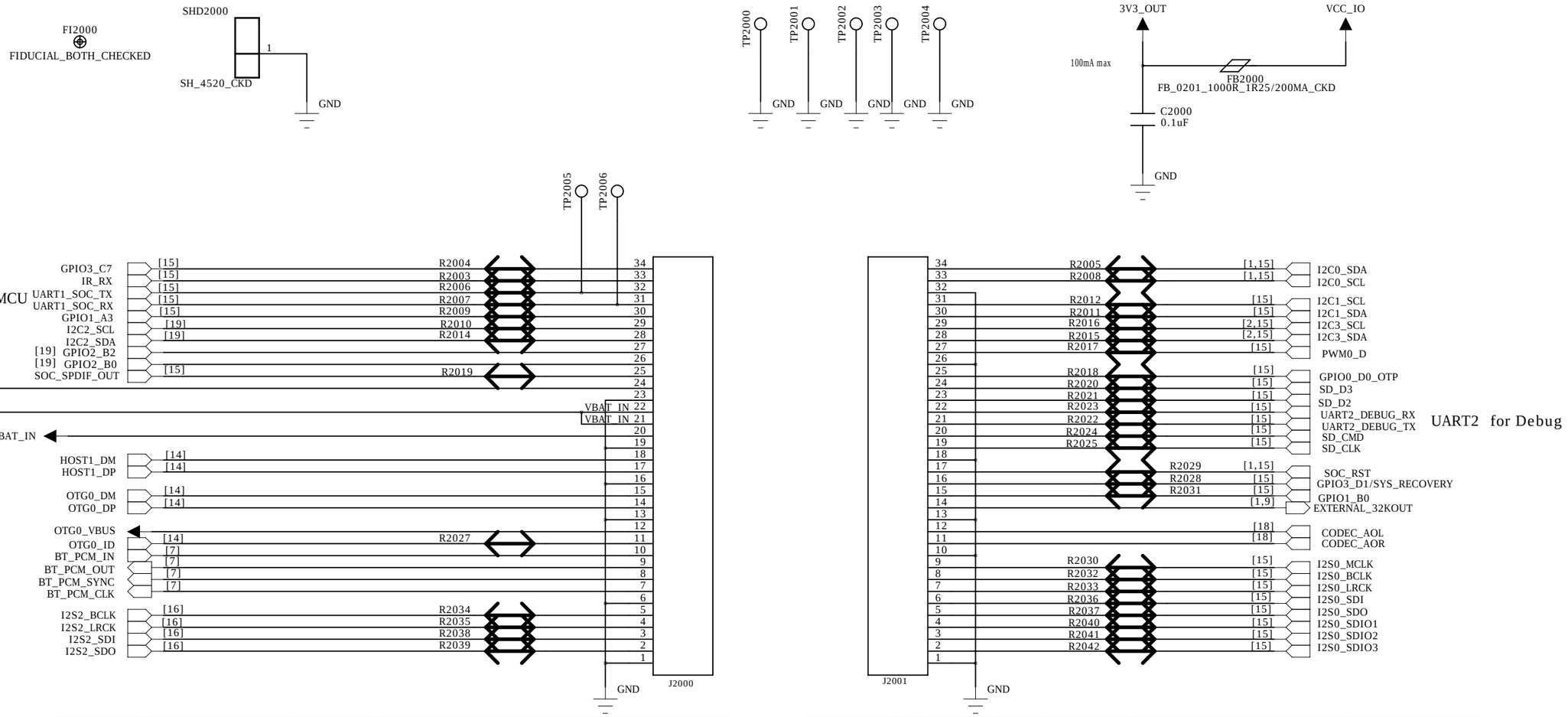
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. R0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 19 OF 22



DELTA_N-Part01

Number	Pin Define	Level	Pin Name	IO Domain
34	GPIO3_C7	3.3V	GPIO3_C7_u	VCCIO4
33	IR_RX	3.3V	GPIO1_B3/UART1_RTSN/IR_u;PMIC_OUT1	VCCIO4
32	UART1_SOC_TX	3.3V	GPIO1_B1/UART1_TX/UART2_TX_u	VCCIO4
31	UART1_SOC_RX	3.3V	GPIO1_B2/UART1_RX/UART2_RX_u	VCCIO4
30	GPIO1_A3	3.3V	GPIO1_A3_d	VCCIO4
29	I2C2_SCL	3.3V	GPIO2_C5/I2C2_SCL/GMAC_RXD2/CARD_RST_d	VCCIO1
28	I2C2_SDA	3.3V	GPIO2_C4/I2C2_SDA/GMAC_RXD3/CARD_CLK_d	VCCIO1
27	GPIO2_B2	3.3V	GPIO2_B2/GMAC_CRS/TS_FAIL_d	VCCIO1
26	GPIO2_B0	3.3V	GPIO2_B0/GMAC_RXDV/MAC_SPEED_d	VCCIO1
25	SOC_SPDIF_OUT	3.3V	GPIO3_D7/TEST_CLKO/SPDIF_d	VCCIO4
24	3V3_OUT	--------		PW
23	GND	GND	GND	GND
22	VBAT_IN1	--------		PW
21	VBAT_IN2	--------		PW
20	COMBO_VBAT_IN	--------		PW
19	GND	GND	GND	GND
18	HOST1_DM	--------	USB1_DM	USB PHY
17	HOST1_DP	--------	USB2_DP	USB PHY
16	GND	GND	GND	GND
15	OTG0_DM	--------	USB0_DM	USB PHY
14	OTG0_DP	--------	USB0_DP	USB PHY
13	GND	GND	GND	GND
12	OTG0_VBUS	--------	USB0_VBUS	USB PHY
11	OTG0_ID	--------	USB0_ID	USB PHY
10	BT_PCM_SDI	1.8V	BT_PCM_SDI	CYW43455
9	BT_PCM_SDO	1.8V	BT_PCM_SDO	CYW43455
8	BT_PCM_SYNC	1.8V	BT_PCM_SYNC	CYW43455
7	BT_PCM_CLK	1.8V	BT_PCM_CLK	CYW43455
6	GND	GND	GND	GND
5	I2S2_BCLK	3.3V	GPIO3_B3/PCM_CLK_d	VCCIO2
4	I2S2_LRCK	3.3V	GPIO3_B4/PCM_SYNC_d	VCCIO2
3	I2S2_SDI	3.3V	GPIO0_D2/PWM0/PCM_RX_d	VCCIO2
2	I2S2_SDO0	3.3V	GPIO0_D3/PWM1/PCM_TX_d	VCCIO2
1	GND	GND	GND	GND

DELTA_N-Part02

Number	Pin Define	Level	Pin Name	IO Domain
34	I2C0_SDA(2.2Kpull up)	3.3V	GPIO0_A1/I2C0_SDA_u	VCCIO4
33	I2C0_SCL(2.2K pull up)	3.3V	GPIO0_A0/I2C0_SCL_u	VCCIO4
32	**GND**	**GND**	**GND**	**GND**
31	I2C1_SCL	3.3V	GPIO0_A2/I2C1_SCL_u	VCCIO4
30	I2C1_SDA	3.3V	GPIO0_A3/I2C1_SDA/SDMMC1_CMD_u	VCCIO4
29	I2C3_SCL	3.3V	GPIO0_A6/HDMI_SCL/I2C3_SCL_u	VCCIO4
28	I2C3_SDA	3.3V	GPIO0_A7/HDMI_SDA/I2C3_SDA_u	VCCIO4
27	PWM_C	3.3V	GPIO3_C5/PWM0_d	VCCIO4
26	**GND**	**GND**	**GND**	**GND**
25	GPIO0_D0_OTP	3.3V	GPIO0_D0/OTP_u	VCCIO4
24	SD_D3	3.3V	GPIO1_C5/SDMMC0_D3/JTAG_TMS_u	VCCIO4
23	SD_D2	3.3V	GPIO1_C4/SDMMC0_D2/JTAG_TCK_u	VCCIO4
22	UART2_DEBUG_RX	3.3V	GPIO1_C3/SDMMC0_D1/UART2_RX_u	VCCIO4
21	UART2_DEBUG_TX	3.3V	GPIO1_C2/SDMMC0_D0/UART2_TX_u	VCCIO4
20	SD_CMD	3.3V	GPIO1_B7/SDMMC0_CMD_u	VCCIO4
19	SD_CLK	3.3V	GPIO1_C0/SDMMC0_CLKO_d	VCCIO4
18	**GND**	**GND**	**GND**	**GND**
17	SOC_RST	3.3V	NPOR_u	VCCIO4
16	GPIO3_D1/SYS_RECOVERY	3.3V	GPIO3_D1_u	VCCIO4
15	GPIO1_B0	3.3V	GPIO1_B0/UART1_CTSN/32K_OUT_u	VCCIO4
14	EXTERNAL_32KOUT	--------	CLK	
13	**GND**	**GND**	**GND**	**GND**
12	CODEC_AOL	--------	CODEC_AOL	AV_OUT
11	CODEC_AOR	--------	CODEC_AOR	AV_OUT
10	**GND**	**GND**	**GND**	**GND**
9	I2S0_MCLK	3.3V	GPIO0_B0/I2S0_MCLK_u	VCCIO4
8	I2S0_BCLK	3.3V	GPIO0_B1/I2S0_SCLK/SPI_CLK_u	VCCIO4
7	I2S0_LRCK	3.3V	GPIO0_B4/I2S0_LRCK_TX_u	VCCIO4
6	I2S0_SDI	3.3V	GPIO0_B6/I2S0_SDI/SPI_CSN0_u	VCCIO4
5	I2S0_SDO	3.3V	GPIO0_B5/I2S0_SDO/SPI_RXD_u	VCCIO4
4	I2S0_SDIO1	3.3V	GPIO1_A2/SDMMC1_D1/I2S0_SDIO1_u	VCCIO4
3	I2S0_SDIO2	3.3V	GPIO1_A4/SDMMC1_D2/I2S0_SDIO2_u	VCCIO4
2	I2S0_SDIO3	3.3V	GPIO1_A5/SDMMC1_D3/I2S0_SDIO3_u	VCCIO4
1	**GND**	**GND**	**GND**	**GND**

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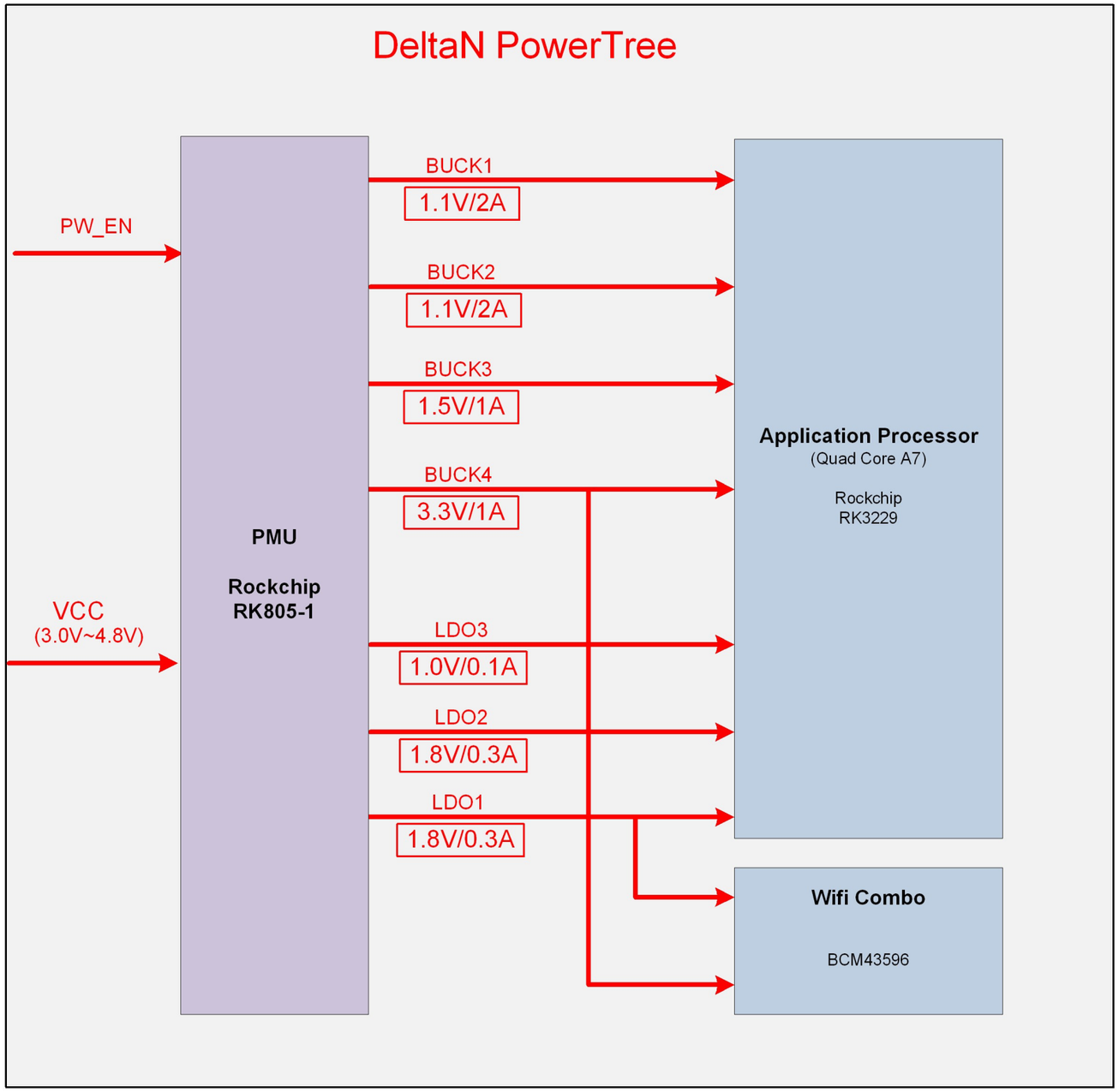
DeltaN PowerTree



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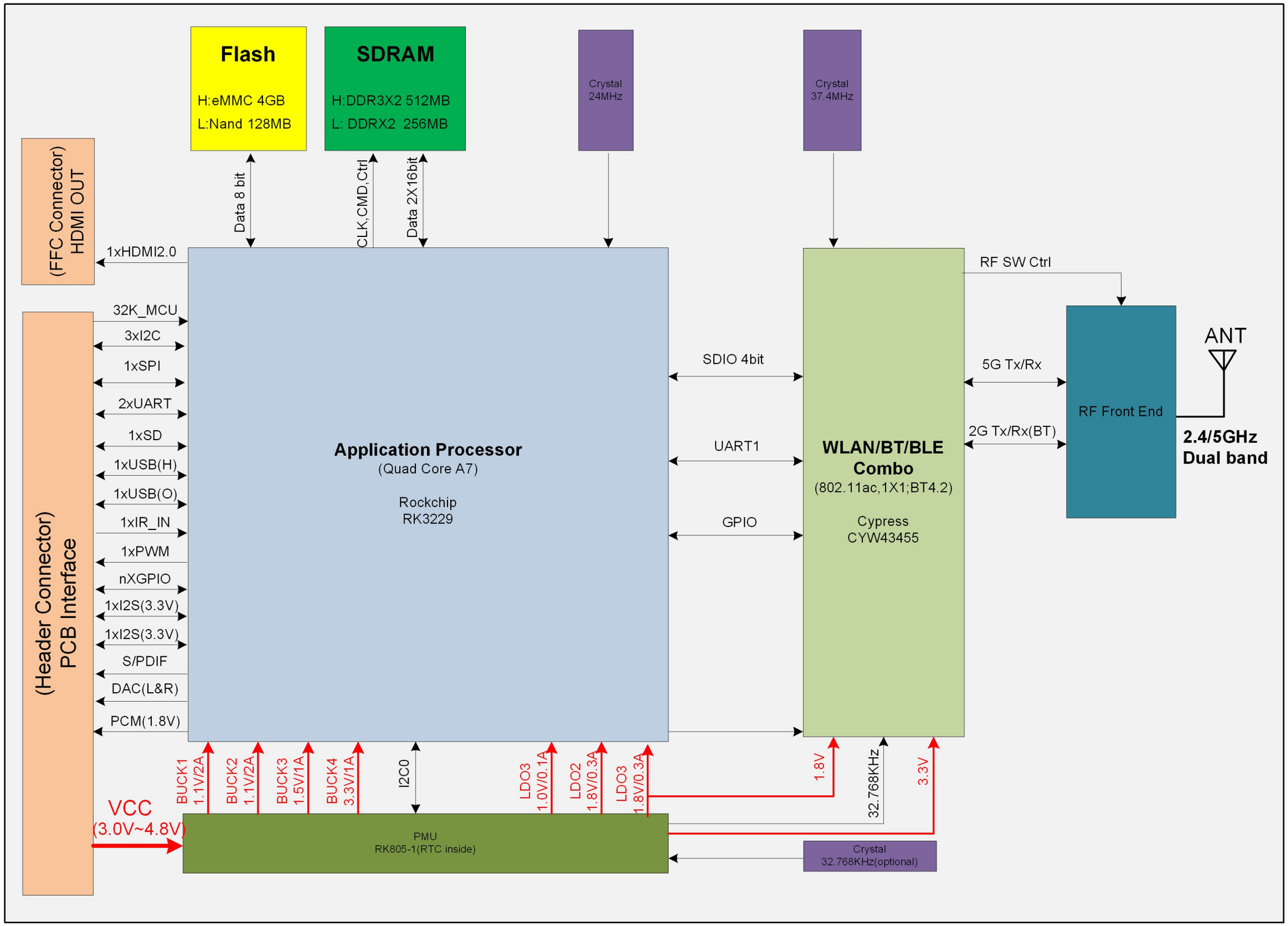
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/11/29	SHEET 21 OF 22



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