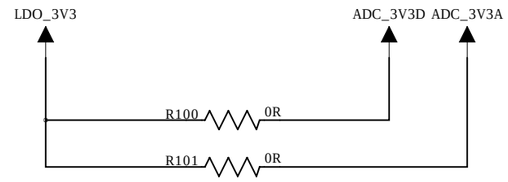
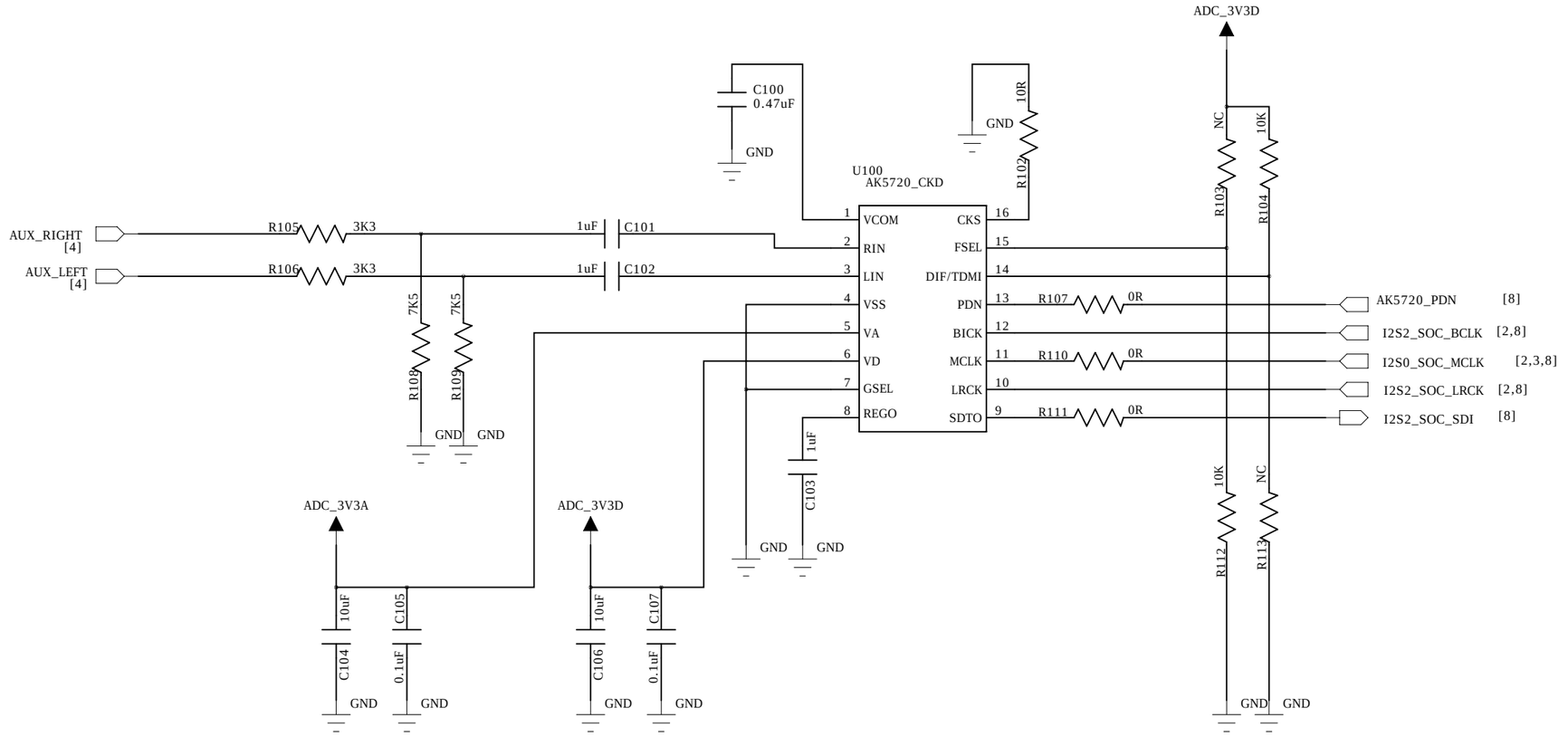




Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 1 OF 17

0.49Vrms input max

[11] WF_REF-
[11] WF_REF+
R200 130K 1uF C200
R201 130K 1uF C201
27K R203 GND
27K R204 GND

PVDD
3R3 R229
1uF C232 GND
PA_3V3 PA_3V3
100K R214
1uF C243
1uF C234
1uF C227 GND

U200
TAS5760MDAPR_DRAFT

1	AVDD	GVDD_REG	32
2	SFT_CLIP	GGND	31
3	ANA_REG	BSTRPA+	30
4	VCOM	SPK_OUTA+	29
5	ANA_REF	PVDD_2	28
6	SPK_FAULT	PGND_2	27
7	SPK_SD	SPK_OUTA-	26
8	FREQ/SDA	BSTRPA-	25
9	PBTL/SCL	BSTRPB-	24
10	DVDD	SPK_OUTB-	23
11	SPK_GAIN0	PGND_1	22
12	SPK_GAIN1	PVDD_1	21
13	SPK_SLEEP/ADR	SPK_OUTB+	20
14	MCLK	BSTRPB+	19
15	SCLK	DGND	18
16	SDIN	LRCK	17
33	POWERPAD		

[8] PA_FAULT
[8] PA_SD
[8,9,10] I2C2_SOC_SDA
[8,9,10] I2C2_SOC_SCL
R208 0R
R209 0R
GND 1uF C235
R222 10K
[8] PA_MUTE
[1,3,8] I2S0_SOC_MCLK
[1,8] I2S2_SOC_BCLK
48K, 64Fs
[8] I2S2_SOC_SDO
R226 0R
R223 0R
R224 0R
[1,8] I2S2_SOC_LRCK
R225 0R
10K R227
I2C ADD:0XD8/0XD9
GND

PVDD
C203 1000pF
0.1uF C204
1uF C205
C206 470u
GND GND GND GND

0.22uF C226
0.22uF C225
0.22uF C224
0.22uF C223

L200 15uH
L201 15uH
L_1010_10UH_20%_DRAFT
L202

0.01uF C207 R206 3R3 GND
0.01uF C217 R211 3R3 GND
0.01uF C220 R212 3R3 GND
0.01uF C230 R215 3R3 GND

1uF C215 GND
1uF C216 GND
1uF C228 GND
1uF C229 GND

TP200 TP201
J200 EHK-2AL_CKD
WF+
WF-

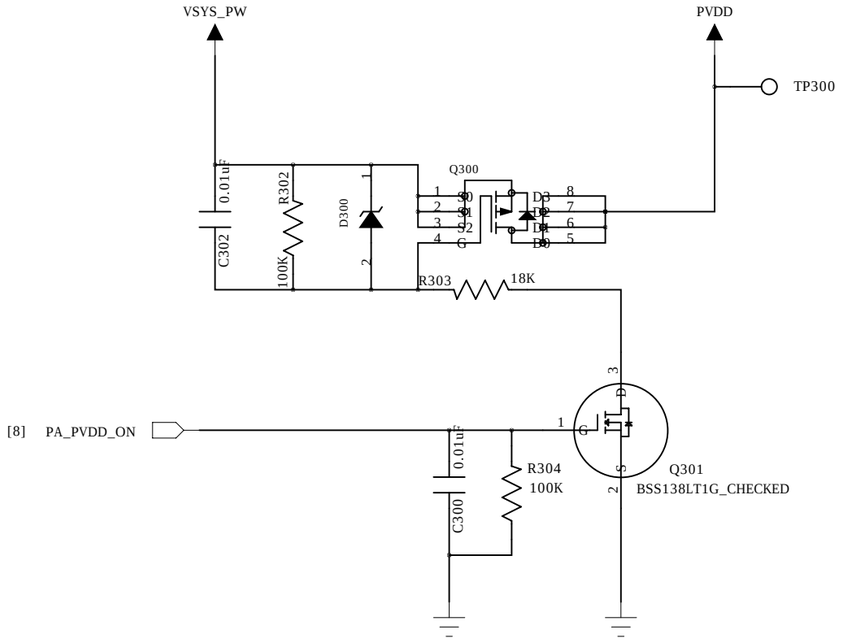
TP202 TP203
J201 EHK-4AL_CKD
TW-
TW+

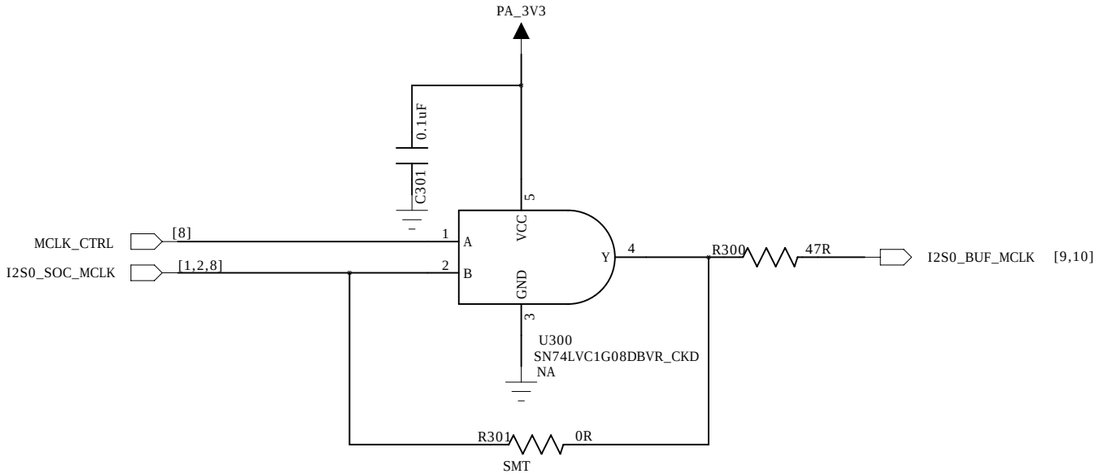
PVDD
C236 1000pF
0.1uF C237
1uF C238
C239 470u
GND GND GND GND

VSYS_3V3
PA_3V3
Q200 RE1C002ZPTL_CHECKED
TP204
100K R2
0.1uF C222
C221 4.7uF
PA_3V3_ON [8]
NA R221
GND GND

0.62Vrms input max
[11] TW_REF+
[11] TW_REF-
R216 56K 1uF C240
R217 56K 1uF C241
27K R218 GND
27K R219 GND

Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 2 OF 17

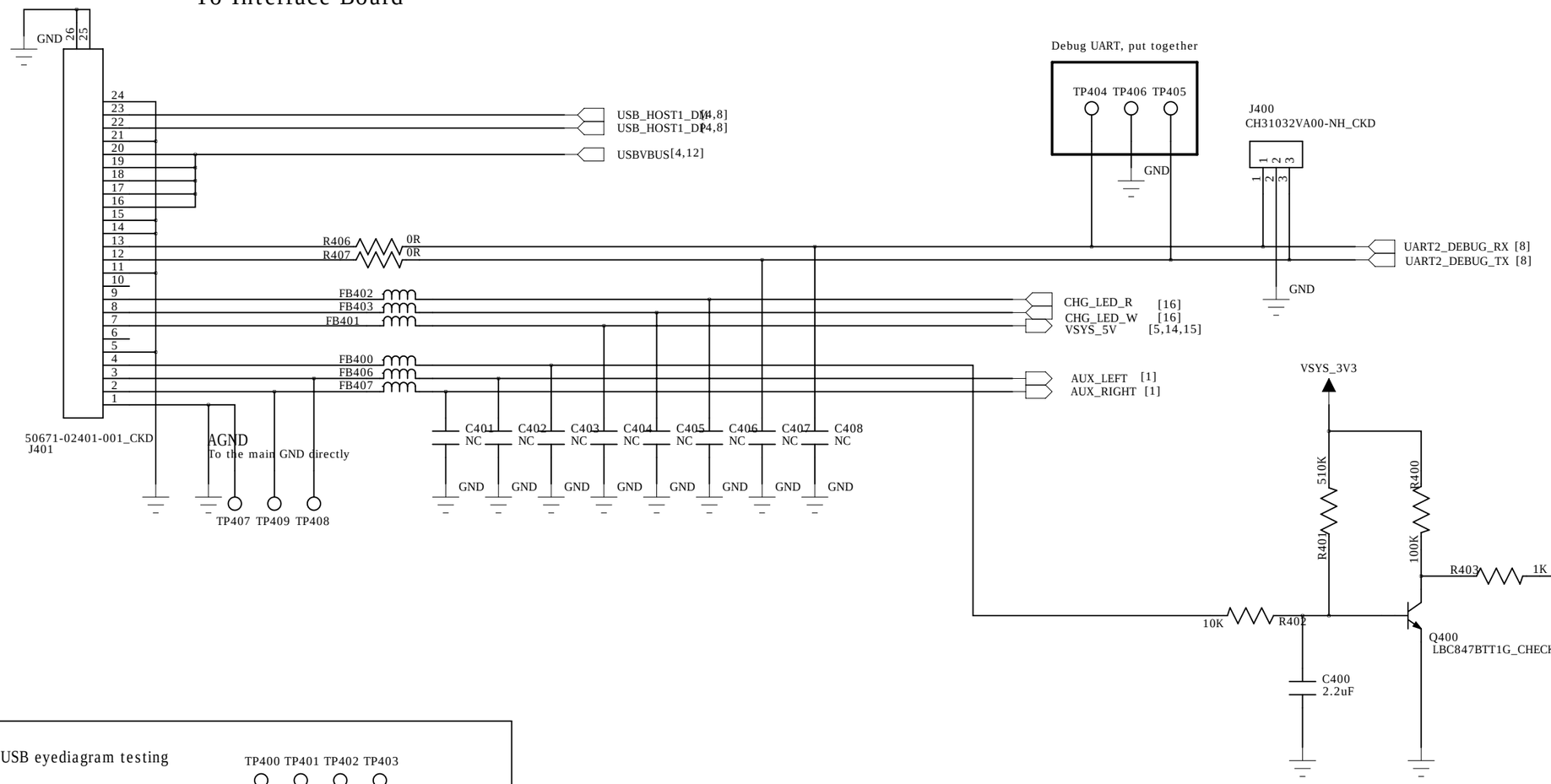


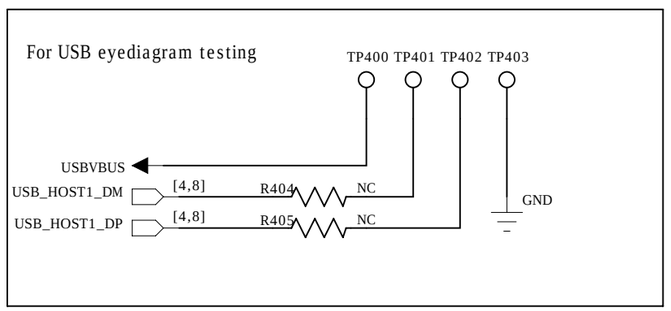


	EGG II	ZIPP3
U900	NA	ON
U1100	NA	ON
U300	NA	ON
R301	ON	NA
C206&C239	470uF	1000uF

Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 3 OF 17

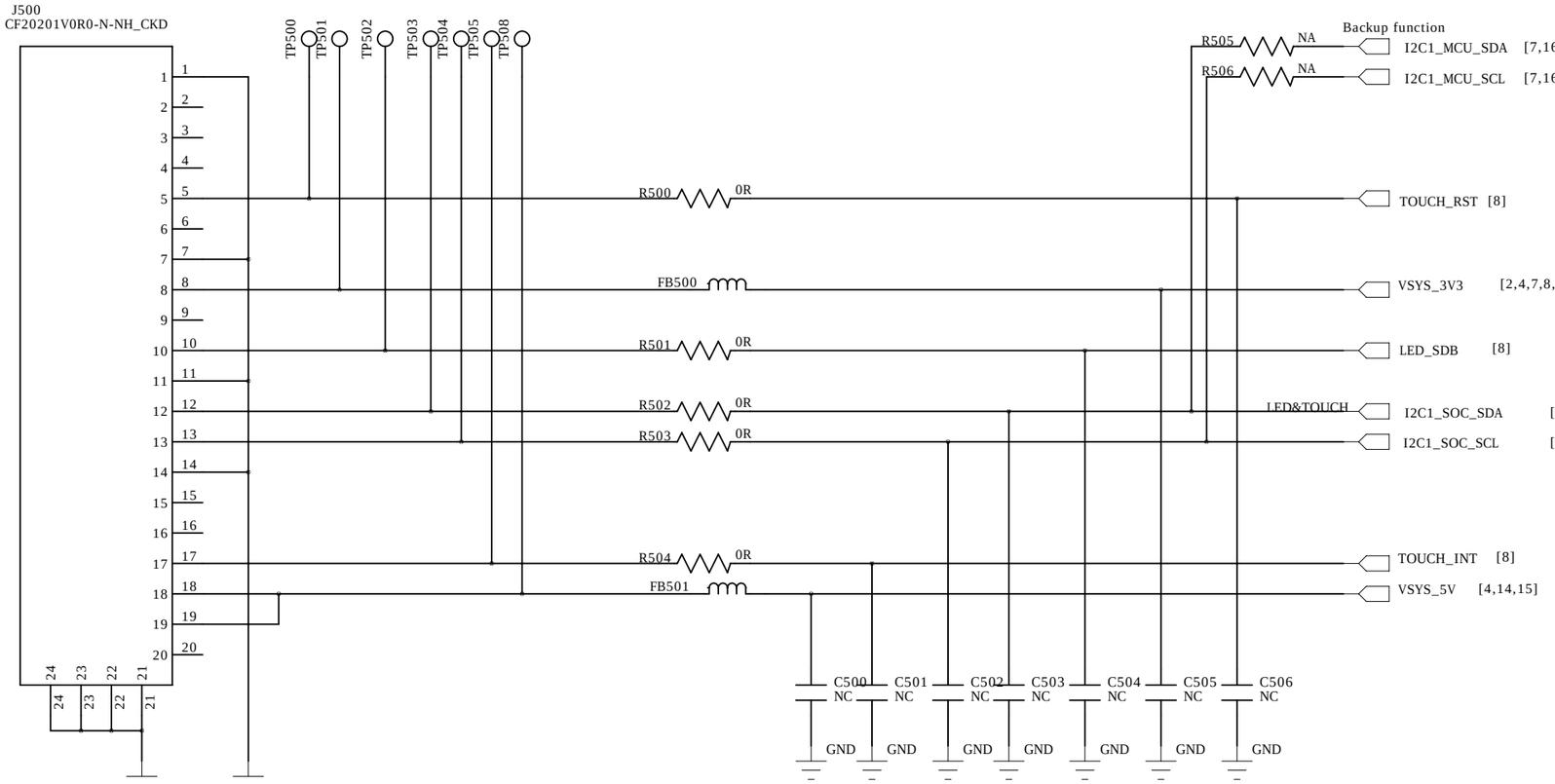
To Interface Board

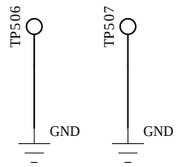




Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 4 OF 17

To LED Board

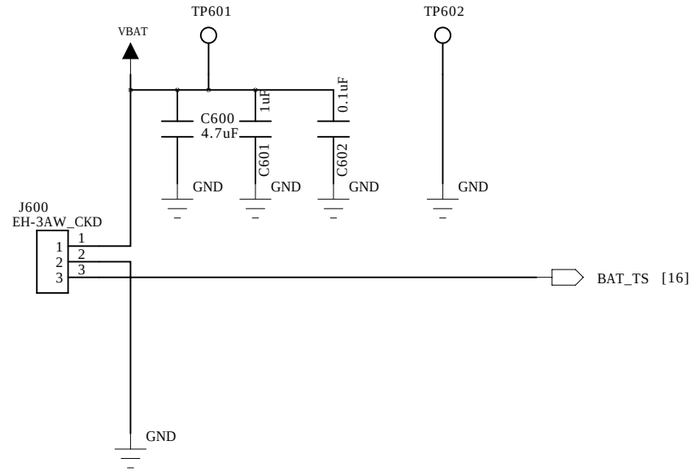


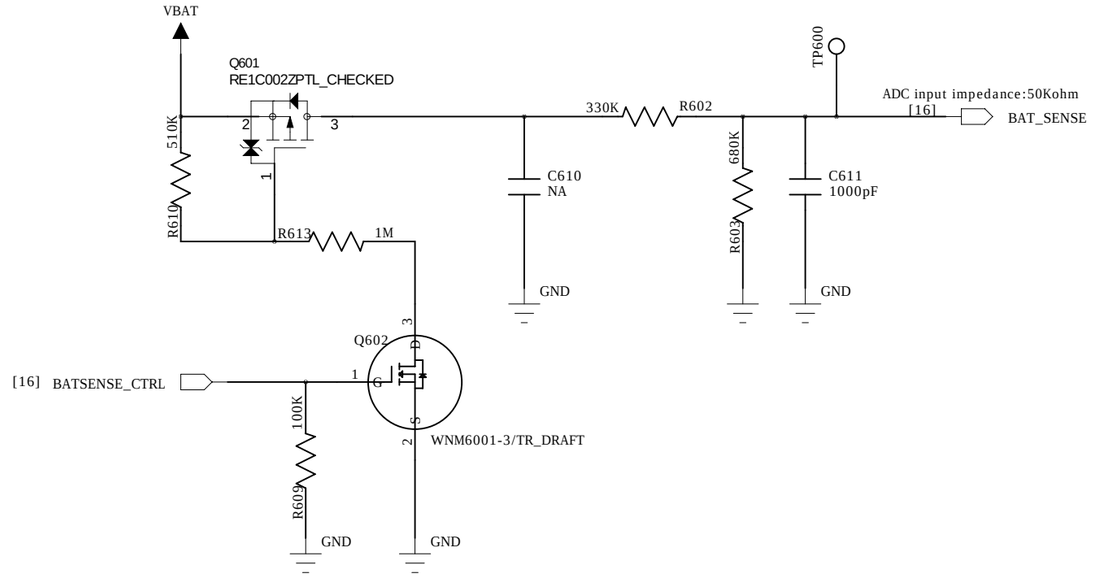


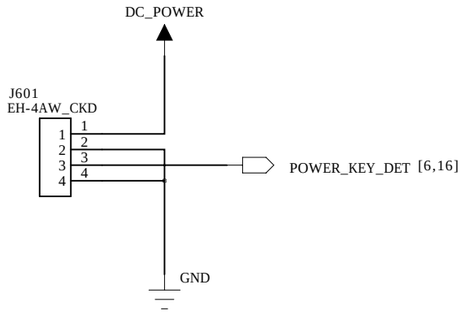
Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 5 OF 17

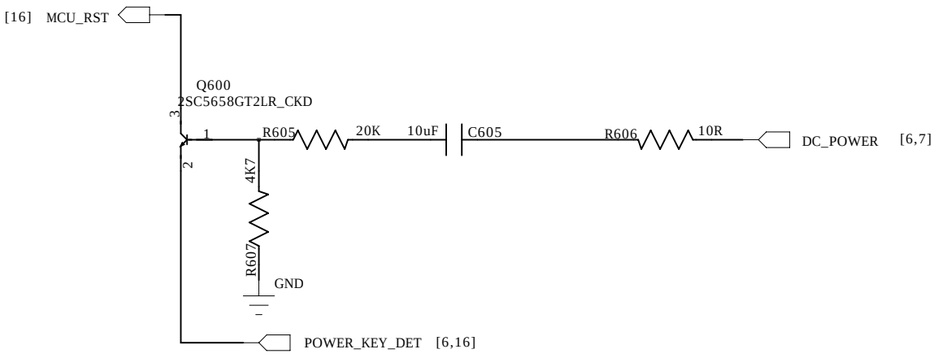
µç³Øµç¿×î´ó16.8V£¬×îÐ¡13.0V

MCU×î´ó²ÉÑùµçÑ¹3.3V µç³Ø²ÉÑùµçÑ¹Ë¥¼õ18dB









Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 6 OF 17

DC_POWER

Input:19V~21V

VSYS_PW

Q700 Q701

R700 0R02

R701 3R3

C713 4.7uF

C700 NC

C701 NC

R702 1R

R703 1R

C714 4.7uF

C708 10uF C709 10uF C710 0.1uF C711 10uF C712 10uF

Q702 Q703

L700 2.2uH

C702 10uF C703 0.1uF C704 10uF C705 10uF C706 10uF C707 10uF

DC_POWER,VSYS_PW,VBAT trace:3mm at least(prefer 5mm)

VBAT

VBAT Input:12V~17V

Q704

R704 750K

R705 47K C717 0.1uF

C715 1uF C716 1uF

Current sense: diff trace

C718 0.22uF C719 0.22uF

R706 0R

R707 1R

R709 1R 0R01

C720 4.7uF

C721 NC C722 1uF C723 1uF

C724 22uF

VSYS_3V3

CHG_VDD MCU_3V3

R712 NC R713 510K

R710 100K R711 NC

U700

GND_PAD 33

UGATE1 11

LGATE1 9

BOOT1 12

PHASE1 10

PHASE2 6

BOOT2 4

LGATE2 7

UGATE2 5

CSIN 14

CSIP 15

ASGATE 13

ADP 16

ACIN 19

ACOK 24

PROCHOT# 23

AMON/BMON 29

BATGONE 25

OTGEN/CMIN 20

SCL 22

SDA 21

COMP 28

PROG 27

DCIN 17

VDD 18

VDDP 8

VSYS 3

CSOP 2

CSON 1

BGATE 32

VBAT 31

OTGPG/CMOUT 26

PSYS 30

ISL9238HRTZ-T_CKD

To PW Ctrol ADP_PG [16]

[16] CHG_PROCHOT

[16] CHG_ABMON

ACIN threshold>0.8V(input>15V)

R716 0R

R717 0R

ADC OUT:Adapter/Battery Current Monitor

R715 1K

R718 0R

CHG_PG

TP700

CHG_PSYSMON [16]

Power output monitor

20W*1.44uA*100K=2.88V

R719 100K C725 NC

C726 4700pF

R714 100K

C727 1000pF R720 0R R721 NC

Default (Input: 19V/0.5A)

I2C1_MCU_SCL [5,16] R722 0R

I2C1_MCU_SDA [5,16] R723 0R

C728 698R NC R724 C730 0.022uF

C729 215K R725 100pF

CHG_VDD

R726 4R7

C731 0.1uF C732 4.7uF C733 4.7uF C734 1uF

C735 1uF

R727 3R3

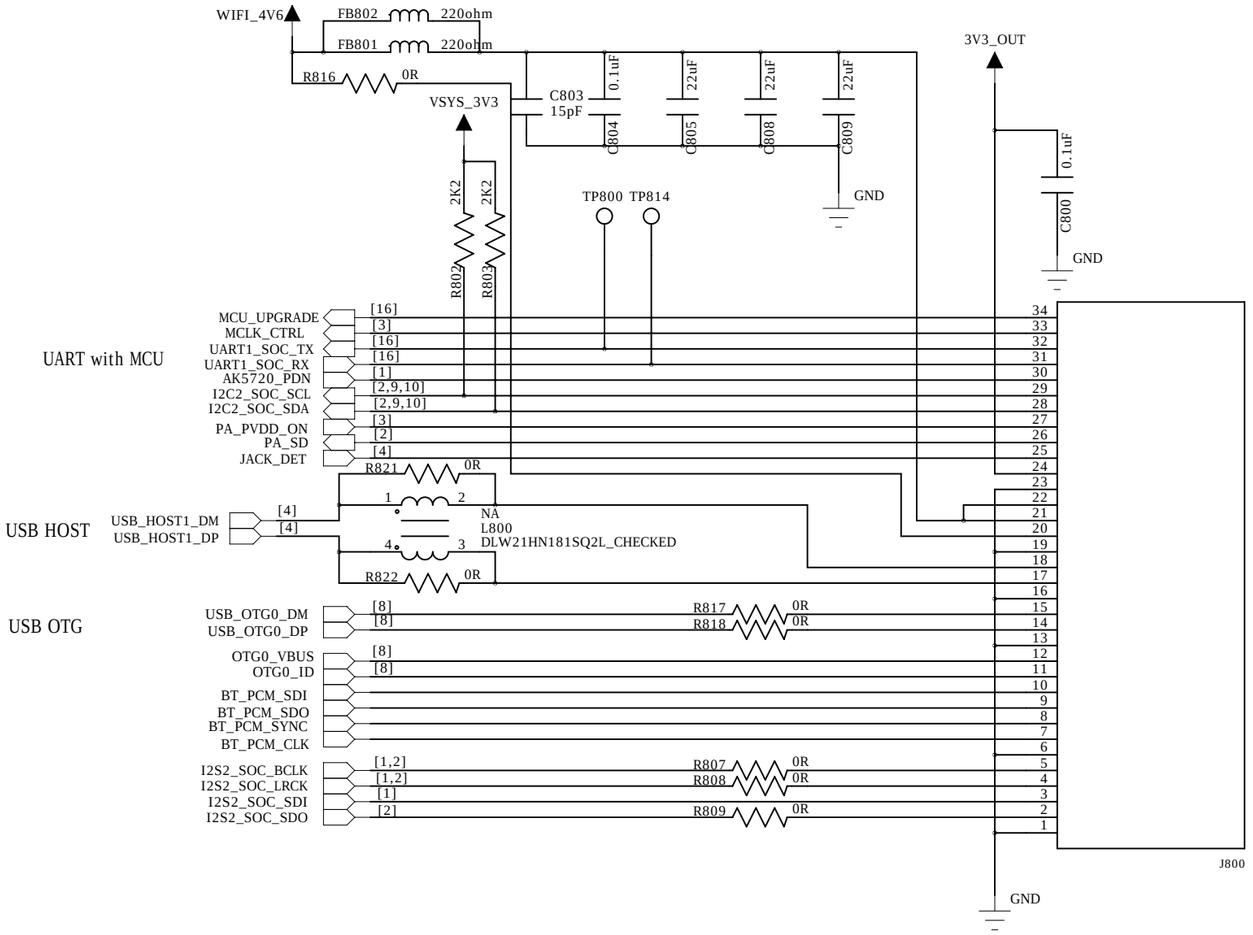
D700 RB520CS-30GT2RA_CKD

D701 RB520CS-30GT2RA_CKD

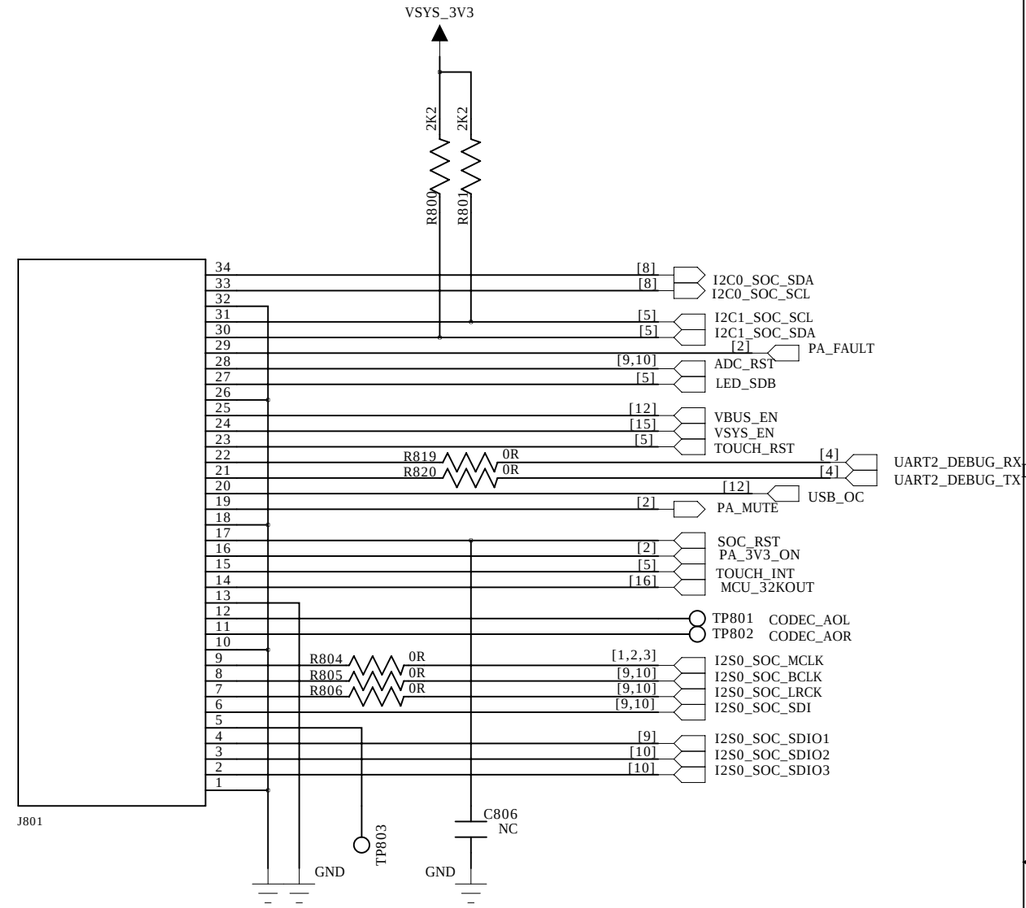
DC_POWER VSYS_PW

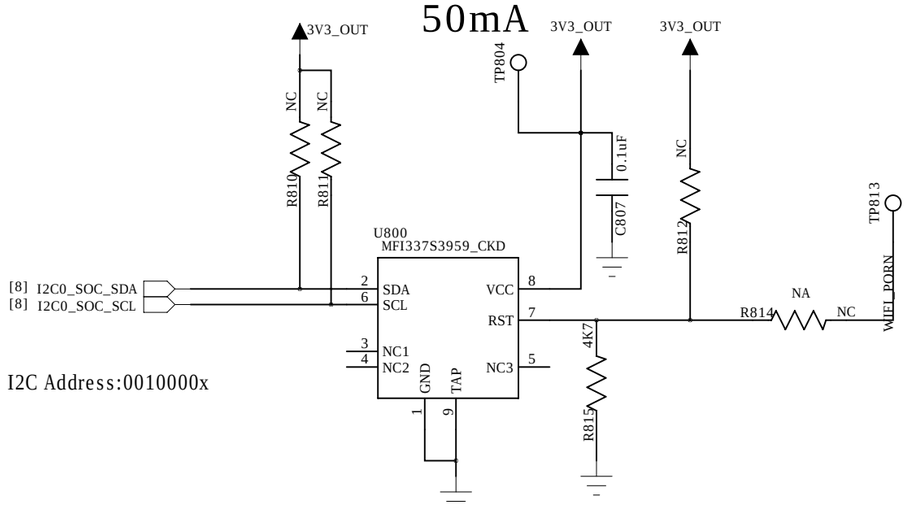
PROG Default: 4cells,733KHz,default 0.476A charging

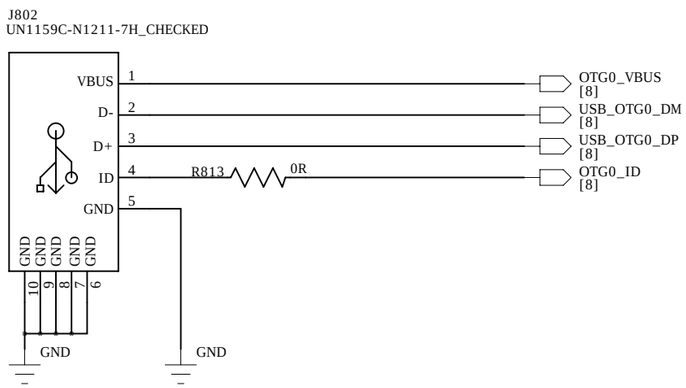
Libratone A/S	PROJECT NAME	EGG II	
LIBRATONE	DRAW NO	ES1	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 7 OF 17

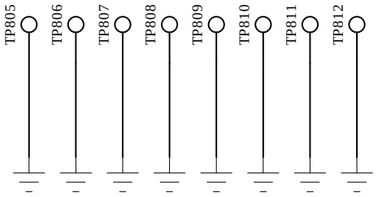


Delta N









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Libratone A/S	PROJECT NAME	EGG II	
LIBRATONE	DRAW NO	ES1	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 8 OF 17

External Power Supply: CP12IN:4.5V
LDO33IN:4.5V
VDDI2S:3.3V

I2C ADD:0X3B

TDM&RST:3.3V level I2C&MCLK: 3V3Level

MIC(1~4)

Rst must stay low for 100ms after all power rails are stable

Audio Slave
Audio TDM 1.8V level with 6ADC
Digital I/O 3.3V level

U900
AC108_DRAFT
NA

Libratone A/S	PROJECT NAME	EGG II	
	DRAW NO	ES1	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 9 OF 17

External Power Supply: CP12IN:4.5V

LDO33IN:4.5V

VDDI2S:3.3V

I2C ADD:0X35

TDM&RST:3.3V level I2C&MCLK: 3V3Level

MIC(5~6)

Rst must stay low for 100ms after all power rails are stable

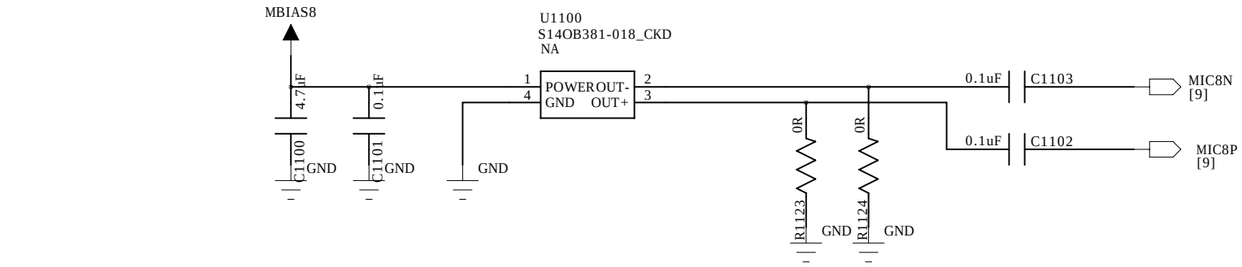
For I2S Encoding Mode

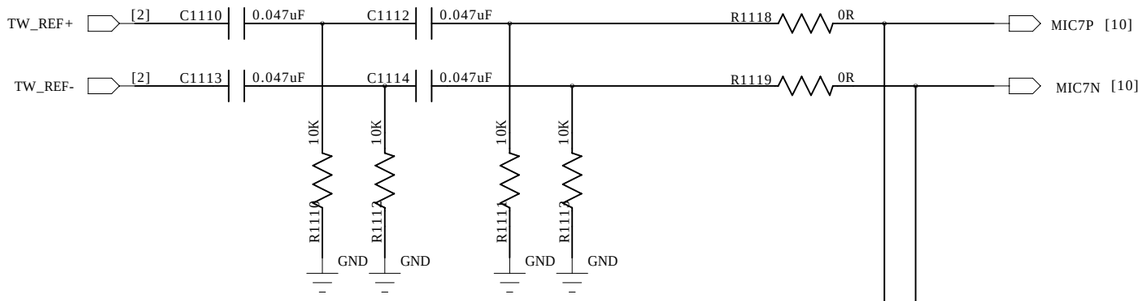
Audio Slave

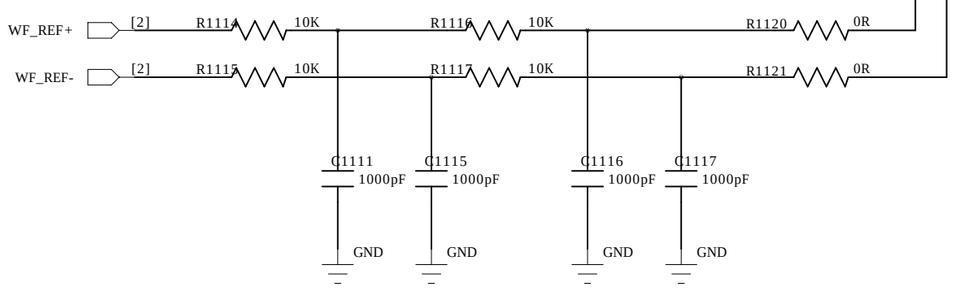
Audio TDM 1.8V level with 6ADC

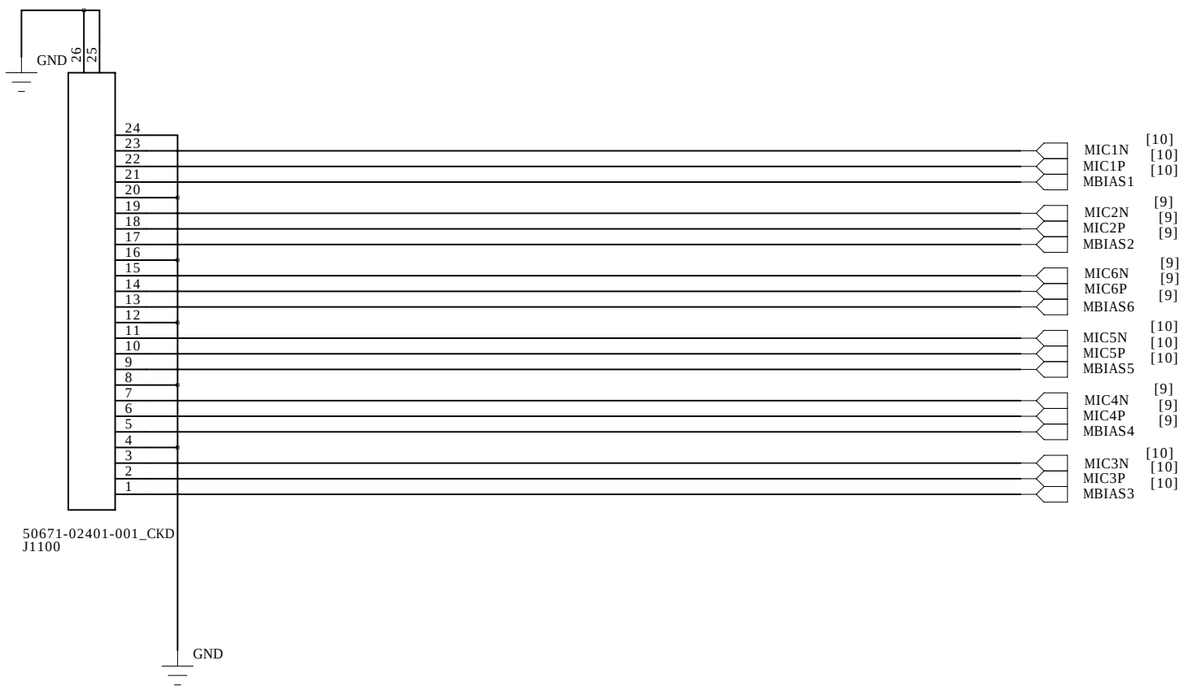
Digital I/O 3.3V level

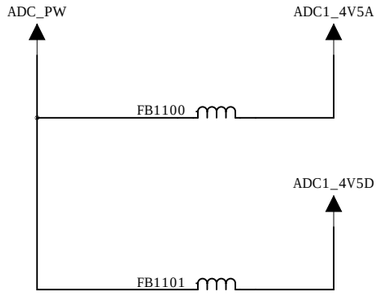
Libratone A/S		PROJECT NAME	EGG II
LIBRATONE		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 10 OF 17

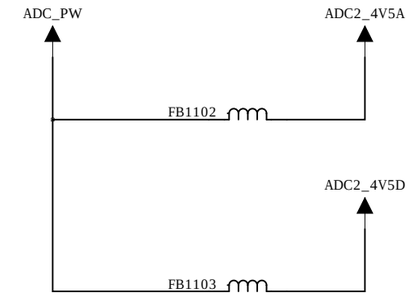


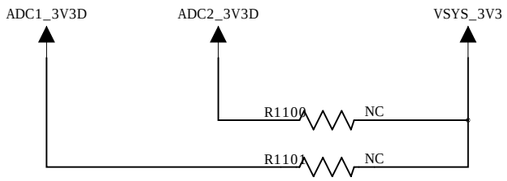






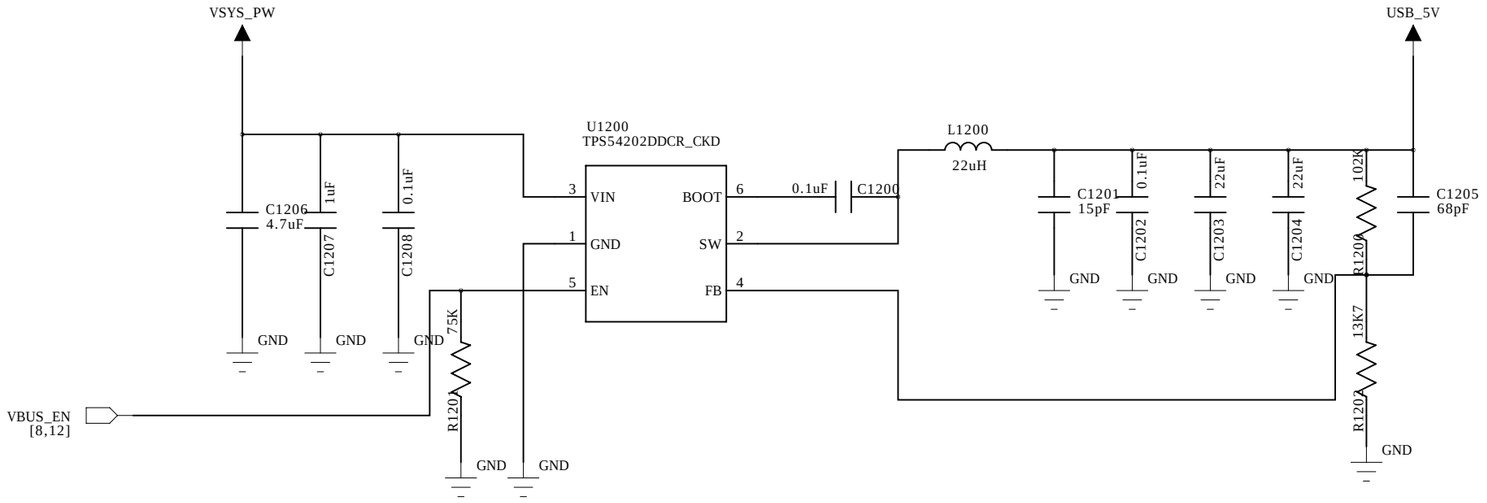




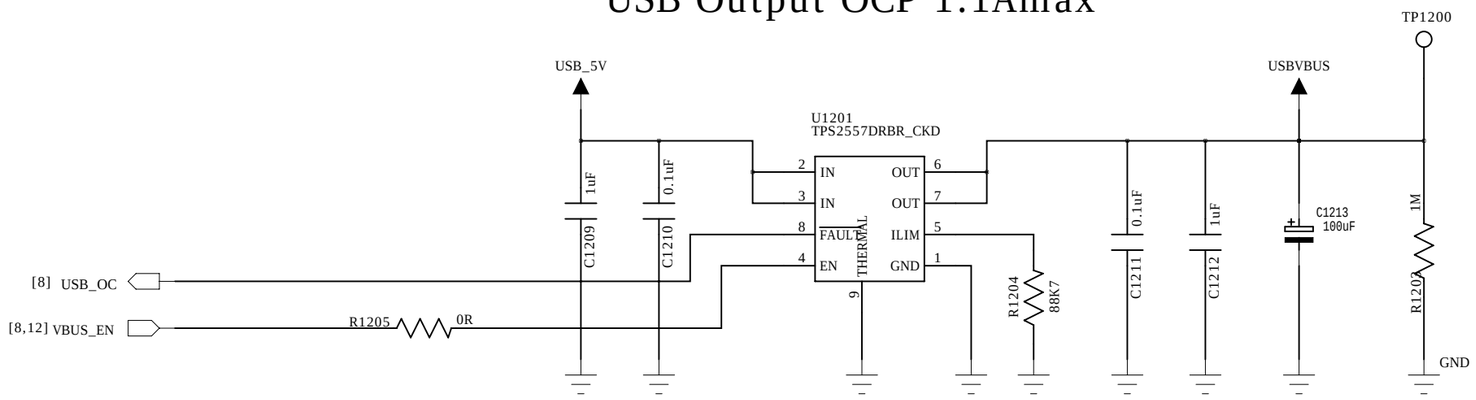


U900-ADC1	Aux_Right/SPK_TW
ADC2	MIC4
ADC3	MIC6
ADC4	MIC2
U1000-ADC1	Aux_Left/SPK_WF
ADC2	MIC3
ADC3	MIC5
ADC4	MIC1

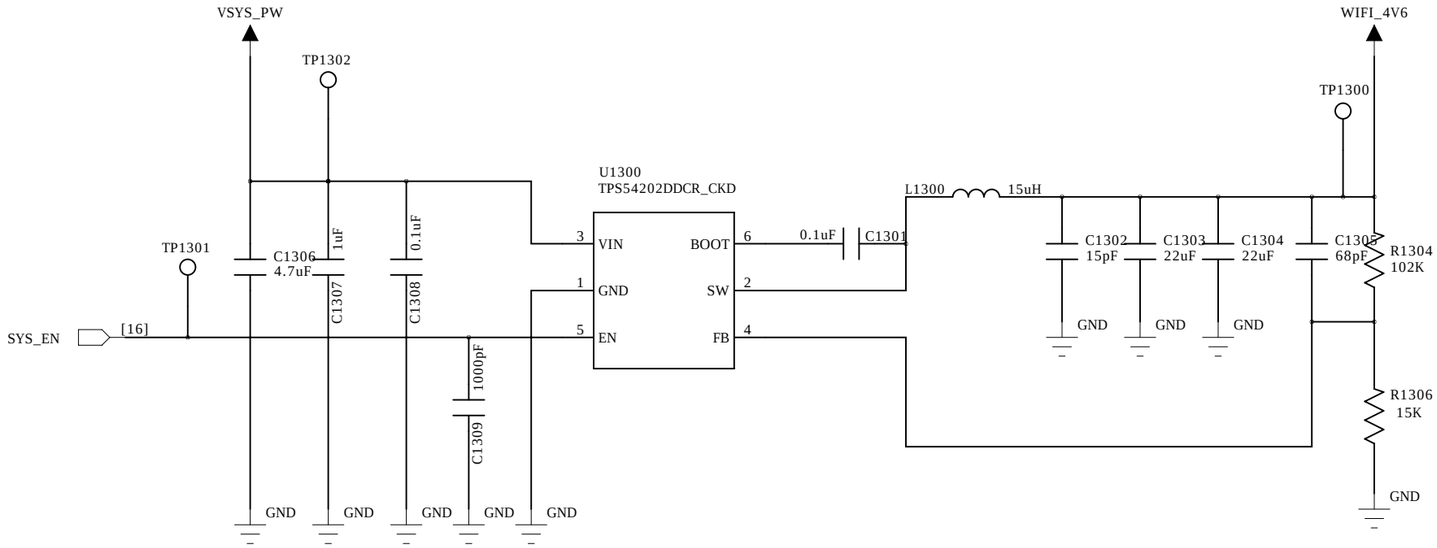
Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 11 OF 17



USB Output OCP 1.1Amax



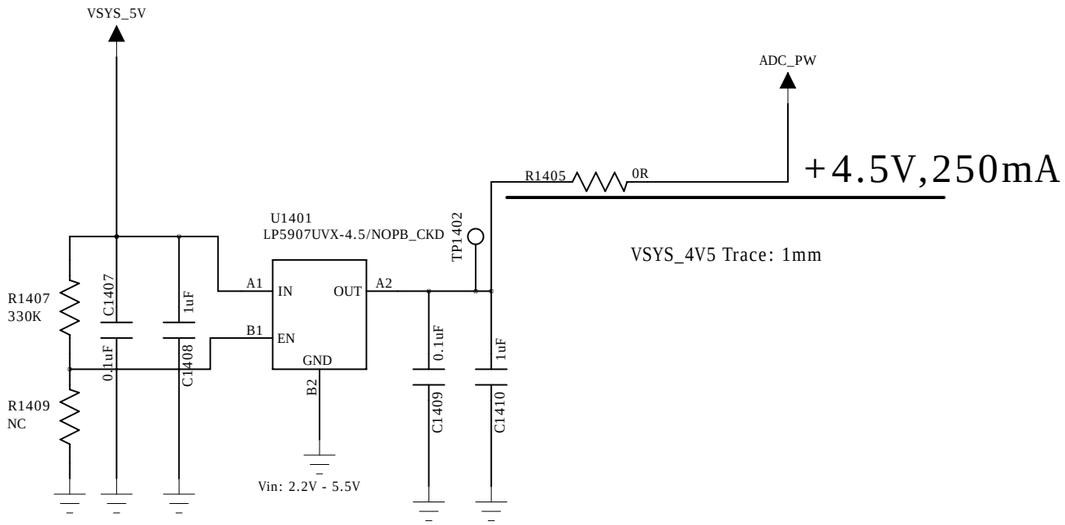
Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 12 OF 17

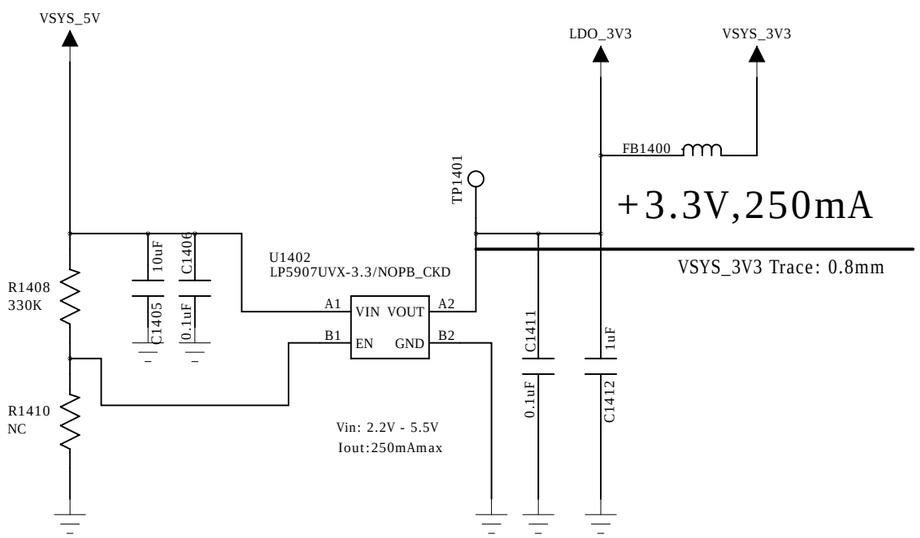


P1300

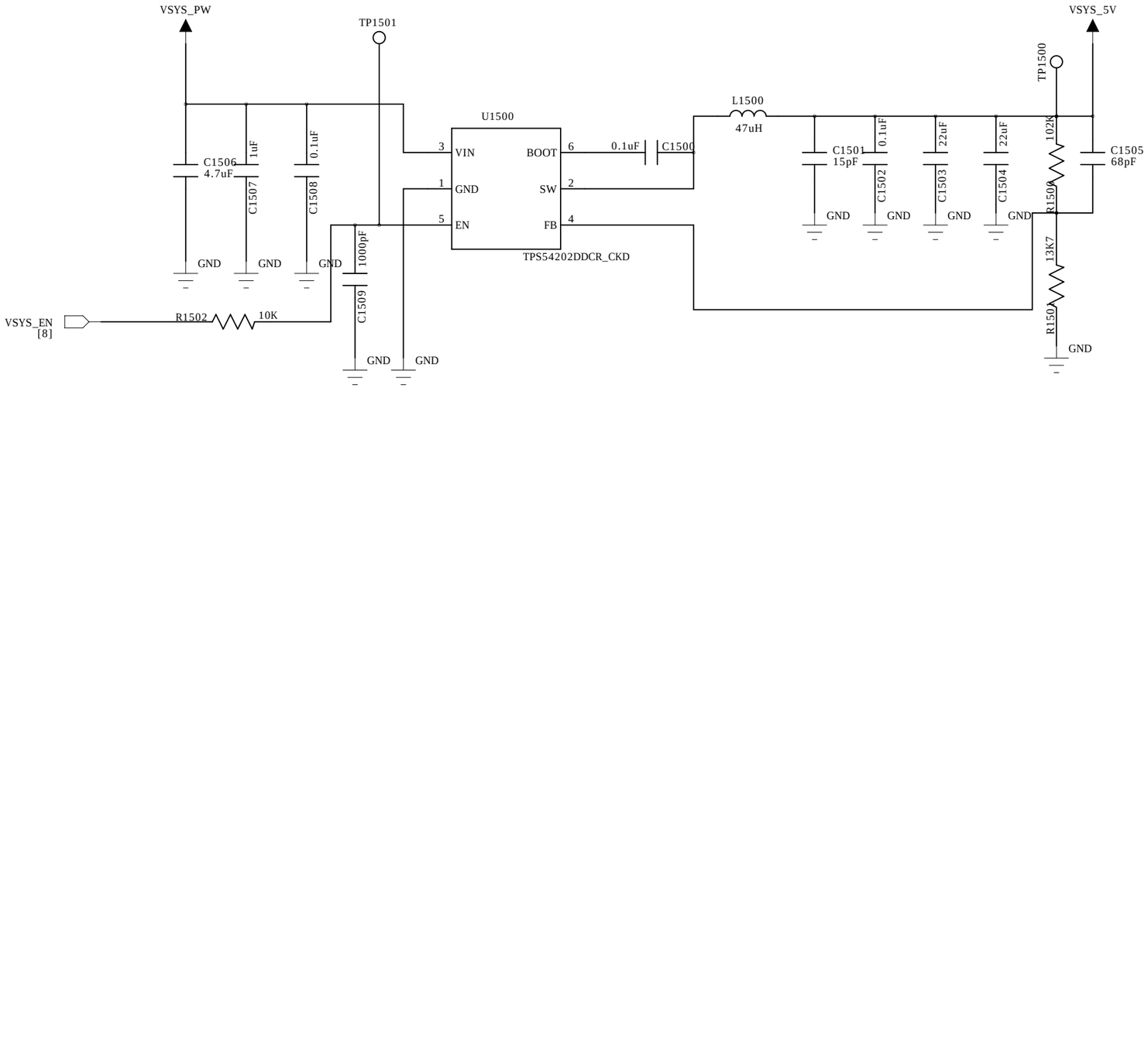
FIDUCIAL_BOTH_CHECKED

Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 13 OF 17

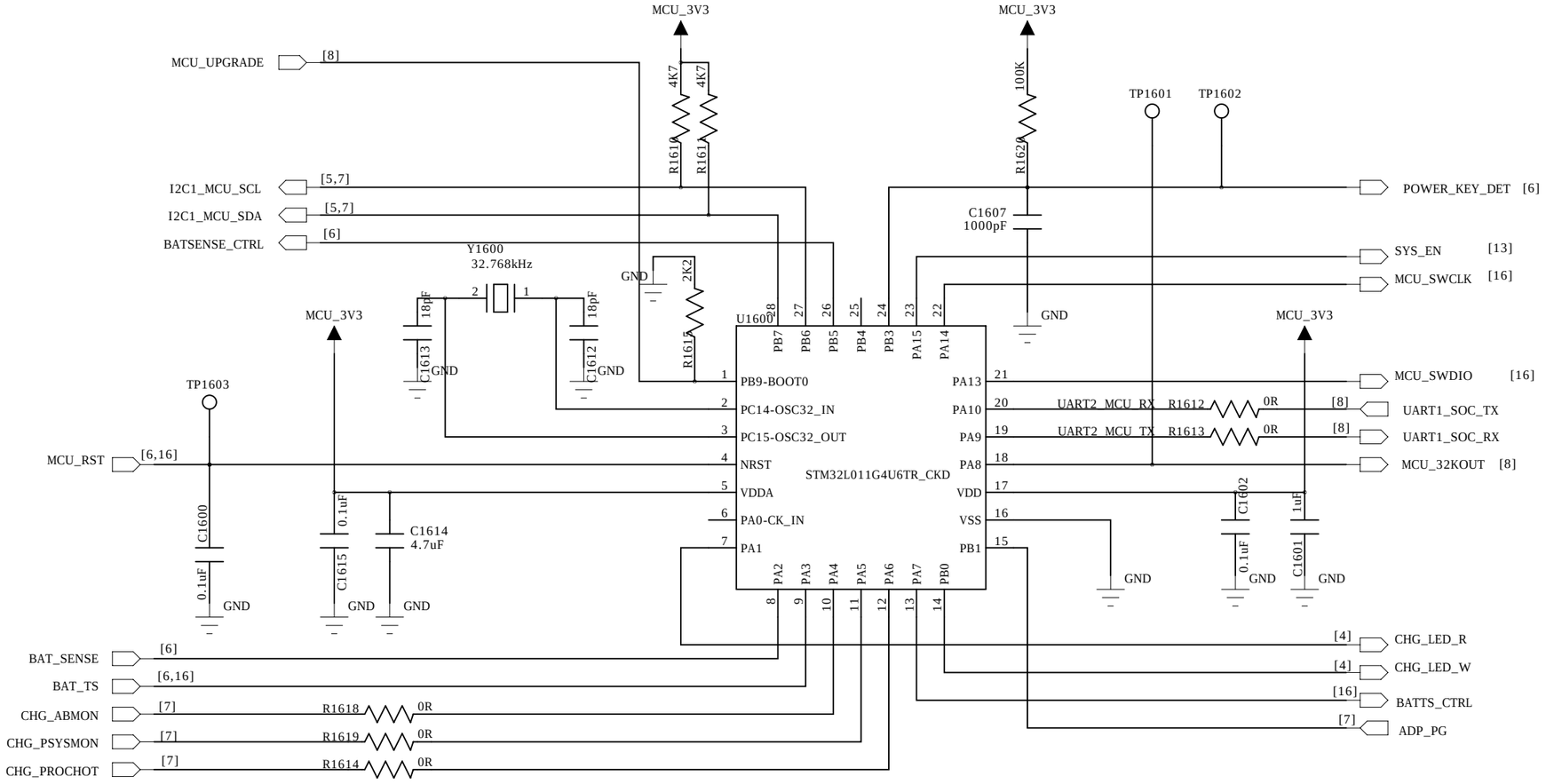


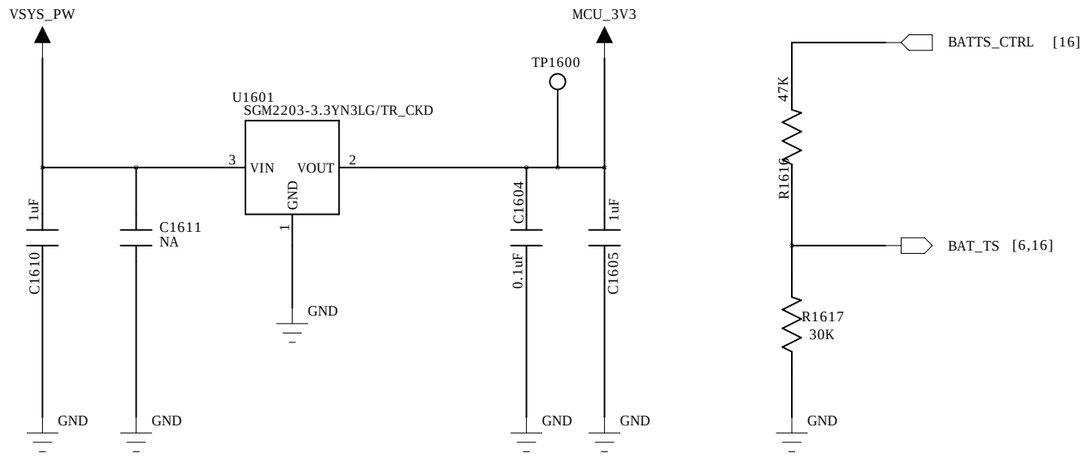


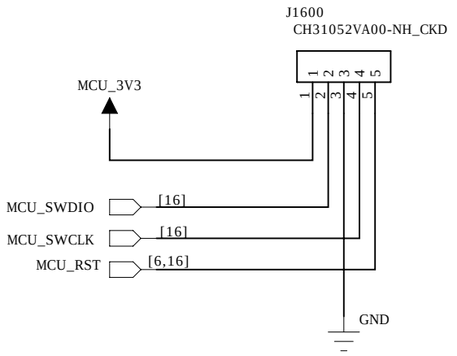
Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 14 OF 17



Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 15 OF 17

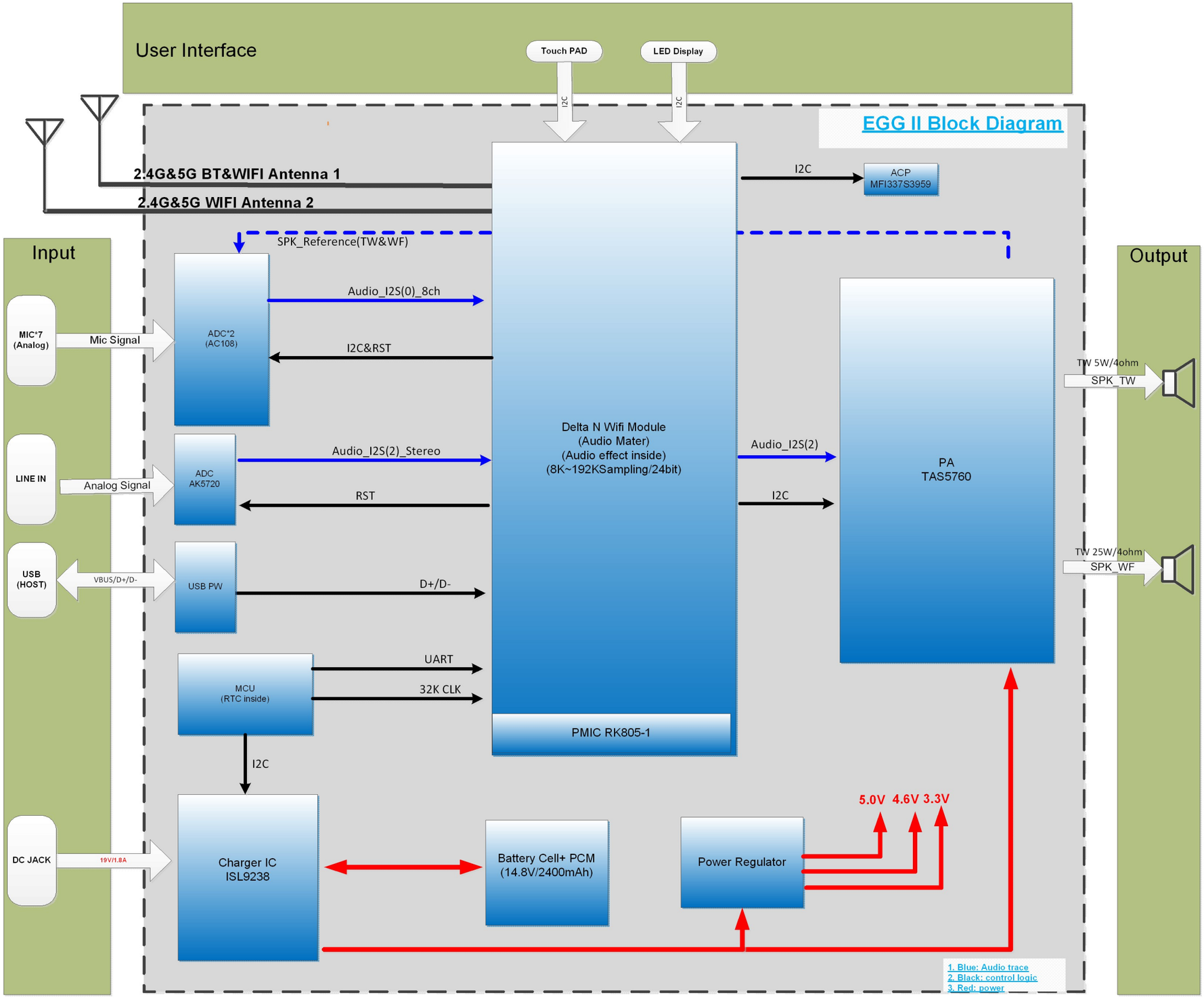






Libratone A/S		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 16 OF 17

EGG II Block Diagram



Libratone A/S		PROJECT NAME	EGG II
LIBRATONE		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 17 OF 17