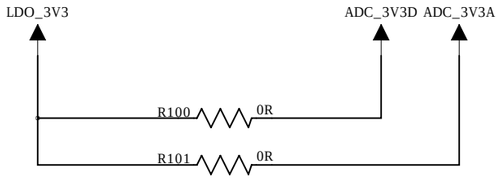
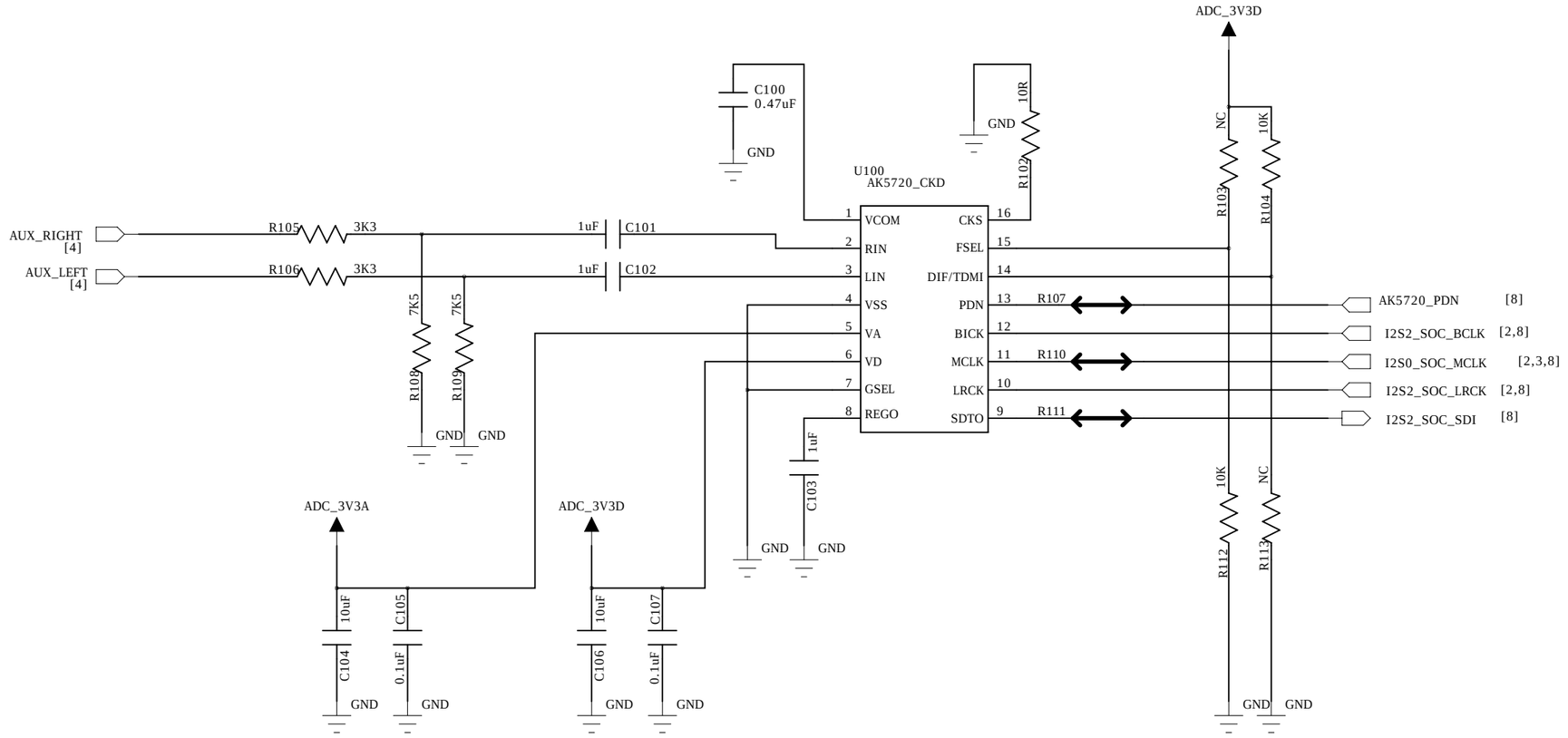




Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 1 OF 18

0.64Vrms input max

[11] WF_REF-
[11] WF_REF+
R200 47K 1uF C200
R201 47K 1uF C201
27K R203 GND
27K R204 GND

! 0207

PVDD
3R3 R229
1uF C232
GND

PA_3V3
PA_3V3
100K R214
1uF C243
1uF C234

U200
TAS5760MDAPR_CKD

1	AVDD	GVDD_REG	32
2	SFT_CLIP	GGND	31
3	ANA_REG	BSTRPA+	30
4	VCOM	SPK_OUTA+	29
5	ANA_REF	PVDD_2	28
6	SPK_FAULT	PGND_2	27
7	SPK_SD	SPK_OUTA-	26
8	FREQ/SDA	BSTRPA-	25
9	PBTL/SCL	BSTRPB-	24
10	DVDD	SPK_OUTB-	23
11	SPK_GAIN0	PGND_1	22
12	SPK_GAIN1	PVDD_1	21
13	SPK_SLEEP/ADR	SPK_OUTB+	20
14	MCLK	BSTRPB+	19
15	SCLK	DGND	18
16	SDIN	LRCK	17
33	POWERPAD		

1uF C227
GND

PVDD
C203 1000pF
0.1uF C204
1uF C205
C206 1000uF/25V
GND GND GND GND

0.01uF C207 R206 3R3 GND
L200 15uH
TP200 TP201
J200 EHK-2AL_CKD
WF+ 1
2
WF-

L201 15uH
1uF C215 GND
1uF C216 GND
0.01uF C217 R211 3R3 GND

0.22uF C226
0.22uF C225
0.22uF C224
0.22uF C223

[8] PA_SD
[8,9,10] I2C2_SOC_SDA
[8,9,10] I2C2_SOC_SCL
R208
R209
GND 1uF C235
R222 10K
[8] PA_MUTE
[1,3,8] I2S0_SOC_MCLK
[1,8] I2S2_SOC_BCLK
[8] I2S2_SOC_SDO
48K, 64Fs
R226
R223
R224
[1,8] I2S2_SOC_LRCK
R225
10K R227
I2C ADD:0XD8/0XD9
GND

L_1010_10UH_20%_CKD
L202

0.01uF C220 R212 3R3 GND
TP202 TP203
J201 EHK-4AL_CKD
TW- 1
TW+ 2
3
4

PVDD
C236 1000pF
0.1uF C237
1uF C238
C239 1000uF/25V
GND GND GND GND

1uF C228 GND
1uF C229 GND
0.01uF C230 R215 3R3 GND

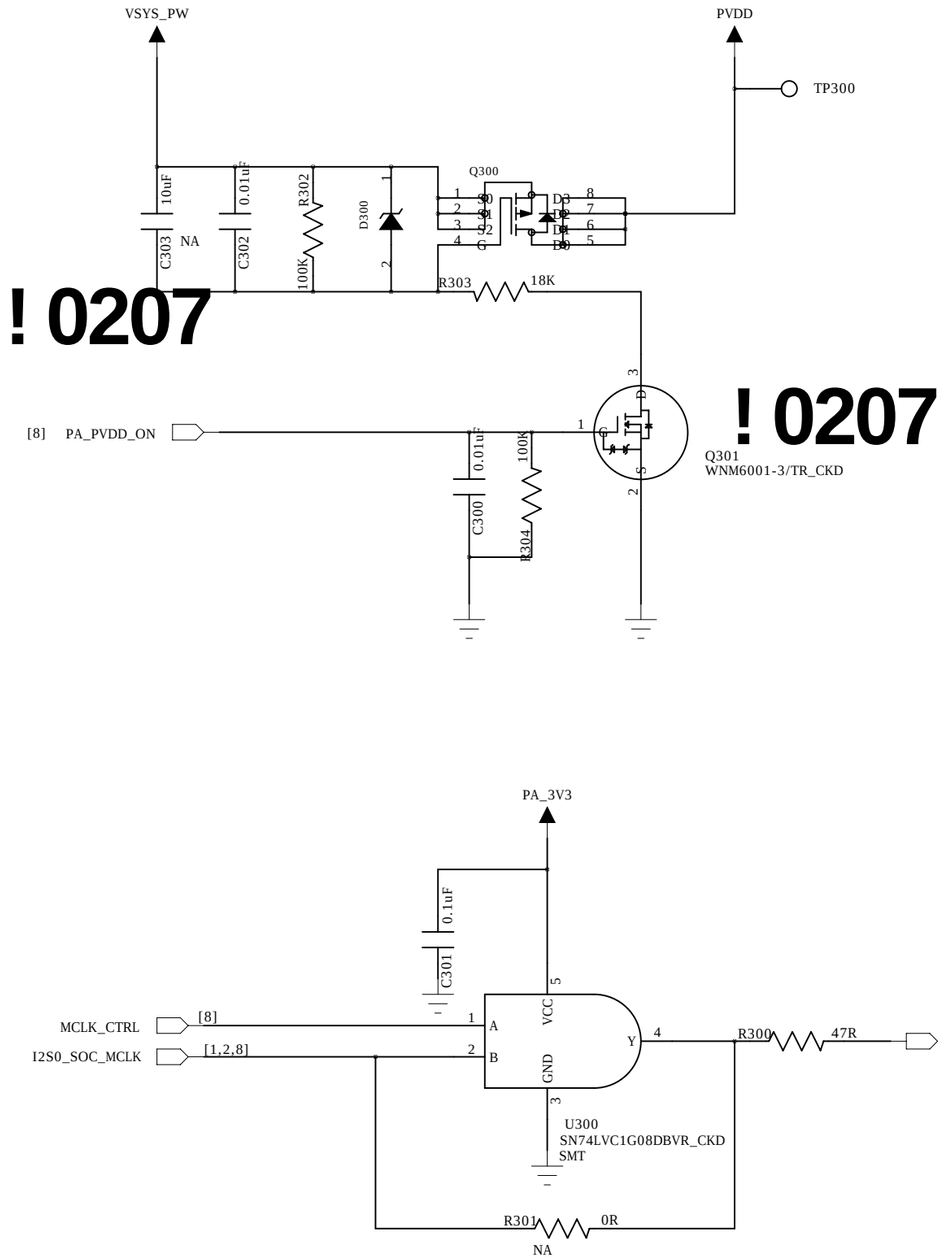
VSYS_3V3
PA_3V3
Q200
RE1C002ZPTL_CHECKED
TP204
100K R229
0.1uF C222
C221 4.7uF
PA_3V3_ON [8]
NA R221
GND GND

0.55Vrms input max

[11] TW_REF+
[11] TW_REF-
R216 24K 1uF C240
R217 24K 1uF C241
27K R218 GND
27K R219 GND

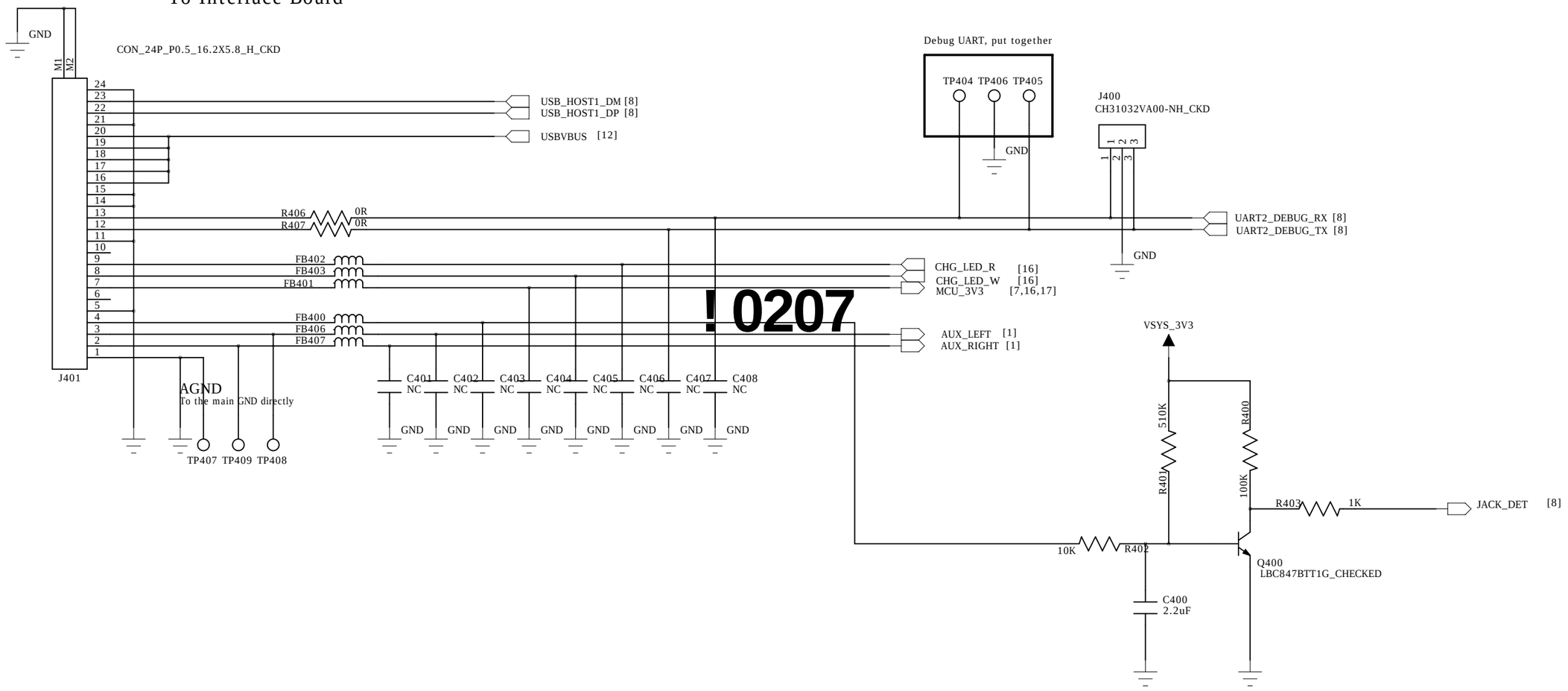
! 0207

Libratone A/S	PROJECT NAME	EGG II & ZIPP3	
LIBRATONE	DRAW NO	ES2	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 2 OF 18



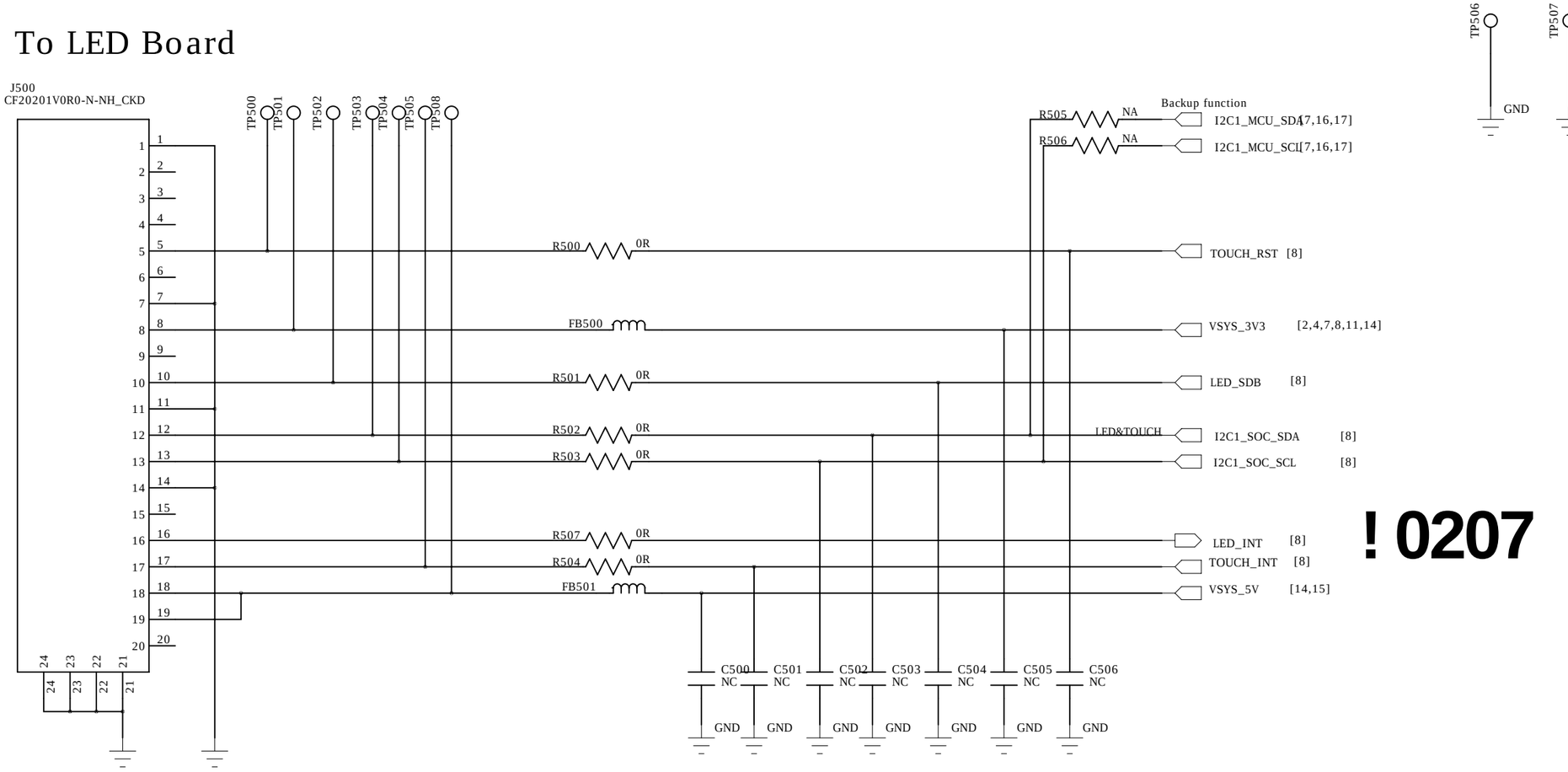
	EGG II	ZIPP3
U900	NA	ON
U1100	NA	ON
U300	NA	ON
R301	ON	NA
C206&C239	470uF	1000uF

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 3 OF 18



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 4 OF 18

To LED Board



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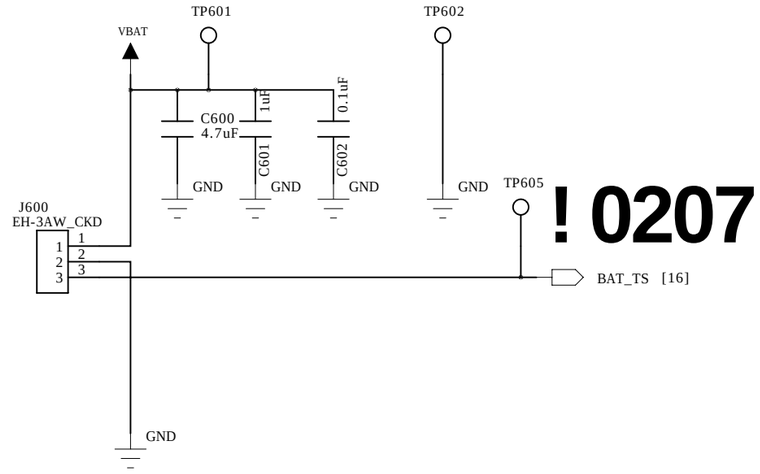
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 5 OF 18

µç³ØµçÁ¿×î´ó16.8V£¬×îÐ¡13.0V

MCU×î´óÉÑùµçÑ¹3.3V µç³ØÉÑùµçÑ¹Ë¥¼õ18dB



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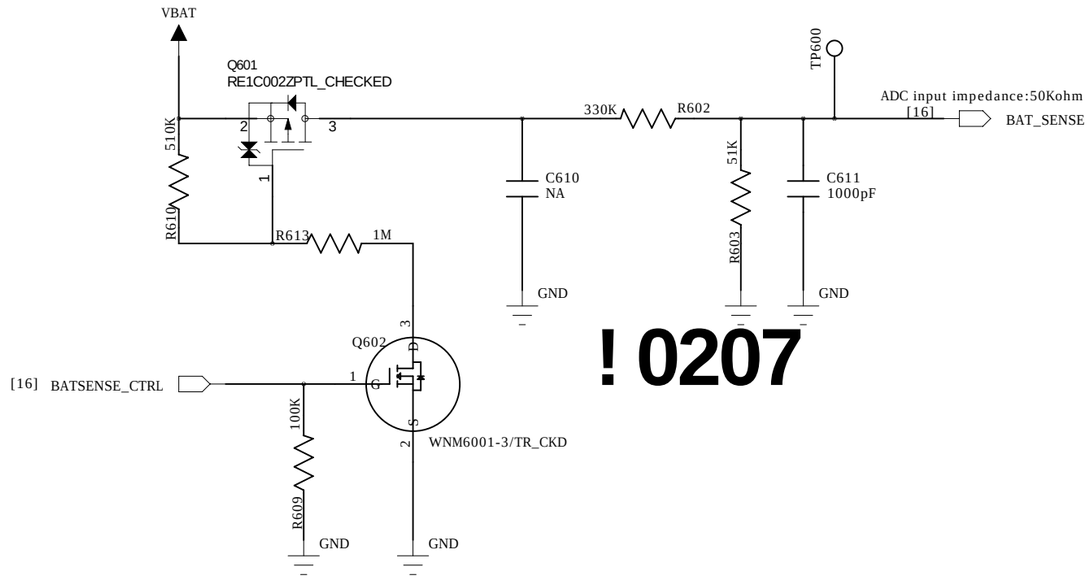

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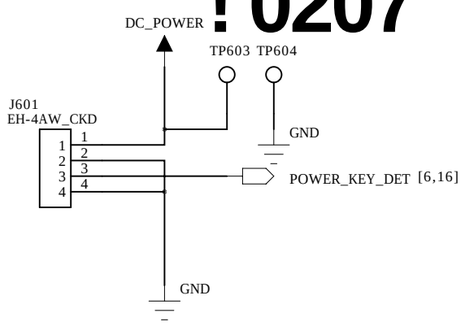

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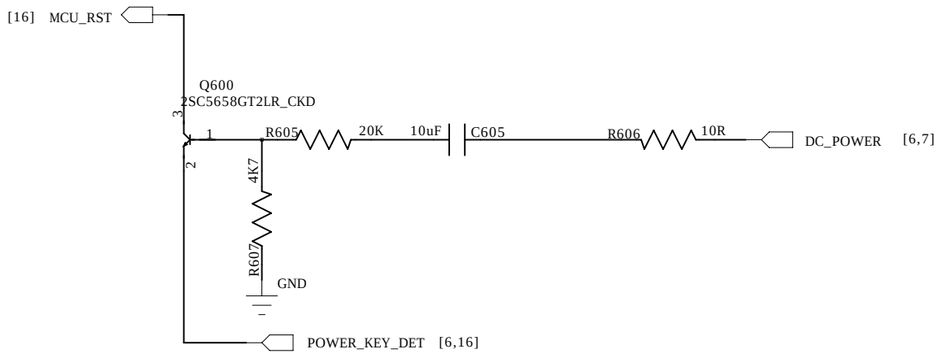


Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 6 OF 18

DC_POWER

Input:19V~21V

VSYS_PW

Q700 Q701

R700 0R02

3R3 R701

C713 4.7uF

750K R704

47K R705

0.1uF C717

C700 NC

C701 NC

1R R702

1R R703

C714 4.7uF

1uF C715

1uF C716

10uF C708 10uF C709 0.1uF C710 10uF C711 10uF C712

Q702 Q703

L700 2.2uH

10uF C702 0.1uF C703 10uF C704 10uF C705 10uF C706 10uF C707

DC_POWER,VSYS_PW,VBAT trace:3mm at least(pref

VBAT

VBAT Input:12V~17V

Q704

Current sense: diff trace

Current sense: diff trace

0.22uF C718 0.22uF C719

R706 0R

R707 1R

R709 1R

0R01 R708

C720 4.7uF

C721 NC

1uF C722

1uF C723

C724 22uF

MCU_3V3

CHG_VDD MCU_3V3

100K NC R710 R711

NC R712

510K R713

U700

GND_PAD 33

UGATE1 11

LGATE1 9

BOOT1 12

PHASE1 10

PHASE2 6

BOOT2 4

LGATE2 7

UGATE2 5

VSYS 3

CSOP 2

CSON 1

BGATE 32

VBAT 31

OTGPG/CMOUT 26

PSYS 30

CSIN 14

CSIP 15

ASGATE 13

ADP 16

ACIN 19

ACOK 24

PROCHOT# 23

AMON/BMON 29

BATGONE 25

OTGEN/CMIN 20

SCL 22

SDA 21

COMP 28

PROG 27

DCIN 17

VDD 18

VDDP 8

ISL9238HRTZ-T_CKD

VSYS_3V3

100K R714

To PW Ctrol ADP_PG [16]

[16] CHG_PROCHOT

[16] CHG_ABMON

ACIN threshold>0.8V(input>15V)

R716 0R

R717 0R

ADC OUT:Adapter/Battery Current Monitor

R715 1K

R718 0R

CHG_PG

TP700

CHG_PSYSMON [16]

Power output monitor

20W*1.44uA*100K=2.88V

100K R719

C725 NC

C726 4700pF

1000pF C727

0R R720

NC R721

Default (Input: 19V/0.5A)

I2C1_MCU_SCL [5,16,17]

I2C1_MCU_SDA [5,16,17]

R722 0R

R723 0R

DC_POWER

VSYS_PW

CHG_VDD

D700 RB520CS-30GT2RA_CKD

D701 RB520CS-30GT2RA_CKD

698R R724

215K R725

C728 NC

C729 100pF

C730 0.022uF

R726 4R7

0.1uF C731

C732 4.7uF

C733 4.7uF

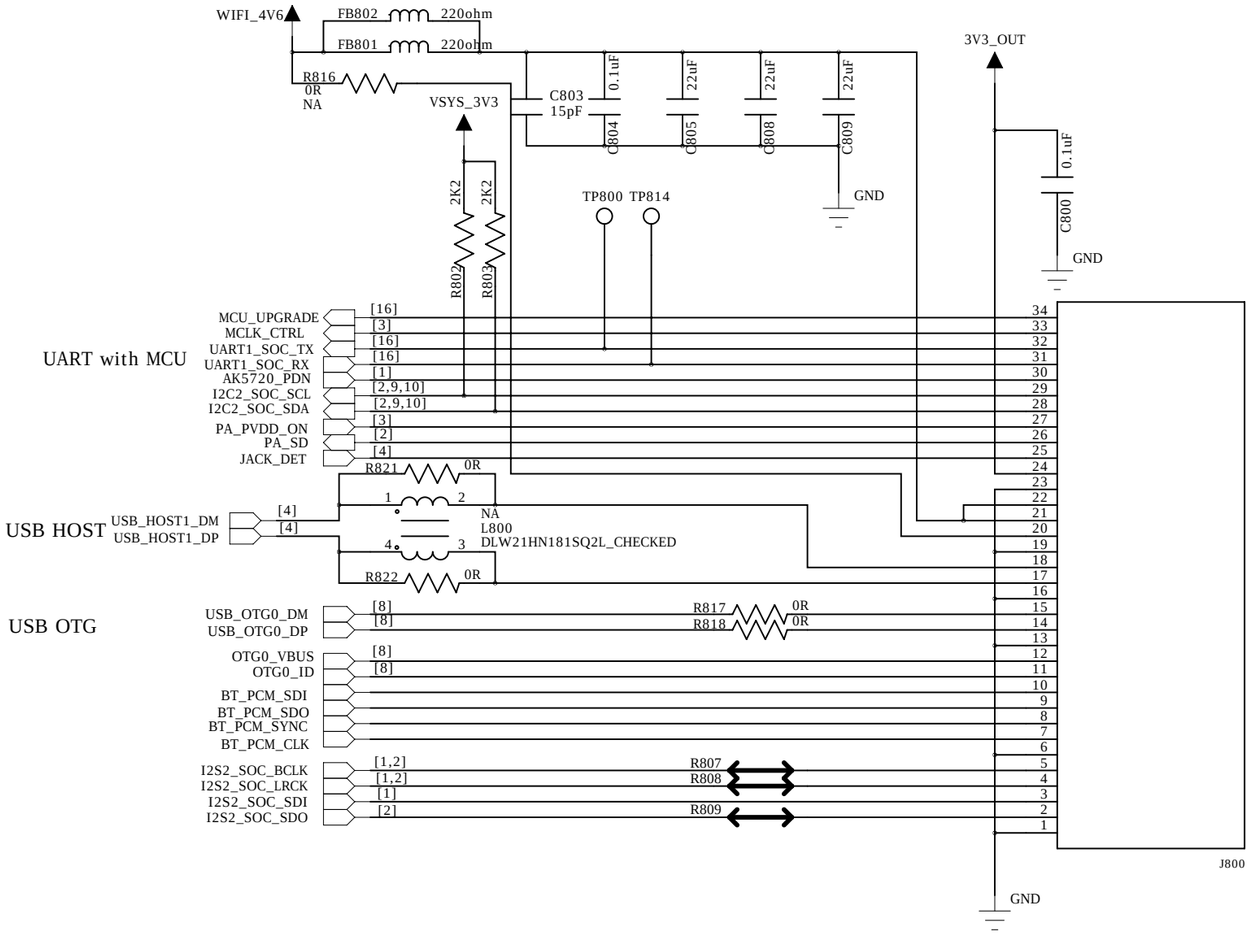
1uF C734

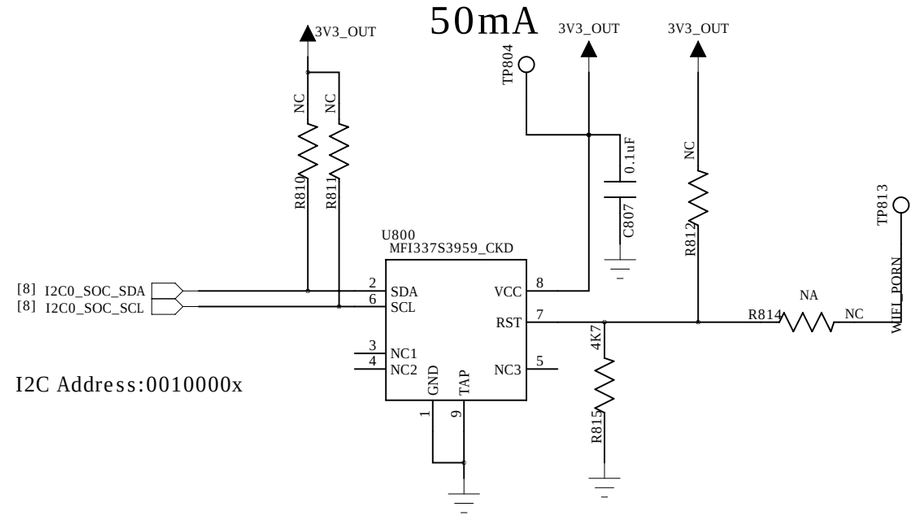
R727 3R3

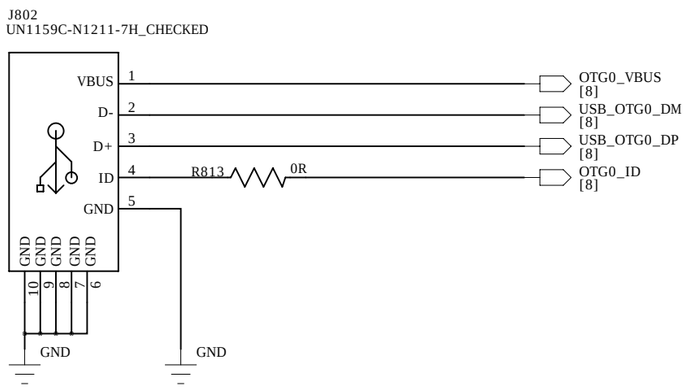
1uF C735

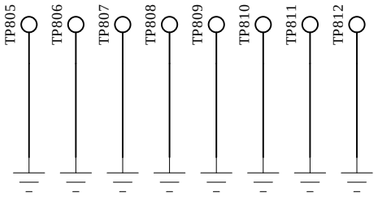
PROG Default: 4cells,733KHz,default 0.476A charging

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 7 OF 18







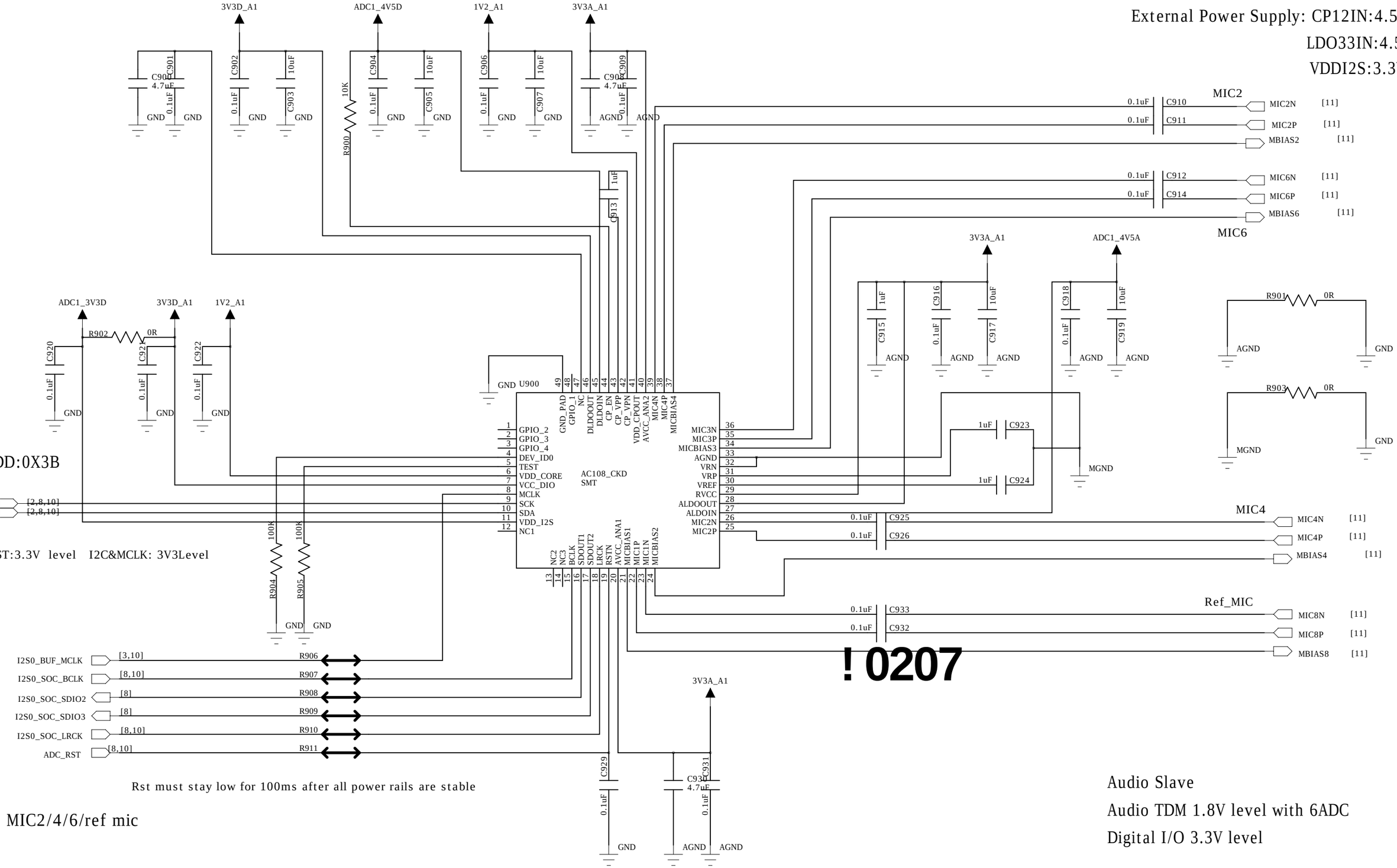


Libratone A/S	PROJECT NAME	EGG II & ZIPP3	
	DRAW NO	ES2	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 8 OF 18

External Power Supply: CP12IN:4.5V

LDO33IN:4.5V

VDDI2S:3.3V



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 9 OF 18

External Power Supply: CP12IN:4.5V

LDO33IN:4.5V

VDDI2S:3.3V

I2C ADD:0X35

TDM&RST:3.3V level I2C&MCLK: 3V3Level

Rst must stay low for 100ms after all power rails are stable

MIC1/3/5/ref sig

For I2S Encoding Mode

input referen

Audio Slave

Audio TDM 1.8V level with 6ADC

Digital I/O 3.3V level

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
LIBRATONE		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 10 OF 18

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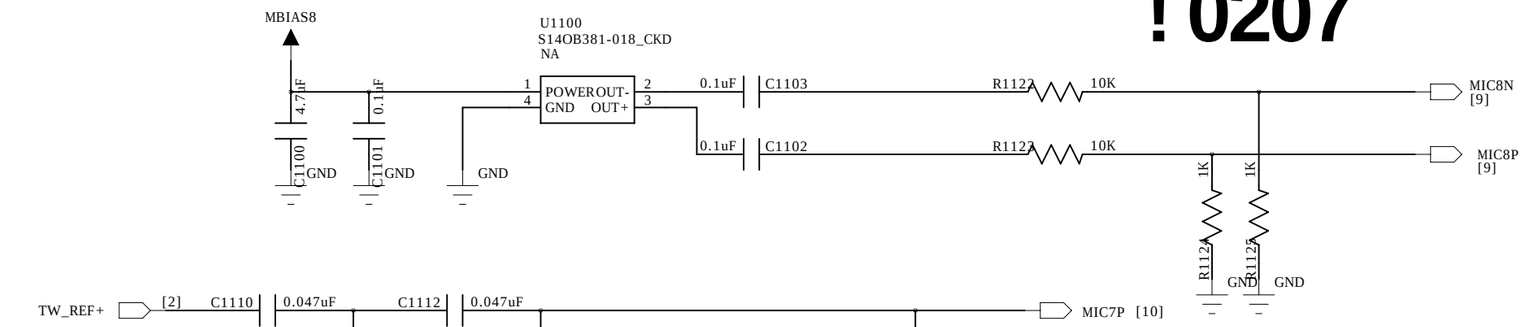

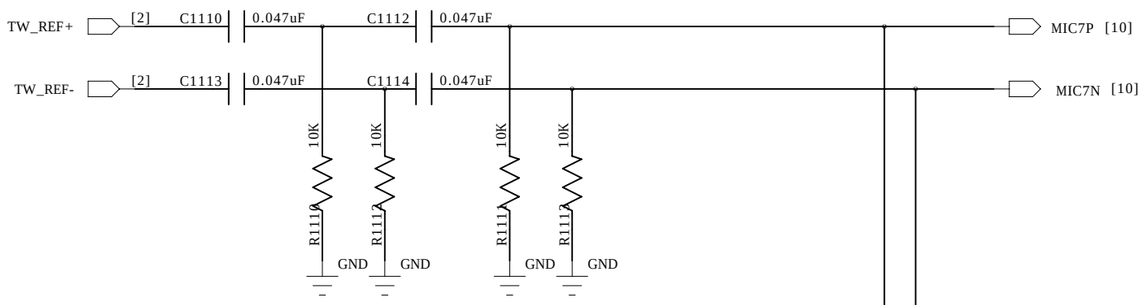

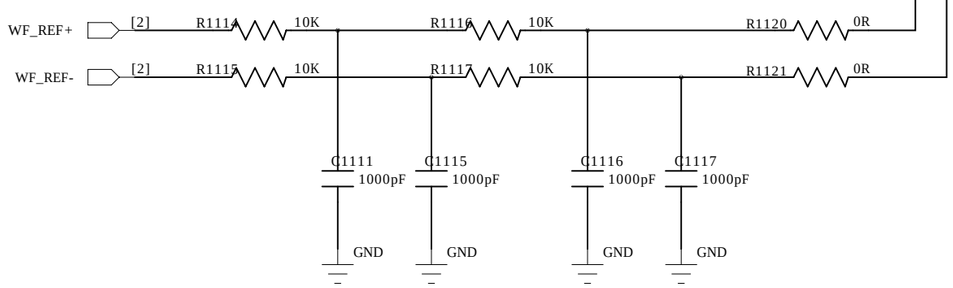

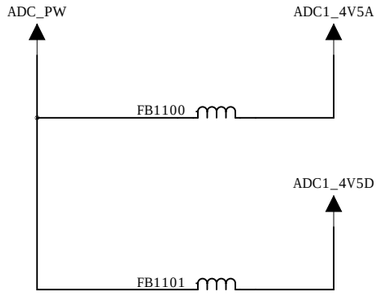

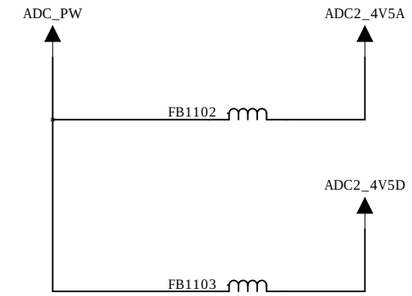

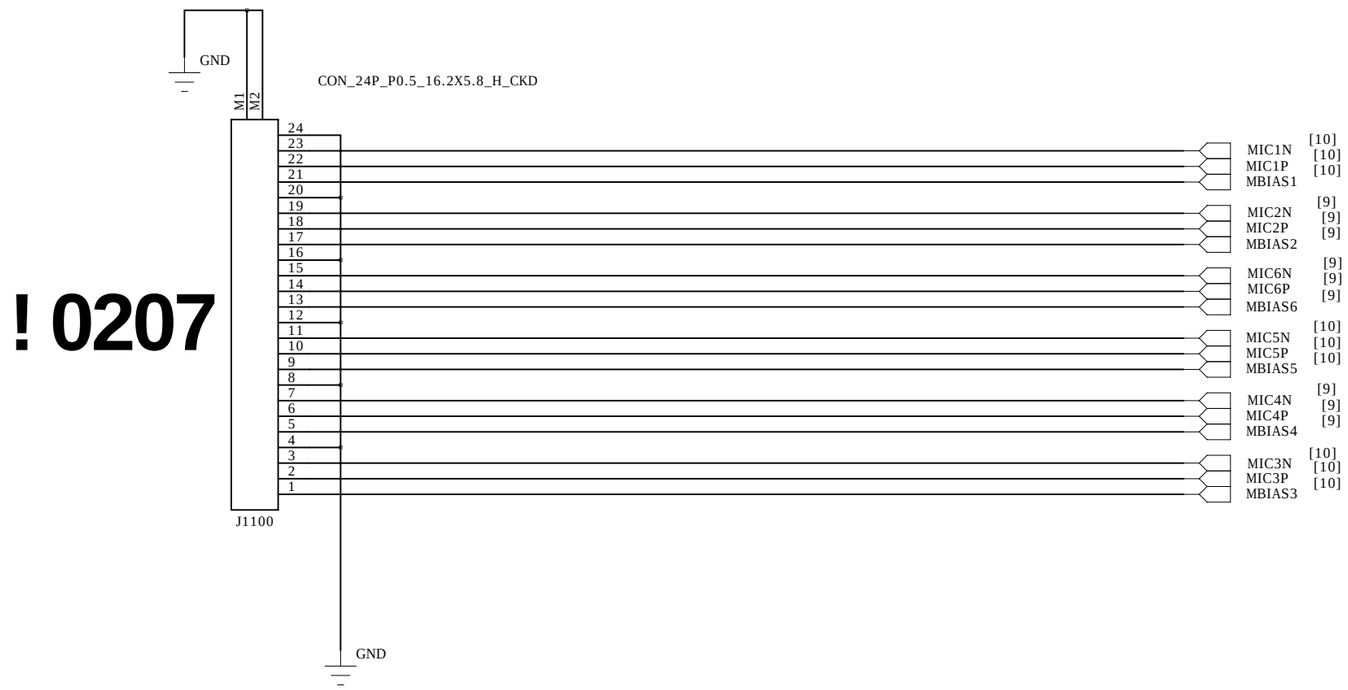

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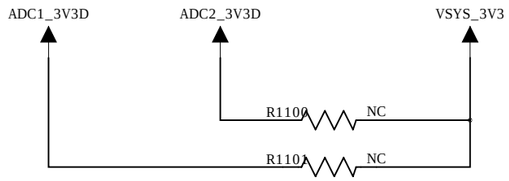
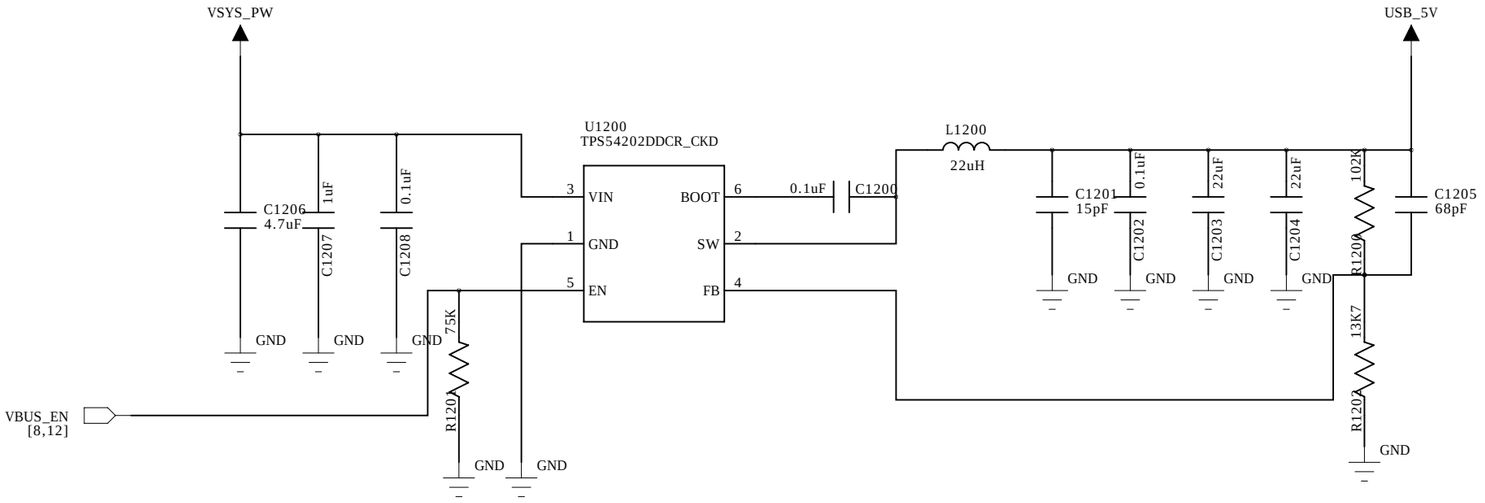
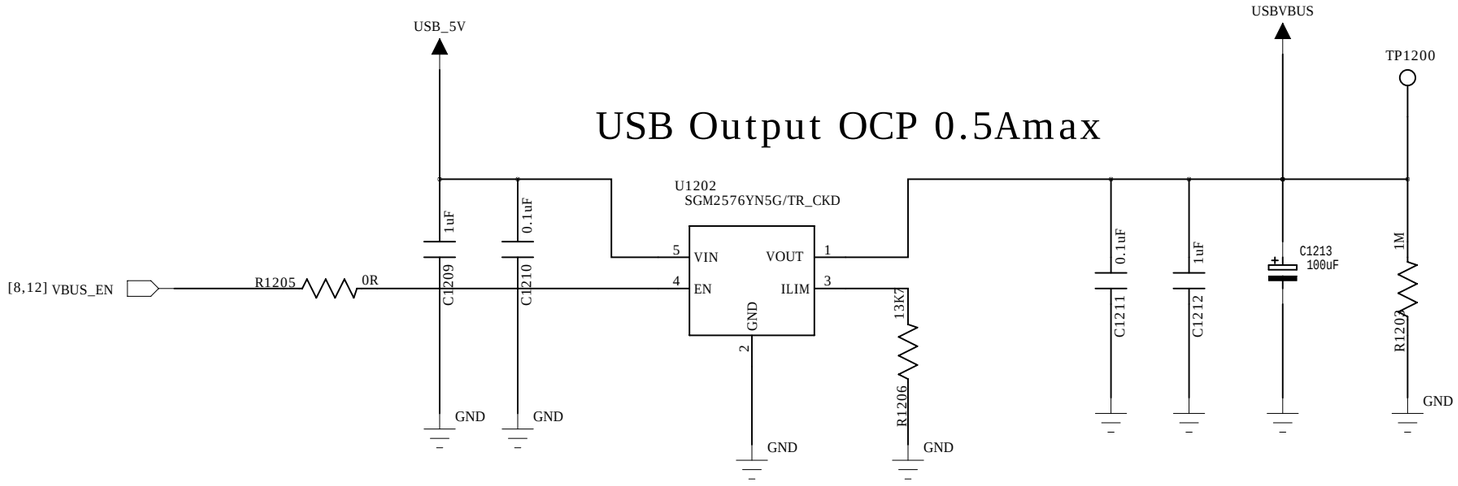


U900-ADC1	Aux_Right/SPK_TW
ADC2	MIC4
ADC3	MIC6
ADC4	MIC2
U1000-ADC1	Aux_Left/SPK_WF
ADC2	MIC3
ADC3	MIC5
ADC4	MIC1

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 11 OF 18





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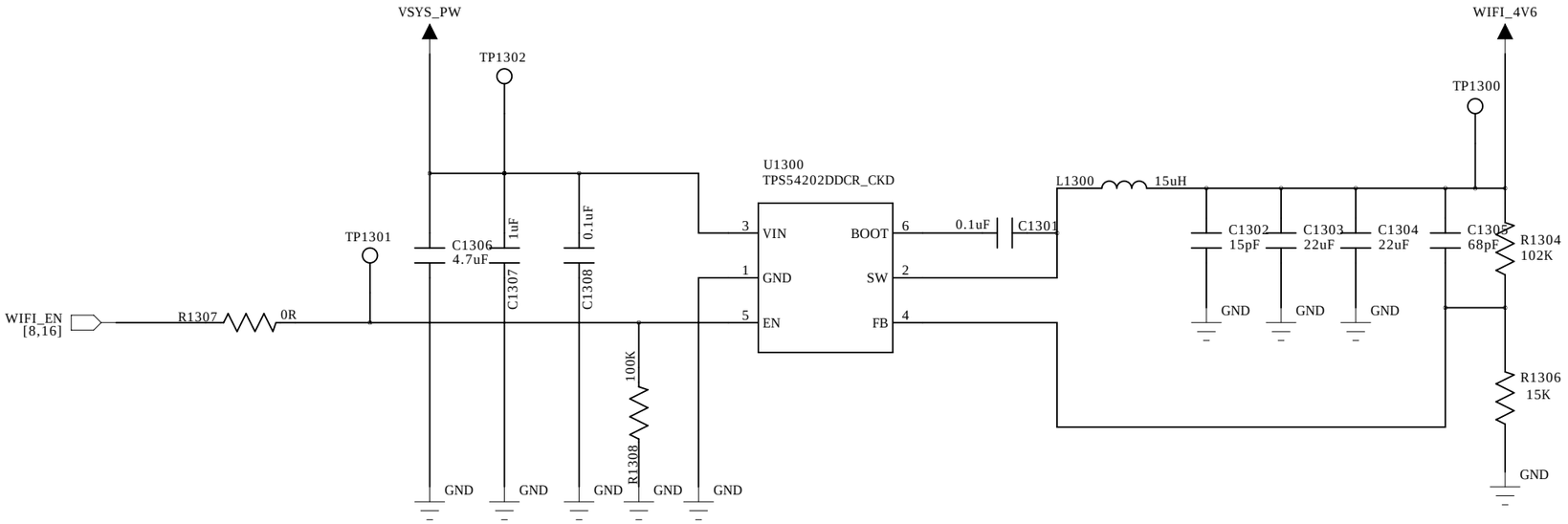
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 12 OF 18



P1300

FIDUCIAL_BOTH_CHECKED

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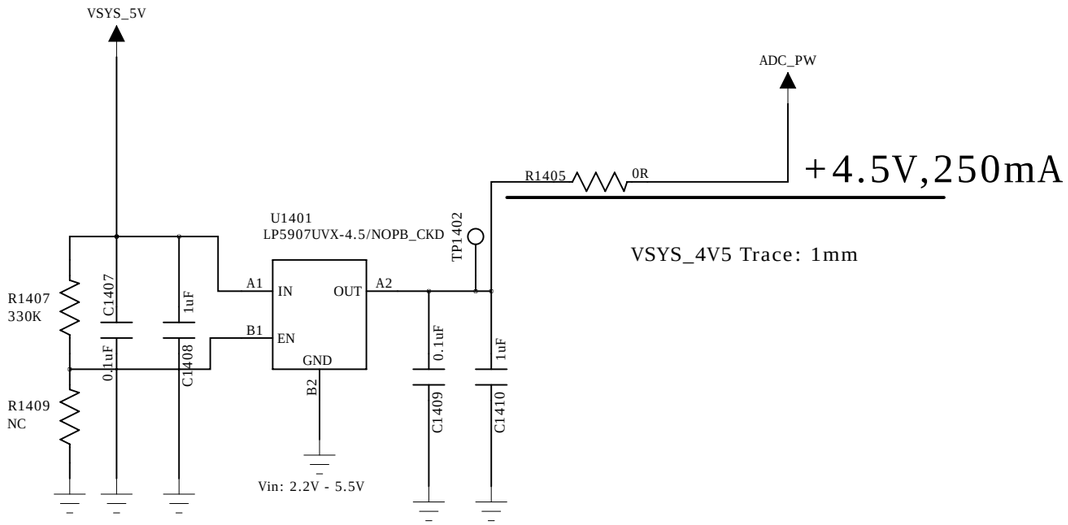
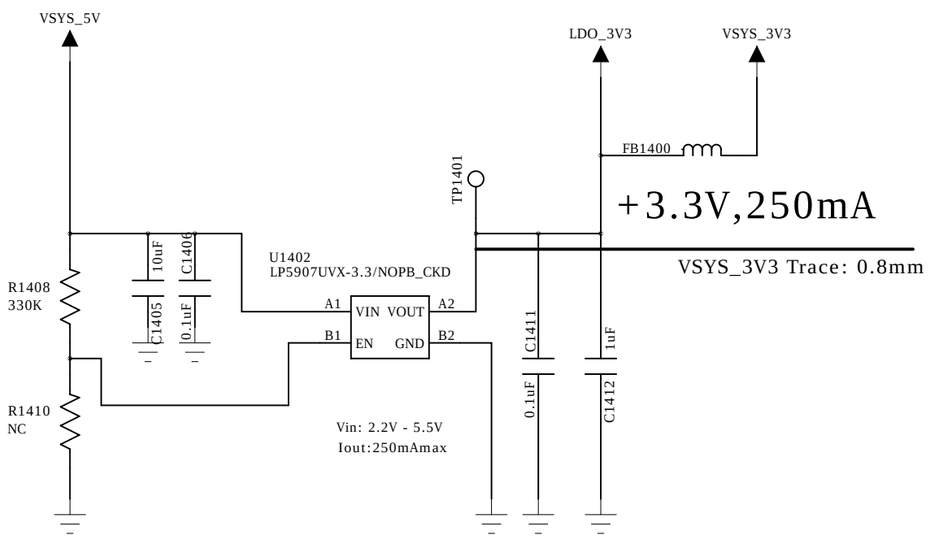
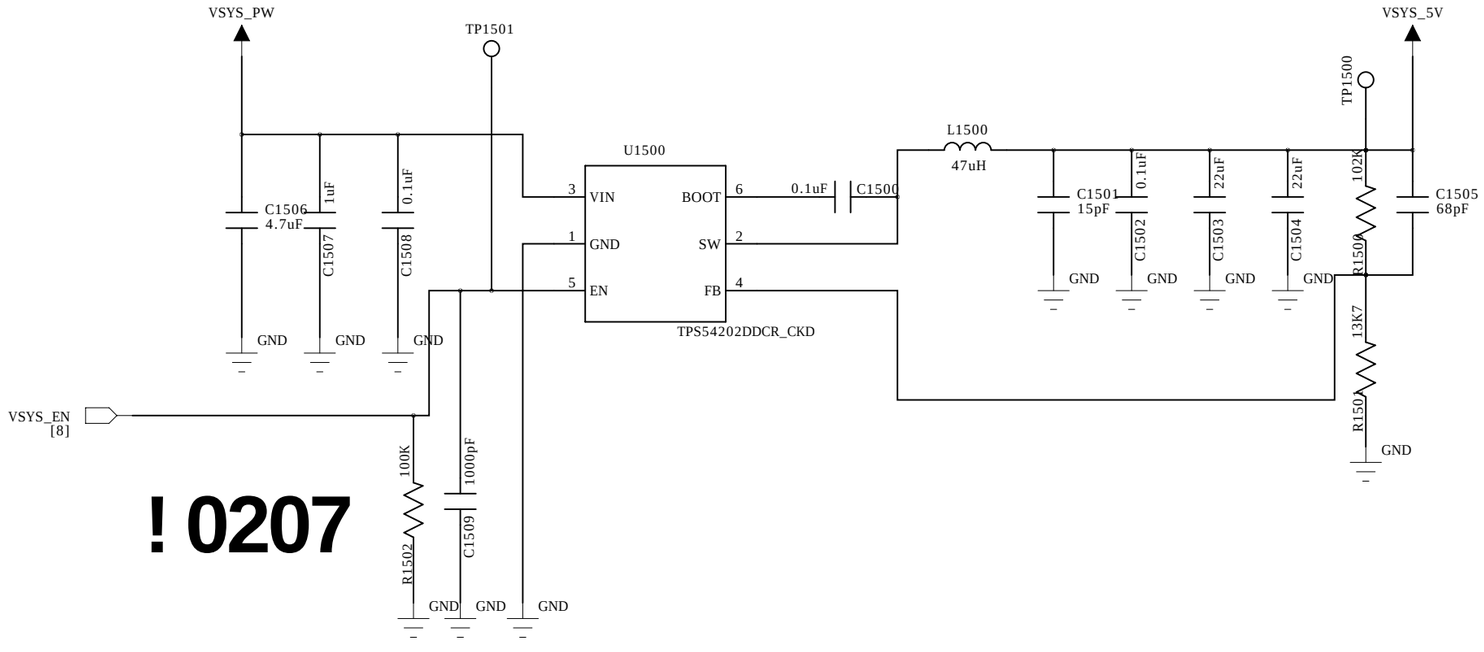
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 13 OF 18





Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 14 OF 18



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 15 OF 18

MCU_UPGRADE [8]
I2C1_MCU_SCL [5,7,17]
I2C1_MCU_SDA [5,7,17]
BATSENSE_CTRL [6]
MCU_RST [6,16]
MCU_CTRL [8]
BAT_SENSE [6]
BAT_TS [6,16]
CHG_ABMON [7]
CHG_PSYSMON [7]
CHG_PROCHOT [7]

MCU_3V3
4K7 R1618
4K7 R1619
100K R1620
GND
2K2 R1615
Y1600 32.768kHz
18pF C1613
18pF C1612
TP1603
Q1600 WNM6001-3/TR_CKD
100K R1622
C1600 0.1uF
0.1uF C1615
C1614 4.7uF
R1618 0R
R1619 0R
R1614 0R

U1600 STM32L011G4U6TR_CKD
PB9-BOOT0 1
PC14-OSC32_IN 2
PC15-OSC32_OUT 3
NRST 4
VDDA 5
PA0-CK_IN 6
PA1 7
PA2 8
PA3 9
PA4 10
PA5 11
PA6 12
PA7 13
PB0 14
PB1 15
VSS 16
VDD 17
PA8 18
PA9 19
PA10 20
PA13 21
PA14 22
PA15 23
PB3 24
PB4 25
PB5 26
PB6 27
PB7 28

TP1601 TP1602
C1607 1000pF
D1600 RB520CS-30GT2RA_CKD
C1602 0.1uF
1uF C1601

UART2_MCU_RX R1612 0R [8] UART1_SOC_TX
UART2_MCU_TX R1613 0R [8] UART1_SOC_RX

G_INT1 [17]
POWER_KEY_DET [6]
WIFI_EN [8,13]
MCU_SWCLK [16]
MCU_SWDIO [16]
MCU_32KOUT [8]
CHG_LED_R [4]
CHG_LED_W [4]
BATTS_CTRL [16]
ADP_PG [7]

! 0207
! 0207

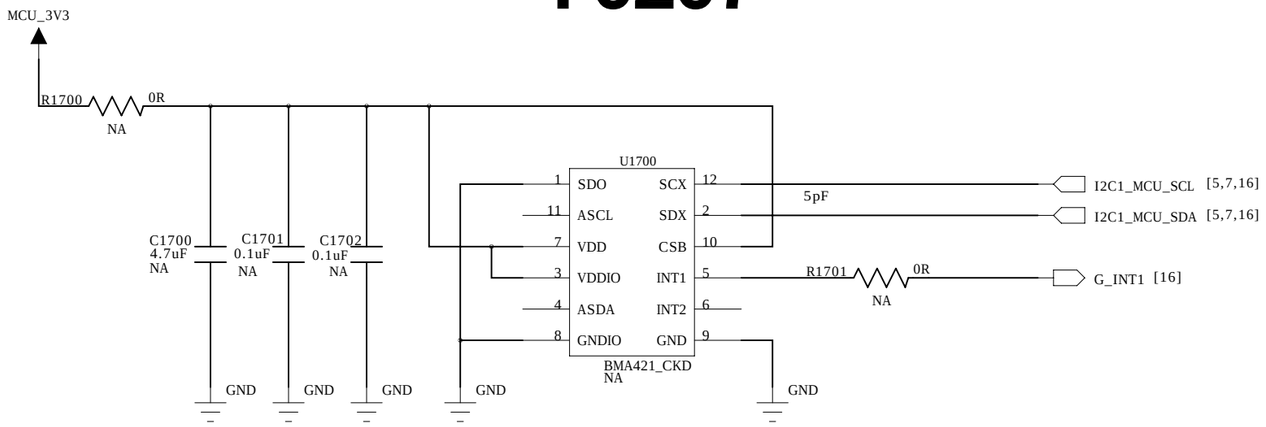
VSYS_PW
! 0207
U1601 SGM2203-3.3YK3G/TR_CKD
VIN VOUT GND
1uF C1610
C1611 NA
TP1600
R1621 0R
C1604 0.1uF
1uF C1605
! 0207

BATTS_CTRL [16]
47K R1616
BAT_TS [6,16]
R1617 30K

J1600 CH31052VA00-NH_CKD
MCU_SWDIO [16]
MCU_SWCLK [16]
MCU_RST [6,16]

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 16 OF 18

! 0207



Active current @ Performance mdoe : 160 uA
Suspend mode ; 2.5uA
Lower power mode : 14uA

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
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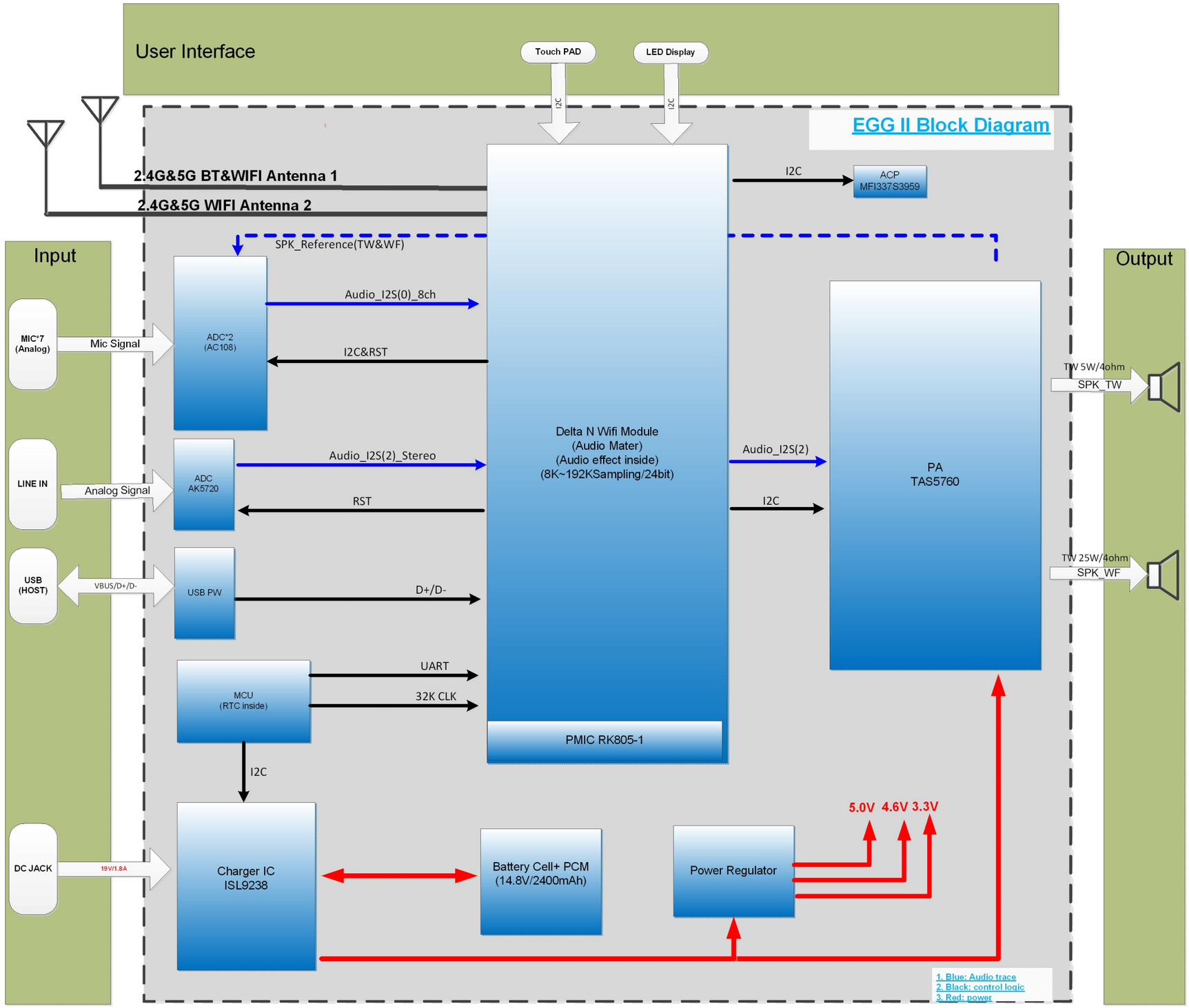
! 0207

EGG II Block Diagram



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 18 OF 18