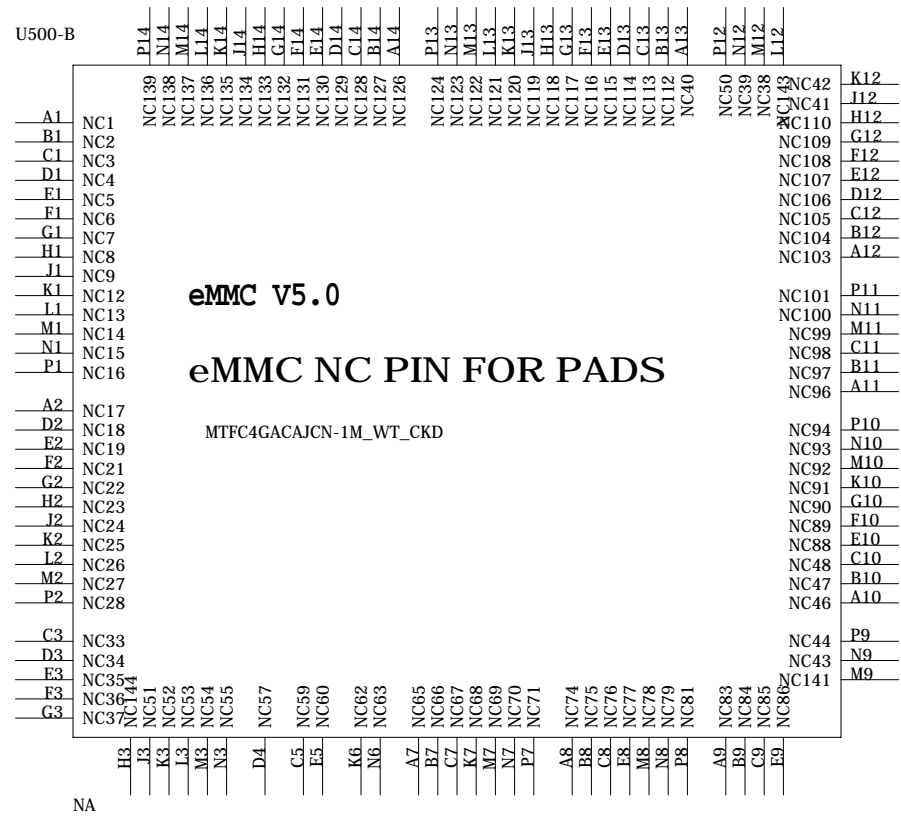
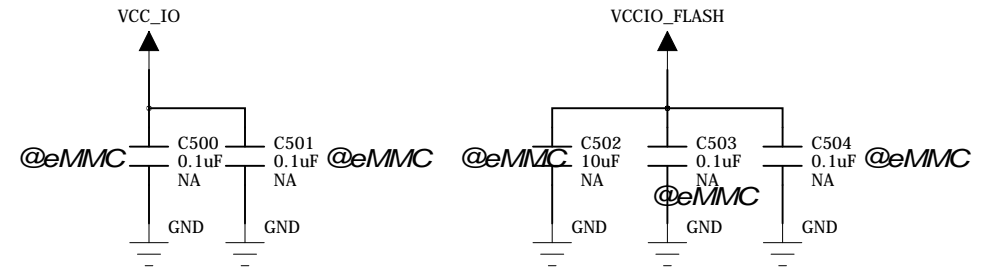
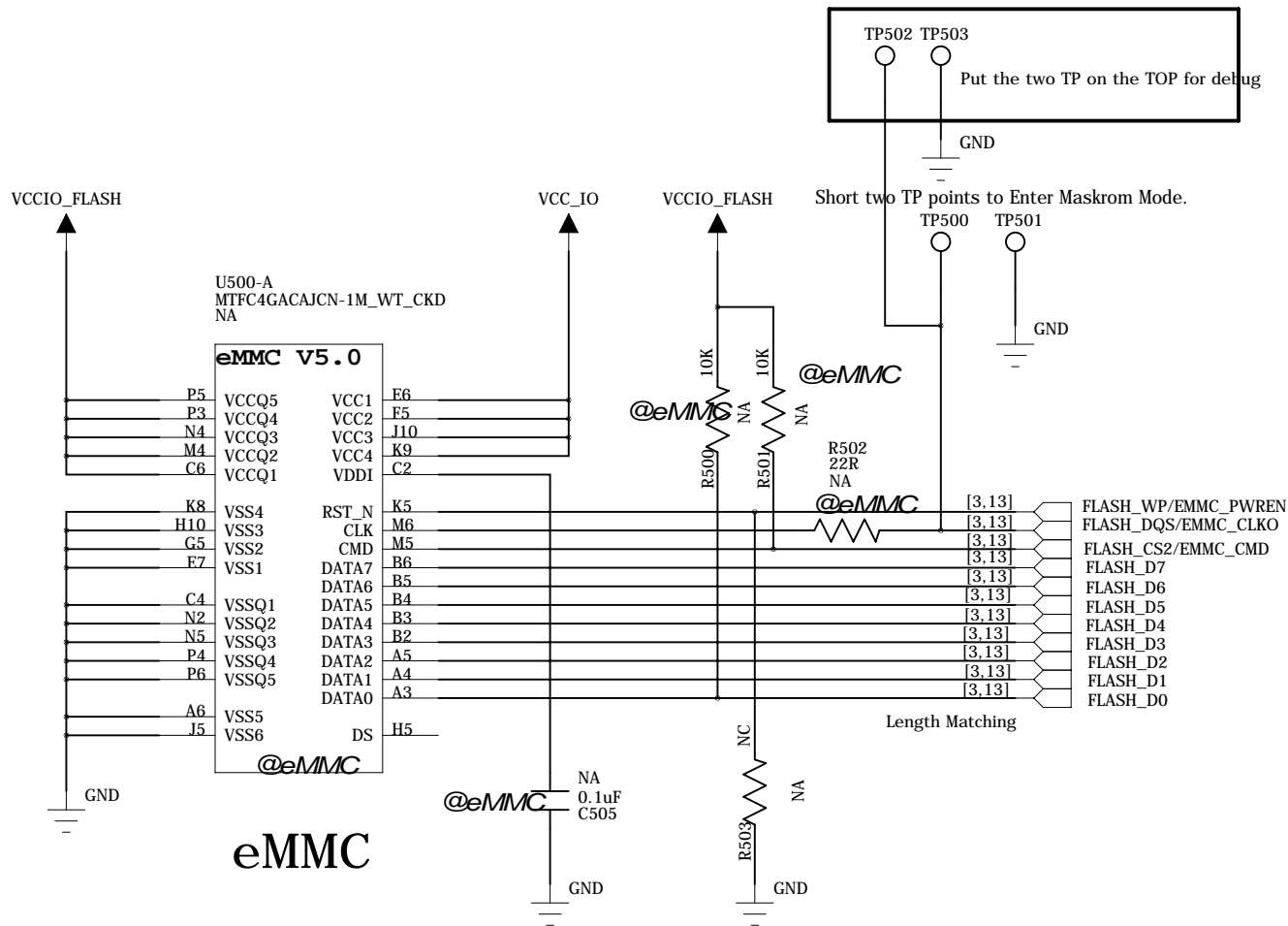

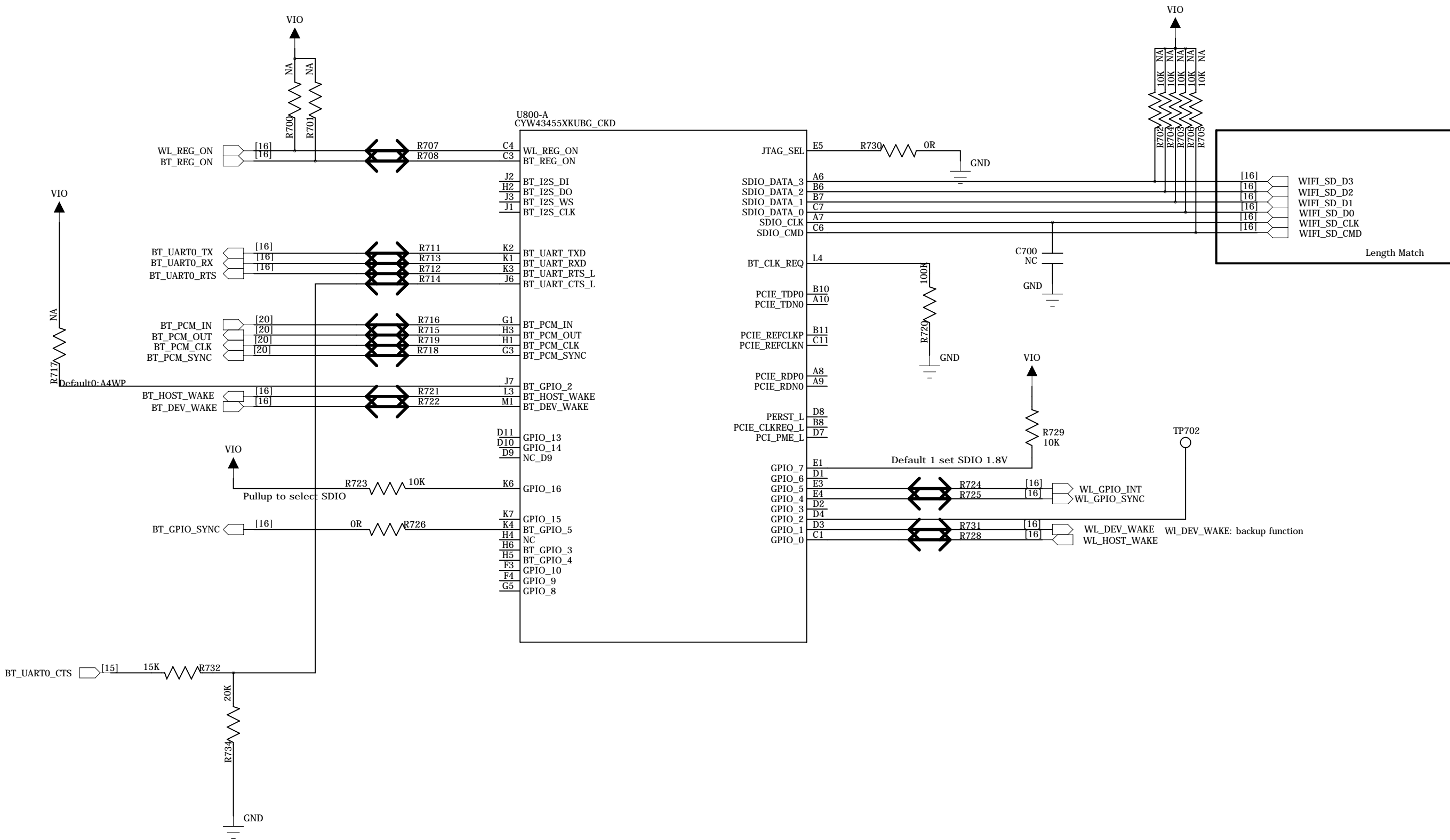




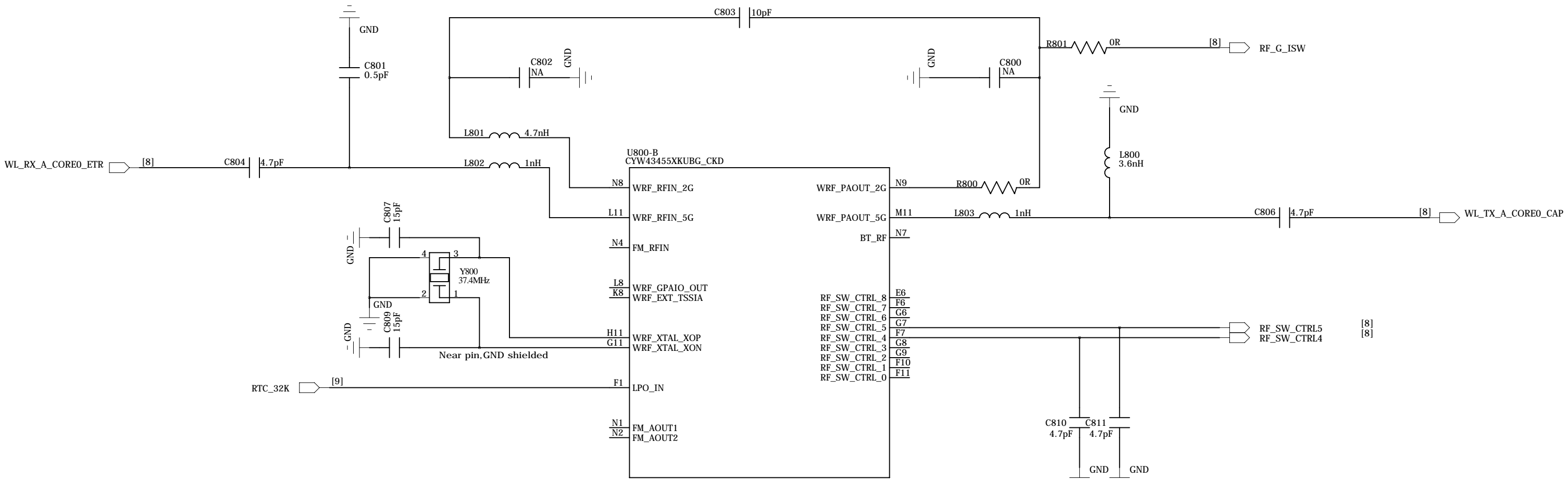
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		DESCRIPTION	WiFiBT Module
APPROVAL	CHECK	DESIGN	REV.
<Approved By>	<Checked By>	Danny Han	R3
DATE	DATE	DATE	SHEET
<Approved Date>	<Checked Date>	2017/12/26	2 OF 22



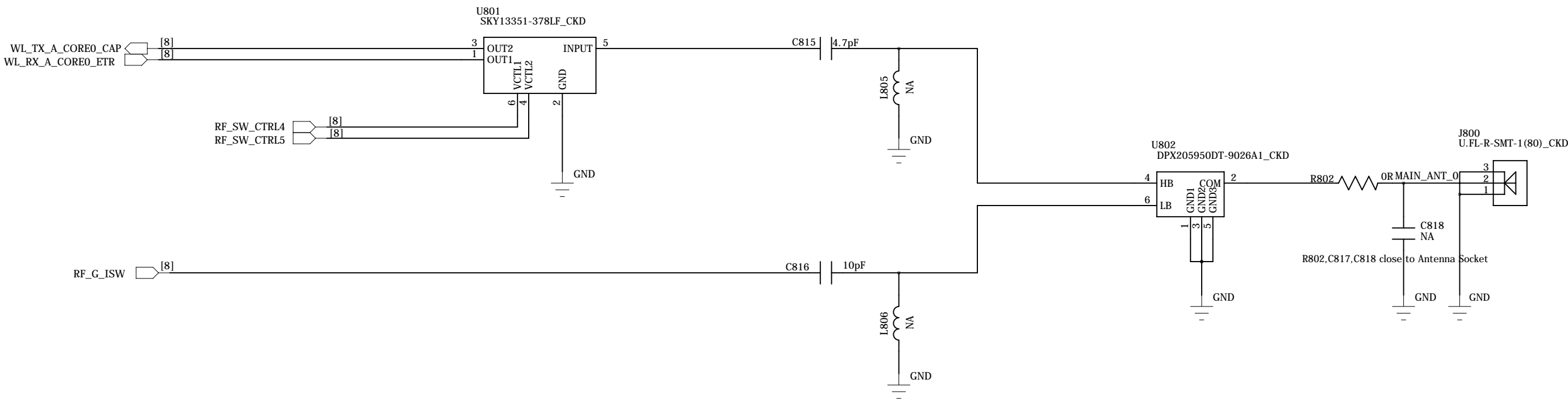
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DATE <Approved Date>	DATE <Checked Date>	DATE 2017/12/26	SHEET	5	OF 22



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DATE <Approved Date>	DATE <Checked Date>	DATE 2017/12/26	SHEET 7 OF 22



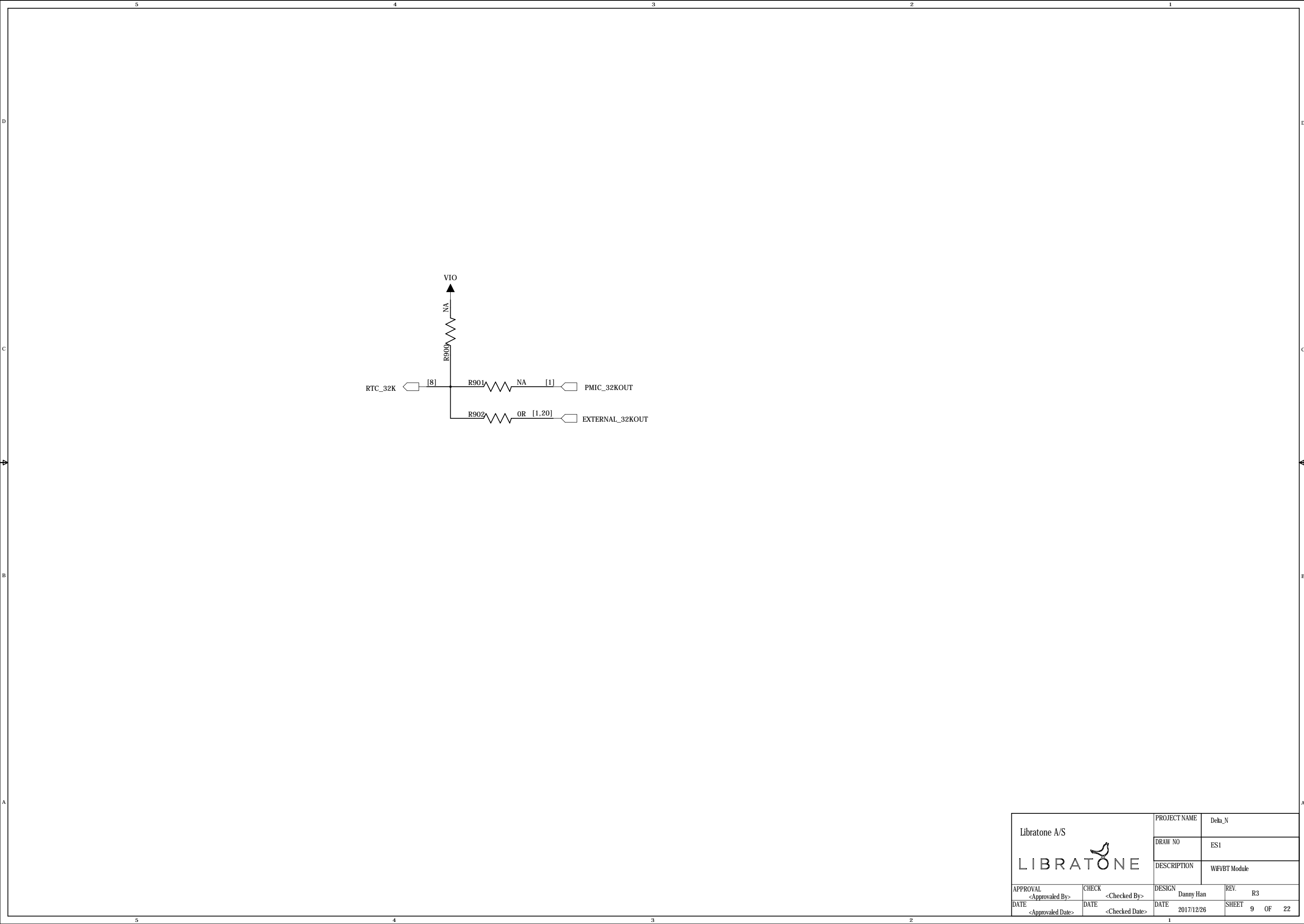
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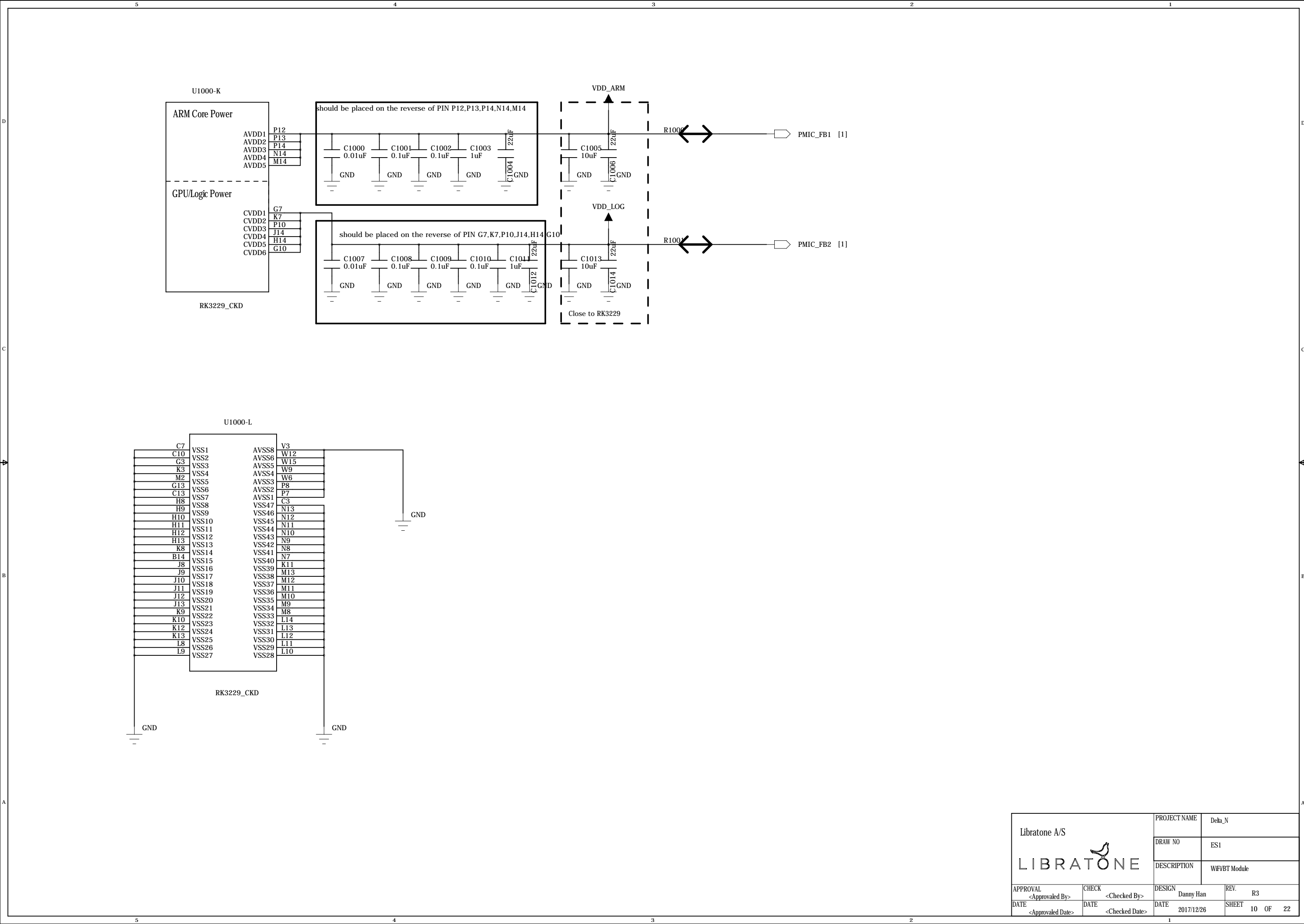
A-Band RF T/R Switch Truth Table

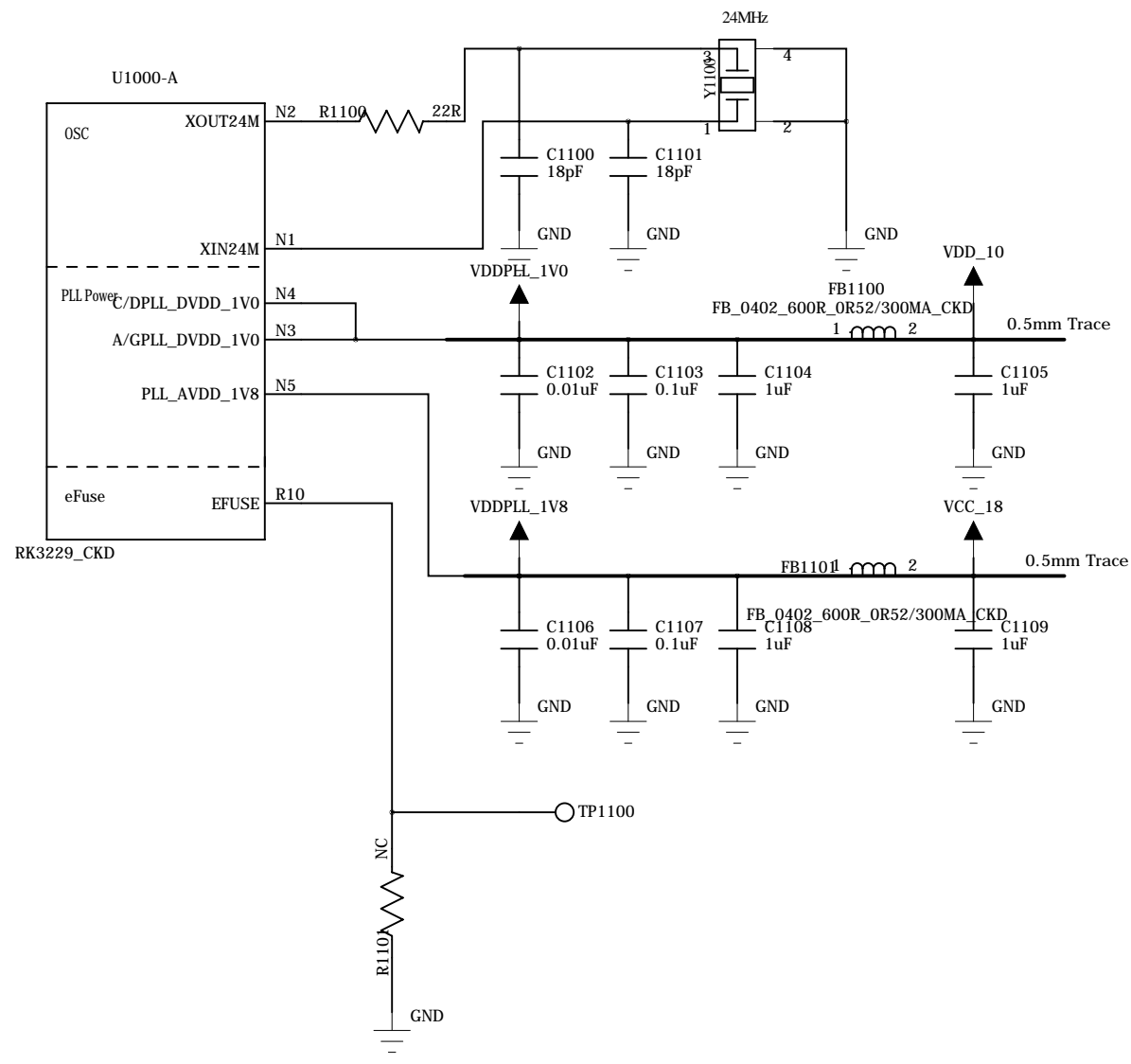
	RF_SW_CTRL4	RF_SW_CTRL5
WLAN_TX	H	L
WLAN_RX	L	H


<div>Libratone A/S</div> <div>LIBRATONE</div>		PROJECT NAME	Delta_N
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		DESCRIPTION	WiFi/BT Module
		DESIGN	Danny Han
APPROVAL	CHECK	DATE	REV.
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DATE	DATE	SHEET	8 OF 22
<Approved Date>	<Checked Date>		

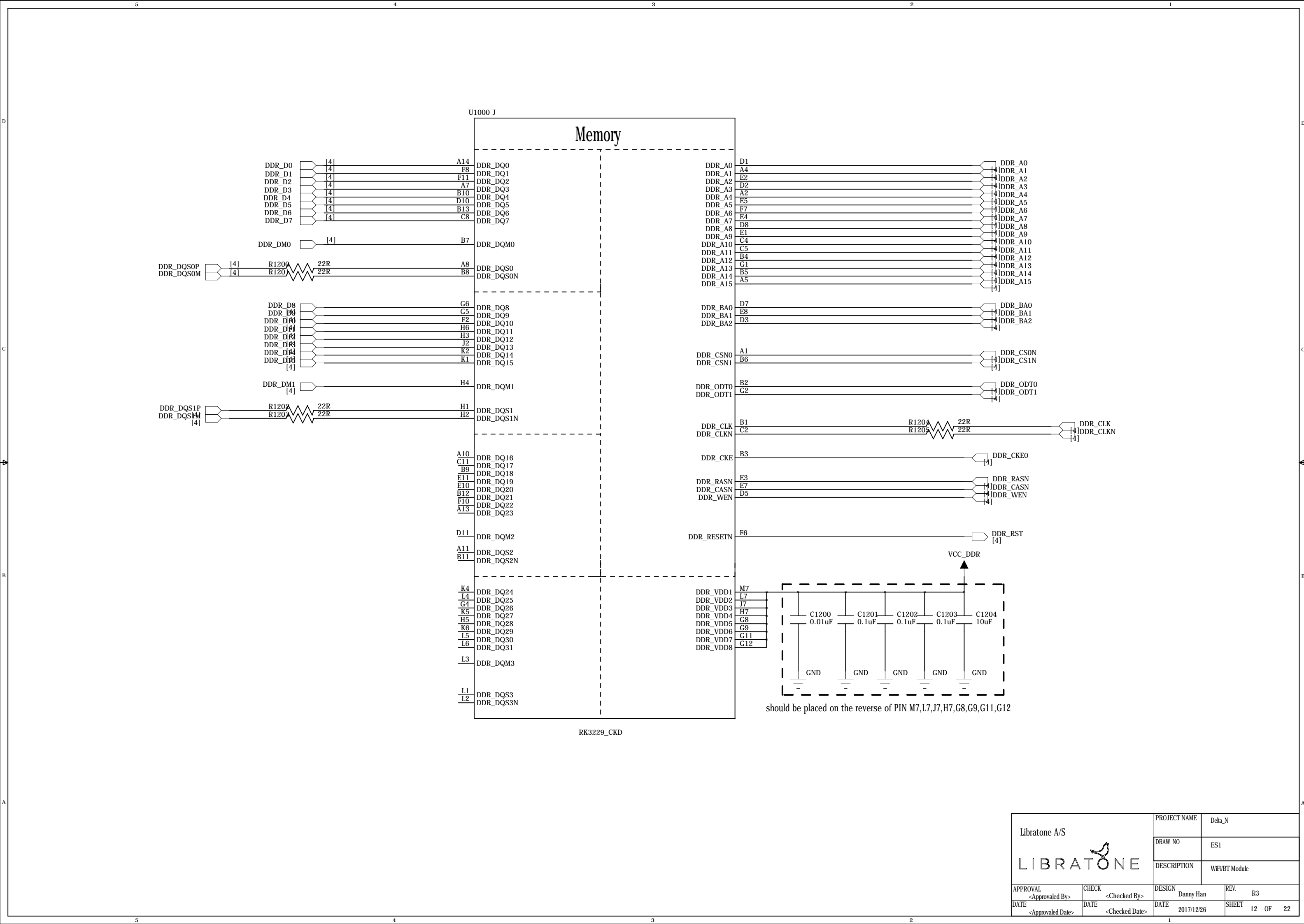


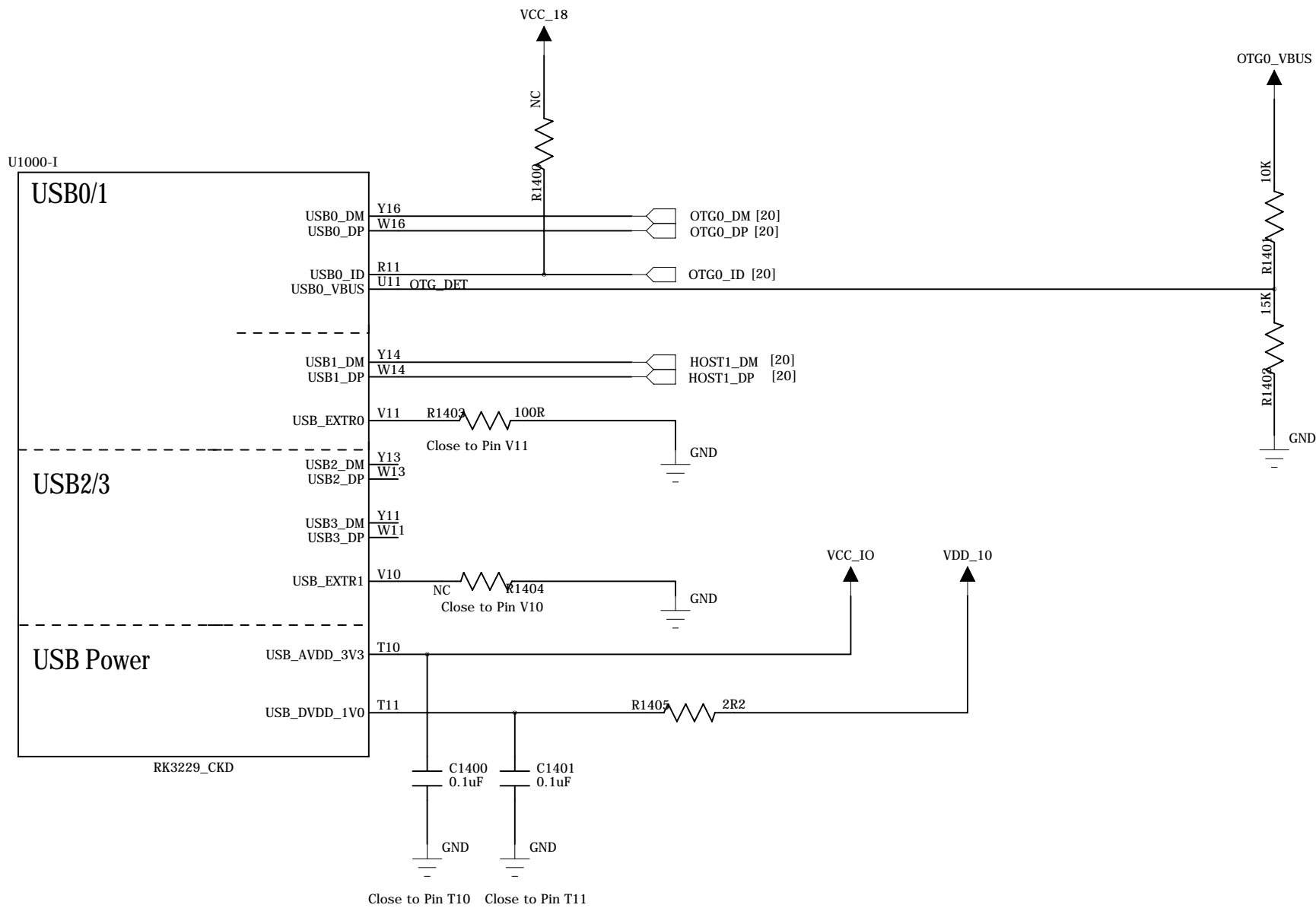
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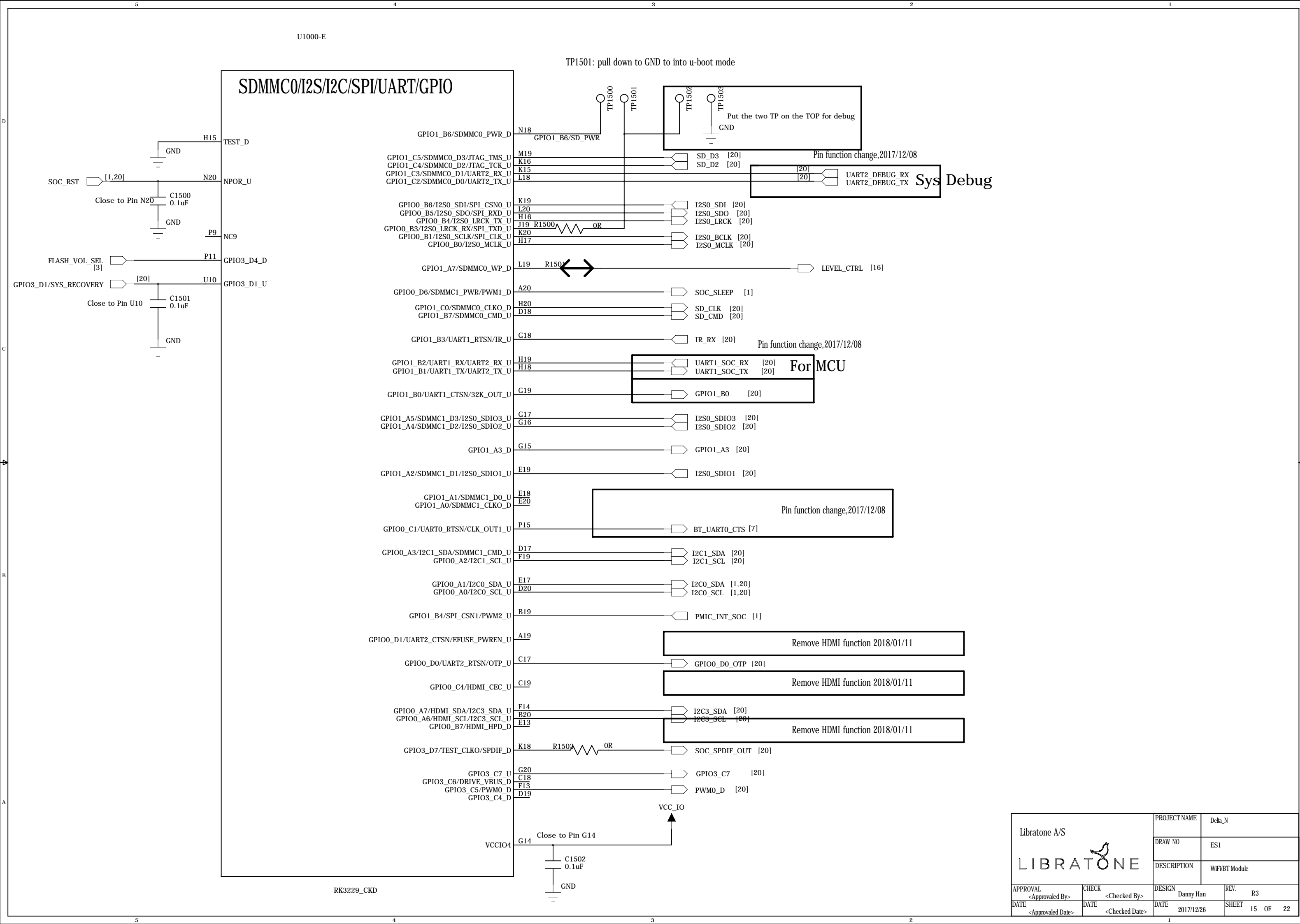


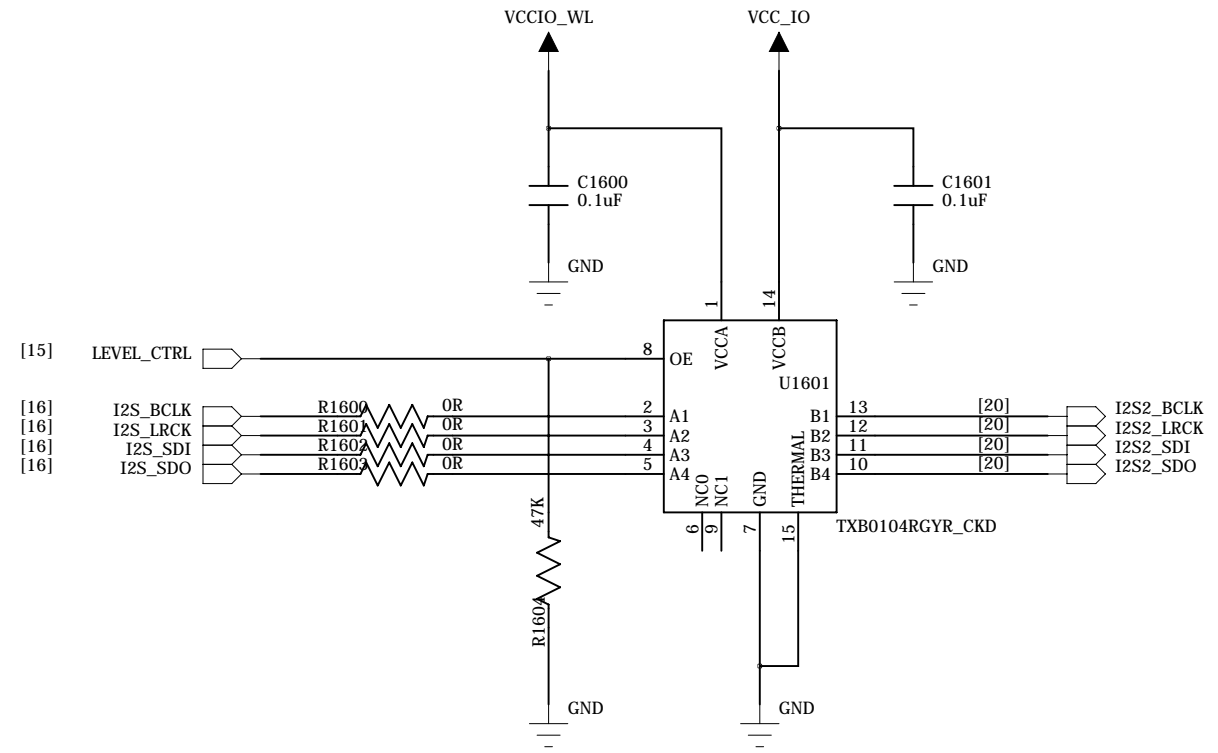
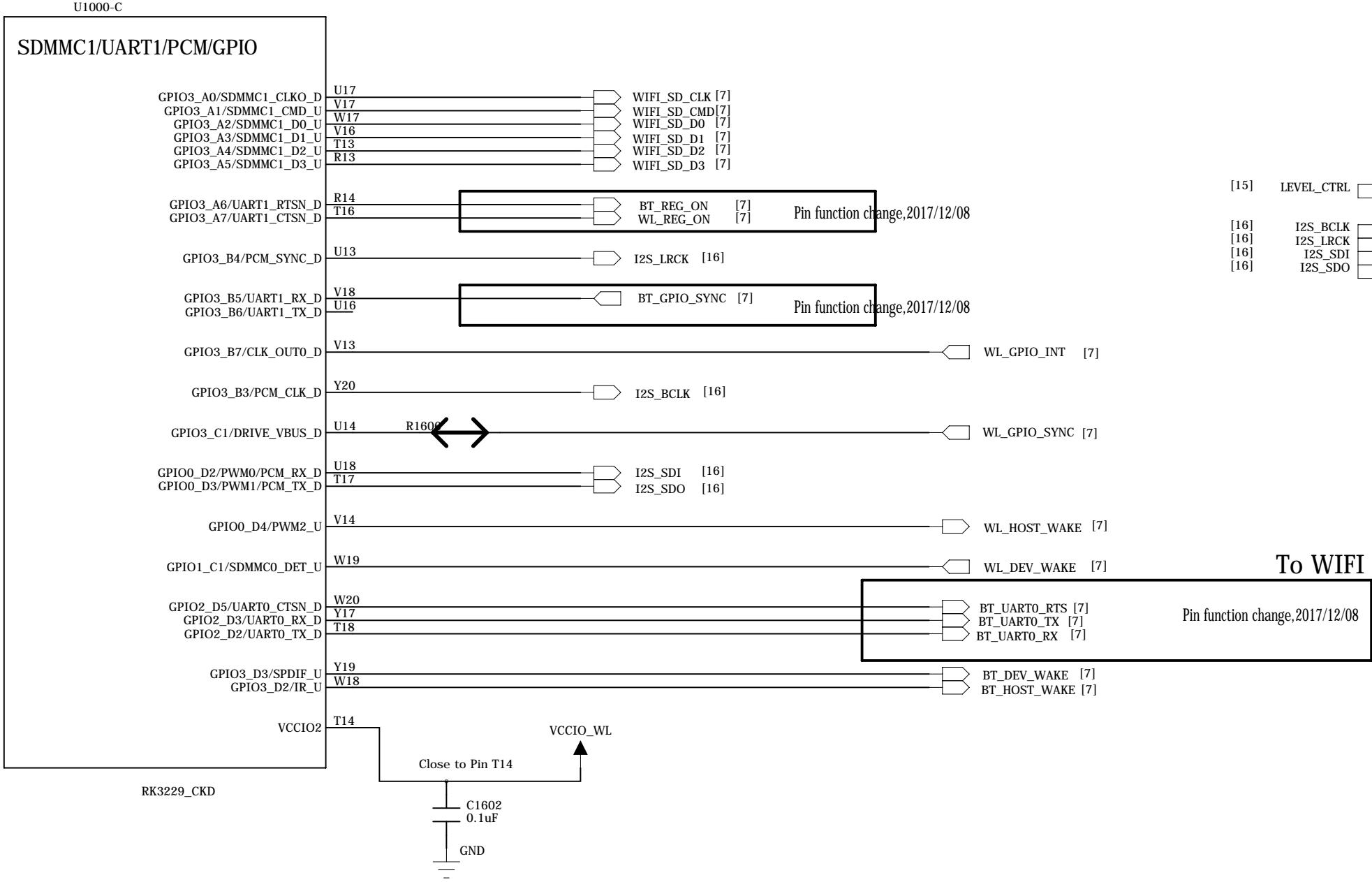
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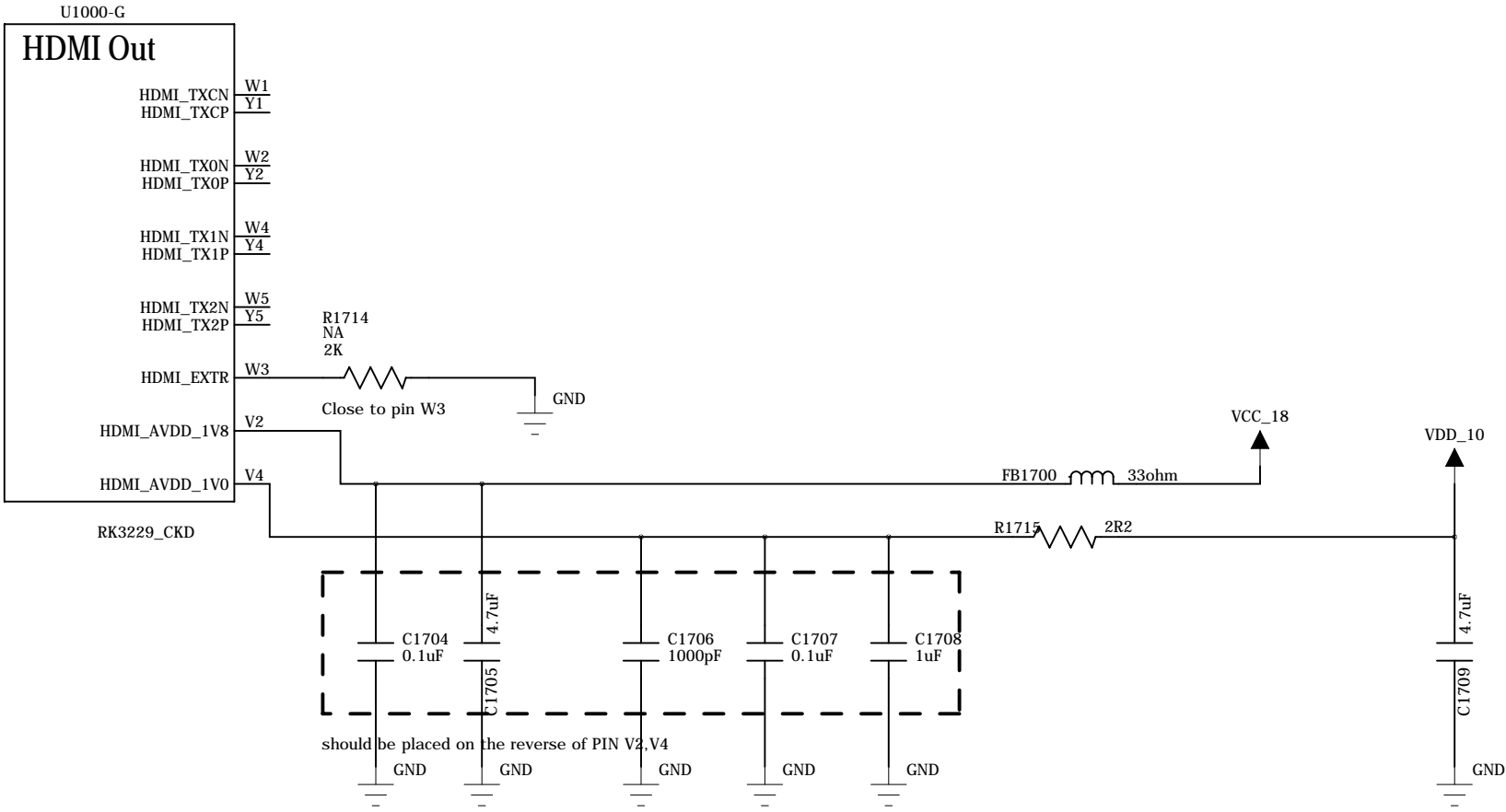



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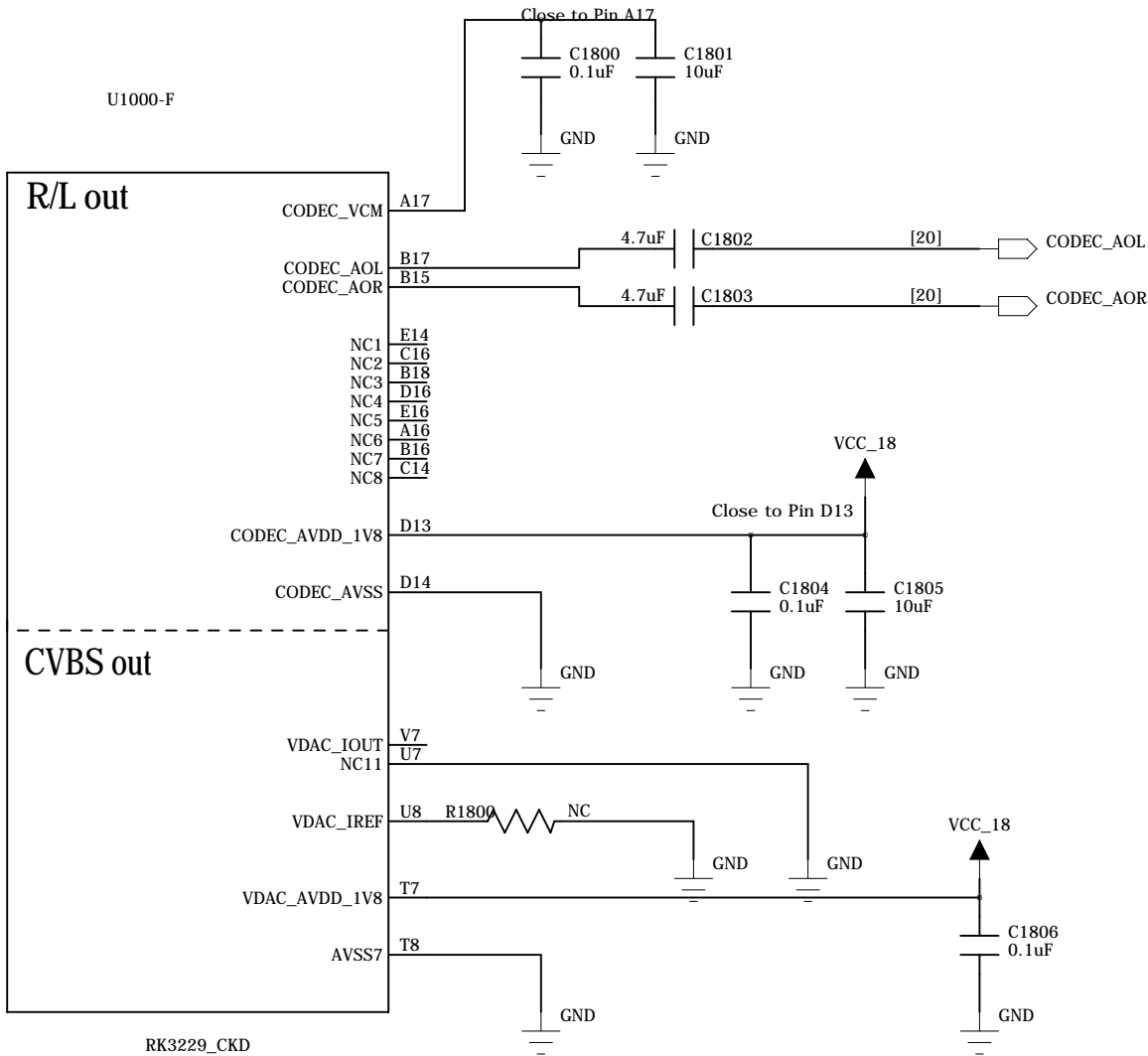





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DATE <Approved Date>	DATE <Checked Date>	DATE 2017/12/26	SHEET 16 OF 22

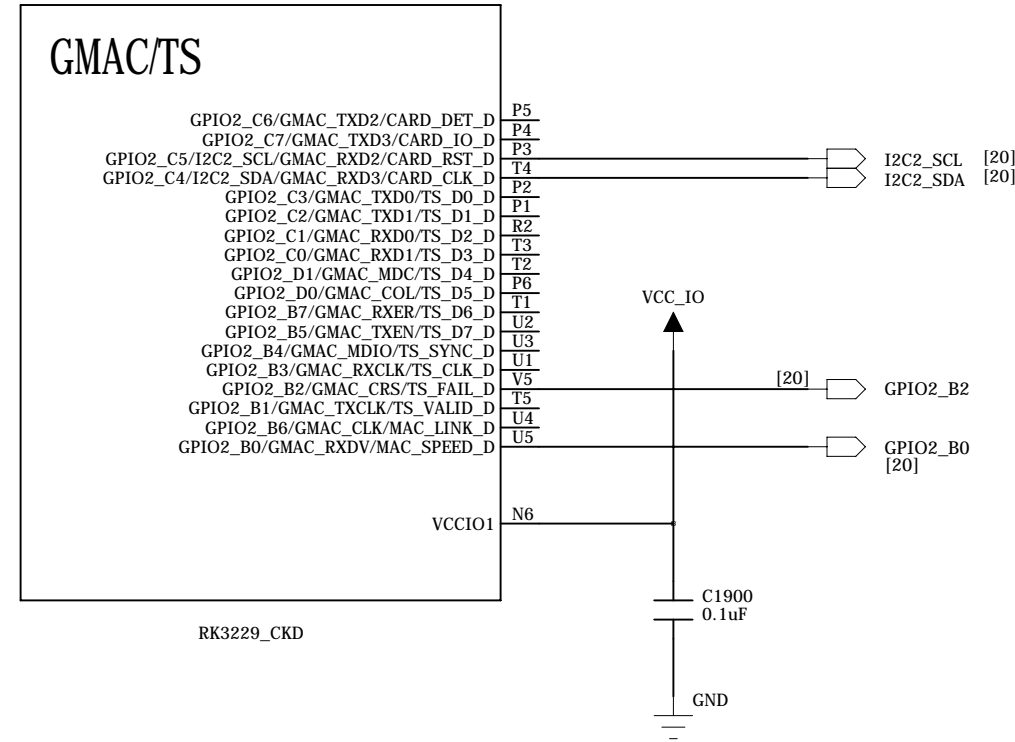


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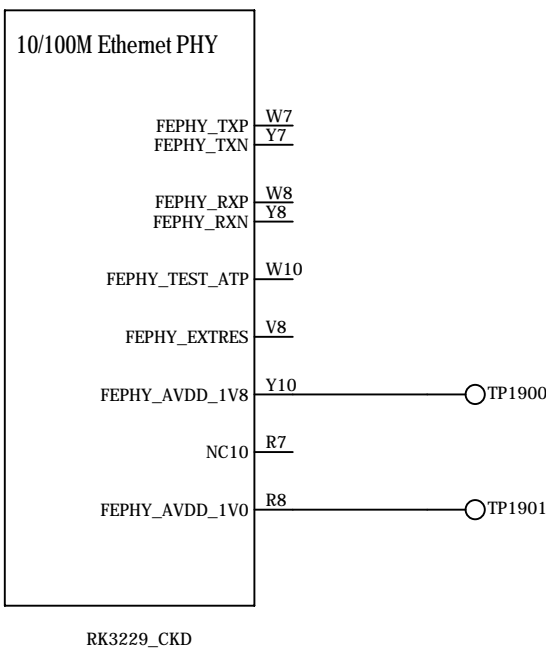


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DATE <Approved Date>	DATE <Checked Date>	DATE 2017/12/26	SHEET 18 OF 22	

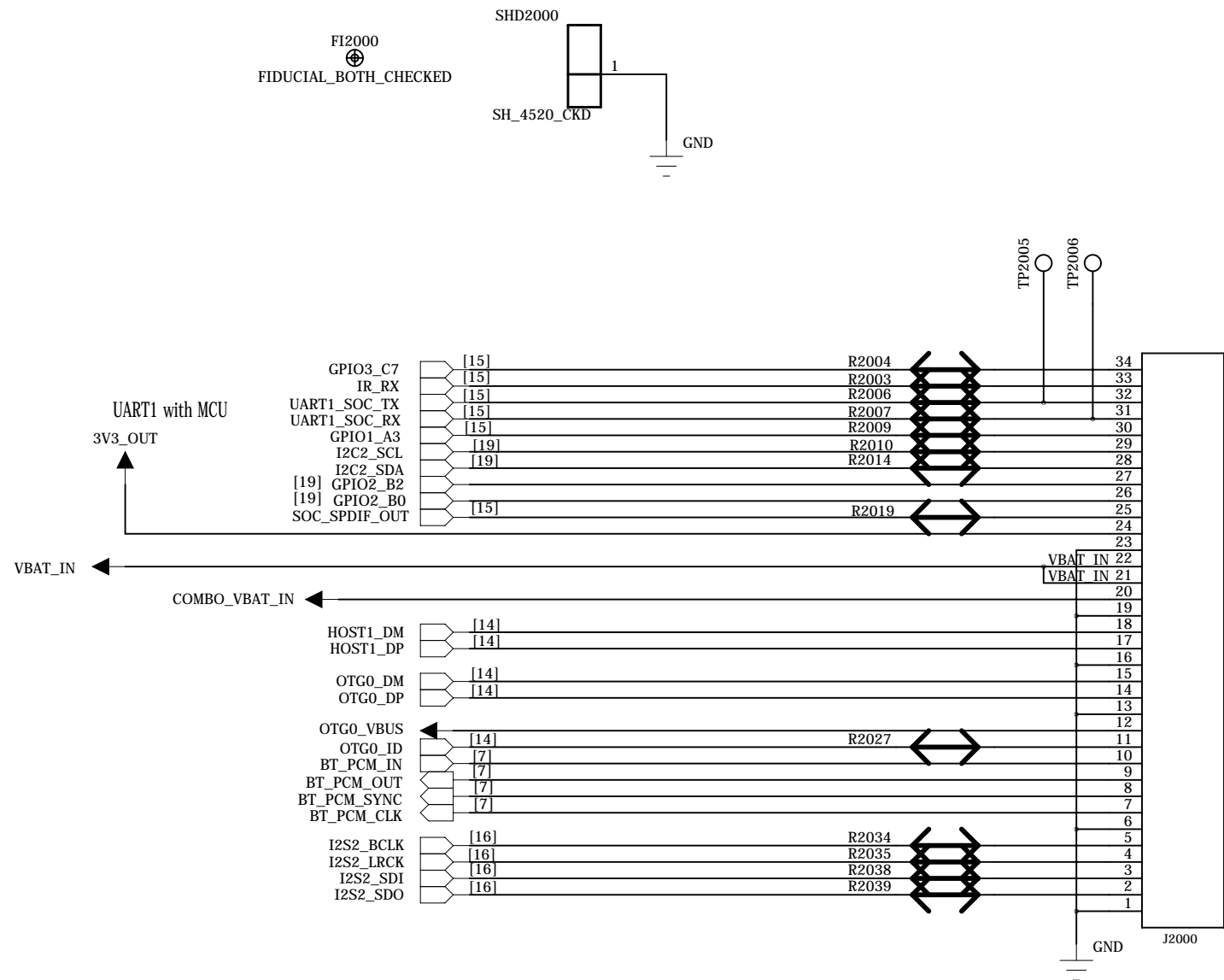
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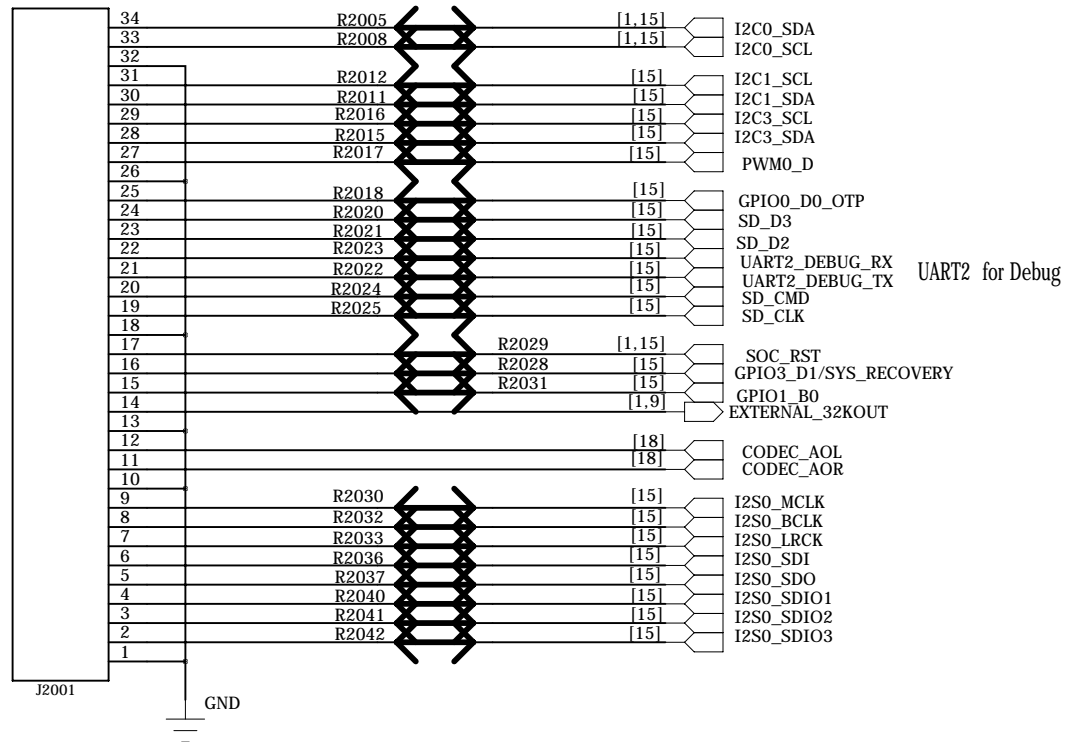
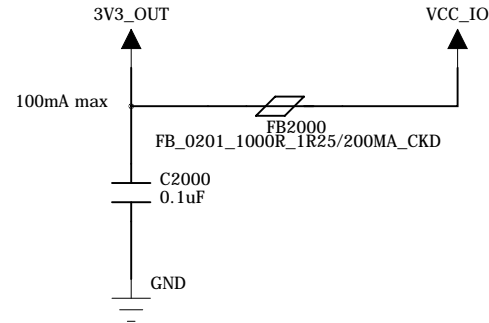
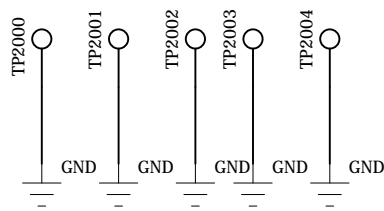
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APPROVAL <Approved By>	CHECK <Checked By>	DESIGN Danny Han	REV. R3
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DELTA_N-Part01				
Number	Pin Define	Level	Pin Name	IO Domain
34	GPIO3_C7	3.3V	GPIO3_C7_u	VCCIO4
33	IR_RX	3.3V	GPIO1_B3/UART1_RTSN/IR_u;PMIC_OUT1	VCCIO4
32	UART1_SOC_TX	3.3V	GPIO1_B1/UART1_TX/UART2_TX_u	VCCIO4
31	UART1_SOC_RX	3.3V	GPIO1_B2/UART1_RX/UART2_RX_u	VCCIO4
30	GPIO1_A3	3.3V	GPIO1_A3_d	VCCIO4
29	I2C2_SCL	3.3V	GPIO2_C5/I2C2_SCL/GMAC_RXD2/CARD_RST_d	VCCIO1
28	I2C2_SDA	3.3V	GPIO2_C4/I2C2_SDA/GMAC_RXD3/CARD_CLK_d	VCCIO1
27	GPIO2_B2	3.3V	GPIO2_B2/GMAC_CRS/TS_FAIL_d	VCCIO1
26	GPIO2_B0	3.3V	GPIO2_B0/GMAC_RXDV/MAC_SPEED_d	VCCIO1
25	SOC_SPDIF_OUT	3.3V	GPIO3_D7/TEST_CLK0/SPDIF_d	VCCIO4
24	3V3_OUT	-----		PW
23	GND	GND		GND
22	VBAT_IN1	-----		PW
21	VBAT_IN2	-----		PW
20	COMBO_VBAT_IN	-----		PW
19	GND	GND		GND
18	HOST1_DM	-----	USB1_DM	USB PHY
17	HOST1_DP	-----	USB2_DP	USB PHY
16	GND	GND		GND
15	OTG0_DM	-----	USB0_DM	USB PHY
14	OTG0_DP	-----	USB0_DP	USB PHY
13	GND	GND		GND
12	OTG0_VBUS	-----	USB0_VBUS	USB PHY
11	OTG0_ID	-----	USB0_ID	USB PHY
10	BT_PCM_SDI	1.8V	BT_PCM_SDI	CYW43455
9	BT_PCM_SDO	1.8V	BT_PCM_SDO	CYW43455
8	BT_PCM_SYNC	1.8V	BT_PCM_SYNC	CYW43455
7	BT_PCM_CLK	1.8V	BT_PCM_CLK	CYW43455
6	GND	GND		GND
5	I2S2_BCLK	3.3V	GPIO3_B3/PCM_CLK_d	VCCIO2
4	I2S2_LRCK	3.3V	GPIO3_B4/PCM_SYNC_d	VCCIO2
3	I2S2_SDI	3.3V	GPIO0_D2/PWM0/PCM_RX_d	VCCIO2
2	I2S2_SDO	3.3V	GPIO0_D3/PWM1/PCM_TX_d	VCCIO2
1	GND	GND		GND



DELTA_N-Part02				
Number	Pin Define	Level	Pin Name	IO Domain
34	I2C0_SDA(2.2Kpull up)	3.3V	GPIO0_A1/I2C0_SDA_u	VCCIO4
33	I2C0_SCL(2.2K pull up)	3.3V	GPIO0_A0/I2C0_SCL_u	VCCIO4
32	GND	GND		GND
31	I2C1_SCL	3.3V	GPIO0_A2/I2C1_SCL_u	VCCIO4
30	I2C1_SDA	3.3V	GPIO0_A3/I2C1_SDA/SDMMC1_CMD_u	VCCIO4
29	I2C3_SCL	3.3V	GPIO0_A6/HDMI_SCL/I2C3_SCL_u	VCCIO4
28	I2C3_SDA	3.3V	GPIO0_A7/HDMI_SDA/I2C3_SDA_u	VCCIO4
27	PWM_C	3.3V	GPIO3_C5/PWM0_d	VCCIO4
26	GND	GND		GND
25	GPIO0_D0_OTP	3.3V	GPIO0_D0/OTP_u	VCCIO4
24	SD_D3	3.3V	GPIO1_C5/SDMMC0_D3/JTAG_TMS_u	VCCIO4
23	SD_D2	3.3V	GPIO1_C4/SDMMC0_D2/JTAG_TCK_u	VCCIO4
22	UART2_DEBUG_RX	3.3V	GPIO1_C3/SDMMC0_D1/UART2_RX_u	VCCIO4
21	UART2_DEBUG_TX	3.3V	GPIO1_C2/SDMMC0_D0/UART2_TX_u	VCCIO4
20	SD_CMD	3.3V	GPIO1_B7/SDMMC0_CMD_u	VCCIO4
19	SD_CLK	3.3V	GPIO1_C0/SDMMC0_CLK0_d	VCCIO4
18	GND	GND		GND
17	SOC_RST	3.3V	NPOR_u	VCCIO4
16	GPIO3_D1/SYS_RECOVERY	3.3V	GPIO3_D1_u	VCCIO4
15	GPIO1_B0	3.3V	GPIO1_B0/UART1_CTSN/32K_OUT_u	VCCIO4
14	EXTERNAL_32KOUT	-----	CLK	
13	GND	GND		GND
12	CODEC_AOL	-----	CODEC_AOL	AV_OUT
11	CODEC_AOR	-----	CODEC_AOR	AV_OUT
10	GND	GND		GND
9	I2S0_MCLK	3.3V	GPIO0_B0/I2S0_MCLK_u	VCCIO4
8	I2S0_BCLK	3.3V	GPIO0_B1/I2S0_SCLK/SPL_CLK_u	VCCIO4
7	I2S0_LRCK	3.3V	GPIO0_B4/I2S0_LRCK_TX_u	VCCIO4
6	I2S0_SDI	3.3V	GPIO0_B6/I2S0_SDI/SPL_CSNO_u	VCCIO4
5	I2S0_SDO	3.3V	GPIO0_B5/I2S0_SDO/SPL_RXD_u	VCCIO4
4	I2S0_SDIO1	3.3V	GPIO1_A2/SDMMC1_D1/I2S0_SDIO1_u	VCCIO4
3	I2S0_SDIO2	3.3V	GPIO1_A4/SDMMC1_D2/I2S0_SDIO2_u	VCCIO4
2	I2S0_SDIO3	3.3V	GPIO1_A5/SDMMC1_D3/I2S0_SDIO3_u	VCCIO4
1	GND	GND		GND

Libratone A/S



APPROVAL <Approved By>

DATE <Approved Date>

CHECK <Checked By>

DATE <Checked Date>

PROJECT NAME Delta_N

DRAW NO ES1

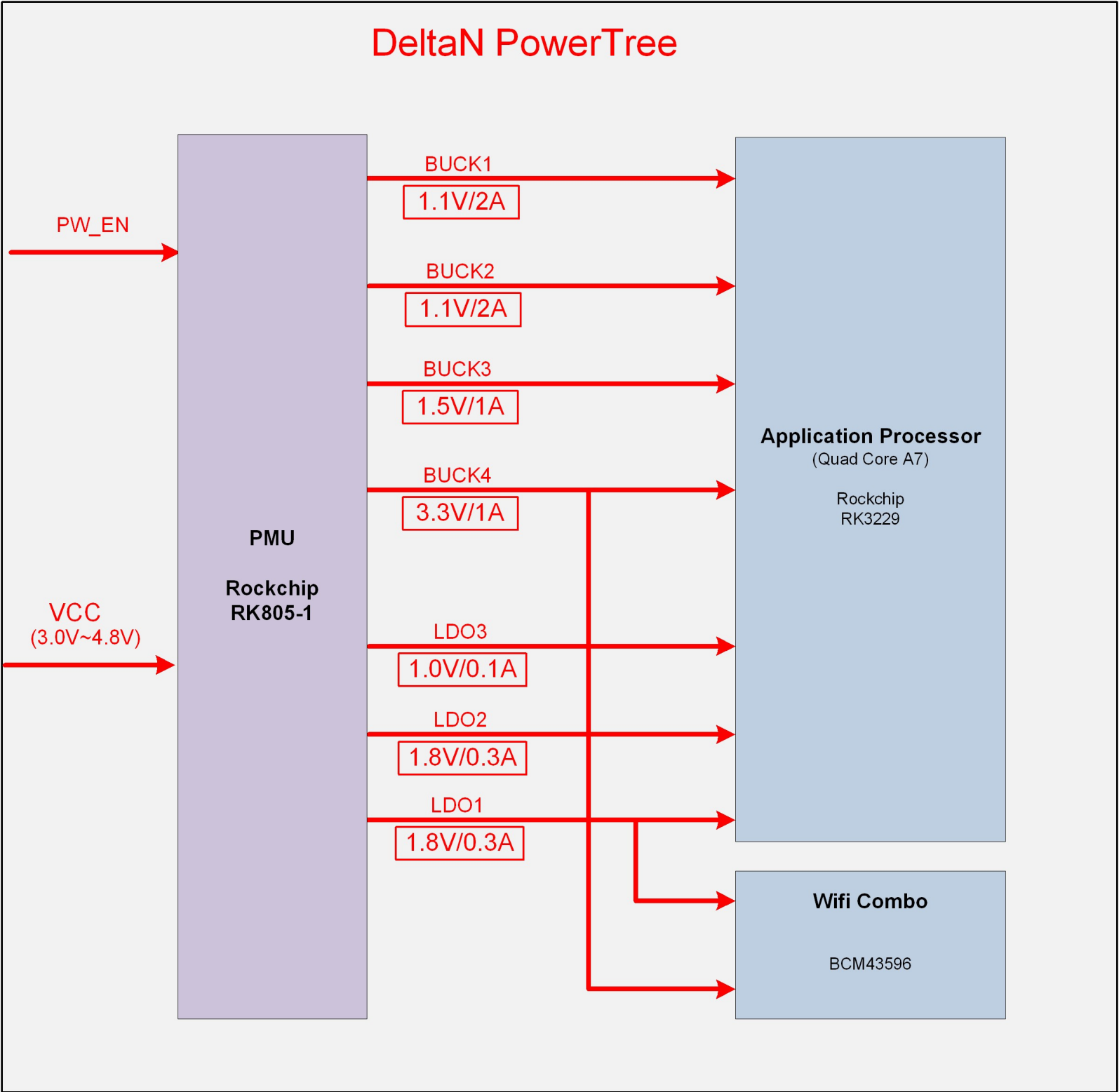
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DESIGN Danny Han

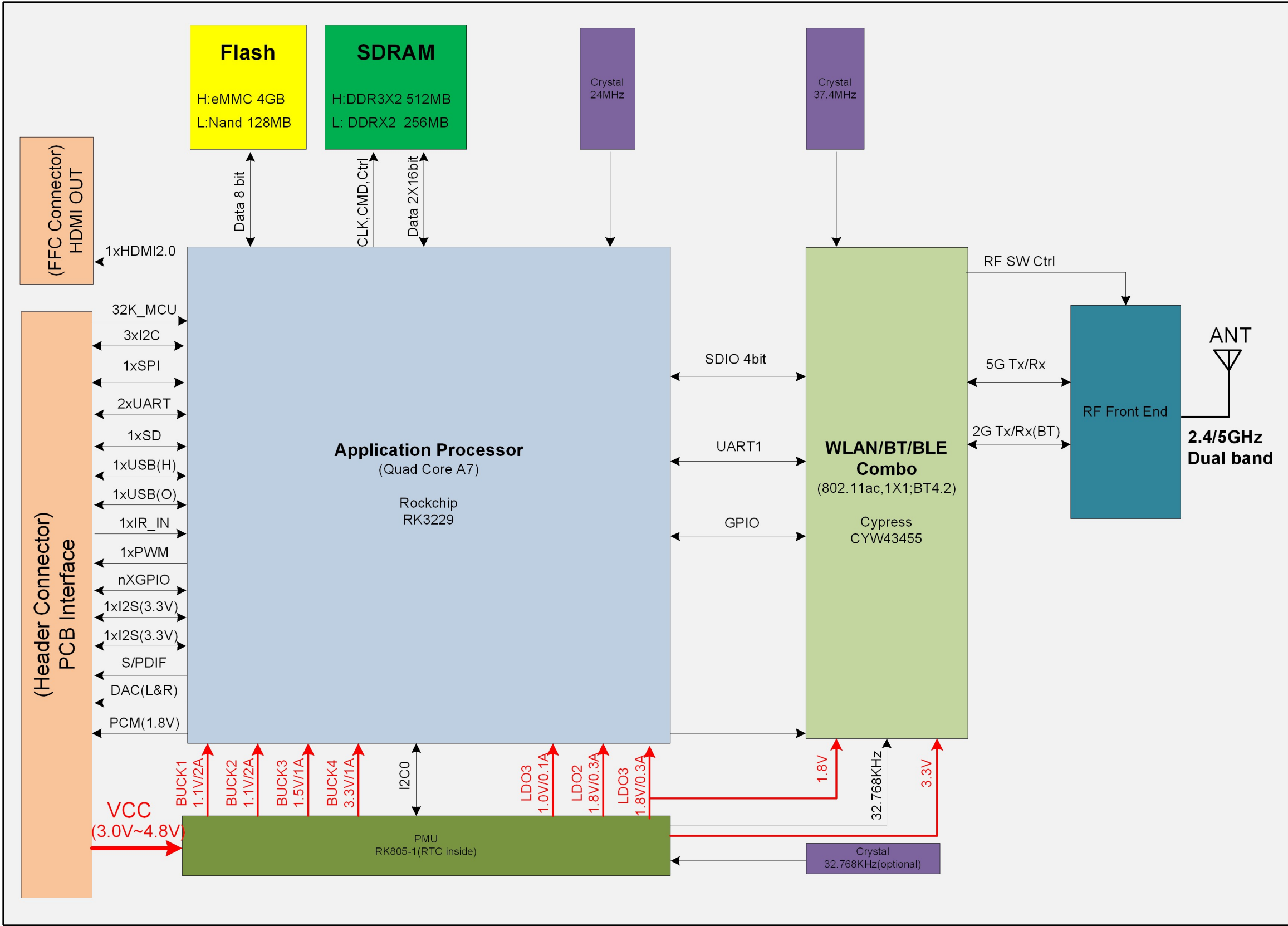
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<div>Libratone A/S</div> <div>LIBRATONE</div>		PROJECT NAME	Delta_N	
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<Approved By>	<Checked By>	Danny Han	R3	
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APPROVAL		CHECK		DESIGN	
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