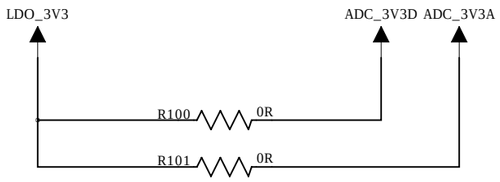
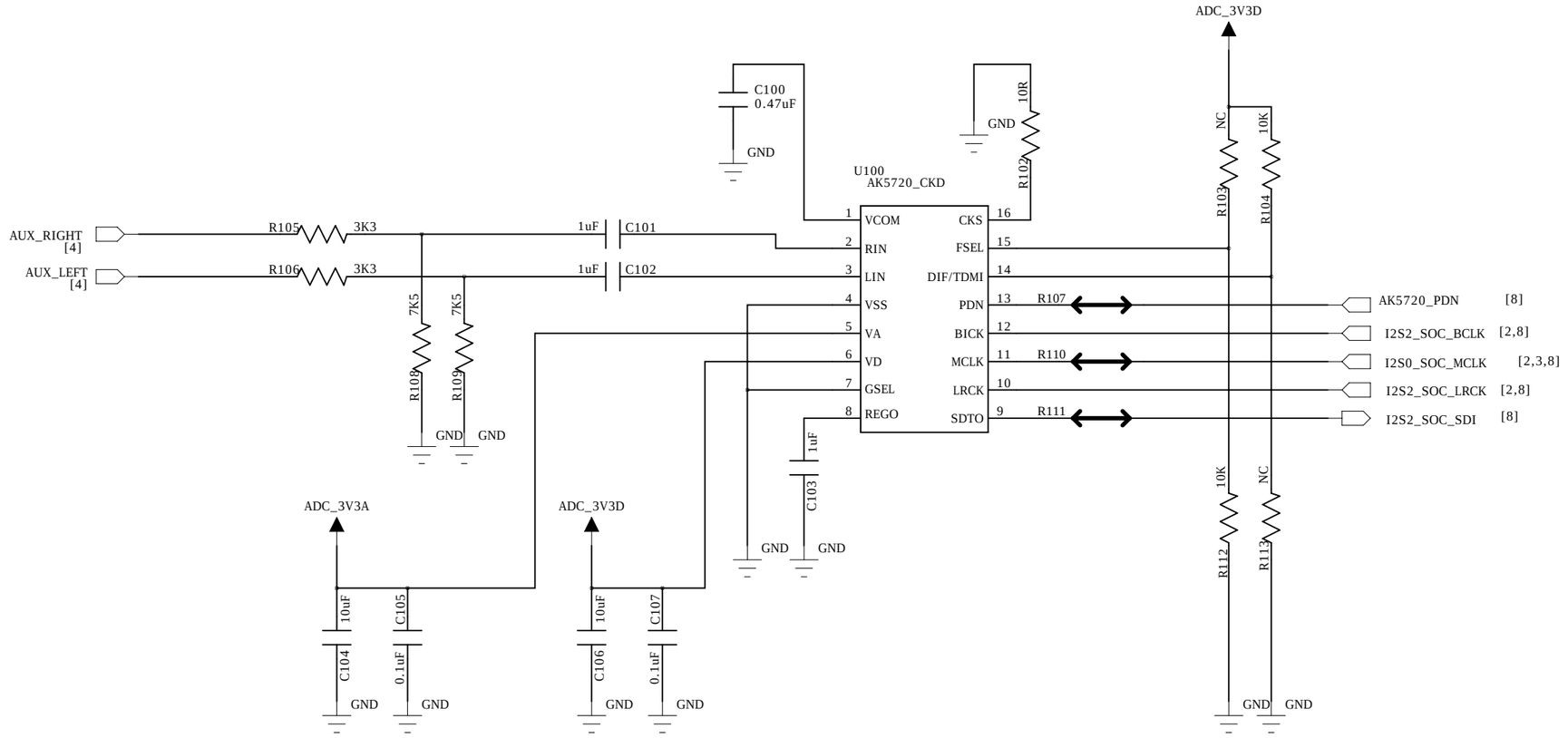
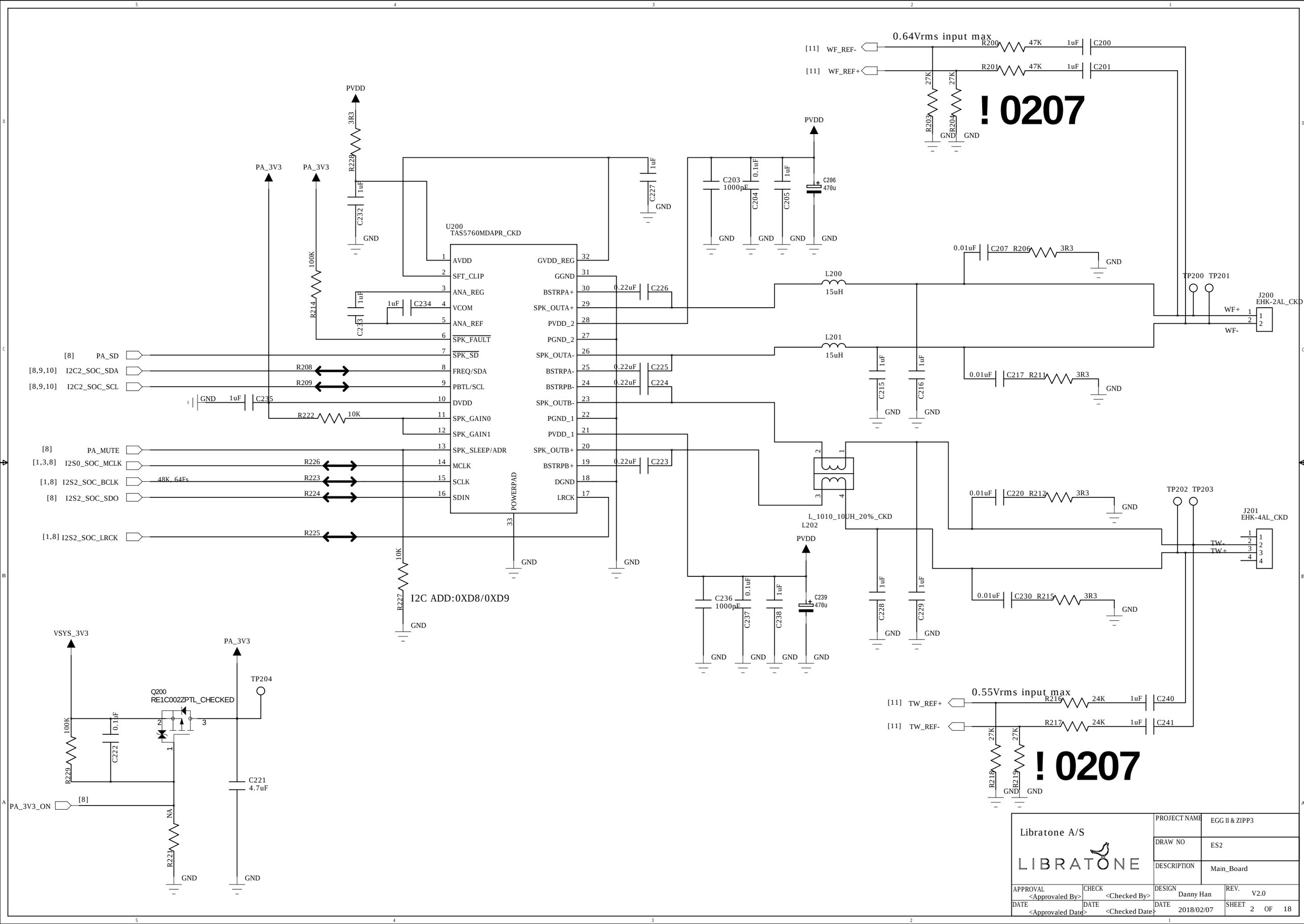
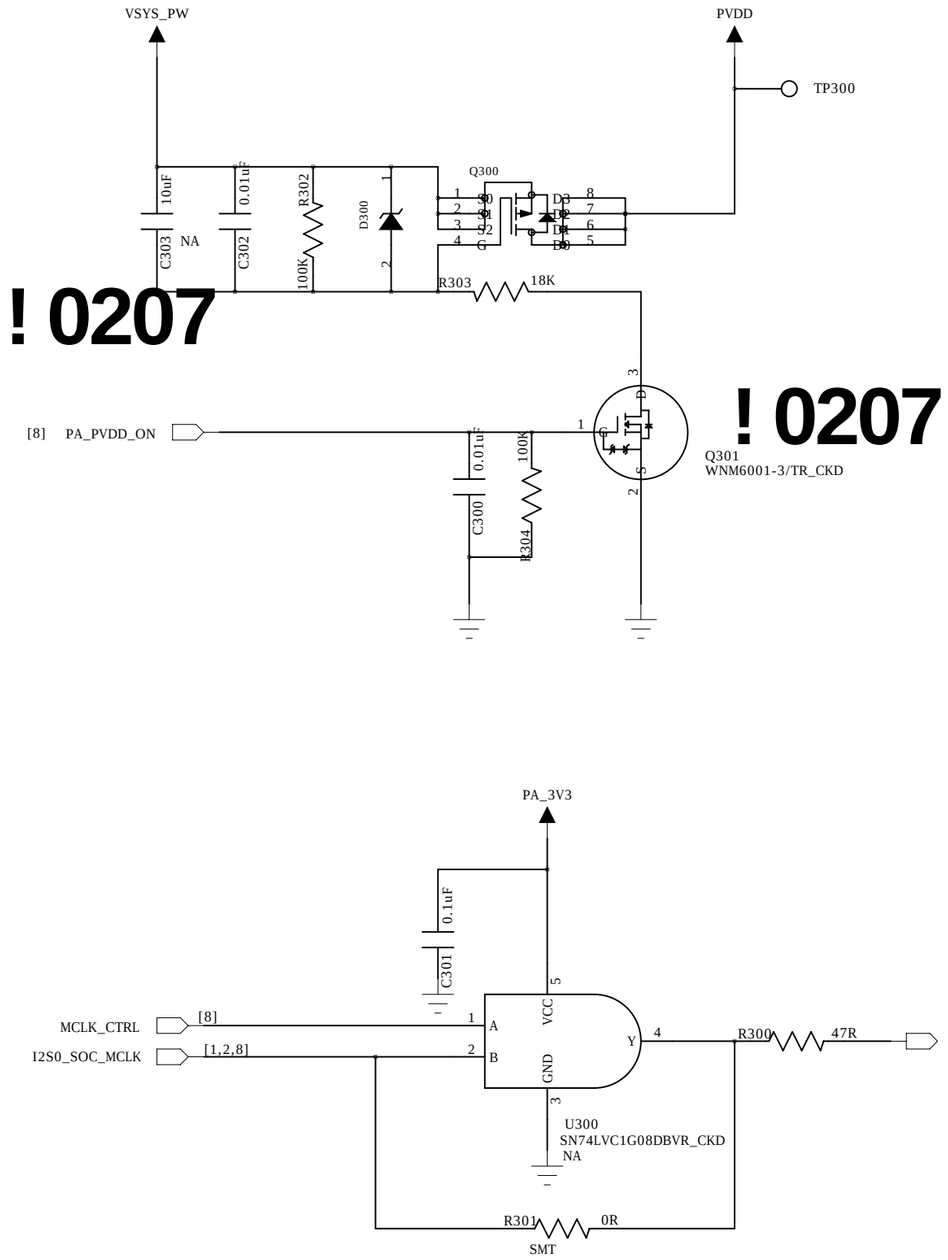




Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 1 OF 18

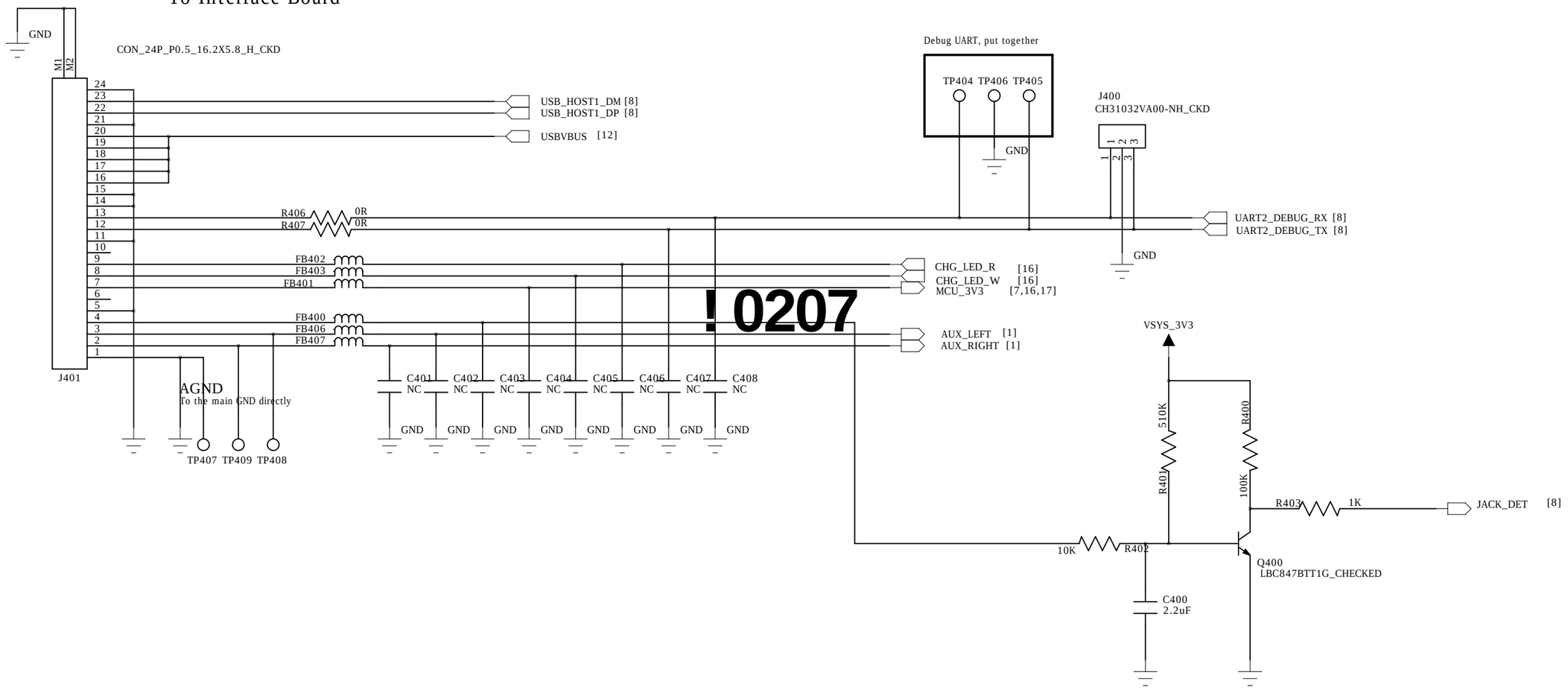


Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 2 OF 18



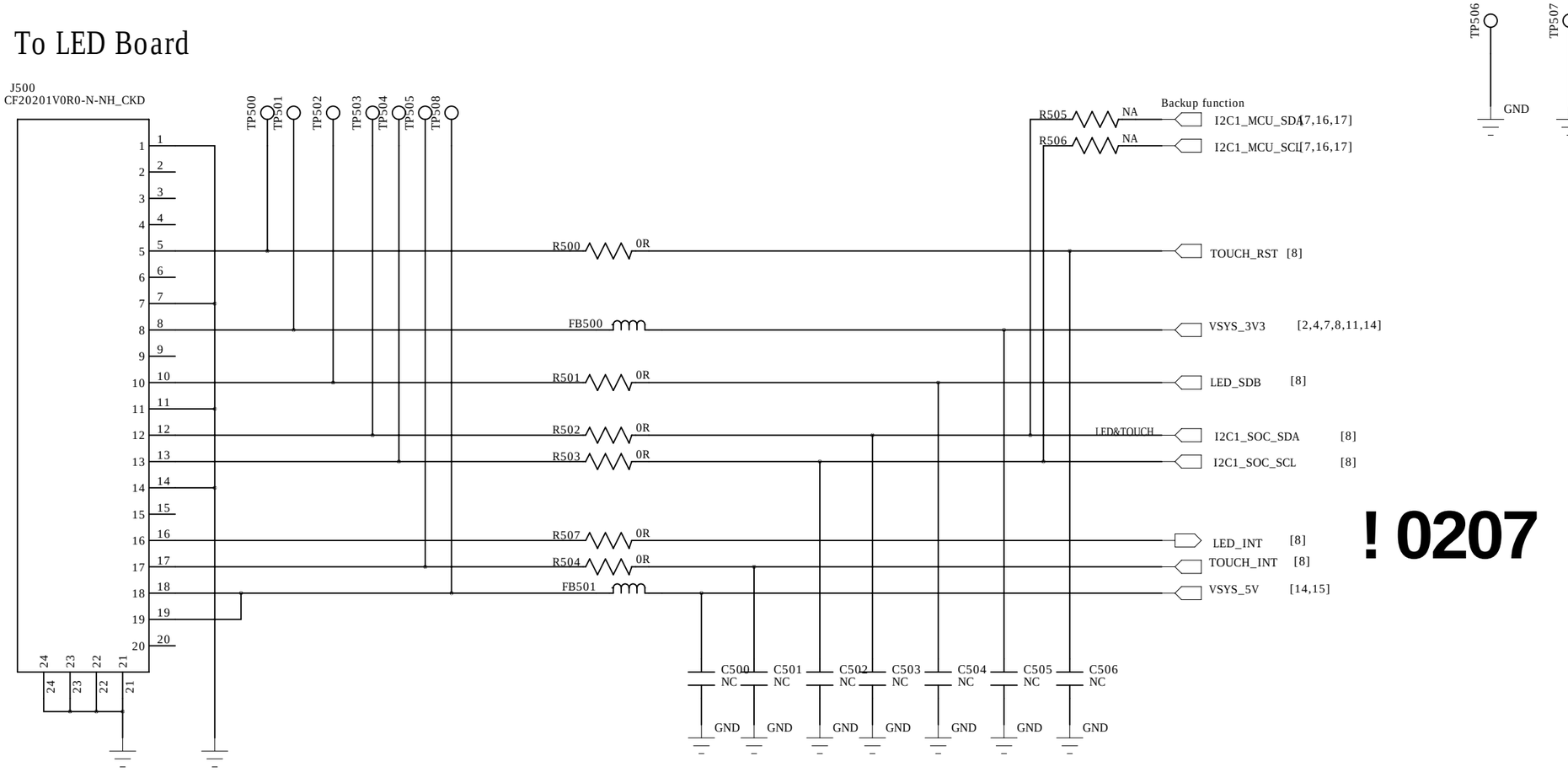
	EGG II	ZIPP3
U900	NA	ON
U1100	NA	ON
U300	NA	ON
R301	ON	NA
C206&C239	470uF	1000uF

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 3 OF 18



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 4 OF 18

To LED Board



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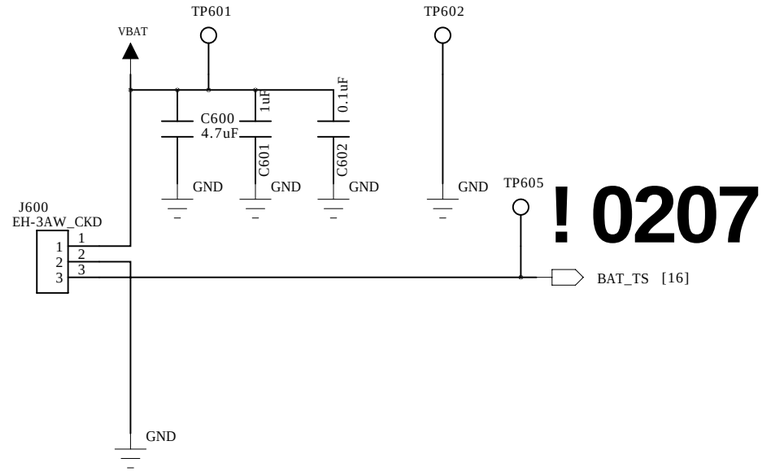
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 5 OF 18

µç³ØµçÁ¿×î´ó16.8V£¬×îÐ¡13.0V

MCU×î´ó²ÉÑùµçÑ¹3.3V µç³Ø²ÉÑùµçÑ¹Ë¥¼õ18dB



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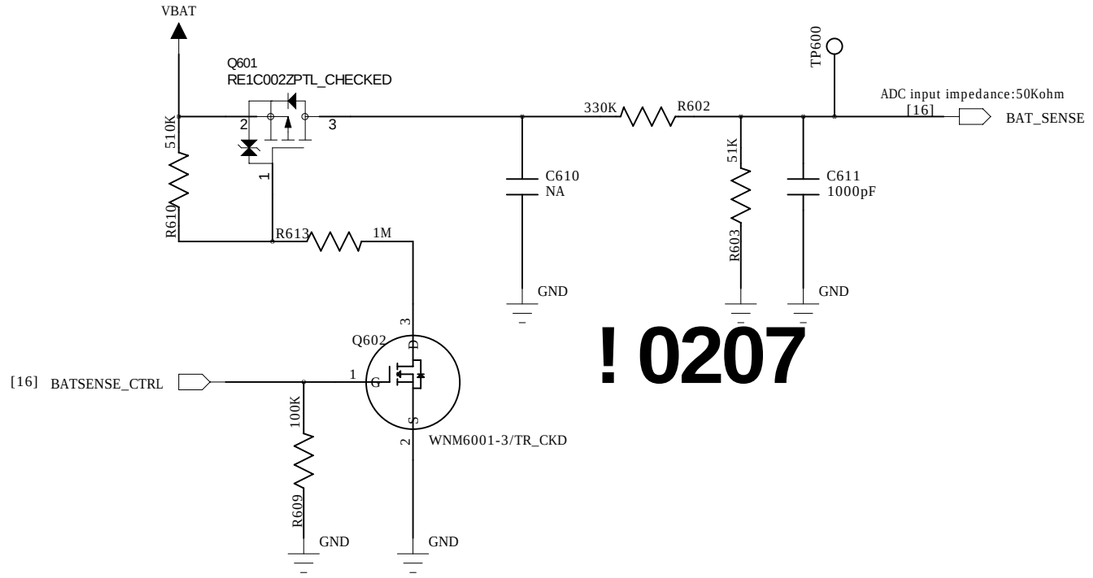

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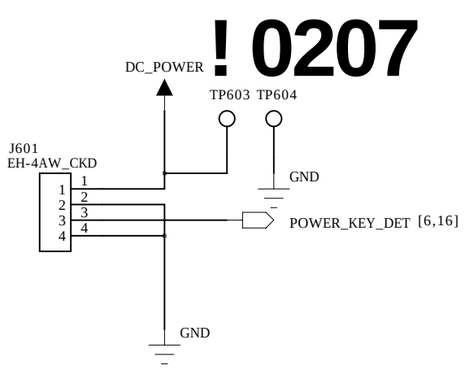

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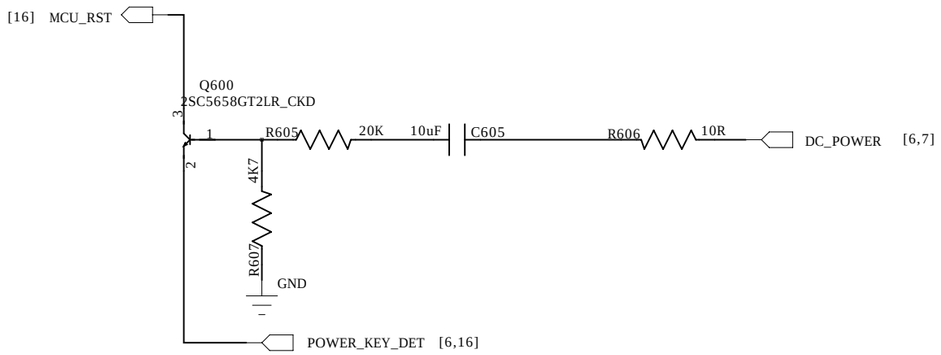
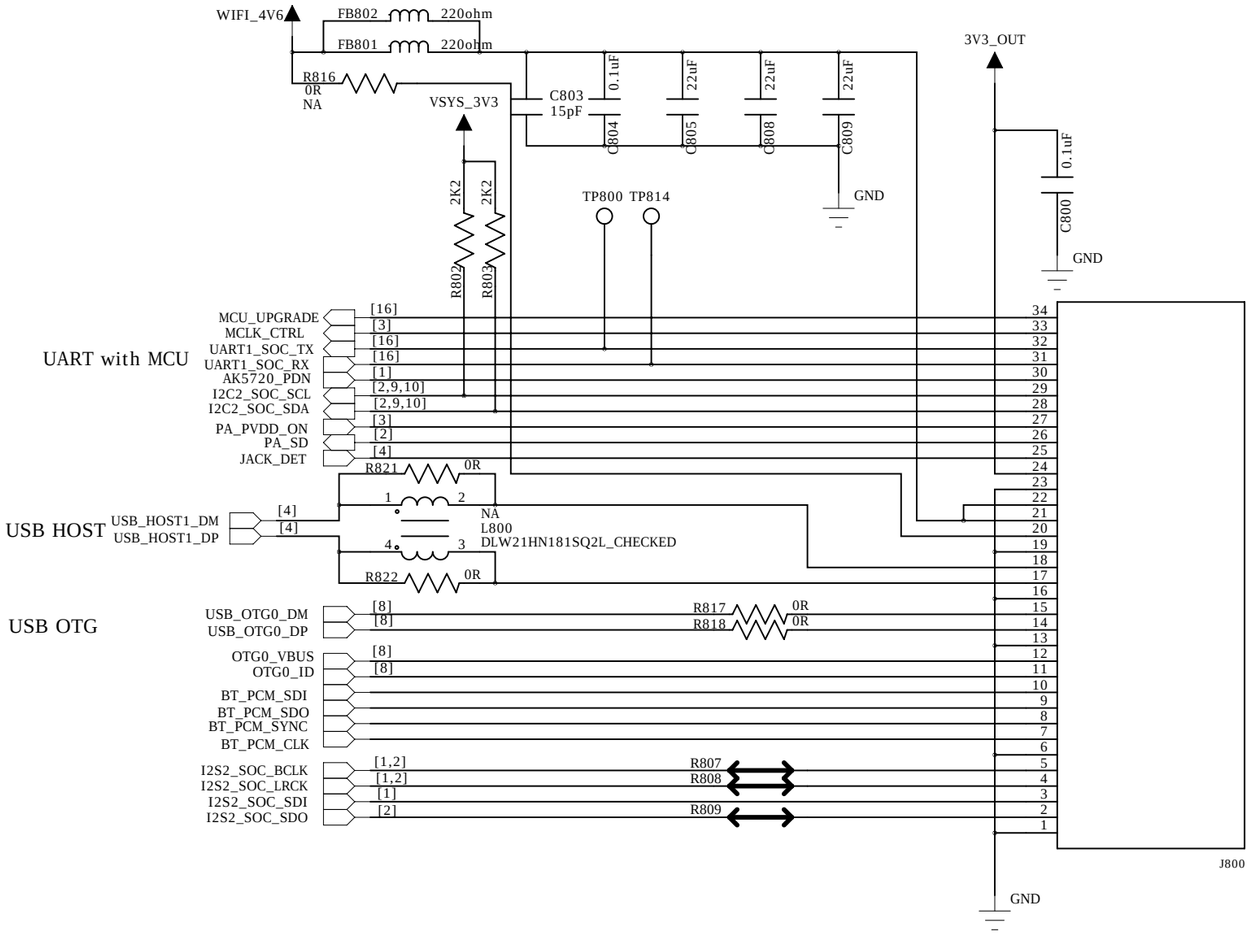
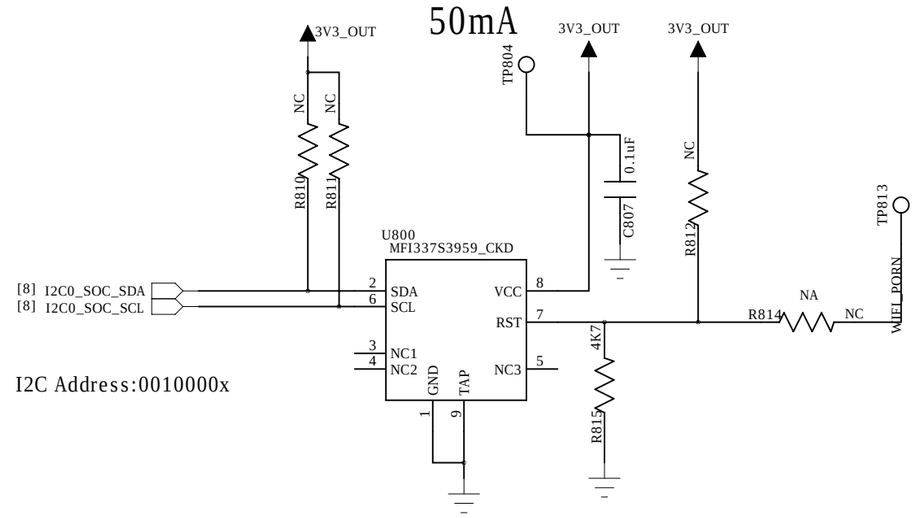


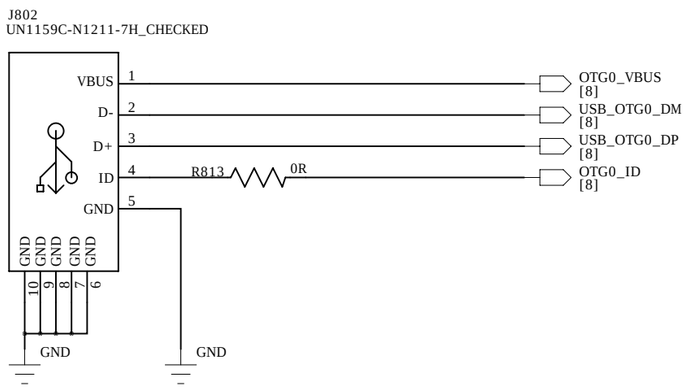
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 6 OF 18

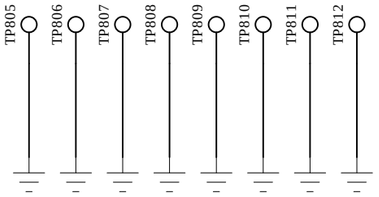
DC_POWER
Input:19V~21V
VSYS_PW
DC_POWER,VSYS_PW,VBAT trace:3mm at least(prefer
VBAT
VBAT Input:12V~17V
Current sense: diff trace
Current sense: diff trace
ACIN threshold>0.8V(input>15V)
ADC OUT:Adapter/Battery Current Monitor
Power output monitor
20W*1.44uA*100K=2.88V
ISL9238HRTZ-T_CKD
Default (Input: 19V/0.5A)
PROG Default: 4cells,733KHz,default 0.476A charging
To PW Ctrol
ADP_PG
CHG_PROCHOT
CHG_ABMON
CHG_PSYSMON
CHG_PG
I2C1_MCU_SCL
I2C1_MCU_SDA
MCU_3V3
CHG_VDD
VSYS_3V3
D700
RB520CS-30GT2RA_CKD
D701
RB520CS-30GT2RA_CKD
L700
2.2uH
TP700

Libratone A/S	PROJECT NAME: EGG II & ZIPP3
LIBRATONE	DRAW NO: ES2
	DESCRIPTION: Main_Board
APPROVAL: <Approvaled By>	CHECK: <Checked By>
DESIGN: Danny Han	REV.: V2.0
DATE: <Approvaled Date>	DATE: <Checked Date>
DATE: 2018/02/07	SHEET: 7 OF 18









Libratone A/S	PROJECT NAME	EGG II & ZIPP3	
	DRAW NO	ES2	
LIBRATONE	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 8 OF 18

External Power Supply: CP12IN:4.5V
LDO33IN:4.5V
VDDI2S:3.3V

I2C ADD:0X3B

TDM&RST:3.3V level I2C&MCLK: 3V3Level

Rst must stay low for 100ms after all power rails are stable

MIC2/4/6/ref mic

Audio Slave
Audio TDM 1.8V level with 6ADC
Digital I/O 3.3V level

!Q207

Not use for EGGII

Libratone A/S	PROJECT NAME	EGG II & ZIPP3	
LIBRATONE	DRAW NO	ES2	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 9 OF 18

External Power Supply: CP12IN:4.5V

LDO33IN:4.5V

VDDI2S:3.3V

I2C ADD:0X35

TDM&RST:3.3V level I2C&MCLK: 3V3Level

Rst must stay low for 100ms after all power rails are stable

MIC1/3/5/ref sig

For I2S Encoding Mode

Audio Slave

Audio TDM 1.8V level with 6ADC

Digital I/O 3.3V level

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
LIBRATONE		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 10 OF 18

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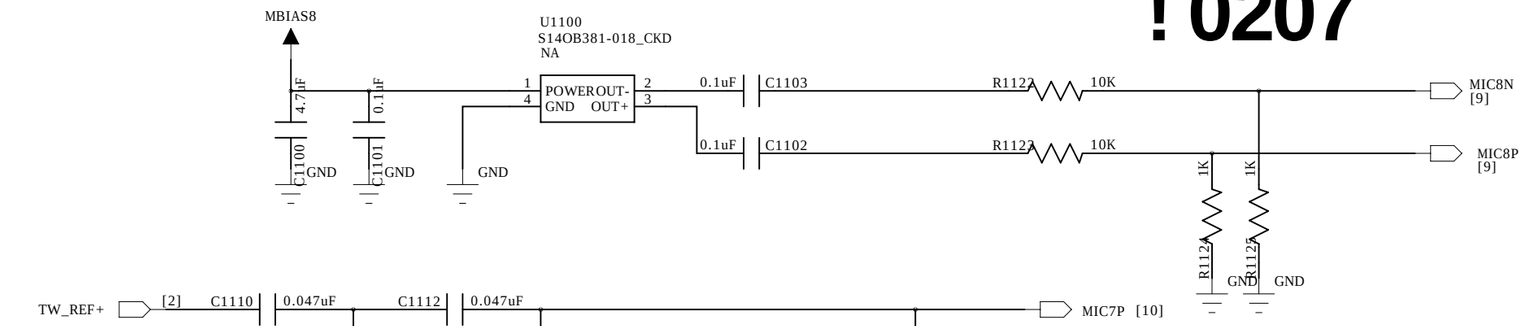

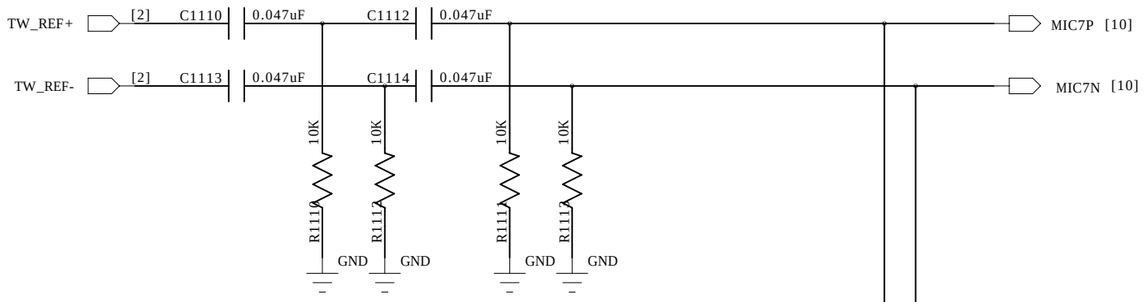

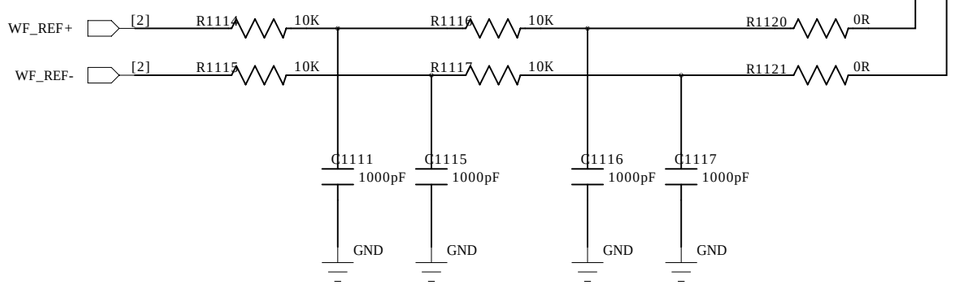

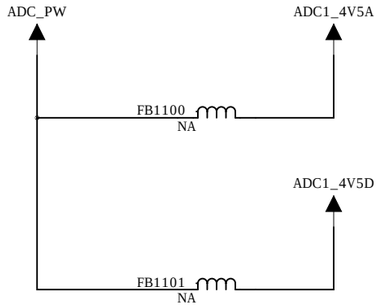

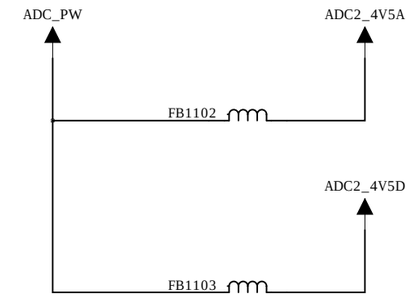

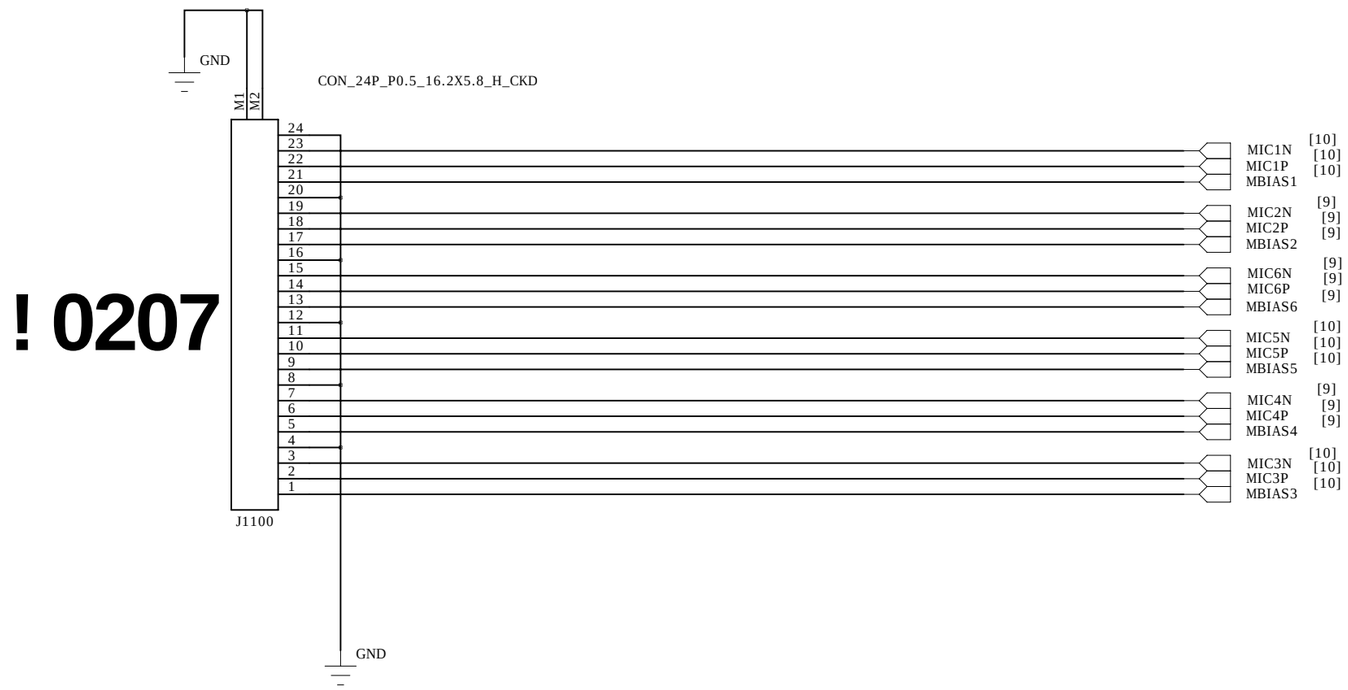

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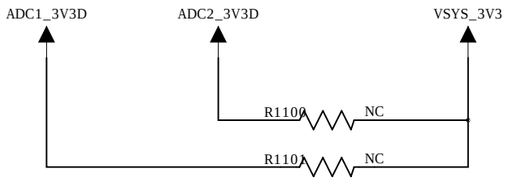
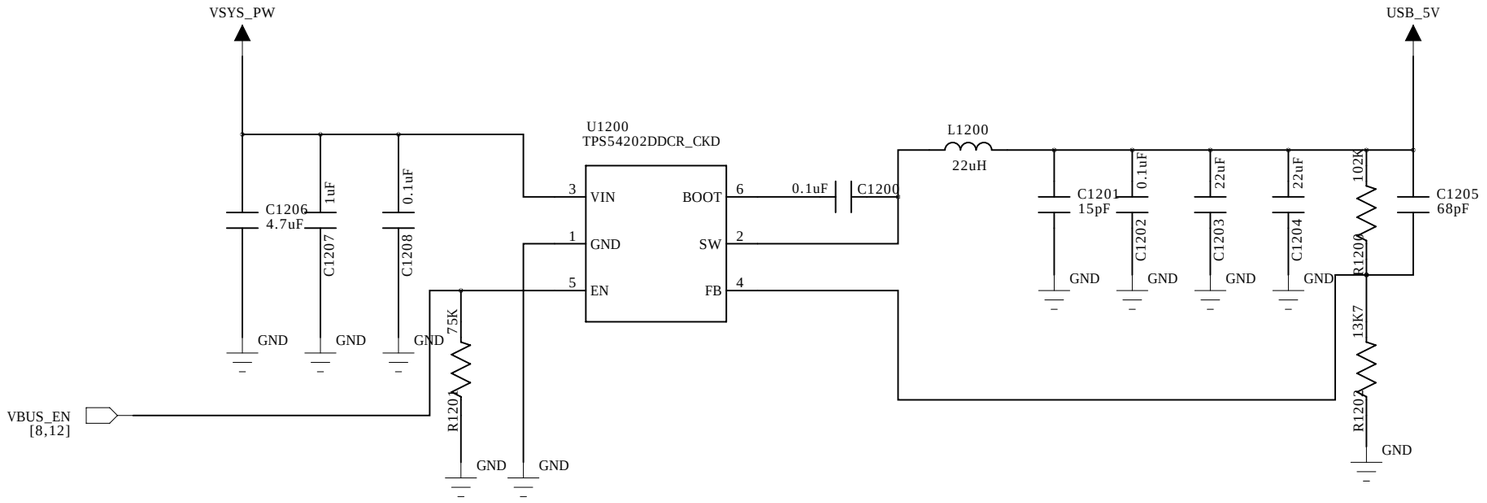
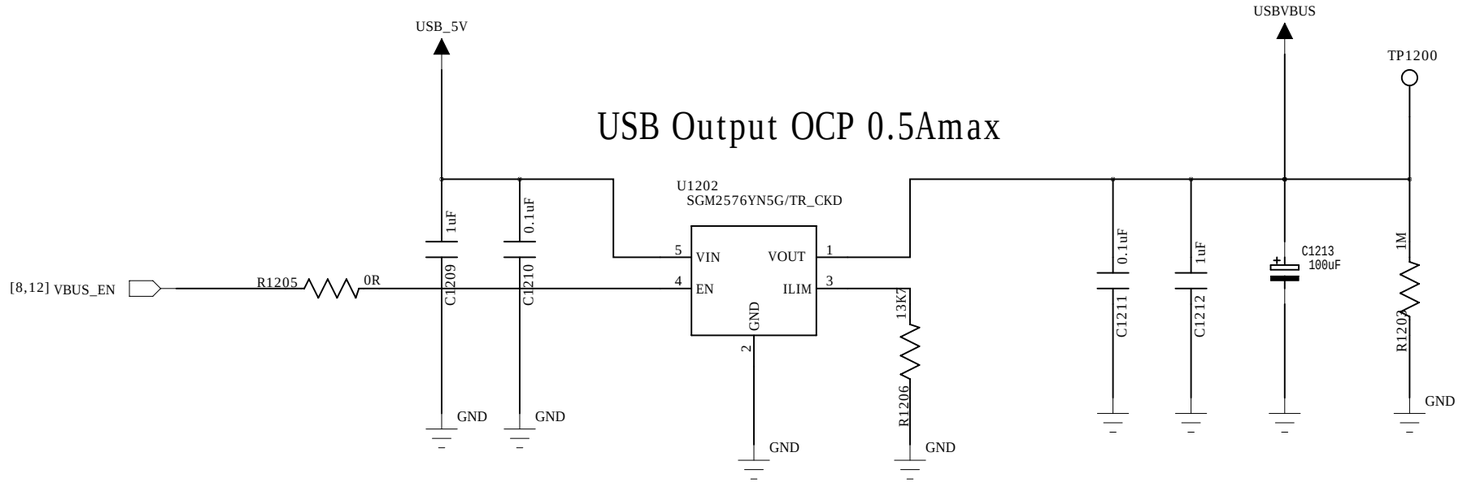


U900-ADC1	Aux_Right/SPK_TW
ADC2	MIC4
ADC3	MIC6
ADC4	MIC2
U1000-ADC1	Aux_Left/SPK_WF
ADC2	MIC3
ADC3	MIC5
ADC4	MIC1

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 11 OF 18





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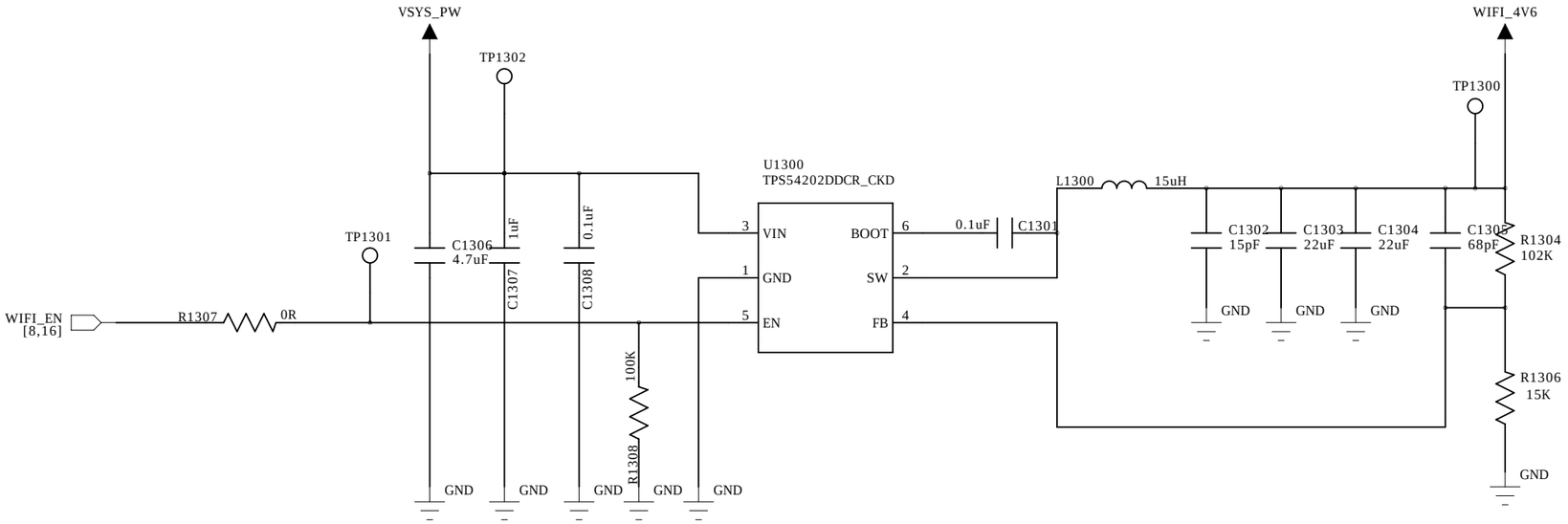
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 12 OF 18



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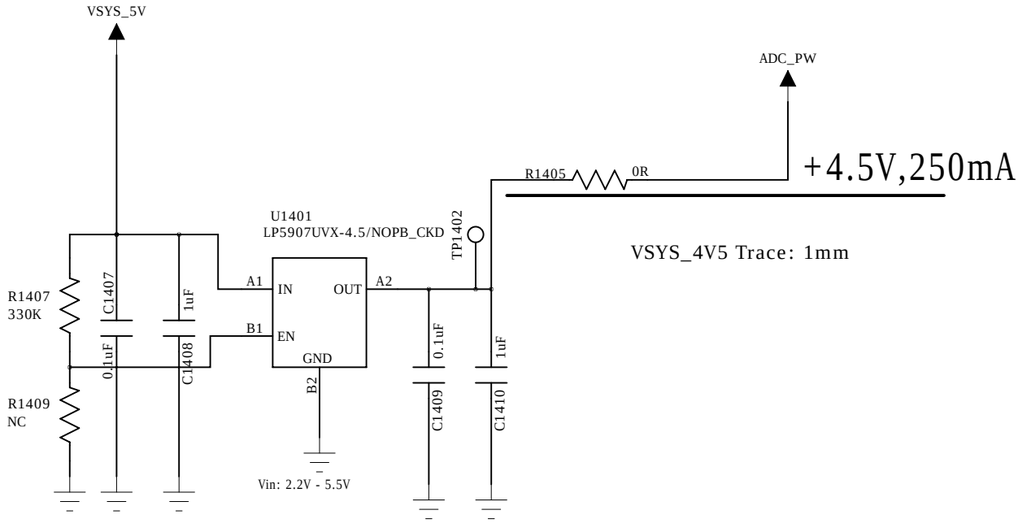
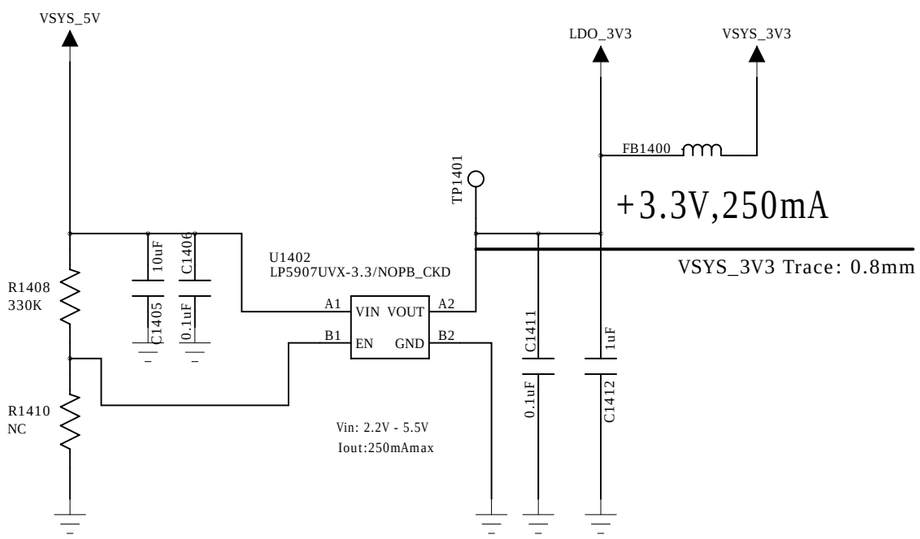
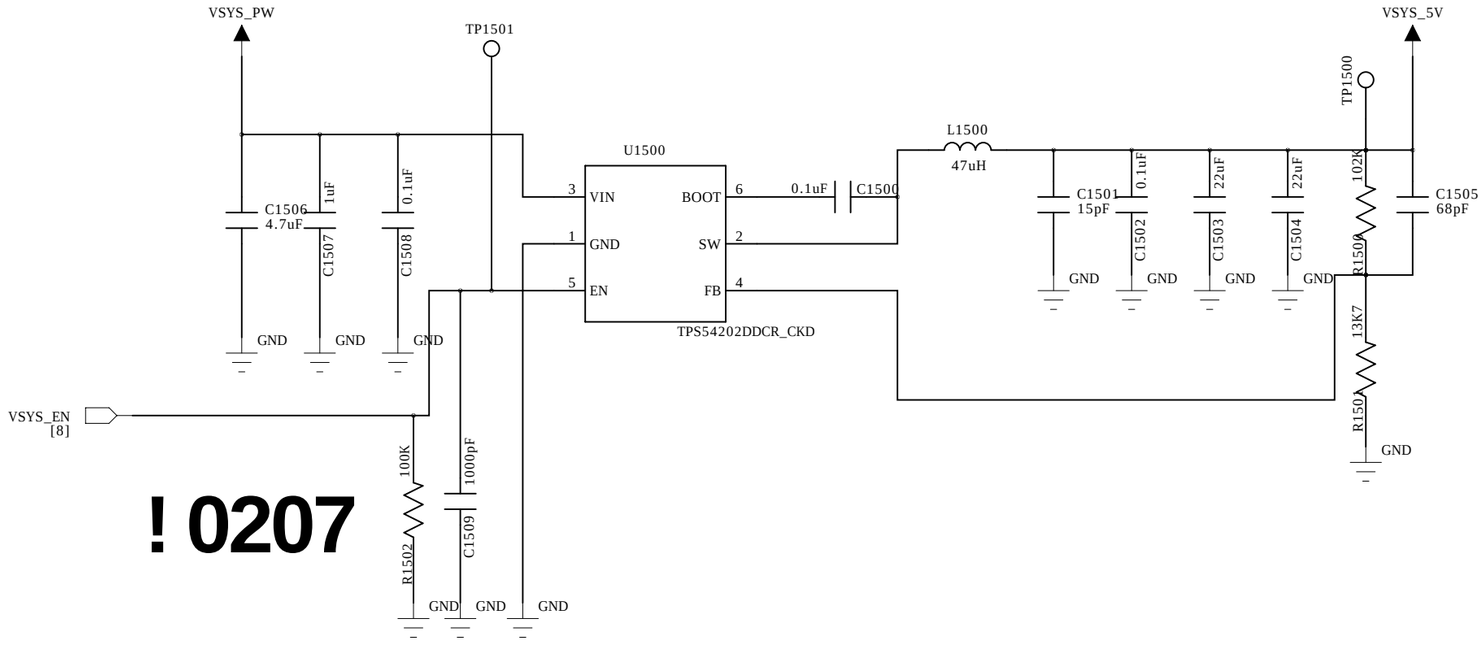
Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 13 OF 18





Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 14 OF 18



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 15 OF 18

MCU_UPGRADE [8]
I2C1_MCU_SCL [5,7,17]
I2C1_MCU_SDA [5,7,17]
BATSENSE_CTRL [6]
MCU_RST [6,16]
MCU_CTRL [8]
BAT_SENSE [6]
BAT_TS [6,16]
CHG_ABMON [7]
CHG_PSYSMON [7]
CHG_PROCHOT [7]

MCU_3V3
4K7 R1618
4K7 R1617
2K2 R1615
100K R1620
100K R1622
GND

Y1600
32.768kHz
18pF C1613
18pF C1612

Q1600
WNM6001-3/TR_CKD

TP1603
0.1uF C1600
0.1uF C1615
4.7uF C1614

U1600
STM32L011G4U6TR_CKD
PB9-BOOT0
PC14-OSC32_IN
PC15-OSC32_OUT
NRST
VDDA
PA0-CK_IN
PA1
PA13
PA10
PA9
PA8
VDD
VSS
PB1

R1618 0R
R1619 0R
R1614 0R

TP1601
TP1602

C1607
1000pF

D1600
RB520CS-30GT2RA_CKD

UART2_MCU_RX R1612 0R [8] UART1_SOC_TX
UART2_MCU_TX R1613 0R [8] UART1_SOC_RX

C1602 0.1uF
C1601 1uF

G_INT1 [17]
POWER_KEY_DET [6]
WIFI_EN [8,13]
MCU_SWCLK [16]
MCU_SWDIO [16]
UART1_SOC_TX [8]
UART1_SOC_RX [8]
MCU_32KOUT [8]
CHG_LED_R [4]
CHG_LED_W [4]
BATTS_CTRL [16]
ADP_PG [7]

! 0207
! 0207

VSYS_PW
! 0207
U1601
SGM2203-3.3YK3G/TR_CKD
VIN VOUT GND
1uF C1610
C1611 NA
TP1600
R1621 0R
C1604 0.1uF
1uF C1605
! 0207

BATTS_CTRL [16]
47K R1616
BAT_TS [6,16]
R1617 30K

J1600
CH31052VA00-NH_CKD
MCU_SWDIO [16]
MCU_SWCLK [16]
MCU_RST [6,16]

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 16 OF 18

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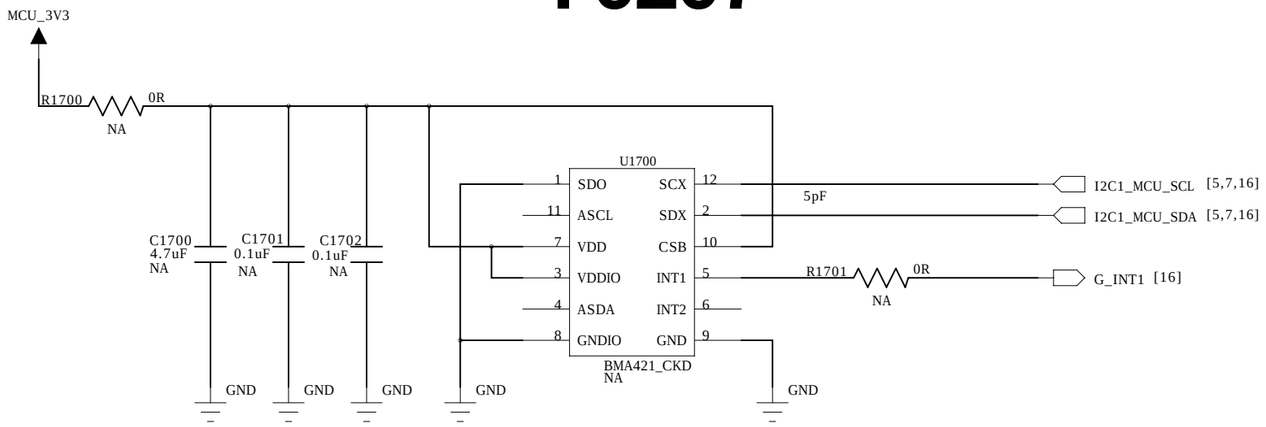
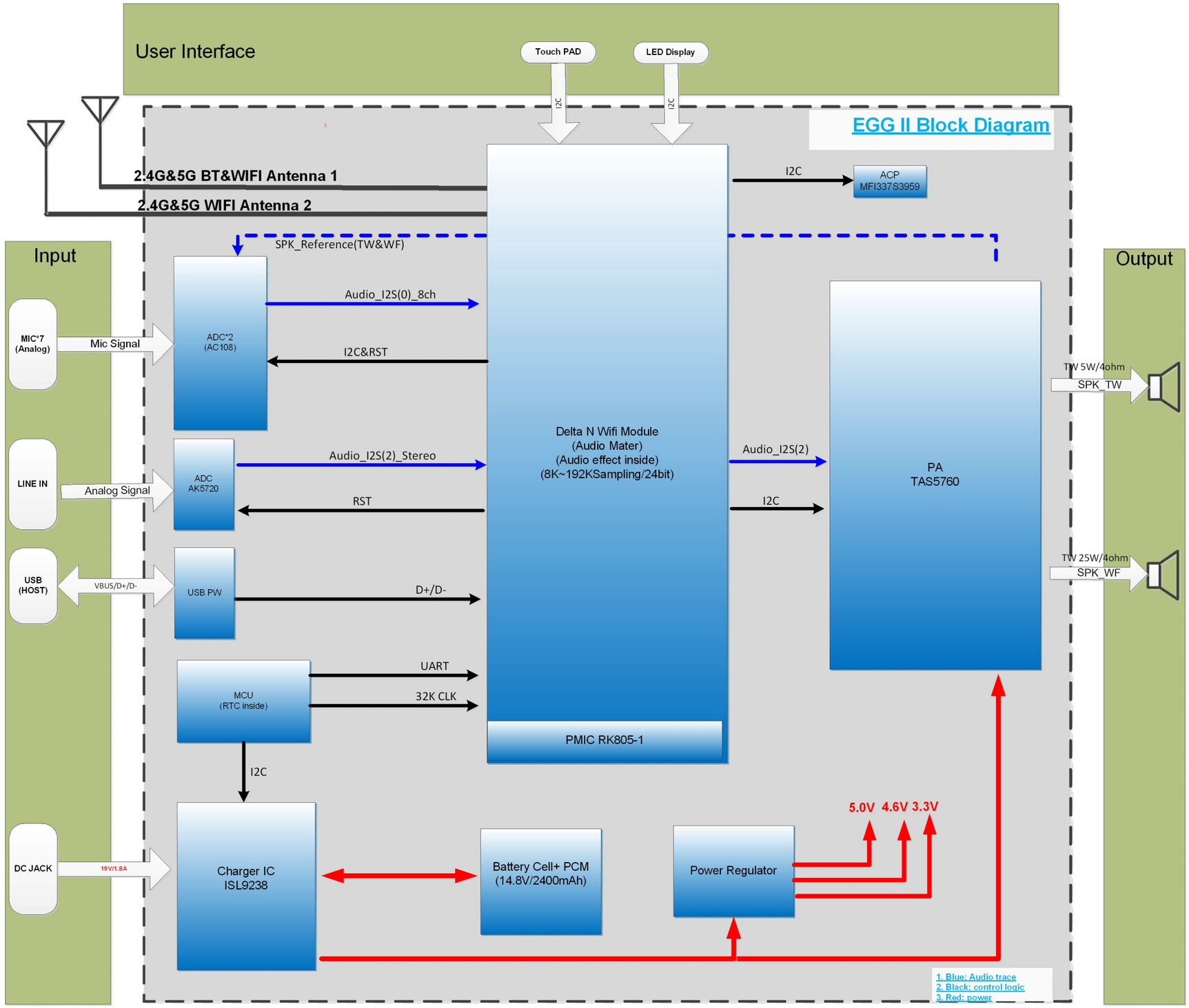


Active current @ Performance mdoe : 160 uA
Suspend mode ; 2.5uA
Lower power mode : 14uA

Libratone A/S		PROJECT NAME	EGG II & ZIPP3
		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 17 OF 18

! 0207

EGG II Block Diagram



Libratone A/S		PROJECT NAME	EGG II & ZIPP3
LIBRATONE		DRAW NO	ES2
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V2.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2018/02/07	SHEET 18 OF 18