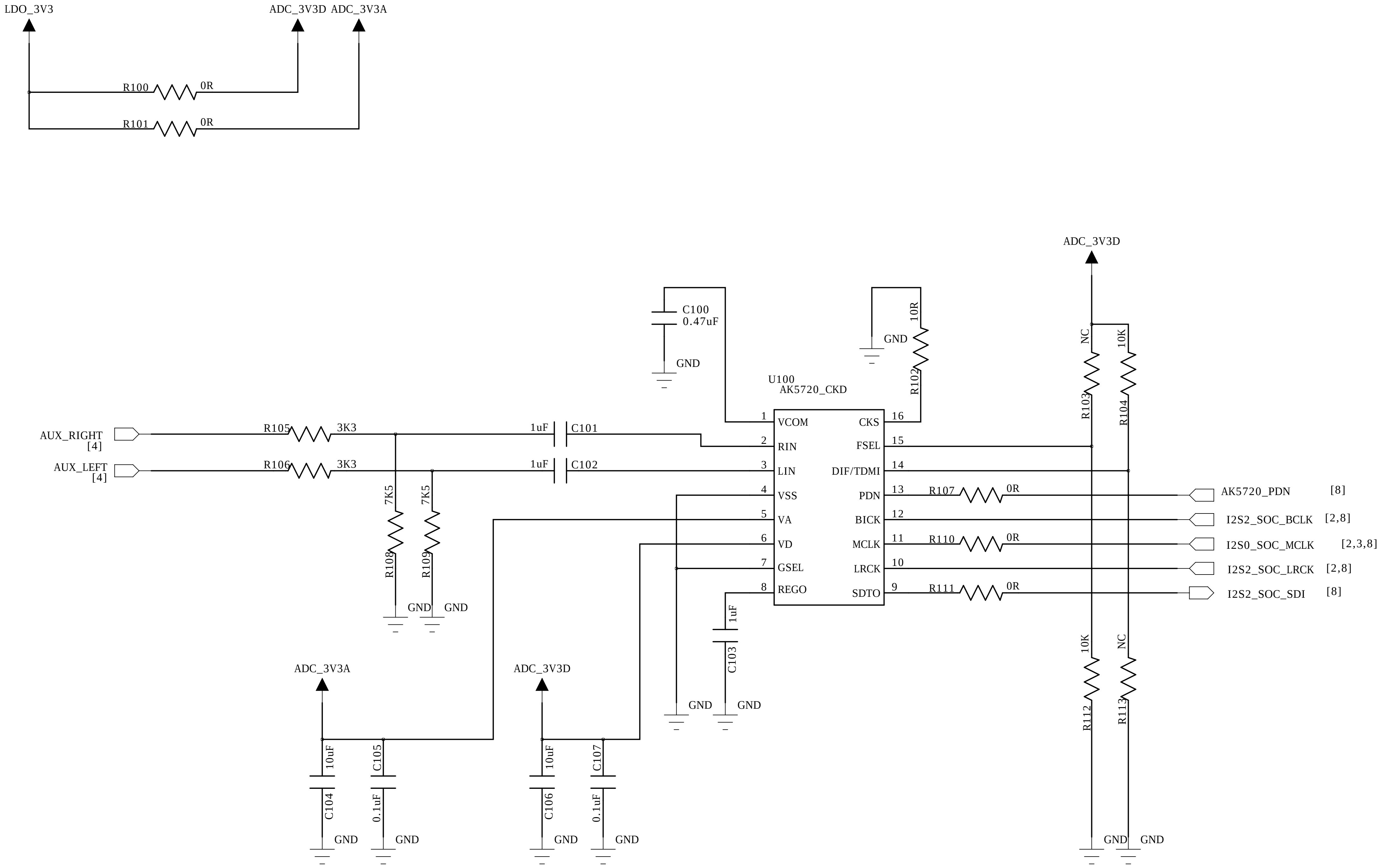
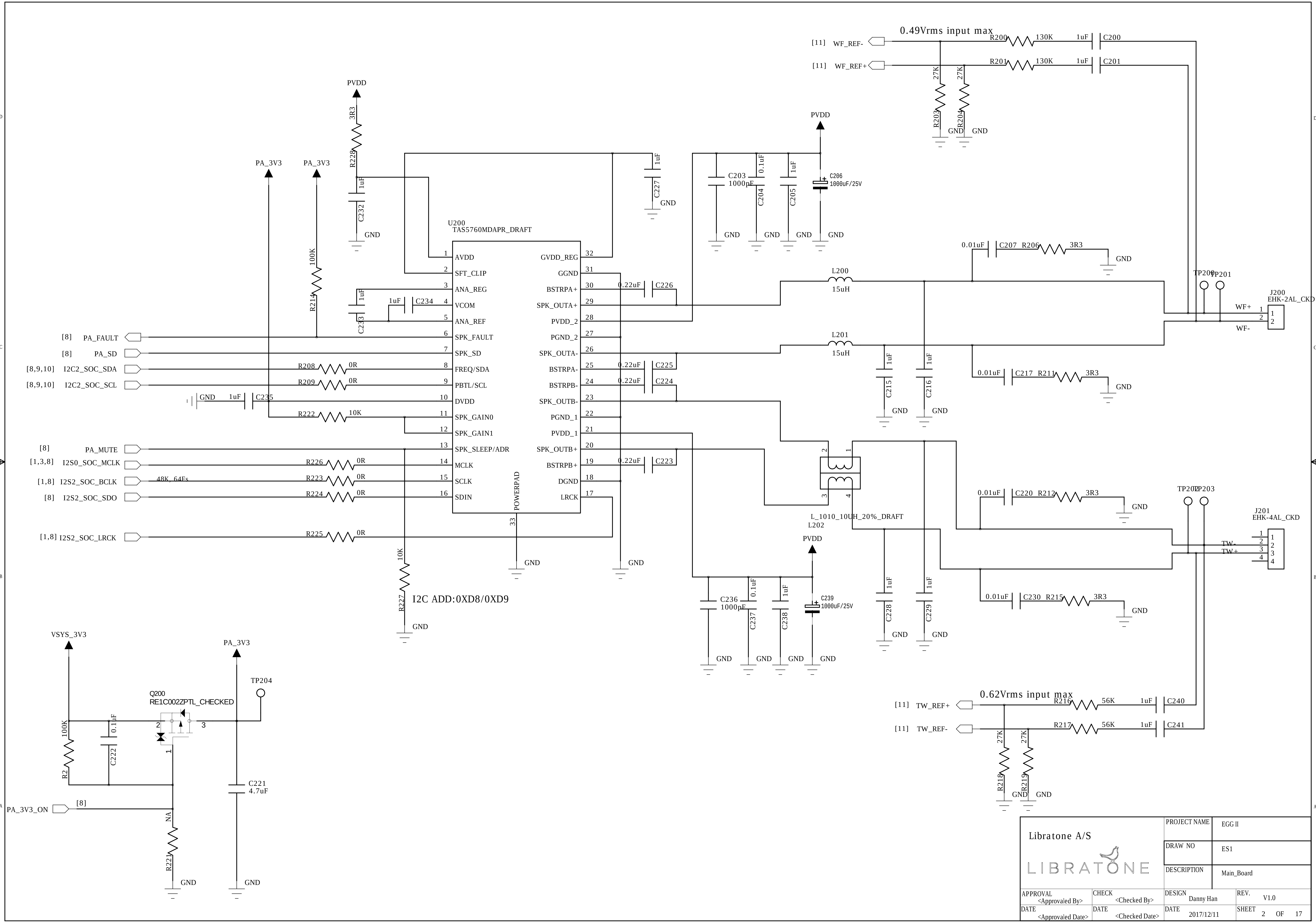

LDO_3V3
ADC_3V3D
ADC_3V3A
R100
0R
R101
0R
ADC_3V3D
C100
0.47uF
GND
10R
GND
R102
NC
R103
10K
R104
U100
AK5720_CKD
AUX_RIGHT
[4]
AUX_LEFT
[4]
R105
3K3
R106
3K3
1uF
C101
1uF
C102
1 VCOM
2 RIN
3 LIN
4 VSS
5 VA
6 VD
7 GSEL
8 REGO
16 CKS
15 FSEL
14 DIF/TDMI
13 PDN
12 BICK
11 MCLK
10 LRCK
9 SDTO
R107
0R
R110
0R
R111
0R
AK5720_PDN [8]
I2S2_SOC_BCLK [2,8]
I2S0_SOC_MCLK [2,3,8]
I2S2_SOC_LRCK [2,8]
I2S2_SOC_SDI [8]
7K5
R108
7K5
R109
GND
GND
1uF
C103
GND
GND
10K
R112
NC
R113
GND
GND
ADC_3V3A
10uF
C104
C105
0.1uF
GND
GND
ADC_3V3D
10uF
C106
C107
0.1uF
GND
GND

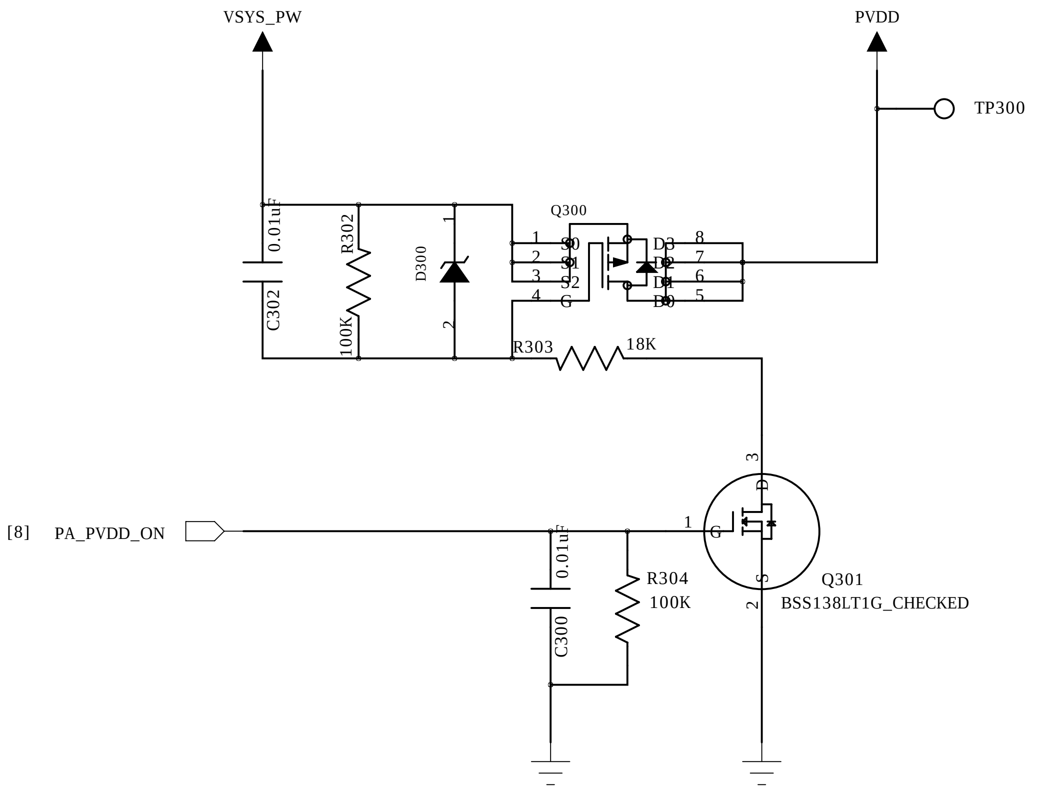
Libratone A/S LIBRATONE	PROJECT NAME	EGG II	
	DRAW NO	ES1	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 1 OF 17

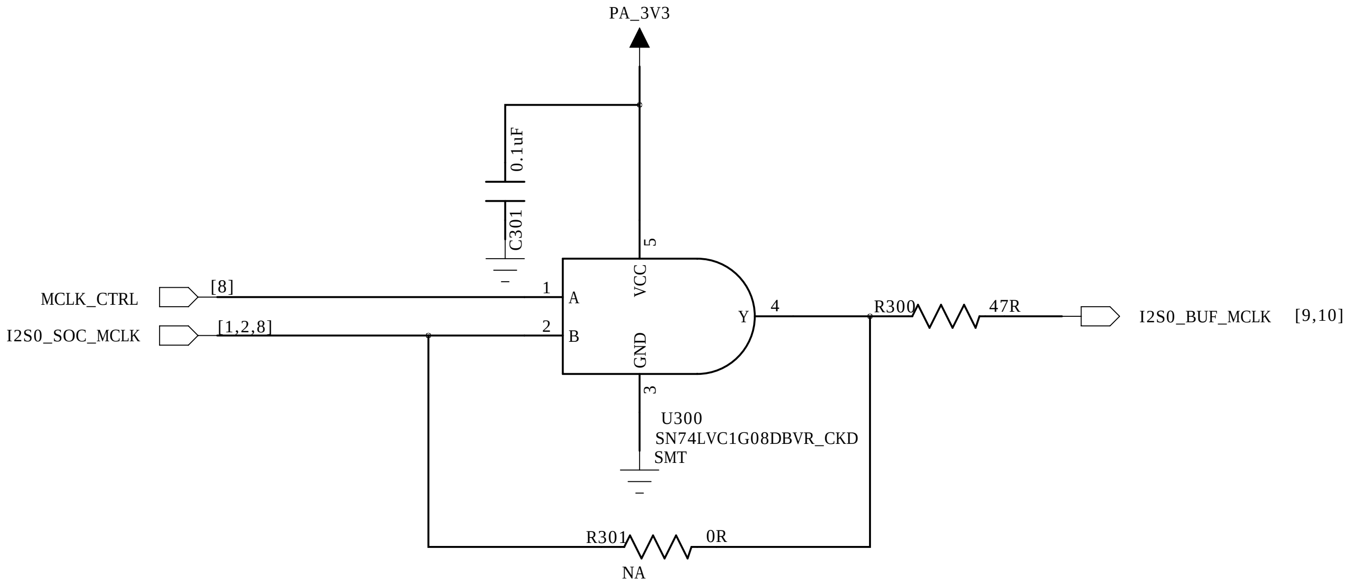

0.49Vrms input max
[11] WF_REF-
[11] WF_REF+
R200 130K 1uF C200
R201 130K 1uF C201
27K R203 GND
27K R204 GND
PVDD
3R3 R228
1uF C232 GND
PA_3V3
PA_3V3
100K R214
1uF C227 GND
PVDD
C203 1000pF GND
0.1uF C204 GND
1uF C205 GND
C206 1000uF/25V GND
U200
TAS5760MDAPR_DRAFT
1 AVDD
2 SFT_CLIP
3 ANA_REG
4 VCOM
5 ANA_REF
6 SPK_FAULT
7 SPK_SD
8 FREQ/SDA
9 PBTL/SCL
10 DVDD
11 SPK_GAIN0
12 SPK_GAIN1
13 SPK_SLEEP/ADR
14 MCLK
15 SCLK
16 SDIN
32 GVDD_REG
31 GGND
30 BSTRPA+
29 SPK_OUTA+
28 PVDD_2
27 PGND_2
26 SPK_OUTA-
25 BSTRPA-
24 BSTRPB-
23 SPK_OUTB-
22 PGND_1
21 PVDD_1
20 SPK_OUTB+
19 BSTRPB+
18 DGND
17 LRCK
33 POWERPAD GND
1uF C233
1uF C234
0.22uF C226
0.22uF C225
0.22uF C224
0.22uF C223
GND
[8] PA_FAULT
[8] PA_SD
[8,9,10] I2C2_SOC_SDA R208 0R
[8,9,10] I2C2_SOC_SCL R209 0R
GND 1uF C235
R222 10K
[8] PA_MUTE
[1,3,8] I2S0_SOC_MCLK R226 0R
[1,8] I2S2_SOC_BCLK 48K, 64Fs R223 0R
[8] I2S2_SOC_SDO R224 0R
[1,8] I2S2_SOC_LRCK R225 0R
10K R227 GND
I2C ADD:0XD8/0XD9
0.01uF C207 R206 3R3 GND
L200 15uH
L201 15uH
0.01uF C217 R211 3R3 GND
1uF C215 GND
1uF C216 GND
TP200 TP201
J200 EHK-2AL_CKD
WF+ 1 1
2 2 WF-
2 1 3 4
L_1010_10UH_20%_DRAFT
L202
0.01uF C220 R212 3R3 GND
TP202 TP203
J201 EHK-4AL_CKD
1 1
2 2 TW-
3 3 TW+
4 4
PVDD
C236 1000pF GND
0.1uF C237 GND
1uF C238 GND
C239 1000uF/25V GND
1uF C228 GND
1uF C229 GND
0.01uF C230 R215 3R3 GND
0.62Vrms input max
[11] TW_REF+ R216 56K 1uF C240
[11] TW_REF- R217 56K 1uF C241
27K R218 GND
27K R219 GND
VSYS_3V3
PA_3V3
TP204
Q200
RE1C002ZPTL_CHECKED
2 3 1
100K R2
0.1uF C222
C221 4.7uF
PA_3V3_ON [8]
NA R221 GND
GND

Libratone A/S

LIBRATONE

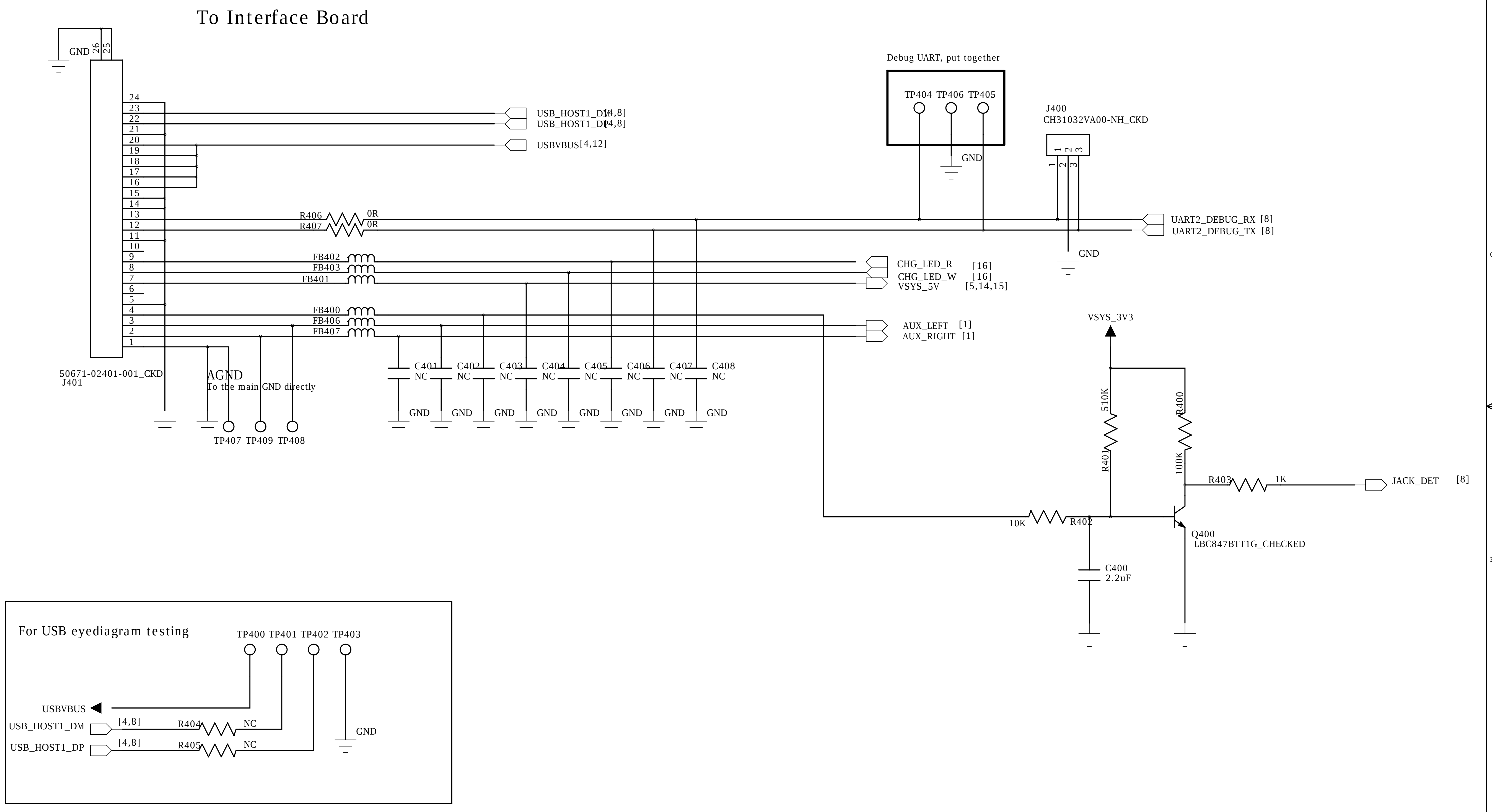
PROJECT NAME	EGG II		
DRAW NO	ES1		
DESCRIPTION	Main_Board		
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 2 OF 17


VSYS_PW
PVDD
TP300
C302
0.01uF
R302
100K
D300
1
2
Q300
1
2
3
4
S0
S1
S2
G
D3
D2
D1
D0
8
7
6
5
R303
18K
3
D
[8]
PA_PVDD_ON
1
G
0.01uF
C300
R304
100K
S
2
Q301
BSS138LT1G_CHECKED


PA_3V3
0.1uF
C301
5
VCC
MCLK_CTRL
[8]
1
A
I2S0_SOC_MCLK
[1,2,8]
2
B
Y
4
GND
3
R300
47R
I2S0_BUF_MCLK
[9,10]
U300
SN74LVC1G08DBVR_CKD
SMT
R301
0R
NA

	EGG Ⅱ	ZIPP3
U900	NA	ON
U1100	NA	ON
U300	NA	ON
R301	ON	NA
C206&C239	470uF	1000uF

Libratone A/S LIBRATONE		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 3 OF 17


To Interface Board
GND
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
50671-02401-001_CKD
J401
USB_HOST1_DM [4,8]
USB_HOST1_DP [4,8]
USBVBUS [4,12]
R406 0R
R407 0R
FB402
FB403
FB401
FB400
FB406
FB407
AGND
To the main GND directly
TP407 TP409 TP408
C401 NC
C402 NC
C403 NC
C404 NC
C405 NC
C406 NC
C407 NC
C408 NC
GND
Debug UART, put together
TP404 TP406 TP405
GND
J400
CH31032VA00-NH_CKD
1 2 3
UART2_DEBUG_RX [8]
UART2_DEBUG_TX [8]
GND
CHG_LED_R [16]
CHG_LED_W [16]
VSYS_5V [5,14,15]
AUX_LEFT [1]
AUX_RIGHT [1]
VSYS_3V3
510K
R401
R400
100K
R403
1K
JACK_DET
[8]
10K
R402
Q400
LBC847BTT1G_CHECKED
C400
2.2uF
For USB eyediagram testing
TP400 TP401 TP402 TP403
USBVBUS
USB_HOST1_DM
[4,8]
R404
NC
USB_HOST1_DP
[4,8]
R405
NC
GND

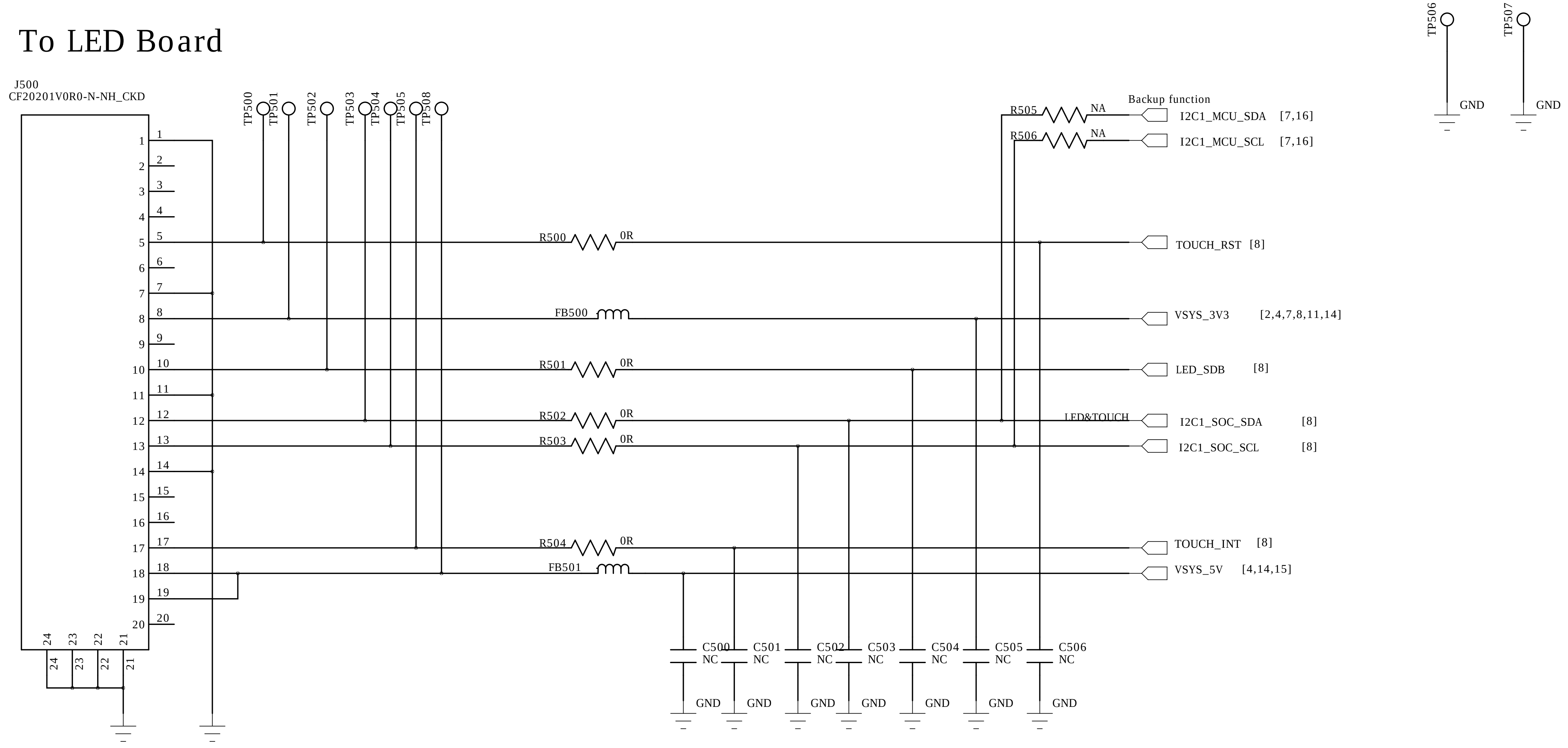
Libratone A/S

LIBRATONE

PROJECT NAME	EGG II
DRAW NO	ES1
DESCRIPTION	Main_Board

APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 4 OF 17

To LED Board


J500
CF20201V0R0-N-NH_CKD
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
24
23
22
21
TP500
TP501
TP502
TP503
TP504
TP505
TP508
TP506
TP507
GND
GND
R500
0R
FB500
R501
0R
R502
0R
R503
0R
R504
0R
FB501
R505
NA
R506
NA
Backup function
I2C1_MCU_SDA [7,16]
I2C1_MCU_SCL [7,16]
TOUCH_RST [8]
VSYS_3V3 [2,4,7,8,11,14]
LED_SDB [8]
LED&TOUCH
I2C1_SOC_SDA [8]
I2C1_SOC_SCL [8]
TOUCH_INT [8]
VSYS_5V [4,14,15]
C500
NC
C501
NC
C502
NC
C503
NC
C504
NC
C505
NC
C506
NC
GND
GND
GND
GND
GND
GND
GND

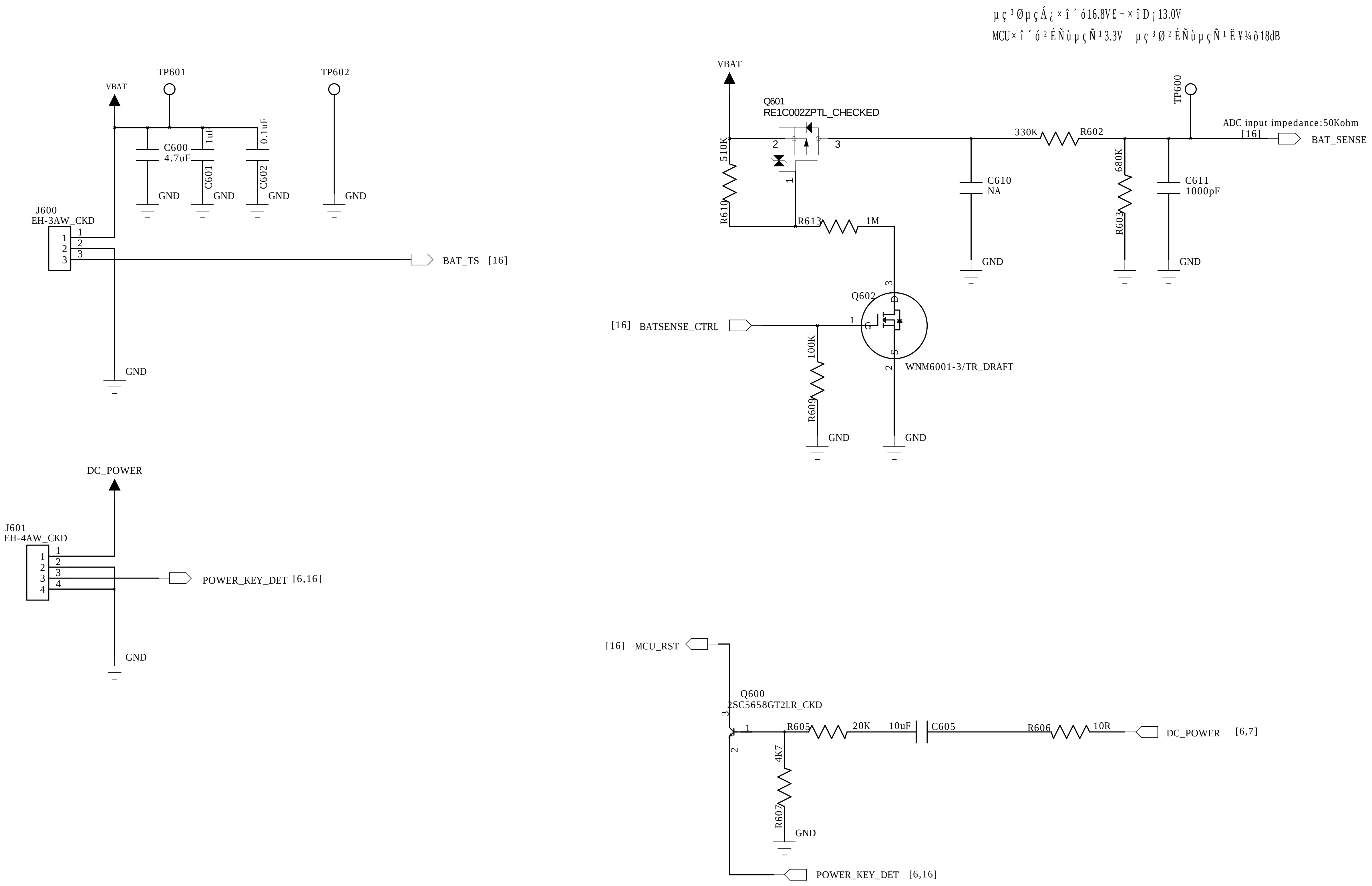
Libratone A/S

LIBRATONE

PROJECT NAME	EGG II				
DRAW NO	ES1				
DESCRIPTION	Main_Board				
APPROVAL	<Approvaled By>	CHECK	<Checked By>	DESIGN	Danny Han
DATE	<Approvaled Date>	DATE	<Checked Date>	DATE	2017/12/11

REV. V1.0

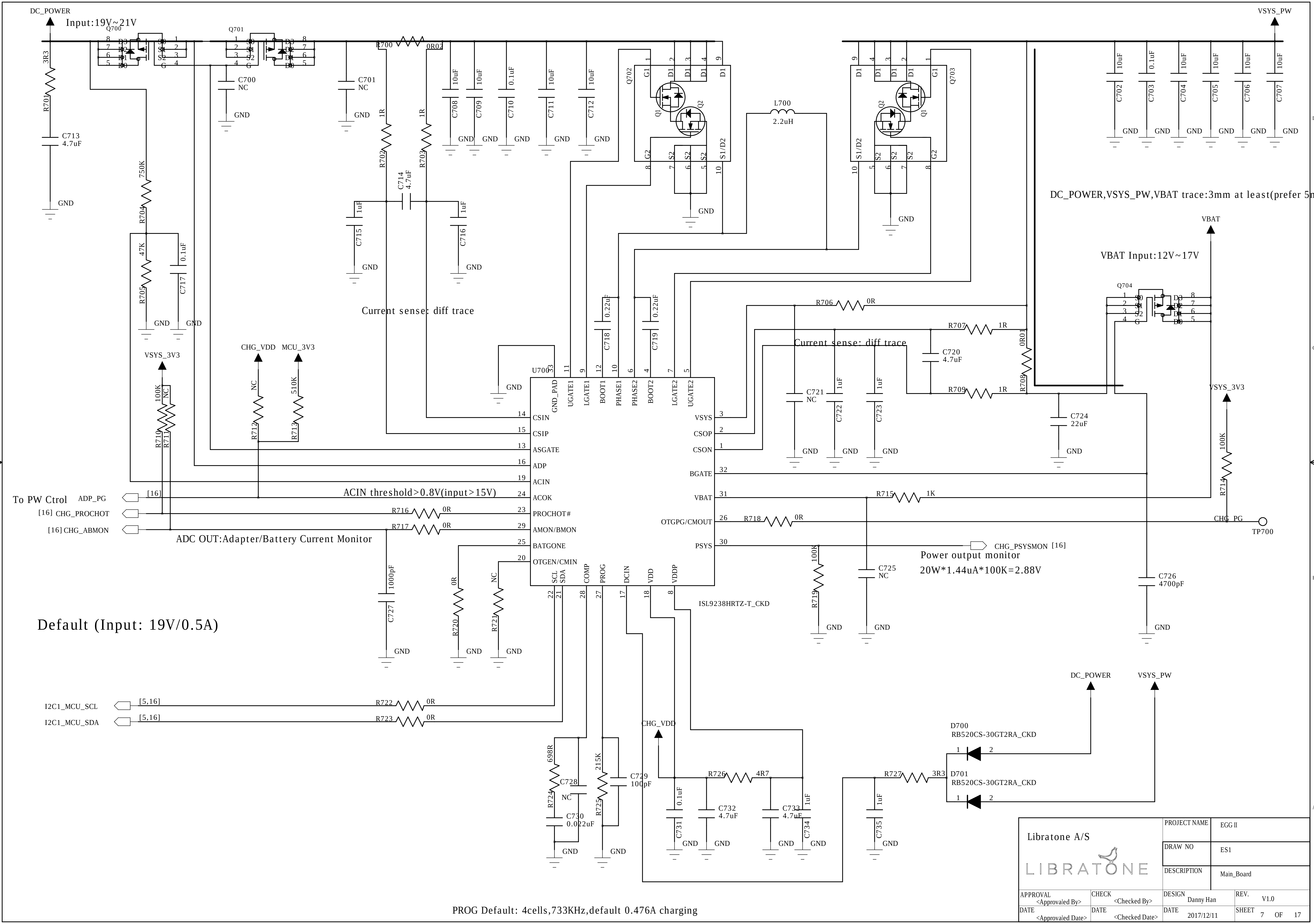
SHEET 5 OF 17


µç³ØµçÁ¿×î´ó16.8V£¬×îÐ¡13.0V
MCU×î´ó²ÉÑùµçÑ¹3.3V µç³Ø²ÉÑùµçÑ¹Ë¥¼õ18dB
TP601
TP602
VBAT
C600
4.7uF
1uF
C601
0.1uF
C602
GND
J600
EH-3AW_CKD
1
2
3
BAT_TS [16]
VBAT
Q601
RE1C002ZPTL_CHECKED
510K
R610
R613
1M
330K
R602
TP600
ADC input impedance:50Kohm
[16]
BAT_SENSE
C610
NA
680K
R603
C611
1000pF
Q602
[16] BATSENSE_CTRL
G
D
S
100K
R609
WNM6001-3/TR_DRAFT
DC_POWER
J601
EH-4AW_CKD
4
POWER_KEY_DET [6,16]
[16] MCU_RST
Q600
2SC5658GT2LR_CKD
R605
20K
10uF
C605
R606
10R
DC_POWER [6,7]
4K7
R607
POWER_KEY_DET [6,16]

Libratone A/S

LIBRATONE

PROJECT NAME	EGG II		
DRAW NO	ES1		
DESCRIPTION	Main_Board		
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 6 OF 17


DC_POWER
VSYS_PW
Q700
Q701
Q702
Q703
Q704
R700 0R02
R701 3R3
C713 4.7uF
R704 750K
R705 47K
C717 0.1uF
C700 NC
C701 NC
R702 1R
R703 1R
C714 4.7uF
C715 1uF
C716 1uF
C708 10uF
C709 10uF
C710 0.1uF
C711 10uF
C712 10uF
L700 2.2uH
C702 10uF
C703 0.1uF
C704 10uF
C705 10uF
C706 10uF
C707 10uF
VBAT
C718 0.22uF
C719 0.22uF
R706 0R
R707 1R
R708 0R01
R709 1R
C720 4.7uF
C721 NC
C722 1uF
C723 1uF
C724 22uF
VSYS_3V3
CHG_VDD
MCU_3V3
R710 100K
R711 NC
R712 NC
R713 510K
U700
GND_PAD
UGATE1
LGATE1
BOOT1
PHASE1
PHASE2
BOOT2
LGATE2
UGATE2
CSIN
CSIP
ASGATE
ADP
ACIN
ACOK
PROCHOT#
AMON/BMON
BATGONE
OTGEN/CMIN
VSYS
CSOP
CSON
BGATE
VBAT
OTGPG/CMOUT
PSYS
SCL
SDA
COMP
PROG
DCIN
VDD
VDDP
ISL9238HRTZ-T_CKD
ADP_PG [16]
[16] CHG_PROCHOT
[16] CHG_ABMON
R716 0R
R717 0R
R714 100K
R715 1K
R718 0R
CHG_PG
TP700
CHG_PSYSMON [16]
R719 100K
C725 NC
C726 4700pF
C727 1000pF
R720 0R
R721 NC
I2C1_MCU_SCL [5,16]
I2C1_MCU_SDA [5,16]
R722 0R
R723 0R
R724 698R
C728 NC
C730 0.022uF
R725 215K
C729 100pF
C731 0.1uF
R726 4R7
C732 4.7uF
C733 4.7uF
C734 1uF
R727 3R3
C735 1uF
D700 RB520CS-30GT2RA_CKD
D701 RB520CS-30GT2RA_CKD
GND

Input:19V~21V

DC_POWER,VSYS_PW,VBAT trace:3mm at least(prefer 5m

VBAT Input:12V~17V

Current sense: diff trace

Current sense: diff trace

To PW Ctrol

ACIN threshold>0.8V(input>15V)

ADC OUT:Adapter/Battery Current Monitor

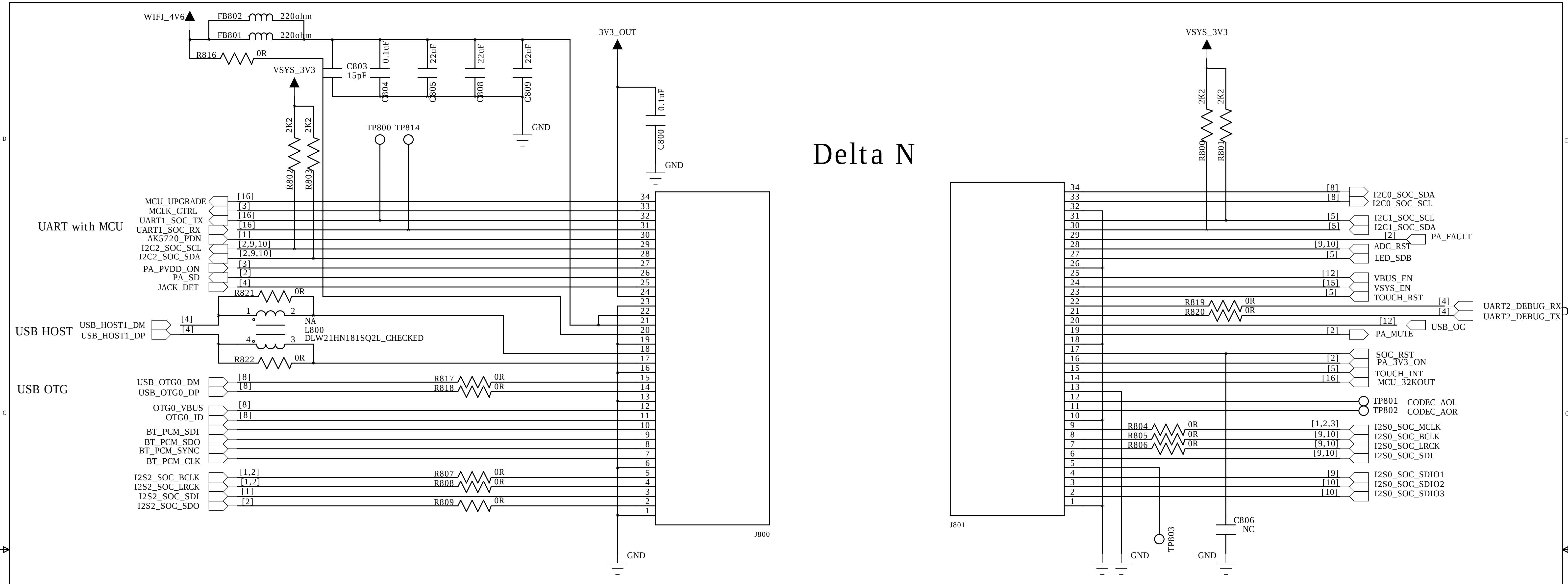
Power output monitor
20W*1.44uA*100K=2.88V

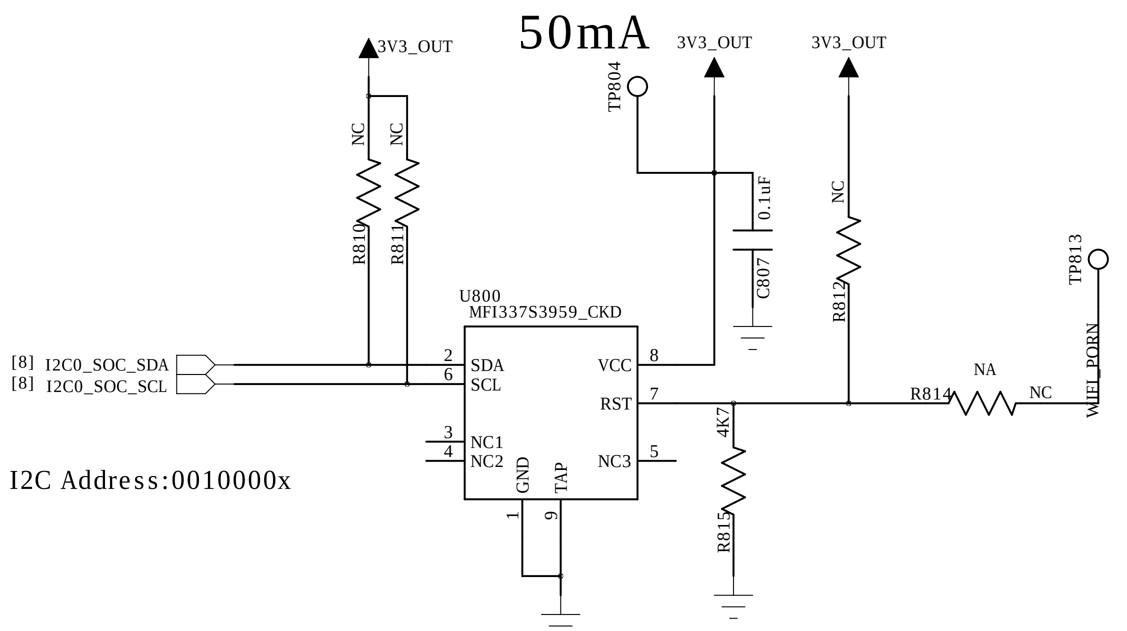
Default (Input: 19V/0.5A)

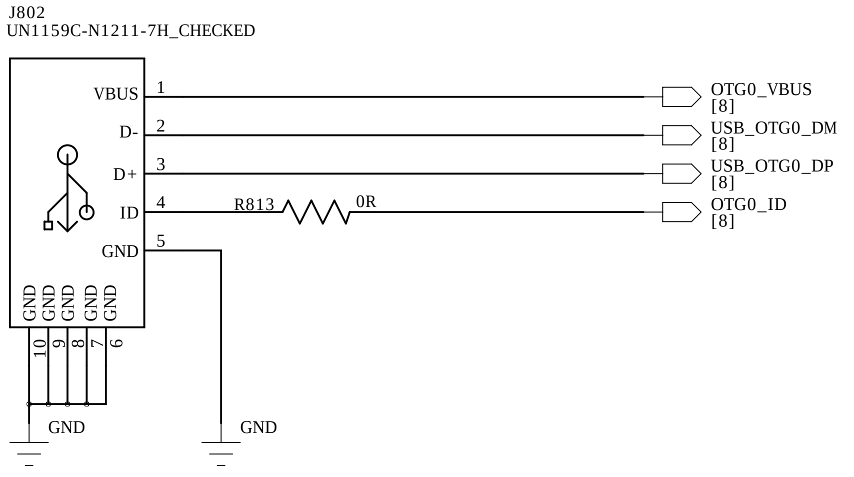
PROG Default: 4cells,733KHz,default 0.476A charging

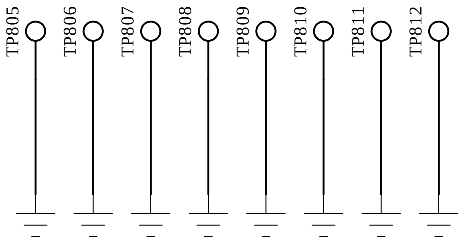
Libratone A/S LIBRATONE	PROJECT NAME	EGG II
	DRAW NO	ES1
	DESCRIPTION	Main_Board

APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 7 OF 17


WIFI_4V6
FB802 220ohm
FB801 220ohm
R816 0R
VSYS_3V3
C803 15pF
0.1uF C804
22uF C805
22uF C808
22uF C809
GND
2K2 R802
2K2 R803
TP800 TP814
3V3_OUT
0.1uF C800
GND
Delta N
UART with MCU
MCU_UPGRADE [16]
MCLK_CTRL [3]
UART1_SOC_TX [16]
UART1_SOC_RX [16]
AK5720_PDN [1]
I2C2_SOC_SCL [2,9,10]
I2C2_SOC_SDA [2,9,10]
PA_PVDD_ON [3]
PA_SD [2]
JACK_DET [4]
R821 0R
USB HOST
USB_HOST1_DM [4]
USB_HOST1_DP [4]
1 2 4 3
NA
L800
DLW21HN181SQ2L_CHECKED
R822 0R
USB OTG
USB_OTG0_DM [8]
USB_OTG0_DP [8]
R817 0R
R818 0R
OTG0_VBUS [8]
OTG0_ID [8]
BT_PCM_SDI
BT_PCM_SDO
BT_PCM_SYNC
BT_PCM_CLK
I2S2_SOC_BCLK [1,2]
I2S2_SOC_LRCK [1,2]
I2S2_SOC_SDI [1]
I2S2_SOC_SDO [2]
R807 0R
R808 0R
R809 0R
34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
J800
GND
VSYS_3V3
2K2 R800
2K2 R801
J801
34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
[8] I2C0_SOC_SDA
[8] I2C0_SOC_SCL
[5] I2C1_SOC_SCL
[5] I2C1_SOC_SDA
[2] PA_FAULT
[9,10] ADC_RST
[5] LED_SDB
[12] VBUS_EN
[15] VSYS_EN
[5] TOUCH_RST
R819 0R
R820 0R
[4] UART2_DEBUG_RX
[4] UART2_DEBUG_TX
[12] USB_OC
[2] PA_MUTE
SOC_RST
[2] PA_3V3_ON
[5] TOUCH_INT
[16] MCU_32KOUT
TP801 CODEC_AOL
TP802 CODEC_AOR
R804 0R
R805 0R
R806 0R
[1,2,3] I2S0_SOC_MCLK
[9,10] I2S0_SOC_BCLK
[9,10] I2S0_SOC_LRCK
[9,10] I2S0_SOC_SDI
[9] I2S0_SOC_SDIO1
[10] I2S0_SOC_SDIO2
[10] I2S0_SOC_SDIO3
C806 NC
TP803
GND
GND


3V3_OUT
50mA
3V3_OUT
3V3_OUT
TP804
NC R810
NC R811
0.1uF C807
NC R812
TP813
U800
MFI337S3959_CKD
[8] I2C0_SOC_SDA
[8] I2C0_SOC_SCL
2 SDA
6 SCL
3 NC1
4 NC2
GND 1
TAP 9
VCC 8
RST 7
NC3 5
4K7 R815
R814 NA NC
WIFI_PORN
I2C Address:0010000x


J802
UN1159C-N1211-7H_CHECKED
VBUS 1
D- 2
D+ 3
ID 4
GND 5
GND GND GND GND GND
10 9 8 7 6
R813 0R
OTG0_VBUS [8]
USB_OTG0_DM [8]
USB_OTG0_DP [8]
OTG0_ID [8]
GND
GND


TP805
TP806
TP807
TP808
TP809
TP810
TP811
TP812

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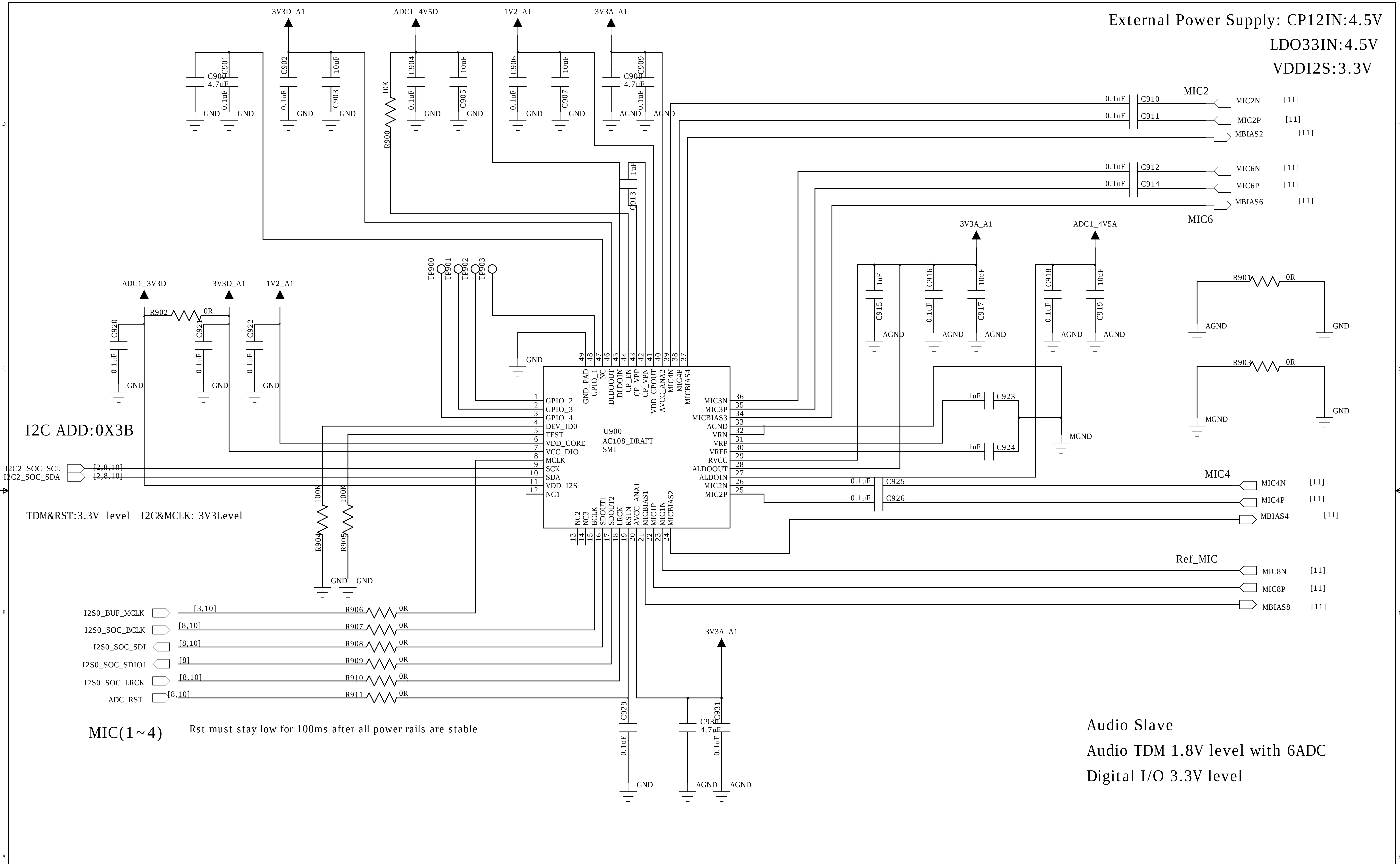
Libratone A/S

LIBRATONE

PROJECT NAME EGG II
DRAW NO ES1
DESCRIPTION Main_Board
APPROVAL <Approvaled By>
CHECK <Checked By>
DESIGN Danny Han
REV. V1.0
DATE <Approvaled Date>
DATE <Checked Date>
DATE 2017/12/11
SHEET 8 OF 17


3V3D_A1
ADC1_4V5D
1V2_A1
3V3A_A1
C900 4.7uF
C901 0.1uF
C902 0.1uF
C903 10uF
C904 0.1uF
C905 10uF
C906 0.1uF
C907 10uF
C908 4.7uF
C909 0.1uF
R900 10K
C913 1uF
GND
AGND
MGND
C910 0.1uF
C911 0.1uF
C912 0.1uF
C914 0.1uF
MIC2
MIC2N [11]
MIC2P [11]
MBIAS2 [11]
MIC6N [11]
MIC6P [11]
MBIAS6 [11]
MIC6
ADC1_4V5A
C915 1uF
C916 0.1uF
C917 10uF
C918 0.1uF
C919 10uF
R901 0R
R903 0R
TP900
TP901
TP902
TP903
ADC1_3V3D
R902 0R
C920 0.1uF
C921 0.1uF
C922 0.1uF
U900
AC108_DRAFT
SMT
1 GPIO_2
2 GPIO_3
3 GPIO_4
4 DEV_ID0
5 TEST
6 VDD_CORE
7 VCC_DIO
8 MCLK
9 SCK
10 SDA
11 VDD_I2S
12 NC1
13 NC2
14 NC3
15 BCLK
16 SDOUT1
17 SDOUT2
18 LRCK
19 RSTN
20 AVCC_ANA1
21 MICBIAS1
22 MIC1P
23 MIC1N
24 MICBIAS2
25 MIC2P
26 MIC2N
27 ALDOIN
28 ALDOOUT
29 RVCC
30 VREF
31 VRP
32 VRN
33 AGND
34 MICBIAS3
35 MIC3P
36 MIC3N
37 MICBIAS4
38 MIC4P
39 MIC4N
40 AVCC_ANA2
41 VDD_CPOUT
42 CP_VPN
43 CP_VPP
44 CP_EN
45 DLDOIN
46 DLDOOUT
47 NC
48 GPIO_1
49 GND_PAD
C923 1uF
C924 1uF
C925 0.1uF
C926 0.1uF
MIC4
MIC4N [11]
MIC4P [11]
MBIAS4 [11]
Ref_MIC
MIC8N [11]
MIC8P [11]
MBIAS8 [11]
I2C2_SOC_SCL [2,8,10]
I2C2_SOC_SDA [2,8,10]
R904 100K
R905 100K
I2S0_BUF_MCLK [3,10]
I2S0_SOC_BCLK [8,10]
I2S0_SOC_SDI [8,10]
I2S0_SOC_SDIO1 [8]
I2S0_SOC_LRCK [8,10]
ADC_RST [8,10]
R906 0R
R907 0R
R908 0R
R909 0R
R910 0R
R911 0R
C929 0.1uF
C930 4.7uF
C931 0.1uF

External Power Supply: CP12IN:4.5V
LDO33IN:4.5V
VDDI2S:3.3V

I2C ADD:0X3B

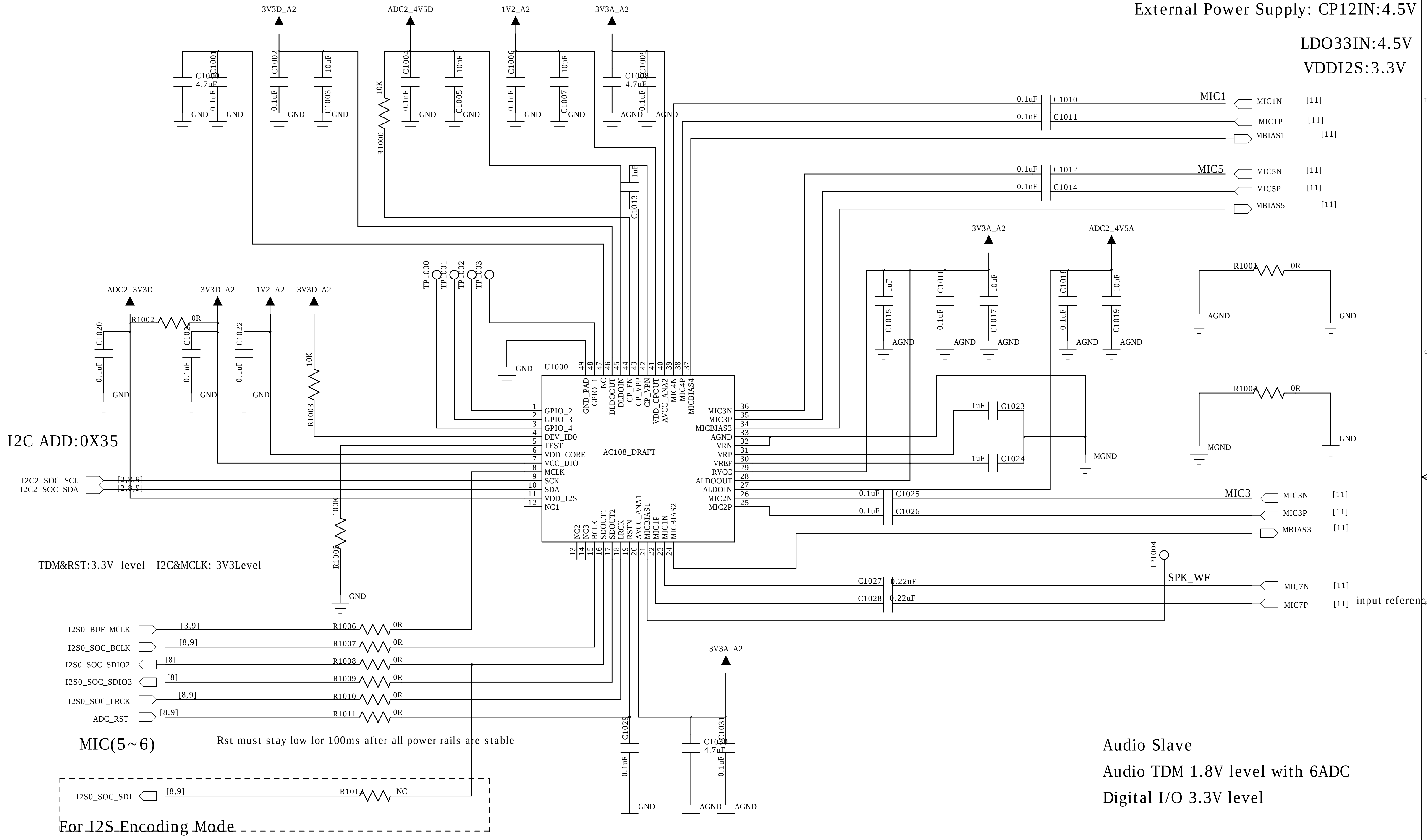
TDM&RST:3.3V level I2C&MCLK: 3V3Level

MIC(1~4)

Rst must stay low for 100ms after all power rails are stable

Audio Slave
Audio TDM 1.8V level with 6ADC
Digital I/O 3.3V level

Libratone A/S LIBRATONE	PROJECT NAME	EGG II	
	DRAW NO	ES1	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 9 OF 17


3V3D_A2
ADC2_4V5D
1V2_A2
3V3A_A2
C1000 4.7uF
C1001 0.1uF
C1002 0.1uF
C1003 10uF
C1004 0.1uF
C1005 10uF
C1006 0.1uF
C1007 10uF
C1008 4.7uF
C1009 0.1uF
R1000 10K
GND
AGND
C1010 0.1uF
C1011 0.1uF
MIC1
MIC1N [11]
MIC1P [11]
MBIAS1 [11]
C1012 0.1uF
C1014 0.1uF
MIC5
MIC5N [11]
MIC5P [11]
MBIAS5 [11]
C1013 1uF
3V3A_A2
ADC2_4V5A
C1015 1uF
C1016 0.1uF
C1017 10uF
C1018 0.1uF
C1019 10uF
R1001 0R
R1004 0R
MGND
ADC2_3V3D
3V3D_A2
1V2_A2
3V3D_A2
R1002 0R
C1020 0.1uF
C1021 0.1uF
C1022 0.1uF
R1003 10K
TP1000
TP1001
TP1002
TP1003
U1000
AC108_DRAFT
GPIO_2
GPIO_3
GPIO_4
DEV_ID0
TEST
VDD_CORE
VCC_DIO
MCLK
SCK
SDA
VDD_I2S
NC1
GND_PAD
GPIO_1
NC
DLDOOUT
DLDOIN
CP_EN
CP_VPP
CP_VPN
VDD_CPOUT
AVCC_ANA2
MIC4N
MIC4P
MICBIAS4
MIC3N
MIC3P
MICBIAS3
AGND
VRN
VRP
VREF
RVCC
ALDOOUT
ALDOIN
MIC2N
MIC2P
NC2
NC3
BCLK
SDOUT1
SDOUT2
LRCK
RSTN
AVCC_ANA1
MICBIAS1
MIC1P
MIC1N
MICBIAS2
C1023 1uF
C1024 1uF
C1025 0.1uF
C1026 0.1uF
MIC3
MIC3N [11]
MIC3P [11]
MBIAS3 [11]
TP1004
SPK_WF
C1027 0.22uF
C1028 0.22uF
MIC7N [11]
MIC7P [11]
input referenc
I2C ADD:0X35
I2C2_SOC_SCL [2,8,9]
I2C2_SOC_SDA [2,8,9]
R1005 100K
TDM&RST:3.3V level I2C&MCLK: 3V3Level
I2S0_BUF_MCLK [3,9]
I2S0_SOC_BCLK [8,9]
I2S0_SOC_SDIO2 [8]
I2S0_SOC_SDIO3 [8]
I2S0_SOC_LRCK [8,9]
ADC_RST [8,9]
R1006 0R
R1007 0R
R1008 0R
R1009 0R
R1010 0R
R1011 0R
MIC(5~6)
Rst must stay low for 100ms after all power rails are stable
I2S0_SOC_SDI [8,9]
R1012 NC
For I2S Encoding Mode
3V3A_A2
C1029 0.1uF
C1030 4.7uF
C1031 0.1uF

External Power Supply: CP12IN:4.5V

LDO33IN:4.5V

VDDI2S:3.3V

Audio Slave

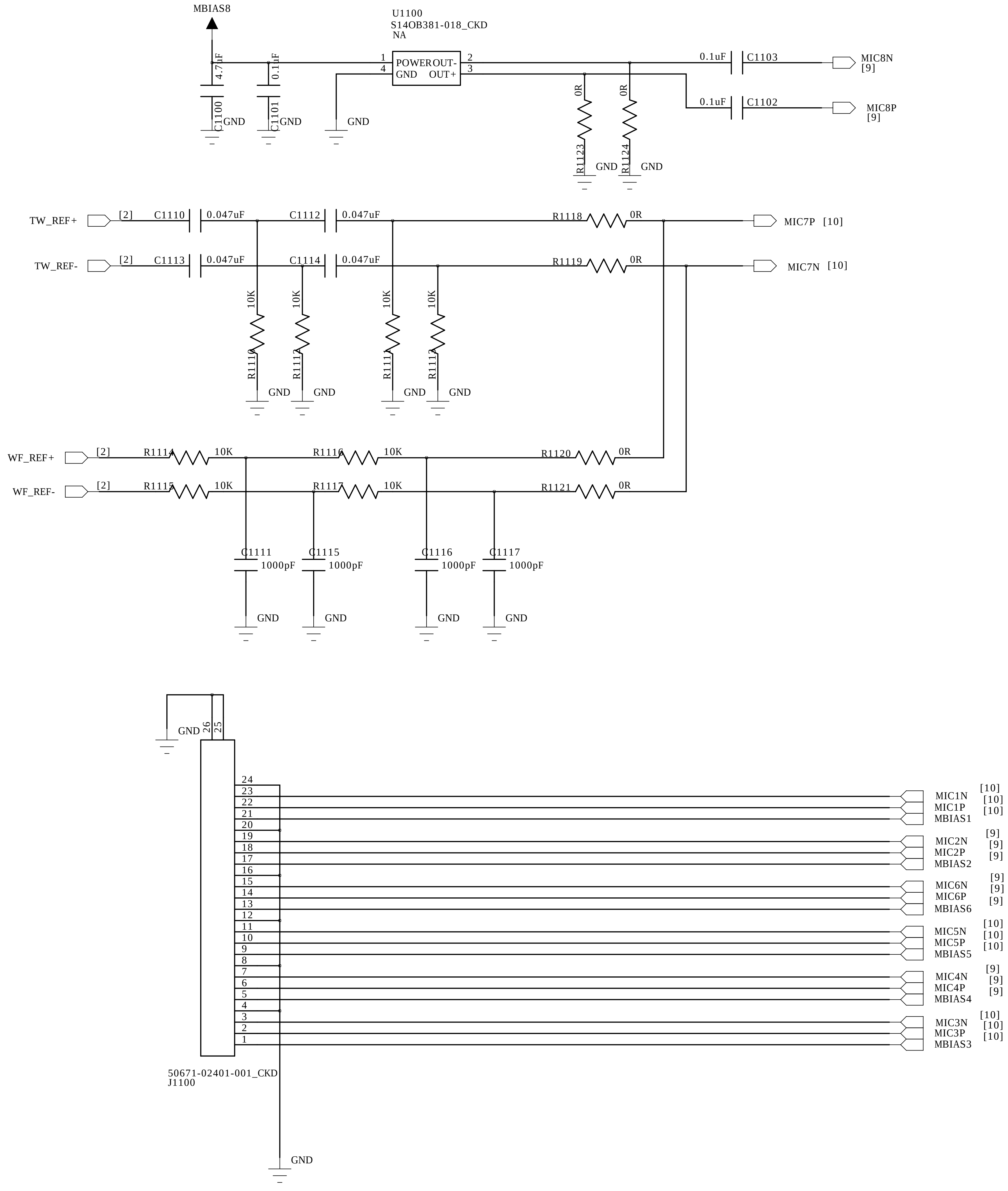
Audio TDM 1.8V level with 6ADC

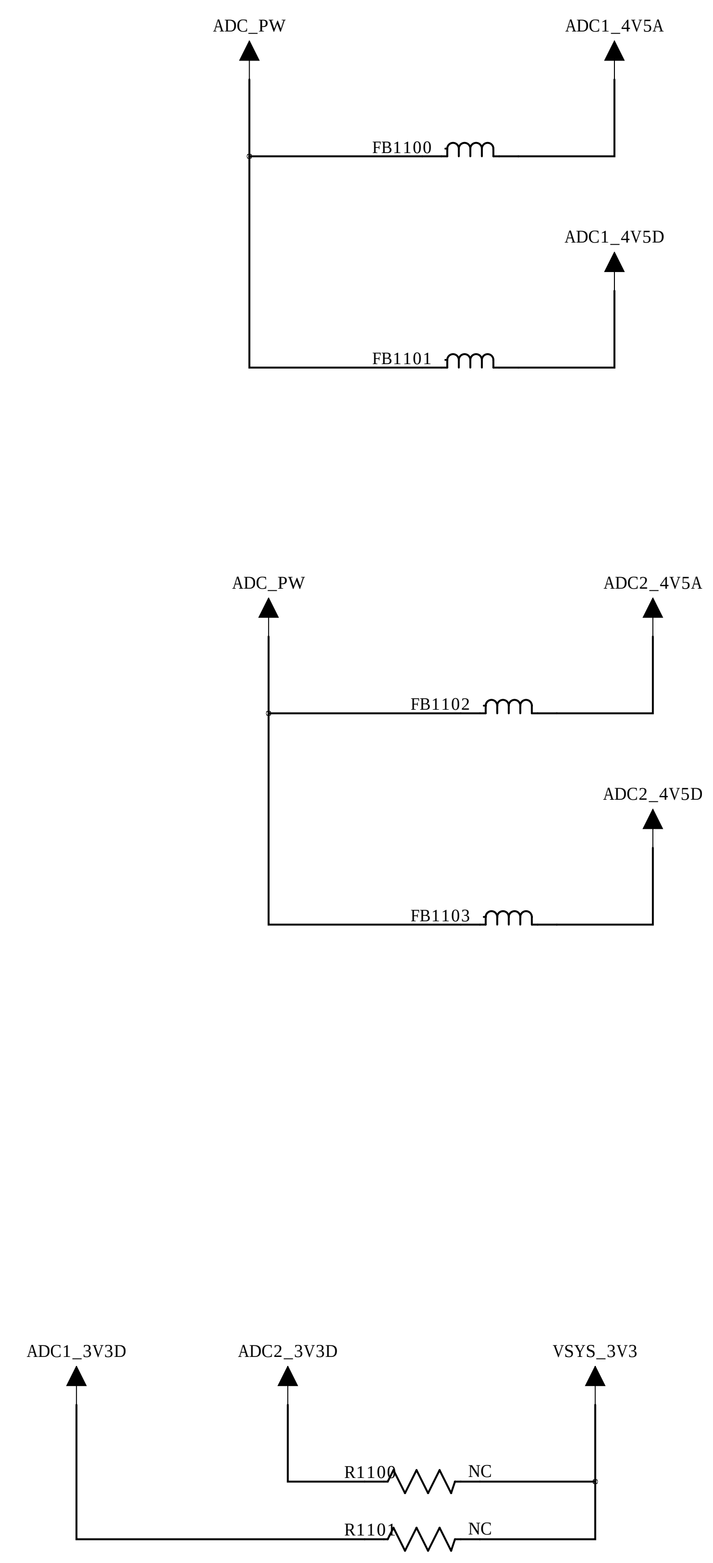
Digital I/O 3.3V level

Libratone A/S

LIBRATONE

PROJECT NAME	EGG II		
DRAW NO	ES1		
DESCRIPTION	Main_Board		
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 10 OF 17


MBIAS8
U1100
S14OB381-018_CKD
NA
POWER
GND
OUT-
OUT+
1
4
2
3
4.7uF
C1100
0.1uF
C1101
GND
GND
GND
0R
R1123
0R
R1124
GND
GND
0.1uF
C1103
MIC8N
[9]
0.1uF
C1102
MIC8P
[9]
TW_REF+
[2]
C1110
0.047uF
C1112
0.047uF
R1118
0R
MIC7P [10]
TW_REF-
[2]
C1113
0.047uF
C1114
0.047uF
R1119
0R
MIC7N [10]
10K
R1110
10K
R1112
10K
R1111
10K
R1113
GND
GND
GND
GND
WF_REF+
[2]
R1114
10K
R1116
10K
R1120
0R
WF_REF-
[2]
R1115
10K
R1117
10K
R1121
0R
C1111
1000pF
C1115
1000pF
C1116
1000pF
C1117
1000pF
GND
GND
GND
GND
GND
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
MIC1N [10]
MIC1P [10]
MBIAS1 [10]
MIC2N [9]
MIC2P [9]
MBIAS2 [9]
MIC6N [9]
MIC6P [9]
MBIAS6 [9]
MIC5N [10]
MIC5P [10]
MBIAS5 [10]
MIC4N [9]
MIC4P [9]
MBIAS4 [9]
MIC3N [10]
MIC3P [10]
MBIAS3 [10]
50671-02401-001_CKD
J1100
GND

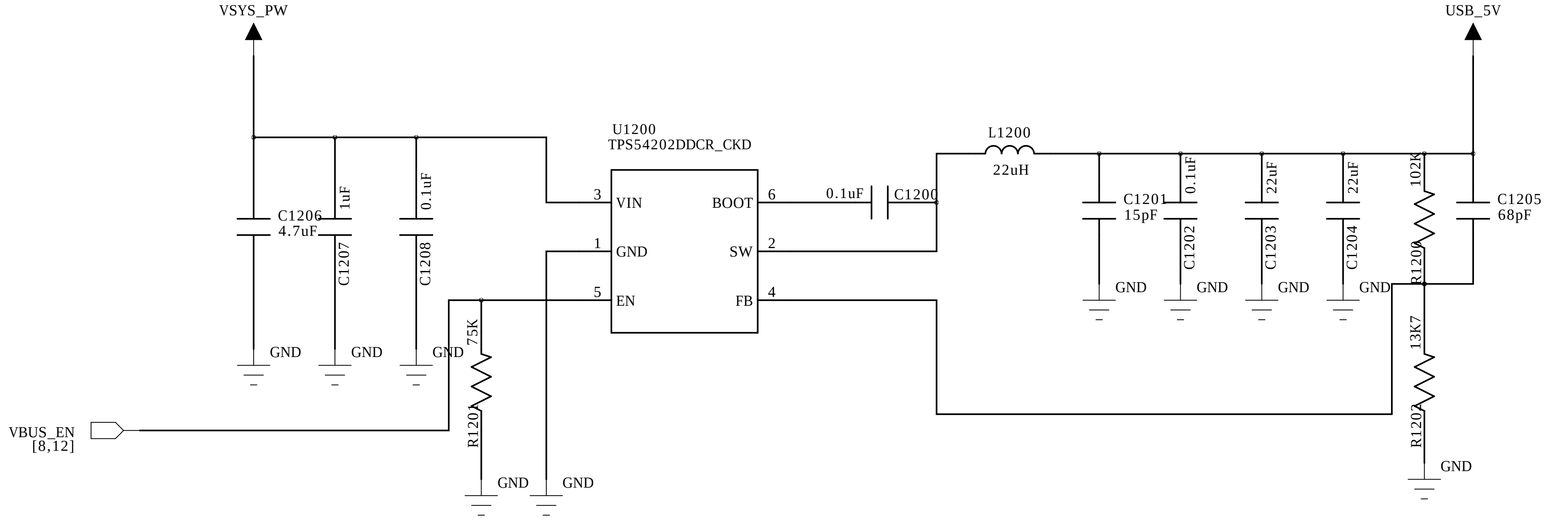

ADC_PW
ADC1_4V5A
FB1100
ADC1_4V5D
FB1101
ADC_PW
ADC2_4V5A
FB1102
ADC2_4V5D
FB1103
ADC1_3V3D
ADC2_3V3D
VSYS_3V3
R1100
NC
R1101
NC

U900-ADC1	Aux_Right/SPK_TW
ADC2	MIC4
ADC3	MIC6
ADC4	MIC2
U1000-ADC1	Aux_Left/SPK_WF
ADC2	MIC3
ADC3	MIC5
ADC4	MIC1

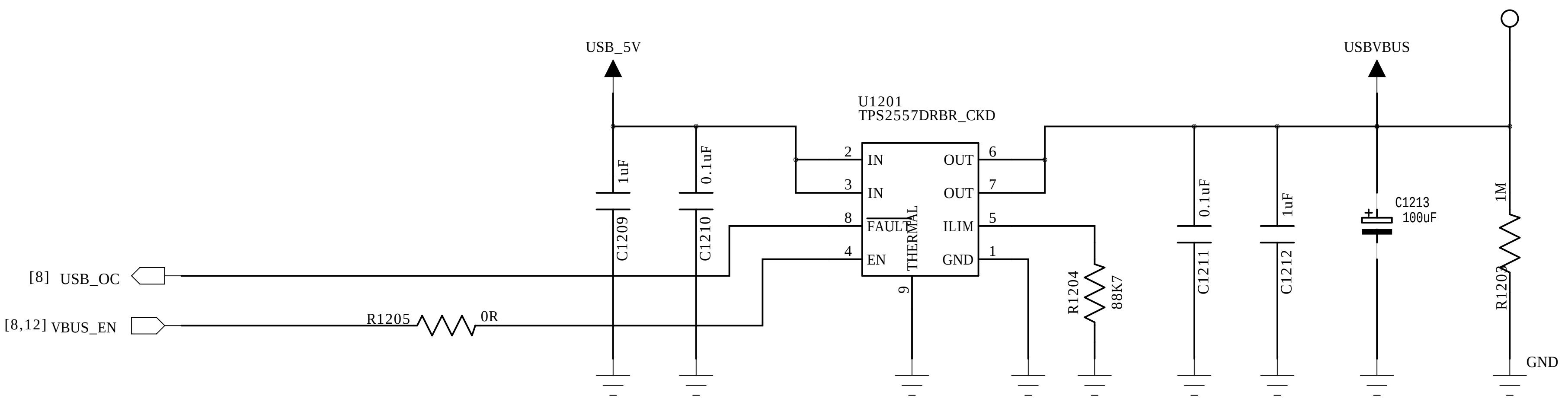
Libratone A/S

LIBRATONE

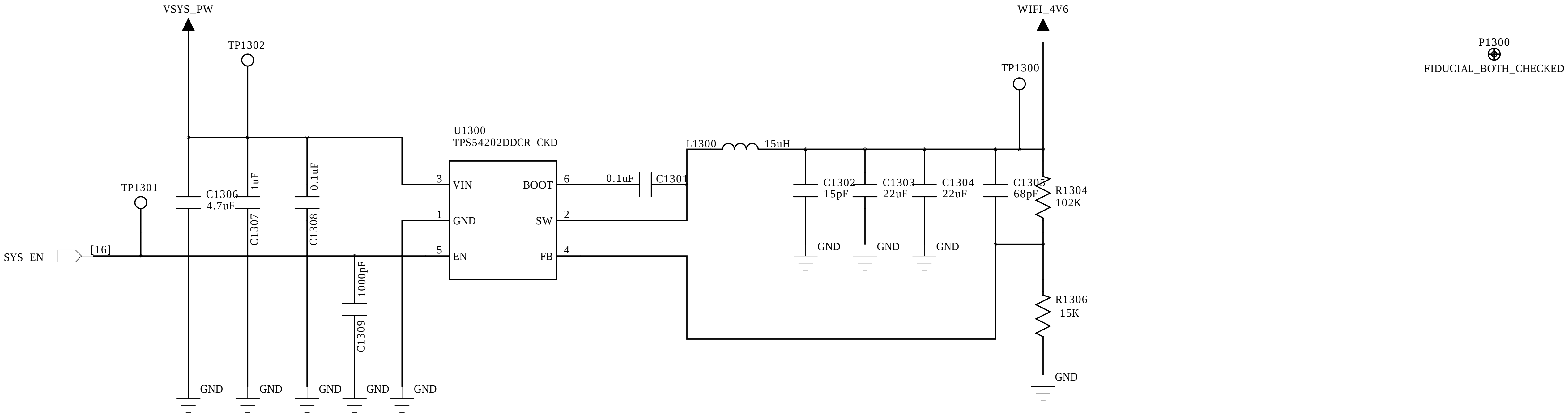
PROJECT NAME	EGG II		
DRAW NO	ES1		
DESCRIPTION	Main_Board		
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 11 OF 17


VSYS_PW
USB_5V
U1200
TPS54202DDCR_CKD
VIN
GND
EN
BOOT
SW
FB
3
1
5
6
2
4
0.1uF
C1200
L1200
22uH
C1206
4.7uF
C1207
1uF
C1208
0.1uF
C1201
15pF
C1202
0.1uF
C1203
22uF
C1204
22uF
C1205
68pF
R1200
102K
R1202
13K7
R1201
75K
VBUS_EN
[8,12]
GND

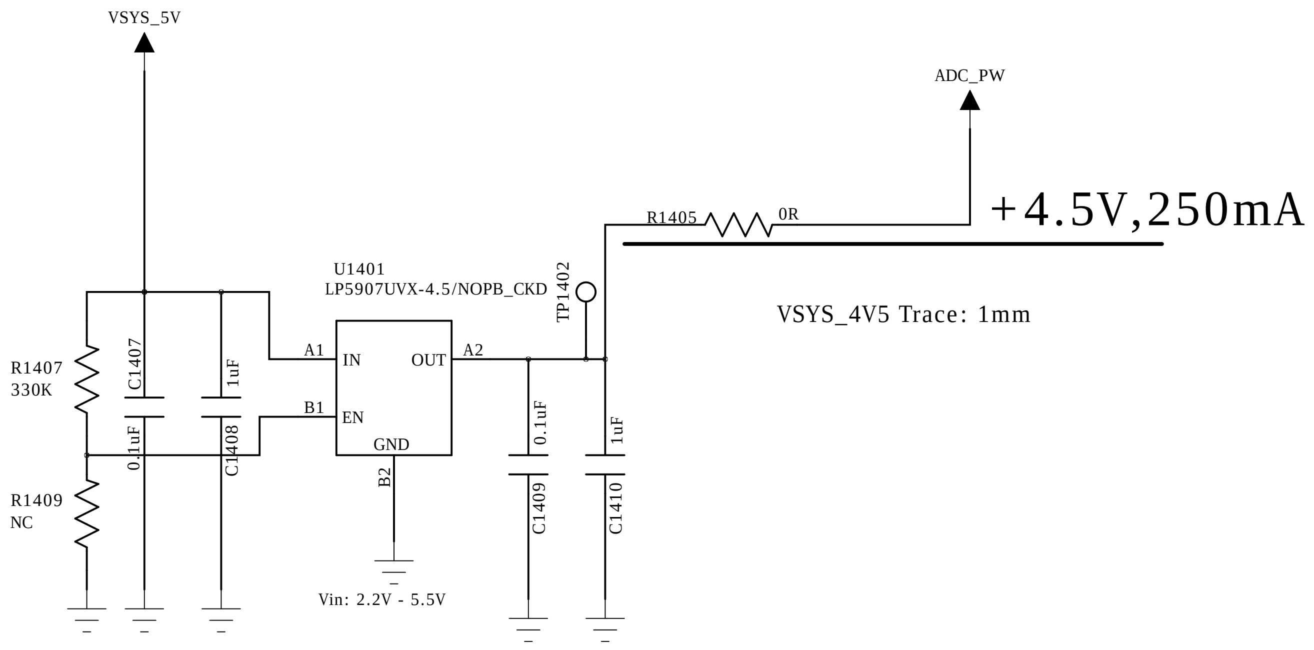
USB Output OCP 1.1Amax

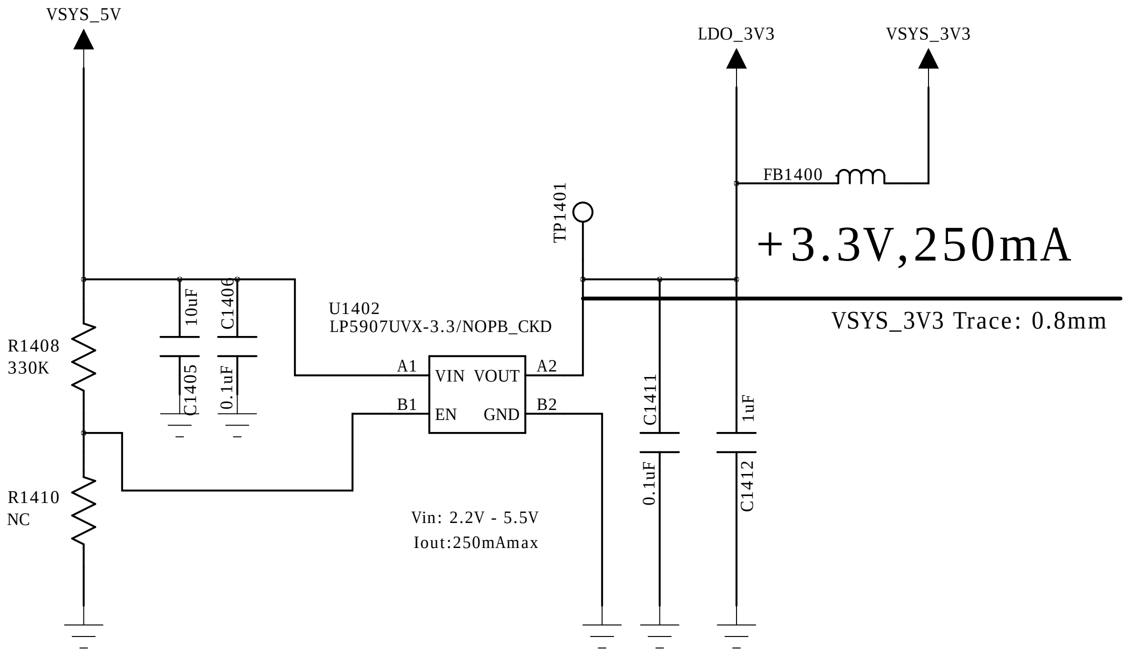

TP1200
USB_5V
USBVBUS
U1201
TPS2557DRBR_CKD
IN
IN
FAULT
EN
OUT
OUT
ILIM
GND
THERMAL
2
3
8
4
6
7
5
1
9
C1209
1uF
C1210
0.1uF
C1211
0.1uF
C1212
1uF
C1213
100uF
R1204
88K7
R1203
1M
R1205
0R
[8] USB_OC
[8,12] VBUS_EN
GND

Libratone A/S LIBRATONE		PROJECT NAME	EGG II		
		DRAW NO	ES1		
		DESCRIPTION	Main_Board		
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN	Danny Han	REV.	V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE	2017/12/11	SHEET	12 OF 17


VSYS_PW
TP1302
TP1301
C1306
4.7uF
1uF
C1307
0.1uF
C1308
1000pF
C1309
SYS_EN
[16]
U1300
TPS54202DDCR_CKD
3 VIN
1 GND
5 EN
BOOT 6
SW 2
FB 4
0.1uF
C1301
L1300
15uH
C1302
15pF
C1303
22uF
C1304
22uF
C1305
68pF
R1304
102K
R1306
15K
WIFI_4V6
TP1300
GND
P1300
FIDUCIAL_BOTH_CHECKED

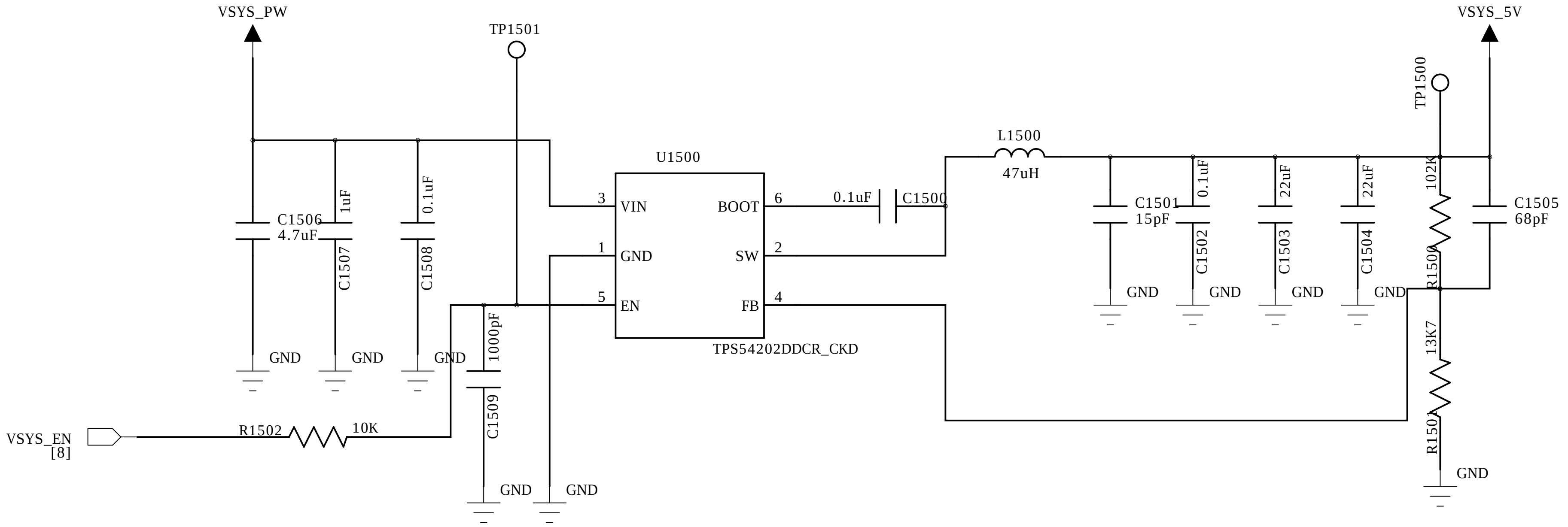
Libratone A/S	PROJECT NAME	EGG II	
	DRAW NO	ES1	
	DESCRIPTION	Main_Board	
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 13 OF 17


VSYS_5V
ADC_PW
R1405
0R
+4.5V,250mA
U1401
LP5907UVX-4.5/NOPB_CKD
TP1402
VSYS_4V5 Trace: 1mm
R1407
330K
C1407
0.1uF
1uF
C1408
A1
IN
OUT
A2
B1
EN
GND
B2
0.1uF
C1409
1uF
C1410
R1409
NC
Vin: 2.2V - 5.5V


VSYS_5V
LDO_3V3
VSYS_3V3
FB1400
TP1401
+3.3V,250mA
VSYS_3V3 Trace: 0.8mm
10uF
C1406
C1405
0.1uF
U1402
LP5907UVX-3.3/NOPB_CKD
R1408
330K
A1
VIN
VOUT
A2
B1
EN
GND
B2
C1411
0.1uF
1uF
C1412
R1410
NC
Vin: 2.2V - 5.5V
Iout:250mAmax

Libratone A/S LIBRATONE	PROJECT NAME	EGG II
	DRAW NO	ES1
	DESCRIPTION	Main_Board

APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 14 OF 17

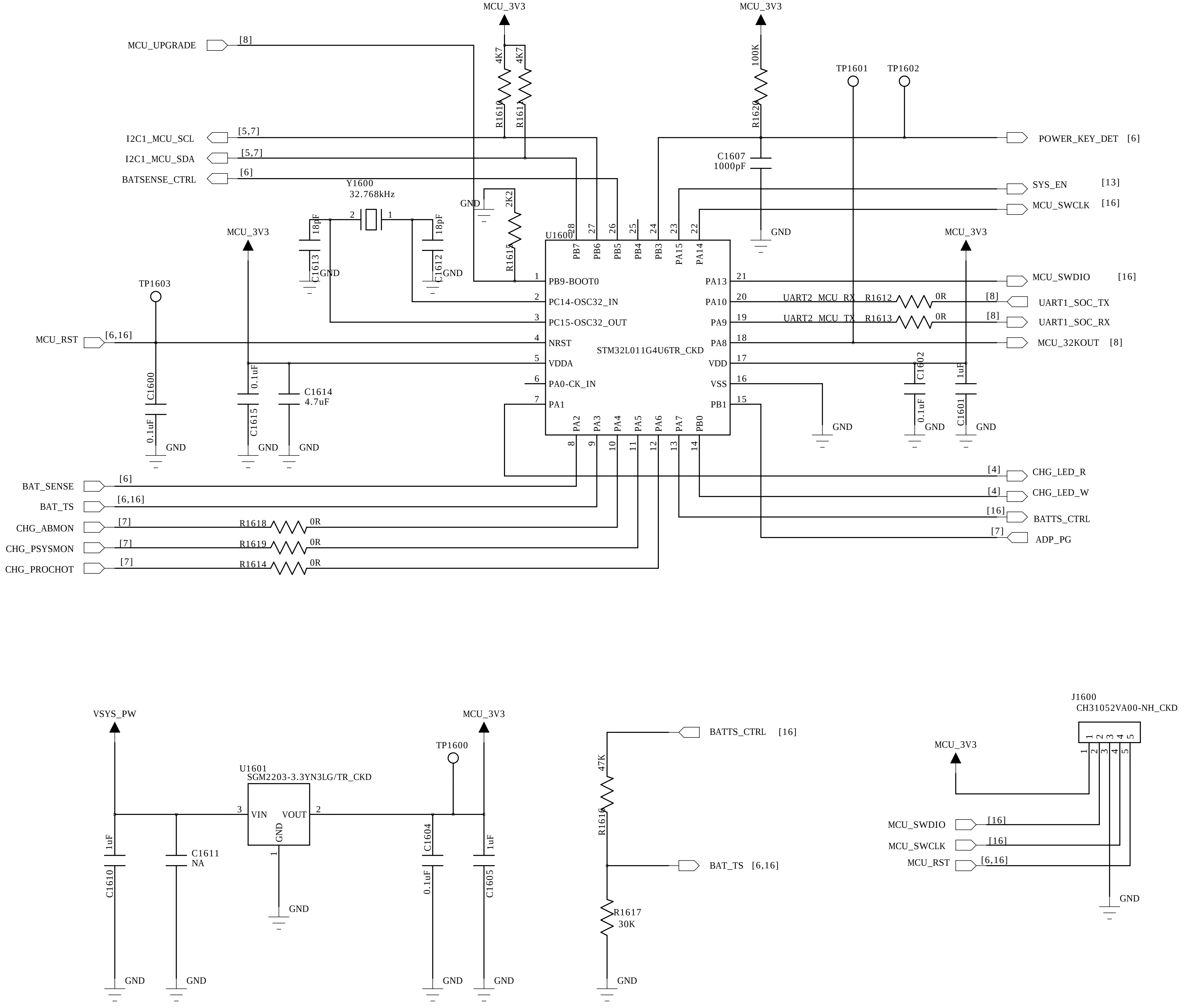

VSYS_PW
TP1501
VSYS_5V
TP1500
U1500
L1500
47uH
3 VIN
1 GND
5 EN
BOOT 6
SW 2
FB 4
TPS54202DDCR_CKD
0.1uF
C1500
C1506
4.7uF
C1507
1uF
C1508
0.1uF
C1509
1000pF
C1501
15pF
C1502
0.1uF
C1503
22uF
C1504
22uF
C1505
68pF
R1500
102K
R1501
13K7
VSYS_EN
[8]
R1502
10K
GND

Libratone A/S

LIBRATONE

PROJECT NAME	EGG II
DRAW NO	ES1
DESCRIPTION	Main_Board

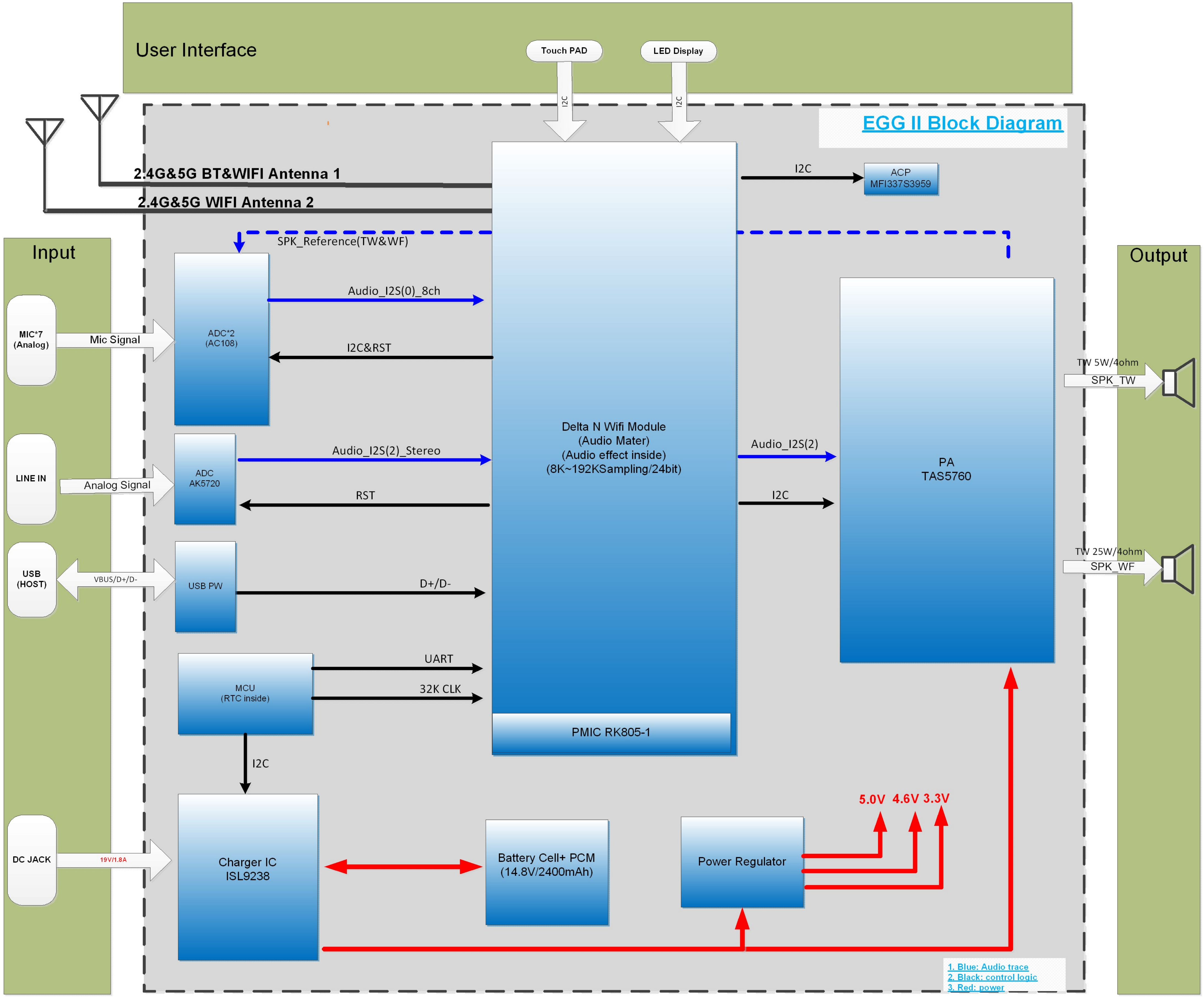
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 15 OF 17


MCU_3V3
MCU_3V3
MCU_UPGRADE
[8]
4K7
4K7
R1610
R1611
100K
R1620
TP1601
TP1602
I2C1_MCU_SCL
[5,7]
I2C1_MCU_SDA
[5,7]
BATSENSE_CTRL
[6]
POWER_KEY_DET [6]
C1607
1000pF
SYS_EN
[13]
MCU_SWCLK
[16]
Y1600
32.768kHz
GND
2K2
R1615
18pF
C1613
18pF
C1612
GND
GND
GND
MCU_3V3
U1600
MCU_3V3
TP1603
STM32L011G4U6TR_CKD
PB7
PB6
PB5
PB4
PB3
PA15
PA14
PB9-BOOT0
PC14-OSC32_IN
PC15-OSC32_OUT
NRST
VDDA
PA0-CK_IN
PA1
PA13
PA10
PA9
PA8
VDD
VSS
PB1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
MCU_SWDIO
[16]
UART2_MCU_RX
R1612
0R
[8]
UART1_SOC_TX
UART2_MCU_TX
R1613
0R
[8]
UART1_SOC_RX
MCU_32KOUT
[8]
MCU_RST
[6,16]
C1600
0.1uF
0.1uF
C1615
C1614
4.7uF
C1602
0.1uF
1uF
C1601
GND
CHG_LED_R
[4]
CHG_LED_W
[4]
BATTS_CTRL
[16]
ADP_PG
[7]
BAT_SENSE
[6]
BAT_TS
[6,16]
CHG_ABMON
[7]
R1618
0R
CHG_PSYSMON
[7]
R1619
0R
CHG_PROCHOT
[7]
R1614
0R
VSYS_PW
MCU_3V3
TP1600
U1601
SGM2203-3.3YN3LG/TR_CKD
VIN
VOUT
GND
1uF
C1610
C1611
NA
C1604
0.1uF
1uF
C1605
GND
BATTS_CTRL [16]
47K
R1616
BAT_TS [6,16]
R1617
30K
GND
J1600
CH31052VA00-NH_CKD
MCU_3V3
MCU_SWDIO
[16]
MCU_SWCLK
[16]
MCU_RST
[6,16]
GND

Libratone A/S

LIBRATONE

PROJECT NAME EGG II
DRAW NO ES1
DESCRIPTION Main_Board
APPROVAL <Approvaled By>
CHECK <Checked By>
DESIGN Danny Han
REV. V1.0
DATE <Approvaled Date>
DATE <Checked Date>
DATE 2017/12/11
SHEET 16 OF 17


EGG II Block Diagram
User Interface
Touch PAD
LED Display
I2C
I2C
2.4G&5G BT&WIFI Antenna 1
2.4G&5G WIFI Antenna 2
I2C
ACP
MFI337S3959
SPK_Reference(TW&WF)
Input
MIC*7
(Analog)
Mic Signal
ADC*2
(AC108)
Audio_I2S(0)_8ch
I2C&RST
LINE IN
Analog Signal
ADC
AK5720
Audio_I2S(2)_Stereo
RST
USB
(HOST)
VBUS/D+/D-
USB PW
D+/D-
MCU
(RTC inside)
UART
32K CLK
I2C
Delta N Wifi Module
(Audio Mater)
(Audio effect inside)
(8K~192KSampling/24bit)
PMIC RK805-1
Audio_I2S(2)
I2C
PA
TAS5760
Output
TW 5W/4ohm
SPK_TW
TW 25W/4ohm
SPK_WF
DC JACK
19V/1.8A
Charger IC
ISL9238
Battery Cell+ PCM
(14.8V/2400mAh)
Power Regulator
5.0V
4.6V
3.3V
1. Blue: Audio trace
2. Black: control logic
3. Red: power

Libratone A/S LIBRATONE		PROJECT NAME	EGG II
		DRAW NO	ES1
		DESCRIPTION	Main_Board
APPROVAL <Approvaled By>	CHECK <Checked By>	DESIGN Danny Han	REV. V1.0
DATE <Approvaled Date>	DATE <Checked Date>	DATE 2017/12/11	SHEET 17 OF 17