

a-Si TFT LCD Single-Chip Driver 480(RGB) x 864 Resolution 16.7M-color with Internal GRAM

Specification Preliminary

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1. Introduction

The ILI9806 is a 16.7M single-chip SOC driver for a-Si TFT liquid crystal display panels with a resolution of up to 480 (RGB) x 864 memory size. The ILI9806 is comprised of a 1440-channel source driver, a gate-IC-less level shifter, a 1,244,160-byte GRAM for graphic data of 480 (RGB) x 864 dots, and a power supply circuit.

The ILI9806 supports parallel MPU 8-/9-/16-/18-/24-bit data bus interfaces and a 3-line serial peripheral interface to input commands. The ILI9806 supports a RGB (16-/18-/24-bit) data bus for video image display. For high-speed serial interface, the MIPI DSI and MDDI (Mobile Display Digital Interface) interface mode, the ILI9806 supports two data lanes and one clock lane for high-speed and low power transmission in both directions with low EMI noise.

The ILI9806 operates with a wide range of an analog power supply. The ILI9806 supports 8-color display, sleep mode and deep standby power management functions, ideal for medium or small size portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players, and similar devices with color graphics display. Additionally, it has an internal DC/DC converter that generates the LCD driving voltage and the voltage follower circuit for LCD driver.

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2. Features

- Display resolution options:
 - > 480 (RGB) (H) x 864 (V) with GRAM
 - > 480 (RGB) (H) x 854 (V) with GRAM
 - > 480 (RGB) (H) x 800 (V) with GRAM
 - > 480 (RGB) (H) x 720 (V) with GRAM
 - > 480 (RGB) (H) x 640 (V) with GRAM
- Display color modes
 - > Full color mode:

16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)

Reduced color modes:

262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)

65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)

8 colors (Idle Mode On): 8 colors (3-bit data, R: 1-bit, G: 1-bit, B: 1-bit)

- Display module:
 - On-chip Frame Memory size 1,244,160 bytes, 480 (RGB) (H) x 864 (V) x 24 bits
 - > Supports 1440 source channel outputs
 - Supports gate control signals to gate driver in the panel
 - Supports 1-dot/2-dot/3-dot/4-dot/column/Zigzag inversion
 - Gamma correction (1 preset Gamma curve)
 - > On module VCOM control (VCL+0.2V to 0V common electrode output voltage range)
- Display interface types:
 - > MPU mode:

MIPI-DBI Type B (Display Bus Interface, 80 System) interface, 8/9/16/18/24-bit bus

MIPI-DBI Type C (Serial data transfer interface, 3-line SPI) interface

MIPI-DSI (Display Serial Interface) interface:

Supports one data lane/maximum speed 850Mbps or

Supports two data lanes/maximum speed 500Mbps

Supports DSI version 1.01.00

Supports D-PHY version 1.00.00

Supports DCS version 1.02.00

MDDI (Mobile Display Serial Interface):

Supports one data lane/maximum speed 800Mbps or

Supports two data lanes/maximum speed 400Mbps

Supports MDDI V1.2 1 strobe

> MIPI-DPI (Display Pixel Interface) interface:

16 bit/pixel (R: 5-bit, G: 6-bit, B: 5-bit)

18 bit/pixel (R: 6-bit, G: 6-bit, B: 6-bit)

24 bit/pixel (R: 8-bit, G: 8-bit, B: 8-bit)





- Power saving modes:
 - Deep-standby mode
 - Sleep mode
- Other on-chip functions/Miscellaneous
 - > Supports inversion mode
 - Software programmable color depth mode
 - Oscillator for display clock generation
 - Supports DC VCOM driving
 - > DC VCOM voltage generator and adjustment
 - > OTP (One-Time Programming) memory store initialization register settings
 - > Provide 3 times to store DC VCOM value setting, ID setting
 - Supports CABC (Content Adaptive Brightness Control) function
 - > Supports 3-Gamma DGC (Digital Gamma Correction) function
 - Color enhancement function
 - DC/DC converter
 - VGH/VGLO voltage generator for gate control signal in panel
 - > Supports gate control signals to gate driver in panel (GIP)
- Input power:
 - ► I/O supply voltage range for VDDI to VSSI = 1.65V ~ 3.3V (VDDI)
 - Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR = 2.5V ~ 3.3V
 - ➤ MIPI/MDDI regulator range for VDDAM to VSSAM = 2.5V ~ 3.3V
 - > OTP programming voltage, VPP = 7.5V
- Source/VCOM/Gate power supply voltage:
 - > AVDD-AVSS = 4.75 to 6.5V (Step-up 1 output voltage range)
 - > AVEE-AVSS = -6.5 to -4.75V (Step-up 2 output voltage range)
 - VCL-GND = -VCl to -1.8V (Step-up 3 output voltage range)
 - ▶ DC VCOM = VCL+0.2V to 0V, a step 12.5mV (Common electrode voltage range)
 - > VGMP = 3.0V to 6.1875V (AVDD-0.3V) (Positive gamma high voltage range)
 - > VGSP = 0.0V to 3.475V (Positive gamma low voltage range)
 - > VGMN = -3.0V to -6.1875V (AVEE+0.3V) (Negative gamma high voltage range)
 - ➤ VGSN = 0.0V to -3.475V (Negative gamma low voltage range)
 - > VGH-AVSS = 12V to 20V (Positive gate driver output voltage range)
 - ➤ VGL-AVSS = -7V to -15V (Negative gate driver output voltage range)
 - LVGL-AVSS = -7V to -15V (Negative gate driver output voltage range)
 - > VRGH = 1.0V ~ 6.0V (AVDD-0.3V) (Panel voltage range)

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3. Device Overview

3.1. Block Diagram

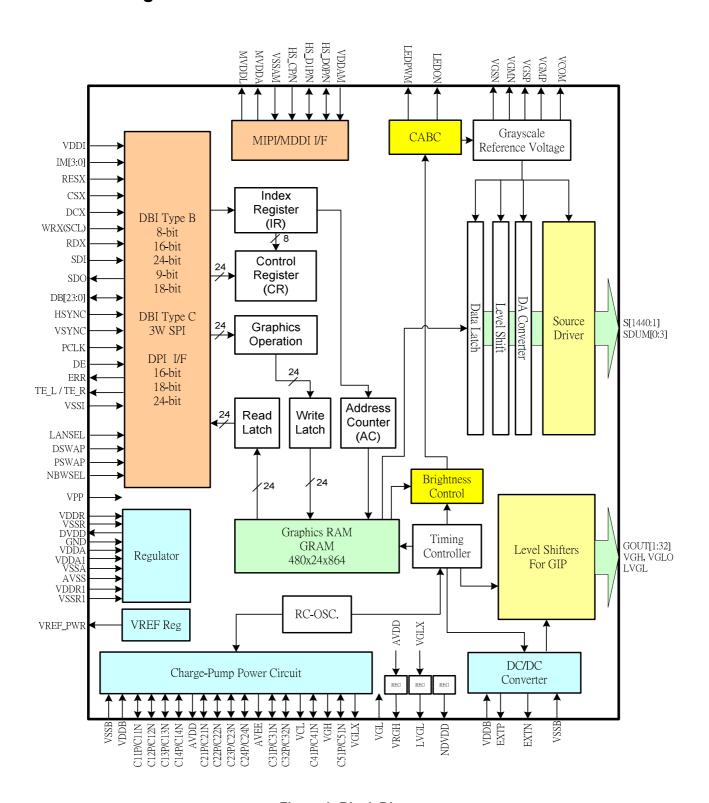


Figure 1: Block Diagram

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3.2. Block Function Description

3.2.1. System Interface

The interface operating mode (DBI, DPI or DSI) is selected by hardware pins IM [3:0], as shown in Table 1 below.

Table 1: System Operating Mode Note 1

IM3	IM2	IM1	IM0	Interface	IO Pin in Use
0	0	0	0	DBI Type B 8-bit bus interface	DB [7:0], WRX, RDX, CSX, DCX
0	0	0	1	DBI Type B 16-bit bus interface	DB [15:0], WRX, RDX, CSX, DCX
0	0	1	0	DBI Type B 24-bit bus interface	DB [23:0], WRX, RDX, CSX, DCX
1	1	0	0	DBI Type B 9-bit bus interface	DB [8:0], WRX, RDX, CSX, DCX
1	1	0	1	DBI Type B 18-bit bus interface	DB [17:0], WRX, RDX, CSX, DCX
Х	0	1	1	DPI with DBI Type C 3-line 9-bit	DB [23:0], SDI, SDO, SCL, CSX
0	1	0	1	MIPI DSI Interface	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN
0	1	1	0	MDDI Interface	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN

3.2.2. Parallel RGB Interface

The RGB interface is used as the external interface for displaying moving pictures. When the RGB interface is selected, display operations are synchronized with the externally supplied signals, VSYNC, HSYNC, and PCLK. In the RGB interface mode, data (DB23-0) are written in synchronization with these signals according to the polarity of the Enable Signal (DE). This is done in order to prevent flicker on the display while updating display data.

The RGB interface allows transferring data only when updating the frames of a moving picture by writing all display data to the internal RAM. This method is a contributing factor for the low power requirement of moving picture display.

The ILI9806 includes an IR (index register) which stores the index data of internal control register and GRAM. When DCX = L, the command is written into the driver IC via the DBI interface. When DCX = H, GRAM data via the R2Ch register is written through the data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading display data from the GRAM.

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Note 1 Set Number of colors using set pixel format: 3Ah.





3.2.3. Address Counter (AC)

The address counter (AC) assigns an address for writing pixel data to the GRAM, or for reading pixel data from the GRAM. Each time a pixel data is written into the GRAM, the X address or Y address of the AC is automatically increased by 1 (or decreased by 1), as determined by the register setting (MV, MX and MY bit). To simplify the address control of the GRAM access, the window address function allows writing data only to a window area of the GRAM specified by Column and Row address registers. After data is written to the GRAM, the AC will be increased or decreased within the setting window address range specified by the Column address register (start: SC, end: EC) and the Row address register (start: SP, end: EP). The window address function enables writing data only in the rectangular area set by users on the GRAM.

3.2.4. Graphic RAM (GRAM)

GRAM is the graphic RAM storing bit-pattern data of 1,244,160 bytes with 24 bits per pixel, enabling a maximum of 480(RGB) x 864 dots graphic display.

3.2.5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates the LCD drive voltage which corresponds to 256 grayscale level set in the Gamma correction register. The ILI9806 can display up to 16.7M colors at maximum.

3.2.6. Timing Generating

The timing generator is used to generate timing signals for operating internal circuits. The timing generator generates timing signals for internal circuits, such as the internal GRAM. Timing for display operations (such as RAM read operation) and timing for internal operations (such as RAM access by the MPU) are outputted separately so that they do not interfere with each other.

3.2.7. Oscillator

The ILI9806 incorporates with an RC oscillator circuit. Command settings are used to change the frame frequency.

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3.2.8. Source Driver Circuit

The LCD display driver circuit consists of a 480-output source driver (S1~S1440). The display pattern data is latched when 480RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.9. Panel Control Circuit

The panel control circuit outputs GOUT [1:32] signals at either the VGH or VGLO or AVDD level.

3.2.10. Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to the register setting.

3.2.11. MIPI DSI Controller Circuit

The MIPI DSI controller circuit consists of the D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer and analog transceiver. The D-PHY controls communication with the analog block, and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams, and the PPU controls transmitting packet distribution and merging. The internal data and command buffer is used for temporary storage of incoming commands and display data.

3.2.12. MDDI

The ILI9806 supports MDDI as a differential small amplitude serial interface for high-speed data transfer.

3.2.13. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

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3.3. Pin Descriptions

Table 2: Bus Interface Pins

Bus Interface Pins																				
Pin Name	I/O						escription	าร												
Timitamo	""	- Select the interfa	ace n	node				10												
		-																		
			IM3	IM2	IM1	IM0	Interface													
			0	0	0	0	DBI Type	B 8-bit												
			0	0	0	1	DBI Type	B 16-bit												
IM [3:0]	ı		0	0	1	0	DBI Type	B 24-bit												
1101 [0.0]	ļ '		1	1	0	0	DBI Type	B 9-bit												
			1	1	0	1	DBI Type	B 18-bit												
			Х	0	1	1	DPI with E	DBI Type C 3-line 9-bit												
			0	1	0	1	MIPI DSI													
			0	1	1	0	MDDI													
		- The external res	et inp	out																
RESX	I		ip wit	h a lo	w inp	ut. Be	sure to e	execute a power-on res	et after supplying											
		power A chip select sig	nal.																	
CSX	ı		Low: the chip is selected and accessible High: the chip is not selected and not accessible																	
		Fix to VDDI or VS						ible												
		- The DBI Type B interface (DCX): The signal for command or				command or														
DCX	ı	parameter select Low: Comman	parameter select.																	
Box	'	'	'	'	ı	'	'	'	ı	'	•	•	High: Paramet	ter						
		- Serves as a read						aina adaa												
RDX	I	Fix to VDDI or V						sing eage.												
MDV			syste	em (V	/RX):	Serve	es as a w	rite signal and writes da	ata at the rising											
WRX (SCL)	I	edge. - Serial interface (SCL): Seri	al clo	ck int	out													
, ,		Fix to VDDI or VS	SSI I	evel v	vhen	not ir	ı use.													
		- A 24-bit parallel	bi-dir		nal da erface		s for MPU	Data Pin in Use	1											
		_	DDI T			Mode			-											
		_		/pe B 8				DB [7:0]	_											
		<u> </u>		/pe B 1				DB [15:0]												
DB [23:0]	I/O	1	DBI Ty	pe B 2	4-bit			DB [23:0]	_											
		1	DBI Ty	/pe B 9	-bit			DB [8:0]												
]	DBI Ty	/pe B 1	8-bit			DB [17:0]												
		1	DPI wi	th DBI	Type (3-line	9-bit	DB [23:0], SDI, SDO]											
		Fix to VDDI or VS	SSI 14	י ופעב	vhen	not i:	1 1150													
SDI		Serial data input p																		
(SDA)	I/O																			
	l	SDI: Serial data input pin																		

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		SDA: Serial data input/output bidirectional pin																					
		Fix to VDDI or VSSI level when not in use.																					
	_	Serial o	lata outpu	ut pin use	ed for the	SPI Inte	erface.																
SDO	0	Leave	the pin o	pen whe	en not in	use.																	
		-Tearin	-Tearing effect output																				
TE_L/TE_R	0		E_L= TE_		n nat in																		
D0114			<i>the pin o</i> ock signa				ion																
PCLK	l	Fix to	VDDI or \	/SSI leve	el when i	not in us	se.																
VSYNC	ı						rface opei	ration															
1107/110			VDDI or Nonchronia				ice operat	ion															
HSYNC	I	Fix to	VDDI or \	/SSI leve	el when i	not in us	se.																
			enable si	•	RGB inter	face ope	eration																
DE	I		r: access n: access		İ																		
		_	VDDI or \			not in us	se.																
			SI differe																				
					ey shou	ld be co	nnected	to VSSAI	И														
HS_CP					trobe sig		NI (Cth.)	ara diffa	مسم امنا مسم	م مانده ا	sianala M	ماده المادة											
HS_CN	I	Short a	(SID+) a	ilu 113_U ile so tr	nat the		rentiai Sin sistance	ali Swilig : hecomes	signais. ivi less tha	ake the w	m The												
			short as possible so that the COG resistance becomes less than 10 ohm. specifications of the interface must be compliant with the MDDI specification.							11. 1110													
		If MDDI are not in use, they should be connected to VSSAM.																					
												SI differe											
HS_D0P	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	1/0				ey shou	ld be co	nnected	to VSSAI	И				
HS_D0N												1/0	1/0	1/0		lata signa		e Don (Doto \ o	ro difforo	otial amal	Lowing	ianala M
HS_D1P											HS_D0P (Data+) and HS_D0N (Data-) are differential small swing signal wiring as short as possible so that the COG resistance becomes less than												
HS_D1N							specifications of the interface must be compliant with the MDDI specifications						iiii. Tiic										
							onnected		•														
		- CRC and ECC error output pin for the MIPI interface, activated by S/W command. This																					
ERR	0	pin is output low when it is not activated. When this pin is activated, it is output high if CRC/ECC error is found. Leave the pin open when not in use.						output hi	gh if														
							anes in MI	PI/MDDI i	interface.														
LANCEL			r: 1 data I																				
LANSEL	I	_	n: 2 data																				
			VSSI leve			е.																	
			ential cloo PI interfac		y swap																		
					1 OI WIII	Tinteriac	,				Pins]									
			DSWAP	PSWAP			I	I	l	l													
					HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N													
			0	0	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N													
DSWAP	I			1	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P													
PSWAP			,	0	HS_CP	HS_CN	HS_D1P	HS_D1N	HS_D0P	HS_D0N													
			1	1	HS_CN	HS_CP	HS_D1N	HS_D1P	HS_D0N	HS_D0P													
					1		ı	I	ı	ı	1												

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		For MDDI interface									
			DSWAP	PSWAP			F	Pins			
			DSWAP	PSWAP	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N	
			0	0	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N	
			U	1	HS_CN	HS_CP	HS_D0N	HS_D0P	HS_D1N	HS_D1P	
		Fix to	VSSI leve	el when i	not in us	e.					
RGBBP	I		- Test Pin Fix to VSSI level.								
GPO [3:0]	0		- Test Pin Leave the pin open.								
EXB1T	ı	Lov Hig	- Input pin to select the external DC/DC circuit. Low: Using internal DC/DC for AVDD / AVEE High: Using external DC/DC for AVDD / AVEE Fix to VSSI level when not in use.								
NBWSEL	I	Lov Hig	- Input pin to select the gamma voltage level sequence of V0~V255. Low: V0 > V1 > > V254 > V255, normally white High: V255 > V254 > > V1 > V0, normally black Fix to VDDI level when not in use.								
LEDON	0		- Used for turning On/Off external LED backlight control. Leave the pin open when not in use.								
LEDPWM	0	- The PWM frequency output for LED driver control. Leave the pin open when not in use.									





Table 3: Driver Output Pins

Driver Output Pins						
Pin Name	I/O	Туре	Descriptions			
S [1:1440]	0	LCD	- Source output voltage signals applied to a LCD panel			
GOUT [1:32]	0	LCD	- Gate control signals and the swing voltage level is VGH to VGLO			
SDUM [0:3]	0	LCD	- Dummy Source Leave the pin open when not in use.			
VGH	0	LCD	- High voltage level for gate control signals and gate circuit of panel VGH is already connected to VGH in IC.			
VGLO (VGLO_L / VGLO_R)	0	LCD	- Low voltage level for gate control signals and gate circuit of panel			
LVGL (LVGL_L/ LVGL_R)	0	LCD	- Low voltage level for gate circuit of panel LVGL is already connected to VGL_REG in IC. (VGL_REG is the output voltage generated from VGL. LDO output used for panel voltage.) - Connect a capacitor for stabilization			
VGMP (VGMP_PAD)	0	LCD	- Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.			
VGSP (VGSP_PAD)	0	LCD	- Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.			
VGMN (VGMN_PAD)	0	LCD	- Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.			
VGSN (VGSN_PAD)	0	LCD	- Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.			

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Table 4: Charge Pump Relative Pins

Charge Pump Relative Pins								
Pin Name	I/O	Туре	Descriptions					
AVDD	0	Stabilizing capacitor	Output voltage from step-up circuit 1, generated from VDDB. Connect to a stabilizing capacitor between AVDD and VSSB.					
AVEE	0	Stabilizing capacitor	Output voltage from step-up circuit 2, generated from VDDB. Connect to a stabilizing capacitor between AVEE and VSSB.					
VCL	0	Stabilizing capacitor	Output voltage from step-up circuit 3, generated from VDDB. Connect to a stabilizing capacitor between VCL and VSSB.					
VGH	0	Stabilizing capacitor	Output voltage from step-up circuit 4, generated from VDDB. Connect to a stabilizing capacitor between VGH and VSSB.					
VGL	0	Stabilizing capacitor	- Substrate voltage for driver IC - Output voltage from step-up circuit 5, generated from VDDB Connect to a stabilizing capacitor between VGL and VSSB.					
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating AVDD level Capacitor connection pins for the step-up circuit 1.					
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating AVEE level Capacitor connection pins for the step-up circuit 2.					
C31P, C31N C32P, C32N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VCL level Capacitor connection pins for the step-up circuit 3.					
C41P, C41N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VGH level Capacitor connection pins for the step-up circuit 4.					
C51P, C51N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VGL level Capacitor connection pins for the step-up circuit 5.					

Table 5: DC/DC Converter Pins

DC/DC Converter Pins								
Pin Name	I/O	Туре	Descriptions					
EXTN (CTRL_A)	0	Positive NMOS	-PWM control output for gate of NMOS in positive DC/DC converter (for AVDD) -CTRL_A: Control signal for an external charge pump IC (ex: ILI4002)					
EXTP (CTRL_B)	0	Negative PMOS	-PWM control output for gate of PMOS in negative DC/DC converter (for AVEE) -CTRL_B: Control signal for an external charge pump IC (ex: ILI4002)					

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Table 6: Power Pins

Power Pins											
Pin Name	I/O	Туре	Descriptions								
VRGH (VRGH_L / VRGH_R)	0	LDO Stabilizing Capacitor	- Output voltage generated from AVDD Connect a capacitor for stabilization. Leave the pin open when not in use.								
VREF_PWR	0	LDO Stabilizing Capacitor	- Reference voltage for regulator output Connect a capacitor for stabilization.								
VDDA	Р	Analog	 Power supply for analog system. VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V. 								
VDDA1	Р	Analog	 Power supply for analog system. VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V. 								
VDDR	Р	Regulator	 Power supply for regulator system. VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V. 								
VDDR1	Р	Regulator	 Power supply for regulator system. VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V. 								
VDDB	Р	DC/DC	 Power supply for DC/DC converter. VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V. 								
VDDI	Р	I/O	- Power supply for I/O block. Exclude MIPI/MDDI interface.								
DVDD	0	Stabilizing Capacitor	- Internal logic voltage output - Connect a capacitor for stabilization.								
NDVDD	0	Stabilizing Capacitor	Negative internal logic voltage output Connect a capacitor for stabilization.								
VDDAM	Р	MIPI/MDDI	- Power supply for MIPI/MDDI analog system.								
MVDDA	0	MIPI Stabilizing Capacitor	- Regulator output for internal MIPI / MDDI analog system (1.5V typical) - Connect a capacitor for stabilization.								
MVDDL	0	MIPI Stabilizing Capacitor	 Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization. 								
VSSA	Р	Analog	- System ground for analog circuit.								
VSSR	Р	Regulator	- System ground for regulator circuit.								
VSSR1	Р	Regulator	- System ground for regulator circuit.								
VSSB	Р	DC/DC	- System ground for DC/DC convertor.								
VSSI	Р	I/O	- System ground for interface system.								
GND	Р	Digital	- System ground for internal digital system.								
AVSS	Р	Source OP	- System ground for source OP system.								
VSSAM	Р	MIPI/MDDI	- System ground for MIPI/MDDI system.								
VPP	I	OTP	- OTP programming power.								
VCOM	0	LDO	- Output voltage generated from VCI / VCL								

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(VCOM_L/	Stabilizing	- Connect a capacitor for stabilization.
VCOM_R)	Capacitor	VCOM=VCOM_L=VCOM_R

Table 7: Test Pins

			Test Pins
Pin Name	I/O	Туре	Descriptions
PADA [1:4] PADB [1:4]	I/O		- Dummy Pin.
CONTACT1A CONTACT1B	I/O		- Test pin, for test bonding quality, IC internal will connect CONTACT1A with CONTACT1B.
KBBC	0		- Test pin, not accessible to user. MUST be left open.
VSEL	-		- Dummy pin.
TEST [0:3]	I		- Test pin, not accessible to user. MUST be left open. (Internal weakly pull low)
OSC_TEST	I		- Test pin, not accessible to user, MUST be left open (Internal weakly pull low)
VSSIDUM [0:106]	0		 These are dummy pins with VSSI potential (not have any function inside). Signal traces cannot pass through on glass under these pads.
DUMMY	-		- Dummy pads. Leave the pin open.

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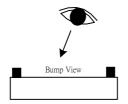


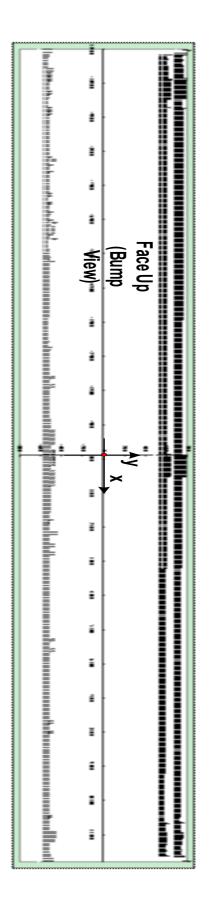


3.4. Pin Assignment

Chip Size: 24360um X 1530um Chip Thickness: 280um (typ.) Pad Location: Pad Center Coordinate Origin: Chip center

Au Bump Size : 1. 14um X 115um 2. 40um X 120um

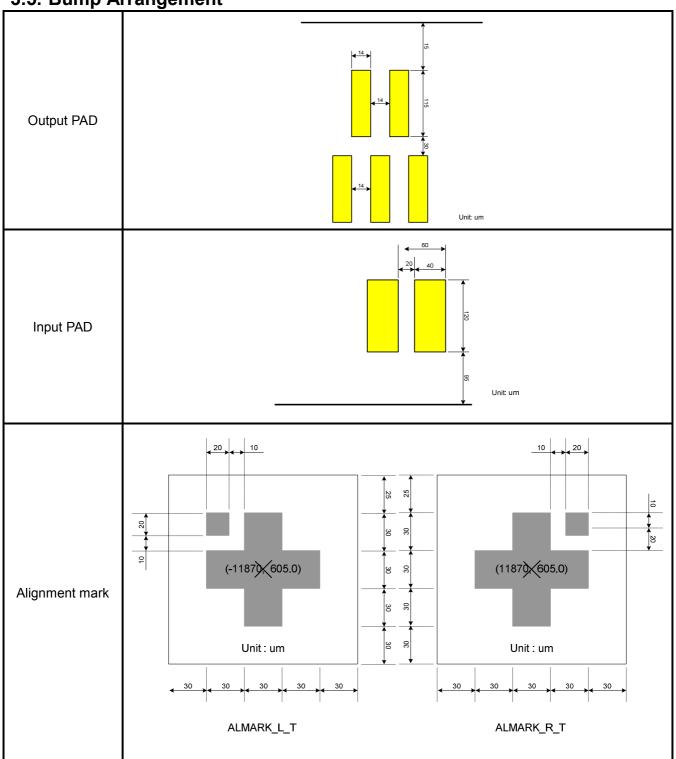




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3.5. Bump Arrangement



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3.6. Pad Coordination

No. Septiment Monte Mo	<u>J.C</u>	o. Pau C	, , , , , , , , , , , , , , , , , , , 	uma									_			
	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	Ν	o. Text Name	X-axis	Y-axis
PADAL	1	VSSIDUM0	-11880	-620	61	VGMP_PAD	-8250	-620	121	DB[20]	-4650	-620	18	31 VSSAM	-1050	-620
	2	VSSIDUM1	-11790	-620	62	GND	-8190	-620	122	DB[19]	-4590	-620	18	32 VSSAM	-990	-620
	3	PADA1	-11730	-620	63	GND	-8130	-620	123	DB[18]	-4530	-620	18	33 VSSAM	-930	-620
	4	PADB1	-11670	-620	64	GND	-8070	-620	124	DB[17]	-4470	-620	18	34 VSSAM	-870	-620
	5	VCOM_L	-11610	-620	65	DVDD	-8010	-620	125	DB[16]	-4410	-620	18	S VSSAM	-810	-620
	6	VCOM L	-11550	-620	66	DVDD	-7950	-620	126	DB[15]	-4350	-620	18	6 HS_D1P	-750	-620
	7	VCOM L	-11490	-620	67	DVDD	-7890	-620	127		-4290	-620	18	7 HS D1P	-690	-620
		_			68	VDDB		-620	128		-4230	-620	18		-630	-620
10 CONTACTIA 1150 420 70 VIDBS 771 VIDBS							-	_					-	_		
14 CONTACTIB 11290 620 72 VPT 1130 620 73 VPT 1130 620													-			
12 VPP	-												_		_	<u> </u>
14 VPP		1						_					_	_	_	
14 VPP													_		_	<u> </u>
15 VPP	-	1					-			1			-		_	-
16 WPP		1				-	-	_					_			
17	_												_		_	<u> </u>
18							-	_	136	DB[5]		-620	19			
19	17	VGL	-10890	-620			-7290	-620	137		-3690	-620	19	7 HS_CP	-90	-620
100 SQLO_L 10710 620 80 VDDL -7;101 4:20 4:20 14:10 DRI[1] -3;510 -5;20 -2;00 18;CN 990 -6;20 -2;00 14:10 DRI[1] -3;510 -5;20 -2;00 -2;00 -3	18	VGL	-10830	-620	78	AVSS	-7230	-620	138	DB[3]	-3630	-620	19	98 HS_CP	-30	-620
1	19	VGLO_L	-10770	-620	79	AVSS	-7170	-620	139	DB[2]	-3570	-620	19	9 HS_CP	30	-620
22 VKB_L	20	VGLO_L	-10710	-620	80	VDDI	-7110	-620	140	DB[1]	-3510	-620	20	00 HS_CN	90	-620
22 VGH_L -10590 -620 -82 -88 VSWAP -6930 -620 -84 -88	21	LVGL_L	-10650	-620	81	LANSEL	-7050	-620	141	DB[0]	-3450	-620	20	1 HS_CN	150	-620
24	22	LVGL L	-10590	-620	82	DSWAP	-6990	-620	142	DE	-3390	-620	20	2 HS_CN	210	-620
24	23	VRGH L	-10530	-620	83	PSWAP	-6930	-620	143	PCLK	-3330	-620	20	3 HS CN	270	-620
25 VCL	24			-620	84		-6870	-620	144	HS	-3270	-620	20			-620
26		_			85								_		_	<u> </u>
27 VCL	-					+	-		-				-		_	-
28 VCL		1				+		_					-	_		
29 VREF_PWR -10170 -620 8 DUMMY -6510 -620 -620 19 DENMY -6510 -620 -620 11 VDDI -650 -620													_		_	<u> </u>
30						+	-	_					-			
31 VREF_PWR -10050 -620 91 VDD1 -6450 -620 151 VDD1 -2850 -620 211 HS_DON 870 -620 152 VDD1 -2790 -620 213 HS_DON 810 -620 153 VSSA -9870 -620 94 M3 -6270 -620 154 VSSI -2760 -620 214 VSSAM 990 -620 620 635 VSSA -9810 -620 95 M2 -6210 -620 155 VSSI -2610 -620 215 VSSAM 990 -620 620 636 VSSA -9875 -620 96 M1 -6150 -620 155 VSSI -2610 -620 215 VSSAM 990 -620 620 638 VDDA -9890 -620 98 GPO3 -620 156 AVDD -2550 -620 216 MVDDL 1010 -620 620		_						_					_	_		
32 VREF_PWR -9990 -620 73 VSSA -9930 -620 74 M3 -620 620 75 M2 621	-	_											_		_	<u> </u>
33 VSSA -9930 -620 93 DUMMY -6330 -620 154 VSSI -2730 -620 214 VSSAM 930 -620 620 635 VSSA -9970 -620 96 IM1 -6150 -620 155 VSSI -2610 -620 215 VSSAM 930 -620 620 638 VDDA -9690 -620 98 GPO2 -5970 -620 156 AVDD -2430 -620 216 MVDDL 1100 -620 620 640 VDDA -9510 -620 100 GPO1 -5910 -620 159 AVDD -2430 -620 218 MVDDL 1170 -620 620 640 VDDA -9510 -620 100 GPO1 -5910 -620 159 AVDD -2430 -620 219 MVDDA 1230 -620 129 MVDDA 1230 -620 123 MVDDA 1230 -620 1230 MVDDA 1230 -620	-	_			<u> </u>	+	-						-		_	+
34 VSSA	32							_			1		_	_		
95 M2	33		-9930	-620	93		-6330	-620	153			-620	2.	.3 HS_D0N	870	-620
Section Sect	34	VSSA	-9870	-620	94	IM3	-6270	-620	154		-2670	-620	2.	4 VSSAM	930	-620
37 VDDA	35	VSSA	-9810	-620	95	IM2	-6210	-620	155	VSSI	-2610	-620	2.	.5 VSSAM	990	-620
38	36	VSSA	-9750	-620	96	IM1	-6150	-620	156	AVDD	-2550	-620	2	.6 MVDDL	1050	-620
39 VDDA	37	VDDA	-9690	-620	97	IM0	-6090	-620	157	AVDD	-2490	-620	2	7 MVDDL	1110	-620
10	38	VDDA	-9630	-620	98	GPO3	-6030	-620	158	AVDD	-2430	-620	2.	8 MVDDL	1170	-620
41 VDDR -9450 -620 101 GPO0 -5850 -620 161 AVSS -2250 -620 221 MVDDA 1350 -620 42 VDDR -9390 -620 102 EXBIT -5790 -620 162 AVSS -2190 -620 222 VDDAM 1410 -620 44 VDDR -9270 -620 104 VSEL -5670 -620 164 AVEE -2070 -620 222 VDDAM 1410 -620 46 VSSR -9210 -620 105 SDO -5610 -620 165 AVEE -2010 -620 222 VDDAM 1530 -620 48 VSSR -9900 -620 106 SDI -5550 -620 166 AVEE -1950 -620 225 VDDAM 1590 -620 49 TEST[0] -8970 -620 108 WRX -5430 -620 168 AVEE -1830 -620 227 VDDAM 1590 -620 51 TEST[2] -8850 -620 111 RESX -5370 -620 169 VDDAI -1770 -620	39	VDDA	-9570	-620	99	GPO2	-5970	-620	159	AVDD	-2370	-620	2	9 MVDDA	1230	-620
42 VDDR -9390 -620 43 VDDR -9330 -620 44 VDDR -9370 -620 44 VDDR -9270 -620 45 VSSR -9210 -620 46 VSSR -9210 -620 105 SDO -5610 -620 106 SDI -5550 -620 166 AVEE -2010 -620 222 VDDAM 1470 -620 46 VSSR -9150 -620 106 SDI -5550 -620 107 DCX -5490 -620 48 VSSR -9030 -620 108 WRX -5430 -620 109 RDX -5370 -620 110 CSX -5310 -620 120 TEST[1] -8910 -620 111 RESX -5250 -620 121 VSSI -5190 -620 122 TEST[3] -870 -620 123 VDDR -8730 -620 124 VDDAI -1170 -62	40	VDDA	-9510	-620	100	GPO1	-5910	-620	160	AVSS	-2310	-620	22	0 MVDDA	1290	-620
42 VDDR -9390 -620 43 VDDR -9330 -620 44 VDDR -9370 -620 44 VDDR -9270 -620 45 VSSR -9210 -620 46 VSSR -9210 -620 105 SDO -5610 -620 106 SDI -5550 -620 166 AVEE -2010 -620 222 VDDAM 1470 -620 46 VSSR -9150 -620 106 SDI -5550 -620 107 DCX -5490 -620 48 VSSR -9030 -620 108 WRX -5430 -620 109 RDX -5370 -620 110 CSX -5310 -620 120 TEST[1] -8910 -620 111 RESX -5250 -620 121 VSSI -5190 -620 122 TEST[3] -870 -620 123 VDDR -8730 -620 124 VDDAI -1170 -62	-					+	-		-				-		_	-
43 VDDR	-						-	_					_		_	+
44 VDDR -9270 -620 45 VSSR -9210 -620 46 VSSR -9150 -620 47 VSSR -9090 -620 48 VSSR -9090 -620 48 VSSR -9030 -620 49 TEST[0] -8970 -620 10 REST[1] -8910 -620 110 CSX -5310 -620 51 TEST[2] -8850 -620 111 RESX -5550 -620 112 VSSI -510 -620 113 VSSI -510 -620 114 VSSI -550 -620 115 VDDI -4950 -620 116 SNR -510 -620 110 CSX -5310 -620 111 RESX -5550 -620 112 VSSI -510 -620 113 VSSI -510 -620 114 VSSI -500 -620 115 VDDI -500 -620 116 GND -1350 -620 </td <td>-</td> <td></td> <td></td> <td></td> <td><u> </u></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>-</td> <td>-</td> <td>-</td> <td> </td>	-				<u> </u>								-	-	-	
45 VSSR		1				-	-		-				-	-	-	+
46 VSSR -9150 -620 106 SDI -5550 -620 166 AVEE -1950 -620 226 VDDAM 1650 -620 48 VSSR -9030 -620 108 WRX -5490 -620 168 AVEE -1890 -620 226 VDDAM 1650 -620 49 TEST[0] -8970 -620 110 CSX -5370 -620 169 VDDA1 -1770 -620 228 VDDR1 1770 -620 51 TEST[2] -8850 -620 111 RESX -5250 -620 170 VDDA1 -1710 -620 230 OSC_TEST 1890 -620 52 TEST[3] -8790 -620 113 VSSI -5130 -620 172 VDDA1 -1550 -620 231 TE_R 1950 -620 53 VDDR -8730 -620 114 VSSI -5130 -620	-						1						-			
16 17 17 17 18 18 18 18 18	-				<u> </u>								_			
48 VSSR -9030 -620 49 TEST[0] -8970 -620 50 TEST[1] -8910 -620 51 TEST[2] -8850 -620 52 TEST[3] -8790 -620 53 VDDR -8730 -620 54 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 116 VDDI -4950 -620 117 VDDI -4890 -620 118 DB[23] -4830 -620 119 DB[21] -4710 -620 180 VGMN_PAD -8310 -620 109 RDX -5370 -620 110 CSX -5310 -620 111 RESX -5250 -620 112 VSSI -5190 -620 113 VSSI -5190 -620 173 GND -1530 -620 174 GND -1470 -620 175 GND -1410 -620 176 GND -1350 -620 177 DVDD -1290 -620 <tr< td=""><td></td><td></td><td></td><td></td><td></td><td>+</td><td>-</td><td></td><td></td><td>1</td><td></td><td></td><td>-</td><td></td><td>_</td><td>+</td></tr<>						+	-			1			-		_	+
49 TEST[0] -8970 -620 50 TEST[1] -8910 -620 51 TEST[2] -8850 -620 52 TEST[3] -8790 -620 53 VDDR -8730 -620 54 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 57 VGSN_PAD -8490 -620 58 VGSP_PAD -8430 -620 118 DB[23] -4830 -620 59 VGMN_PAD -8370 -620 119 DB[21] -4710 -620 120 DB[21] -4710 -620 169 VDDA1 -1710 -620 170 VDDA1 -1710 -620 171 VDDA1 -1650 -620 172 VDDA1 -1590 -620 173 GND -1530 -620 174 GND -1470 -620 175 GND -1410 -620 176 GND -1350 -620 177 DVDD -1290 -620 178 DVDD -1290 -620	-					-	1				1		-			<u> </u>
50 TEST[1] -8910 -620 51 TEST[2] -8850 -620 52 TEST[3] -8790 -620 53 VDDR -8730 -620 54 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 116 VDDI -4950 -620 117 VDDD -1350 -620 172 VDDA1 -1590 -620 173 GND -1530 -620 174 GND -1470 -620 175 GND -1470 -620 175 GND -1410 -620 175 GND -1410 -620 176 GND -1350 -620 176 GND -1350 -620 177 DVDD -1290 -620 237 NDVDD 236 NDVDD	-				<u> </u>	+	-						-	-		
51 TEST[2] -8850 -620 52 TEST[3] -8790 -620 53 VDDR -8730 -620 54 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 116 VDDI -4950 -620 117 VDD -1470 -620 173 GND -1470 -620 174 GND -1470 -620 175 GND -1410 -620 176 GND -1410 -620 177 DVDD -120 -620 178 DVDD -1350 -620 179 DVDD -1290 -620 231 TE_R 1950 -620 232 VSSR1 2010 -620 233 VSSR1 2010 -620 175 GND -1410 -620 236 NDVDD 235 VSSR1 2100 236 NDVDD -237 NDVDD 238 VRGH 237 NDVDD 238 VRGH 237 NDVDD 238 VRGH					-	+	-						-		_	+
52 TEST[3] -8790 -620 53 VDDR -8730 -620 54 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 57 VGSN_PAD -8490 -620 112 VDDI -4890 -620 116 VDDI -4890 -620 117 VDDI -4890 -620 118 DB[23] -4830 -620 119 DB[21] -4710 -620 180 DVDD -1110 -620 180 DVDD -1110 -620 232 VSSR1 2010 -620 233 VSSR1 2070 -620 175 GND -1410 -620 235 VSSR1 2130 -620 236 NDVDD -235 VSSR1 2100 -620 237 NDVDD 2236 NDVDD -236 NDVDD -237 NDVDD -237 NDVDD -238 VRGH 237 NDVDD -238 VRGH 237 NDVDD -238 VRGH 239 VRGH -2490 -620 -620 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td>1</td><td></td><td></td><td></td><td>1</td><td></td><td>_</td><td>_</td><td></td><td></td></t<>							1				1		_	_		
53 VDDR -8730 -620 54 DUMMY -8670 -620 55 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 116 VDDI -4950 -620 117 VDDI -4890 -620 118 DB[23] -4830 -620 119 DB[21] -4710 -620 180 DVDD -110 -620 173 GND -1410 -620 175 GND -1410 -620 176 GND -1350 -620 177 DVDD -1290 -620 237 NDVDD 236 NDVDD 237 237 NDVDD 238 VRGH 237 238 VRGH 237 -620 238 VRGH 239 VRGH 239 VRGH 2430													_			
54 DUMMY -8670 -620 55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 57 VGSN_PAD -8490 -620 116 VDDI -4950 -620 117 VDDI -4950 -620 118 DB[23] -4830 -620 119 DB[23] -4770 -620 180 DVDD -1170 -620 180 DVDD -1170 -620 180 DVDD -1110 -620 234 VSSR1 2130 -620 175 GND -1410 -620 177 DVDD -1290 -620 237 NDVDD 2310 -620 238 VRGH 237 NDVDD 239 VRGH 239 VRGH 240 -620 180 DVDD -1110 -620 -620 2490 -620 <td>52</td> <td></td> <td>-8790</td> <td>-620</td> <td>112</td> <td>+</td> <td>-</td> <td>-620</td> <td></td> <td></td> <td></td> <td>-620</td> <td>-</td> <td></td> <td>2010</td> <td>-620</td>	52		-8790	-620	112	+	-	-620				-620	-		2010	-620
55 DUMMY -8610 -620 56 VGSN_PAD -8550 -620 57 VGSN_PAD -8490 -620 116 VDDI -4950 -620 117 VDDI -4950 -620 118 DB[23] -4830 -620 119 DB[23] -4770 -620 120 DB[21] -4710 -620 180 DVDD -110 -620 180 DVDD -1110 -620 235 VSSR1 2190 -620 236 NDVDD 236 NDVDD 2310 -620 237 NDVDD 238 VRGH 2370 -620 239 VRGH 239 VRGH 2430 -620 240 EXTP 2490 -620	53	VDDR	-8730	-620	113		-5130	-620	173	GND	-1530	-620	23		2070	-620
56 VGSN_PAD -8550 -620 57 VGSN_PAD -8490 -620 58 VGSP_PAD -8430 -620 59 VGMN_PAD -8370 -620 110 DB[21] -4710 -620 170 GND -1350 -620 177 DVDD -1290 -620 178 DVDD -1170 -620 179 DVDD -1170 -620 230 NDVDD 237 NDVDD 230 230 VRGH 2370 -620 230 VRGH 239 VRGH 2470 -620 180 DVDD -1110 -620 -620 240 EXTP 2490 -620	54	DUMMY	-8670	-620	114	VSSI	-5070	-620	174	GND	-1470	-620	23	VSSR1	2130	-620
57 VGSN_PAD -8490 -620 117 VDDI -4890 -620 177 DVDD -1290 -620 237 NDVDD 2310 -620 59 VGMN_PAD -8370 -620 119 DB[21] -4710 -620 180 DVDD -110 -620 237 NDVDD 2310 -620 179 DVDD -1170 -620 239 VRGH 2430 -620 180 DVDD -1110 -620 240 EXTP 2490 -620	55	DUMMY	-8610	-620	115	VDDI	-5010	-620	175	GND	-1410	-620	23	VSSR1	2190	-620
58 VGSP_PAD -8430 -620 118 DB[23] -4830 -620 178 DVDD -1230 -620 238 VRGH 2370 -620 59 VGMN_PAD -8310 -620 119 DB[21] -4710 -620 180 DVDD -1170 -620 238 VRGH 2370 -620 180 DVDD -1110 -620 240 EXTP 2490 -620	56	VGSN_PAD	-8550	-620	116	VDDI	-4950	-620	176	GND	-1350	-620	23	MDVDD	2250	-620
58 VGSP_PAD -8430 -620 118 DB[23] -4830 -620 178 DVDD -1230 -620 238 VRGH 2370 -620 59 VGMN_PAD -8310 -620 119 DB[21] -4710 -620 180 DVDD -1170 -620 238 VRGH 2370 -620 180 DVDD -1110 -620 240 EXTP 2490 -620	57	VGSN_PAD	-8490	-620	117	VDDI	-4890	-620	177	DVDD	-1290	-620	23	7 NDVDD	2310	-620
59 VGMN_PAD -8370 -620 119 DB[22] -4770 -620 179 DVDD -1170 -620 239 VRGH 2430 -620 60 VGMN_PAD -8310 -620 120 DB[21] -4710 -620 180 DVDD -1110 -620 239 VRGH 2430 -620	58			-620	118	DB[23]	-4830	-620	178	DVDD	-1230	-620	23	8 VRGH	2370	-620
60 VGMN_PAD -8310 -620 120 DB[21] -4710 -620 180 DVDD -1110 -620 240 EXTP 2490 -620							1				1		-		_	<u> </u>
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No. 241	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
	EXTP	2550	-620	301	C21P	6150	-620	361	C41P	9750	-620	421	VRGH_R	11480	477.5
242	DUMMY	2610	-620	302	C21N	6210	-620	362	C41N	9810	-620	422	VRGH_R	11466	622.5
-	DUMMY	2670	-620	303	C21N	6270	-620	363	C41N	9870	-620	423	VGLO_R	11452	477.5
	EXTN	2730	-620	304	C21N	6330	-620	364	VGH	9930	-620	424	VGLO_R	11438	622.5
	EXTN	2790	-620	305	C22P	6390	-620	365	VGH	9990	-620	425	VGLO_R	11424	477.5
246	DUMMY	2850	-620	306	C22P	6450	-620	366	VGH	10050	-620	426	GOUT3	11410	622.5
247	DUMMY	2910	-620	307	C22P	6510	-620	367	VGH	10110	-620	427	GOUT3	11396	477.5
248	VDDB	2970	-620	308	C22N	6570	-620	368	VRGH_R	10170	-620	428	GOUT4	11382	622.5
249	VDDB	3030	-620	309	C22N	6630	-620	369	VRGH_R	10230	-620	429	GOUT4	11368	477.5
-	VDDB	3090	-620	310	C22N	6690	-620	370	C51P	10290	-620	430	GOUT5	11354	622.5
-	VDDB	3150	-620	311	C23P	6750	-620	371	C51P	10350	-620	431	GOUT5	11340	477.5
252	VDDB	3210	-620	312	C23P	6810	-620	372	C51N	10410	-620	432	GOUT6	11326	622.5
-	VDDB	3270	-620	313	C23P	6870	-620	373	C51N	10470	-620	433	GOUT6	11312	477.5
-	VSSB	3330	-620	314	C23N	6930	-620	374	LVGL_R	10530	-620	434	GOUT7	11298	622.5
	VSSB	3390	-620	315	C23N	6990	-620	375	LVGL_R	10590	-620	435	GOUT7	11284	477.5
	VSSB	3450	-620	316	C23N	7050	-620	376	VGLO_R	10650	-620	436	GOUT8	11270	622.5
-	VSSB	3510	-620	317	C24P	7110	-620	377	VGLO_R	10710	-620	437	GOUT8	11256	477.5
	VSSB	3570	-620	318	C24P	7170	-620	378	VGL	10770	-620	438	GOUT9	11242	622.5
-	VSSB C11D	3630	-620	319	C24P	7230	-620	379	VGL	10830	-620	439	GOUT9	11228	477.5
	C11P C11P	3690 3750	-620 -620	320 321	C24N C24N	7290 7350	-620 -620	380	VGL VGL	10890 10950	-620 -620	440	GOUT10 GOUT10	11214 11200	622.5 477.5
	C11P C11P	3750	-620	321	C24N C24N	7350	-620	381	DUMMY	11010	-620	441	GOUT10 GOUT11	11200	622.5
	C11N	3870	-620	323	VDDB	7410	-620	382	DUMMY	11010	-620	442	GOUT11 GOUT11	11172	477.5
-	C11N	3930	-620	323	VDDB	7530	-620	384	DUMMY	11130	-620	444	GOUT11 GOUT12	11172	622.5
	C11N	3990	-620	325	VDDB	7590	-620	385	DUMMY	11190	-620	445	GOUT12 GOUT12	11144	477.5
	C12P	4050	-620	326	VDDB	7650	-620	386	DUMMY	11250	-620	446	GOUT12 GOUT13	11130	622.5
-	C12P	4110	-620	327	VDDB	7710	-620	387	DUMMY	11310	-620	447	GOUT13	11116	477.5
	C12P	4170	-620	328	VCL	7770	-620	388	VCOM_R	11370	-620	448	GOUT14	11102	622.5
-	C12N	4230	-620	329	VCL	7830	-620	389	VCOM_R	11430	-620	449	GOUT14	11088	477.5
	C12N	4290	-620	330	VCL	7890	-620	390	VCOM_R	11490	-620	450	GOUT15	11074	622.5
271	C12N	4350	-620	331	VCL	7950	-620	391	VCOM_R	11550	-620	451	GOUT15	11060	477.5
272	C13N	4410	-620	332	VCL	8010	-620	392	VCOM_R	11610	-620	452	GOUT16	11046	622.5
273	C13N	4470	-620	333	VCL	8070	-620	393	PADA2	11670	-620	453	GOUT16	11032	477.5
274	C13N	4530	-620	334	VCL	8130	-620	394	PADB2	11730	-620	454	VGH	11018	622.5
275	C13P	4590	-620	335	AVSS	8190	-620	395	VSSIDUM2	11790	-620	455	VGH	11004	477.5
276	C13P	4650	-620	336	AVSS	8250	-620	396	VSSIDUM3	11880	-620	456	VGH	10990	622.5
-	C13P	4710	-620	337	AVSS	8310	-620	397	DUMMY	12054	622.5	457	VGH	10976	477.5
	C14P	4770	-620	338	VSSB	8370	-620	398	DUMMY	12040	477.5	458	VGH	10962	622.5
	C14P	4830	-620	-	VSSB	8430	-620	-	DUMMY	12026	622.5		VGH	10948	477.5
-	C14P	4890	-620	340	VSSB	8490	-620	400	DUMMY	12012	477.5	460	VGH	10934	622.5
	C14N	4950	-620	341	VSSB	8550	-620	401	DUMMY	11998	622.5	461	VGH	10920	477.5
	C14N	5010	-620	-	C31P	8610	-620	402	VSSIDUM4	11760	622.5		VGLO_R	10906	622.5
	C14N	5070	-620	343	C31P	8670	-620	403	VSSIDUM5	11732	477.5	463	VGLO_R	10892	477.5
	AVDD AVDD	5130	-620 620	344	C31P	8730	-620 620	404	VSSIDUM6	11718	622.5	464	VGLO_R VGLO_R	10878	622.5 477.5
-	AVDD	5190 5250	-620 -620	345 346	C31N	8790 8850	-620 -620	405	PADA3 PADB3	11704	477.5 622.5	465	VGLO_R VGLO_R	10864 10850	
	AVDD	5250	-620	346	C31N C31N	8850	-620	406	VGH	11690 11676	622.5 477.5	466	VGLO_R VGLO_R	10830	622.5 477.5
	AVSS	5370	-620	348	C31N	8910 8970	-620	407	VGH	11662	622.5		VGLO_R VGLO_R	10830	622.5
	AVSS	5430	-620	349	C32N	9030	-620	409	VGH	11648	477.5	469	VGLO_R VGLO_R	10822	477.5
-	AVSS	5490	-620	350	C32N	9090	-620	410	VGLO R	11634	622.5	470	VGLO_R VGLO_R	10794	622.5
	AVSS	5550	-620	351	C32P	9150	-620	411	VGLO_R	11620	477.5	471	VSSIDUM7	10780	477.5
	AVSS	5610	-620	352	C32P	9210	-620	412	VGLO_R	11606	622.5	472	VSSIDUM8	10766	622.5
	AVEE	5670	-620	353	C32P	9270	-620	413	GOUT1	11592	477.5	473	SDUM0	10752	477.5
	AVEE	5730	-620	-	DVDD	9330	-620	414	GOUT1	11578	622.5	474	SDUM1	10738	622.5
	AVEE	5790	-620	-	DVDD	9390	-620	415	GOUT2	11564	477.5	475	S1	10724	477.5
	AVEE	5850	-620	-	DVDD	9450	-620	416	GOUT2	11550	622.5		S2	10710	622.5
	AVEE	5910	-620	357	GND	9510	-620	417	LVGL_R	11536	477.5		S3	10696	477.5
	AVEE	5970	-620	358	GND	9570	-620	418	LVGL_R	11522	622.5	478	S4	10682	622.5
-	C21P	6030	-620	359	GND	9630	-620	419	LVGL_R	11508	477.5	479	S5	10668	477.5
	C21P	6090	-620	360	C41P	9690	-620	420	VRGH R	11494	622.5	480	S6	10654	622.5

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No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
481	S7	10640	477.5	541	S67	9800	477.5	601	S127	8960	477.5	661	S187	8120	477.5
482	S8	10626	622.5	542	S68	9786	622.5	602	S128	8946	622.5	662	S188	8106	622.5
483	S9	10612	477.5	543	S69	9772	477.5	603	S129	8932	477.5	663	S189	8092	477.5
484	S10	10598	622.5	544	S70	9758	622.5	604	S130	8918	622.5	664	S190	8078	622.5
485	S11	10584	477.5	545	S71	9744	477.5	605	S131	8904	477.5	665	S191	8064	477.5
486	S12	10570	622.5	546	S72	9730	622.5	606	S132	8890	622.5	666	S192	8050	622.5
487	S13	10556	477.5	547	S73	9716	477.5	607	S133	8876	477.5	667	S193	8036	477.5
488	S14	10542	622.5	548	S74	9702	622.5	608	S134	8862	622.5	668	S194	8022	622.5
489	S15	10528	477.5	549	S75	9688	477.5	609	S135	8848	477.5	669	S195	8008	477.5
490	S16	10514	622.5	550	S76	9674	622.5	610	S136	8834	622.5	670	S196	7994	622.5
491	S17	10500	477.5	551	S77	9660	477.5	611	S137	8820	477.5	671	S197	7980	477.5
492	S18	10486	622.5	552	S78	9646	622.5	612	S138	8806	622.5	672	S198	7966	622.5
493	S19	10472	477.5	553	S79	9632	477.5	613	S139	8792	477.5	673	S199	7952	477.5
494	S20	10458	622.5	554	S80	9618	622.5	614	S140	8778	622.5	674	S200	7938	622.5
495	S21	10444	477.5	555	S81	9604	477.5	615	S141	8764	477.5	675	S201	7924	477.5
496	S22	10430	622.5	556	S82	9590	622.5	616	S142	8750	622.5	676	S202	7910	622.5
497	S23	10416	477.5	557	S83	9576	477.5	617	S143	8736	477.5	677	S203	7896	477.5
498	S24	10402	622.5	558	S84	9562	622.5	618	S144	8722	622.5	678	S204	7882	622.5
499	S25 S26	10388	477.5 622.5	559	S85 S86	9548 9534	477.5 622.5	619	S145	8708 8694	477.5 622.5	679	S205 S206	7868 7854	477.5 622.5
500	S26 S27	10374	477.5	560 561	S87	9534	622.5 477.5	620 621	S146 S147	8680	477.5	680 681	S206 S207	7854 7840	477.5
501	S28	10346	622.5	562	S88	9520	622.5	622	S147 S148	8666	622.5	682	S207	7826	622.5
502	S29	10346	477.5	563	S89	9492	477.5	623	S146 S149	8652	477.5	683	S206 S209	7812	477.5
504	S30	10332	622.5	564	S90	9478	622.5	624	S150	8638	622.5	684	S210	7798	622.5
505	S31	10304	477.5	565	S91	9464	477.5	625	S151	8624	477.5	685	S211	7784	477.5
506	S32	10290	622.5	566	S92	9450	622.5	626	S152	8610	622.5	686	S212	7770	622.5
507	S33	10276	477.5	567	S93	9436	477.5	627	S153	8596	477.5	687	S213	7756	477.5
508	S34	10262	622.5	568	S94	9422	622.5	628	S154	8582	622.5	688	S214	7742	622.5
509	S35	10248	477.5	569	S95	9408	477.5	629	S155	8568	477.5	689	S215	7728	477.5
510	S36	10234	622.5	570	S96	9394	622.5	630	S156	8554	622.5	690	S216	7714	622.5
511	S37	10220	477.5	571	S97	9380	477.5	631	S157	8540	477.5	691	S217	7700	477.5
512	S38	10206	622.5	572	S98	9366	622.5	632	S158	8526	622.5	692	S218	7686	622.5
513	S39	10192	477.5	573	S99	9352	477.5	633	S159	8512	477.5	693	S219	7672	477.5
514	S40	10178	622.5	574	S100	9338	622.5	634	S160	8498	622.5	694	S220	7658	622.5
515	S41	10164	477.5	575	S101	9324	477.5	635	S161	8484	477.5	695	S221	7644	477.5
516	S42	10150	622.5	576	S102	9310	622.5	636	S162	8470	622.5	696	S222	7630	622.5
517	S43	10136	477.5	577	S103	9296	477.5	637	S163	8456	477.5	697	S223	7616	477.5
518	S44	10122	622.5	578	S104	9282	622.5	638	S164	8442	622.5	698	S224	7602	622.5
519	S45	10108	477.5	579	S105	9268	477.5	639	S165	8428	477.5	699	S225	7588	477.5
520	S46	10094	622.5	580	S106	9254	622.5	640	S166	8414	622.5	700	S226	7574	622.5
521	S47	10080	477.5	581	S107	9240	477.5	641	S167	8400	477.5	701	S227	7560	477.5
-	S48	10066	622.5	_	S108	9226	622.5	-	S168	8386	622.5	702	S228	7546	622.5
-	S49	10052	477.5	583	S109	9212	477.5	-	S169	8372	477.5	703	S229	7532	477.5
-	S50	10038	622.5	_	S110	9198	622.5	-	S170	8358	622.5	704	S230	7518	622.5
	S51	10024	477.5	_	S111	9184	477.5		S171	8344	477.5	705	S231	7504	477.5
-	S52	10010	622.5	586		9170	622.5	646	S172	8330	622.5	706	S232	7490	622.5
-	S53	9996	477.5	587	S113	9156	477.5	647	+	8316	477.5	707	S233	7476	477.5
-	S54	9982	622.5	588	S114	9142	622.5		S174	8302	622.5	708	S234	7462	622.5
-	S55	9968	477.5		S115	9128	477.5	649	S175	8288	477.5	709	S235	7448	477.5
	S56	9954	622.5		S116	9114	622.5	-	S176	8274	622.5	710	S236	7434	622.5
	S57	9940	477.5	_	S117	9100	477.5	651	S177	8260	477.5	711	S237	7420	477.5
-	S58	9926	622.5	592		9086	622.5	652	S178	8246	622.5		S238	7406	622.5
_	S59	9912	477.5	_	S119	9072	477.5		S179	8232	477.5		S239	7392	477.5
-	S60	9898	622.5		S120	9058	622.5	_	S180	8218	622.5		S240	7378	622.5
-	S61	9884	477.5	-	S121	9044	477.5		S181	8204	477.5		S241	7364	477.5
-	S62 S63	9870	622.5 477.5	596	S122 S123	9030 9016	622.5 477.5	656	S182 S183	8190 8176	622.5 477.5	716 717	S242 S243	7350	622.5 477.5
	S64	9856 9842	622.5	598	S123	9002	622.5	-	S184	8162	622.5	717	S243 S244	7336 7322	622.5
-	S65	9828	477.5	599	S124	8988	477.5		S185	8148	477.5	719	S244 S245	7308	477.5
540	S66	9814	622.5	600	S126	8974	622.5	660	S186	8134	622.5	720	S245	7294	622.5
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No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
721	S247	7280	477.5	781	S307	6440	477.5	841	S367	5600	477.5	901	S427	4760	477.5
722	S248	7266	622.5	782	S308	6426	622.5	842		5586	622.5	902	S428	4746	622.5
723	S249	7252	477.5	783	S309	6412	477.5	843	S369	5572	477.5	903	S429	4732	477.5
724	S250	7238	622.5	784	S310	6398	622.5	844	S370	5558	622.5	904	S430	4718	622.5
725	S251	7224	477.5	785	S311	6384	477.5	845	S371	5544	477.5	905	S431	4704	477.5
726	S252	7210	622.5	786	S312	6370	622.5	846	S372	5530	622.5	906	S432	4690	622.5
727	S253	7196	477.5	787	S313	6356	477.5	847	S373	5516	477.5	907	S433	4676	477.5
728	S254	7182	622.5	788	S314	6342	622.5	848		5502	622.5	908	S434	4662	622.5
729	S255	7168	477.5	789	S315	6328	477.5	849	S375	5488	477.5	909	S435	4648	477.5
730	S256	7154	622.5	790	S316	6314	622.5	850	+	5474	622.5	910	S436	4634	622.5
731	S257	7140	477.5	791	S317	6300	477.5	851	S377	5460	477.5	911	S437	4620	477.5
732	S258	7126	622.5	792	S318	6286	622.5	852		5446	622.5	912	S438	4606	622.5
733	S259	7112	477.5	793	S319	6272	477.5	853	+	5432	477.5	913	S439	4592	477.5
734	S260	7098	622.5	794	S320	6258	622.5	854		5418	622.5	914	S440	4578	622.5
735	S261	7084	477.5	795	S321	6244	477.5	855		5404	477.5	915	S441	4564	477.5
736	S262	7070	622.5	796	S322	6230	622.5	856	+	5390	622.5	916	S442	4550	622.5
737 738	S263 S264	7056 7042	477.5 622.5	797 798	S323 S324	6216 6202	477.5 622.5	857 858	S383 S384	5376 5362	477.5 622.5	917	S443 S444	4536 4522	477.5 622.5
739	S265	7042	477.5	799	S325	6188	477.5	859	+	5348	477.5	919	S445	4508	477.5
740	S266	7028	622.5	800	S326	6174	622.5	860	1	5334	622.5	920	S446	4494	622.5
741	S267	7000	477.5	801	S327	6160	477.5	861	S387	5320	477.5	921	S447	4480	477.5
742	S268	6986	622.5	802	S328	6146	622.5	862	+	5306	622.5	922	S448	4466	622.5
743	S269	6972	477.5	803	S329	6132	477.5	863		5292	477.5	923	S449	4452	477.5
744	S270	6958	622.5	804	S330	6118	622.5	864	S390	5278	622.5	924	S450	4438	622.5
745	S271	6944	477.5	805	S331	6104	477.5	865	S391	5264	477.5	925	S451	4424	477.5
746	S272	6930	622.5	806	S332	6090	622.5	866	S392	5250	622.5	926	S452	4410	622.5
747	S273	6916	477.5	807	S333	6076	477.5	867	S393	5236	477.5	927	S453	4396	477.5
748	S274	6902	622.5	808	S334	6062	622.5	868	S394	5222	622.5	928	S454	4382	622.5
749	S275	6888	477.5	809	S335	6048	477.5	869	S395	5208	477.5	929	S455	4368	477.5
750	S276	6874	622.5	810	S336	6034	622.5	870	S396	5194	622.5	930	S456	4354	622.5
751	S277	6860	477.5	811	S337	6020	477.5	871	S397	5180	477.5	931	S457	4340	477.5
752	S278	6846	622.5	812	S338	6006	622.5	872	S398	5166	622.5	932	S458	4326	622.5
753	S279	6832	477.5	813	S339	5992	477.5	873	S399	5152	477.5	933	S459	4312	477.5
754	S280	6818	622.5	814	S340	5978	622.5	874		5138	622.5	934	S460	4298	622.5
755	S281	6804	477.5	815	S341	5964	477.5	875		5124	477.5	935	S461	4284	477.5
756	S282	6790	622.5	816	S342	5950	622.5	876	+	5110	622.5	936	S462	4270	622.5
757	S283	6776	477.5	817	S343	5936	477.5	877	S403	5096	477.5	937	S463	4256	477.5
758	S284	6762	622.5	818	S344	5922	622.5	878		5082	622.5	938	S464	4242	622.5
759	S285	6748	477.5	819	S345	5908	477.5	879	+	5068	477.5	939	S465	4228	477.5
	S286	6734	622.5		S346	5894	622.5		S406	5054	622.5	940		4214	622.5
761 762	S287 S288	6720	477.5	821	S347	5880	477.5	881		5040 5026	477.5 622.5	941	S467	4200	477.5 622.5
	S288 S289	6706 6692	622.5 477.5		S348 S349	5866 5852	622.5 477.5	883		5026	477.5	942	-	4186 4172	622.5 477.5
764	S299	6678	622.5		S350	5838	622.5	884	_	4998	622.5	943	+	4172	622.5
	S290 S291	6664	477.5		S350	5824	477.5	885		4996	477.5	944	+	4144	477.5
	S291	6650	622.5		S352	5810	622.5	886	1	4970	622.5	946	+	4130	622.5
767	S293	6636	477.5		S353	5796	477.5	887	_	4956	477.5	947	S473	4116	477.5
	S294	6622	622.5		S354	5782	622.5	888		4942	622.5	948	S474	4102	622.5
	S295	6608	477.5	829	+	5768	477.5	889	1	4928	477.5	949	1	4088	477.5
	S296	6594	622.5	-	S356	5754	622.5	890	_	4914	622.5	950	S476	4074	622.5
	S297	6580	477.5		S357	5740	477.5	891	1	4900	477.5	951	S477	4060	477.5
	S298	6566	622.5		S358	5726	622.5	892		4886	622.5	952	1	4046	622.5
	S299	6552	477.5		S359	5712	477.5	893	_	4872	477.5	953	S479	4032	477.5
	S300	6538	622.5	834	+	5698	622.5	894	S420	4858	622.5	954	S480	4018	622.5
775	S301	6524	477.5	835	S361	5684	477.5	895	S421	4844	477.5	955	S481	4004	477.5
776	S302	6510	622.5	836	S362	5670	622.5	896	S422	4830	622.5	956	S482	3990	622.5
777	S303	6496	477.5	837	S363	5656	477.5	897	S423	4816	477.5	957	S483	3976	477.5
778	S304	6482	622.5	838	S364	5642	622.5	898	S424	4802	622.5	958	S484	3962	622.5
779	S305	6468	477.5	839	S365	5628	477.5	899	S425	4788	477.5	959	S485	3948	477.5
780	S306	6454	622.5	840	S366	5614	622.5	900	S426	4774	622.5	960	S486	3934	622.5
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No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No	. Text Name	X-axis	Y-axis
961	S487	3920	477.5	1021	S547	3080	477.5	1081		2240	477.5	114		1400	477.5
962	S488	3906	622.5	1022	S548	3066	622.5	1082	S608	2226	622.5	114	2 S668	1386	622.5
963	S489	3892	477.5	1023	S549	3052	477.5	1083	S609	2212	477.5	114	3 S669	1372	477.5
964	S490	3878	622.5	1024	S550	3038	622.5	1084	S610	2198	622.5	114	4 S670	1358	622.5
965	S491	3864	477.5	1025	S551	3024	477.5	1085	S611	2184	477.5	114	5 S671	1344	477.5
966	S492	3850	622.5	1026	S552	3010	622.5	1086	S612	2170	622.5	114	6 S672	1330	622.5
967	S493	3836	477.5	1027	S553	2996	477.5	1087	S613	2156	477.5	114	7 S673	1316	477.5
968	S494	3822	622.5	1028	S554	2982	622.5	1088	S614	2142	622.5	114	8 S674	1302	622.5
969	S495	3808	477.5	1029	S555	2968	477.5	1089	S615	2128	477.5	114	9 S675	1288	477.5
970	S496	3794	622.5	1030	S556	2954	622.5	1090	S616	2114	622.5	115	60 S676	1274	622.5
971	S497	3780	477.5	1031	S557	2940	477.5	1091	S617	2100	477.5	11	51 S677	1260	477.5
972	S498	3766	622.5	1032		2926	622.5	1092		2086	622.5	115	_	1246	622.5
973	S499	3752	477.5	1033	+	2912	477.5	1093	+	2072	477.5	118		1232	477.5
974	S500	3738	622.5	1034		2898	622.5	1094	+	2058	622.5	118		1218	622.5
975	S501	3724	477.5	1035		2884	477.5	1095		2044	477.5	118	_	1204	477.5
976	S502	3710	622.5	1036	+	2870	622.5	1096		2030	622.5	115		1190	622.5
977	S503	3696	477.5	1037	+	2856	477.5	1097	+	2016	477.5	115		1176	477.5
978	S504	3682	622.5	1038		2842	622.5	1098		2002	622.5	118		1162	622.5
979	S505	3668	477.5	1039	+	2828	477.5	1099	+	1988	477.5	115	-	1148	477.5
980	S506 S507	3654	622.5	1040		2814 2800	622.5	1100	+	1974	622.5 477.5	116	-	1134	622.5 477.5
981	S507 S508	3640	477.5 622.5	1041	S567		477.5	1101		1960		116	_	1120	622.5
982 983	S508 S509	3626 3612	622.5 477.5	1042		2786 2772	622.5 477.5	1102	+	1946 1932	622.5 477.5	116	-	1106 1092	477.5
984	S510	3598	622.5	1043		2758	622.5	1103	+	1932	622.5	116	-	1092	622.5
985	S510	3584	477.5	1044		2744	477.5	1105		1904	477.5	116		1076	477.5
986	S512	3570	622.5	1046		2730	622.5	1106	+	1890	622.5	116		1050	622.5
987	S512	3556	477.5	1047		2716	477.5	1107	+	1876	477.5	116	-	1036	477.5
988	S514	3542	622.5	1048	+	2702	622.5	1108		1862	622.5	116	_	1022	622.5
989	S515	3528	477.5	1049		2688	477.5	1109	+	1848	477.5	116	-	1008	477.5
990	S516	3514	622.5	1050		2674	622.5	1110		1834	622.5	117		994	622.5
991	S517	3500	477.5	1051	+	2660	477.5	-	S637	1820	477.5	117		980	477.5
992	S518	3486	622.5	1052		2646	622.5	1112	+	1806	622.5	117		966	622.5
993	S519	3472	477.5	1053		2632	477.5	1113	S639	1792	477.5	117	'3 S699	952	477.5
994	S520	3458	622.5	1054	+	2618	622.5	1114	+	1778	622.5	117	-	938	622.5
995	S521	3444	477.5	1055	S581	2604	477.5	1115	S641	1764	477.5	117	'5 S701	924	477.5
996	S522	3430	622.5	1056	S582	2590	622.5	1116	S642	1750	622.5	117	6 S702	910	622.5
997	S523	3416	477.5	1057	S583	2576	477.5	1117	S643	1736	477.5	117	7 S703	896	477.5
998	S524	3402	622.5	1058	S584	2562	622.5	1118	S644	1722	622.5	117	'8 S704	882	622.5
999	S525	3388	477.5	1059	S585	2548	477.5	1119	S645	1708	477.5	117	9 S705	868	477.5
1000	S526	3374	622.5	1060	S586	2534	622.5	1120	S646	1694	622.5	118	S706	854	622.5
1001	S527	3360	477.5	1061	S587	2520	477.5	1121	S647	1680	477.5	118	S707	840	477.5
1002	S528	3346	622.5	1062	S588	2506	622.5	1122	S648	1666	622.5	118	2 S708	826	622.5
1003	S529	3332	477.5	1063	S589	2492	477.5	1123	S649	1652	477.5	118	3 S709	812	477.5
	S530	3318	622.5		S590	2478	622.5	_	S650	1638	622.5	-	4 S710	798	622.5
	S531	3304	477.5		S591	2464	477.5	_	S651	1624	477.5	-	5 S711	784	477.5
-	S532	3290	622.5		S592	2450	622.5		S652	1610	622.5	-	6 S712	770	622.5
	S533	3276	477.5		S593	2436	477.5	-	S653	1596	477.5	_	37 S713	756	477.5
	S534	3262	622.5	-	S594	2422	622.5	_	S654	1582	622.5	_	8 S714	742	622.5
	S535	3248	477.5		S595	2408	477.5		S655	1568	477.5	-	9 S715	728	477.5
-	S536	3234	622.5		S596	2394	622.5	_	S656	1554	622.5	-	0 S716	714	622.5
	S537	3220	477.5		S597	2380	477.5	_	S657	1540	477.5	-	11 S717	700	477.5
	S538	3206	622.5		S598	2366	622.5		S658	1526	622.5	-	2 S718	686	622.5
-	S539	3192	477.5		S599	2352	477.5	-	S659	1512	477.5	-	3 S719	672	477.5
	S540	3178	622.5		S600	2338	622.5	_	S660	1498	622.5	-	94 S720	658	622.5
-	S541	3164	477.5		S601	2324	477.5		S661	1484	477.5	-	VSSIDUM9	644	477.5
_	S542 S543	3150	622.5		S602 S603	2310 2296	622.5 477.5	_	S662 S663	1470 1456	622.5 477.5	_	6 VSSIDUM10 7 VSSIDUM11	630	622.5 477.5
	S543 S544	3136 3122	477.5 622.5		S604	2282	622.5	_	S664	1442	622.5	-	8 VSSIDUM12	616 602	622.5
-	S544 S545	3108	477.5	-	S605	2268	477.5	-	S665	1442	477.5	-	9 VSSIDUM13	588	477.5
-	S546	3094	622.5		S606	2254	622.5	-	S666	1414	622.5	_	0 VSSIDUM14	-	622.5
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No	Toyt Name	Y avia	V avia	No	Toyt Name	Y ovic	V avia	No	Toyt Name	Y ovic	V avia	No	Toyt Name	Y ovic	V avia
No.	Text Name VSSIDUM16	X-axis 546	Y-axis 622.5	No. 1261	Text Name S742	X-axis	Y-axis 477.5	No. 1321	Text Name S802	-1176	Y-axis 477.5	No.	Text Name 1 S862	-2016	Y-axis 477.5
1201	VSSIDUM16 VSSIDUM20	490	622.5	1261	.	-350	622.5	1321	+	-1176	622.5	138		-2016	622.5
1202	VSSIDUM21	476	477.5	1263	.	-364	477.5	1323	+	-1204	477.5	138		-2044	477.5
1203	VSSIDUM21	462	622.5	1264		-378	622.5	1324		-1218	622.5	138		-2058	622.5
1205	VSSIDUM23	448	477.5	1265	.	-392	477.5	1325	+	-1232	477.5	138	+	-2072	477.5
1206	VSSIDUM24	434	622.5	1266		-406	622.5	1326		-1246	622.5	138	+	-2086	622.5
1207	VSSIDUM25	420	477.5	1267	S748	-420	477.5	1327		-1260	477.5	138		-2100	477.5
1208	VSSIDUM26	406	622.5	1268	.	-434	622.5	1328		-1274	622.5	138		-2114	622.5
1209	VSSIDUM27	392	477.5	1269	.	-448	477.5	1329	+	-1288	477.5	138	-	-2128	477.5
1210	VSSIDUM28	378	622.5		S751	-462	622.5	1330		-1302	622.5	139	+	-2142	622.5
1211	VSSIDUM29	364	477.5	1271	S752	-476	477.5	1331		-1316	477.5	139		-2156	477.5
1212	VSSIDUM30	350	622.5	1272	S753	-490	622.5	1332	S813	-1330	622.5	139	2 S873	-2170	622.5
1213	VSSIDUM31	336	477.5	1273	S754	-504	477.5	1333	S814	-1344	477.5	139	3 S874	-2184	477.5
1214	VSSIDUM32	322	622.5	1274	S755	-518	622.5	1334	S815	-1358	622.5	139	4 S875	-2198	622.5
1215	VSSIDUM33	308	477.5	1275	S756	-532	477.5	1335	S816	-1372	477.5	139	5 S876	-2212	477.5
1216	VSSIDUM34	294	622.5	1276	S757	-546	622.5	1336	S817	-1386	622.5	139	6 S877	-2226	622.5
1217	VSSIDUM35	280	477.5	1277	S758	-560	477.5	1337	S818	-1400	477.5	139	7 S878	-2240	477.5
1218	VSSIDUM36	266	622.5	1278	S759	-574	622.5	1338	S819	-1414	622.5	139	8 S879	-2254	622.5
1219	VSSIDUM37	252	477.5	1279	S760	-588	477.5	1339	S820	-1428	477.5	139	9 S880	-2268	477.5
1220	VSSIDUM38	238	622.5	1280	S761	-602	622.5	1340	S821	-1442	622.5	140	S881	-2282	622.5
1221	VSSIDUM39	224	477.5	1281	S762	-616	477.5	1341	S822	-1456	477.5	140	1 S882	-2296	477.5
1222	VSSIDUM40	210	622.5	1282	S763	-630	622.5	1342	S823	-1470	622.5	140	2 S883	-2310	622.5
1223	VSSIDUM41	196	477.5	1283	S764	-644	477.5	1343	S824	-1484	477.5	140	3 S884	-2324	477.5
1224	VSSIDUM42	182	622.5	1284	S765	-658	622.5	1344	S825	-1498	622.5	140	4 S885	-2338	622.5
1225	VSSIDUM43	168	477.5	1285	S766	-672	477.5	1345	S826	-1512	477.5	140	5 S886	-2352	477.5
1226	VSSIDUM44	154	622.5	1286	.	-686	622.5	1346		-1526	622.5	140	+	-2366	622.5
1227	VSSIDUM45	140	477.5	1287	S768	-700	477.5	1347		-1540	477.5	140		-2380	477.5
1228	VSSIDUM46	126	622.5	1288	.	-714	622.5	1348	+	-1554	622.5	140	+	-2394	622.5
1229	VSSIDUM47	112	477.5	1289	.	-728	477.5	1349		-1568	477.5	140		-2408	477.5
1230	VSSIDUM48	98	622.5	1290	.	-742	622.5	1350	+	-1582	622.5	141	+	-2422	622.5
1231	VSSIDUM49	84	477.5	1291	S772	-756	477.5	1351	S832	-1596	477.5	141	+	-2436	477.5
1232	VSSIDUM50	70	622.5	1292		-770 -704	622.5	1352	+	-1610	622.5	141		-2450	622.5
1233	VSSIDUM51	56	477.5		S774	-784 -700	477.5	1353	+	-1624	477.5	141	+	-2464	477.5
1234 1235	VSSIDUM52 VSSIDUM53	42 28	622.5 477.5	1294 1295	.	-798 -812	622.5 477.5	1354		-1638 -1652	622.5 477.5	141		-2478 -2492	622.5 477.5
1235	VSSIDUM54	14	622.5		S777	-826	622.5	1356		-1666	622.5	141		-2492	622.5
1237	VSSIDUM55	0	477.5	1290	S778	-840	477.5	1357	S838	-1680	477.5	141	+	-2520	477.5
1238	VSSIDUM56	-14	622.5	1298	.	-854	622.5	1358		-1694	622.5	141		-2534	622.5
	VSSIDUM57	-28	477.5		S780	-868	477.5	-	S840	-1708	477.5	_	9 S900	-2548	477.5
	S721	-42	622.5		S781	-882	622.5		S841	-1722	622.5		0 S901	-2562	622.5
	S722	-56	477.5		S782	-896	477.5		S842	-1736	477.5		1 S902	-2576	477.5
	S723	-70	622.5		S783	-910	622.5		S843	-1750	622.5		2 S903	-2590	622.5
-	S724	-84	477.5		S784	-924	477.5		S844	-1764	477.5	_	3 S904	-2604	477.5
	S725	-98	622.5		S785	-938	622.5		S845	-1778	622.5	142	1	-2618	622.5
	S726	-112	477.5		S786	-952	477.5		S846	-1792	477.5		5 S906	-2632	477.5
	S727	-126	622.5		S787	-966	622.5		S847	-1806	622.5		6 S907	-2646	622.5
1247	S728	-140	477.5	1307	S788	-980	477.5	1367	S848	-1820	477.5	142	7 S908	-2660	477.5
1248	S729	-154	622.5	1308	S789	-994	622.5	1368	S849	-1834	622.5	142	8 S909	-2674	622.5
1249	S730	-168	477.5	1309	S790	-1008	477.5	1369	S850	-1848	477.5	142	9 S910	-2688	477.5
1250	S731	-182	622.5	1310	S791	-1022	622.5	1370	S851	-1862	622.5	143	S911	-2702	622.5
1251	S732	-196	477.5	1311	S792	-1036	477.5	1371	S852	-1876	477.5	143	1 S912	-2716	477.5
1252	S733	-210	622.5	1312	S793	-1050	622.5	1372	S853	-1890	622.5	143	2 S913	-2730	622.5
	S734	-224	477.5		S794	-1064	477.5		S854	-1904	477.5	_	3 S914	-2744	477.5
	S735	-238	622.5		S795	-1078	622.5		S855	-1918	622.5		4 S915	-2758	622.5
	S736	-252	477.5		S796	-1092	477.5		S856	-1932	477.5	_	5 S916	-2772	477.5
-	S737	-266	622.5		S797	-1106	622.5		S857	-1946	622.5	_	6 S917	-2786	622.5
	S738	-280	477.5	_	S798	-1120	477.5		S858	-1960	477.5		7 S918	-2800	477.5
	S739	-294	622.5		S799	-1134	622.5		S859	-1974	622.5		8 S919	-2814	622.5
	S740	-308	477.5		S800	-1148	477.5		S860	-1988	477.5		9 S920	-2828	477.5
1260	S741	-322	622.5	1320	S801	-1162	622.5	1380	S861	-2002	622.5	144	S921	-2842	622.5

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Fig.	No.	Text Name	Y-avia	Y-axis	No.	Toyt Name	Y. avia	Y-axis	No.	Toyt Name	Y. avia	Y-axis	No	Toyt Name	Y. avia	Y-axis
1445 5020	_												_			477.5
1445 1445 1476 1476 1476 1476 1476 1477 1478						.		-	-					+		622.5
1444 5826 2868 622.5 1506 5868 3738 622.5 1506 5104 477.5 1505 5106 477.5 1505 5106 477.5 1505 5106 477.5 1505 5106 477.5 1505 5106 477.5 1505 5106 477.5 1505 5106 477.5 1506 5104 4606 622.5 1506 5107 4406 622.5 1507 4406 622.5 1508 4406					-	.		-	-					+		477.5
1445 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1447 1446 1446 1446 1447 1446																622.5
March Subsect Company Compan					-	.		-	-					+		477.5
May	1446	S927	-2926	622.5	1506	S987	-3766	622.5	1566	S1047	-4606	622.5	162	6 S1107	-5446	622.5
1445 5939	1447	S928	-2940	477.5	1507	S988	-3780	477.5	1567	S1048	-4620	477.5	162	7 S1108	-5460	477.5
1455 5832 - 2986 4775 1516 5896 - 3822 622.5 1572 5876 5105 - 4662 622.5 1630 51111 - 5502 60 1452 5833 - 3001 622.5 - 1512 5893 - 3806 622.5 - 1572 58063 - 4696 622.5 - 1633 51112 - 5564 41 4145 5905 - 3038 622.5 - 1513 5894 - 3896 477.5 - 1515 5896 - 3898 - 3898 - 477.5 - 1515 5896 - 3898 - 3898 - 477.5 - 1515 - 1516 - 1	1448	S929	-2954	622.5	1508	S989	-3794	622.5	1568	S1049	-4634	622.5	162	8 S1109	-5474	622.5
1451 5932	1449	S930	-2968	477.5	1509	S990	-3808	477.5	1569	S1050	-4648	477.5	162	9 S1110	-5488	477.5
1462 5933 3-3010 622.5 1512 5993 3-3850 622.5 1572 51063 4-4900 622.5 1632 51113 3-5530 62 625 1464 5835 3-3038 622.5 1514 5996 3-386 477.5 1515 5996 3-386 622.5 1574 5105 5105 4-704 477.5 1633 51114 5-554 625 1465 5937 3-306 622.5 1516 5997 3-906 622.5 1576 5105 4-704 4-77.5 1625 5996 3-382 4-77.5 1516 5999 3-904 622.5 1576 5105 5-706 4-746 622.5 1638 51116 5-6572 4146 685 5939 3-904 622.5 1516 5999 3-904 622.5 1576 51059 4-774 622.5 1638 51116 5-658 622.5 1516 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51116 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51116 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 5999 3-904 622.5 1576 51059 4-774 622.5 1637 51118 51000 3-904 622.5 1576 51059 4-774 622.5 1637 51118 51000 3-904 622.5 1576 51059 4-774 622.5 1637 51118 51000 4-775 15000 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-775 4-786 4-786 4-775 4-786 4-786 4-775 4-786 4-775 4-786 4-786 4-775 4-786 4-786 4-775 4-786 4-775 4-786 4-786 4-775 4-786 4-786 4-775 4-786 4-786 4-775 4-786 4-786 4-775 4-786 4-786	1450	S931	-2982	622.5	1510	S991	-3822	622.5	1570	S1051	-4662	622.5	163	0 S1111	-5502	622.5
1855 3934 -3924 477.5 1515 3994 -3986 477.5 1573 51054 -4704 477.5 1633 51114 -5575 675	1451	S932	-2996	477.5	1511	S992	-3836	477.5	1571	S1052	-4676	477.5	163	1 S1112	-5516	477.5
1456 S936 -3038 G225 1516 S996 -3862 477.5 1516 S996 -3862 477.5 1516 S997 -3906 G22.5 1516 S997 -3906 G22.5 1516 S996 -3862 477.5 1577 S1056 -4732 477.5 1586 S1117 -5586 G2 G25	1452	S933	-3010	622.5	1512	S993	-3850	622.5	1572	S1053	-4690	622.5	163	2 S1113	-5530	622.5
1455 5996 -3002 477.5 1515 5996 -3902 477.5 1575 51056 -4722 477.5 1568 5117 -5286 502 1518 5998 -3902 477.5 1578 51057 -4746 622.5 1588 51117 -5286 502 1468 58939 -3094 622.5 1519 51000 -3948 477.5 1578 51056 -4774 622.5 1589 51057 -4746 477.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 51057 -4746 622.5 1589 510	1453					.		-	1573				163	3 S1114		477.5
1455 3937 -3066 622.5 1516 5897 -3060 622.5 1517 51056 -4746 622.5 1518 51056 -4766 477.5 1518 51056 -4766 477.5 1518 51056 -4766 477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -477.5 1518 51056 -4766 -477.5 1518 51056 -4766 -477.5 1518 51056 -477.5 15						.		-	1574							622.5
1459 5938 3090 477.5 1518 5990 3934 622.5 1518 5990 3934 622.5 1518 5990 3934 622.5 1518 5990 3934 622.5 1518 5990 3934 622.5 1518 5990 3934 622.5 1518 5990 3934 622.5 1518 5990 477.5 1528 51000 3948 477.5 1528 51000 3948 477.5 1528 51000 3948 477.5 1528 51000 3948 477.5 1528 51000 3948 477.5 1528 51000 3948 477.5 1528 51000 3948 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002 3976 477.5 1528 51002																477.5
1458 5939 3094 622.5 1518 5999 3934 622.8 1578 51059 477.8 477.5 1638 51112 500.0 622.5 1529 51001 3962 622.5 1529 51001 3962 622.5 1529 51001 3962 622.5 1529 51002 3976 477.5 1561 51002 4816 477.5 1641 51122 5626 441 442 622.5 1529 51003 3990 622.5 1529 51003 3990 622.5 1529 51003 3990 622.5 1529 51003 3990 622.5 1529 51003 3990 622.5 1529 51003 3990 477.5 1528 51003 4980 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51003 477.5 1528 51004 4004 477.5 1528 51004 4004 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51006 4032 477.5 1528 51009 4074 622.5 1588 51060 4892 477.5 1648 51120 5-768 6148					-	.		-	-					+		622.5
1450 S940					-	.		-								477.5
1460 S941																622.5
1461 5942 .3136 477.5 1622 51002 .3976 477.5 1581 \$1002 .4816 477.5 1623 \$1003 .3990 622.5 1582 \$1063 .4830 622.5 1624 \$1013 .5900 627.5 1624 \$1013 .4900 477.5 1623 \$1003 .4900 477.5 1623 \$1003 .4900 477.5 1624 \$1005 .4018 .622.5 1626 \$1007 .4004 .477.5 1623 .4830 .622.5 1624 .4018 .4014 .477.5 .4018 .4014									-				-	+		477.5 622.5
1462 S943						.		-	-				-	_		477.5
1463 S944 -3164 477.5 1523 S1004 -4004 477.5 1563 S1066 -4884 477.5 1664 S1124 -5684 4765 1468 S945 -3178 622.5 1526 S1006 -4022 477.5 1568 S1066 -4872 477.5 147.5 1468 S947 -3206 622.5 1526 S1007 -4906 622.5 1526 S1007 -4906 622.5 1526 S1007 -4906 477.5 1587 S1068 -4900 477.5 1645 S1122 -5726 67 1468 S947 -3204 672.5 1528 S1009 -4074 622.5 1588 S1069 -4914 622.5 1469 S950 -3248 477.5 1529 S1010 -4088 477.5 1589 S1070 -4928 477.5 1470 S951 -3262 622.5 1532 S1011 -4102 622.5 1590 S1071 -4942 622.5 1625 S1132 -5786 47 1471 S952 -3276 477.5 1531 S1012 -4116 477.5 1591 S1072 -4966 477.5 1651 S1132 -5786 47 1473 S955 -3318 622.5 1532 S1013 -4130 622.5 1592 S1073 -4998 622.5 1475 S956 -3332 477.5 1535 S1016 -4172 477.5 1594 S1075 -4998 622.5 1475 S956 -3332 477.5 1535 S1016 -4172 477.5 1596 S1077 -5026 622.5 1656 S1131 -5824 47 476 S957 -3346 622.5 1538 S1019 -4214 622.5 1598 S1077 -5026 622.5 1656 S1131 -5826 47 478 S959 -3374 622.5 1538 S1019 -4214 622.5 1599 S1076 -5012 477.5 1655 S1138 -5880 47 488 S969 -3348 477.5 1544 S1022 -4226 477.5 1602 S1083 -5110 622.5 1602 S1083 -5110 622.5 1666 S1140 -5998 47 1488 S969 -3446 477.5 1544 S1022 -4226 477.5 1602 S1083 -5108 -522.6 1602 S1083 -5108 622.5 1666 S1140 -5998 47 1488 S969 -3486 622.5 1546 S1027 -4326 622.5 1600 S1081 -5086 477.5 1665 S1140 -5998 47 1488 S969 -3486 622.5 1544 S1022 -4226 477.5 1603 S1084 -5124 477.5 1665 S1140 -5998 47 1488 S969 -3486 622.5 1546 S1027 -4326 622.5 1600 S1089 -5194 622.5 1666 S1140 -5998 47 1489 S977																622.5
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1465 5946 .3192 477.5 1525 51006 .4032 477.5 1566 51066 .4872 477.5 1566 51066 .4872 477.5 1466 51127 .5726 626 627.5 1467 5948 .3202 477.5 1526 51008 .4000 477.5 1587 51068 .4900 477.5 1467 5948 .3202 477.5 1528 51009 .4074 622.5 1588 51069 .4914 622.5 1648 51128 .5724 47 627.5 1469 5950 .3248 477.5 1529 51010 .4088 477.5 1589 51070 .4928 477.5 1649 51130 .5768 47 627.5 1470 5951 .3262 622.5 1532 51011 .4102 622.5 1599 51071 .4942 622.5 1650 51131 .5762 .66 .477.5 1472 5953 .3290 622.5 1532 51013 .4130 622.5 1529 51072 .4956 .477.5 .4956 .477.5 .478 .478 .4956 .3318 622.5 .478 .4158 .4258 .475 .4158 .4258 .4258 .475 .4258					-	.		-	-					+		622.5
1466 5947 -3206 622.5 1467 5948 -3220 477.5 1527 5108 -4060 477.5 1588 51067 -4886 622.5 1468 5949 -3234 622.5 1469 5950 -3248 477.5 1528 51010 -4088 477.5 1588 51070 -4928 477.5 1470 5951 -3262 622.5 1530 51011 -4102 622.5 1590 51071 -4942 622.5 1689 51131 -5782 62 1473 5954 -3304 477.5 1533 51014 -4114 477.5 1591 51072 -4956 477.5 1591 51013 -4130 622.5 1473 5956 -3332 477.5 1533 51014 -4116 477.5 1591 51072 -4956 622.5 1685 51131 -5782 62 1473 5955 -3336 622.5 1536 51016 -4172 477.5 1591 51072 -4956 622.5 1665 51131 -5782 62 1473 5956 -3336 622.5 1536 51017 -4186 622.5 1592 51073 -4970 622.5 1653 51134 -5824 47 477.5 1476 5957 -3346 622.5 1536 51016 -4172 477.5 1593 51074 -4984 477.5 1653 51136 -5852 47 477.5 1478 5959 -3336 622.5 1538 51016 -4172 477.5 1595 51076 -5012 477.5 1665 51136 -5852 47 477.5 1480 5960 -3338 477.5 1538 51019 -4214 622.5 1481 5962 -3416 477.5 1538 51020 -4228 477.5 1697 51078 -5026 622.5 1666 51137 -5866 62 478.5 1485 5966 -3472 477.5 1545 51022 -4256 477.5 1605 51081 -5022 5166 51141 -5936 47 488 5967 -3486 622.5 1544 51022 -4256 477.5 1603 51084 -715 1661 51142 -5936 47 488 5967 -3486 622.5 1548 51026 -4312 477.5 1603 51084 -477.5 1661 51142 -5936 47 488 5967 -3486 622.5 1548 51022 -4256 477.5 1603 51084 -477.5 1663 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148 -602.5 1662 51148																477.5
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1491 S972 -3556 477.5 1492 S973 -3570 622.5 1493 S974 -3584 477.5 1494 S975 -3598 622.5 1495 S976 -3612 477.5 1496 S977 -3626 622.5 1497 S978 -3640 477.5 1498 S979 -3654 622.5 1499 S980 -3668 477.5 1551 S1032 -4396 477.5 162 S1093 -5250 622.5 1612 S1093 -5250 622.5 1613 S1094 -5264 477.5 1614 S1095 -5278 622.5 1615 S1096 -5292 477.5 1615 S1096 -5292 477.5 1616 S1097 -5306 622.5 162 S1038 -4480 477.5 1616 S1097 -5306 <td></td> <td>-</td> <td>_</td> <td></td> <td>622.5</td>													-	_		622.5
1492 S973 -3570 622.5 1552 S1033 -4410 622.5 1612 S1093 -5250 622.5 1672 S1153 -6090 62 1493 S974 -3584 477.5 1553 S1034 -4424 477.5 1613 S1094 -5264 477.5 1673 S1154 -6104 47 1494 S975 -3612 477.5 1555 S1036 -4438 622.5 1614 S1095 -5278 622.5 1674 S1155 -6118 62 1496 S977 -3626 622.5 1556 S1037 -4466 622.5 1615 S1096 -5292 477.5 1675 S1156 -6132 47 1497 S978 -3640 477.5 1557 S1038 -4480 477.5 1616 S1097 -5306 622.5 1676 S1157 -6146 62 1498 S979 -3654 622.5 1558 S1039 -4494 622.5 1618 S1099 -5334 622.5 1678 S1150						1							-			477.5
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1496 S977 -3626 622.5 1497 S978 -3640 477.5 1498 S979 -3654 622.5 1499 S980 -3668 477.5 1559 S1030 -4494 622.5 1616 S1097 -5306 622.5 1617 S1098 -5320 477.5 1618 S1099 -5334 622.5 1678 S1159 -6160 47 1679 S1150 -6174 62 1679 S1160 -6188 47 1679 S1160 -6188 47													_		l	477.5
1498 S979 -3654 622.5 1558 S1039 -4494 622.5 1618 S1099 -5334 622.5 1678 S1159 -6174 62 1499 S980 -3668 477.5 1559 S1040 -4508 477.5 477.5 1619 S1100 -5348 477.5 477.5 1679 S1160 -6188 477.5	1496	S977	-3626				-4466	622.5	1616	S1097	-5306		167	6 S1157	-6146	622.5
1499 S980 -3668 477.5 1559 S1040 -4508 477.5 1619 S1100 -5348 477.5 1679 S1160 -6188 47	1497	S978	-3640	477.5	1557	S1038	-4480	477.5	1617	S1098	-5320	477.5	167	7 S1158	-6160	477.5
	1498	S979	-3654	622.5	1558	S1039	-4494	622.5	1618	S1099	-5334	622.5	167	8 S1159	-6174	622.5
	1499	S980	-3668	477.5	1559	S1040	-4508	477.5	1619	S1100	-5348	477.5	167	9 S1160	-6188	477.5
	1500	S981	-3682	622.5	1560	S1041	-4522	622.5			-5362	622.5	168	0 S1161	-6202	622.5

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No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis
1681	S1162	-6216	477.5	1741	S1222	-7056	477.5	1801	S1282	-7896	477.5	186		-8736	477.5
1682	S1162 S1163	-6230	622.5	1741		-7070	622.5	1802	S1282	-7910	622.5	186		-8750	622.5
1683	S1164	-6244	477.5	1743		-7084	477.5	1803	S1284	-7924	477.5	186		-8764	477.5
—	S1165	-6258	622.5	1744		-7098	622.5	1804		-7938	622.5	186		-8778	622.5
1685	S1166	-6272	477.5	1745		-7112	477.5	1805		-7952	477.5	186		-8792	477.5
1686	S1167	-6286	622.5	1746	.	-7126	622.5	1806	S1287	-7966	622.5	186		-8806	622.5
1687	S1168	-6300	477.5	1747	S1228	-7140	477.5	1807	S1288	-7980	477.5	186		-8820	477.5
1688	S1169	-6314	622.5	1748	S1229	-7154	622.5	1808	S1289	-7994	622.5	186	3 S1349	-8834	622.5
1689	S1170	-6328	477.5	1749	S1230	-7168	477.5	1809	S1290	-8008	477.5	186	9 S1350	-8848	477.5
1690	S1171	-6342	622.5	1750	S1231	-7182	622.5	1810	S1291	-8022	622.5	187	S1351	-8862	622.5
1691	S1172	-6356	477.5	1751	S1232	-7196	477.5	1811	S1292	-8036	477.5	187	1 S1352	-8876	477.5
1692	S1173	-6370	622.5	1752	S1233	-7210	622.5	1812	S1293	-8050	622.5	187	2 S1353	-8890	622.5
1693	S1174	-6384	477.5	1753	S1234	-7224	477.5	1813	S1294	-8064	477.5	187	S1354	-8904	477.5
1694	S1175	-6398	622.5	1754	S1235	-7238	622.5	1814	S1295	-8078	622.5	187	1 S1355	-8918	622.5
1695	S1176	-6412	477.5	1755	S1236	-7252	477.5	1815	S1296	-8092	477.5	187	5 S1356	-8932	477.5
1696	S1177	-6426	622.5	1756	S1237	-7266	622.5	1816	S1297	-8106	622.5	187	S1357	-8946	622.5
1697	S1178	-6440	477.5	1757	S1238	-7280	477.5	1817	S1298	-8120	477.5	187	7 S1358	-8960	477.5
1698	S1179	-6454	622.5	1758	S1239	-7294	622.5	1818	S1299	-8134	622.5	187	S1359	-8974	622.5
1699	S1180	-6468	477.5	1759	S1240	-7308	477.5	1819	S1300	-8148	477.5	187	S1360	-8988	477.5
1700	S1181	-6482	622.5	1760	S1241	-7322	622.5	1820	S1301	-8162	622.5	188	S1361	-9002	622.5
	S1182	-6496	477.5	1761	S1242	-7336	477.5	1821	S1302	-8176	477.5	188	1 S1362	-9016	477.5
1702	S1183	-6510	622.5	1762	S1243	-7350	622.5	1822	S1303	-8190	622.5	188	2 S1363	-9030	622.5
1703	S1184	-6524	477.5	1763		-7364	477.5	1823	S1304	-8204	477.5	188	3 S1364	-9044	477.5
1704	S1185	-6538	622.5	1764	S1245	-7378	622.5	1824	S1305	-8218	622.5	188	1 S1365	-9058	622.5
1705	S1186	-6552	477.5	1765	S1246	-7392	477.5	1825	S1306	-8232	477.5	188	S1366	-9072	477.5
1706	S1187	-6566	622.5	1766	S1247	-7406	622.5	1826	S1307	-8246	622.5	188		-9086	622.5
1707	S1188	-6580	477.5	1767	S1248	-7420	477.5	1827	S1308	-8260	477.5	188	7 S1368	-9100	477.5
1708	S1189	-6594	622.5	1768	S1249	-7434	622.5	1828	S1309	-8274	622.5	188	3 S1369	-9114	622.5
1709	S1190	-6608	477.5	1769	S1250	-7448	477.5	1829	S1310	-8288	477.5	188	9 S1370	-9128	477.5
-	S1191	-6622	622.5		S1251	-7462	622.5	1830	.	-8302	622.5	189	-	-9142	622.5
1711	S1192	-6636	477.5	1771	S1252	-7476	477.5	1831	S1312	-8316	477.5	189		-9156	477.5
1712	S1193	-6650	622.5	1772		-7490	622.5	1832	S1313	-8330	622.5	189	2 S1373	-9170	622.5
-	S1194	-6664	477.5		S1254	-7504	477.5	1833	.	-8344	477.5		3 S1374	-9184	477.5
	S1195	-6678	622.5	1774	.	-7518	622.5	-	S1315	-8358	622.5	189	-	-9198	622.5
	S1196	-6692	477.5	1775		-7532	477.5	1835		-8372	477.5	189		-9212	477.5
-	S1197	-6706	622.5		S1257	-7546	622.5	1836	.	-8386	622.5		S1377	-9226	622.5
1717	S1198	-6720	477.5	1777	S1258	-7560	477.5	1837	S1318	-8400	477.5	189		-9240	477.5
1718	S1199	-6734	622.5	1778	.	-7574	622.5	1838		-8414	622.5	189		-9254	622.5
	S1200	-6748	477.5		S1260	-7588	477.5		S1320	-8428	477.5		9 S1380	-9268	477.5
_	S1201	-6762	622.5		S1261	-7602	622.5	-	S1321	-8442	622.5	_	S1381	-9282	622.5
_	S1202	-6776	477.5		S1262	-7616	477.5	-	S1322	-8456	477.5	_	1 S1382	-9296	477.5
-	S1203	-6790	622.5		S1263	-7630 -7644	622.5		S1323	-8470	622.5		2 S1383	-9310	622.5
_	S1204	-6804	477.5		S1264	-7644	477.5	-	S1324	-8484	477.5		S1384	-9324	477.5
_	S1205	-6818	622.5		S1265	-7658 7672	622.5	-	S1325	-8498	622.5	_	S1385	-9338	622.5
-	S1206	-6832	477.5		S1266	-7672 7686	477.5	_	S1326	-8512 8526	477.5		S1386	-9352	477.5
	S1207	-6846	622.5		S1267	-7686 -7700	622.5	-	S1327	-8526	622.5	_	S1387	-9366	622.5
-	S1208 S1209	-6860	477.5		S1268 S1269	-7700	477.5	-	S1328	-8540 8554	477.5		7 S1388 3 S1389	-9380	477.5
		-6874	622.5			-7714	622.5		S1329	-8554	622.5		-	-9394	622.5
-	S1210	-6888	477.5		S1270	-7728 -7742	477.5		S1330	-8568 8582	477.5	_	S1390	-9408	477.5
	S1211	-6902	622.5		S1271	-7742 7756	622.5	-	S1331	-8582 8506	622.5		S1391	-9422	622.5
_	S1212	-6916	477.5		S1272	-7756 -7770	477.5		S1332	-8596 8610	477.5		1 S1392	-9436	477.5
	S1213	-6930	622.5		S1273	-7770 -7794	622.5	_	S1333	-8610	622.5	_	2 S1393	-9450	622.5
	S1214	-6944	477.5		S1274	-7784	477.5		S1334	-8624 8638	477.5		S1394	-9464	477.5
	S1215	-6958	622.5		S1275	-7798	622.5	-	S1335	-8638	622.5		\$1395 \$1306	-9478	622.5
	S1216	-6972	477.5		S1276	-7812 -7826	477.5	-	S1336	-8652	477.5	_	S1396	-9492	477.5
	S1217	-6986	622.5		S1277	-7826 -7840	622.5	-	S1337	-8666	622.5	_	S1397	-9506	622.5
_	S1218	-7000 -7014	477.5		S1278	-7840 -7840	477.5	_	S1338	-8680	477.5		7 S1398	-9520	477.5
	S1219	-7014	622.5		S1279	-7854 -7869	622.5	-	S1339	-8694	622.5		S1399	-9534	622.5
	S1220	-7028	477.5		S1280	-7868	477.5	-	S1340	-8708	477.5		S1400	-9548	477.5
1/40	S1221	-7042	622.5	1800	S1281	-7882	622.5	1860	S1341	-8722	622.5	192	S1401	-9562	622.5

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1922 S1403	No.	Text Name	X-axis	Y-axis	No.	Text Name	X-axis	Y-axis	N	0.	Text Name	X-axis	Y-axis
	1921	S1402	-9576	477.5	1981	VSSIDUM60	-10416	477.5	20	41	GOUT25	-11256	477.5
1924 S1406 9618 622.5 1928 VSSIDUM64 1-10472 477.5 1928 CSSIDUM65 1-10472 477.5 1928 CSSIDUM65 1-10472 477.5 1928 CSSIDUM65 1-10486 622.5 1928 S1408 9680 477.5 1928 VSSIDUM65 1-10486 622.5 1929 S1410 9688 477.5 1928 VSSIDUM65 1-10486 622.5 1929 S1410 9688 477.5 1928 VSSIDUM66 1-10486 622.5 1929 VSSIDUM67 1-10486 622.5 1929 VSSIDUM68 1-10486 622.5 1929 VSSIDUM67 1-10486 622.5 1929 VSSIDUM67 1-10486 622.5 1929 VSSIDUM67 1-10486 622.5 1929 VSSIDUM76 1-10486 622.5 1929 VSSIDUM76 1-10486 622.5 1929 VSSIDUM76 1-10486 622.5 1929 VSSIDUM76 1-10546 622.5	1922	S1403	-9590	622.5	1982	VSSIDUM61	-10430	622.5	20	42	GOUT25	-11270	622.5
1925 15406 .9632 477.5	1923	S1404	-9604	477.5	1983	VSSIDUM62	-10444	477.5	20	43	GOUT26	-11284	477.5
1922 1940	1924	S1405	-9618	622.5	1984	VSSIDUM63	-10458	622.5	20	44	GOUT26	-11298	622.5
1922 S1408 .9860 .477.5	1925	S1406	-9632	477.5	1985	VSSIDUM64	-10472	477.5	20	45	GOUT27	-11312	477.5
1928 S1409 .09674 622.5	1926	S1407	-9646	622.5	1986	VSSIDUM65	-10486	622.5	20	46	GOUT27	-11326	622.5
1920 S1410	1927	S1408	-9660	477.5	1987	VSSIDUM66	-10500	477.5	20	47	GOUT28	-11340	477.5
1930 S1411	1928	S1409	-9674	622.5	1988	VSSIDUM67	-10514	622.5	20	48	GOUT28	-11354	622.5
1931 S1412	-				l				_	_			477.5
1932 S1414 9-974	-				l				_				622.5
1933 S1414					l				_				477.5
1934 S1415 .9758 622.5 1994 VSSIDUM73 .10596 622.5 1936 S1416 .9772 477.5 1995 VSSIDUM74 .10612 477.5 1996 SSIDUM75 .10626 622.5 1937 S1418 .9800 477.5 1997 VSSIDUM76 .10640 477.5 1938 S1419 .99814 622.5 1998 VSSIDUM77 .10654 622.5 1938 S1419 .9982 622.5 1998 VSSIDUM79 .10684 477.5 1994 VSSIDUM80 .10684 477.5 1994 VSSIDUM80 .10684 477.5 1994 VSSIDUM80 .10684 477.5 1994 VSSIDUM80 .10784 477.5 1994 S1422 .9986 477.5 .2001 VSSIDUM80 .10796 622.5 1934 S1424 .9884 477.5 .2003 VSSIDUM80 .10796 622.5 1937 S1428 .9994 477.5 .2006 VSSIDUM80 .10764 477.5 .2006 VSSIDUM80 .10764 477.5 .2006 VSSIDUM80 .10784 477.5 .2006 VSSIDUM80 .10784 477.5 .2006 VSSIDUM80 .10784 .477.5 .2006 VSSIDUM80 .10784 .477.5 .2006 VSSIDUM80 .10784 .477.5 .2006 VSSIDUM80 .10784 .477.5 .2006 .477.5 .2006 .477.5 .2006 .477.5 .2006 .477.5 .2006 .477.5 .2007 .478.5 .2006 .477.5 .2007 .478.5 .2006 .477.5 .2006 .477.5 .2006 .477.5 .2007 .478.5 .2006 .477.5 .2007 .478.5 .2006 .477.5 .2006					l								622.5
1935 S1416 9772 477.5 1936 S1417 9786 622.5 1939 VSSIDUM76 10606 622.5 1939 S1419 9814 622.5 1939 VSSIDUM77 10654 622.5 1939 S1420 9828 477.5 1939 VSSIDUM77 10654 622.5 1939 VSSIDUM77 10654 622.5 1939 VSSIDUM77 10654 622.5 1939 VSSIDUM78 10686 477.5 1939 VSSIDUM78 10686 477.5 1939 VSSIDUM78 10686 477.5 1939 VSSIDUM79 10682 622.5 1944 S1422 9856 477.5 1939 VSSIDUM80 10696 477.5 1942 S1423 9870 622.5 1943 S1424 9884 477.5 1945 S1426 9888 622.5 1945 S1426 9912 477.5 1946 S1427 9926 622.5 1945 S1428 9994 477.5 1946 S1427 9926 622.5 1945 S1428 9994 477.5 1946 S1427 9926 622.5 1949 S1429 9954 622.5 1949 S1430 9998 477.5 1950 S1431 9998 622.5 1951 S1432 9996 477.5 1952 S1433 10004 477.5 1952 S1433 10004 477.5 1955 S1436 10006 477.5 1955 S1436 10006 477.5 1955 S1436 10006 477.5 1955 S1436 10006 477.5 1956 S1437 10006 622.5 1951 S1430 10006 477.5 1956 S1437 10006 622.5 1957 S1438 10004 477.5 1956 S1437 10006 622.5 1956 S1437 10006 622.5 1956 S1437 10006 622.5 1956 S1437 10006 622.5 1956 S1430 10006 477.5 1956 S1437 10006 622.5 1956 S1430 10006 477.5 1958 S1430 10006 477.5 1958 S1430 10006 477.5 1958 S1430 10006 477.5 1958 S1430 10006 477.5 1956	-				l				_		_		477.5
1936 S1417					l				—		_		622.5
1937 S1418 9800 477.5 1938 S1419 9814 622.5 1939 S15IDUM7 10654 622.5 2058 VRGH_L .11480 477.5 1940 S1421 .9842 622.5 2000 VSSIDUM7 .10682 622.5 2060 LVGL_L .11522 622.5 1941 S1422 .9856 477.5 2001 VSSIDUM80 .10698 477.5 2060 LVGL_L .11526 622.5 1943 S1424 .9884 477.5 2003 VSSIDUM80 .10696 477.5 2060 LVGL_L .11526 622.5 1945 S1426 .9912 477.5 2003 VSSIDUM81 .10710 622.5 2061 LVGL_L .11536 477.5 1946 S1427 .9926 622.5 2004 VSSIDUM81 .10752 477.5 2064 GOUT32 .11562 622.5 1945 S1426 .9995 622.5 2006 VSSIDUM86 .10760 622.5 2066 GOUT32 .11562 622.5 2075 VSSIDUM86 .10760 622.5 2075 VSSIDUM86 .10760 622.5 2075 VSSIDUM88 .10760 622.5 2075 VSSIDUM89 .10820 622.5 2075 VSSIDUM90 .10820 622.5 2075 VSSIDUM10 .10760 622.5 2075 VSSIDUM90 .10820 622.5 2075 2075 VSSIDUM10 .10760 622.5 2075 VSSIDUM90 .10820 622.5 2075 2075 VSSIDUM10 .10760 622.5 2075 2075 VSSIDUM90 .10820 622.5 2075 2075 VSSIDUM10 .10760 622.5 2075 2075 2075 2075 2075 2075 2075 2075 2075 2075 2075 2075 2075 2075 2075	-				l				l		_		477.5
1938 S1419		_			l				_		_		622.5
1939 S1420					l				_		_		477.5
1940 S1421					l				_		_		622.5
1941 S1422					l				—		_		477.5
1942 S1423		_			l				_	-			622.5
1943 S1424					l				_		_		
1944 S1425	-				l —				_				
1945 S1426 -9912 477.5 2005 VSSIDUM84 -10752 477.5 2066 GOUT32 -11592 477.5 2068 S1427 -9926 622.5 2006 VSSIDUM85 -10766 622.5 2066 VGLO_L -11606 622.5 2067 VGLO_L -11604 477.5 2078 VSSIDUM85 -10794 622.5 2068 VGLO_L -11620 477.5 2078 VSSIDUM85 -10794 622.5 2069 VGLO_L -11634 622.5 2079 VSSIDUM85 -10794 622.5 2069 VGLO_L -11634 622.5 2079 VSSIDUM89 -10822 622.5 2070 VGH -11662 622.5 2070 VGH -11662 622.5 2071 VGSIDUM90 -10836 477.5 2071 VGH -11676 477.5 2071 VGH -11674 477.5 2071 VGH -11676 477.5 2071 VGH -11676 477.5 2071 VGSIDUM91 -10850 622.5 2072 PADA4 -11690 622.5 2074 VSSIDUM91 -10850 622.5 2074 VSSIDUM104 -11704 477.5 2075 VSSIDUM104 -11704 477.5 2075 VSSIDUM104 -11704 477.5 2075 VSSIDUM104 -11704 477.5 2075 VSSIDUM105 -11704 477.5 2076 VSSIDUM105 -11704 477.5 2076 VSSIDUM105 -11704 477.5 2076 VSSIDUM105 -11704 477.5 2076 VSSIDUM104 -11704 477.5 2076 VSSIDUM105 -11705 622.5 2076 VSSIDUM105 -11706 622.5 2076 VSSIDUM105 -11706 622.5 2076 VSSIDUM105 -11706 622.5 2076 VSSIDUM105 -11706 622.5 2076 VSSIDUM107 -10934	_			l				_				622.5	
1946 S1427					l								477.5
1947 S1428 -9940 477.5 2007 VSSIDUM86 -10780 477.5 2068 VGLO_L -11620 477.5 1948 S1429 -9954 622.5 2008 VSSIDUM87 -10794 622.5 2068 VGLO_L -11634 622.5 1959 S1430 -9968 477.5 2010 VSSIDUM88 -10822 622.5 2070 VGH -11666 477.5 2011 VSSIDUM89 -10826 477.5 2071 VGH -11676 477.5 2073 VGLO_L -10764 477.5 2074 VGLO_L -10784 477.5 2074 VGLO_L -10248 477.5 2074 VGH -10346 622.5 2074 VGH -10346 622.5 2074 VGH -10346 477.5 2074 VGH -10248 477.5 2074 VGH -10248 477.5 2074 VGH -10248 477.5 2074 VGH -10346 622.5 2074 VGH -10346 622.5 2074 VGH -10346 477.5 2074 VGH -10346 477.5 2074 VGH -10346 477.5 2074 VGH -10248 477.5 2074 VGH -10346 477.5 2074 VGH -10248 477.5 2074 VGH -10346 477.5 2074 VGH -10248 477.5 2074 VGH -10248 477.5 2074 VGH -10346 477.5 2074 VGH -10248 477.5 2074 VGH -10248 477.5 2074 VGH -10248 477.5 2074 VGH -10248 477.5 2074 VGH -10346	-				l				_				622.5
1948 S1429	-				l				—		_		477.5
1949 S1430					l				_		_		622.5
1950 S1431	-				l				_		_		477.5
1951 S1432					l				_				622.5
1952 S1433					l				_				477.5
1953 S1434	-				l				_				622.5
1954 S1435 -10038 622.5 2014 VSSIDUM93 -10878 622.5 2074 VSSIDUM104 -11718 622 622.5 2015 VSSIDUM94 -10892 477.5 2075 VSSIDUM105 -11732 477.5 2016 VSSIDUM95 -10906 622.5 2076 VSSIDUM106 -11760 622.5 2016 VSSIDUM95 -10906 622.5 2076 VSSIDUM106 -11760 622.5 2018 VSSIDUM96 -10920 477.5 2018 VSSIDUM96 -10920 477.5 2018 VSSIDUM96 -10920 477.5 2018 VSSIDUM96 -10920 477.5 2018 VSSIDUM98 -10948 477.5 2019 VSSIDUM98 -10948 477.5 2019 VSSIDUM99 -10962 622.5 2020 VSSIDUM99 -10962 622.5 2020 VSSIDUM99 -10962 622.5 2020 VSSIDUM99 -10962 622.5 2020 VSSIDUM100 -10976 477.5 2021 VSSIDUM100 -10976 477.5 2022 VSSIDUM100 -10976 477.5 2023 VSSIDUM100 -10976 477.5 2024 VSSIDUM100 -10976 477.5 2025 GOUT17 -11032 477.5 2026 GOUT17 -11032 477.5 2026 GOUT17 -11032 477.5 2026 GOUT18 -11074 622.5 2028 GOUT18 -11074 622.5 2029 GOUT19 -11088 477.5 2029 GOUT20 -11116 477.5 2029 GOUT20 -11116 477.5 2029 GOUT20 -11116 477.5 2029 GOUT20 -11116 477.5 2029 GOUT21 -11144 477.5 2029 GOUT21 -11144 477.5 2029 GOUT22 -11172 477.5 2029 GOUT22 -11172 477.5 2029 GOUT22 -11172 477.5 2029 GOUT22 -11116 622.5 2024 GOUT23 -11124 622.5 2024 GOUT23 -11128 477.5 2025 GOUT23 -11124 622.5 2026 GOUT23 -11128 477.5 2027 GOUT23 -11128 477.5 2027 GOUT24 -11228 47					l —				_				477.5
1955 S1436	-				l —				_				622.5
1957 S1438	1955	S1436	-10052	477.5	2015	VSSIDUM94		477.5	20	75	VSSIDUM105	-11732	477.5
1958 S1439	1956	S1437	-10066	622.5	2016	VSSIDUM95	-10906	622.5	20	76	VSSIDUM106	-11760	622.5
1959 S1440	1957	S1438	-10080	477.5	2017	VSSIDUM96	-10920	477.5	20	77	DUMMY	-11998	622.5
1960 SDUM2	1958	S1439	-10094	622.5	2018	VSSIDUM97	-10934	622.5	20	78	DUMMY	-12012	477.5
1961 SDUM3	1959	S1440	-10108	477.5	2019	VSSIDUM98	-10948	477.5	20	79	DUMMY	-12026	622.5
1962 VSSIDUM58 -10150 622.5 2022 VSSIDUM101 -10990 622.5 2023 VSSIDUM102 -11004 477.5 2024 VSSIDUM102 -11004 477.5 2024 VSSIDUM103 -11018 622.5 2025 GOUT17 -11032 477.5 2026 GOUT17 -11032 477.5 2026 GOUT17 -11046 622.5 2028 GOUT17 -11046 622.5 2028 GOUT18 -11060 477.5 2028 GOUT18 -11074 622.5 2029 GOUT19 -11088 477.5 2029 GOUT19 -11088 477.5 2029 GOUT19 -11102 622.5 2029 GOUT20 -11116 477.5 2029 GOUT21 -11144 477.5 2029 GOUT21 -11144 477.5 2029 GOUT22 -11172 477.5 2029 GOUT22 -11172 477.5 2029 GOUT22 -11172 477.5 2029 GOUT23 -11120 477.5 2029 GOUT23 -11124 622.5 2029 GOUT24 -11228 477.5 2029 GOUT2	1960	SDUM2	-10122	622.5	2020	VSSIDUM99	-10962	622.5	20	80	DUMMY	-12040	477.5
1963 VSSIDUM59 -10164 477.5 1964 VGLO_L -10178 622.5 2024 VSSIDUM102 -11004 477.5 2025 GOUT17 -11032 477.5 2026 GOUT17 -11032 477.5 2026 GOUT17 -11046 622.5 2027 GOUT18 -11060 477.5 2028 GOUT18 -11060 477.5 2028 GOUT18 -11060 477.5 2028 GOUT18 -11074 622.5 2029 GOUT19 -11088 477.5 2029 GOUT19 -11088 477.5 2029 GOUT19 -11102 622.5 2029 GOUT19 -11104 477.5 2028 GOUT20 -11116 477.5 2028 GOUT20 -11116 477.5 2028 GOUT21 -11144 477.5 2028 GOUT22 -11172 477.5 2028 GOUT22 -11172 477.5 2029 GOUT23 -11120 477.5 2029 GOUT23 -11200 477.5 2029 GOUT23 -11214 622.5 2029 GOUT23 -11214 622.5 2029 GOUT24 -11228 477.5 2029 GOUT34 -11228	1961	SDUM3	-10136	477.5	2021	VSSIDUM100	-10976	477.5	20	81	DUMMY	-12054	622.5
1964 VGLO_L	1962	VSSIDUM58	-10150	622.5	2022	VSSIDUM101	-10990	622.5					
1965 VGLO_L	1963	VSSIDUM59	-10164	477.5	2023	VSSIDUM102	-11004	477.5					
1966 VGLO_L -10206 622.5 2026 GOUT17 -11046 622.5 2027 GOUT18 -11060 477.5 2028 GOUT18 -11074 622.5 2029 GOUT19 -11088 477.5 2029 GOUT19 -11088 477.5 2029 GOUT19 -11102 622.5 2029 GOUT20 -11110 477.5 2030 GOUT20 -11110 477.5 2031 GOUT20 -11110 477.5 2032 GOUT20 -11130 622.5 2033 GOUT21 -11144 477.5 2034 GOUT21 -11158 622.5 2034 GOUT22 -11172 477.5 2035 GOUT22 -11172 477.5 2036 GOUT22 -11186 622.5 2037 GOUT23 -11200 477.5 2038 GOUT23 -11210 477.5 2038 GOUT23 -11210 477.5 2038 GOUT23 -11214 622.5 2039 GOUT24 -11228 477.5 1964	VGLO_L	-10178	622.5	2024	VSSIDUM103	-11018	622.5						
1967 VGLO_L -10220 477.5 1968 VGLO_L -10234 622.5 1969 VGLO_L -10248 477.5 1970 VGLO_L -10262 622.5 1971 VGLO_L -10276 477.5 1972 VGLO_L -10290 622.5 1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -10332 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10360 477.5 1978 VGH -10360 477.5 1979 VGH -10388 477.5 </td <td>1965</td> <td>VGLO_L</td> <td>-10192</td> <td>477.5</td> <td>2025</td> <td>GOUT17</td> <td>-11032</td> <td>477.5</td> <td>A</td> <td>llig</td> <td>nment Mark</td> <td>X-axis</td> <td>Y-axis</td>	1965	VGLO_L	-10192	477.5	2025	GOUT17	-11032	477.5	A	llig	nment Mark	X-axis	Y-axis
1968 VGLO_L -10234 622.5 1969 VGLO_L -10248 477.5 1970 VGLO_L -10262 622.5 1971 VGLO_L -10276 477.5 1972 VGLO_L -10290 622.5 1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -10324 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10360 477.5 1978 VGH -10388 477.5 1979 VGH -10388 477.5 2038 GOUT23 -11172 477.5 2036 GOUT22 -11186 622.5 2037 GOUT23 -11200 477.5 2038 GOUT24 -1128 477.5	1966	VGLO_L	-10206	622.5	2026	GOUT17	-11046	622.5				11870	605
1969 VGLO_L -10248 477.5 1970 VGLO_L -10262 622.5 1971 VGLO_L -10276 477.5 1972 VGLO_L -10290 622.5 1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -10322 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 1979 VGH -10388 477.5 2039 GOUT24 -11186 622.5 2031 GOUT20 -11110 477.5 2032 GOUT21 -11144 477.5 2034 GOUT21 -11158 622.5 2035 GOUT22 -11172 477.5 2036 GOUT22 -11186 622.5 2037 GOUT23 -11200 477.5 2038 GOUT23 -11214 622.5 2039 GOUT24 -11228 477.5	1967	VGLO_L	-10220	477.5	2027	GOUT18	-11060	477.5		ΑL	MART_L_T	-11870	605
1970 VGLO_L -10262 622.5 1971 VGLO_L -10276 477.5 1972 VGLO_L -10290 622.5 1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -10324 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 2038 GOUT24 -111102 622.5 2037 GOUT25 -11172 477.5 2038 GOUT22 -11186 622.5 2037 GOUT23 -11200 477.5 2038 GOUT24 -1128 477.5	1968	VGLO_L	-10234	622.5	2028	GOUT18	-11074	622.5					
1971 VGLO_L -10276 477.5 1972 VGLO_L -10290 622.5 1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -10324 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 2038 GOUT23 -11172 477.5 2037 GOUT23 -11200 477.5 2038 GOUT23 -11214 622.5 2037 GOUT23 -11214 622.5 2038 GOUT24 -11228 477.5	1969	VGLO_L	-10248	477.5	2029	GOUT19	-11088	477.5					
1972 VGLO_L -10290 622.5 1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -1032 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10374 622.5 1979 VGH -10388 477.5 2038 GOUT23 -11200 477.5 2038 GOUT23 -11214 622.5 2038 GOUT23 -11214 622.5 2039 GOUT24 -11228 477.5					l								
1973 VGH -10304 477.5 1974 VGH -10318 622.5 1975 VGH -10332 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 2038 GOUT22 -11172 477.5 2037 GOUT23 -11200 477.5 2038 GOUT23 -11214 622.5 1979 VGH -10388 477.5 2039 GOUT24 -11228 477.5 477.5			-10276	477.5				477.5					
1974 VGH -10318 622.5 1975 VGH -10332 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 2038 GOUT22 -11120 477.5 2037 GOUT23 -11200 477.5 2038 GOUT23 -11214 622.5 2039 GOUT24 -1128 477.5													
1975 VGH -10332 477.5 1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 2037 GOUT23 -11200 477.5 2038 GOUT23 -11214 622.5 2039 GOUT24 -11228 477.5	-												
1976 VGH -10346 622.5 1977 VGH -10360 477.5 1978 VGH -10374 622.5 1979 VGH -10388 477.5 2038 GOUT23 -11214 622.5 2038 GOUT24 -11228 477.5	_				l								
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1980 VGH		l .	-10402	622.5			-11242	622.5	L				

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System Interface

3.7. DBI Type B Parallel Interface

The ILI9806 supports an 8-/9-/16-/18-/24-bit MPU DBI Type B parallel interface. The chip-select CSX (active low) is used to enable or disable the ILI9806 chip. The RESX (active low) is an external reset signal, the WRX is parallel data write strobe, the RDX is parallel data read strobe, and DB [23:0] is parallel data bus.

The ILI9806 latches the input data at the rising edge of the WRX signal. The DCX is the signal for data/command selection. When DCX = 1, DB [23:0] bits are RAM data or command parameters. When DCX = 0, DB [23:0] bits are commands. The DBI Type B bi-directional interface is used for communication between the MPU controller and LCD driver chip. The selection of the parallel interface is shown in Table 8.

Table 8: DBI Type B Parallel Interface

IM3	IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	DCX	Function
						"H"	"L"	Write command code.
0	0	0	0	DBI Type B	"H"		"H"	Read internal status.
U	U	U	U	8-bit bus interface		"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.
						"H"	"L"	Write command code.
0	0	0	1	DBI Type B	"H"	J	"H"	Read internal status.
0	U	U	ı	16-bit bus interface		"H"	"H"	Write parameter or display data.
					"H"	J	"H"	Reads parameter or display data.
						"H"	"L"	Write command code.
0	0	1	0	DBI Type B	"H"	J	"H"	Read internal status.
0	U	'	U	24-bit bus interface		"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.
						"H"	"L"	Write command code.
1	1	0	0	DBI Type B	"H"		"H"	Read internal status.
	1	U	U	9-bit bus interface		"H"	"H"	Write parameter or display data.
					"H"	ſ	"H"	Reads parameter or display data.
						"H"	"L"	Write command code.
1	1	0	1	DBI Type B	"H"	J	"H"	Read internal status.
	'	U	1	18-bit bus interface		"H"	"H"	Write parameter or display data.
					"H"		"H"	Reads parameter or display data.

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3.7.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information while the display module captures the information from the host processor on the rising edge of the WRX. When the DCX signal is driven to low level, the input data on the interface is interpreted as command information. The DCX signal can also be pulled to high level when the data is RAM data or command parameter.

Figure 2 shows the write cycle of the DBI Type B interface.

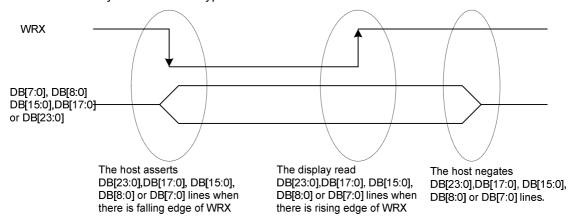


Figure 2: DBI Type B Write Cycle Note

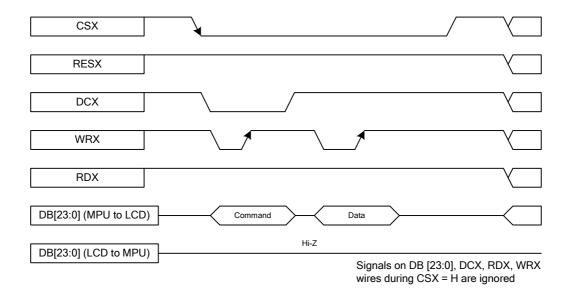


Figure 3: DBI Type B Write Cycle Sequence

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Note WRX is an unsynchronized signal, which can be terminated when not in use.





3.7.2. Read Cycle Sequence

The RDX signal is driven from high to low and then pulled back to high during the read cycle. The display module provides information to the host processor while the host processor reads the display module information on the rising edge of the RDX signal. When the DCX signal is driven to the low level, the input data on the interface is interpreted as internal status or parameter data. The DCX signal also can be pulled to high level when the data on the interface is RAM data or a command parameter data.

The following figure shows a read cycle of the DBI Type B interface.

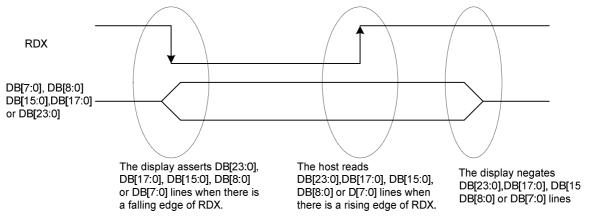


Figure 4: DBI Type B Read Cycle Note 1

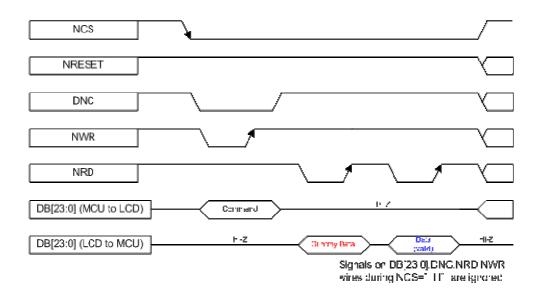


Figure 5: DBI Type B Read Cycle Sequence Note 2

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Note 1 RDX is an unsynchronized signal, which can be terminated when not in use.

Note 2 Read Data is only valid when the DCX input is pulled high. If the DCX signal is driven low during the read cycle then the display information outputs will be High-Z.





3.7.3. DBI Type B Interface Set Table

24-bit data bus DB [23:0] interface, IM [3:0] = 0010



Figure 6: DBI Type B 24-bit Data Bus

18-bit data bus DB [17:0] interface, IM [3:0] = 1101



Figure 7: DBI Type B 18-bit Data Bus

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16-bit data bus DB [15:0] interface, IM [3:0] = 0001



Figure 8: DBI Type B 16-bit Data Bus

9-bit data bus DB [8:0] interface, IM [3:0] = 1100

	ווו נס.טן וווו	.0	400	,	[•	. •]	-													
	Register	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0										
Command/Parameter Write	2Ch / 3Ch		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]										
Command/Parameter Read	2Eh / 3Eh		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]										
					Firs	t Tran	sfer							Seco	nd Tra	nsfer				
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Suppriame Memory White	3'h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]		G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	$\overline{/}$	
																				_
					Firs	t Tran	sfer							Seco	nd Tra	nsfer				
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Soppi rame Memory vvine	3'h6	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	
					Firs	t Tran	sfer							Seco	nd Tra	nsfer				Third Transfer
			_		T															
Ohnn Frama Mamany Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0
9bpp Frame Memory Write	Set_pixel_format 3'h7	DB8	DB7	DB6	DB5 R1[DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5 G1[DB3	DB2	DB1	DB0	DB8 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 B1[7:0]

Figure 9: DBI Type B 9-bit Data Bus

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8-bit data bus DB [7:0] interface, IM [3:0] = 0000

	Register	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

				ļ	First T	ransfe	r					S	econd	Transf	er		
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Supp Frame Memory White		R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

				ŀ	First T	ransfe	r					Se	econd	Transf	er					٦	Third T	ransfe	r		
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
obpp Frame Memory Write	3'h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	/	/	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	$\overline{/}$	/	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	/	

				F	First Tr	ansfe	r					S	econd	Transf	er					Т	hird T	ransfe	r		
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
obpp Frame Welliory White	3'h7				R1[7:0]							G1[7:0]							B1[7	':O]			
Frame Memory Read	*				r1[7	7:0]							g1[7:0]							b1[7:	:0]			

Figure 10: DBI Type B 8-bit Data Bus





3.8. DBI Type C Serial Interface

The selection of this interface is done by the IM [3:0] pins. See Table 9.

Table 9: DBI Type C Serial Interface

IM3	IM2	IM1	IM0	DBI Type C Mode	CSX	SDA	SCL	Function
Х	0	1	1	3-line serial interface	"L"	-	L	Read/Write command, parameter or display data.

The ILI9806 uses a 3-line 9-bit serial interface for communication between the host and the ILI9806. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the DPI interface data transfer, the unused pins are unaffected. The Serial clock (SCL) is used only for the interface with the MPU, so it can be stopped when no communication is necessary.

3.8.1. Write Cycle Sequence

In the Write Mode of the interface, the host writes commands and data to the ILI9806. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is "low", the transmission byte is interpreted as a command byte. If the D/C bit is "high", the transmission byte is stored in the GRAM as display data, or stored in the command register as a parameter data.

Any instruction can be sent in any order to the ILI9806 and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See below for the detail of data format for 3-line serial interface.

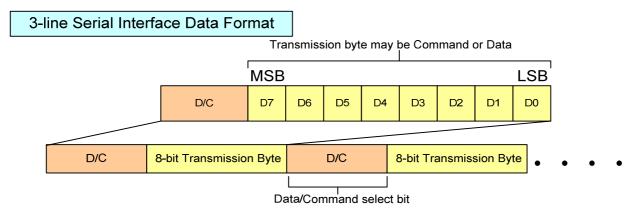


Figure 11: DBI Type C Data Format

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The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the ILI9806 on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences as described in the Figure 12 below.

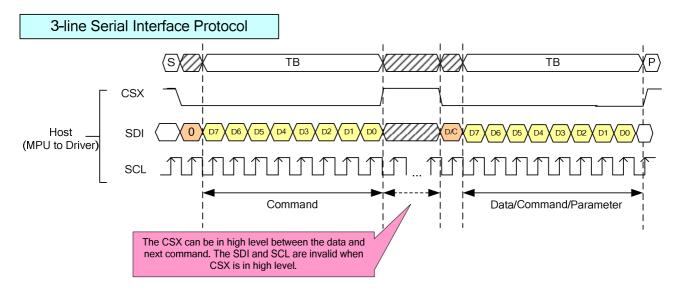


Figure 12: DBI Type C Protocol

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3.8.2. Read Cycle Sequence

In the Read Mode of the interface, the host reads the register value from the ILI9806. The host sends a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ILI9806 samples the SDI (input data) at the rising edge of the SCL (serial clock), and shifts SDO (output data) at the falling edge of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

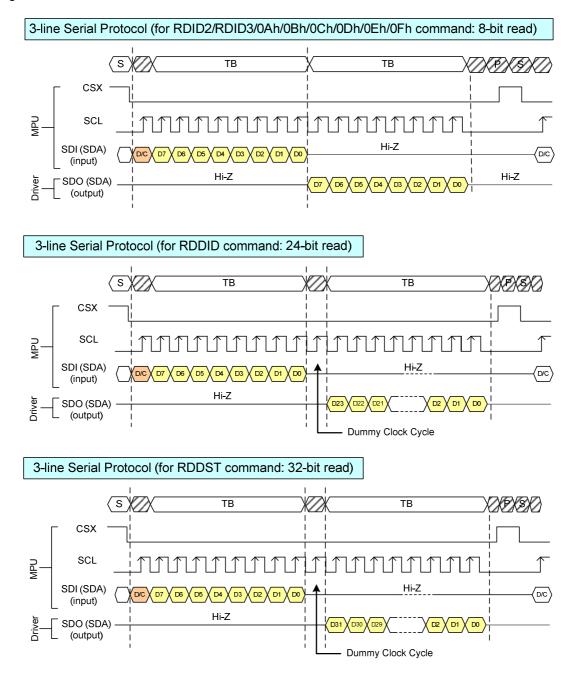


Figure 13: DBI Type C Read Cycle Sequence

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3.9. Data Transfer Break and Recovery

If data transmission is interrupted by the CSX pulse while transferring a Command, Frame Memory data or multiple parameter command before Bit D0 of the byte has been completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is activated again.

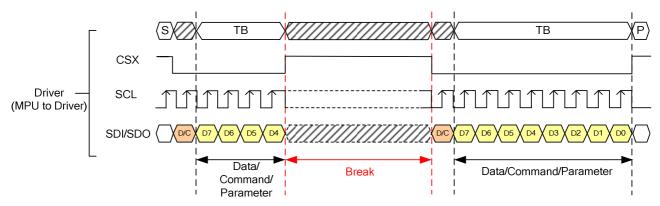


Figure 14: Data Transfer Break and Recovery

If there is a break when transmitting a command with multiple parameters and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below.

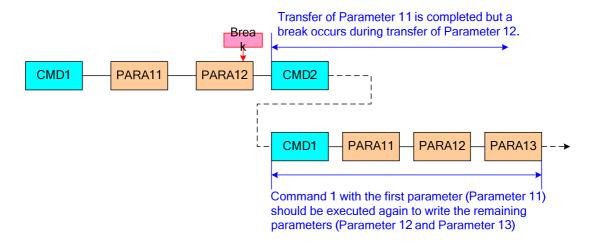


Figure 15: Data Transfer Break - Case 1

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If a command with multiple parameters is sent and a break occurs when a new command is sent before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command remain at the previous value.

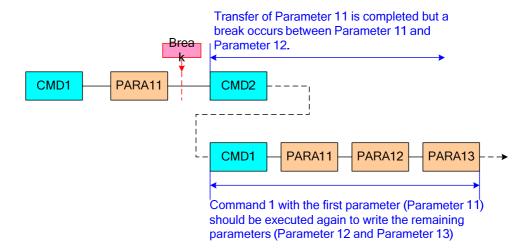


Figure 16: Data Transfer Break - Case 2

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3.10. Data Transfer Pause

Transferring a Command, Frame Memory Data, or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ILI9806 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

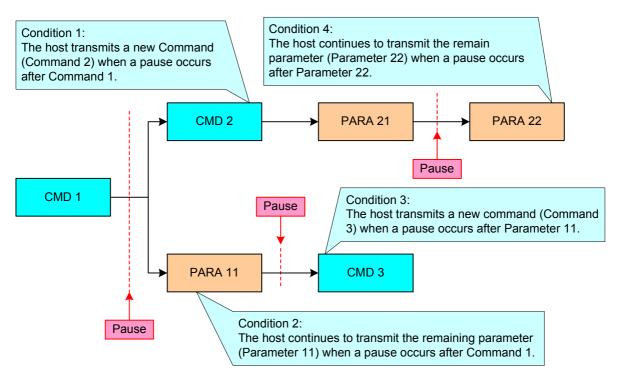


Figure 17: Data Transfer Pause

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3.10.1. Serial Interface Pause

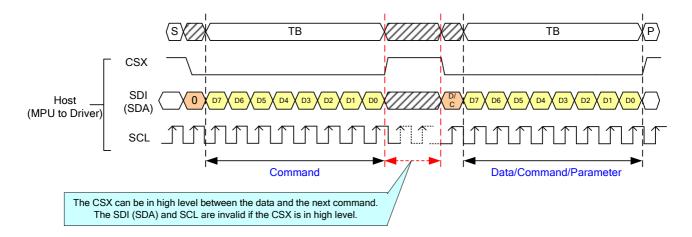


Figure 18: DBI Type C Data Transfer Pause

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

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3.10.2. Parallel Interface Pause

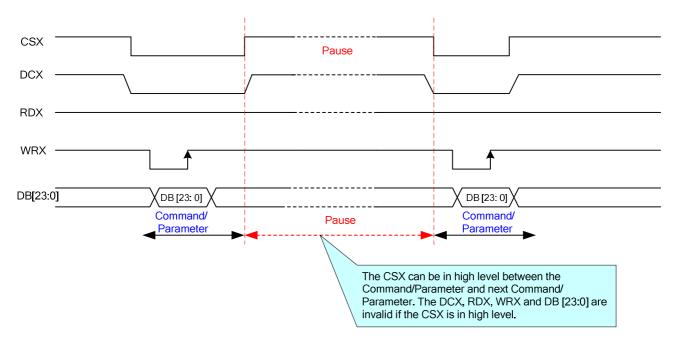


Figure 19: DBI Type B Data Transfer Pause

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

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3.10.3. Data Transfer Mode

The ILI9806 provides five different types of color depth: 8-bit/per pixel, 9-bit/per pixel, 16-bit/per pixel, 18-bit/per pixel, and 24-bit/pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods^{Note}.

3.10.4. Method 1

The Image data is sent to the Frame Memory in the successive Frame writing, each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and the next Frame is written.

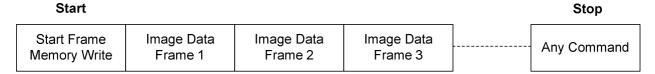


Figure 20: Data Transfer Mode - Method 1

3.10.5. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop the Frame Memory Writing. Then Start Memory Write command is sent, and a new Frame is downloaded.

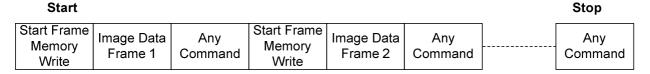


Figure 21: Data Transfer Mode - Method 2

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Note 1. These apply to all five kinds of color depth on both serial and parallel interfaces.

^{2.} The Frame Memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the Frame Memory.





3.11. DPI (RGB) Interface

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

BPGRAM	Display data path
0	Write into Memory

RM	Interface for RAM access
0	System interface
1	RGB interface

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DCK cannot be stopped unless it enters the Sleep In mode.

DM	RGB interface operating clock selection
0	Internal system clock
1	RGB interface DCK (Dot clock)

3.11.1. DPI Interface Selection

The DPI interface is operated with VSYNC, HSYNC, ENABLE, DCK, and DB [23:0] lines. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in the Table 10 and Figure 22.

Table 10: DPI Interface Selection

	DPI [2:0]	DPI (RGB) Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VSYNC, HSYNC, ENABLE, DB [20:16] , DB [13:8], DB [4:0]
1	1	0	18-bit RGB interface	VSYNC, HSYNC, ENABLE, DB [21:16] , DB [13:8], DB [5:0]
1	1	1	24-bit RGB interface	VSYNC, HSYNC, ENABLE, DB [23:0]
	Other			Setting prohibited

16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5

DB2	23 DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]				B[4]	B[3]	B[2]	B[1]	B[0]

18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		R[5]	R4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7

												-	-										
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	R[6]	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 22: DPI Interface 16/18/24-bit Pixel Format Selection

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The Pixel clock (DCK) runs all the time without stop, and it is used to enter VSYNC, HSYNC, ENABLE, and DB [23:0] states when there is a rising edge of the DCK. The DCK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is a low enable and its state is read to the display module by the rising edge of the DCK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is a low enable and its state is read to the display module by the rising edge of the DCK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred to the display is received. This is a high enable and its state is read to the display module by the rising edge of the DCK signal. DB [23:0] are used to indicate what is the information of the image that is transferred to the display (when ENABLE = 0 (low) and there is a rising edge of DCK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by the rising edge of the DCK signal. In RGB interface modes, the input display data is written to the GRAM first then outputs the corresponding source voltage according to the gray data from the GRAM.

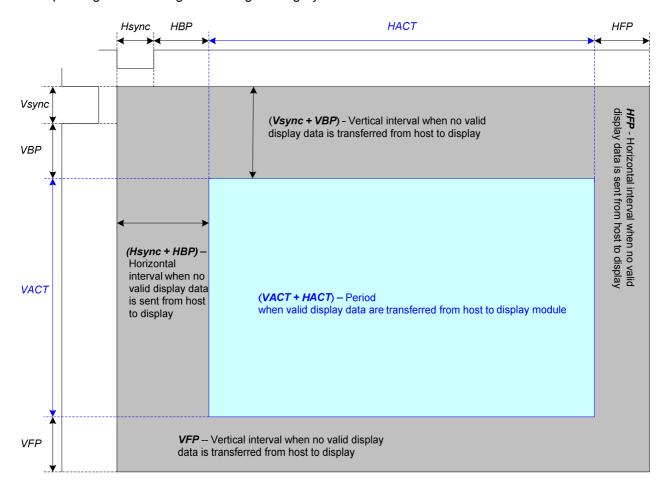


Figure 23: General DPI Timing Diagram

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3.11.2. DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI interface mode is illustrated in Figure 24.

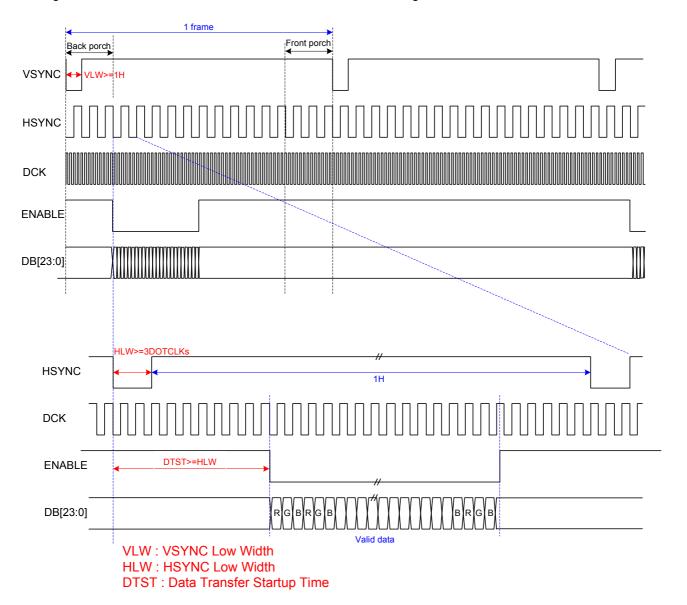


Figure 24: DPI Interface Timing diagram Note

 $^{^{}Note}$ VSPL = 0, HSPL = 0, DPL = 0, and EPL = 0 of Interface Mode Control B0h command.





3.12. DSI System Interface

3.12.1. General Description

The MIPI DSI is enabled or disabled by the external IM [3:0] pin.

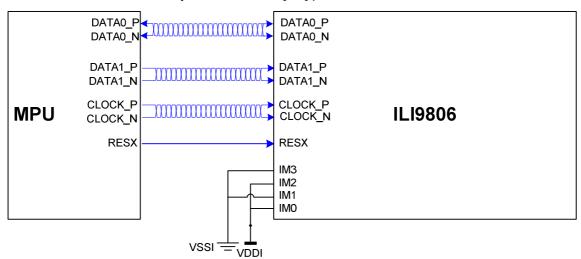


Figure 25: DSI System Interface Diagram

IM	13	IM2	IM1	IM0	MPU Interface	Data Pin in Use
O)	1	0	1	DSI interface	DSI_CP, DSI_CN DSI_D0P, DSI_D0N DSI_D1P, DSI_D1N

The communication is separated into two different levels between the MPU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

3.12.2. Interface Level Communication

3.12.3. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to the Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when information is to be transferred from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 11: High Speed and Low-Power Lane Pair State Codes

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Lane Pair State Code	Line DC Vo	Itage Levels	High Speed (HS)	Low F	Power
Lane Fall State Code	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

3.12.4. DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM), or High Speed Clock Mode (HSCM). Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Likewise, clock lanes are in the single ended mode (LP = Low Power) when entering in or leaving the High Speed Clock Mode (HSCM). These entering and leaving protocols use clock lanes in the single ended mode to generate an entering or leaving sequence.

The principal flow chart of the different power modes of clock lanes is illustrated below.

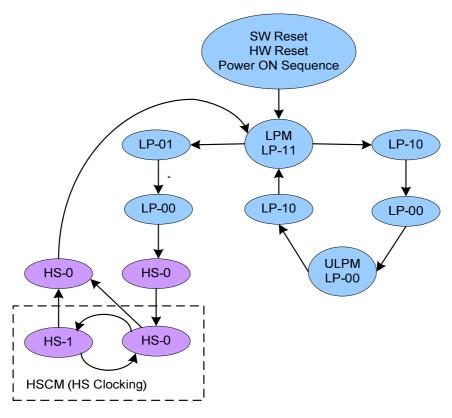


Figure 26: Power Modes of Clock Lanes

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Note 1 Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.

Note 2 If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, the lane pair returns to the LP-11 of the Control Mode.





3.12.5. Low Power Mode (LPM)

When DSI-CLK lanes enter the LP-11 State Code, DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM) in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence => LP-11
- 2) After DSI-CLK+/- lanes leave the Ultra Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM) The sequence is illustrated below.

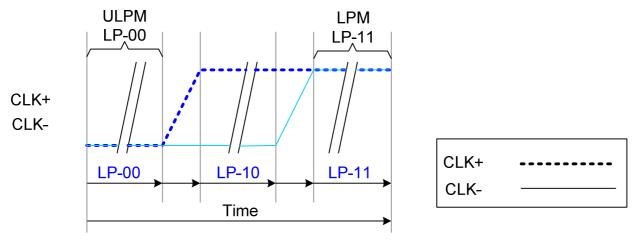


Figure 27: From ULPM to LPM

3) After DSI-CLK+/- lanes leave the High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0 => LP-11 (LPM). The sequence is illustrated below.

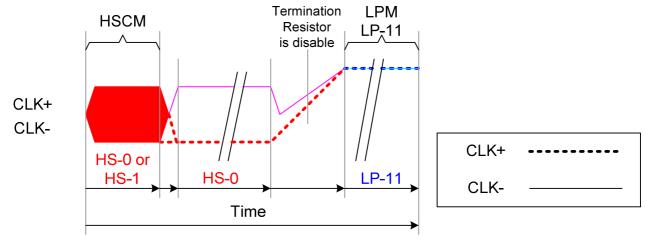


Figure 28: From High Speed Clock Mode (HSCM) to LPM

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All the changes of the three modes are illustrated in the flow chart below.

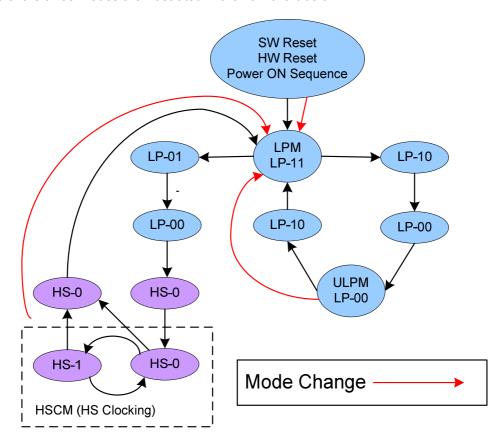


Figure 29: All the Changes of the Three Modes to the LPM

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3.12.6. Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM) when DSI-CLK lanes enter the LP-00 State Code. The only possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). The sequence is illustrated below.

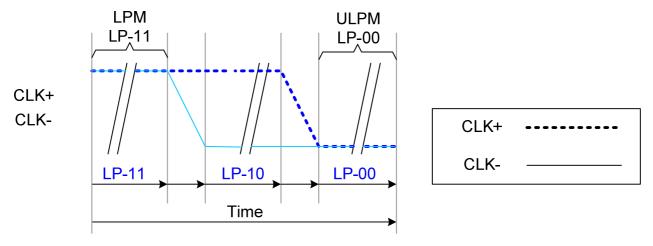


Figure 30: From LPM to ULPM

The mode change is illustrated below.

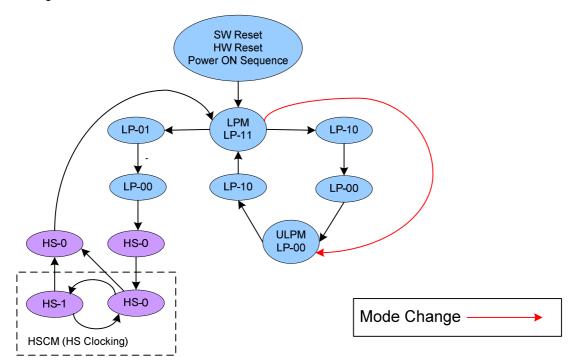


Figure 31: Mode Change from LPM to ULPM

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3.12.7. High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM) when DSI-CLK lanes start to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). The sequence is illustrated below.

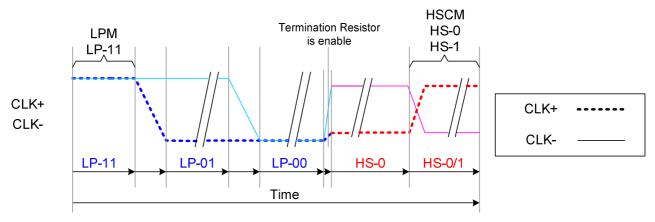


Figure 32: From LPM to HSCM

The mode change is illustrated below.

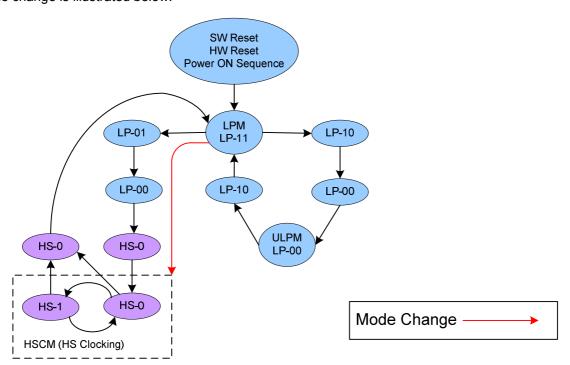


Figure 33: Mode Change from LPM to HSCM

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The high speed clock (DSI-CLK+/-) starts before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

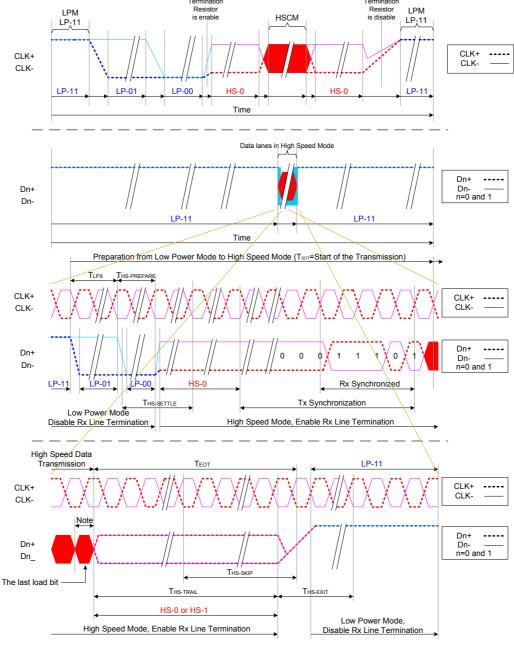


Figure 34: High Speed Clock Burst^{Note}

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 $^{^{\}it Note}$ 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

^{2.} If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.





3.12.8. DSI-D1 and DSI-D0 Data Lanes

3.12.9. General

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven to different modes:

- Escape Mode (only DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)
- Bus Turnaround Request (only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined in the following table.

Table 12: Entering and Leaving Sequences^{Note}

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

3.12.10. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode.

These Escape Modes are used to:

- Send "Low-Power Data Transmission" (LPDT) from the MPU to the display module,
- Drive data lanes to "Ultra-Low Power State" (ULPS),
- Indicate "Remote Application Reset" (RAR), which can reset the display module,
- Indicate "Tearing Effect" (TEE), which is used to transmit a TE line event from the display module to the MPU,
- Indicate "Acknowledge" (ACK), which is used to transmit a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded when one of the data lanes changes from low-to-high-to-low, then this changed data lane presents the value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0). For example, when DSI-D0- changes from low-to-high-to-low, the receiver latches a data bit, which value is the logical 0. The receiver uses this low-to-high-to-low transition for its internal clock.
- · A load if necessary
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

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Note 1. DSI-D1+/- and DSI-D0+/- data lanes are used.

^{2.} See more information in the chapter of Bus Turnaround.



This basic construction is illustrated below:

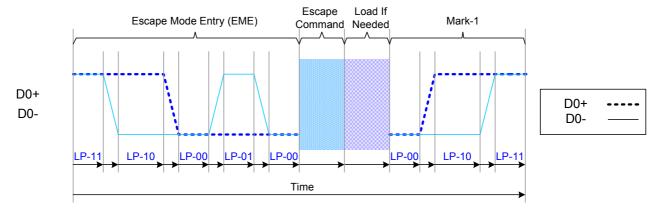


Figure 35: General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as described in Table 13: Escape Commands.

An example of a Mode type Escape Command is Ultra-Low Power Mode, where the MPU instructs the display module to enter its Ultra-Low Power Mode.

An example of a Trigger type Escape Command is Tearing Effect. In this case, the MPU has already instructed the display module to provide this trigger and is waiting for a response. The display module then sends a TE trigger (TEE) on the next V-sync event.

Escape commands are defined in the table below.

Table 13: Escape Commands Note

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	1	Х
Ultra-Low Power Mode	Mode	0001 1110 b	Х	Х
Undefined-1, Note 1	Mode	1001 1111 b	1	-
Undefined-2, Note 1	Mode	1101 1110 b	1	ı
Remote Application Reset	Trigger	0110 0010 b	-	X
Tearing Effect	Trigger	0101 1101 b	-	X
Acknowledge	Trigger	0010 0001 b	-	Χ
Uknown-5, Note 1	Trigger	1010 0000 b	-	-

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^{Note} 1. This Escape command is not implemented in the display module.

^{2.} n = 1

^{3.} x = Supported

^{4. - =} Not Supported