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ILI9806

a-Si TFT LCD Single-Chip Driver
480(RGB) x 864 Resolution
16.7M-color with Internal GRAM

Specification
Preliminary

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ILI TECHNOLOGY CORP.
8F, No. 38, Taiyuan St, Jhubei City,
Taiwan 302, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600585
http://www.ilitek.com

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1. Introduction

The ILI9806 is a 16.7M single-chip SOC driver for a-Si TFT liquid crystal display panels with a resolution of up to 480 (RGB) x 864 memory size. The ILI9806 is comprised of a 1440-channel source driver, a gate-IC-less level shifter, a 1,244,160-byte GRAM for graphic data of 480 (RGB) x 864 dots, and a power supply circuit.

The ILI9806 supports parallel MPU 8-/9-/16-/18-/24-bit data bus interfaces and a 3-line serial peripheral interface to input commands. The ILI9806 supports a RGB (16-/18-/24-bit) data bus for video image display. For high-speed serial interface, the MIPI DSI and MDDI (Mobile Display Digital Interface) interface mode, the ILI9806 supports two data lanes and one clock lane for high-speed and low power transmission in both directions with low EMI noise.

The ILI9806 operates with a wide range of an analog power supply. The ILI9806 supports 8-color display, sleep mode and deep standby power management functions, ideal for medium or small size portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players, and similar devices with color graphics display. Additionally, it has an internal DC/DC converter that generates the LCD driving voltage and the voltage follower circuit for LCD driver.

2. Features

- Display resolution options:
  - 480 (RGB) (H) x 864 (V) with GRAM
  - 480 (RGB) (H) x 854 (V) with GRAM
  - 480 (RGB) (H) x 800 (V) with GRAM
  - 480 (RGB) (H) x 720 (V) with GRAM
  - 480 (RGB) (H) x 640 (V) with GRAM

- Display color modes
  - Full color mode:

    16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
  - Reduced color modes:

    262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)

    65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)

    8 colors (Idle Mode On): 8 colors (3-bit data, R: 1-bit, G: 1-bit, B: 1-bit)

- Display module:
  - On-chip Frame Memory size 1,244,160 bytes, 480 (RGB) (H) x 864 (V) x 24 bits
  - Supports 1440 source channel outputs
  - Supports gate control signals to gate driver in the panel
  - Supports 1-dot/2-dot/3-dot/4-dot/column/Zigzag inversion
  - Gamma correction (1 preset Gamma curve)
  - On module VCOM control (VCL+0.2V to 0V common electrode output voltage range)

- Display interface types:
  - MPU mode:

    MIPI-DBI Type B (Display Bus Interface, 80 System) interface, 8/9/16/18/24-bit bus

    MIPI-DBI Type C (Serial data transfer interface, 3-line SPI) interface
  - MIPI-DSI (Display Serial Interface) interface:

    Supports one data lane/maximum speed 850Mbps or

    Supports two data lanes/maximum speed 500Mbps

    Supports DSI version 1.01.00

    Supports D-PHY version 1.00.00

    Supports DCS version 1.02.00
  - MDDI (Mobile Display Serial Interface):

    Supports one data lane/maximum speed 800Mbps or

    Supports two data lanes/maximum speed 400Mbps

    Supports MDDI V1.2 1 strobe
  - MIPI-DPI (Display Pixel Interface) interface:

    16 bit/pixel (R: 5-bit, G: 6-bit, B: 5-bit)

    18 bit/pixel (R: 6-bit, G: 6-bit, B: 6-bit)

    24 bit/pixel (R: 8-bit, G: 8-bit, B: 8-bit)

- Power saving modes:
  - Deep-standby mode
  - Sleep mode

- Other on-chip functions/Miscellaneous
  - Supports inversion mode
  - Software programmable color depth mode
  - Oscillator for display clock generation
  - Supports DC VCOM driving
  - DC VCOM voltage generator and adjustment
  - OTP (One-Time Programming) memory store initialization register settings
  - Provide 3 times to store DC VCOM value setting, ID setting
  - Supports CABC (Content Adaptive Brightness Control) function
  - Supports 3-Gamma DGC (Digital Gamma Correction) function
  - Color enhancement function
  - DC/DC converter
  - VGH/VGLO voltage generator for gate control signal in panel
  - Supports gate control signals to gate driver in panel (GIP)

- Input power:
  - I/O supply voltage range for VDDI to VSSI = 1.65V ~ 3.3V (VDDI)
  - Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR = 2.5V ~ 3.3V
  - MIPI/MDDI regulator range for VDDAM to VSSAM = 2.5V ~ 3.3V
  - OTP programming voltage, VPP = 7.5V

- Source/VCOM/Gate power supply voltage:
  - AVDD-AVSS = 4.75 to 6.5V (Step-up 1 output voltage range)
  - AVEE-AVSS = -6.5 to -4.75V (Step-up 2 output voltage range)
  - VCL-GND = -VCI to -1.8V (Step-up 3 output voltage range)
  - DC VCOM = VCL+0.2V to 0V, a step 12.5mV (Common electrode voltage range)
  - VGMP = 3.0V to 6.1875V (AVDD-0.3V) (Positive gamma high voltage range)
  - VGSP = 0.0V to 3.475V (Positive gamma low voltage range)
  - VGMN = -3.0V to -6.1875V (AVEE+0.3V) (Negative gamma high voltage range)
  - VGSN = 0.0V to -3.475V (Negative gamma low voltage range)
  - VGH-AVSS = 12V to 20V (Positive gate driver output voltage range)
  - VGL-AVSS = -7V to -15V (Negative gate driver output voltage range)
  - LVGL-AVSS = -7V to -15V (Negative gate driver output voltage range)
  - VRGH = 1.0V ~ 6.0V (AVDD-0.3V) (Panel voltage range)

3. Device Overview

3.1. Block Diagram

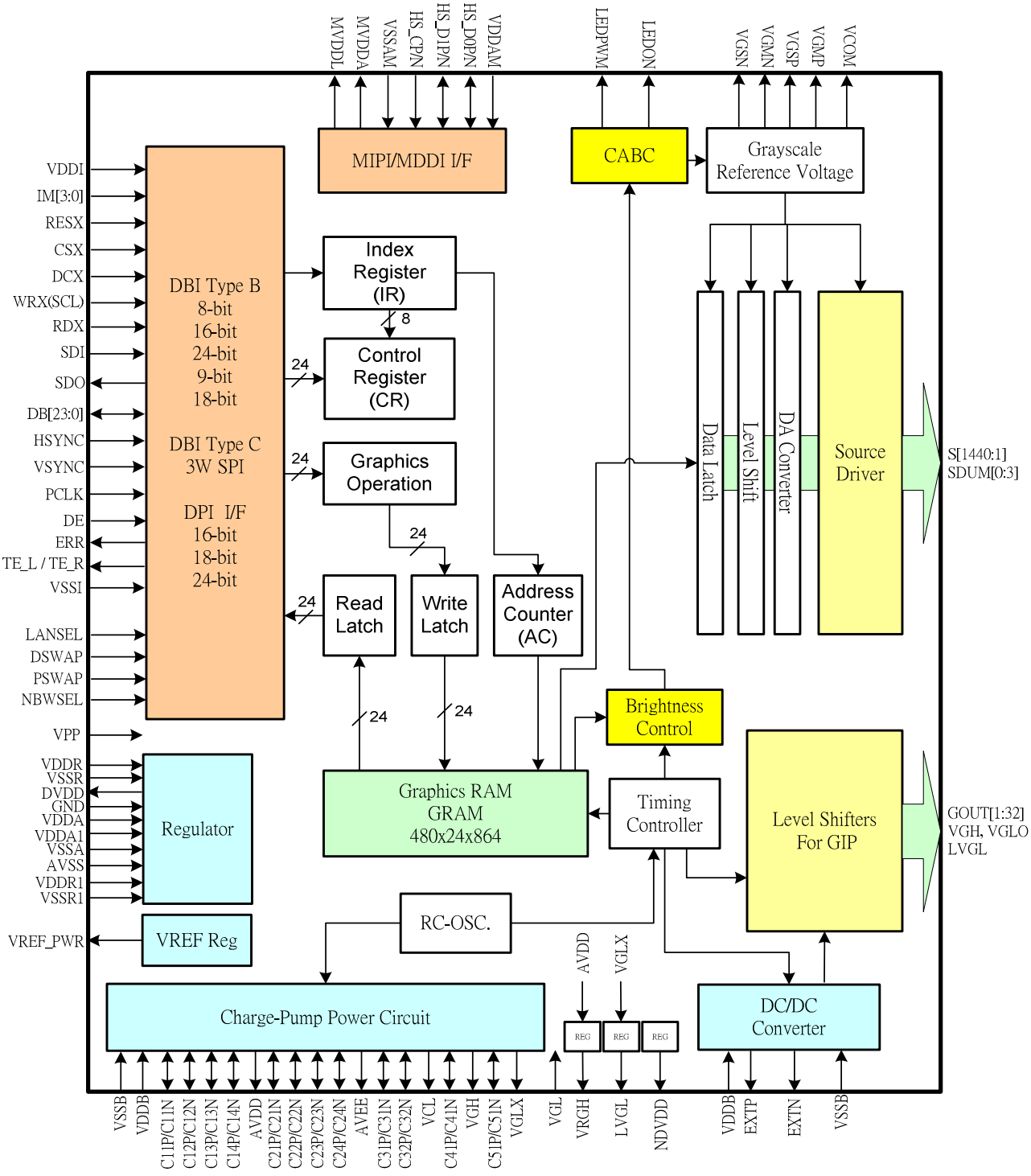


Figure 1: Block Diagram

3.2. Block Function Description

3.2.1. System Interface

The interface operating mode (DBI, DPI or DSI) is selected by hardware pins IM [3:0], as shown in Table 1 below.

Table 1: System Operating Mode [Note 1]

IM3	IM2	IM1	IM0	Interface	IO Pin in Use
0	0	0	0	DBI Type B 8-bit bus interface	DB [7:0], WRX, RDX, CSX, DCX
0	0	0	1	DBI Type B 16-bit bus interface	DB [15:0], WRX, RDX, CSX, DCX
0	0	1	0	DBI Type B 24-bit bus interface	DB [23:0], WRX, RDX, CSX, DCX
1	1	0	0	DBI Type B 9-bit bus interface	DB [8:0], WRX, RDX, CSX, DCX
1	1	0	1	DBI Type B 18-bit bus interface	DB [17:0], WRX, RDX, CSX, DCX
X	0	1	1	DPI with DBI Type C 3-line 9-bit	DB [23:0], SDI, SDO, SCL, CSX
0	1	0	1	MIPI DSI Interface	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN
0	1	1	0	MDDI Interface	HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN

3.2.2. Parallel RGB Interface

The RGB interface is used as the external interface for displaying moving pictures. When the RGB interface is selected, display operations are synchronized with the externally supplied signals, VSYNC, HSYNC, and PCLK. In the RGB interface mode, data (DB23-0) are written in synchronization with these signals according to the polarity of the Enable Signal (DE). This is done in order to prevent flicker on the display while updating display data.

The RGB interface allows transferring data only when updating the frames of a moving picture by writing all display data to the internal RAM. This method is a contributing factor for the low power requirement of moving picture display.

The ILI9806 includes an IR (index register) which stores the index data of internal control register and GRAM. When DCX = L, the command is written into the driver IC via the DBI interface. When DCX = H, GRAM data via the R2Ch register is written through the data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading display data from the GRAM.

Note 1 Set Number of colors using set pixel format: 3Ah.

3.2.3. Address Counter (AC)

The address counter (AC) assigns an address for writing pixel data to the GRAM, or for reading pixel data from the GRAM. Each time a pixel data is written into the GRAM, the X address or Y address of the AC is automatically increased by 1 (or decreased by 1), as determined by the register setting (MV, MX and MY bit). To simplify the address control of the GRAM access, the window address function allows writing data only to a window area of the GRAM specified by Column and Row address registers. After data is written to the GRAM, the AC will be increased or decreased within the setting window address range specified by the Column address register (start: SC, end: EC) and the Row address register (start: SP, end: EP). The window address function enables writing data only in the rectangular area set by users on the GRAM.

3.2.4. Graphic RAM (GRAM)

GRAM is the graphic RAM storing bit-pattern data of 1,244,160 bytes with 24 bits per pixel, enabling a maximum of 480(RGB) x 864 dots graphic display.

3.2.5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates the LCD drive voltage which corresponds to 256 grayscale level set in the Gamma correction register. The ILI9806 can display up to 16.7M colors at maximum.

3.2.6. Timing Generating

The timing generator is used to generate timing signals for operating internal circuits. The timing generator generates timing signals for internal circuits, such as the internal GRAM. Timing for display operations (such as RAM read operation) and timing for internal operations (such as RAM access by the MPU) are outputted separately so that they do not interfere with each other.

3.2.7. Oscillator

The ILI9806 incorporates with an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.8. Source Driver Circuit

The LCD display driver circuit consists of a 480-output source driver (S1~S1440). The display pattern data is latched when 480RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.9. Panel Control Circuit

The panel control circuit outputs GOUT [1:32] signals at either the VGH or VGLO or AVDD level.

3.2.10. Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to the register setting.

3.2.11. MIPI DSI Controller Circuit

The MIPI DSI controller circuit consists of the D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer and analog transceiver. The D-PHY controls communication with the analog block, and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams, and the PPU controls transmitting packet distribution and merging. The internal data and command buffer is used for temporary storage of incoming commands and display data.

3.2.12. MDDI

The ILI9806 supports MDDI as a differential small amplitude serial interface for high-speed data transfer.

3.2.13. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

3.3. Pin Descriptions

Table 2: Bus Interface Pins

<table>
<tr><th colspan="3">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>IM [3:0]</td><td>I</td><td>- Select the interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>DBI Type B 8-bit</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>DBI Type B 16-bit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>DBI Type B 24-bit</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>DBI Type B 9-bit</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>DBI Type B 18-bit</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>1</td><td>DPI with DBI Type C 3-line 9-bit</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>MIPI DSI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>MDDI</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input
- Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>- A chip select signal.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>DCX</td><td>I</td><td>- The DBI Type B interface (DCX): The signal for command or parameter select.
Low: Command
High: Parameter
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>- Serves as a read signal and read data at the rising edge.
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>WRX
(SCL)</td><td>I</td><td>- The DBI Type B system (WRX): Serves as a write signal and writes data at the rising edge.
- Serial interface (SCL): Serial clock input
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>DB [23:0]</td><td>I/O</td><td>- A 24-bit parallel bi-directional data bus for MPU system
<table>
<tr><th>Interface Mode</th><th>Data Pin in Use</th></tr>
<tr><td>DBI Type B 8-bit</td><td>DB [7:0]</td></tr>
<tr><td>DBI Type B 16-bit</td><td>DB [15:0]</td></tr>
<tr><td>DBI Type B 24-bit</td><td>DB [23:0]</td></tr>
<tr><td>DBI Type B 9-bit</td><td>DB [8:0]</td></tr>
<tr><td>DBI Type B 18-bit</td><td>DB [17:0]</td></tr>
<tr><td>DPI with DBI Type C 3-line 9-bit</td><td>DB [23:0], SDI, SDO</td></tr>
</table>
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>SDI
(SDA)</td><td>I/O</td><td>Serial data input pin used for the SPI Interface.
SDI: Serial data input pin</td></tr>
</table>

<table>
<tr><td></td><td></td><td>SDA: Serial data input/output bidirectional pin
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial data output pin used for the SPI Interface.
Leave the pin open when not in use.</td></tr>
<tr><td>TE_L / TE_R</td><td>O</td><td>-Tearing effect output
TE = TE_L= TE_R
Leave the pin open when not in use.</td></tr>
<tr><td>PCLK</td><td>I</td><td>- Dot clock signal for RGB interface operation
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>- Frame synchronizing signal for RGB interface operation
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>- Line synchronizing signal for RGB interface operation
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td>DE</td><td>I</td><td>- Data enable signal for RGB interface operation
Low: access enabled
High: access inhibited
Fix to VDDI or VSSI level when not in use.</td></tr>
<tr><td rowspan="2">HS_CP
HS_CN</td><td rowspan="2">I</td><td>MIPI DSI differential clock pair
If MIPI are not in use, they should be connected to VSSAM.</td></tr>
<tr><td>MDDI strobe signal lines
HS_CP (Stb+) and HS_CN (Stb-) are differential small swing signals. Make the wiring as short as possible so that the COG resistance becomes less than 10 ohm. The specifications of the interface must be compliant with the MDDI specification.
If MDDI are not in use, they should be connected to VSSAM.</td></tr>
<tr><td rowspan="2">HS_D0P
HS_D0N
HS_D1P
HS_D1N</td><td rowspan="2">I/O</td><td>MIPI DSI differential data pair.
If MIPI are not in use, they should be connected to VSSAM</td></tr>
<tr><td>MDDI data signal lines
HS_D0P (Data+) and HS_D0N (Data-) are differential small swing signals. Make the wiring as short as possible so that the COG resistance becomes less than 10 ohm. The specifications of the interface must be compliant with the MDDI specification.
If MDDI are not in use, they should be connected to VSSAM.</td></tr>
<tr><td>ERR</td><td>O</td><td>- CRC and ECC error output pin for the MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it is output high if CRC/ECC error is found.
Leave the pin open when not in use.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>- Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface.
Low: 1 data lane
High: 2 data lanes
Fix to VSSI level when not in use.</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>- Differential clock polarity swap
For MIPI interface
<table>
<tr><th rowspan="2">DSWAP</th><th rowspan="2">PSWAP</th><th colspan="6">Pins</th></tr>
<tr><th>HS_CP</th><th>HS_CN</th><th>HS_D0P</th><th>HS_D0N</th><th>HS_D1P</th><th>HS_D1N</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>HS_CP</td><td>HS_CN</td><td>HS_D0P</td><td>HS_D0N</td><td>HS_D1P</td><td>HS_D1N</td></tr>
<tr><td>1</td><td>HS_CN</td><td>HS_CP</td><td>HS_D0N</td><td>HS_D0P</td><td>HS_D1N</td><td>HS_D1P</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>HS_CP</td><td>HS_CN</td><td>HS_D1P</td><td>HS_D1N</td><td>HS_D0P</td><td>HS_D0N</td></tr>
<tr><td>1</td><td>HS_CN</td><td>HS_CP</td><td>HS_D1N</td><td>HS_D1P</td><td>HS_D0N</td><td>HS_D0P</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td></td><td>For MDDI interface
<table>
<tr><th rowspan="2">DSWAP</th><th rowspan="2">PSWAP</th><th colspan="6">Pins</th></tr>
<tr><th>HS_CP</th><th>HS_CN</th><th>HS_D0P</th><th>HS_D0N</th><th>HS_D1P</th><th>HS_D1N</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>HS_CP</td><td>HS_CN</td><td>HS_D0P</td><td>HS_D0N</td><td>HS_D1P</td><td>HS_D1N</td></tr>
<tr><td>1</td><td>HS_CN</td><td>HS_CP</td><td>HS_D0N</td><td>HS_D0P</td><td>HS_D1N</td><td>HS_D1P</td></tr>
</table>
Fix to VSSI level when not in use.</td></tr>
<tr><td>RGBBP</td><td>I</td><td>- Test Pin
Fix to VSSI level.</td></tr>
<tr><td>GPO [3:0]</td><td>O</td><td>- Test Pin
Leave the pin open.</td></tr>
<tr><td>EXB1T</td><td>I</td><td>- Input pin to select the external DC/DC circuit.
Low: Using internal DC/DC for AVDD / AVEE
High: Using external DC/DC for AVDD / AVEE
Fix to VSSI level when not in use.</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>- Input pin to select the gamma voltage level sequence of V0~V255.
Low: V0 > V1 >…> V254 > V255, normally white
High: V255 > V254 >…> V1 > V0, normally black
Fix to VDDI level when not in use.</td></tr>
<tr><td>LEDON</td><td>O</td><td>- Used for turning On/Off external LED backlight control.
Leave the pin open when not in use.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>- The PWM frequency output for LED driver control.
Leave the pin open when not in use.</td></tr>
</table>

Table 3: Driver Output Pins

Driver Output Pins			
Pin Name	I/O	Type	Descriptions
S [1:1440]	O	LCD	- Source output voltage signals applied to a LCD panel
GOUT [1:32]	O	LCD	- Gate control signals and the swing voltage level is VGH to VGLO
SDUM [0:3]	O	LCD	- Dummy Source ***Leave the pin open when not in use.***
VGH	O	LCD	- High voltage level for gate control signals and gate circuit of panel VGH is already connected to VGH in IC.
VGLO (VGLO_L / VGLO_R)	O	LCD	- Low voltage level for gate control signals and gate circuit of panel
LVGL (LVGL_L / LVGL_R)	O	LCD	- Low voltage level for gate circuit of panel LVGL is already connected to VGL_REG in IC. (VGL_REG is the output voltage generated from VGL. LDO output used for panel voltage.) - Connect a capacitor for stabilization
VGMP (VGMP_PAD)	O	LCD	- Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP (VGSP_PAD)	O	LCD	- Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VGMN (VGMN_PAD)	O	LCD	- Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
VGSN (VGSN_PAD)	O	LCD	- Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.

Table 4: Charge Pump Relative Pins

Charge Pump Relative Pins			
Pin Name	I/O	Type	Descriptions
AVDD	O	Stabilizing capacitor	- Output voltage from step-up circuit 1, generated from VDDB. - Connect to a stabilizing capacitor between AVDD and VSSB.
AVEE	O	Stabilizing capacitor	- Output voltage from step-up circuit 2, generated from VDDB. - Connect to a stabilizing capacitor between AVEE and VSSB.
VCL	O	Stabilizing capacitor	- Output voltage from step-up circuit 3, generated from VDDB. - Connect to a stabilizing capacitor between VCL and VSSB.
VGH	O	Stabilizing capacitor	- Output voltage from step-up circuit 4, generated from VDDB. - Connect to a stabilizing capacitor between VGH and VSSB.
VGL	O	Stabilizing capacitor	- Substrate voltage for driver IC - Output voltage from step-up circuit 5, generated from VDDB. - Connect to a stabilizing capacitor between VGL and VSSB.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating AVDD level. - Capacitor connection pins for the step-up circuit 1.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating AVEE level. - Capacitor connection pins for the step-up circuit 2.
C31P, C31N C32P, C32N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VCL level. - Capacitor connection pins for the step-up circuit 3.
C41P, C41N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VGH level. - Capacitor connection pins for the step-up circuit 4.
C51P, C51N	-	Flying capacitor	- Connect the charge-pumping capacitor for generating VGL level. - Capacitor connection pins for the step-up circuit 5.

Table 5: DC/DC Converter Pins

DC/DC Converter Pins			
Pin Name	I/O	Type	Descriptions
EXTN (CTRL_A)	O	Positive NMOS	-PWM control output for gate of NMOS in positive DC/DC converter (for AVDD) -CTRL_A : Control signal for an external charge pump IC (ex: ILI4002)
EXTP (CTRL_B)	O	Negative PMOS	-PWM control output for gate of PMOS in negative DC/DC converter (for AVEE) -CTRL_B : Control signal for an external charge pump IC (ex: ILI4002)

Table 6: Power Pins

Power Pins			
Pin Name	I/O	Type	Descriptions
VRGH (VRGH_L / VRGH_R)	O	LDO Stabilizing Capacitor	- Output voltage generated from AVDD. - Connect a capacitor for stabilization. ***Leave the pin open when not in use.***
VREF_PWR	O	LDO Stabilizing Capacitor	- Reference voltage for regulator output. - Connect a capacitor for stabilization.
VDDA	P	Analog	- Power supply for analog system. - VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDA1	P	Analog	- Power supply for analog system. - VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDR	P	Regulator	- Power supply for regulator system. - VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDR1	P	Regulator	- Power supply for regulator system. - VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDB	P	DC/DC	- Power supply for DC/DC converter. - VDDA, VDDR, VDDA1, VDDB and VDDR1 should be the same input voltage level of 2.5 ~ 3.3V.
VDDI	P	I/O	- Power supply for I/O block. ***Exclude MIPI/MDDI interface.***
DVDD	O	Stabilizing Capacitor	- Internal logic voltage output - Connect a capacitor for stabilization.
NDVDD	O	Stabilizing Capacitor	- Negative internal logic voltage output - Connect a capacitor for stabilization.
VDDAM	P	MIPI/MDDI	- Power supply for MIPI/MDDI analog system.
MVDDA	O	MIPI Stabilizing Capacitor	- Regulator output for internal MIPI / MDDI analog system (1.5V typical) - Connect a capacitor for stabilization.
MVDDL	O	MIPI Stabilizing Capacitor	- Regulator output for internal MIPI low power system (1.2V typical) - Connect a capacitor for stabilization.
VSSA	P	Analog	- System ground for analog circuit.
VSSR	P	Regulator	- System ground for regulator circuit.
VSSR1	P	Regulator	- System ground for regulator circuit.
VSSB	P	DC/DC	- System ground for DC/DC convertor.
VSSI	P	I/O	- System ground for interface system.
GND	P	Digital	- System ground for internal digital system.
AVSS	P	Source OP	- System ground for source OP system.
VSSAM	P	MIPI/MDDI	- System ground for MIPI/MDDI system.
VPP	I	OTP	- OTP programming power.
VCOM	O	LDO	- Output voltage generated from VCI / VCL

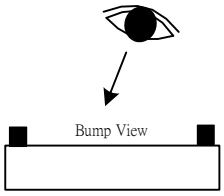
(VCOM_L / VCOM_R)		Stabilizing Capacitor	- Connect a capacitor for stabilization. VCOM=VCOM_L=VCOM_R

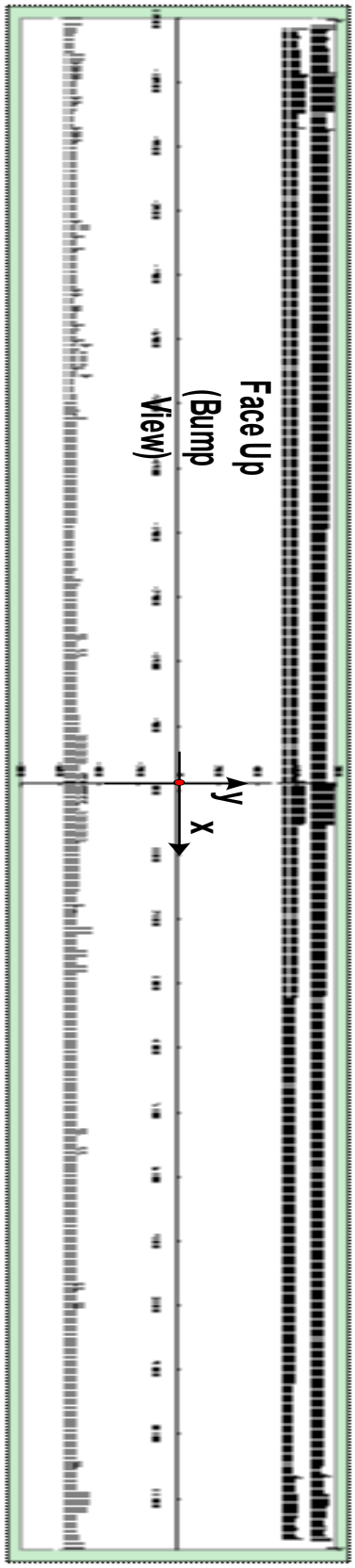
Table 7: Test Pins

Test Pins			
Pin Name	I/O	Type	Descriptions
PADA [1:4] PADB [1:4]	I/O		- Dummy Pin.
CONTACT1A CONTACT1B	I/O		- Test pin, for test bonding quality, IC internal will connect CONTACT1A with CONTACT1B.
KBBC	O		- Test pin, not accessible to user. MUST be left open.
VSEL	-		- Dummy pin.
TEST [0:3]	I		- Test pin, not accessible to user. MUST be left open. (Internal weakly pull low)
OSC_TEST	I		- Test pin, not accessible to user, MUST be left open (Internal weakly pull low)
VSSIDUM [0:106]	O		- These are dummy pins with VSSI potential (not have any function inside). - Signal traces cannot pass through on glass under these pads.
DUMMY	-		- Dummy pads. ***Leave the pin open.***

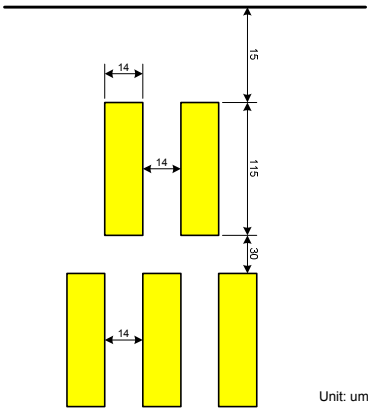
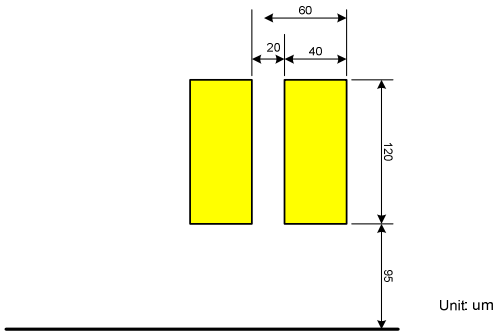
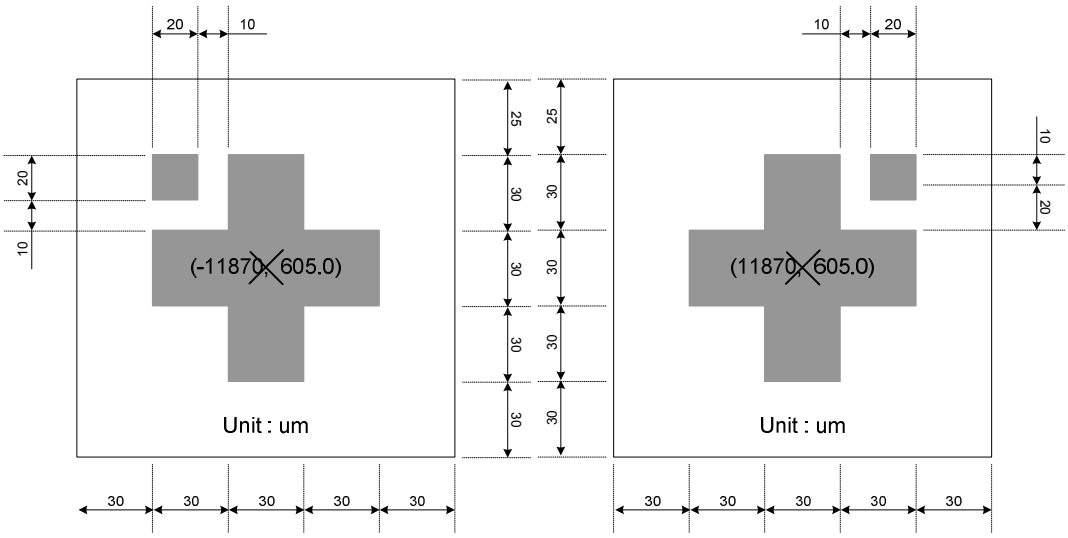
3.4. Pin Assignment

Chip Size：24360um X 1530um
Chip Thickness：280um (typ.)
Pad Location：Pad Center
Coordinate Origin：Chip center
Au Bump Size：
1. 14um X 115um
2. 40um X 120um





3.5. Bump Arrangement

Output PAD	
Input PAD	
Alignment mark	

3.6. Pad Coordination

No.	Text Name	X-axis	Y-axis
1	VSSIDUM0	-11880	-620
2	VSSIDUM1	-11790	-620
3	PADA1	-11730	-620
4	PADB1	-11670	-620
5	VCOM_L	-11610	-620
6	VCOM_L	-11550	-620
7	VCOM_L	-11490	-620
8	VCOM_L	-11430	-620
9	VCOM_L	-11370	-620
10	CONTACT1A	-11310	-620
11	CONTACT1B	-11250	-620
12	VPP	-11190	-620
13	VPP	-11130	-620
14	VPP	-11070	-620
15	VPP	-11010	-620
16	VPP	-10950	-620
17	VGL	-10890	-620
18	VGL	-10830	-620
19	VGLO_L	-10770	-620
20	VGLO_L	-10710	-620
21	LVGL_L	-10650	-620
22	LVGL_L	-10590	-620
23	VRGH_L	-10530	-620
24	VRGH_L	-10470	-620
25	VCL	-10410	-620
26	VCL	-10350	-620
27	VCL	-10290	-620
28	VCL	-10230	-620
29	VREF_PWR	-10170	-620
30	VREF_PWR	-10110	-620
31	VREF_PWR	-10050	-620
32	VREF_PWR	-9990	-620
33	VSSA	-9930	-620
34	VSSA	-9870	-620
35	VSSA	-9810	-620
36	VSSA	-9750	-620
37	VDDA	-9690	-620
38	VDDA	-9630	-620
39	VDDA	-9570	-620
40	VDDA	-9510	-620
41	VDDR	-9450	-620
42	VDDR	-9390	-620
43	VDDR	-9330	-620
44	VDDR	-9270	-620
45	VSSR	-9210	-620
46	VSSR	-9150	-620
47	VSSR	-9090	-620
48	VSSR	-9030	-620
49	TEST[0]	-8970	-620
50	TEST[1]	-8910	-620
51	TEST[2]	-8850	-620
52	TEST[3]	-8790	-620
53	VDDR	-8730	-620
54	DUMMY	-8670	-620
55	DUMMY	-8610	-620
56	VGSN_PAD	-8550	-620
57	VGSN_PAD	-8490	-620
58	VGSP_PAD	-8430	-620
59	VGMN_PAD	-8370	-620
60	VGMN_PAD	-8310	-620
61	VGMP_PAD	-8250	-620
62	GND	-8190	-620
63	GND	-8130	-620
64	GND	-8070	-620
65	DVDD	-8010	-620
66	DVDD	-7950	-620
67	DVDD	-7890	-620
68	VDDB	-7830	-620
69	VDDB	-7770	-620
70	VDDB	-7710	-620
71	VCL	-7650	-620
72	VCL	-7590	-620
73	VCL	-7530	-620
74	VCL	-7470	-620
75	VCL	-7410	-620
76	VCL	-7350	-620
77	AVSS	-7290	-620
78	AVSS	-7230	-620
79	AVSS	-7170	-620
80	VDDI	-7110	-620
81	LANSEL	-7050	-620
82	DSWAP	-6990	-620
83	PSWAP	-6930	-620
84	VSSI	-6870	-620
85	DUMMY	-6810	-620
86	NBWSEL	-6750	-620
87	DUMMY	-6690	-620
88	DUMMY	-6630	-620
89	DUMMY	-6570	-620
90	DUMMY	-6510	-620
91	VDDI	-6450	-620
92	RGBBP	-6390	-620
93	DUMMY	-6330	-620
94	IM3	-6270	-620
95	IM2	-6210	-620
96	IM1	-6150	-620
97	IM0	-6090	-620
98	GPO3	-6030	-620
99	GPO2	-5970	-620
100	GPO1	-5910	-620
101	GPO0	-5850	-620
102	EXB1T	-5790	-620
103	TE_L	-5730	-620
104	VSEL	-5670	-620
105	SDO	-5610	-620
106	SDI	-5550	-620
107	DCX	-5490	-620
108	WRX	-5430	-620
109	RDX	-5370	-620
110	CSX	-5310	-620
111	RESX	-5250	-620
112	VSSI	-5190	-620
113	VSSI	-5130	-620
114	VSSI	-5070	-620
115	VDDI	-5010	-620
116	VDDI	-4950	-620
117	VDDI	-4890	-620
118	DB[23]	-4830	-620
119	DB[22]	-4770	-620
120	DB[21]	-4710	-620
121	DB[20]	-4650	-620
122	DB[19]	-4590	-620
123	DB[18]	-4530	-620
124	DB[17]	-4470	-620
125	DB[16]	-4410	-620
126	DB[15]	-4350	-620
127	DB[14]	-4290	-620
128	DB[13]	-4230	-620
129	DB[12]	-4170	-620
130	DB[11]	-4110	-620
131	DB[10]	-4050	-620
132	DB[9]	-3990	-620
133	DB[8]	-3930	-620
134	DB[7]	-3870	-620
135	DB[6]	-3810	-620
136	DB[5]	-3750	-620
137	DB[4]	-3690	-620
138	DB[3]	-3630	-620
139	DB[2]	-3570	-620
140	DB[1]	-3510	-620
141	DB[0]	-3450	-620
142	DE	-3390	-620
143	PCLK	-3330	-620
144	HS	-3270	-620
145	VS	-3210	-620
146	LEDPWM	-3150	-620
147	LEDON	-3090	-620
148	KBBC	-3030	-620
149	ERR	-2970	-620
150	VDDI	-2910	-620
151	VDDI	-2850	-620
152	VDDI	-2790	-620
153	VSSI	-2730	-620
154	VSSI	-2670	-620
155	VSSI	-2610	-620
156	AVDD	-2550	-620
157	AVDD	-2490	-620
158	AVDD	-2430	-620
159	AVDD	-2370	-620
160	AVSS	-2310	-620
161	AVSS	-2250	-620
162	AVSS	-2190	-620
163	AVSS	-2130	-620
164	AVEE	-2070	-620
165	AVEE	-2010	-620
166	AVEE	-1950	-620
167	AVEE	-1890	-620
168	AVEE	-1830	-620
169	VDDA1	-1770	-620
170	VDDA1	-1710	-620
171	VDDA1	-1650	-620
172	VDDA1	-1590	-620
173	GND	-1530	-620
174	GND	-1470	-620
175	GND	-1410	-620
176	GND	-1350	-620
177	DVDD	-1290	-620
178	DVDD	-1230	-620
179	DVDD	-1170	-620
180	DVDD	-1110	-620
181	VSSAM	-1050	-620
182	VSSAM	-990	-620
183	VSSAM	-930	-620
184	VSSAM	-870	-620
185	VSSAM	-810	-620
186	HS_D1P	-750	-620
187	HS_D1P	-690	-620
188	HS_D1P	-630	-620
189	HS_D1P	-570	-620
190	HS_D1N	-510	-620
191	HS_D1N	-450	-620
192	HS_D1N	-390	-620
193	HS_D1N	-330	-620
194	VSSAM	-270	-620
195	VSSAM	-210	-620
196	HS_CP	-150	-620
197	HS_CP	-90	-620
198	HS_CP	-30	-620
199	HS_CP	30	-620
200	HS_CN	90	-620
201	HS_CN	150	-620
202	HS_CN	210	-620
203	HS_CN	270	-620
204	VSSAM	330	-620
205	VSSAM	390	-620
206	HS_D0P	450	-620
207	HS_D0P	510	-620
208	HS_D0P	570	-620
209	HS_D0P	630	-620
210	HS_D0N	690	-620
211	HS_D0N	750	-620
212	HS_D0N	810	-620
213	HS_D0N	870	-620
214	VSSAM	930	-620
215	VSSAM	990	-620
216	MVDDL	1050	-620
217	MVDDL	1110	-620
218	MVDDL	1170	-620
219	MVDDA	1230	-620
220	MVDDA	1290	-620
221	MVDDA	1350	-620
222	VDDAM	1410	-620
223	VDDAM	1470	-620
224	VDDAM	1530	-620
225	VDDAM	1590	-620
226	VDDAM	1650	-620
227	VDDR1	1710	-620
228	VDDR1	1770	-620
229	VDDR1	1830	-620
230	OSC_TEST	1890	-620
231	TE_R	1950	-620
232	VSSR1	2010	-620
233	VSSR1	2070	-620
234	VSSR1	2130	-620
235	VSSR1	2190	-620
236	NDVDD	2250	-620
237	NDVDD	2310	-620
238	VRGH	2370	-620
239	VRGH	2430	-620
240	EXTP	2490	-620

No.	Text Name	X-axis	Y-axis
241	EXTP	2550	-620
242	DUMMY	2610	-620
243	DUMMY	2670	-620
244	EXTN	2730	-620
245	EXTN	2790	-620
246	DUMMY	2850	-620
247	DUMMY	2910	-620
248	VDDB	2970	-620
249	VDDB	3030	-620
250	VDDB	3090	-620
251	VDDB	3150	-620
252	VDDB	3210	-620
253	VDDB	3270	-620
254	VSSB	3330	-620
255	VSSB	3390	-620
256	VSSB	3450	-620
257	VSSB	3510	-620
258	VSSB	3570	-620
259	VSSB	3630	-620
260	C11P	3690	-620
261	C11P	3750	-620
262	C11P	3810	-620
263	C11N	3870	-620
264	C11N	3930	-620
265	C11N	3990	-620
266	C12P	4050	-620
267	C12P	4110	-620
268	C12P	4170	-620
269	C12N	4230	-620
270	C12N	4290	-620
271	C12N	4350	-620
272	C13N	4410	-620
273	C13N	4470	-620
274	C13N	4530	-620
275	C13P	4590	-620
276	C13P	4650	-620
277	C13P	4710	-620
278	C14P	4770	-620
279	C14P	4830	-620
280	C14P	4890	-620
281	C14N	4950	-620
282	C14N	5010	-620
283	C14N	5070	-620
284	AVDD	5130	-620
285	AVDD	5190	-620
286	AVDD	5250	-620
287	AVDD	5310	-620
288	AVSS	5370	-620
289	AVSS	5430	-620
290	AVSS	5490	-620
291	AVSS	5550	-620
292	AVSS	5610	-620
293	AVEE	5670	-620
294	AVEE	5730	-620
295	AVEE	5790	-620
296	AVEE	5850	-620
297	AVEE	5910	-620
298	AVEE	5970	-620
299	C21P	6030	-620
300	C21P	6090	-620

No.	Text Name	X-axis	Y-axis
301	C21P	6150	-620
302	C21N	6210	-620
303	C21N	6270	-620
304	C21N	6330	-620
305	C22P	6390	-620
306	C22P	6450	-620
307	C22P	6510	-620
308	C22N	6570	-620
309	C22N	6630	-620
310	C22N	6690	-620
311	C23P	6750	-620
312	C23P	6810	-620
313	C23P	6870	-620
314	C23N	6930	-620
315	C23N	6990	-620
316	C23N	7050	-620
317	C24P	7110	-620
318	C24P	7170	-620
319	C24P	7230	-620
320	C24N	7290	-620
321	C24N	7350	-620
322	C24N	7410	-620
323	VDDB	7470	-620
324	VDDB	7530	-620
325	VDDB	7590	-620
326	VDDB	7650	-620
327	VDDB	7710	-620
328	VCL	7770	-620
329	VCL	7830	-620
330	VCL	7890	-620
331	VCL	7950	-620
332	VCL	8010	-620
333	VCL	8070	-620
334	VCL	8130	-620
335	AVSS	8190	-620
336	AVSS	8250	-620
337	AVSS	8310	-620
338	VSSB	8370	-620
339	VSSB	8430	-620
340	VSSB	8490	-620
341	VSSB	8550	-620
342	C31P	8610	-620
343	C31P	8670	-620
344	C31P	8730	-620
345	C31N	8790	-620
346	C31N	8850	-620
347	C31N	8910	-620
348	C32N	8970	-620
349	C32N	9030	-620
350	C32N	9090	-620
351	C32P	9150	-620
352	C32P	9210	-620
353	C32P	9270	-620
354	DVDD	9330	-620
355	DVDD	9390	-620
356	DVDD	9450	-620
357	GND	9510	-620
358	GND	9570	-620
359	GND	9630	-620
360	C41P	9690	-620

No.	Text Name	X-axis	Y-axis
361	C41P	9750	-620
362	C41N	9810	-620
363	C41N	9870	-620
364	VGH	9930	-620
365	VGH	9990	-620
366	VGH	10050	-620
367	VGH	10110	-620
368	VRGH_R	10170	-620
369	VRGH_R	10230	-620
370	C51P	10290	-620
371	C51P	10350	-620
372	C51N	10410	-620
373	C51N	10470	-620
374	LVGL_R	10530	-620
375	LVGL_R	10590	-620
376	VGLO_R	10650	-620
377	VGLO_R	10710	-620
378	VGL	10770	-620
379	VGL	10830	-620
380	VGL	10890	-620
381	VGL	10950	-620
382	DUMMY	11010	-620
383	DUMMY	11070	-620
384	DUMMY	11130	-620
385	DUMMY	11190	-620
386	DUMMY	11250	-620
387	DUMMY	11310	-620
388	VCOM_R	11370	-620
389	VCOM_R	11430	-620
390	VCOM_R	11490	-620
391	VCOM_R	11550	-620
392	VCOM_R	11610	-620
393	PADA2	11670	-620
394	PADB2	11730	-620
395	VSSIDUM2	11790	-620
396	VSSIDUM3	11880	-620
397	DUMMY	12054	622.5
398	DUMMY	12040	477.5
399	DUMMY	12026	622.5
400	DUMMY	12012	477.5
401	DUMMY	11998	622.5
402	VSSIDUM4	11760	622.5
403	VSSIDUM5	11732	477.5
404	VSSIDUM6	11718	622.5
405	PADA3	11704	477.5
406	PADB3	11690	622.5
407	VGH	11676	477.5
408	VGH	11662	622.5
409	VGH	11648	477.5
410	VGLO_R	11634	622.5
411	VGLO_R	11620	477.5
412	VGLO_R	11606	622.5
413	GOUT1	11592	477.5
414	GOUT1	11578	622.5
415	GOUT2	11564	477.5
416	GOUT2	11550	622.5
417	LVGL_R	11536	477.5
418	LVGL_R	11522	622.5
419	LVGL_R	11508	477.5
420	VRGH_R	11494	622.5

No.	Text Name	X-axis	Y-axis
421	VRGH_R	11480	477.5
422	VRGH_R	11466	622.5
423	VGLO_R	11452	477.5
424	VGLO_R	11438	622.5
425	VGLO_R	11424	477.5
426	GOUT3	11410	622.5
427	GOUT3	11396	477.5
428	GOUT4	11382	622.5
429	GOUT4	11368	477.5
430	GOUT5	11354	622.5
431	GOUT5	11340	477.5
432	GOUT6	11326	622.5
433	GOUT6	11312	477.5
434	GOUT7	11298	622.5
435	GOUT7	11284	477.5
436	GOUT8	11270	622.5
437	GOUT8	11256	477.5
438	GOUT9	11242	622.5
439	GOUT9	11228	477.5
440	GOUT10	11214	622.5
441	GOUT10	11200	477.5
442	GOUT11	11186	622.5
443	GOUT11	11172	477.5
444	GOUT12	11158	622.5
445	GOUT12	11144	477.5
446	GOUT13	11130	622.5
447	GOUT13	11116	477.5
448	GOUT14	11102	622.5
449	GOUT14	11088	477.5
450	GOUT15	11074	622.5
451	GOUT15	11060	477.5
452	GOUT16	11046	622.5
453	GOUT16	11032	477.5
454	VGH	11018	622.5
455	VGH	11004	477.5
456	VGH	10990	622.5
457	VGH	10976	477.5
458	VGH	10962	622.5
459	VGH	10948	477.5
460	VGH	10934	622.5
461	VGH	10920	477.5
462	VGLO_R	10906	622.5
463	VGLO_R	10892	477.5
464	VGLO_R	10878	622.5
465	VGLO_R	10864	477.5
466	VGLO_R	10850	622.5
467	VGLO_R	10836	477.5
468	VGLO_R	10822	622.5
469	VGLO_R	10808	477.5
470	VGLO_R	10794	622.5
471	VSSIDUM7	10780	477.5
472	VSSIDUM8	10766	622.5
473	SDUM0	10752	477.5
474	SDUM1	10738	622.5
475	S1	10724	477.5
476	S2	10710	622.5
477	S3	10696	477.5
478	S4	10682	622.5
479	S5	10668	477.5
480	S6	10654	622.5

No.	Text Name	X-axis	Y-axis
481	S7	10640	477.5
482	S8	10626	622.5
483	S9	10612	477.5
484	S10	10598	622.5
485	S11	10584	477.5
486	S12	10570	622.5
487	S13	10556	477.5
488	S14	10542	622.5
489	S15	10528	477.5
490	S16	10514	622.5
491	S17	10500	477.5
492	S18	10486	622.5
493	S19	10472	477.5
494	S20	10458	622.5
495	S21	10444	477.5
496	S22	10430	622.5
497	S23	10416	477.5
498	S24	10402	622.5
499	S25	10388	477.5
500	S26	10374	622.5
501	S27	10360	477.5
502	S28	10346	622.5
503	S29	10332	477.5
504	S30	10318	622.5
505	S31	10304	477.5
506	S32	10290	622.5
507	S33	10276	477.5
508	S34	10262	622.5
509	S35	10248	477.5
510	S36	10234	622.5
511	S37	10220	477.5
512	S38	10206	622.5
513	S39	10192	477.5
514	S40	10178	622.5
515	S41	10164	477.5
516	S42	10150	622.5
517	S43	10136	477.5
518	S44	10122	622.5
519	S45	10108	477.5
520	S46	10094	622.5
521	S47	10080	477.5
522	S48	10066	622.5
523	S49	10052	477.5
524	S50	10038	622.5
525	S51	10024	477.5
526	S52	10010	622.5
527	S53	9996	477.5
528	S54	9982	622.5
529	S55	9968	477.5
530	S56	9954	622.5
531	S57	9940	477.5
532	S58	9926	622.5
533	S59	9912	477.5
534	S60	9898	622.5
535	S61	9884	477.5
536	S62	9870	622.5
537	S63	9856	477.5
538	S64	9842	622.5
539	S65	9828	477.5
540	S66	9814	622.5
541	S67	9800	477.5
542	S68	9786	622.5
543	S69	9772	477.5
544	S70	9758	622.5
545	S71	9744	477.5
546	S72	9730	622.5
547	S73	9716	477.5
548	S74	9702	622.5
549	S75	9688	477.5
550	S76	9674	622.5
551	S77	9660	477.5
552	S78	9646	622.5
553	S79	9632	477.5
554	S80	9618	622.5
555	S81	9604	477.5
556	S82	9590	622.5
557	S83	9576	477.5
558	S84	9562	622.5
559	S85	9548	477.5
560	S86	9534	622.5
561	S87	9520	477.5
562	S88	9506	622.5
563	S89	9492	477.5
564	S90	9478	622.5
565	S91	9464	477.5
566	S92	9450	622.5
567	S93	9436	477.5
568	S94	9422	622.5
569	S95	9408	477.5
570	S96	9394	622.5
571	S97	9380	477.5
572	S98	9366	622.5
573	S99	9352	477.5
574	S100	9338	622.5
575	S101	9324	477.5
576	S102	9310	622.5
577	S103	9296	477.5
578	S104	9282	622.5
579	S105	9268	477.5
580	S106	9254	622.5
581	S107	9240	477.5
582	S108	9226	622.5
583	S109	9212	477.5
584	S110	9198	622.5
585	S111	9184	477.5
586	S112	9170	622.5
587	S113	9156	477.5
588	S114	9142	622.5
589	S115	9128	477.5
590	S116	9114	622.5
591	S117	9100	477.5
592	S118	9086	622.5
593	S119	9072	477.5
594	S120	9058	622.5
595	S121	9044	477.5
596	S122	9030	622.5
597	S123	9016	477.5
598	S124	9002	622.5
599	S125	8988	477.5
600	S126	8974	622.5
601	S127	8960	477.5
602	S128	8946	622.5
603	S129	8932	477.5
604	S130	8918	622.5
605	S131	8904	477.5
606	S132	8890	622.5
607	S133	8876	477.5
608	S134	8862	622.5
609	S135	8848	477.5
610	S136	8834	622.5
611	S137	8820	477.5
612	S138	8806	622.5
613	S139	8792	477.5
614	S140	8778	622.5
615	S141	8764	477.5
616	S142	8750	622.5
617	S143	8736	477.5
618	S144	8722	622.5
619	S145	8708	477.5
620	S146	8694	622.5
621	S147	8680	477.5
622	S148	8666	622.5
623	S149	8652	477.5
624	S150	8638	622.5
625	S151	8624	477.5
626	S152	8610	622.5
627	S153	8596	477.5
628	S154	8582	622.5
629	S155	8568	477.5
630	S156	8554	622.5
631	S157	8540	477.5
632	S158	8526	622.5
633	S159	8512	477.5
634	S160	8498	622.5
635	S161	8484	477.5
636	S162	8470	622.5
637	S163	8456	477.5
638	S164	8442	622.5
639	S165	8428	477.5
640	S166	8414	622.5
641	S167	8400	477.5
642	S168	8386	622.5
643	S169	8372	477.5
644	S170	8358	622.5
645	S171	8344	477.5
646	S172	8330	622.5
647	S173	8316	477.5
648	S174	8302	622.5
649	S175	8288	477.5
650	S176	8274	622.5
651	S177	8260	477.5
652	S178	8246	622.5
653	S179	8232	477.5
654	S180	8218	622.5
655	S181	8204	477.5
656	S182	8190	622.5
657	S183	8176	477.5
658	S184	8162	622.5
659	S185	8148	477.5
660	S186	8134	622.5
661	S187	8120	477.5
662	S188	8106	622.5
663	S189	8092	477.5
664	S190	8078	622.5
665	S191	8064	477.5
666	S192	8050	622.5
667	S193	8036	477.5
668	S194	8022	622.5
669	S195	8008	477.5
670	S196	7994	622.5
671	S197	7980	477.5
672	S198	7966	622.5
673	S199	7952	477.5
674	S200	7938	622.5
675	S201	7924	477.5
676	S202	7910	622.5
677	S203	7896	477.5
678	S204	7882	622.5
679	S205	7868	477.5
680	S206	7854	622.5
681	S207	7840	477.5
682	S208	7826	622.5
683	S209	7812	477.5
684	S210	7798	622.5
685	S211	7784	477.5
686	S212	7770	622.5
687	S213	7756	477.5
688	S214	7742	622.5
689	S215	7728	477.5
690	S216	7714	622.5
691	S217	7700	477.5
692	S218	7686	622.5
693	S219	7672	477.5
694	S220	7658	622.5
695	S221	7644	477.5
696	S222	7630	622.5
697	S223	7616	477.5
698	S224	7602	622.5
699	S225	7588	477.5
700	S226	7574	622.5
701	S227	7560	477.5
702	S228	7546	622.5
703	S229	7532	477.5
704	S230	7518	622.5
705	S231	7504	477.5
706	S232	7490	622.5
707	S233	7476	477.5
708	S234	7462	622.5
709	S235	7448	477.5
710	S236	7434	622.5
711	S237	7420	477.5
712	S238	7406	622.5
713	S239	7392	477.5
714	S240	7378	622.5
715	S241	7364	477.5
716	S242	7350	622.5
717	S243	7336	477.5
718	S244	7322	622.5
719	S245	7308	477.5
720	S246	7294	622.5

No.	Text Name	X-axis	Y-axis
721	S247	7280	477.5
722	S248	7266	622.5
723	S249	7252	477.5
724	S250	7238	622.5
725	S251	7224	477.5
726	S252	7210	622.5
727	S253	7196	477.5
728	S254	7182	622.5
729	S255	7168	477.5
730	S256	7154	622.5
731	S257	7140	477.5
732	S258	7126	622.5
733	S259	7112	477.5
734	S260	7098	622.5
735	S261	7084	477.5
736	S262	7070	622.5
737	S263	7056	477.5
738	S264	7042	622.5
739	S265	7028	477.5
740	S266	7014	622.5
741	S267	7000	477.5
742	S268	6986	622.5
743	S269	6972	477.5
744	S270	6958	622.5
745	S271	6944	477.5
746	S272	6930	622.5
747	S273	6916	477.5
748	S274	6902	622.5
749	S275	6888	477.5
750	S276	6874	622.5
751	S277	6860	477.5
752	S278	6846	622.5
753	S279	6832	477.5
754	S280	6818	622.5
755	S281	6804	477.5
756	S282	6790	622.5
757	S283	6776	477.5
758	S284	6762	622.5
759	S285	6748	477.5
760	S286	6734	622.5
761	S287	6720	477.5
762	S288	6706	622.5
763	S289	6692	477.5
764	S290	6678	622.5
765	S291	6664	477.5
766	S292	6650	622.5
767	S293	6636	477.5
768	S294	6622	622.5
769	S295	6608	477.5
770	S296	6594	622.5
771	S297	6580	477.5
772	S298	6566	622.5
773	S299	6552	477.5
774	S300	6538	622.5
775	S301	6524	477.5
776	S302	6510	622.5
777	S303	6496	477.5
778	S304	6482	622.5
779	S305	6468	477.5
780	S306	6454	622.5
781	S307	6440	477.5
782	S308	6426	622.5
783	S309	6412	477.5
784	S310	6398	622.5
785	S311	6384	477.5
786	S312	6370	622.5
787	S313	6356	477.5
788	S314	6342	622.5
789	S315	6328	477.5
790	S316	6314	622.5
791	S317	6300	477.5
792	S318	6286	622.5
793	S319	6272	477.5
794	S320	6258	622.5
795	S321	6244	477.5
796	S322	6230	622.5
797	S323	6216	477.5
798	S324	6202	622.5
799	S325	6188	477.5
800	S326	6174	622.5
801	S327	6160	477.5
802	S328	6146	622.5
803	S329	6132	477.5
804	S330	6118	622.5
805	S331	6104	477.5
806	S332	6090	622.5
807	S333	6076	477.5
808	S334	6062	622.5
809	S335	6048	477.5
810	S336	6034	622.5
811	S337	6020	477.5
812	S338	6006	622.5
813	S339	5992	477.5
814	S340	5978	622.5
815	S341	5964	477.5
816	S342	5950	622.5
817	S343	5936	477.5
818	S344	5922	622.5
819	S345	5908	477.5
820	S346	5894	622.5
821	S347	5880	477.5
822	S348	5866	622.5
823	S349	5852	477.5
824	S350	5838	622.5
825	S351	5824	477.5
826	S352	5810	622.5
827	S353	5796	477.5
828	S354	5782	622.5
829	S355	5768	477.5
830	S356	5754	622.5
831	S357	5740	477.5
832	S358	5726	622.5
833	S359	5712	477.5
834	S360	5698	622.5
835	S361	5684	477.5
836	S362	5670	622.5
837	S363	5656	477.5
838	S364	5642	622.5
839	S365	5628	477.5
840	S366	5614	622.5
841	S367	5600	477.5
842	S368	5586	622.5
843	S369	5572	477.5
844	S370	5558	622.5
845	S371	5544	477.5
846	S372	5530	622.5
847	S373	5516	477.5
848	S374	5502	622.5
849	S375	5488	477.5
850	S376	5474	622.5
851	S377	5460	477.5
852	S378	5446	622.5
853	S379	5432	477.5
854	S380	5418	622.5
855	S381	5404	477.5
856	S382	5390	622.5
857	S383	5376	477.5
858	S384	5362	622.5
859	S385	5348	477.5
860	S386	5334	622.5
861	S387	5320	477.5
862	S388	5306	622.5
863	S389	5292	477.5
864	S390	5278	622.5
865	S391	5264	477.5
866	S392	5250	622.5
867	S393	5236	477.5
868	S394	5222	622.5
869	S395	5208	477.5
870	S396	5194	622.5
871	S397	5180	477.5
872	S398	5166	622.5
873	S399	5152	477.5
874	S400	5138	622.5
875	S401	5124	477.5
876	S402	5110	622.5
877	S403	5096	477.5
878	S404	5082	622.5
879	S405	5068	477.5
880	S406	5054	622.5
881	S407	5040	477.5
882	S408	5026	622.5
883	S409	5012	477.5
884	S410	4998	622.5
885	S411	4984	477.5
886	S412	4970	622.5
887	S413	4956	477.5
888	S414	4942	622.5
889	S415	4928	477.5
890	S416	4914	622.5
891	S417	4900	477.5
892	S418	4886	622.5
893	S419	4872	477.5
894	S420	4858	622.5
895	S421	4844	477.5
896	S422	4830	622.5
897	S423	4816	477.5
898	S424	4802	622.5
899	S425	4788	477.5
900	S426	4774	622.5
901	S427	4760	477.5
902	S428	4746	622.5
903	S429	4732	477.5
904	S430	4718	622.5
905	S431	4704	477.5
906	S432	4690	622.5
907	S433	4676	477.5
908	S434	4662	622.5
909	S435	4648	477.5
910	S436	4634	622.5
911	S437	4620	477.5
912	S438	4606	622.5
913	S439	4592	477.5
914	S440	4578	622.5
915	S441	4564	477.5
916	S442	4550	622.5
917	S443	4536	477.5
918	S444	4522	622.5
919	S445	4508	477.5
920	S446	4494	622.5
921	S447	4480	477.5
922	S448	4466	622.5
923	S449	4452	477.5
924	S450	4438	622.5
925	S451	4424	477.5
926	S452	4410	622.5
927	S453	4396	477.5
928	S454	4382	622.5
929	S455	4368	477.5
930	S456	4354	622.5
931	S457	4340	477.5
932	S458	4326	622.5
933	S459	4312	477.5
934	S460	4298	622.5
935	S461	4284	477.5
936	S462	4270	622.5
937	S463	4256	477.5
938	S464	4242	622.5
939	S465	4228	477.5
940	S466	4214	622.5
941	S467	4200	477.5
942	S468	4186	622.5
943	S469	4172	477.5
944	S470	4158	622.5
945	S471	4144	477.5
946	S472	4130	622.5
947	S473	4116	477.5
948	S474	4102	622.5
949	S475	4088	477.5
950	S476	4074	622.5
951	S477	4060	477.5
952	S478	4046	622.5
953	S479	4032	477.5
954	S480	4018	622.5
955	S481	4004	477.5
956	S482	3990	622.5
957	S483	3976	477.5
958	S484	3962	622.5
959	S485	3948	477.5
960	S486	3934	622.5

No.	Text Name	X-axis	Y-axis
961	S487	3920	477.5
962	S488	3906	622.5
963	S489	3892	477.5
964	S490	3878	622.5
965	S491	3864	477.5
966	S492	3850	622.5
967	S493	3836	477.5
968	S494	3822	622.5
969	S495	3808	477.5
970	S496	3794	622.5
971	S497	3780	477.5
972	S498	3766	622.5
973	S499	3752	477.5
974	S500	3738	622.5
975	S501	3724	477.5
976	S502	3710	622.5
977	S503	3696	477.5
978	S504	3682	622.5
979	S505	3668	477.5
980	S506	3654	622.5
981	S507	3640	477.5
982	S508	3626	622.5
983	S509	3612	477.5
984	S510	3598	622.5
985	S511	3584	477.5
986	S512	3570	622.5
987	S513	3556	477.5
988	S514	3542	622.5
989	S515	3528	477.5
990	S516	3514	622.5
991	S517	3500	477.5
992	S518	3486	622.5
993	S519	3472	477.5
994	S520	3458	622.5
995	S521	3444	477.5
996	S522	3430	622.5
997	S523	3416	477.5
998	S524	3402	622.5
999	S525	3388	477.5
1000	S526	3374	622.5
1001	S527	3360	477.5
1002	S528	3346	622.5
1003	S529	3332	477.5
1004	S530	3318	622.5
1005	S531	3304	477.5
1006	S532	3290	622.5
1007	S533	3276	477.5
1008	S534	3262	622.5
1009	S535	3248	477.5
1010	S536	3234	622.5
1011	S537	3220	477.5
1012	S538	3206	622.5
1013	S539	3192	477.5
1014	S540	3178	622.5
1015	S541	3164	477.5
1016	S542	3150	622.5
1017	S543	3136	477.5
1018	S544	3122	622.5
1019	S545	3108	477.5
1020	S546	3094	622.5

No.	Text Name	X-axis	Y-axis
1021	S547	3080	477.5
1022	S548	3066	622.5
1023	S549	3052	477.5
1024	S550	3038	622.5
1025	S551	3024	477.5
1026	S552	3010	622.5
1027	S553	2996	477.5
1028	S554	2982	622.5
1029	S555	2968	477.5
1030	S556	2954	622.5
1031	S557	2940	477.5
1032	S558	2926	622.5
1033	S559	2912	477.5
1034	S560	2898	622.5
1035	S561	2884	477.5
1036	S562	2870	622.5
1037	S563	2856	477.5
1038	S564	2842	622.5
1039	S565	2828	477.5
1040	S566	2814	622.5
1041	S567	2800	477.5
1042	S568	2786	622.5
1043	S569	2772	477.5
1044	S570	2758	622.5
1045	S571	2744	477.5
1046	S572	2730	622.5
1047	S573	2716	477.5
1048	S574	2702	622.5
1049	S575	2688	477.5
1050	S576	2674	622.5
1051	S577	2660	477.5
1052	S578	2646	622.5
1053	S579	2632	477.5
1054	S580	2618	622.5
1055	S581	2604	477.5
1056	S582	2590	622.5
1057	S583	2576	477.5
1058	S584	2562	622.5
1059	S585	2548	477.5
1060	S586	2534	622.5
1061	S587	2520	477.5
1062	S588	2506	622.5
1063	S589	2492	477.5
1064	S590	2478	622.5
1065	S591	2464	477.5
1066	S592	2450	622.5
1067	S593	2436	477.5
1068	S594	2422	622.5
1069	S595	2408	477.5
1070	S596	2394	622.5
1071	S597	2380	477.5
1072	S598	2366	622.5
1073	S599	2352	477.5
1074	S600	2338	622.5
1075	S601	2324	477.5
1076	S602	2310	622.5
1077	S603	2296	477.5
1078	S604	2282	622.5
1079	S605	2268	477.5
1080	S606	2254	622.5

No.	Text Name	X-axis	Y-axis
1081	S607	2240	477.5
1082	S608	2226	622.5
1083	S609	2212	477.5
1084	S610	2198	622.5
1085	S611	2184	477.5
1086	S612	2170	622.5
1087	S613	2156	477.5
1088	S614	2142	622.5
1089	S615	2128	477.5
1090	S616	2114	622.5
1091	S617	2100	477.5
1092	S618	2086	622.5
1093	S619	2072	477.5
1094	S620	2058	622.5
1095	S621	2044	477.5
1096	S622	2030	622.5
1097	S623	2016	477.5
1098	S624	2002	622.5
1099	S625	1988	477.5
1100	S626	1974	622.5
1101	S627	1960	477.5
1102	S628	1946	622.5
1103	S629	1932	477.5
1104	S630	1918	622.5
1105	S631	1904	477.5
1106	S632	1890	622.5
1107	S633	1876	477.5
1108	S634	1862	622.5
1109	S635	1848	477.5
1110	S636	1834	622.5
1111	S637	1820	477.5
1112	S638	1806	622.5
1113	S639	1792	477.5
1114	S640	1778	622.5
1115	S641	1764	477.5
1116	S642	1750	622.5
1117	S643	1736	477.5
1118	S644	1722	622.5
1119	S645	1708	477.5
1120	S646	1694	622.5
1121	S647	1680	477.5
1122	S648	1666	622.5
1123	S649	1652	477.5
1124	S650	1638	622.5
1125	S651	1624	477.5
1126	S652	1610	622.5
1127	S653	1596	477.5
1128	S654	1582	622.5
1129	S655	1568	477.5
1130	S656	1554	622.5
1131	S657	1540	477.5
1132	S658	1526	622.5
1133	S659	1512	477.5
1134	S660	1498	622.5
1135	S661	1484	477.5
1136	S662	1470	622.5
1137	S663	1456	477.5
1138	S664	1442	622.5
1139	S665	1428	477.5
1140	S666	1414	622.5

No.	Text Name	X-axis	Y-axis
1141	S667	1400	477.5
1142	S668	1386	622.5
1143	S669	1372	477.5
1144	S670	1358	622.5
1145	S671	1344	477.5
1146	S672	1330	622.5
1147	S673	1316	477.5
1148	S674	1302	622.5
1149	S675	1288	477.5
1150	S676	1274	622.5
1151	S677	1260	477.5
1152	S678	1246	622.5
1153	S679	1232	477.5
1154	S680	1218	622.5
1155	S681	1204	477.5
1156	S682	1190	622.5
1157	S683	1176	477.5
1158	S684	1162	622.5
1159	S685	1148	477.5
1160	S686	1134	622.5
1161	S687	1120	477.5
1162	S688	1106	622.5
1163	S689	1092	477.5
1164	S690	1078	622.5
1165	S691	1064	477.5
1166	S692	1050	622.5
1167	S693	1036	477.5
1168	S694	1022	622.5
1169	S695	1008	477.5
1170	S696	994	622.5
1171	S697	980	477.5
1172	S698	966	622.5
1173	S699	952	477.5
1174	S700	938	622.5
1175	S701	924	477.5
1176	S702	910	622.5
1177	S703	896	477.5
1178	S704	882	622.5
1179	S705	868	477.5
1180	S706	854	622.5
1181	S707	840	477.5
1182	S708	826	622.5
1183	S709	812	477.5
1184	S710	798	622.5
1185	S711	784	477.5
1186	S712	770	622.5
1187	S713	756	477.5
1188	S714	742	622.5
1189	S715	728	477.5
1190	S716	714	622.5
1191	S717	700	477.5
1192	S718	686	622.5
1193	S719	672	477.5
1194	S720	658	622.5
1195	VSSIDUM9	644	477.5
1196	VSSIDUM10	630	622.5
1197	VSSIDUM11	616	477.5
1198	VSSIDUM12	602	622.5
1199	VSSIDUM13	588	477.5
1200	VSSIDUM14	574	622.5

No.	Text Name	X-axis	Y-axis
1201	VSSIDUM16	546	622.5
1202	VSSIDUM20	490	622.5
1203	VSSIDUM21	476	477.5
1204	VSSIDUM22	462	622.5
1205	VSSIDUM23	448	477.5
1206	VSSIDUM24	434	622.5
1207	VSSIDUM25	420	477.5
1208	VSSIDUM26	406	622.5
1209	VSSIDUM27	392	477.5
1210	VSSIDUM28	378	622.5
1211	VSSIDUM29	364	477.5
1212	VSSIDUM30	350	622.5
1213	VSSIDUM31	336	477.5
1214	VSSIDUM32	322	622.5
1215	VSSIDUM33	308	477.5
1216	VSSIDUM34	294	622.5
1217	VSSIDUM35	280	477.5
1218	VSSIDUM36	266	622.5
1219	VSSIDUM37	252	477.5
1220	VSSIDUM38	238	622.5
1221	VSSIDUM39	224	477.5
1222	VSSIDUM40	210	622.5
1223	VSSIDUM41	196	477.5
1224	VSSIDUM42	182	622.5
1225	VSSIDUM43	168	477.5
1226	VSSIDUM44	154	622.5
1227	VSSIDUM45	140	477.5
1228	VSSIDUM46	126	622.5
1229	VSSIDUM47	112	477.5
1230	VSSIDUM48	98	622.5
1231	VSSIDUM49	84	477.5
1232	VSSIDUM50	70	622.5
1233	VSSIDUM51	56	477.5
1234	VSSIDUM52	42	622.5
1235	VSSIDUM53	28	477.5
1236	VSSIDUM54	14	622.5
1237	VSSIDUM55	0	477.5
1238	VSSIDUM56	-14	622.5
1239	VSSIDUM57	-28	477.5
1240	S721	-42	622.5
1241	S722	-56	477.5
1242	S723	-70	622.5
1243	S724	-84	477.5
1244	S725	-98	622.5
1245	S726	-112	477.5
1246	S727	-126	622.5
1247	S728	-140	477.5
1248	S729	-154	622.5
1249	S730	-168	477.5
1250	S731	-182	622.5
1251	S732	-196	477.5
1252	S733	-210	622.5
1253	S734	-224	477.5
1254	S735	-238	622.5
1255	S736	-252	477.5
1256	S737	-266	622.5
1257	S738	-280	477.5
1258	S739	-294	622.5
1259	S740	-308	477.5
1260	S741	-322	622.5
1261	S742	-336	477.5
1262	S743	-350	622.5
1263	S744	-364	477.5
1264	S745	-378	622.5
1265	S746	-392	477.5
1266	S747	-406	622.5
1267	S748	-420	477.5
1268	S749	-434	622.5
1269	S750	-448	477.5
1270	S751	-462	622.5
1271	S752	-476	477.5
1272	S753	-490	622.5
1273	S754	-504	477.5
1274	S755	-518	622.5
1275	S756	-532	477.5
1276	S757	-546	622.5
1277	S758	-560	477.5
1278	S759	-574	622.5
1279	S760	-588	477.5
1280	S761	-602	622.5
1281	S762	-616	477.5
1282	S763	-630	622.5
1283	S764	-644	477.5
1284	S765	-658	622.5
1285	S766	-672	477.5
1286	S767	-686	622.5
1287	S768	-700	477.5
1288	S769	-714	622.5
1289	S770	-728	477.5
1290	S771	-742	622.5
1291	S772	-756	477.5
1292	S773	-770	622.5
1293	S774	-784	477.5
1294	S775	-798	622.5
1295	S776	-812	477.5
1296	S777	-826	622.5
1297	S778	-840	477.5
1298	S779	-854	622.5
1299	S780	-868	477.5
1300	S781	-882	622.5
1301	S782	-896	477.5
1302	S783	-910	622.5
1303	S784	-924	477.5
1304	S785	-938	622.5
1305	S786	-952	477.5
1306	S787	-966	622.5
1307	S788	-980	477.5
1308	S789	-994	622.5
1309	S790	-1008	477.5
1310	S791	-1022	622.5
1311	S792	-1036	477.5
1312	S793	-1050	622.5
1313	S794	-1064	477.5
1314	S795	-1078	622.5
1315	S796	-1092	477.5
1316	S797	-1106	622.5
1317	S798	-1120	477.5
1318	S799	-1134	622.5
1319	S800	-1148	477.5
1320	S801	-1162	622.5
1321	S802	-1176	477.5
1322	S803	-1190	622.5
1323	S804	-1204	477.5
1324	S805	-1218	622.5
1325	S806	-1232	477.5
1326	S807	-1246	622.5
1327	S808	-1260	477.5
1328	S809	-1274	622.5
1329	S810	-1288	477.5
1330	S811	-1302	622.5
1331	S812	-1316	477.5
1332	S813	-1330	622.5
1333	S814	-1344	477.5
1334	S815	-1358	622.5
1335	S816	-1372	477.5
1336	S817	-1386	622.5
1337	S818	-1400	477.5
1338	S819	-1414	622.5
1339	S820	-1428	477.5
1340	S821	-1442	622.5
1341	S822	-1456	477.5
1342	S823	-1470	622.5
1343	S824	-1484	477.5
1344	S825	-1498	622.5
1345	S826	-1512	477.5
1346	S827	-1526	622.5
1347	S828	-1540	477.5
1348	S829	-1554	622.5
1349	S830	-1568	477.5
1350	S831	-1582	622.5
1351	S832	-1596	477.5
1352	S833	-1610	622.5
1353	S834	-1624	477.5
1354	S835	-1638	622.5
1355	S836	-1652	477.5
1356	S837	-1666	622.5
1357	S838	-1680	477.5
1358	S839	-1694	622.5
1359	S840	-1708	477.5
1360	S841	-1722	622.5
1361	S842	-1736	477.5
1362	S843	-1750	622.5
1363	S844	-1764	477.5
1364	S845	-1778	622.5
1365	S846	-1792	477.5
1366	S847	-1806	622.5
1367	S848	-1820	477.5
1368	S849	-1834	622.5
1369	S850	-1848	477.5
1370	S851	-1862	622.5
1371	S852	-1876	477.5
1372	S853	-1890	622.5
1373	S854	-1904	477.5
1374	S855	-1918	622.5
1375	S856	-1932	477.5
1376	S857	-1946	622.5
1377	S858	-1960	477.5
1378	S859	-1974	622.5
1379	S860	-1988	477.5
1380	S861	-2002	622.5
1381	S862	-2016	477.5
1382	S863	-2030	622.5
1383	S864	-2044	477.5
1384	S865	-2058	622.5
1385	S866	-2072	477.5
1386	S867	-2086	622.5
1387	S868	-2100	477.5
1388	S869	-2114	622.5
1389	S870	-2128	477.5
1390	S871	-2142	622.5
1391	S872	-2156	477.5
1392	S873	-2170	622.5
1393	S874	-2184	477.5
1394	S875	-2198	622.5
1395	S876	-2212	477.5
1396	S877	-2226	622.5
1397	S878	-2240	477.5
1398	S879	-2254	622.5
1399	S880	-2268	477.5
1400	S881	-2282	622.5
1401	S882	-2296	477.5
1402	S883	-2310	622.5
1403	S884	-2324	477.5
1404	S885	-2338	622.5
1405	S886	-2352	477.5
1406	S887	-2366	622.5
1407	S888	-2380	477.5
1408	S889	-2394	622.5
1409	S890	-2408	477.5
1410	S891	-2422	622.5
1411	S892	-2436	477.5
1412	S893	-2450	622.5
1413	S894	-2464	477.5
1414	S895	-2478	622.5
1415	S896	-2492	477.5
1416	S897	-2506	622.5
1417	S898	-2520	477.5
1418	S899	-2534	622.5
1419	S900	-2548	477.5
1420	S901	-2562	622.5
1421	S902	-2576	477.5
1422	S903	-2590	622.5
1423	S904	-2604	477.5
1424	S905	-2618	622.5
1425	S906	-2632	477.5
1426	S907	-2646	622.5
1427	S908	-2660	477.5
1428	S909	-2674	622.5
1429	S910	-2688	477.5
1430	S911	-2702	622.5
1431	S912	-2716	477.5
1432	S913	-2730	622.5
1433	S914	-2744	477.5
1434	S915	-2758	622.5
1435	S916	-2772	477.5
1436	S917	-2786	622.5
1437	S918	-2800	477.5
1438	S919	-2814	622.5
1439	S920	-2828	477.5
1440	S921	-2842	622.5

No.	Text Name	X-axis	Y-axis
1441	S922	-2856	477.5
1442	S923	-2870	622.5
1443	S924	-2884	477.5
1444	S925	-2898	622.5
1445	S926	-2912	477.5
1446	S927	-2926	622.5
1447	S928	-2940	477.5
1448	S929	-2954	622.5
1449	S930	-2968	477.5
1450	S931	-2982	622.5
1451	S932	-2996	477.5
1452	S933	-3010	622.5
1453	S934	-3024	477.5
1454	S935	-3038	622.5
1455	S936	-3052	477.5
1456	S937	-3066	622.5
1457	S938	-3080	477.5
1458	S939	-3094	622.5
1459	S940	-3108	477.5
1460	S941	-3122	622.5
1461	S942	-3136	477.5
1462	S943	-3150	622.5
1463	S944	-3164	477.5
1464	S945	-3178	622.5
1465	S946	-3192	477.5
1466	S947	-3206	622.5
1467	S948	-3220	477.5
1468	S949	-3234	622.5
1469	S950	-3248	477.5
1470	S951	-3262	622.5
1471	S952	-3276	477.5
1472	S953	-3290	622.5
1473	S954	-3304	477.5
1474	S955	-3318	622.5
1475	S956	-3332	477.5
1476	S957	-3346	622.5
1477	S958	-3360	477.5
1478	S959	-3374	622.5
1479	S960	-3388	477.5
1480	S961	-3402	622.5
1481	S962	-3416	477.5
1482	S963	-3430	622.5
1483	S964	-3444	477.5
1484	S965	-3458	622.5
1485	S966	-3472	477.5
1486	S967	-3486	622.5
1487	S968	-3500	477.5
1488	S969	-3514	622.5
1489	S970	-3528	477.5
1490	S971	-3542	622.5
1491	S972	-3556	477.5
1492	S973	-3570	622.5
1493	S974	-3584	477.5
1494	S975	-3598	622.5
1495	S976	-3612	477.5
1496	S977	-3626	622.5
1497	S978	-3640	477.5
1498	S979	-3654	622.5
1499	S980	-3668	477.5
1500	S981	-3682	622.5

No.	Text Name	X-axis	Y-axis
1501	S982	-3696	477.5
1502	S983	-3710	622.5
1503	S984	-3724	477.5
1504	S985	-3738	622.5
1505	S986	-3752	477.5
1506	S987	-3766	622.5
1507	S988	-3780	477.5
1508	S989	-3794	622.5
1509	S990	-3808	477.5
1510	S991	-3822	622.5
1511	S992	-3836	477.5
1512	S993	-3850	622.5
1513	S994	-3864	477.5
1514	S995	-3878	622.5
1515	S996	-3892	477.5
1516	S997	-3906	622.5
1517	S998	-3920	477.5
1518	S999	-3934	622.5
1519	S1000	-3948	477.5
1520	S1001	-3962	622.5
1521	S1002	-3976	477.5
1522	S1003	-3990	622.5
1523	S1004	-4004	477.5
1524	S1005	-4018	622.5
1525	S1006	-4032	477.5
1526	S1007	-4046	622.5
1527	S1008	-4060	477.5
1528	S1009	-4074	622.5
1529	S1010	-4088	477.5
1530	S1011	-4102	622.5
1531	S1012	-4116	477.5
1532	S1013	-4130	622.5
1533	S1014	-4144	477.5
1534	S1015	-4158	622.5
1535	S1016	-4172	477.5
1536	S1017	-4186	622.5
1537	S1018	-4200	477.5
1538	S1019	-4214	622.5
1539	S1020	-4228	477.5
1540	S1021	-4242	622.5
1541	S1022	-4256	477.5
1542	S1023	-4270	622.5
1543	S1024	-4284	477.5
1544	S1025	-4298	622.5
1545	S1026	-4312	477.5
1546	S1027	-4326	622.5
1547	S1028	-4340	477.5
1548	S1029	-4354	622.5
1549	S1030	-4368	477.5
1550	S1031	-4382	622.5
1551	S1032	-4396	477.5
1552	S1033	-4410	622.5
1553	S1034	-4424	477.5
1554	S1035	-4438	622.5
1555	S1036	-4452	477.5
1556	S1037	-4466	622.5
1557	S1038	-4480	477.5
1558	S1039	-4494	622.5
1559	S1040	-4508	477.5
1560	S1041	-4522	622.5

No.	Text Name	X-axis	Y-axis
1561	S1042	-4536	477.5
1562	S1043	-4550	622.5
1563	S1044	-4564	477.5
1564	S1045	-4578	622.5
1565	S1046	-4592	477.5
1566	S1047	-4606	622.5
1567	S1048	-4620	477.5
1568	S1049	-4634	622.5
1569	S1050	-4648	477.5
1570	S1051	-4662	622.5
1571	S1052	-4676	477.5
1572	S1053	-4690	622.5
1573	S1054	-4704	477.5
1574	S1055	-4718	622.5
1575	S1056	-4732	477.5
1576	S1057	-4746	622.5
1577	S1058	-4760	477.5
1578	S1059	-4774	622.5
1579	S1060	-4788	477.5
1580	S1061	-4802	622.5
1581	S1062	-4816	477.5
1582	S1063	-4830	622.5
1583	S1064	-4844	477.5
1584	S1065	-4858	622.5
1585	S1066	-4872	477.5
1586	S1067	-4886	622.5
1587	S1068	-4900	477.5
1588	S1069	-4914	622.5
1589	S1070	-4928	477.5
1590	S1071	-4942	622.5
1591	S1072	-4956	477.5
1592	S1073	-4970	622.5
1593	S1074	-4984	477.5
1594	S1075	-4998	622.5
1595	S1076	-5012	477.5
1596	S1077	-5026	622.5
1597	S1078	-5040	477.5
1598	S1079	-5054	622.5
1599	S1080	-5068	477.5
1600	S1081	-5082	622.5
1601	S1082	-5096	477.5
1602	S1083	-5110	622.5
1603	S1084	-5124	477.5
1604	S1085	-5138	622.5
1605	S1086	-5152	477.5
1606	S1087	-5166	622.5
1607	S1088	-5180	477.5
1608	S1089	-5194	622.5
1609	S1090	-5208	477.5
1610	S1091	-5222	622.5
1611	S1092	-5236	477.5
1612	S1093	-5250	622.5
1613	S1094	-5264	477.5
1614	S1095	-5278	622.5
1615	S1096	-5292	477.5
1616	S1097	-5306	622.5
1617	S1098	-5320	477.5
1618	S1099	-5334	622.5
1619	S1100	-5348	477.5
1620	S1101	-5362	622.5

No.	Text Name	X-axis	Y-axis
1621	S1102	-5376	477.5
1622	S1103	-5390	622.5
1623	S1104	-5404	477.5
1624	S1105	-5418	622.5
1625	S1106	-5432	477.5
1626	S1107	-5446	622.5
1627	S1108	-5460	477.5
1628	S1109	-5474	622.5
1629	S1110	-5488	477.5
1630	S1111	-5502	622.5
1631	S1112	-5516	477.5
1632	S1113	-5530	622.5
1633	S1114	-5544	477.5
1634	S1115	-5558	622.5
1635	S1116	-5572	477.5
1636	S1117	-5586	622.5
1637	S1118	-5600	477.5
1638	S1119	-5614	622.5
1639	S1120	-5628	477.5
1640	S1121	-5642	622.5
1641	S1122	-5656	477.5
1642	S1123	-5670	622.5
1643	S1124	-5684	477.5
1644	S1125	-5698	622.5
1645	S1126	-5712	477.5
1646	S1127	-5726	622.5
1647	S1128	-5740	477.5
1648	S1129	-5754	622.5
1649	S1130	-5768	477.5
1650	S1131	-5782	622.5
1651	S1132	-5796	477.5
1652	S1133	-5810	622.5
1653	S1134	-5824	477.5
1654	S1135	-5838	622.5
1655	S1136	-5852	477.5
1656	S1137	-5866	622.5
1657	S1138	-5880	477.5
1658	S1139	-5894	622.5
1659	S1140	-5908	477.5
1660	S1141	-5922	622.5
1661	S1142	-5936	477.5
1662	S1143	-5950	622.5
1663	S1144	-5964	477.5
1664	S1145	-5978	622.5
1665	S1146	-5992	477.5
1666	S1147	-6006	622.5
1667	S1148	-6020	477.5
1668	S1149	-6034	622.5
1669	S1150	-6048	477.5
1670	S1151	-6062	622.5
1671	S1152	-6076	477.5
1672	S1153	-6090	622.5
1673	S1154	-6104	477.5
1674	S1155	-6118	622.5
1675	S1156	-6132	477.5
1676	S1157	-6146	622.5
1677	S1158	-6160	477.5
1678	S1159	-6174	622.5
1679	S1160	-6188	477.5
1680	S1161	-6202	622.5

No.	Text Name	X-axis	Y-axis
1681	S1162	-6216	477.5
1682	S1163	-6230	622.5
1683	S1164	-6244	477.5
1684	S1165	-6258	622.5
1685	S1166	-6272	477.5
1686	S1167	-6286	622.5
1687	S1168	-6300	477.5
1688	S1169	-6314	622.5
1689	S1170	-6328	477.5
1690	S1171	-6342	622.5
1691	S1172	-6356	477.5
1692	S1173	-6370	622.5
1693	S1174	-6384	477.5
1694	S1175	-6398	622.5
1695	S1176	-6412	477.5
1696	S1177	-6426	622.5
1697	S1178	-6440	477.5
1698	S1179	-6454	622.5
1699	S1180	-6468	477.5
1700	S1181	-6482	622.5
1701	S1182	-6496	477.5
1702	S1183	-6510	622.5
1703	S1184	-6524	477.5
1704	S1185	-6538	622.5
1705	S1186	-6552	477.5
1706	S1187	-6566	622.5
1707	S1188	-6580	477.5
1708	S1189	-6594	622.5
1709	S1190	-6608	477.5
1710	S1191	-6622	622.5
1711	S1192	-6636	477.5
1712	S1193	-6650	622.5
1713	S1194	-6664	477.5
1714	S1195	-6678	622.5
1715	S1196	-6692	477.5
1716	S1197	-6706	622.5
1717	S1198	-6720	477.5
1718	S1199	-6734	622.5
1719	S1200	-6748	477.5
1720	S1201	-6762	622.5
1721	S1202	-6776	477.5
1722	S1203	-6790	622.5
1723	S1204	-6804	477.5
1724	S1205	-6818	622.5
1725	S1206	-6832	477.5
1726	S1207	-6846	622.5
1727	S1208	-6860	477.5
1728	S1209	-6874	622.5
1729	S1210	-6888	477.5
1730	S1211	-6902	622.5
1731	S1212	-6916	477.5
1732	S1213	-6930	622.5
1733	S1214	-6944	477.5
1734	S1215	-6958	622.5
1735	S1216	-6972	477.5
1736	S1217	-6986	622.5
1737	S1218	-7000	477.5
1738	S1219	-7014	622.5
1739	S1220	-7028	477.5
1740	S1221	-7042	622.5

No.	Text Name	X-axis	Y-axis
1741	S1222	-7056	477.5
1742	S1223	-7070	622.5
1743	S1224	-7084	477.5
1744	S1225	-7098	622.5
1745	S1226	-7112	477.5
1746	S1227	-7126	622.5
1747	S1228	-7140	477.5
1748	S1229	-7154	622.5
1749	S1230	-7168	477.5
1750	S1231	-7182	622.5
1751	S1232	-7196	477.5
1752	S1233	-7210	622.5
1753	S1234	-7224	477.5
1754	S1235	-7238	622.5
1755	S1236	-7252	477.5
1756	S1237	-7266	622.5
1757	S1238	-7280	477.5
1758	S1239	-7294	622.5
1759	S1240	-7308	477.5
1760	S1241	-7322	622.5
1761	S1242	-7336	477.5
1762	S1243	-7350	622.5
1763	S1244	-7364	477.5
1764	S1245	-7378	622.5
1765	S1246	-7392	477.5
1766	S1247	-7406	622.5
1767	S1248	-7420	477.5
1768	S1249	-7434	622.5
1769	S1250	-7448	477.5
1770	S1251	-7462	622.5
1771	S1252	-7476	477.5
1772	S1253	-7490	622.5
1773	S1254	-7504	477.5
1774	S1255	-7518	622.5
1775	S1256	-7532	477.5
1776	S1257	-7546	622.5
1777	S1258	-7560	477.5
1778	S1259	-7574	622.5
1779	S1260	-7588	477.5
1780	S1261	-7602	622.5
1781	S1262	-7616	477.5
1782	S1263	-7630	622.5
1783	S1264	-7644	477.5
1784	S1265	-7658	622.5
1785	S1266	-7672	477.5
1786	S1267	-7686	622.5
1787	S1268	-7700	477.5
1788	S1269	-7714	622.5
1789	S1270	-7728	477.5
1790	S1271	-7742	622.5
1791	S1272	-7756	477.5
1792	S1273	-7770	622.5
1793	S1274	-7784	477.5
1794	S1275	-7798	622.5
1795	S1276	-7812	477.5
1796	S1277	-7826	622.5
1797	S1278	-7840	477.5
1798	S1279	-7854	622.5
1799	S1280	-7868	477.5
1800	S1281	-7882	622.5

No.	Text Name	X-axis	Y-axis
1801	S1282	-7896	477.5
1802	S1283	-7910	622.5
1803	S1284	-7924	477.5
1804	S1285	-7938	622.5
1805	S1286	-7952	477.5
1806	S1287	-7966	622.5
1807	S1288	-7980	477.5
1808	S1289	-7994	622.5
1809	S1290	-8008	477.5
1810	S1291	-8022	622.5
1811	S1292	-8036	477.5
1812	S1293	-8050	622.5
1813	S1294	-8064	477.5
1814	S1295	-8078	622.5
1815	S1296	-8092	477.5
1816	S1297	-8106	622.5
1817	S1298	-8120	477.5
1818	S1299	-8134	622.5
1819	S1300	-8148	477.5
1820	S1301	-8162	622.5
1821	S1302	-8176	477.5
1822	S1303	-8190	622.5
1823	S1304	-8204	477.5
1824	S1305	-8218	622.5
1825	S1306	-8232	477.5
1826	S1307	-8246	622.5
1827	S1308	-8260	477.5
1828	S1309	-8274	622.5
1829	S1310	-8288	477.5
1830	S1311	-8302	622.5
1831	S1312	-8316	477.5
1832	S1313	-8330	622.5
1833	S1314	-8344	477.5
1834	S1315	-8358	622.5
1835	S1316	-8372	477.5
1836	S1317	-8386	622.5
1837	S1318	-8400	477.5
1838	S1319	-8414	622.5
1839	S1320	-8428	477.5
1840	S1321	-8442	622.5
1841	S1322	-8456	477.5
1842	S1323	-8470	622.5
1843	S1324	-8484	477.5
1844	S1325	-8498	622.5
1845	S1326	-8512	477.5
1846	S1327	-8526	622.5
1847	S1328	-8540	477.5
1848	S1329	-8554	622.5
1849	S1330	-8568	477.5
1850	S1331	-8582	622.5
1851	S1332	-8596	477.5
1852	S1333	-8610	622.5
1853	S1334	-8624	477.5
1854	S1335	-8638	622.5
1855	S1336	-8652	477.5
1856	S1337	-8666	622.5
1857	S1338	-8680	477.5
1858	S1339	-8694	622.5
1859	S1340	-8708	477.5
1860	S1341	-8722	622.5

No.	Text Name	X-axis	Y-axis
1861	S1342	-8736	477.5
1862	S1343	-8750	622.5
1863	S1344	-8764	477.5
1864	S1345	-8778	622.5
1865	S1346	-8792	477.5
1866	S1347	-8806	622.5
1867	S1348	-8820	477.5
1868	S1349	-8834	622.5
1869	S1350	-8848	477.5
1870	S1351	-8862	622.5
1871	S1352	-8876	477.5
1872	S1353	-8890	622.5
1873	S1354	-8904	477.5
1874	S1355	-8918	622.5
1875	S1356	-8932	477.5
1876	S1357	-8946	622.5
1877	S1358	-8960	477.5
1878	S1359	-8974	622.5
1879	S1360	-8988	477.5
1880	S1361	-9002	622.5
1881	S1362	-9016	477.5
1882	S1363	-9030	622.5
1883	S1364	-9044	477.5
1884	S1365	-9058	622.5
1885	S1366	-9072	477.5
1886	S1367	-9086	622.5
1887	S1368	-9100	477.5
1888	S1369	-9114	622.5
1889	S1370	-9128	477.5
1890	S1371	-9142	622.5
1891	S1372	-9156	477.5
1892	S1373	-9170	622.5
1893	S1374	-9184	477.5
1894	S1375	-9198	622.5
1895	S1376	-9212	477.5
1896	S1377	-9226	622.5
1897	S1378	-9240	477.5
1898	S1379	-9254	622.5
1899	S1380	-9268	477.5
1900	S1381	-9282	622.5
1901	S1382	-9296	477.5
1902	S1383	-9310	622.5
1903	S1384	-9324	477.5
1904	S1385	-9338	622.5
1905	S1386	-9352	477.5
1906	S1387	-9366	622.5
1907	S1388	-9380	477.5
1908	S1389	-9394	622.5
1909	S1390	-9408	477.5
1910	S1391	-9422	622.5
1911	S1392	-9436	477.5
1912	S1393	-9450	622.5
1913	S1394	-9464	477.5
1914	S1395	-9478	622.5
1915	S1396	-9492	477.5
1916	S1397	-9506	622.5
1917	S1398	-9520	477.5
1918	S1399	-9534	622.5
1919	S1400	-9548	477.5
1920	S1401	-9562	622.5

No.	Text Name	X-axis	Y-axis
1921	S1402	-9576	477.5
1922	S1403	-9590	622.5
1923	S1404	-9604	477.5
1924	S1405	-9618	622.5
1925	S1406	-9632	477.5
1926	S1407	-9646	622.5
1927	S1408	-9660	477.5
1928	S1409	-9674	622.5
1929	S1410	-9688	477.5
1930	S1411	-9702	622.5
1931	S1412	-9716	477.5
1932	S1413	-9730	622.5
1933	S1414	-9744	477.5
1934	S1415	-9758	622.5
1935	S1416	-9772	477.5
1936	S1417	-9786	622.5
1937	S1418	-9800	477.5
1938	S1419	-9814	622.5
1939	S1420	-9828	477.5
1940	S1421	-9842	622.5
1941	S1422	-9856	477.5
1942	S1423	-9870	622.5
1943	S1424	-9884	477.5
1944	S1425	-9898	622.5
1945	S1426	-9912	477.5
1946	S1427	-9926	622.5
1947	S1428	-9940	477.5
1948	S1429	-9954	622.5
1949	S1430	-9968	477.5
1950	S1431	-9982	622.5
1951	S1432	-9996	477.5
1952	S1433	-10010	622.5
1953	S1434	-10024	477.5
1954	S1435	-10038	622.5
1955	S1436	-10052	477.5
1956	S1437	-10066	622.5
1957	S1438	-10080	477.5
1958	S1439	-10094	622.5
1959	S1440	-10108	477.5
1960	SDUM2	-10122	622.5
1961	SDUM3	-10136	477.5
1962	VSSIDUM58	-10150	622.5
1963	VSSIDUM59	-10164	477.5
1964	VGLO_L	-10178	622.5
1965	VGLO_L	-10192	477.5
1966	VGLO_L	-10206	622.5
1967	VGLO_L	-10220	477.5
1968	VGLO_L	-10234	622.5
1969	VGLO_L	-10248	477.5
1970	VGLO_L	-10262	622.5
1971	VGLO_L	-10276	477.5
1972	VGLO_L	-10290	622.5
1973	VGH	-10304	477.5
1974	VGH	-10318	622.5
1975	VGH	-10332	477.5
1976	VGH	-10346	622.5
1977	VGH	-10360	477.5
1978	VGH	-10374	622.5
1979	VGH	-10388	477.5
1980	VGH	-10402	622.5

No.	Text Name	X-axis	Y-axis
1981	VSSIDUM60	-10416	477.5
1982	VSSIDUM61	-10430	622.5
1983	VSSIDUM62	-10444	477.5
1984	VSSIDUM63	-10458	622.5
1985	VSSIDUM64	-10472	477.5
1986	VSSIDUM65	-10486	622.5
1987	VSSIDUM66	-10500	477.5
1988	VSSIDUM67	-10514	622.5
1989	VSSIDUM68	-10528	477.5
1990	VSSIDUM69	-10542	622.5
1991	VSSIDUM70	-10556	477.5
1992	VSSIDUM71	-10570	622.5
1993	VSSIDUM72	-10584	477.5
1994	VSSIDUM73	-10598	622.5
1995	VSSIDUM74	-10612	477.5
1996	VSSIDUM75	-10626	622.5
1997	VSSIDUM76	-10640	477.5
1998	VSSIDUM77	-10654	622.5
1999	VSSIDUM78	-10668	477.5
2000	VSSIDUM79	-10682	622.5
2001	VSSIDUM80	-10696	477.5
2002	VSSIDUM81	-10710	622.5
2003	VSSIDUM82	-10724	477.5
2004	VSSIDUM83	-10738	622.5
2005	VSSIDUM84	-10752	477.5
2006	VSSIDUM85	-10766	622.5
2007	VSSIDUM86	-10780	477.5
2008	VSSIDUM87	-10794	622.5
2009	VSSIDUM88	-10808	477.5
2010	VSSIDUM89	-10822	622.5
2011	VSSIDUM90	-10836	477.5
2012	VSSIDUM91	-10850	622.5
2013	VSSIDUM92	-10864	477.5
2014	VSSIDUM93	-10878	622.5
2015	VSSIDUM94	-10892	477.5
2016	VSSIDUM95	-10906	622.5
2017	VSSIDUM96	-10920	477.5
2018	VSSIDUM97	-10934	622.5
2019	VSSIDUM98	-10948	477.5
2020	VSSIDUM99	-10962	622.5
2021	VSSIDUM100	-10976	477.5
2022	VSSIDUM101	-10990	622.5
2023	VSSIDUM102	-11004	477.5
2024	VSSIDUM103	-11018	622.5
2025	GOUT17	-11032	477.5
2026	GOUT17	-11046	622.5
2027	GOUT18	-11060	477.5
2028	GOUT18	-11074	622.5
2029	GOUT19	-11088	477.5
2030	GOUT19	-11102	622.5
2031	GOUT20	-11116	477.5
2032	GOUT20	-11130	622.5
2033	GOUT21	-11144	477.5
2034	GOUT21	-11158	622.5
2035	GOUT22	-11172	477.5
2036	GOUT22	-11186	622.5
2037	GOUT23	-11200	477.5
2038	GOUT23	-11214	622.5
2039	GOUT24	-11228	477.5
2040	GOUT24	-11242	622.5

No.	Text Name	X-axis	Y-axis
2041	GOUT25	-11256	477.5
2042	GOUT25	-11270	622.5
2043	GOUT26	-11284	477.5
2044	GOUT26	-11298	622.5
2045	GOUT27	-11312	477.5
2046	GOUT27	-11326	622.5
2047	GOUT28	-11340	477.5
2048	GOUT28	-11354	622.5
2049	GOUT29	-11368	477.5
2050	GOUT29	-11382	622.5
2051	GOUT30	-11396	477.5
2052	GOUT30	-11410	622.5
2053	VGLO_L	-11424	477.5
2054	VGLO_L	-11438	622.5
2055	VGLO_L	-11452	477.5
2056	VRGH_L	-11466	622.5
2057	VRGH_L	-11480	477.5
2058	VRGH_L	-11494	622.5
2059	LVGL_L	-11508	477.5
2060	LVGL_L	-11522	622.5
2061	LVGL_L	-11536	477.5
2062	GOUT31	-11550	622.5
2063	GOUT31	-11564	477.5
2064	GOUT32	-11578	622.5
2065	GOUT32	-11592	477.5
2066	VGLO_L	-11606	622.5
2067	VGLO_L	-11620	477.5
2068	VGLO_L	-11634	622.5
2069	VGH	-11648	477.5
2070	VGH	-11662	622.5
2071	VGH	-11676	477.5
2072	PADA4	-11690	622.5
2073	PADB4	-11704	477.5
2074	VSSIDUM104	-11718	622.5
2075	VSSIDUM105	-11732	477.5
2076	VSSIDUM106	-11760	622.5
2077	DUMMY	-11998	622.5
2078	DUMMY	-12012	477.5
2079	DUMMY	-12026	622.5
2080	DUMMY	-12040	477.5
2081	DUMMY	-12054	622.5

Alignment Mark	X-axis	Y-axis
ALMART_R_T	11870	605
ALMART_L_T	-11870	605

System Interface

3.7. DBI Type B Parallel Interface

The ILI9806 supports an 8-/9-/16-/18-/24-bit MPU DBI Type B parallel interface. The chip-select CSX (active low) is used to enable or disable the ILI9806 chip. The RESX (active low) is an external reset signal, the WRX is parallel data write strobe, the RDX is parallel data read strobe, and DB [23:0] is parallel data bus.

The ILI9806 latches the input data at the rising edge of the WRX signal. The DCX is the signal for data/command selection. When DCX = 1, DB [23:0] bits are RAM data or command parameters. When DCX = 0, DB [23:0] bits are commands. The DBI Type B bi-directional interface is used for communication between the MPU controller and LCD driver chip. The selection of the parallel interface is shown in Table 8.

Table 8: DBI Type B Parallel Interface

IM3	IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	DCX	Function
0	0	0	0	DBI Type B 8-bit bus interface	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	DBI Type B 16-bit bus interface	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
0	0	1	0	DBI Type B 24-bit bus interface	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
1	1	0	0	DBI Type B 9-bit bus interface	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.
1	1	0	1	DBI Type B 18-bit bus interface	↑	"H"	"L"	Write command code.
					"H"	↑	"H"	Read internal status.
					↑	"H"	"H"	Write parameter or display data.
					"H"	↑	"H"	Reads parameter or display data.

3.7.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information while the display module captures the information from the host processor on the rising edge of the WRX. When the DCX signal is driven to low level, the input data on the interface is interpreted as command information. The DCX signal can also be pulled to high level when the data is RAM data or command parameter.

Figure 2 shows the write cycle of the DBI Type B interface.

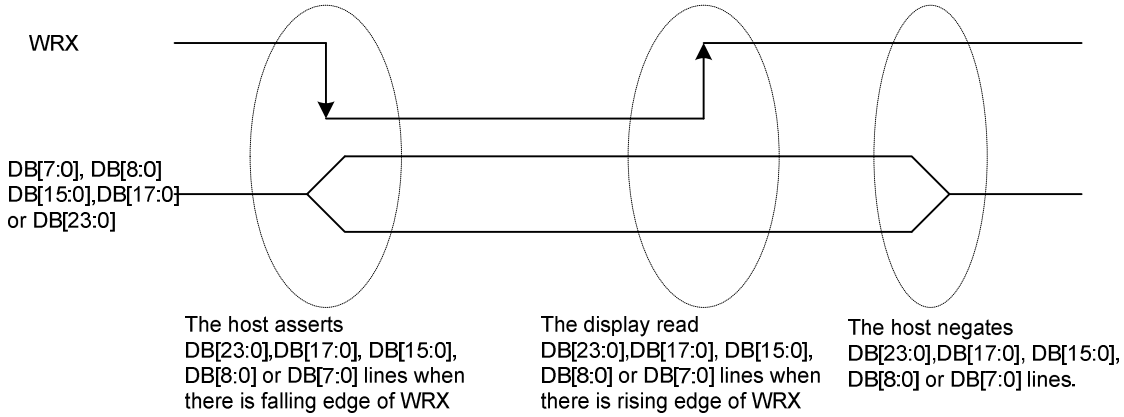


Figure 2: DBI Type B Write Cycle[Note]

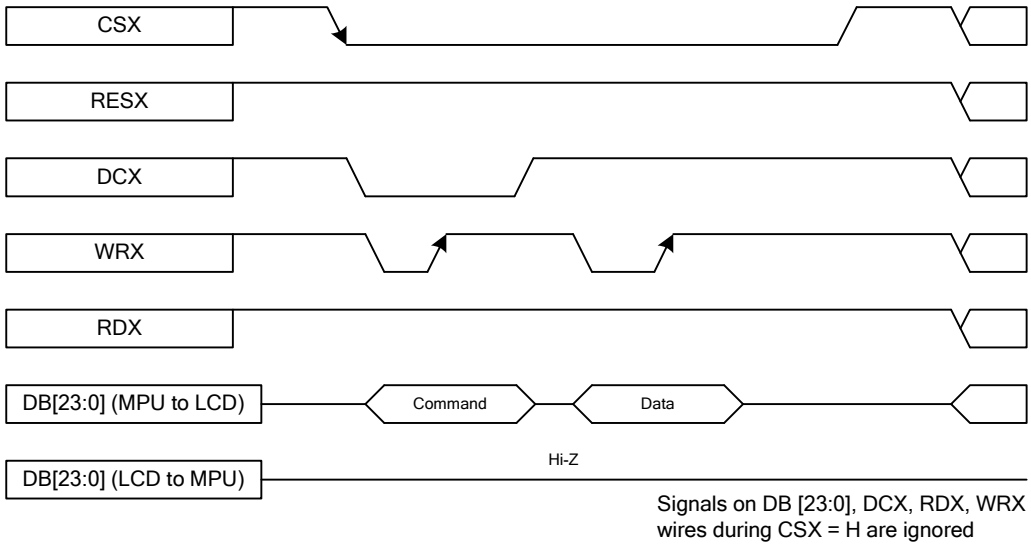


Figure 3: DBI Type B Write Cycle Sequence

Note WRX is an unsynchronized signal, which can be terminated when not in use.

3.7.2. Read Cycle Sequence

The RDX signal is driven from high to low and then pulled back to high during the read cycle. The display module provides information to the host processor while the host processor reads the display module information on the rising edge of the RDX signal. When the DCX signal is driven to the low level, the input data on the interface is interpreted as internal status or parameter data. The DCX signal also can be pulled to high level when the data on the interface is RAM data or a command parameter data.

The following figure shows a read cycle of the DBI Type B interface.

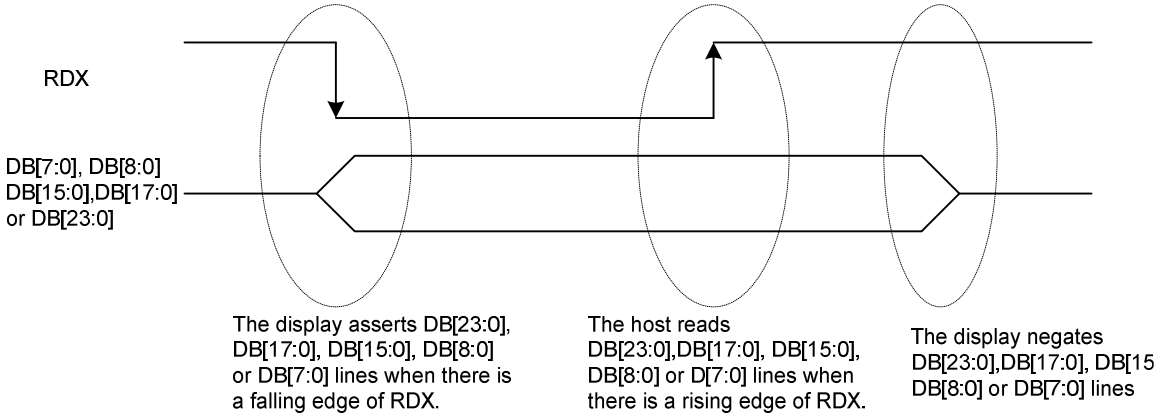


Figure 4: DBI Type B Read Cycle[Note 1]

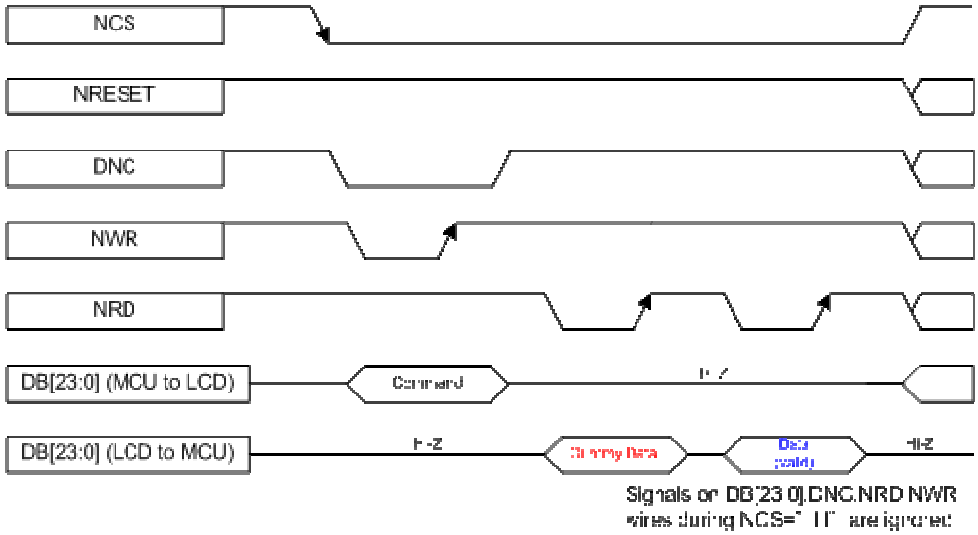


Figure 5: DBI Type B Read Cycle Sequence[Note 2]

Note 1 *RDX is an unsynchronized signal, which can be terminated when not in use.*

Note 2 *Read Data is only valid when the DCX input is pulled high. If the DCX signal is driven low during the read cycle then the display information outputs will be High-Z.*

3.7.3. DBI Type B Interface Set Table

24-bit data bus DB [23:0] interface, IM [3:0] = 0010

	Register	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch																	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh																	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
24bpp Frame Memory Write	3'h7	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	r[7]	r[6]	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[7]	g[6]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[7]	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

Figure 6: DBI Type B 24-bit Data Bus

18-bit data bus DB [17:0] interface, IM [3:0] = 1101

	Register	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h5			R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

	Set_pixel_format	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer			Second Transfer			Third Transfer		
18bpp Frame Memory Write	Set_pixel_format	DB[17:10]	DB[9:8]	DB[7:0]	DB[17:10]	DB[9:8]	DB[7:0]	DB[17:10]	DB[9:8]	DB[7:0]
	3'h7	R1[7:0]		G1[7:0]	B1[7:0]		R2[7:0]	G2[7:0]		B2[7:0]
Frame Memory Read	*	r1[7:0]		g1[7:0]	b1[7:0]		r2[7:0]	g2[7:0]		b2[7:0]

Figure 7: DBI Type B 18-bit Data Bus

16-bit data bus DB [15:0] interface, IM [3:0] = 0001

	Set_pixel_format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer				Second Transfer				Third Transfer			
16bpp Frame Memory Write	Set_pixel_format	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
	3'h6	R1[5:0]		G1[5:0]		B1[5:0]		R2[5:0]		G2[5:0]		B2[5:0]	

		First Transfer		Second Transfer		Third Transfer	
16bpp Frame Memory Write	Set_pixel_format	DB[15:8]	DB[7:0]	DB[15:8]	DB[7:0]	DB[15:8]	DB[7:0]
	3'h7	R1[7:0]	G1[7:0]	B1[7:0]	R2[7:0]	G2[7:0]	B2[7:0]
Frame Memory Read	*	r1[7:0]	g1[7:0]	b1[7:0]	r2[7:0]	g2[7:0]	b2[7:0]

Figure 8: DBI Type B 16-bit Data Bus

9-bit data bus DB [8:0] interface, IM [3:0] = 1100

	Register	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

		First Transfer									Second Transfer								
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]		G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

		First Transfer									Second Transfer								
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer									Second Transfer									Third Transfer								
9bpp Frame Memory Write	Set_pixel_format	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h7	R1[7:0]									G1[7:0]									B1[7:0]								
Frame Memory Read	*	r1[7:0]									g1[7:0]									b1[7:0]								

Figure 9: DBI Type B 9-bit Data Bus

8-bit data bus DB [7:0] interface, IM [3:0] = 0000

	Register	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	2Ch / 3Ch	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	2Eh / 3Eh	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

		First Transfer								Second Transfer							
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h5	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

		First Transfer								Second Transfer								Third Transfer							
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h6	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		

		First Transfer								Second Transfer								Third Transfer							
8bpp Frame Memory Write	Set_pixel_format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	3'h7	R1[7:0]								G1[7:0]								B1[7:0]							
Frame Memory Read	*	r1[7:0]								g1[7:0]								b1[7:0]							

Figure 10: DBI Type B 8-bit Data Bus

3.8. DBI Type C Serial Interface

The selection of this interface is done by the IM [3:0] pins. See Table 9.

Table 9: DBI Type C Serial Interface

IM3	IM2	IM1	IM0	DBI Type C Mode	CSX	SDA	SCL	Function
X	0	1	1	3-line serial interface	"L"	-	↑	Read/Write command, parameter or display data.

The ILI9806 uses a 3-line 9-bit serial interface for communication between the host and the ILI9806. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL), and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the DPI interface data transfer, the unused pins are unaffected. The Serial clock (SCL) is used only for the interface with the MPU, so it can be stopped when no communication is necessary.

3.8.1. Write Cycle Sequence

In the Write Mode of the interface, the host writes commands and data to the ILI9806. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is "low", the transmission byte is interpreted as a command byte. If the D/C bit is "high", the transmission byte is stored in the GRAM as display data, or stored in the command register as a parameter data.

Any instruction can be sent in any order to the ILI9806 and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See below for the detail of data format for 3-line serial interface.

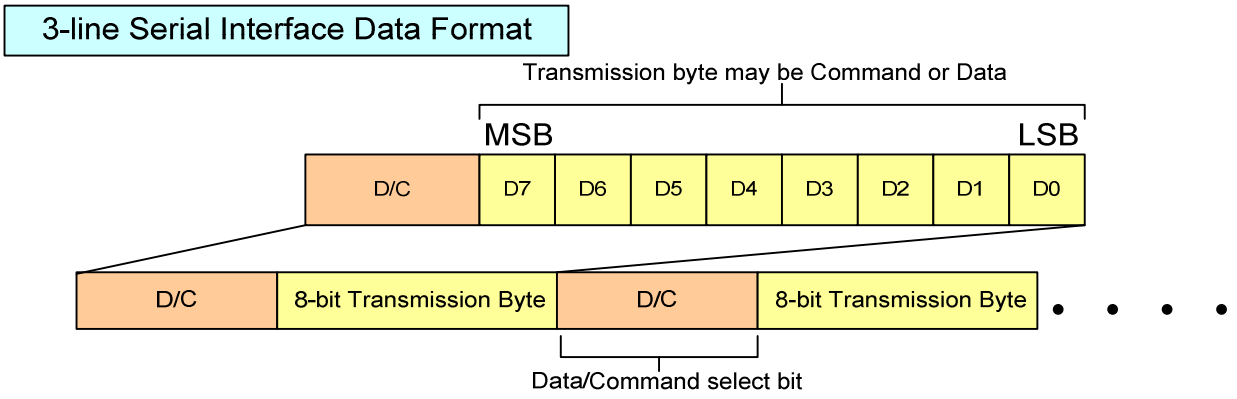


Figure 11: DBI Type C Data Format

The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the ILI9806 on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences as described in the Figure 12 below.

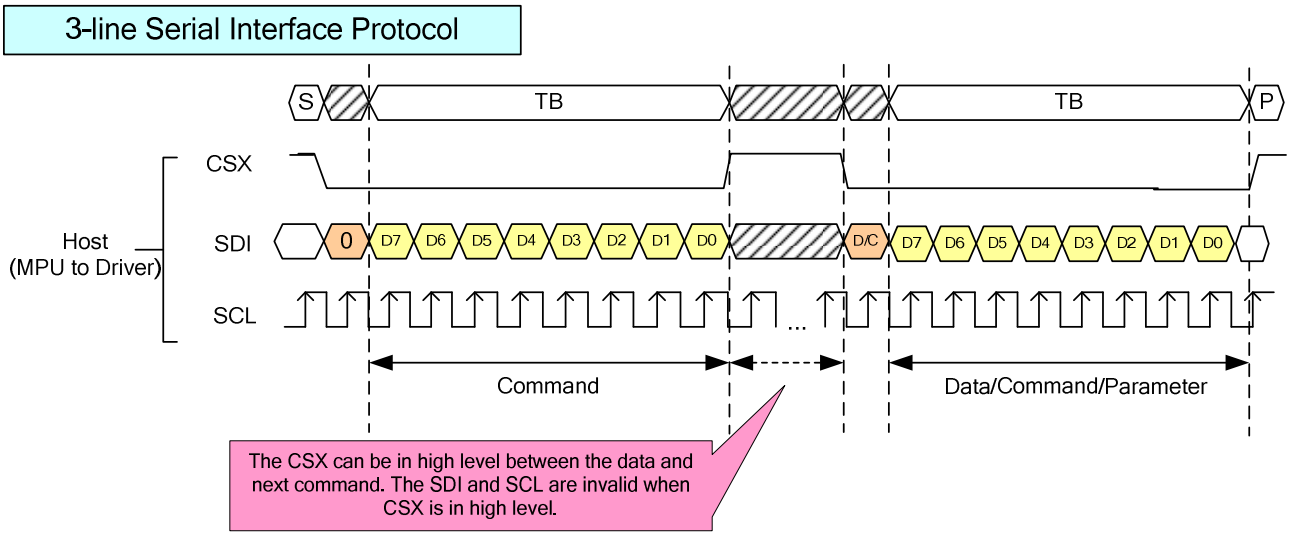


Figure 12: DBI Type C Protocol

3.8.2. Read Cycle Sequence

In the Read Mode of the interface, the host reads the register value from the ILI9806. The host sends a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ILI9806 samples the SDI (input data) at the rising edge of the SCL (serial clock), and shifts SDO (output data) at the falling edge of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

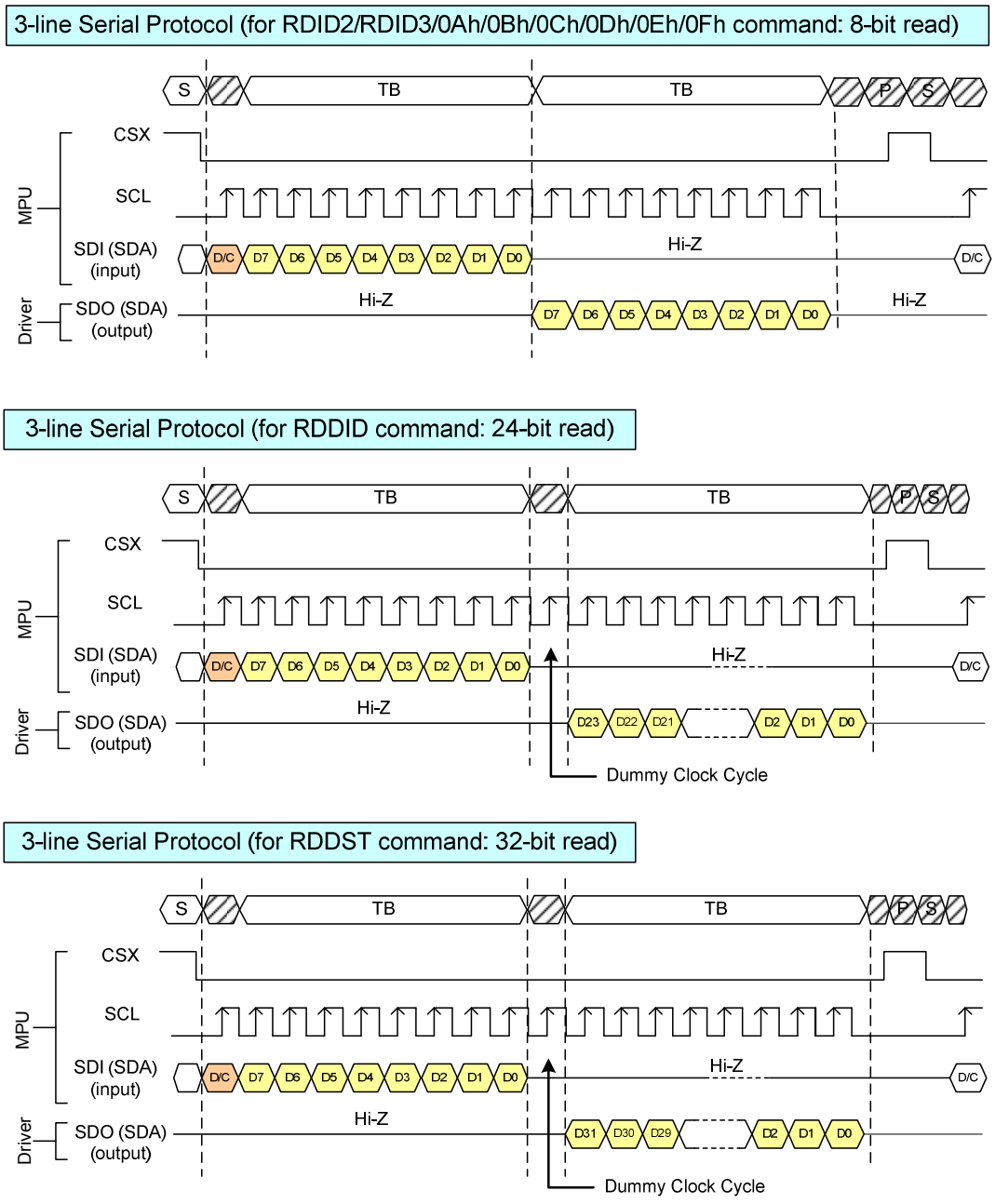


Figure 13: DBI Type C Read Cycle Sequence

3.9. Data Transfer Break and Recovery

If data transmission is interrupted by the CSX pulse while transferring a Command, Frame Memory data or multiple parameter command before Bit D0 of the byte has been completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is activated again.

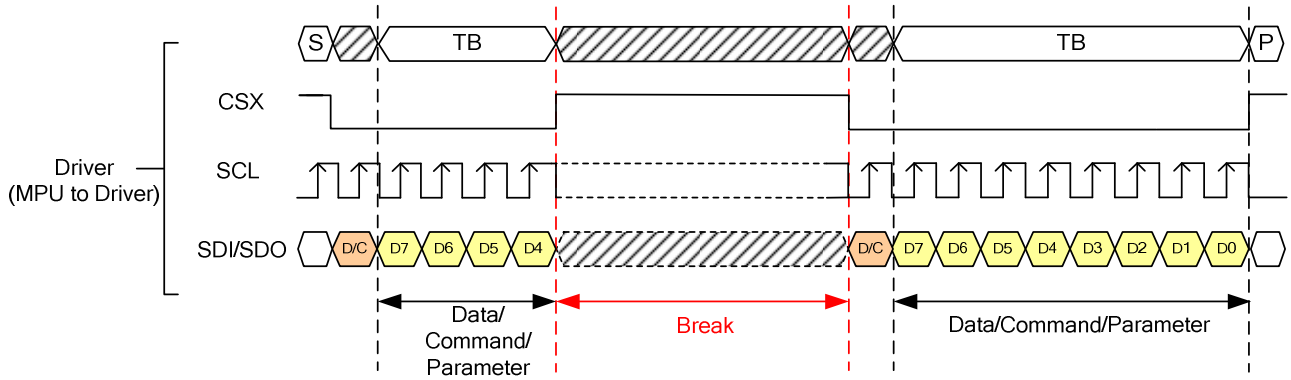


Figure 14: Data Transfer Break and Recovery

If there is a break when transmitting a command with multiple parameters and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below.

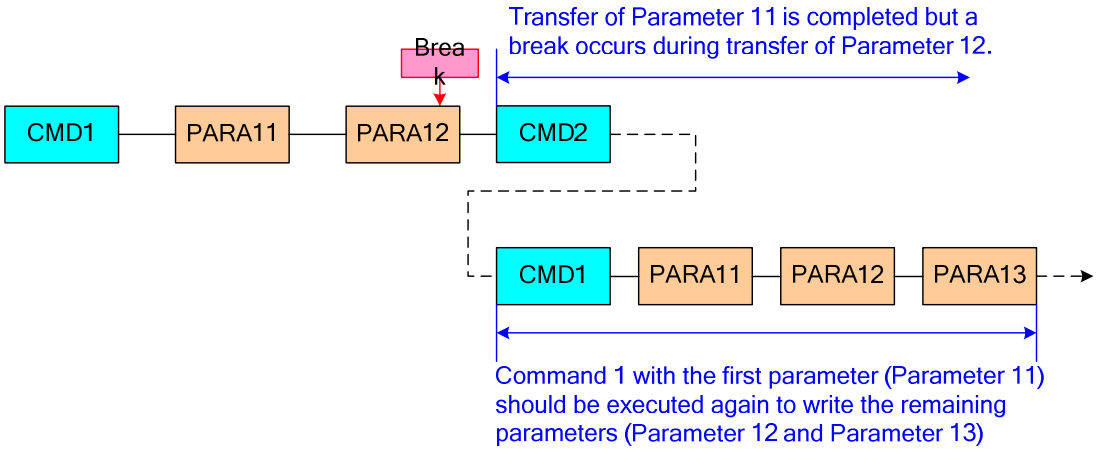


Figure 15: Data Transfer Break - Case 1

If a command with multiple parameters is sent and a break occurs when a new command is sent before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command remain at the previous value.

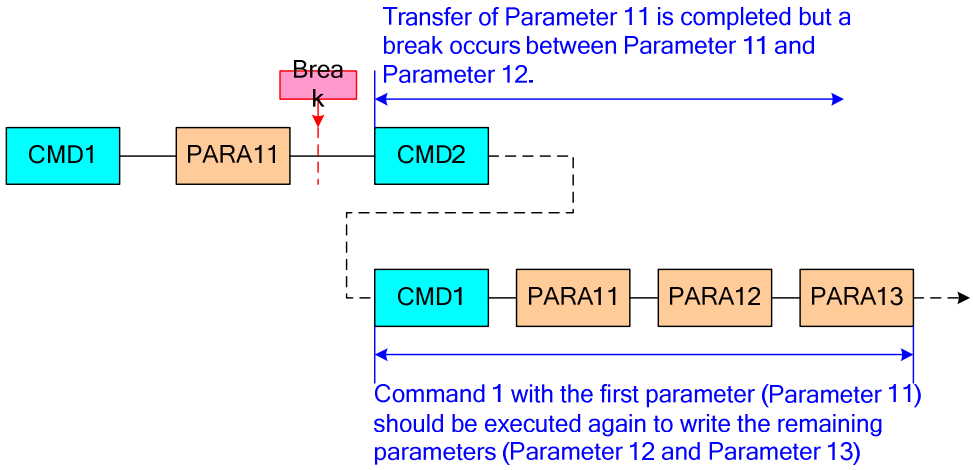


Figure 16: Data Transfer Break - Case 2

3.10. Data Transfer Pause

Transferring a Command, Frame Memory Data, or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ILI9806 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

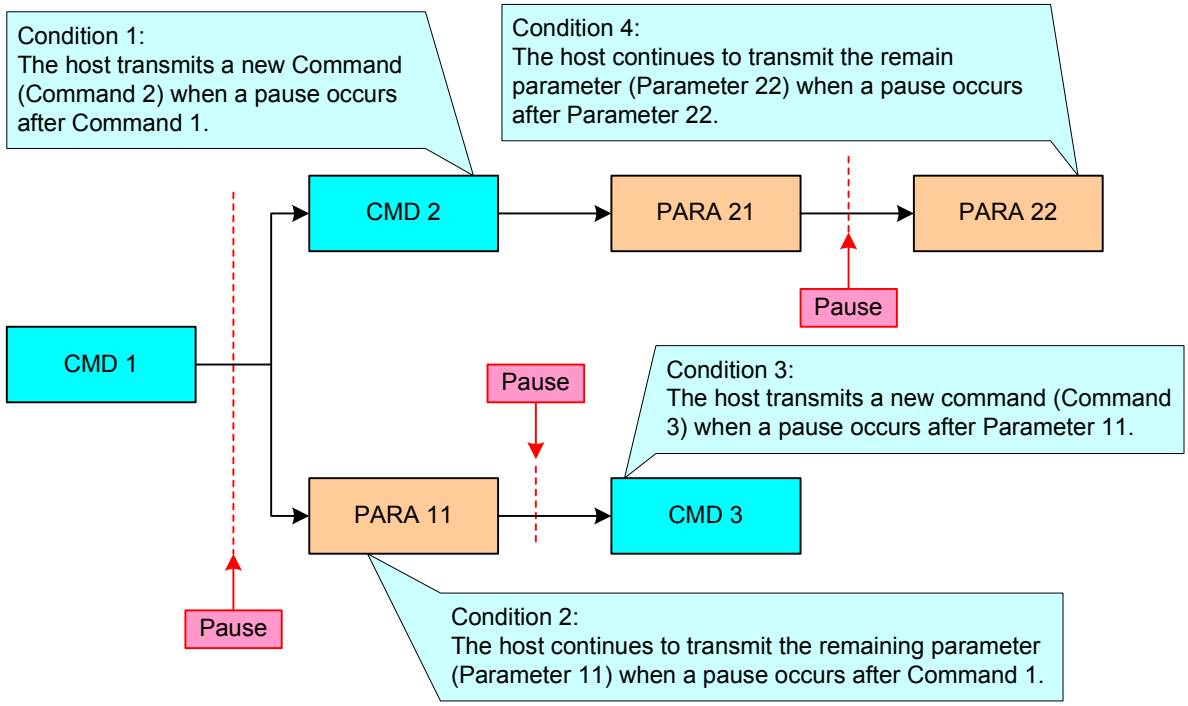


Figure 17: Data Transfer Pause

3.10.1. Serial Interface Pause

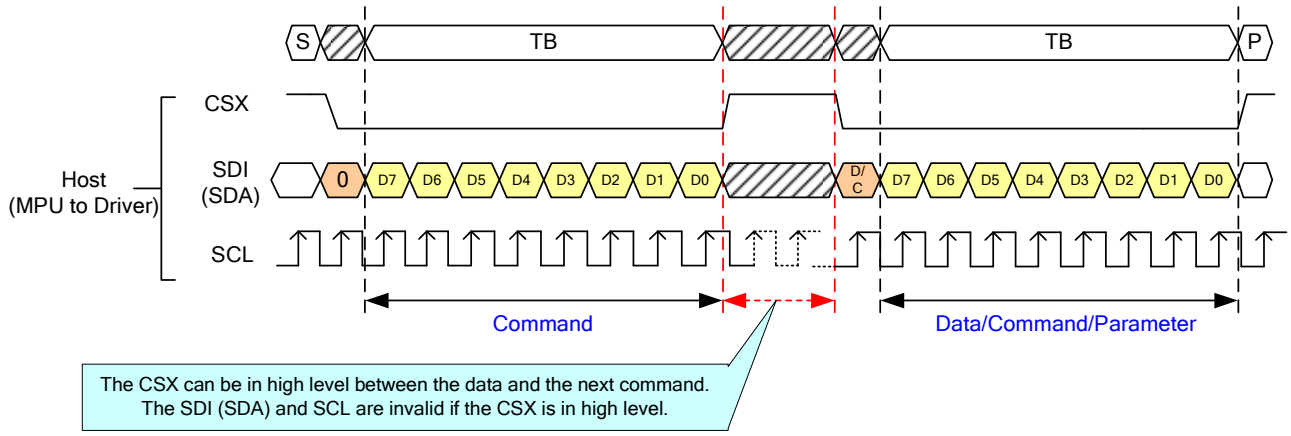


Figure 18: DBI Type C Data Transfer Pause

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

3.10.2. Parallel Interface Pause

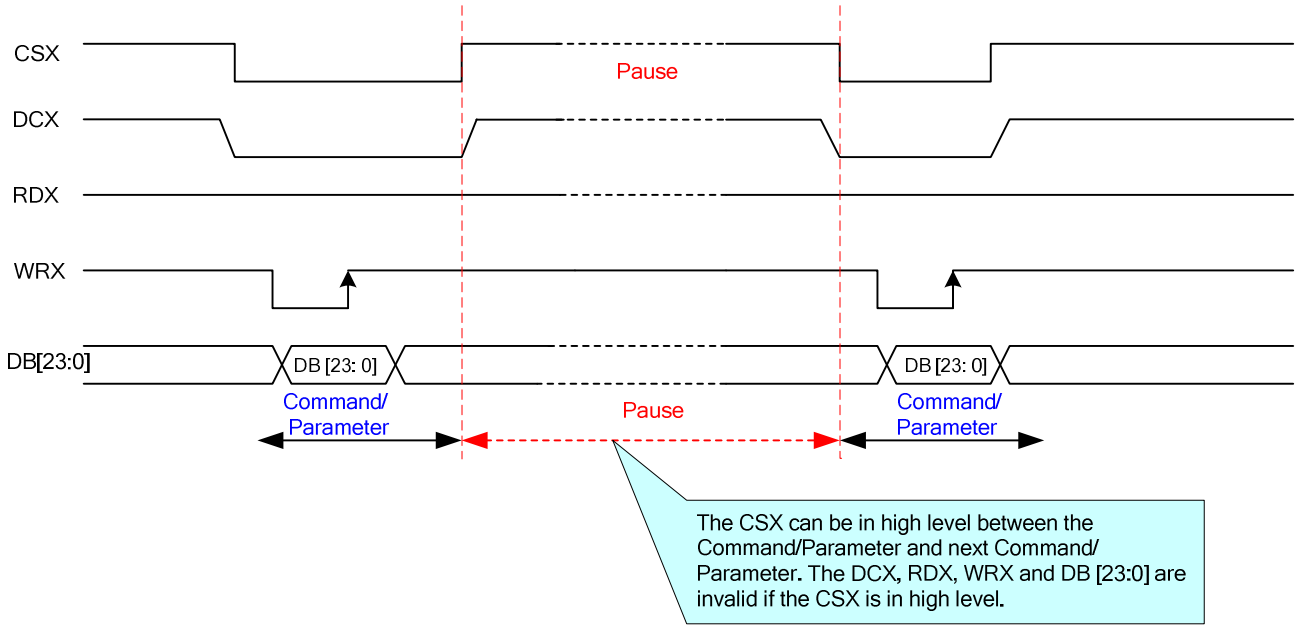


Figure 19: DBI Type B Data Transfer Pause

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

3.10.3. Data Transfer Mode

The ILI9806 provides five different types of color depth: 8-bit/per pixel, 9-bit/per pixel, 16-bit/per pixel, 18-bit/per pixel, and 24-bit/pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods[Note].

3.10.4. Method 1

The Image data is sent to the Frame Memory in the successive Frame writing, each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and the next Frame is written.

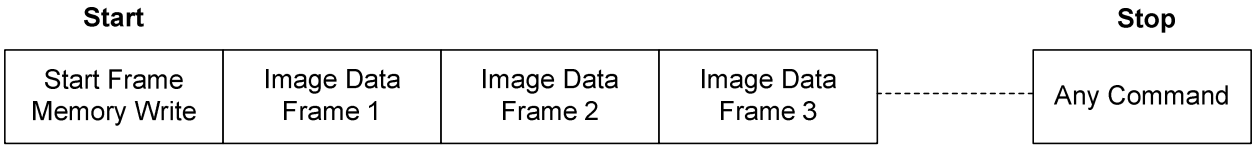


Figure 20: Data Transfer Mode - Method 1

3.10.5. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop the Frame Memory Writing. Then Start Memory Write command is sent, and a new Frame is downloaded.

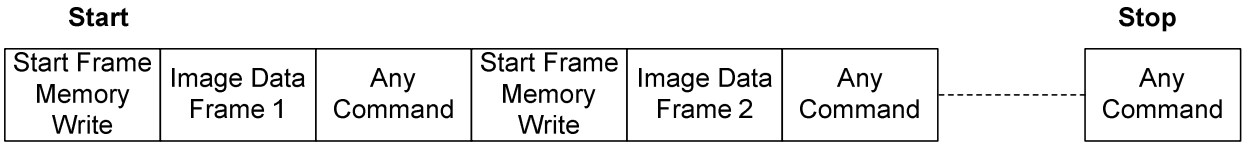


Figure 21: Data Transfer Mode - Method 2

Note 1. These apply to all five kinds of color depth on both serial and parallel interfaces.

2. The Frame Memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the Frame Memory.

3.11. DPI (RGB) Interface

The DPI can display moving pictures by two ways: rewrite into the GRAM and transmit directly to the shift register. The selection is set by the register BPGRAM and RM bit. The RM bit selects an interface for the access operation of the Frame Memory. For the DPI, RM should be set as 1.

BPGRAM	Display data path
0	Write into Memory

RM	Interface for RAM access
0	System interface
1	RGB interface

The DM bit selects the clock operation mode. It allows switching between display operations in synchronization with the internal oscillation clock. If DM = 1, the external DCK cannot be stopped unless it enters the Sleep In mode.

DM	RGB interface operating clock selection
0	Internal system clock
1	RGB interface DCK (Dot clock)

3.11.1. DPI Interface Selection

The DPI interface is operated with VSYNC, HSYNC, ENABLE, DCK, and DB [23:0] lines. It supports several pixel formats that can be selected by DPI [2:0] bits in Pixel Format Set (R3Ah) command. The selection of a given interface is done by DPI [2:0], as shown in the Table 10 and Figure 22.

Table 10: DPI Interface Selection

DPI [2:0]			DPI (RGB) Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VSYNC, HSYNC, ENABLE, DB [20:16] , DB [13:8], DB [4:0]
1	1	0	18-bit RGB interface	VSYNC, HSYNC, ENABLE, DB [21:16] , DB [13:8], DB [5:0]
1	1	1	24-bit RGB interface	VSYNC, HSYNC, ENABLE, DB [23:0]
Other			Setting prohibited	

16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]				B[4]	B[3]	B[2]	B[1]	B[0]

18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	R[6]	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 22: DPI Interface 16/18/24-bit Pixel Format Selection

The Pixel clock (DCK) runs all the time without stop, and it is used to enter VSYNC, HSYNC, ENABLE, and DB [23:0] states when there is a rising edge of the DCK. The DCK cannot be used as the internal clock for other functions of the display module.

Vertical synchronization (VSYNC) is used to indicate when a new frame of the display is received. This is a low enable and its state is read to the display module by the rising edge of the DCK signal.

Horizontal synchronization (HSYNC) is used to indicate when a new line of the frame is received. This is a low enable and its state is read to the display module by the rising edge of the DCK signal.

Data Enable (ENABLE) is used to indicate when the RGB information that should be transferred to the display is received. This is a high enable and its state is read to the display module by the rising edge of the DCK signal. DB [23:0] are used to indicate what is the information of the image that is transferred to the display (when ENABLE = 0 (low) and there is a rising edge of DCK). DB [23:0] can be 0 (low) or 1 (high). These lines are read by the rising edge of the DCK signal. In RGB interface modes, the input display data is written to the GRAM first then outputs the corresponding source voltage according to the gray data from the GRAM.

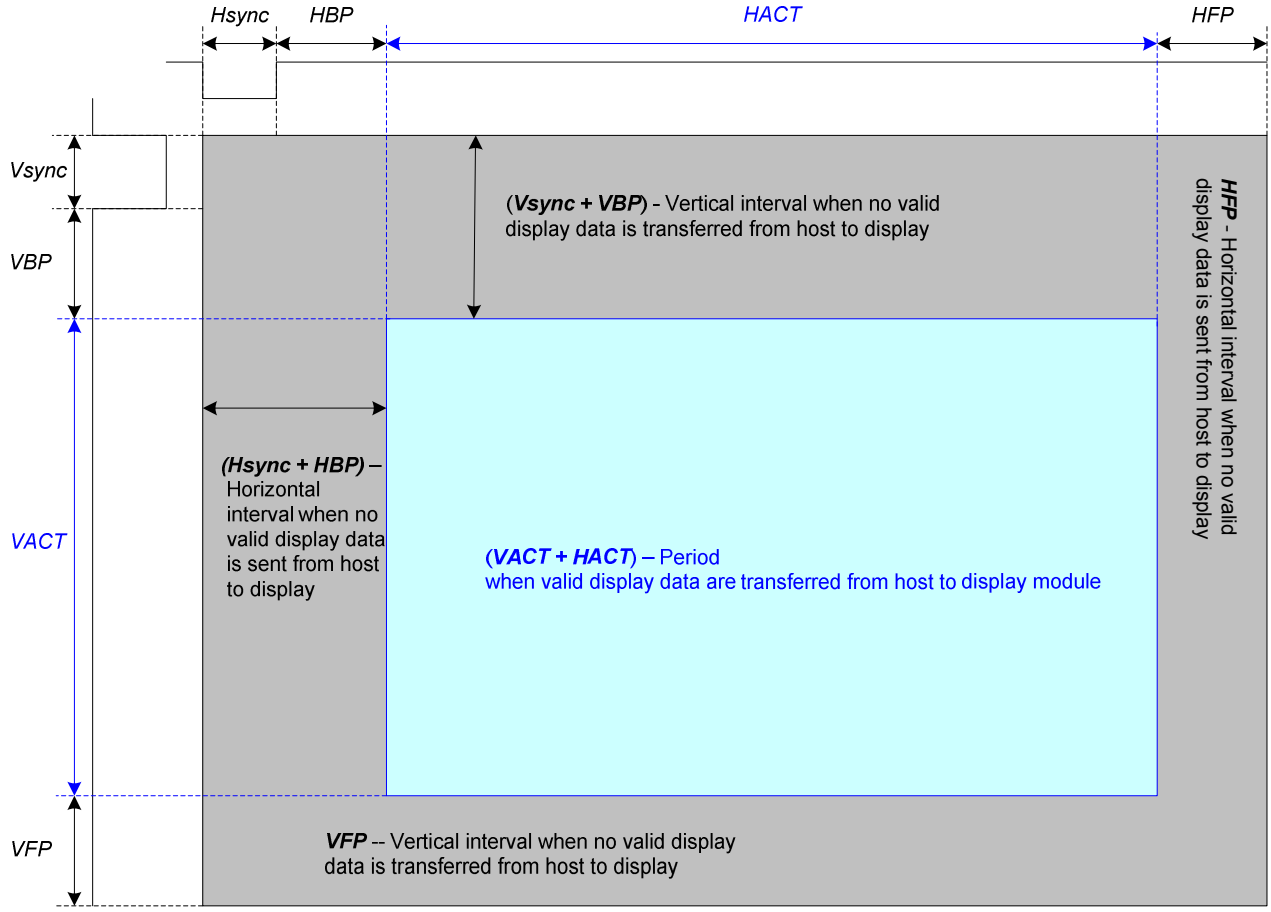


Figure 23: General DPI Timing Diagram

3.11.2. DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI interface mode is illustrated in Figure 24.

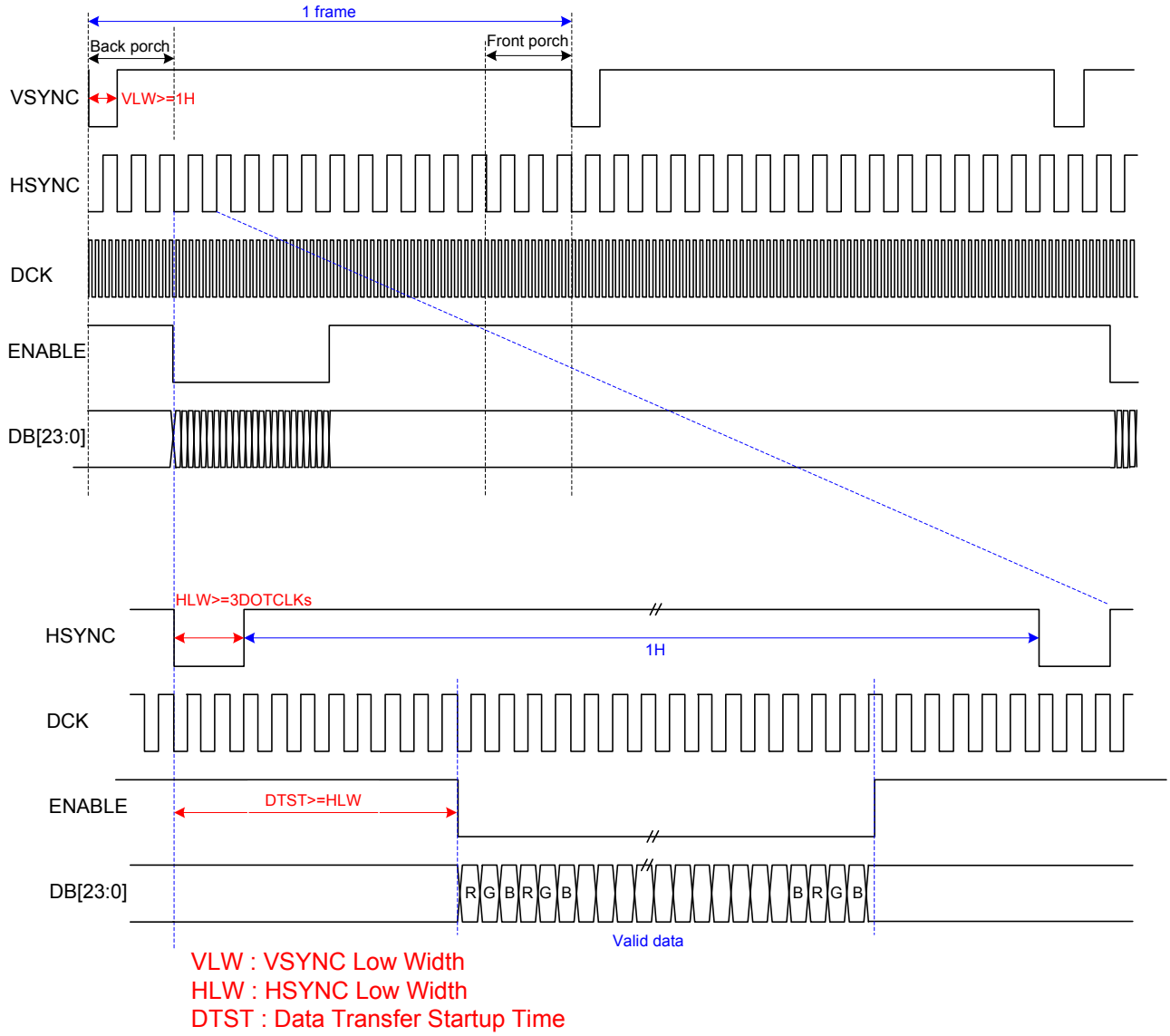


Figure 24: DPI Interface Timing diagram[Note]

Note *VSPL = 0, HSPL = 0, DPL = 0, and EPL = 0 of Interface Mode Control B0h command.*

3.12. DSI System Interface

3.12.1. General Description

The MIPI DSI is enabled or disabled by the external IM [3:0] pin.

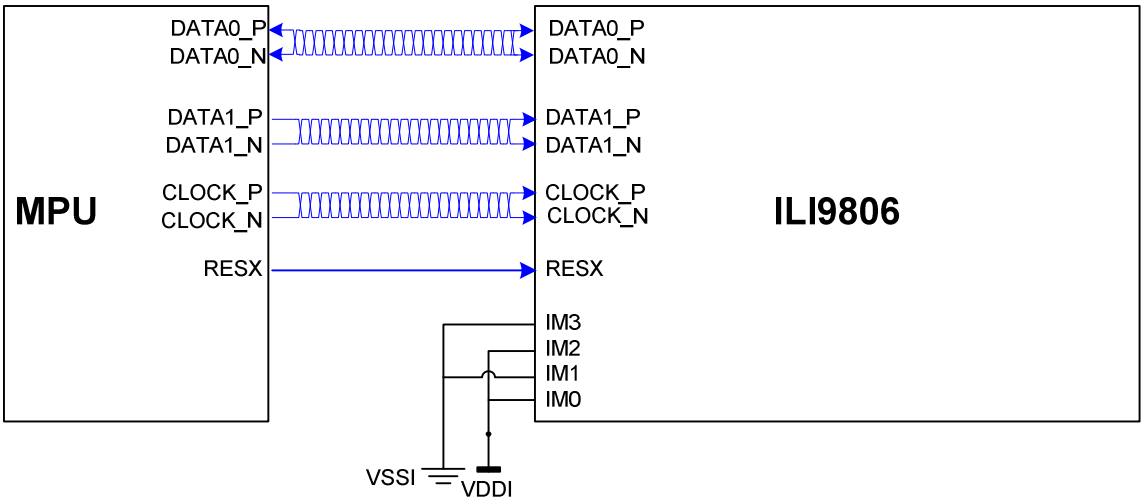


Figure 25: DSI System Interface Diagram

IM3	IM2	IM1	IM0	MPU Interface	Data Pin in Use
0	1	0	1	DSI interface	DSI_CP, DSI_CN DSI_D0P, DSI_D0N DSI_D1P, DSI_D1N

The communication is separated into two different levels between the MPU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

3.12.2. Interface Level Communication

3.12.3. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to the Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when information is to be transferred from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 11: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

3.12.4. DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM), or High Speed Clock Mode (HSCM). Clock lanes are in the single ended mode (LP = Low Power) when entering or leaving the Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Likewise, clock lanes are in the single ended mode (LP = Low Power) when entering in or leaving the High Speed Clock Mode (HSCM). These entering and leaving protocols use clock lanes in the single ended mode to generate an entering or leaving sequence.

The principal flow chart of the different power modes of clock lanes is illustrated below.

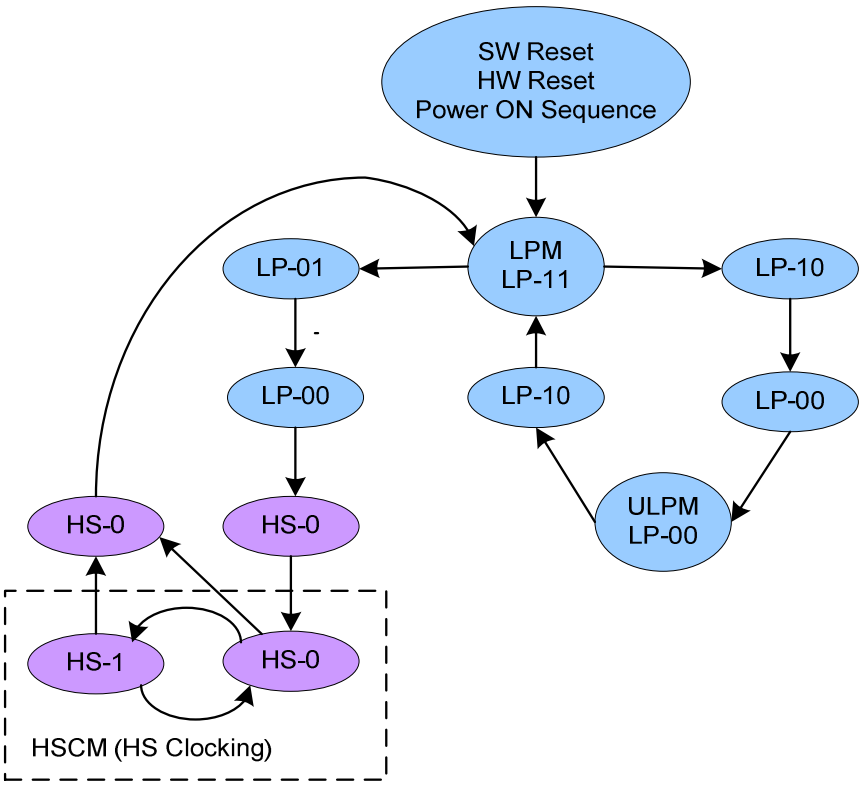


Figure 26: Power Modes of Clock Lanes

Note 1 *Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.*

Note 2 *If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, the lane pair returns to the LP-11 of the Control Mode.*

3.12.5. Low Power Mode (LPM)

When DSI-CLK lanes enter the LP-11 State Code, DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM) in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11

2) After DSI-CLK+/- lanes leave the Ultra Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM)

The sequence is illustrated below.

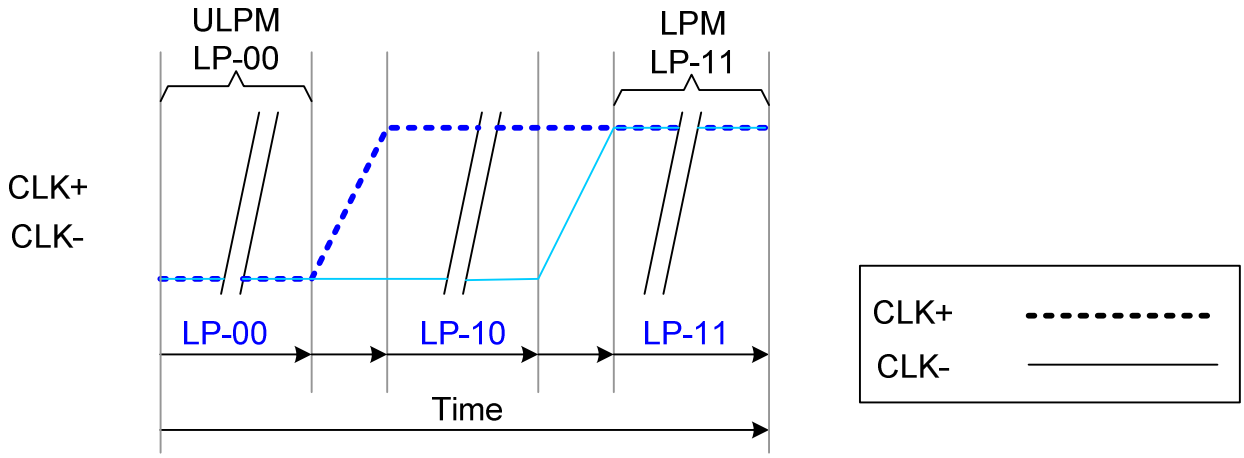


Figure 27: From ULPM to LPM

3) After DSI-CLK+/- lanes leave the High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0 => LP-11 (LPM). The sequence is illustrated below.

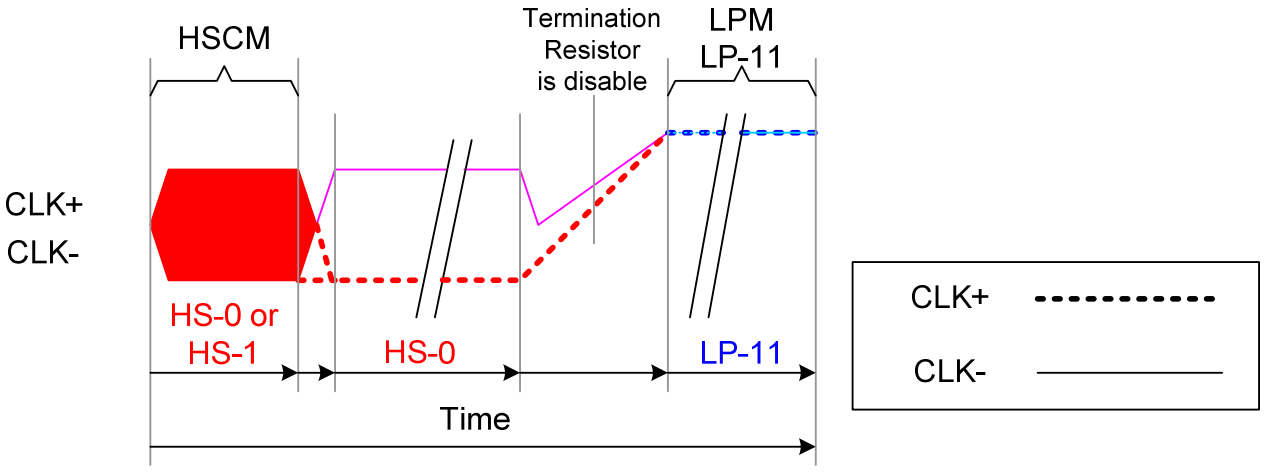


Figure 28: From High Speed Clock Mode (HSCM) to LPM

All the changes of the three modes are illustrated in the flow chart below.

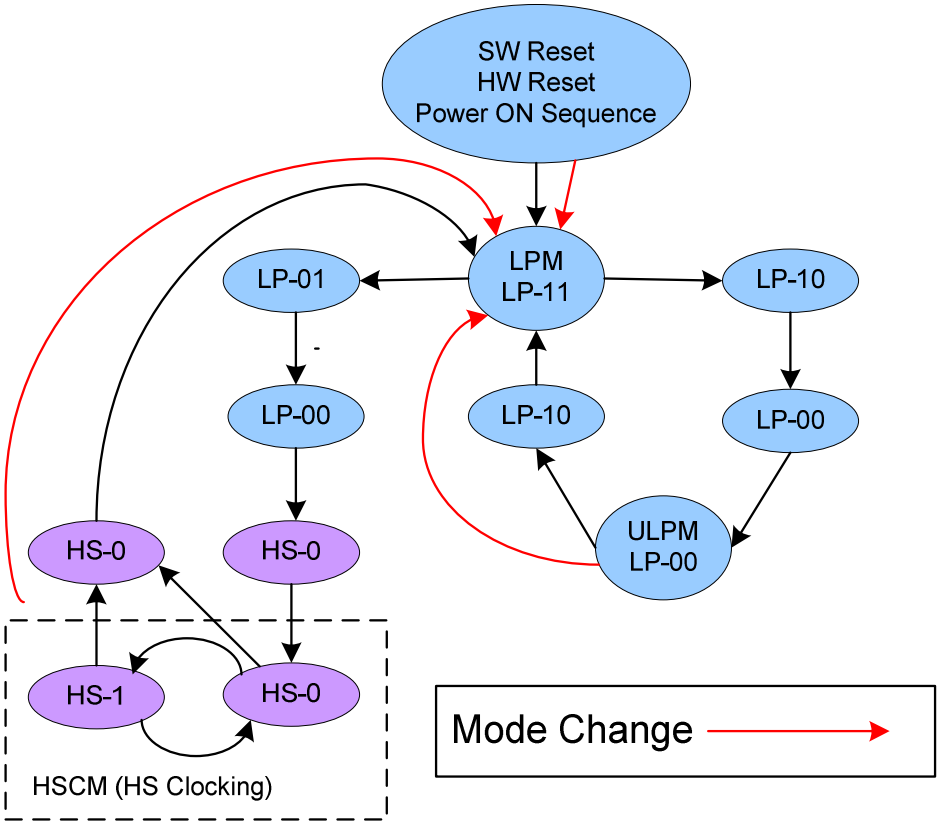


Figure 29: All the Changes of the Three Modes to the LPM

3.12.6. Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM) when DSI-CLK lanes enter the LP-00 State Code. The only possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM).

The sequence is illustrated below.

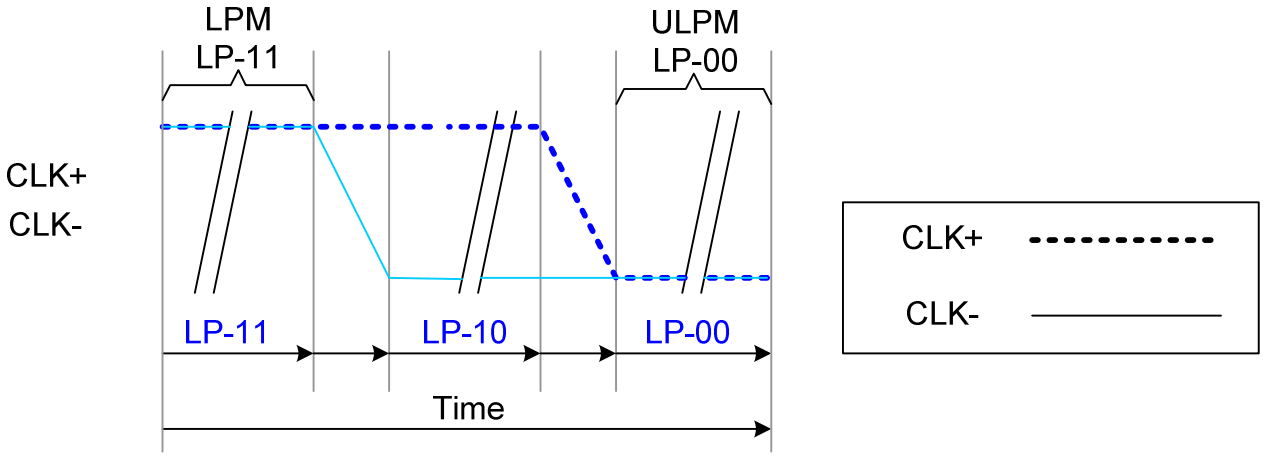


Figure 30: From LPM to ULPM

The mode change is illustrated below.

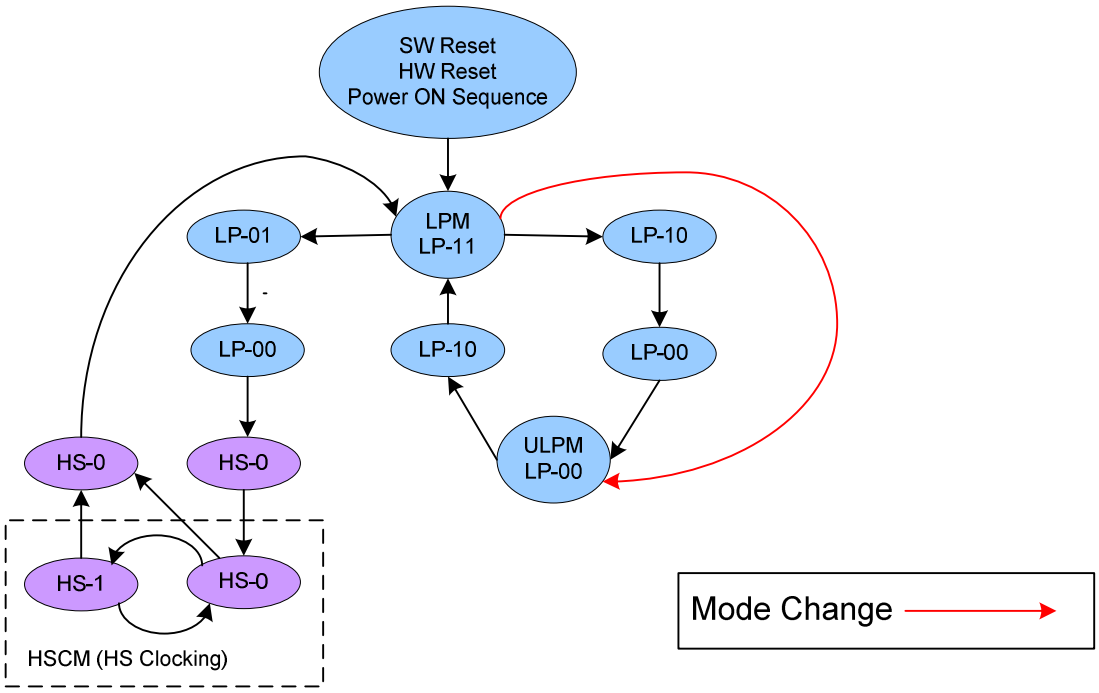


Figure 31: Mode Change from LPM to ULPM

3.12.7. High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM) when DSI-CLK lanes start to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). The sequence is illustrated below.

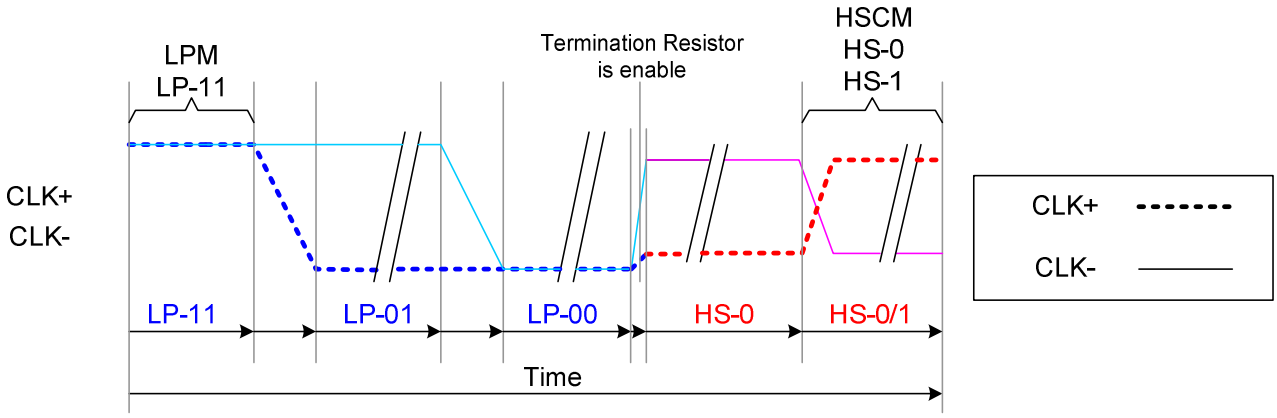


Figure 32: From LPM to HSCM

The mode change is illustrated below.

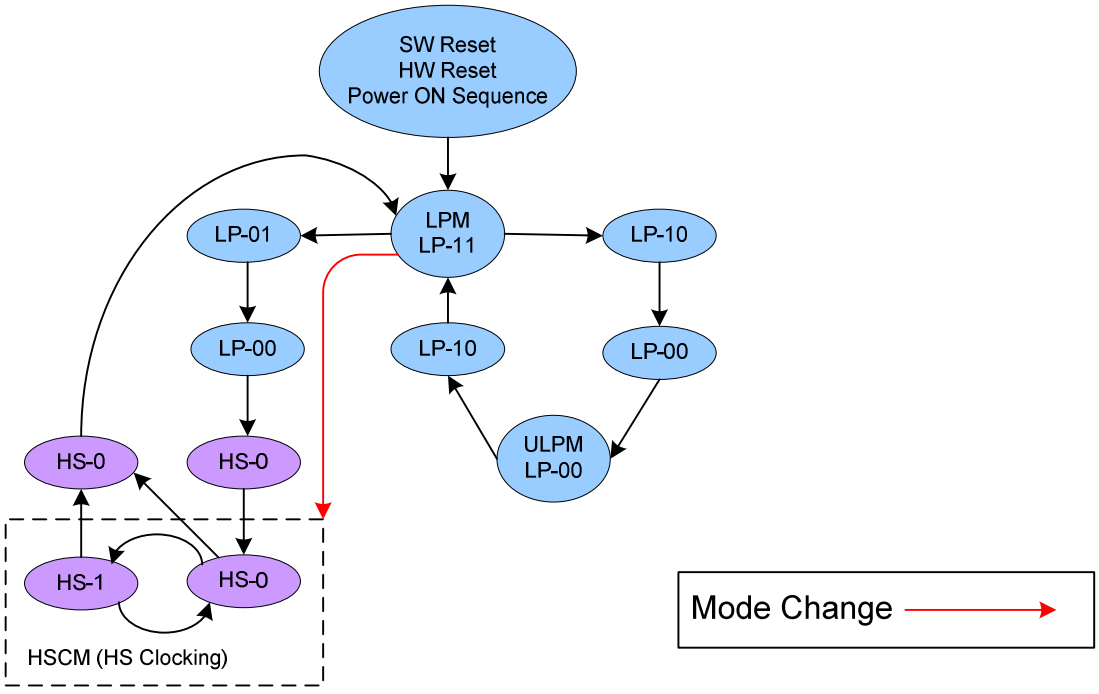


Figure 33: Mode Change from LPM to HSCM

The high speed clock (DSI-CLK+/-) starts before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

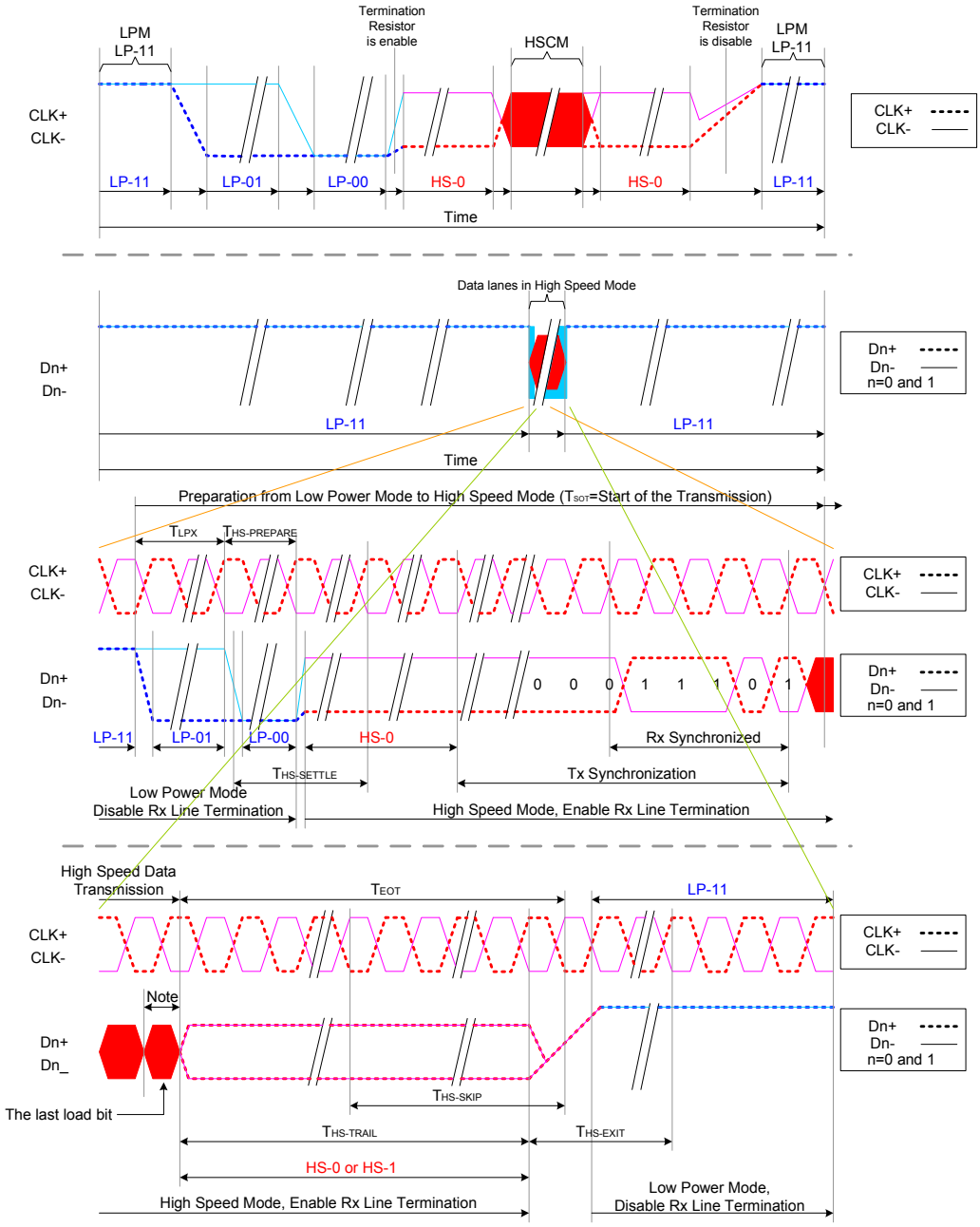


Figure 34: High Speed Clock Burst[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

3.12.8. DSI-D1 and DSI-D0 Data Lanes

3.12.9. General

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven to different modes:

- Escape Mode (only DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)
- Bus Turnaround Request (only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined in the following table.

Table 12: Entering and Leaving Sequences[Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

3.12.10. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode.

These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MPU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Tearing Effect” (TEE), which is used to transmit a TE line event from the display module to the MPU,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded when one of the data lanes changes from low-to-high-to-low, then this changed data lane presents the value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0). For example, when DSI-D0- changes from low-to-high-to-low, the receiver latches a data bit, which value is the logical 0. The receiver uses this low-to-high-to-low transition for its internal clock.
- A load if necessary
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

Note *1. DSI-D1+/- and DSI-D0+/- data lanes are used.*
2. See more information in the chapter of Bus Turnaround.

This basic construction is illustrated below:

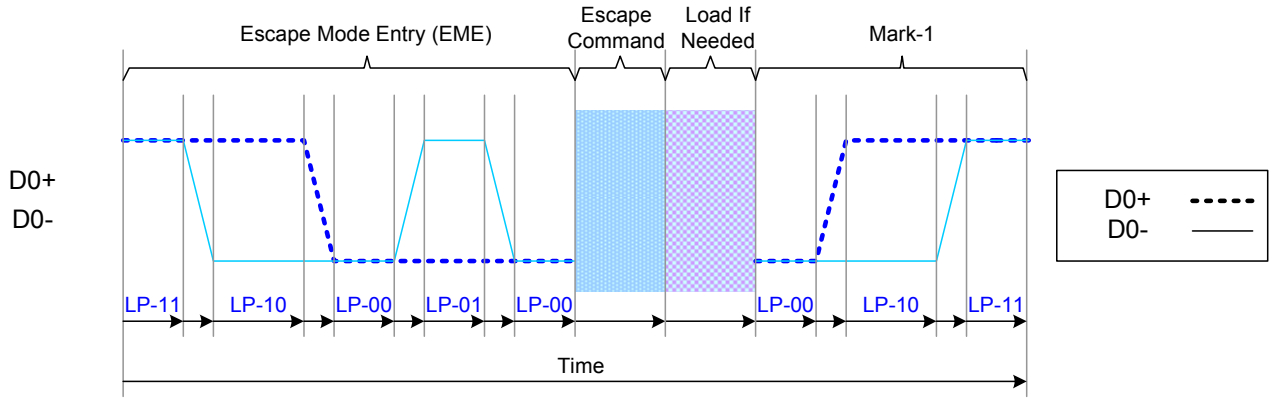


Figure 35: General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as described in Table 13: Escape Commands.

An example of a Mode type Escape Command is Ultra-Low Power Mode, where the MPU instructs the display module to enter its Ultra-Low Power Mode.

An example of a Trigger type Escape Command is Tearing Effect. In this case, the MPU has already instructed the display module to provide this trigger and is waiting for a response. The display module then sends a TE trigger (TEE) on the next V-sync event.

Escape commands are defined in the table below.

Table 13: Escape Commands[Note]

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit ➔ Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, [Note 1]	Mode	1001 1111 b	-	-
Undefined-2, [Note 1]	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Tearing Effect	Trigger	0101 1101 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, [Note 1]	Trigger	1010 0000 b	-	-

Note 1. This Escape command is not implemented in the display module.
2. n = 1
3. x = Supported
4. - = Not Supported