3.12.11. Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module uses the same sequence as which it sends data to the MPU.

The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in the pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

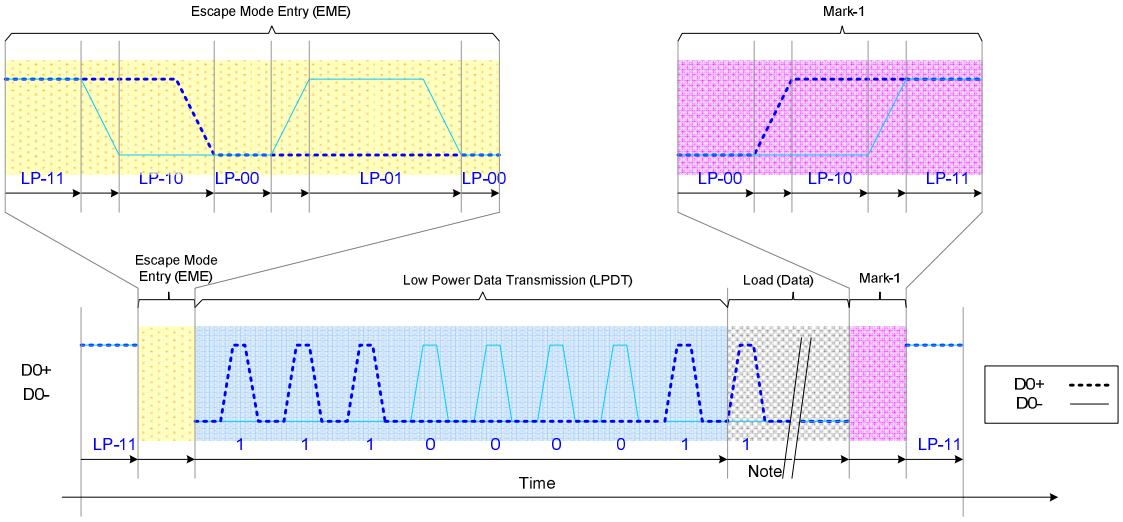


Figure 36: Low-Power Data Transmission (LPDT)[Note]

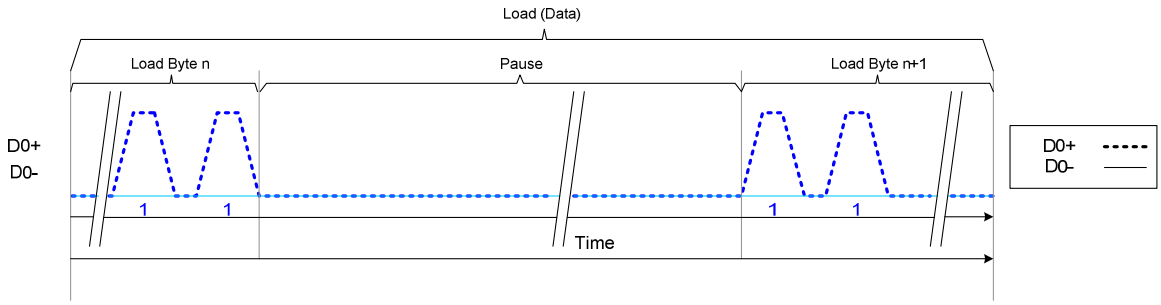


Figure 37: Pause (Example)

Note In this example, load (Data) presents that the first bit is the logical 1.

3.12.12. Ultra-Low Power State (ULPS)

The MPU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode.

The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MPU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

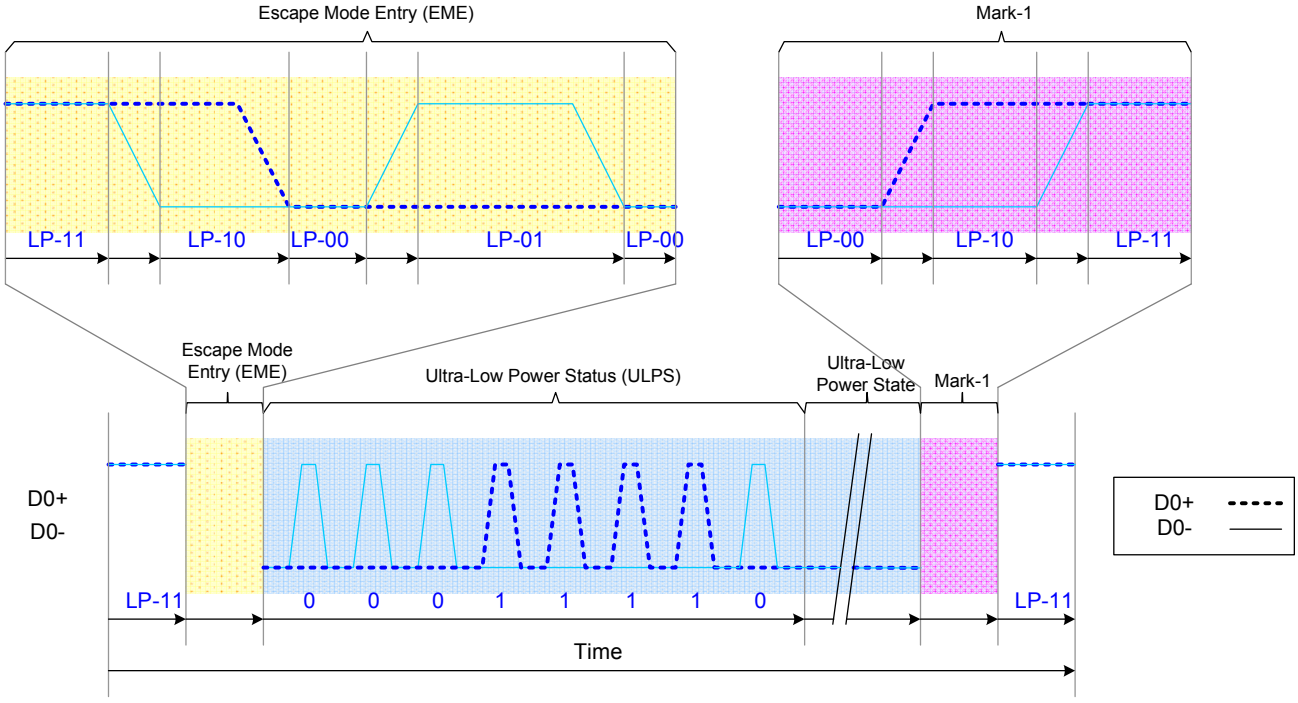


Figure 38: Ultra-Low Power State (ULPS)

3.12.13. Remote Application Reset (RAR)

The MPU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode.

The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in the Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

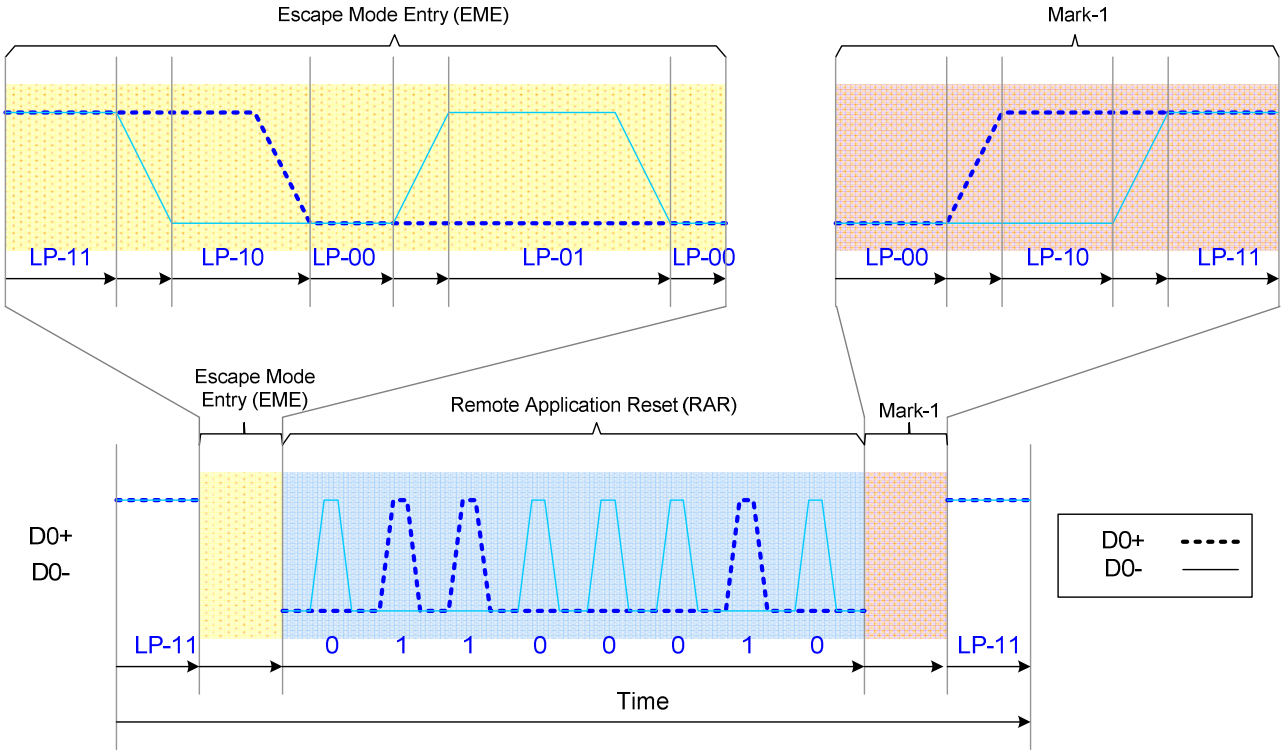


Figure 39: Remote Application Reset (RAR)

3.12.14. Tearing Effect (TEE)

The display module can inform the MPU when a tearing effect event (New V-synch) has happened in the display module by the Tearing Effect (TEE).

The display module sends the Tearing Effect (TEE) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Tearing Effect (TEE) trigger in the Escape Mode: 0101 1101 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

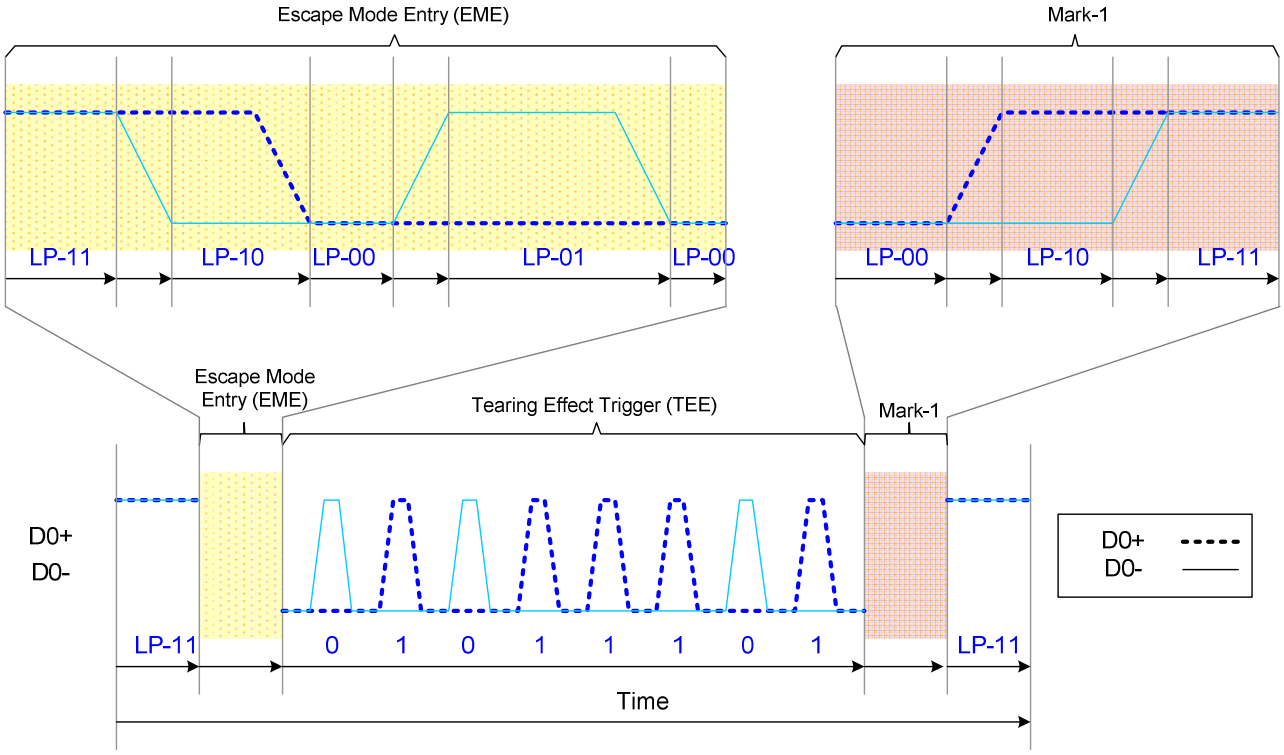


Figure 40: Tearing Effect (TEE)

3.12.15. Acknowledge (ACK)

The display module can inform the MPU that no errors are found by the Acknowledge (ACK).

The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated below for reference purpose:

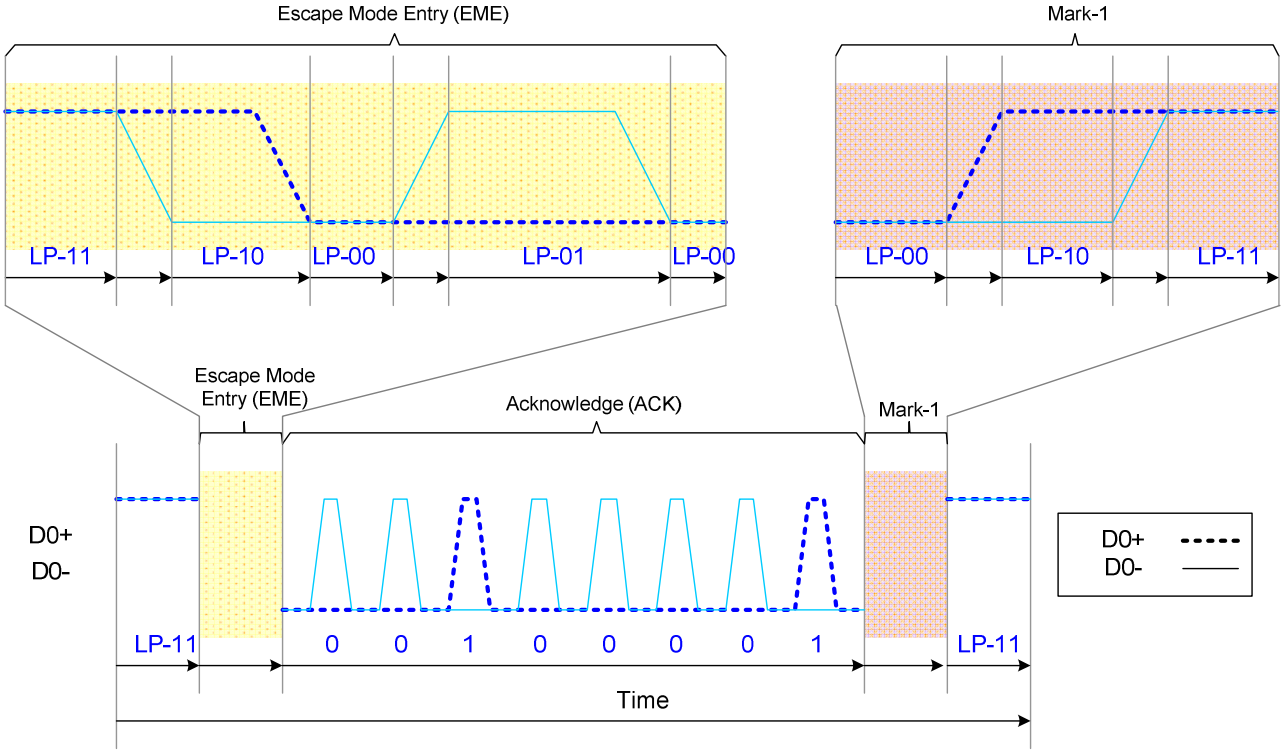


Figure 41: Acknowledge (ACK)

3.12.16. High-Speed Data Transmission (HSDT)

3.12.17. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters the High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already entered the High-Speed Clock Mode (HSCM) through the MPU. See more information in the chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module enter the High-Speed Data Transmission (TSOT of HSDT) with the following sequence:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

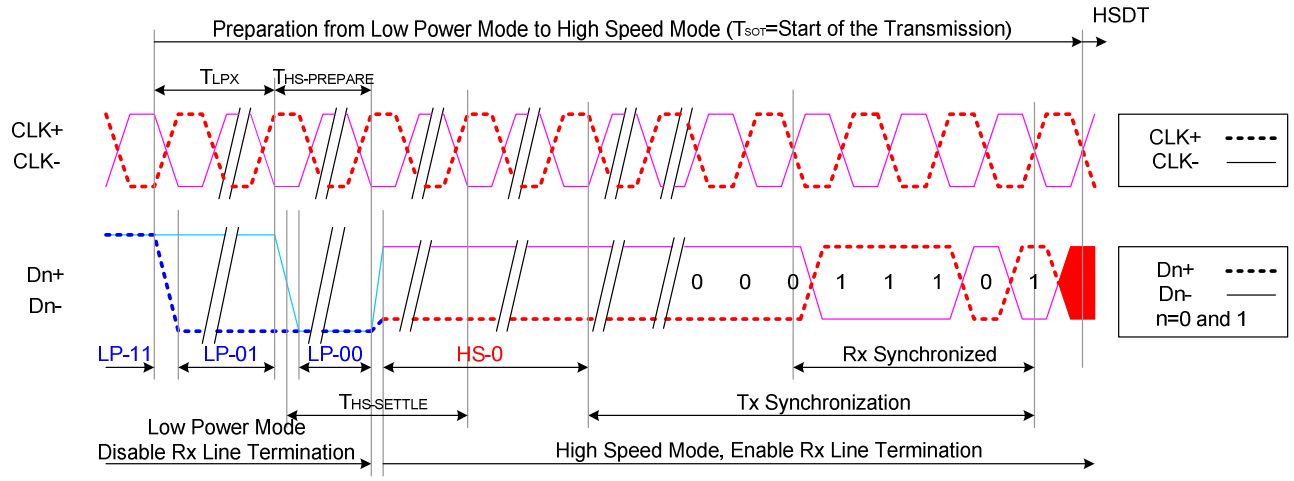


Figure 42: Entering High-Speed Data Transmission (TSOT of HSDT)

3.12.18. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) through the MPU. This HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in the LP-11 mode. See more information in the chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module leave the High-Speed Data Transmission (TEOT of HSDT) with the following sequence:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - o MPU changes to HS-1, if the last load bit is HS-0
  - o MPU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

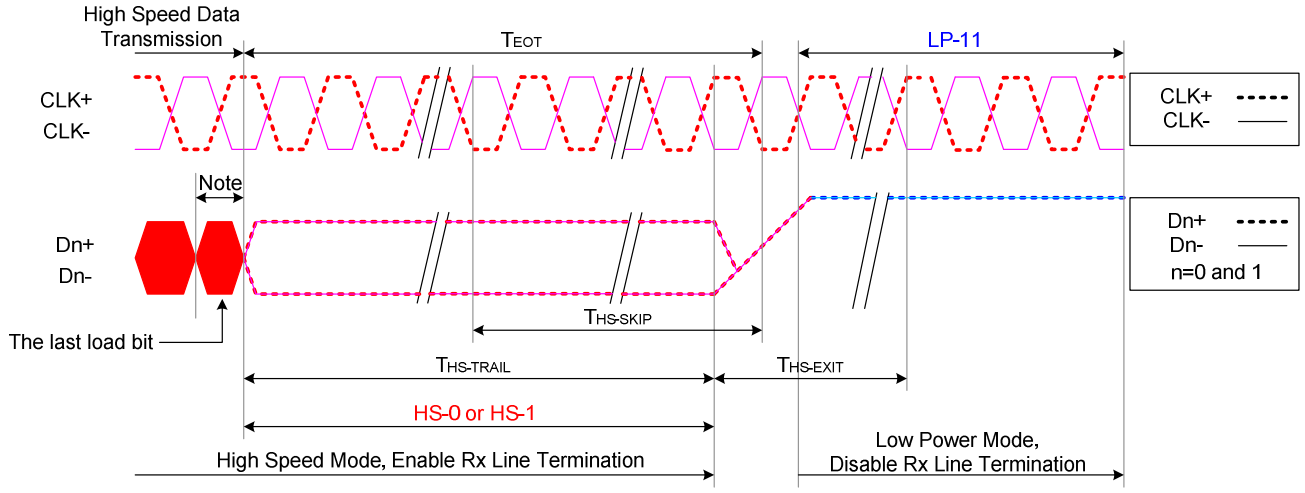


Figure 43: Leaving High-Speed Data Transmission (TEOT of HSDT)[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

3.12.19. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the chapter “Short Packet (SPa) and Long Packet (LPa) Structures”.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated below for reference purpose.

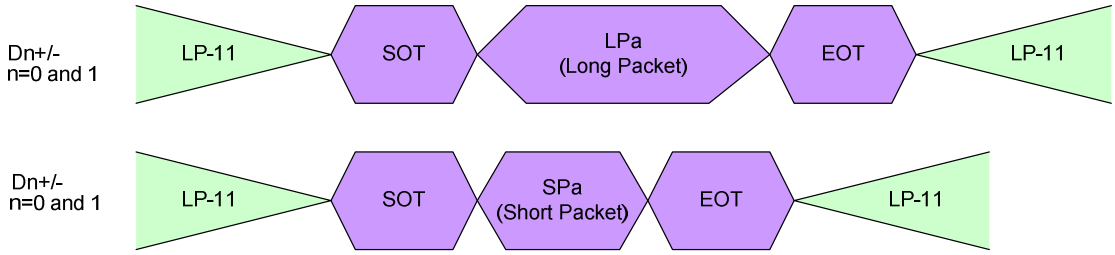


Figure 44: Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated below for reference purposes:

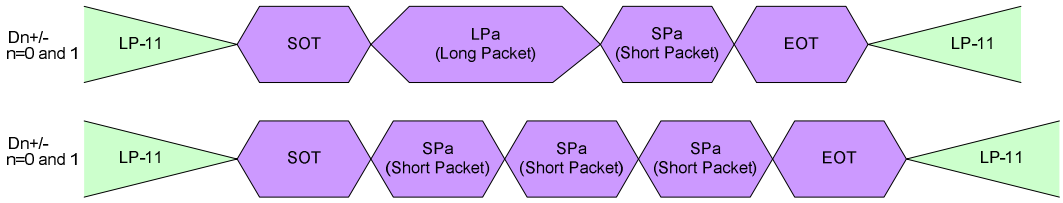


Figure 45: Multiple Packets in High-Speed Data Transmission – Examples

Table 46: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are 1 (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet in High-Speed Data Transmission (HSDT) are as follows.

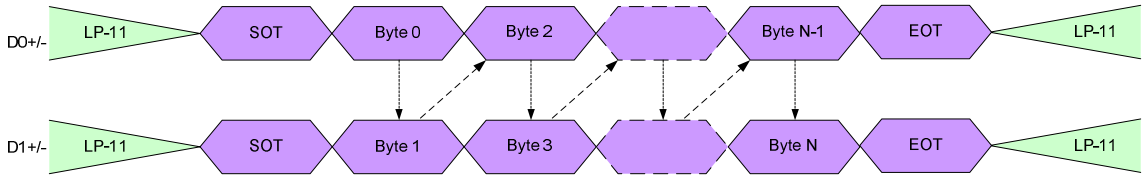


Figure 47: Single Packet in HSDT – Even Number of Bytes

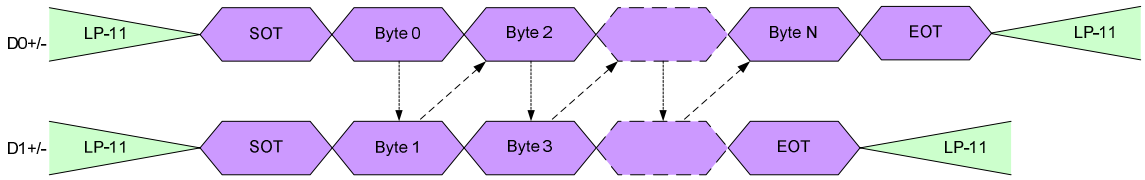


Figure 48: Single Packet in HSDT – Odd Number of Bytes

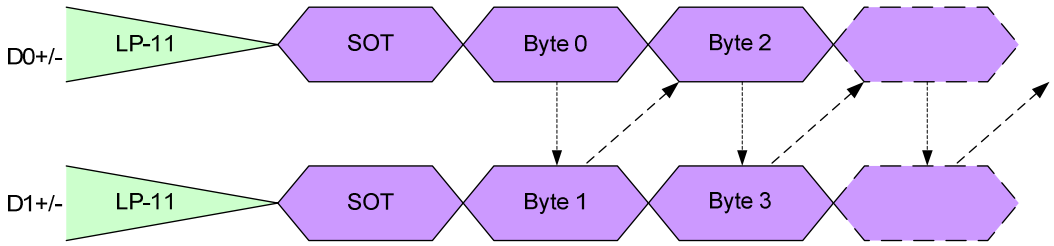


Figure 49: Start of Transmission (SoT) in HSDT for Multiple Packets

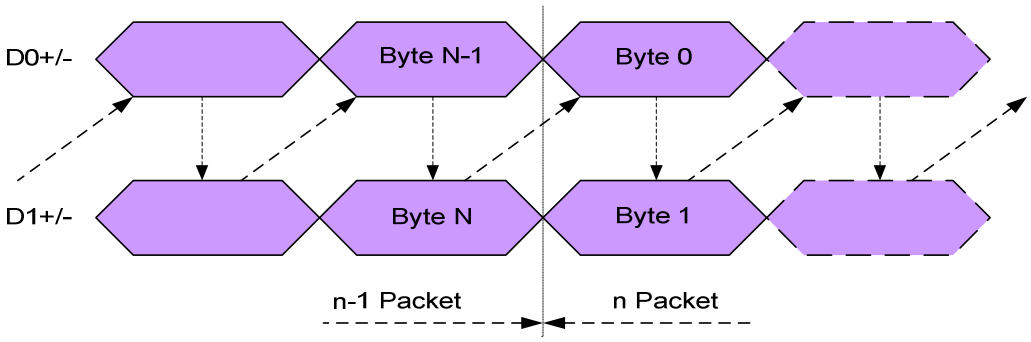


Figure 50: Continuous Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

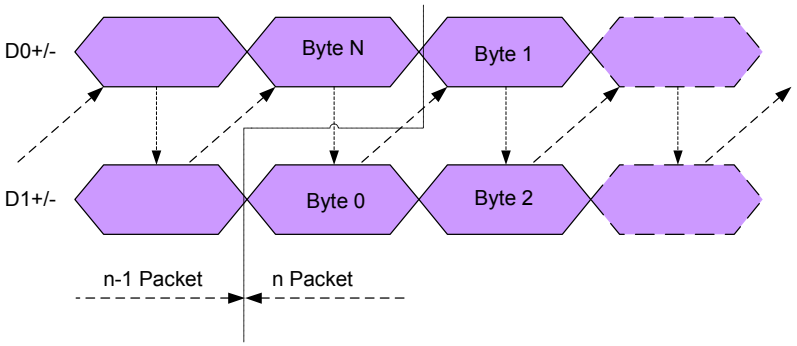


Figure 51: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

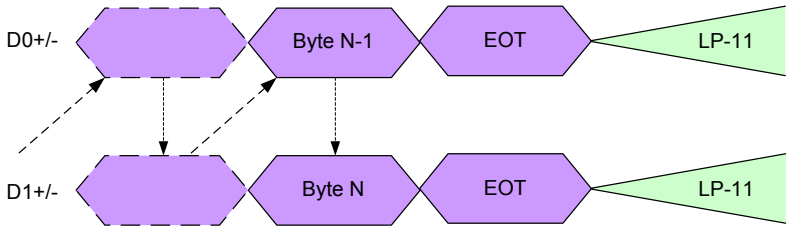


Figure 52: End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

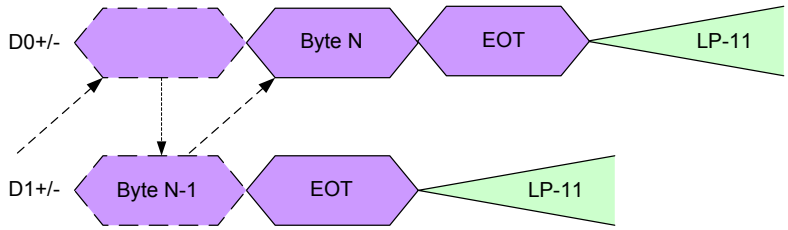


Figure 53: End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

3.12.20. Bus Turnaround (BTA)

The MPU or the display module, which controls DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MPU or the display module.

The MPU and the display module use the same sequence when this bus turnaround procedure is applied. The sequence when the MPU wants to perform the bus turnaround procedure to the display module is described below for reference purpose:

- Start (MPU): LP-11
- Turnaround Request (MPU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MPU waits until the display module starts to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The same bus turnaround procedure (from the MPU to the display module) is illustrated below:

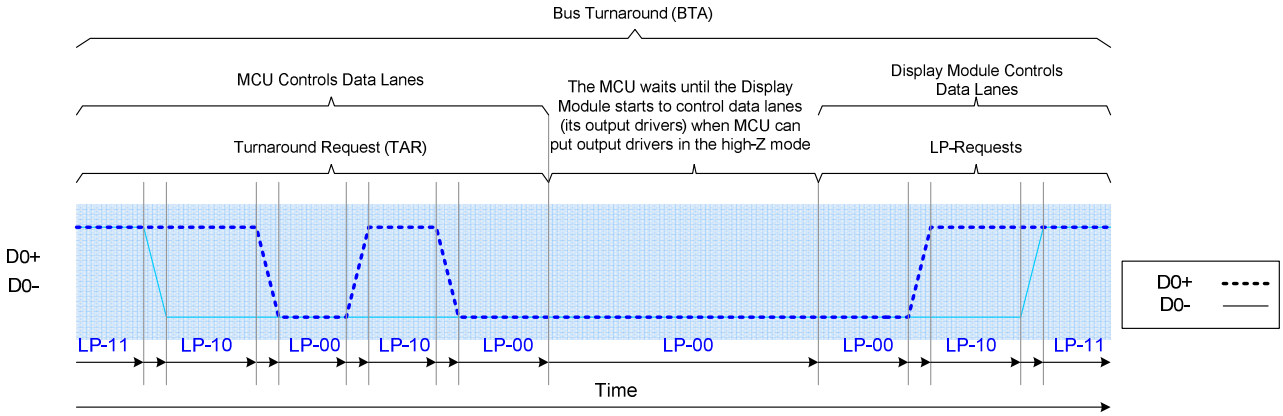


Figure 54: Bus Turnaround Procedure

The MPU and the display module can be switched in Figure 54: Bus Turnaround Procedure, if the Bus Turnaround (BTA) is from the display module to the MPU.

3.12.21. Packet Level Communication

3.12.22. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packets (SPa) and Long Packets (LPa) can always be used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes[Note].

The lengths of the packets are:

• Short Packet (SPa): 4 bytes

• Long Packet (LPa): 6 to 65,541 bytes

The type of the packet (SPa or LPa) can be recognized from their packet headers (PH).

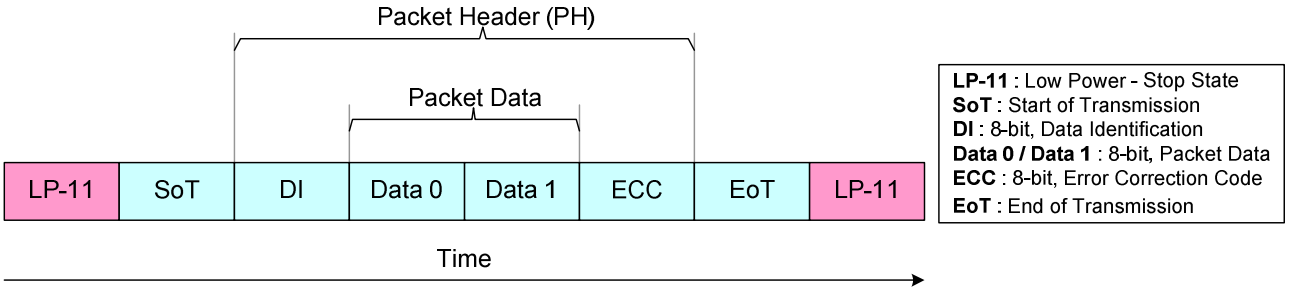


Figure 55: Short Packet (SPa) Structure

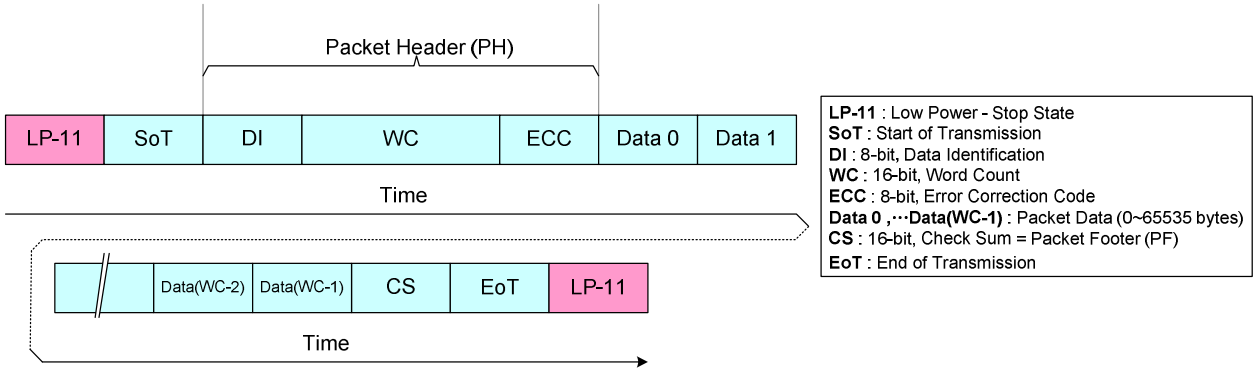


Figure 56: Long Packet (LPa) Structure

Note *Short Packet (SPa) and Long Packet (LPa) present a single packet sending (= including LP-11, SoT, and EoT for each packet sending).*
The other possibility is that SoT, EoT and LP-11 between packets are not necessary if packets are sent in multiple packet formats, for example:

- *LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11*
- *LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11*
- *LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11*

3.12.23. Bit Transmission Order of Bytes in Packets

The bit transmission order in a byte, which is used in packets, is that the Least Significant Bit (LSB) of a byte is sent first and the Most Significant Bit (MSB) of a byte is sent last.

This transmission order is illustrated below for reference purpose.

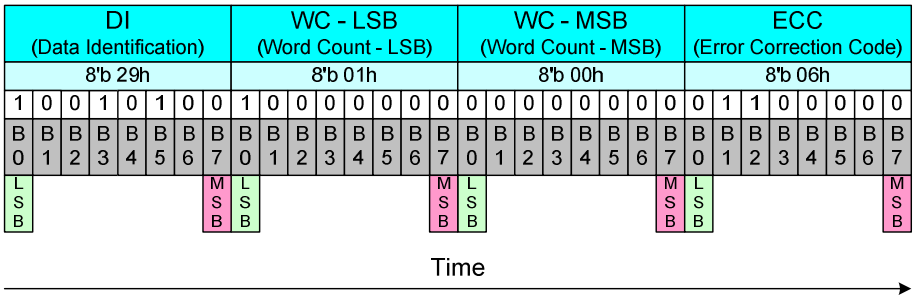


Figure 57: Bit Transmission Order of Bytes in Packets

3.12.24. Byte Transmission Order of Multiple-Byte Information in Packets

The byte transmission order of the multiple-byte information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte of the information is sent last. For example, Word Count (WC) consists of 2 bytes (16 bits); the LS byte is sent first and the MS byte is sent last.

This transmission order is illustrated below for reference purpose.

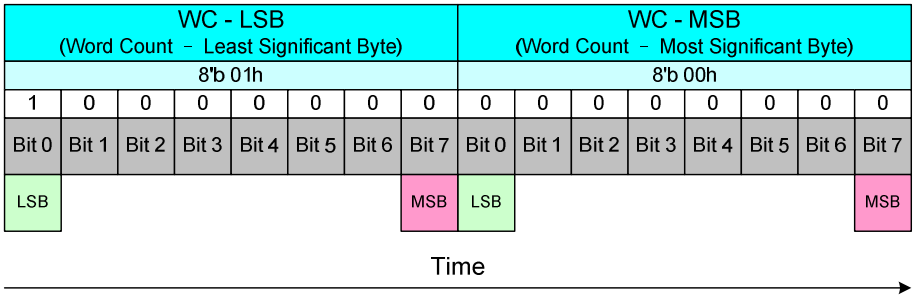


Figure 58: Byte Transmission Order of the Multiple-Byte Information in Packets

3.12.25. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packets (SPa) and Long Packets (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => identify that this is a Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)

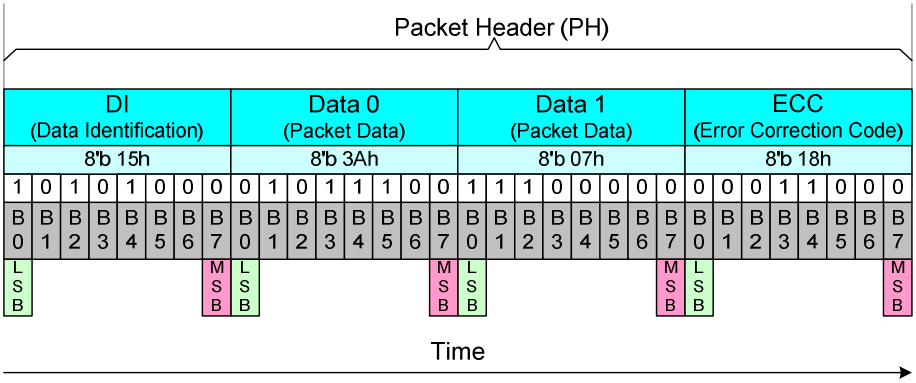


Figure 59: Packet Header (PH) of a Short Packet (SPa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => identify that this is a Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

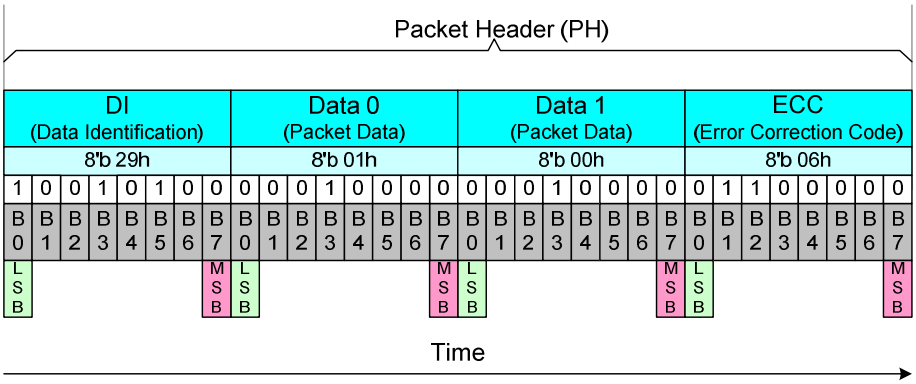


Figure 60: Packet Header (PH) on Long Packet (LPa)

3.12.26. Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated in the figure below.

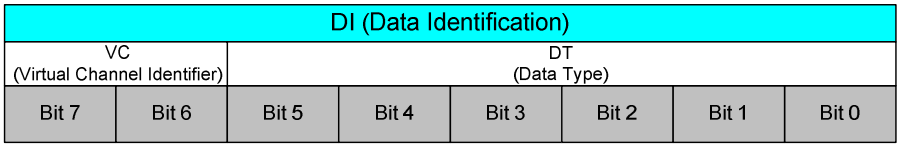


Figure 61: Data Identification (DI) Structure

Data Identification (DI) is illustrated in the Packet Header (PH) below for reference purpose.

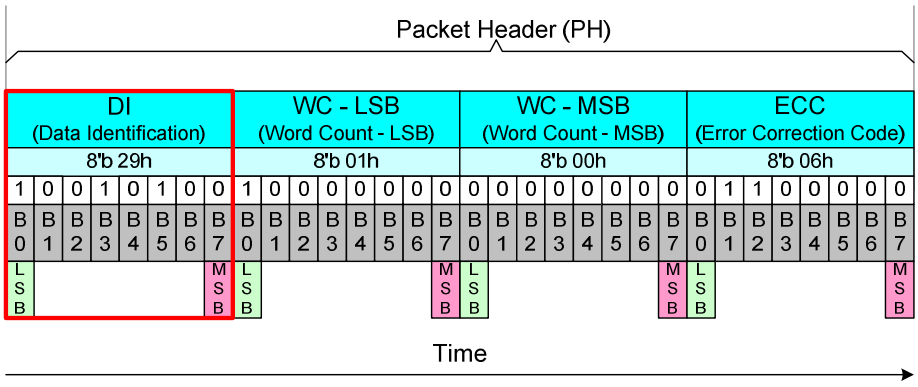


Figure 62: Data Identification (DI) in the Packet Header (PH)

3.12.27. Virtual Channel (VC)

Virtual Channel (VC) is a part of the Data Identification (DI [7…6]) structure and it is used to indicate where a packet is to be sent from the MPU.

Bits of the Virtual Channel (VC) are illustrated below for reference purpose.

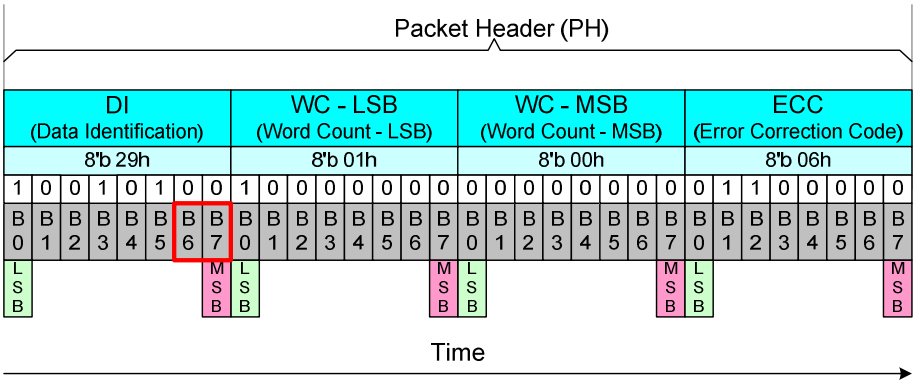


Figure 63: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels to 4 different display modules. Devices use the same virtual channel as which the MPU uses to send packets to them, for example,

- The MPU uses the virtual channel 0 when it sends packets to ILI9806
- ILI9806 also uses the virtual channel 0 when it sends packets to the MPU

This functionality is illustrated below.

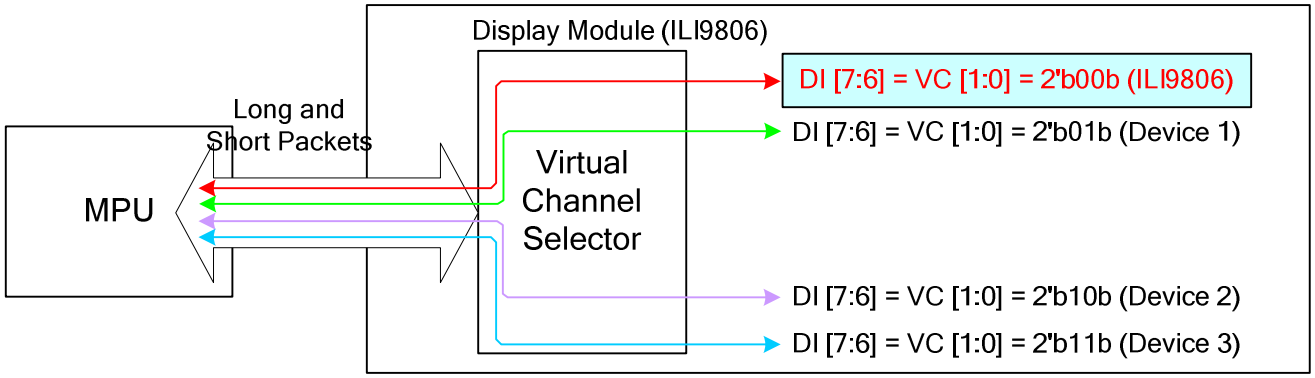


Figure 64: Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00_b) when the MPU sends the End of Transmission Packet to the display module. See the chapter “End of Transmission Packet (EoTP)”.

This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1..0]) is 00b for this display module.

3.12.28. Data Type (DT)

Data Type (DT) is a part of the Data Identification (DI [5…0]) structure and it is used to define the type of the used data in a packet.

Bits of the Data Type (DT) are illustrated below for reference purpose.

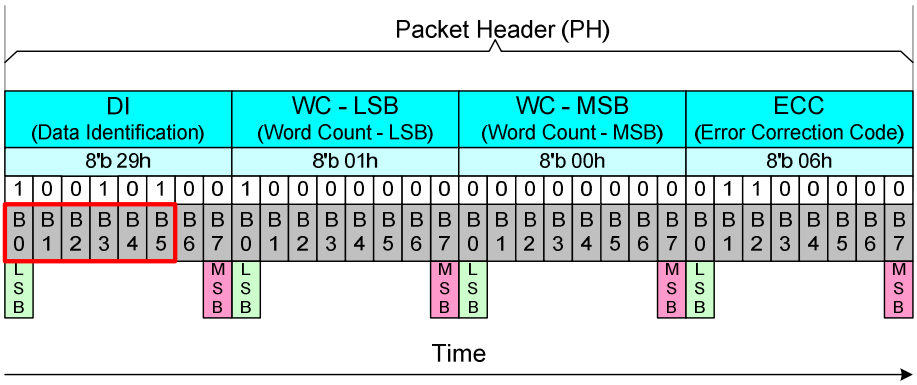


Figure 65: Data Type (DT) in the Packet Header (PH)

This Data Type (DT) also defines the used packet is Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MPU to the display module (or other devices) and vice versa.

These Data Types (DT) are defined in the tables below.

Table 14: Data Types (DT) from the MPU to the Display Module (ILI9806)

From the MPU to the Display Module (ILI9806)									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note 1	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note 2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Note 1 *This can be used when the MPU wants to make sure that it is the end of the transmission in the High Speed Data Transferring (HSDT) mode.*

Note 2 *This can be used when data lanes are to be kept in the High Speed Data Transferring (HSDT) Mode.*

Table 15: Data Types (DT) from the Display Module (ILI9806) to the MPU

From the Display Module (ILI9806) to the MPU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver will ignore other Data Types (DT) if they are not defined in the “Table 14: Data Type (DT) from the MPU to the Display Module (or Other Devices)” or “Table 15: Data Type (DT) from the Display Module (or Other Devices) to the MPU”.

3.12.29. Packet Data (PD) of a Short Packet (SPa)

Packet Data (PD) of a Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI), which indicates that a Short Packet (SPa) is to be sent.

Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

The sending order of Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last.

Bits of Data 1 are set to 0 if the information length is 1 byte.

Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated below for reference purpose.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

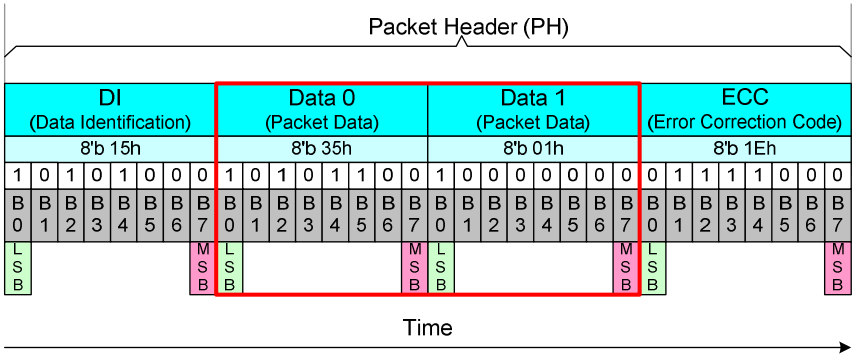


Figure 66: Packet Data (PD) of a Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

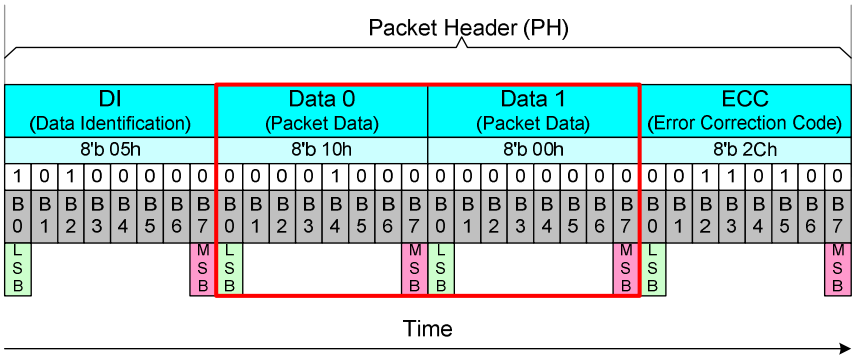


Figure 67: Packet Data (PD) of a Short Packet (SPa), 1 Byte Information

3.12.30. Word Count (WC) of a Long Packet (LPa)

Word Count (WC) of a Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI), which indicates that Long Packet (LPa) is to be sent.

Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) which are to be sent after the Packet Header (PH). The location of Word Count (WC) in a Long Packet is the same as which of Packet Data (PD) in a Short Packet.

Word Count (WC) of a Long Packet (LPa) consists of 2 bytes.

The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first and the Most Significant (MS) Byte is sent last.

Word Count (WC) of a Long Packet (LPa) is illustrated below for reference purposes.

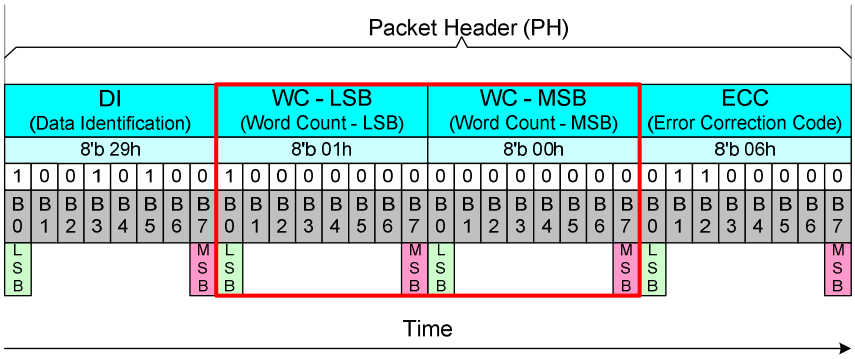


Figure 68: Word Count (WC) of a Long Packet (LPa)

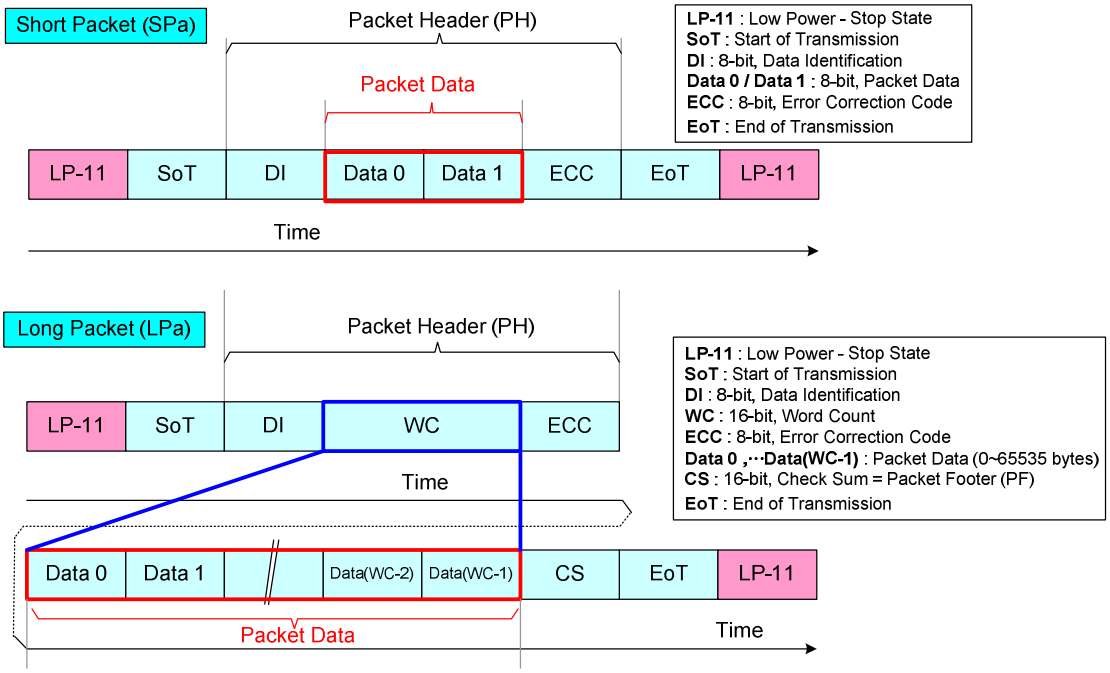


Figure 69: Packet Data in Short and Long Packets

3.12.31. Error Correction Code (ECC)

Error Correction Code (ECC) is a part of the Packet Header (PH), and its purpose is to identify an error or errors.

The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])

D [23…0] and P [7…0] are illustrated below for reference purpose.

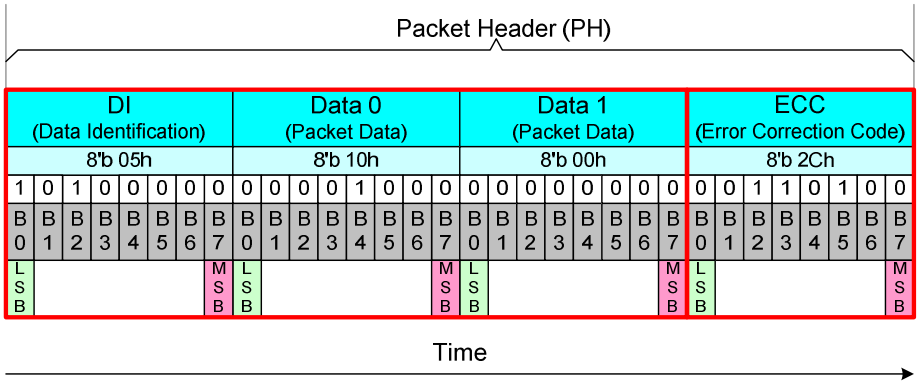


Figure 70: D [23…0] and P [7…0] of a Short Packet (SPa)

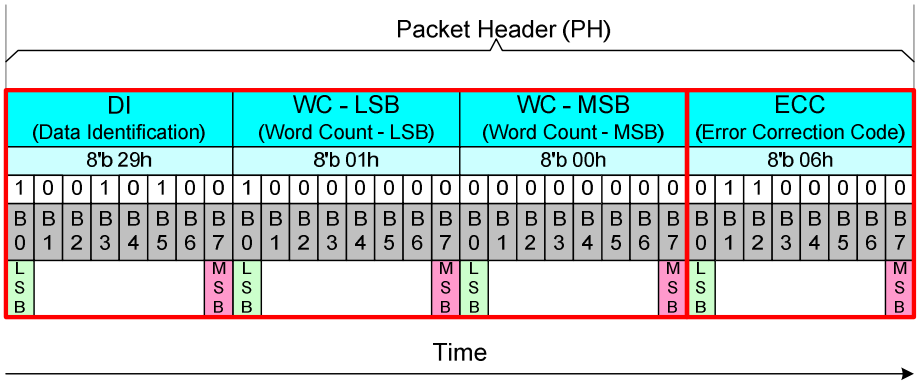


Figure 71: D [23…0] and P [7…0] of a Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors, but only a one-bit error will be corrected. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as below.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because the Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits (P [5…0]) for Error Correction Code (ECC) are needed.

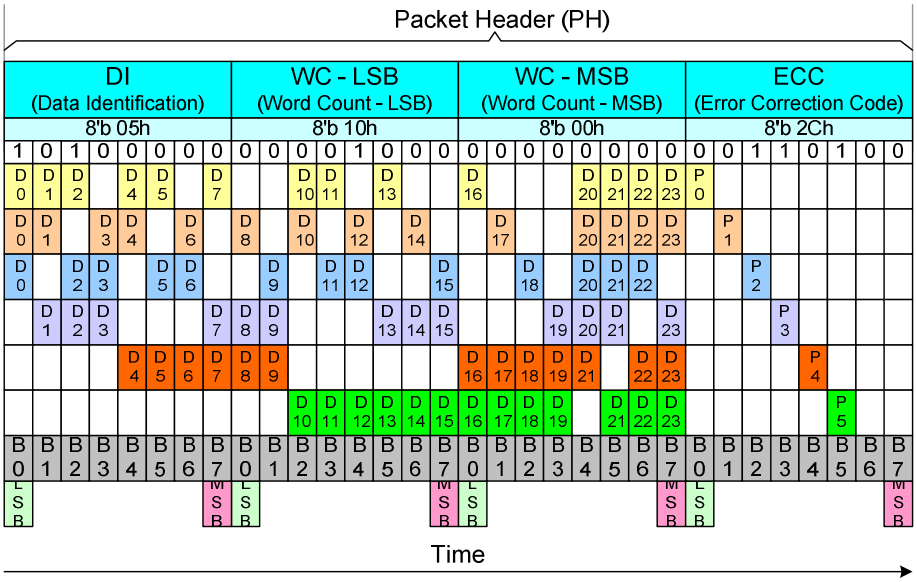


Figure 72: XOR Functionality in a Short Packet (SPa)

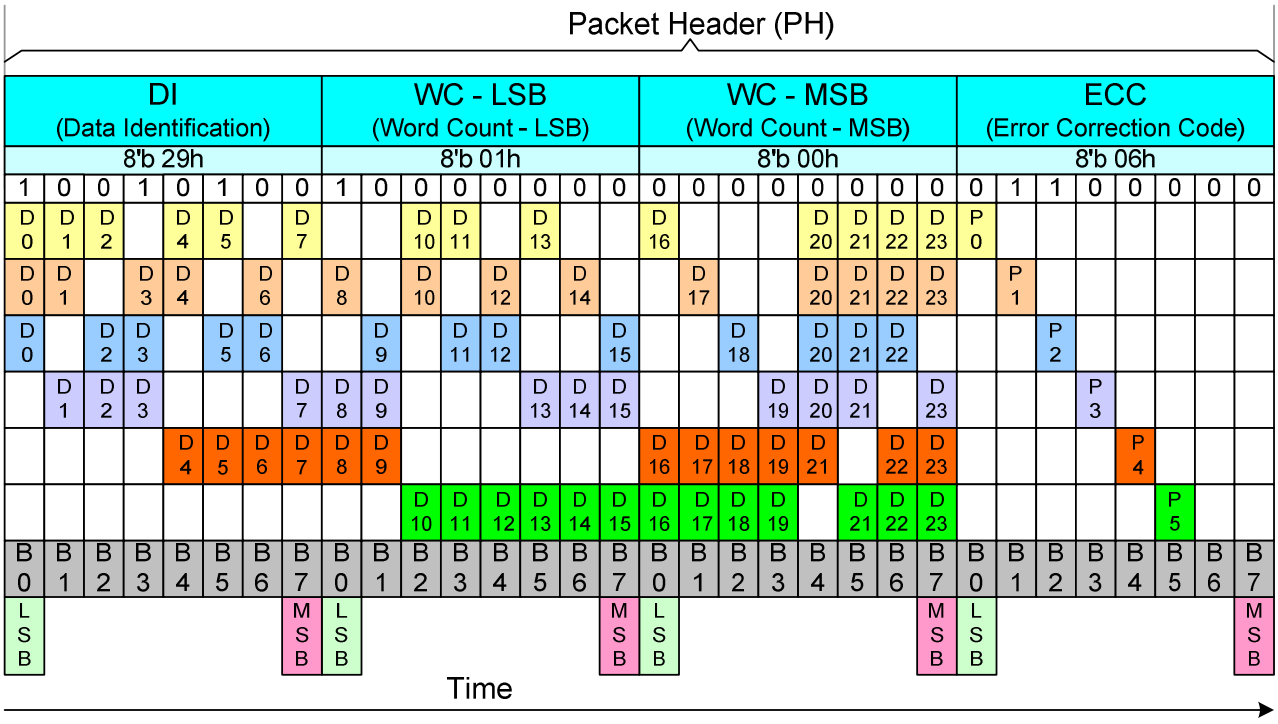


Figure 73: XOR Functionality in a Long Packet (LPa)

The transmitter (the MPU or the Display Module) sends data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (the Display module or the MPU) calculates an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MPU and the receiver is the display module, is illustrated below for reference purposes.

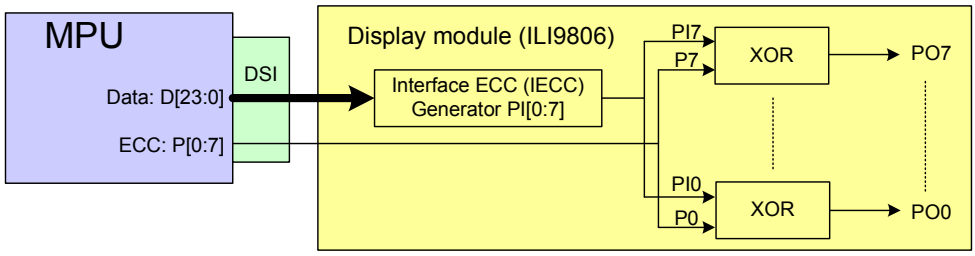


Figure 74: Internal Error Correction Code (IECC) on the Display Module (the Receiver)

The sent data bits (D [23…0]) and ECC (P [7…0]) are received correctly, if the value of the PO [7…0]) is 00h.

The sent data bits (D [23…0]) and ECC (P [7…0]) are not received correctly, if the value of the PO [7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 75: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 76: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D [23…0] on the transmitter side.

The amount of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

Table 16: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO [7…0] is found in Table 16: One Bit Error Value of the Error Correction Code (ECC), and the receiver can correct this one-bit error because this found value also defines the location of the corrupt bit, for example,

• PO [7…0] = 0Eh

• The bit of the data (D [23…0]), which is not correct, is D [3]

More than one error is detected if the value of the PO [7…0] is not in Table 16: One Bit Error Value of the Error Correction Code (ECC), for example, PO [7…0] = 0Ch.

3.12.32. Packet Data (PD) of a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is defined after the Packet Header (PH) of the Long Packet (LPa).

The amount of data bytes is defined in the chapter “Word Count (WC) of a Long Packet (LPa)”.

3.12.33. Packet Footer (PF) of a Long Packet (LPa)

The Packet Footer (PF) of a Long Packet (LPa) is defined after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is the checksum value which is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.

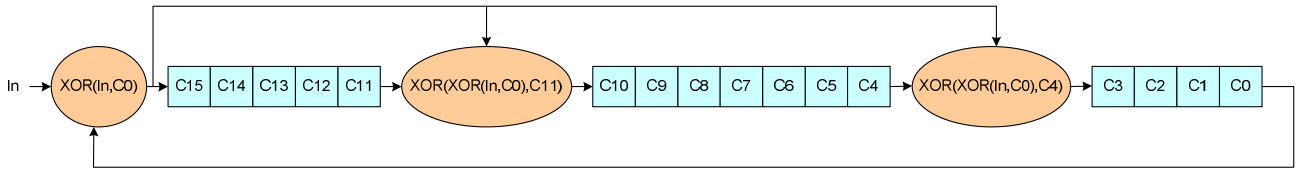
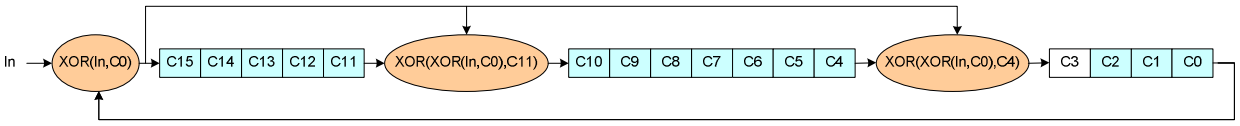


Figure 77: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.
The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit to be inputted into the 16-bit Cyclic Redundancy Check (CRC).
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 78: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example. This example (command 01h has been sent) is illustrated below.

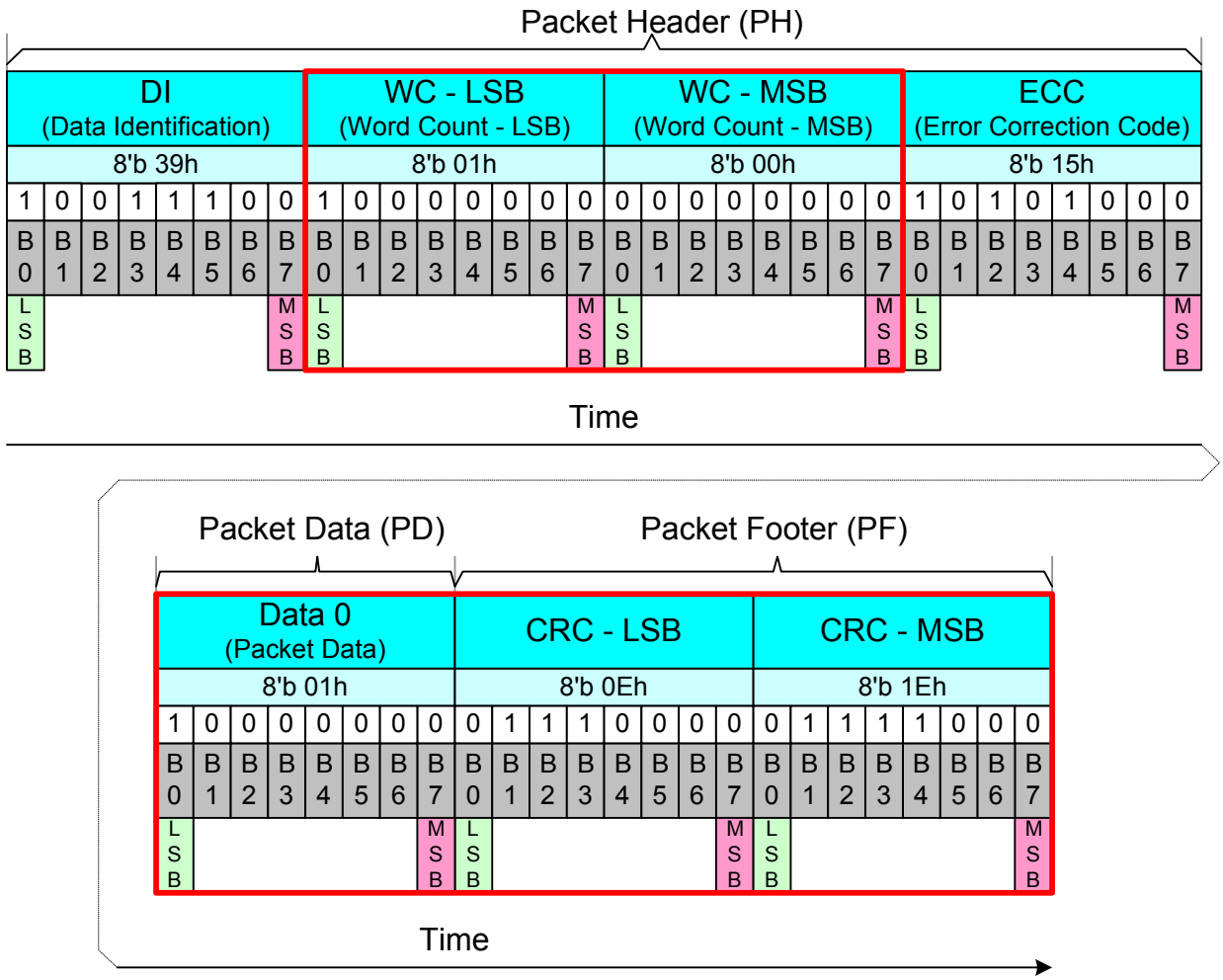


Figure 79: Packet Footer (PF) Example

The receiver calculates its own checksum value from the received Packet Data (PD). The receiver compares its own checksum with the Packet Footer (PF) which the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the checksums of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksums of the receiver and Packet Footer (PF) are not equal.

3.12.34. Packet Transmissions

3.12.35. Packet from the MPU to the Display Module

3.12.36. Display Command Set (DCS)

Display Command Set (DCS), which is defined in the Chapter 4.2 Command Description, is transmitted from the MPU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), which is included in a Short Packet (SPa) and a Long packet (LPa), as illustrated below.

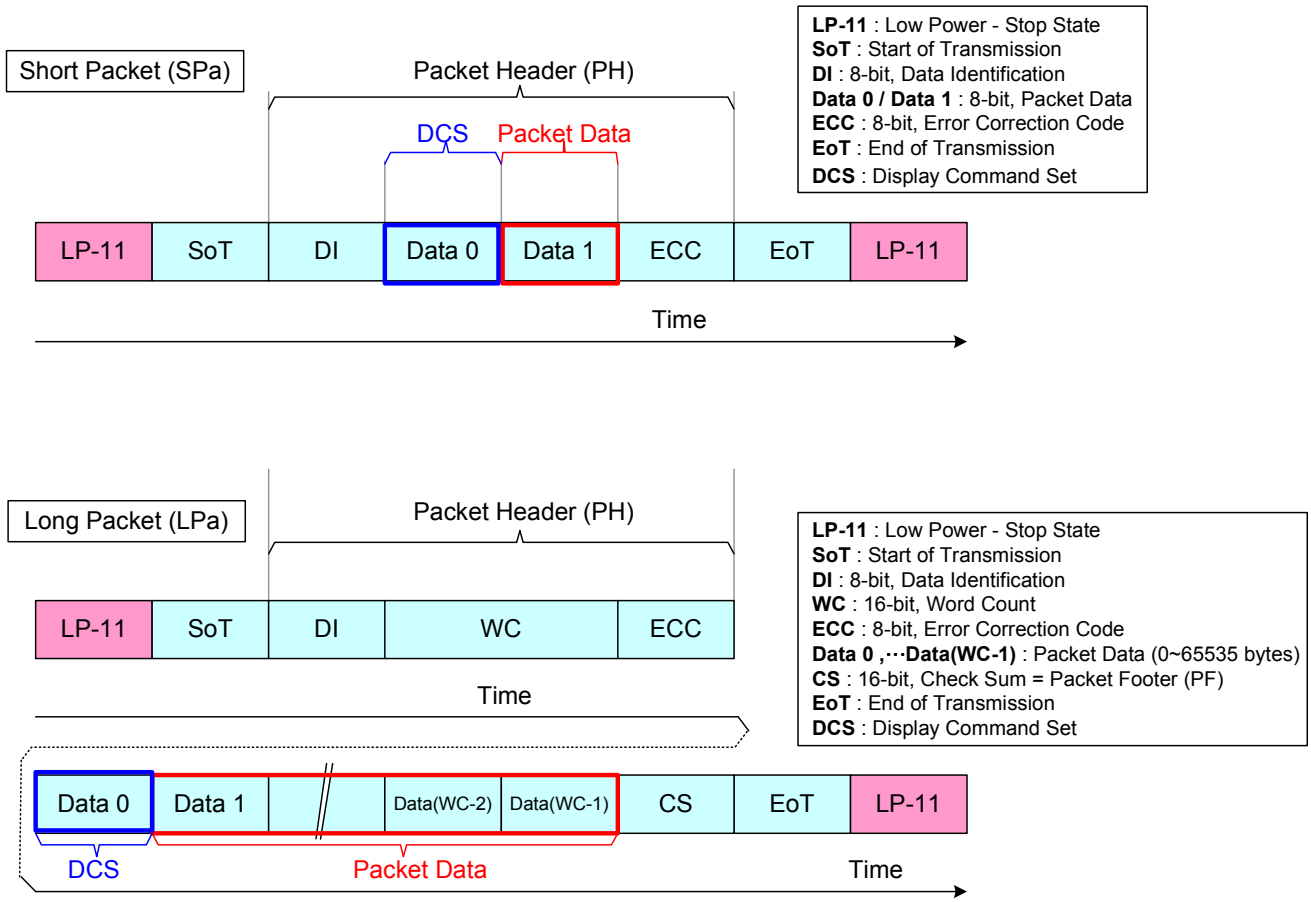


Figure 80: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

3.12.37. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter" is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0101b), from the MPU to the display module. These commands are defined in the table below. (See Chapter 5.2: Command Description.)

Table 17: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Partial Mode On (12h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)

A Short Packet (SPa) is defined as:

• Data Identification (DI)

o Virtual Channel (VC, DI [7…6]): 00b

o Data Type (DT, DI [5…0]): 00 0101b

• Packet Data (PD)

o Data 0: “Sleep In (10h)”, Display Command Set (DCS)

o Data 1: Always 00hex

• Error Correction Code (ECC)

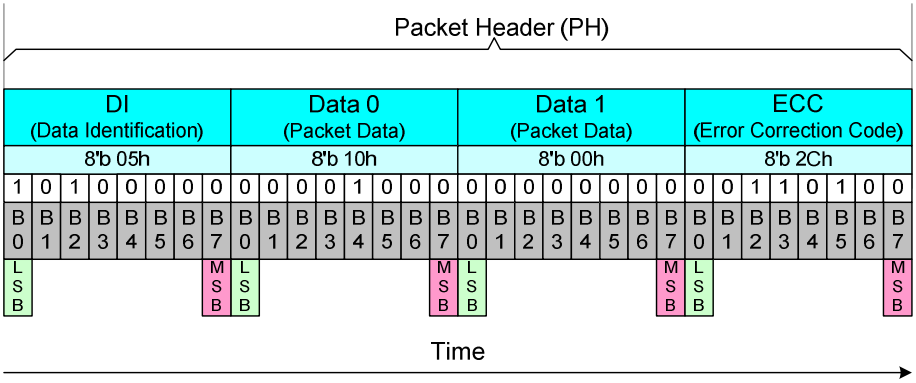


Figure 81: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

3.12.38. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 01 0101b), from the MPU to the display module. These commands are defined in the table below. (See chapter 5.2: Command Description.)

Table 18: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Set (26h)
Memory Write (2Ch), Note
Tearing Effect Line ON(35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

A Short Packet (SPa) is defined as:

• Data Identification (DI)

  o Virtual Channel (VC, DI [7…6]): 00b

  o Data Type (DT, DI [5…0]): 01 0101b

• Packet Data (PD)

  o Data 0: "Gamma Set (26h)", Display Command Set (DCS)

  o Data 1: 01hex, Parameter of the DCS

• Error Correction Code (ECC)

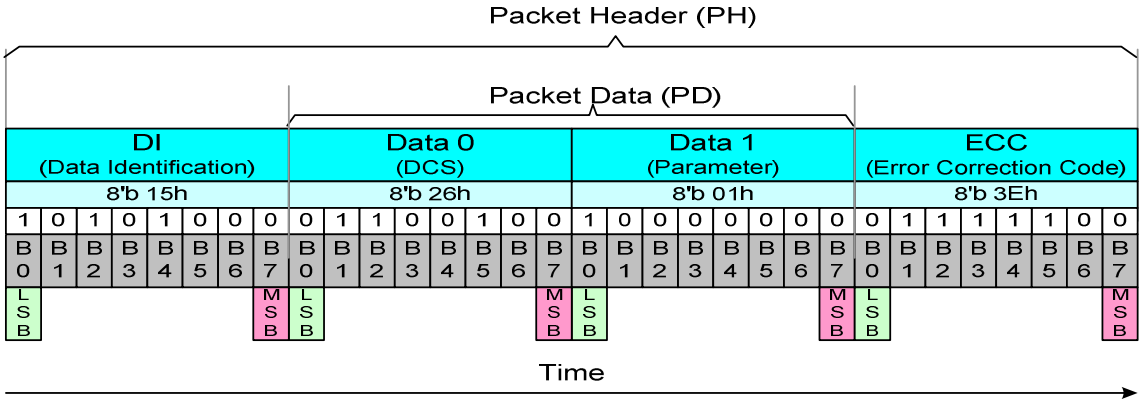


Figure 82: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

Note *One subpixel has been written.*

3.12.39. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 11 1001b), from the MPU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined in the table below. (See chapter 5.2: Command Description.)

Table 19: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h) , Note 1
Software Reset (01h) , Note 1
Sleep In(10h) , Note 1
Sleep Out (11h) , Note 1
Partial Mode On (12h) , Note 1
Normal Display Mode On (13h) , Note 1
All Pixel Off (22h)
All Pixel On (23h)
Gamma Set (26h), Note 2
Display Off (28h) , Note 1
Display ON (29h) , Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), Note 2
Partial Area (30h)
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note 2
Write Display Brightness (51h) , Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

A Long Packet (LPa), when one command (no Parameter) was sent, is defined as:

- Data Identification (DI)
  - o Virtual Channel (VC, DI [7…6]): 00b
  - o Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - o Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

Note 1 It can also be used in a Short Packet (SPa); See chapter "Display Command Set (DCS) Write, No Parameter".

Note 2 It can also be used in a Short Packet (SPa); See chapter "Display Command Set (DCS) Write, 1 Parameter".

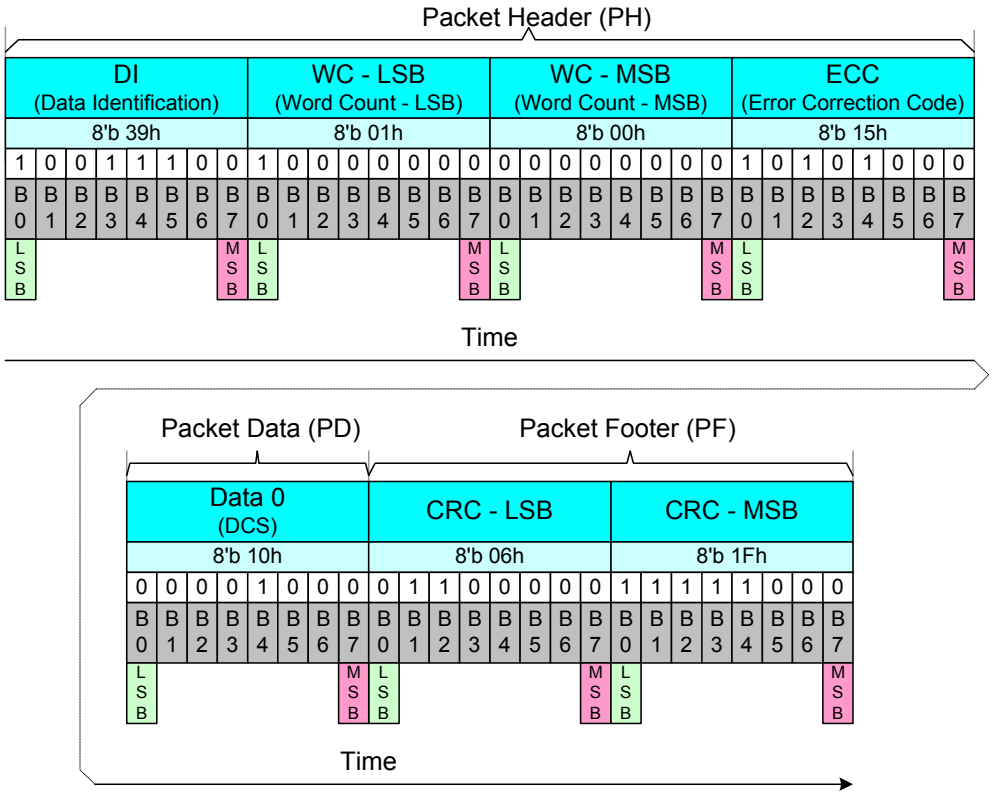


Figure 83: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa), when one Write (1 parameter) was sent, is defined as:

- Data Identification (DI)
  - o Virtual Channel (VC, DI [7…6]): 00b
  - o Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - o Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - o Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - o Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

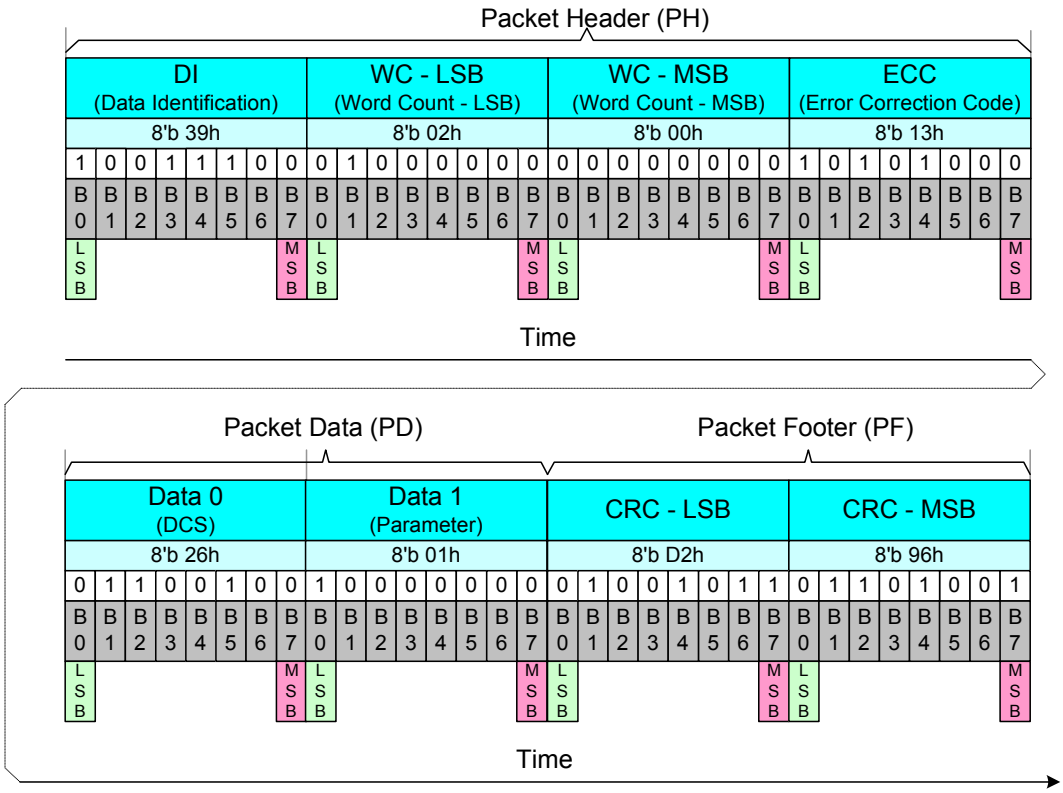


Figure 84: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa), when one Write (4 parameters) was sent, is defined as:

- Data Identification (DI)
  - o Virtual Channel (VC, DI [7…6]): 00b
  - o Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - o Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - o Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)
  - o Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - o Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - o Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - o Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

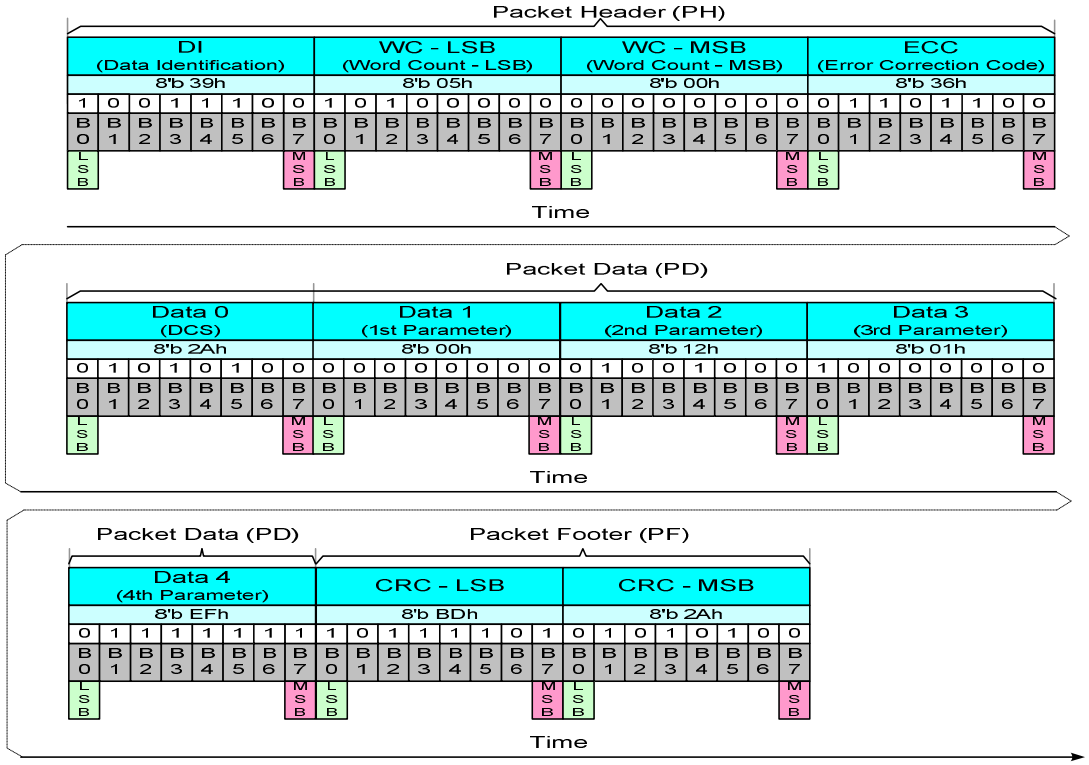


Figure 85: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

3.12.40. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 00 0110b), from the MPU to the display module. These commands are defined in the table below. (See Chapter 5.2: Command Description.)

Table 20: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Read Black/White Low Bits (70h)
Read Bkx (71h)
Read Bky(72h)
Read Wx (73h)
Read Wy (74h)
Read Red/Green Low Bits (75h)
Read Rx (76h)
Read Ry (77h)
Read Gx (78h)
Read Gy (79h)
Read Blue/A Color Low Bits (7Ah)
Read Bx (7Bh)
Read By (7Ch)
Read Ax (7Dh)
Read Ay (7Eh)
Read DDB Start (A1h)
Read DDB Continue (A8h)
First Checksum (AAh)
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MPU has to define to the display module the maximum size of the returned packet. A command used for this purpose is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which uses Short Packets (SPa) before the MPU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This sequence is illustrated below for reference purposes.

Step 1:

- The MPU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
    - o Virtual Channel (VC, DI [7…6]): 00b
    - o Data Type (DT, DI [5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
    - o Data 0: 01hex
    - o Data 1: 00hex
- Error Correction Code (ECC)

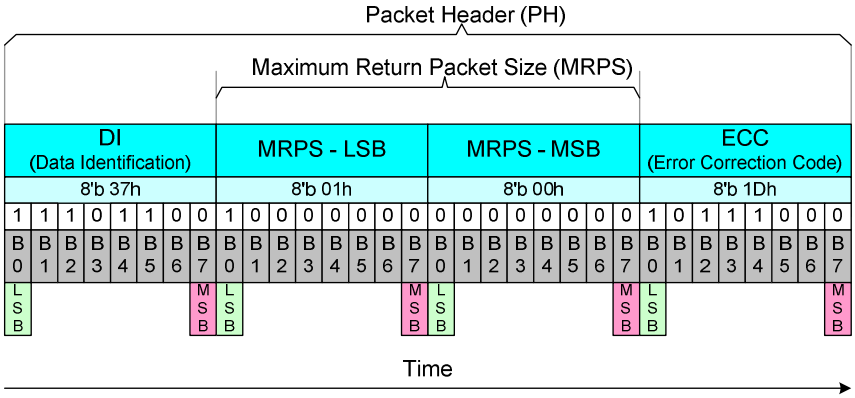


Figure 86 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

- The MPU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MPU sends “Display Command Set (DCS) Read, No Parameter” to the display module.
- Data Identification (DI)
    - o Virtual Channel (VC, DI [7…6]): 00b
    - o Data Type (DT, DI [5…0]): 00 0110b
- Packet Data (PD)
    - o Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
    - o Data 1: Always 00hex
- Error Correction Code (ECC)

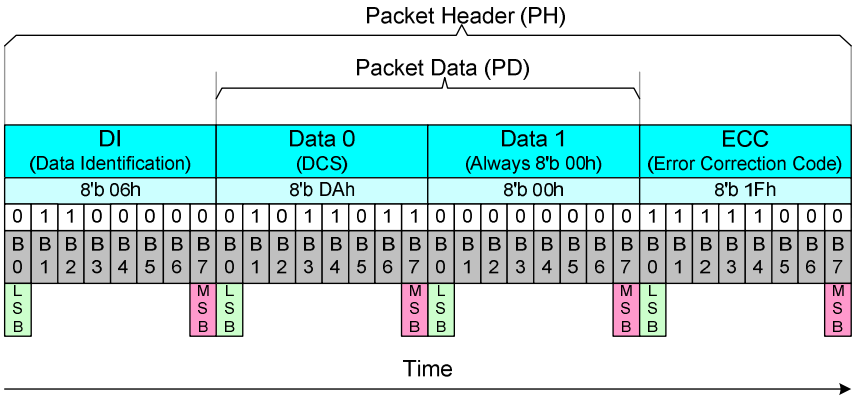


Figure 87 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MPU after the Bus Turnaround (BTA).

1. An acknowledge with Error Report (AwER): it is used in a Short Packet (SPa) if an error is found while receiving a command. See the chapter “Acknowledge with Error Report (AwER)”.
2. Information of the received command: it can be transmitted in a Short Packet (SPa) or Long Packet (LPa).

3.12.41. Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always used in a Long Packet (LPa), which is defined in the Data Type (DT, 001001b), from the MPU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT), if necessary.

The display module can ignore the Packet Data (PD), which is sent by the MPU.

A Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) are sent, is defined as:

• Data Identification (DI)
  o Virtual Channel (VC, DI [7…6]): 00b
  o Data Type (DT, DI [5…0]): 00 1001b
• Word Count (WC)
  o Word Count (WC): 0005hex
• Error Correction Code (ECC)
• Packet Data (PD):
  o Data 0: 89hex (Random data)
  o Data 1: 23hex (Random data)
  o Data 2: 12hex (Random data)
  o Data 3: A2hex (Random data)
  o Data 4: E2hex (Random data)

• Packet Footer (PF)

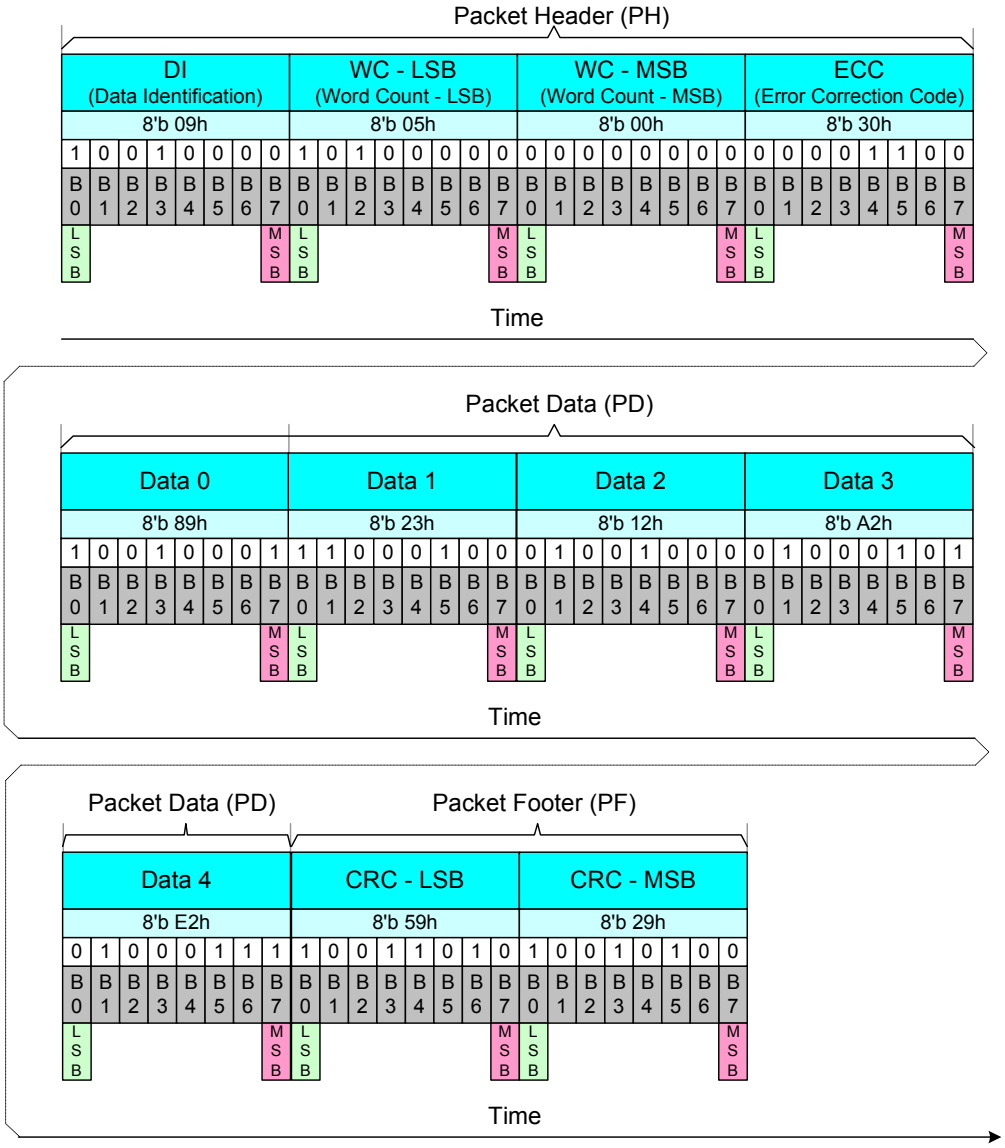


Figure 88: Null Packet, No Data (NP-L) - Example

3.12.42. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is defined in the Data Type (DT, 00 1000b) and optional in the interface level, is always used in a Short Packet (SPa) from the MPU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when the EoTP is added after the last payload packet before "End of Transmission" (EoT).

The MPU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MPU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module will/will not receive "End of Transmission Packet" (EoTP) from the MPU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving Escape mode), which ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MPU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 21: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MPU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MPU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) uses a fixed format as follows:

- Data Identification (DI)
  - o Virtual Channel (VC, DI [7…6]): 00b
  - o Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - o Data 0: 0Fhex
  - o Data 1: 0Fhex
- Error Correction Code (ECC)
  - o ECC: 01hex

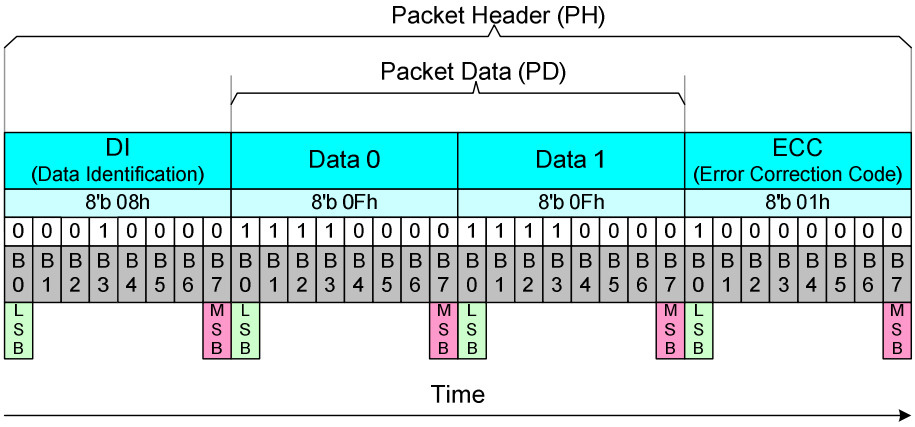


Figure 89: End of Transmission Packet (EoTP)

Some cases of the “End of Transmission Packet” (EoTP) are illustrated below for reference purpose only.

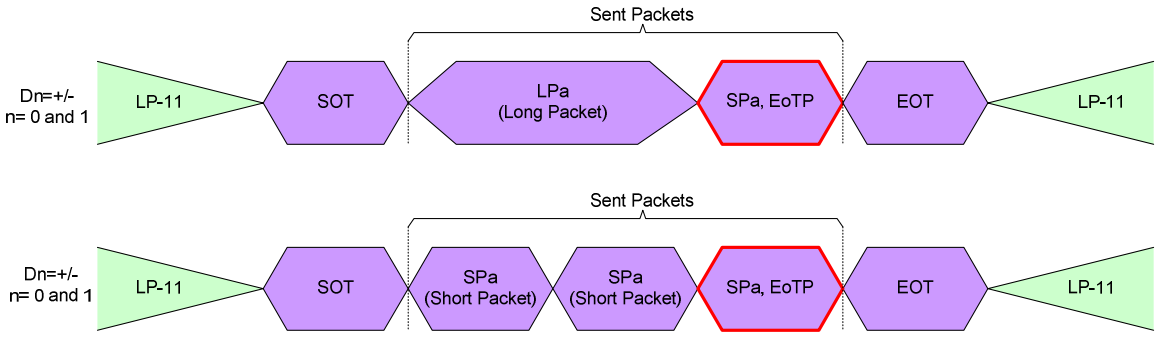


Figure 90: End of Transmission Packet (EoTP) - Examples

3.12.43. Packet from the Display Module to the MPU

3.12.44. Used Packet Types

The display module can use Short Packets (SPa) or Long Packets (LPa) when it returns information to the MPU after the MPU requests information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See the chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined in the Data Type (DT). See the chapter “Data Type (DT)”. If the maximum size of the Packet Data (PD) could be sent in one packet, then the display module cannot separate returned bytes into several packets.

Both cases are illustrated below for reference purpose.

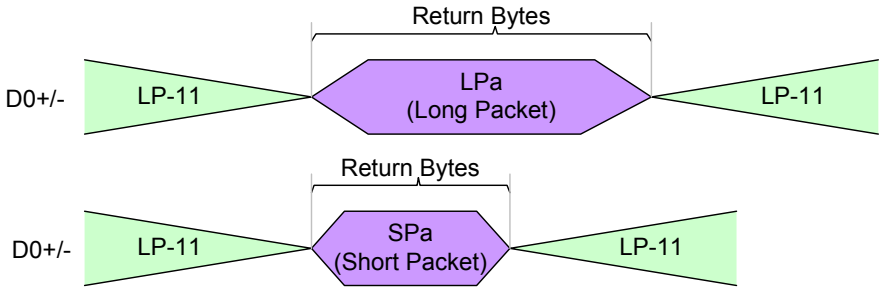


Figure 91: Return Bytes in a Single Packet

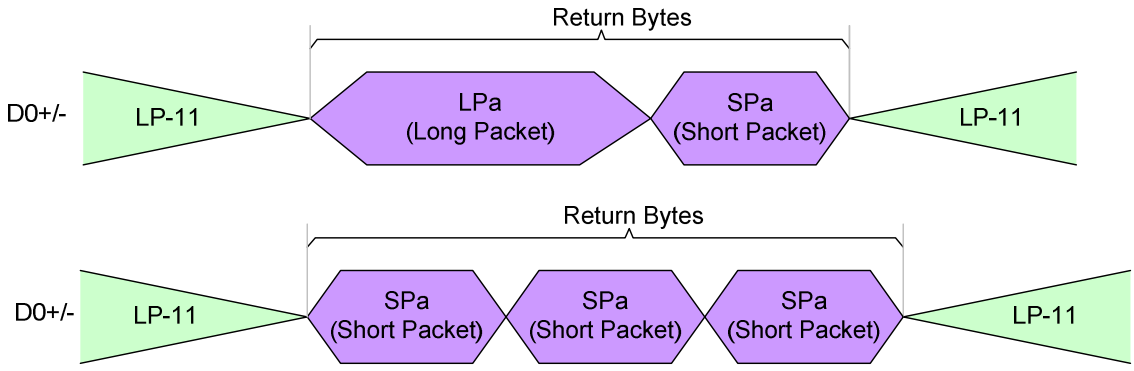


Figure 92: Return Bytes in Several Packets – Not Allowed

Exception:

The display module returns 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MPU when the display module receives a read command (see the chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”), in which a single bit error is detected and corrected by the EEC (see bit 8 in “Table 23: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”).

These returned packets are illustrated below for reference purpose.

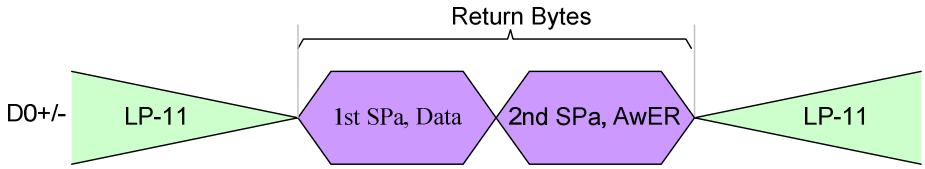


Figure 93: Exception when Return Bytes in Several Packets

AwER = Acknowledge with Error Report

3.12.45. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER), which is defined in the Data Type (DT, 00 0010b), is always transmitted through a Short Packet (SPa) from the display module to the MPU. The 16 bits in the Packet Data (PD) can indicate the current error(s) if one or more than one bit(s) is/are set to 1, as defined in the following table.

Table 22: Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

Table 23: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to 0 internally (Only for Long Packet (LP)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages, which are received from the MPU to the display module, before the Bus Turnaround (BTA).

The display module ignores the received packet which includes an error or errors.

Acknowledge with Error Report (AwER) in a Short Packet (SPa) is defined as:

• Data Identification (DI)
  o Virtual Channel (VC, DI [7…6]): 00b
  o Data Type (DT, DI [5…0]): 00 0010b
• Packet Data (PD)
  o Bit 8: ECC Error, single-bit (detected and corrected)
  o AwER: 0100h
• Error Correction Code (ECC)

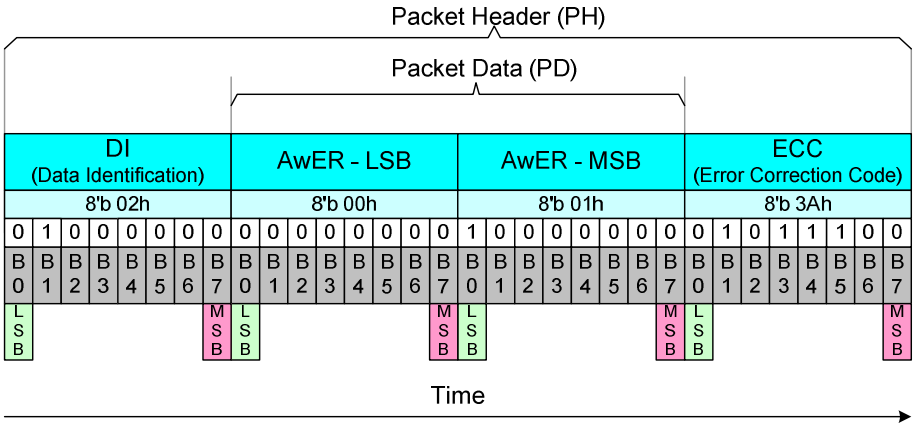


Figure 94: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MPU before the MPU performs the Bus Turnaround (BTA). Some examples are illustrated below for reference purpose.

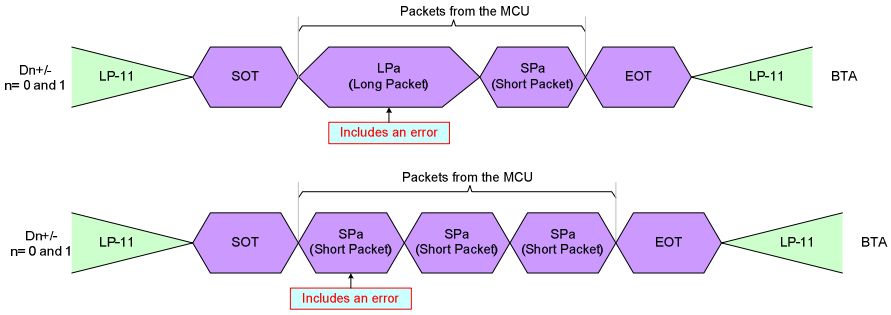


Figure 95: Errors Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets are indicated by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. If a received packet includes an error, the bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1.

The numbers of the packets, including an ***ECC or CRC*** error, are calculated in the RDNUMED register, which can read the “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MPU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated below for reference purpose.

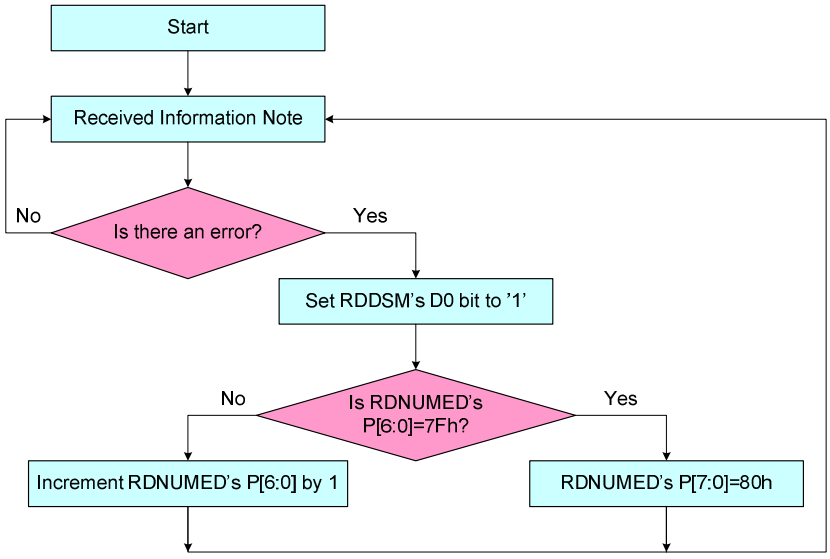


Figure 96: Flow Chart for Errors on DSI[Note]

Note 1. This information can be Interface or Packet Level Communication but it is always from the MPU to the display module in this case.

2. CRC or ECC error

3.12.46. DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in the Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MPU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MPU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

• Data Identification (DI)
  o Virtual Channel (VC, DI [7…6]): 00b
  o Data Type (DT, DI [5…0]): 01 1100b
• Word Count (WC)
  o Word Count (WC): 0005hex
• Error Correction Code (ECC)
• Packet Data (PD):
  o Data 0: 89hex
  o Data 1: 23hex
  o Data 2: 12hex
  o Data 3: A2hex
  o Data 4: E2hex
• Packet Footer (PF)

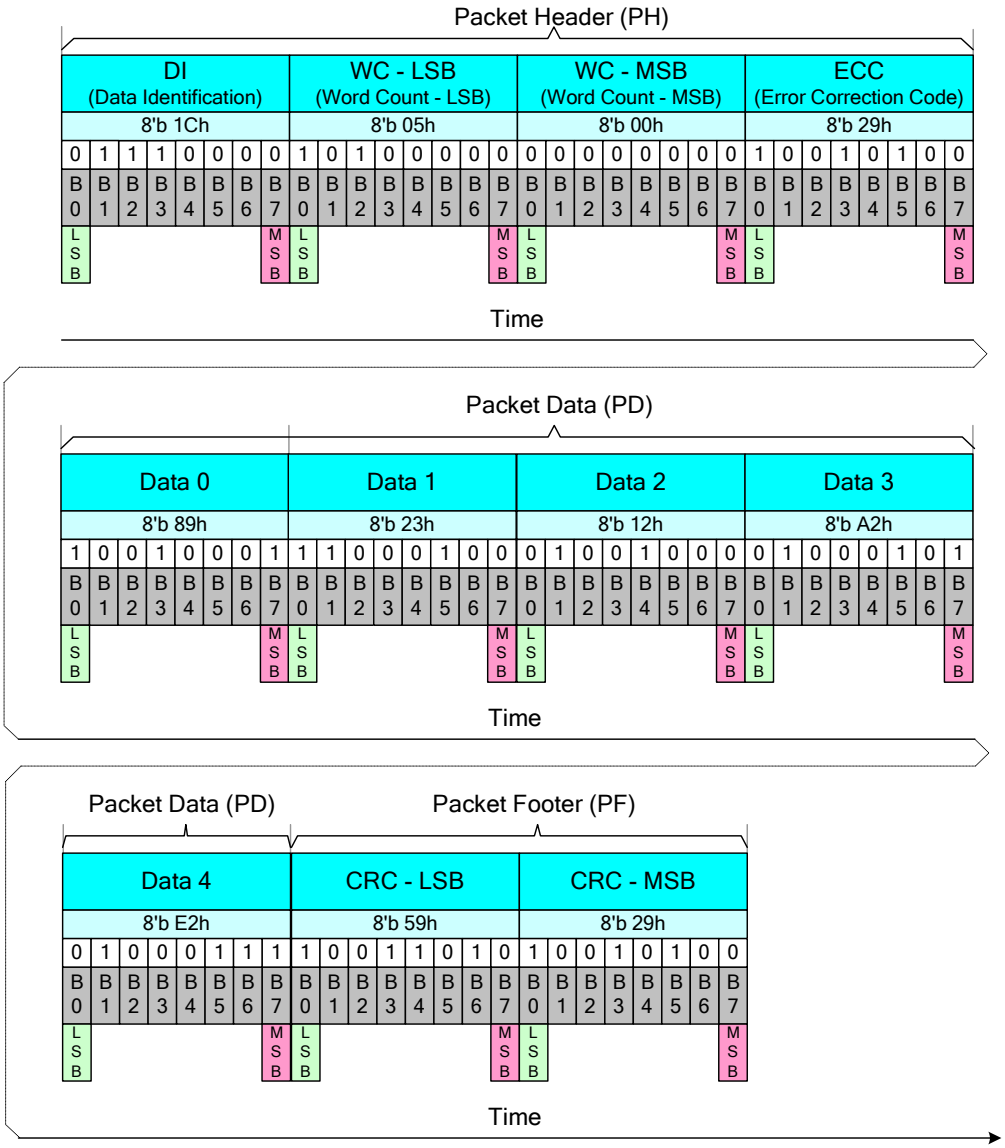


Figure 97: DCS Read Long Response (DCSRR-L) - Example

3.12.47. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned", which is defined in the Data Type (DT, 10 0001b), (DCSRR1-S) is always used in a Short Packet (SPa) from the display module to the MPU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MPU has sent to the display module.

A Short Packet (SPa) is defined as:

• Data Identification (DI)
  o Virtual Channel (VC, DI [7…6]): 00b
  o Data Type (DT, DI [5…0]): 10 0001b
• Packet Data (PD)
  o Data 0: 45hex
  o Data 1: 00hex (Always)
• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

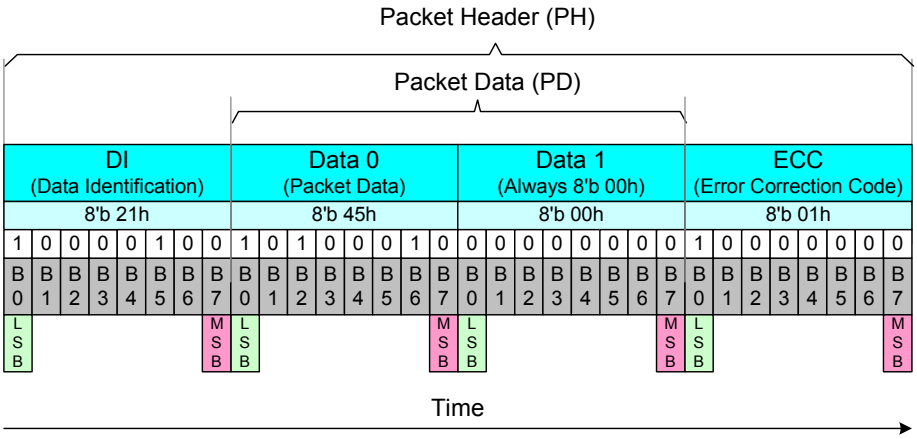


Figure 98: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

3.12.48. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always used in a Short Packet (SPa), which is defined in the Data Type (DT, 10 0010b), from the display module to the MPU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MPU has sent to the display module.

A Short Packet (SPa) is defined as:

• Data Identification (DI)
  o Virtual Channel (VC, DI [7…6]): 00b
  o Data Type (DT, DI [5…0]): 10 0010b
• Packet Data (PD)
  o Data 0: 45hex
  o Data 1: 32hex
• Error Correction Code (ECC)

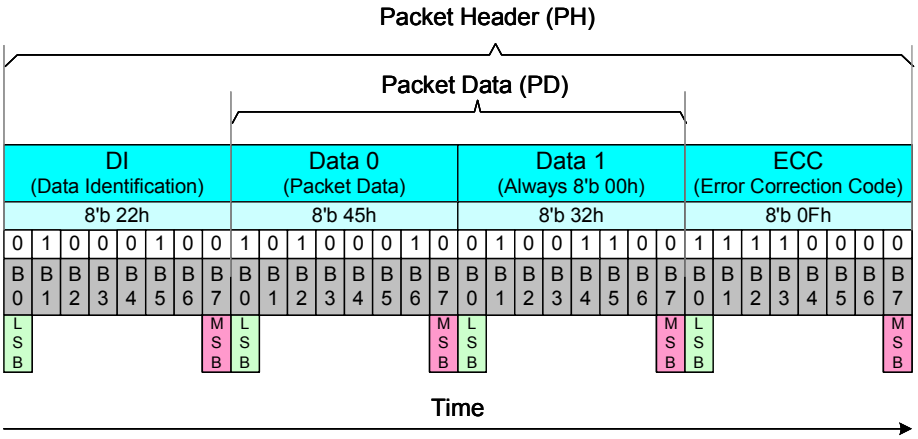


Figure 99: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

3.12.49. Communication Sequences

3.12.50. General

The communication sequences can be done on interface or packet levels between the MPU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes (DSI-D0+/- and DSI-D1+/-), and it is assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See the chapter “DSI-CLK Lanes”.

Functions of the interface level communication are described in the following table.

Table 24: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 25: Packet Level Communication

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MPU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
Display Module (ILI9806)	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

3.12.51. Sequences

3.12.52. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined in the chapter "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)", and examples of sequences on how this packet is used is described in the following tables.

Table 26: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 27: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 28: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

3.12.53. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined in the chapter "Display Command Set (DCS) Write, No Parameter (DCSWN-S)", and examples of sequences on how this packet is used are described in the following tables.

Table 29: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 30: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 31: DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

3.12.54. DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined in the chapter "Display Command Set (DCS) Write Long (DCSW-L)", and examples of sequences on how this packet is used are described in the following tables.

Table 32: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 33: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 34: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

Table 35: DCS Write Long Sequence – Example 4[Note]

DCS Write Long Sequence – Example 4						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	Memory Write (2Ch)
3	DCSW-L	HSDT	→	--	--	Memory Write Continue (3Ch)
4	DCSW-L	HSDT	→	--	--	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	→	--	--	Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	→	--	--	End of Transmission Packet
7	--	LP-11	→	--	--	End

3.12.55. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined in the chapter "Display Command Set (DCS) Read, No Parameter (DCSRN-S)", and examples of sequences on how this packet is used are described in the following tables.

Table 36: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
17	--	LP-11	→	--	--	End
18						

Note This is an example that image data are sent in 4 packets.

19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
23	--	LP-11	→	--	--	End

Table 37: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ”Memory Read” (2Eh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
23	--	LP-11	→	--	--	End

3.12.56. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined in the chapter “Null Packet, No Data (NP-L)”, and an example of sequence on how this packet is used is described in the following table.

Table 38: Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

3.12.57. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined in the chapter “End of Transmission Packet (EoTP)”, and an example of sequence on how this packet is used is described in the following table.

Table 39: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MPU		Information Direction	Display Module (ILI9806)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

3.12.58. 16 Bit/Pixel Writing

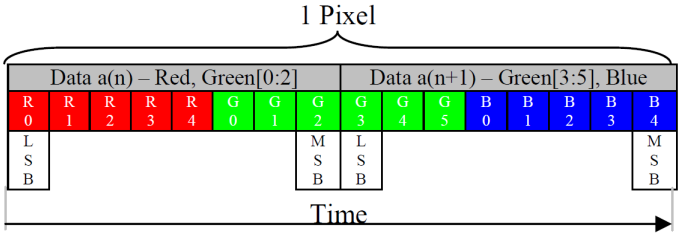


Figure 100: One Pixel Bit and Write Color Orders

The MPU can send the following packet to the display module.

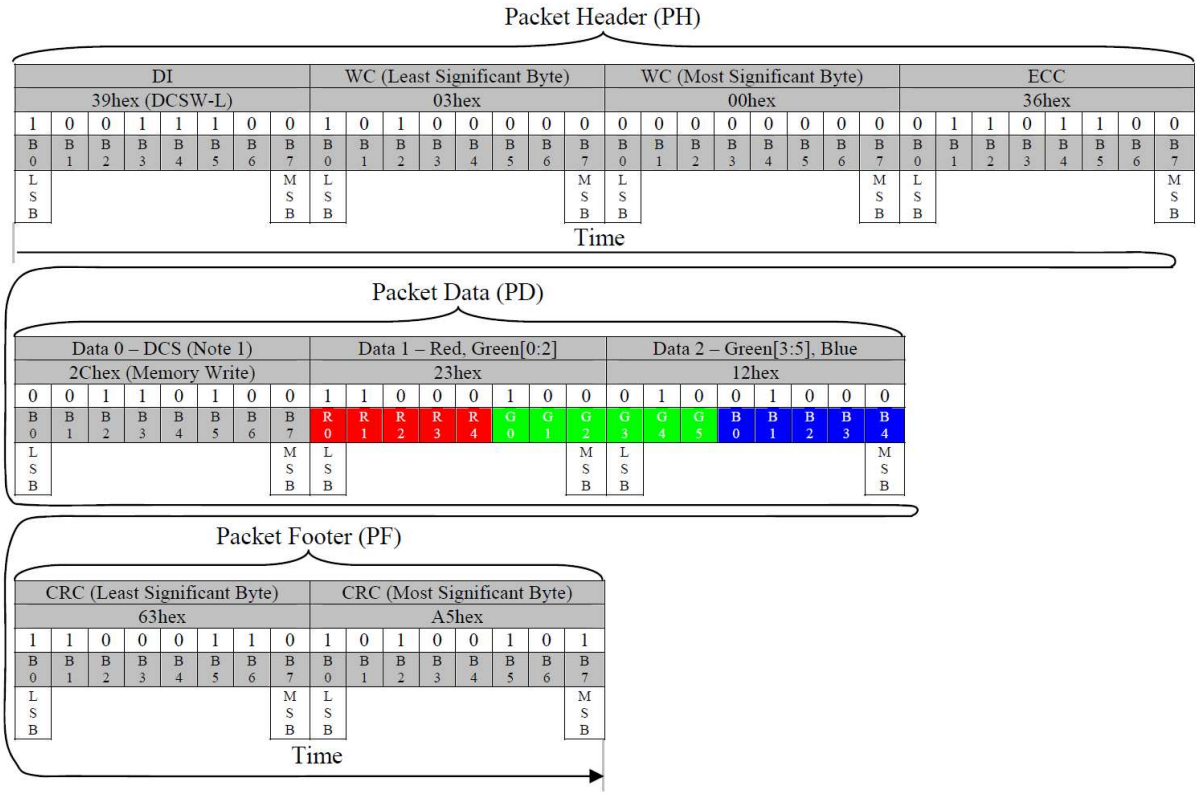


Figure 101: One Pixel Write (DCSW-L) – Example 1[Note]

Note
1. *DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.*
2. *It is possible that one pixel information is split into different packets which end and star as follows: RG – GB (2 packets).*
3. *A packet can include several pixels (not just one pixel as in this example).*

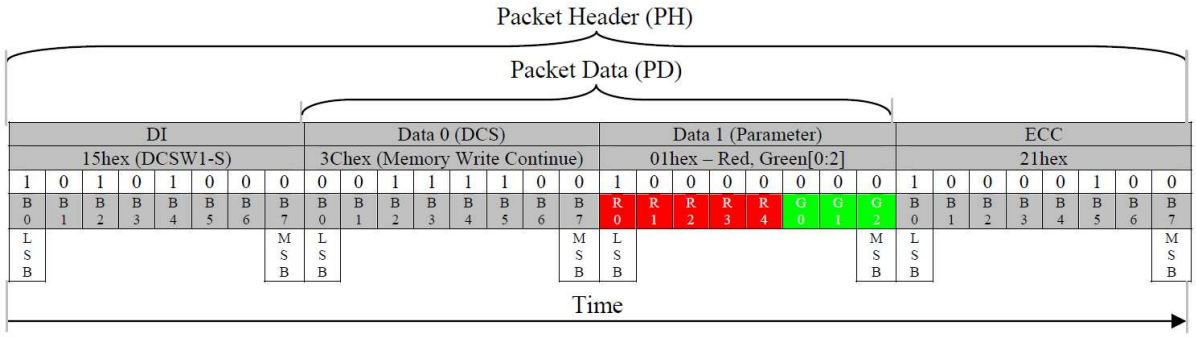


Figure 102: Red/Green [0:2] Subpixel Write (DCSW1-S) – Example 2[Note 1]

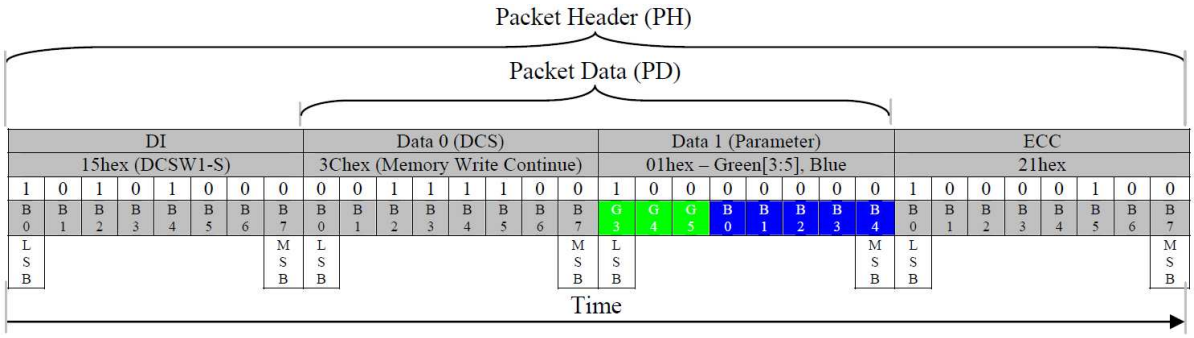


Figure 103: Green [3:5]/Blue Subpixel Write (DCSW1-S) – Example 3[Note 2]

3.12.59. 24 Bit/Pixel Writing

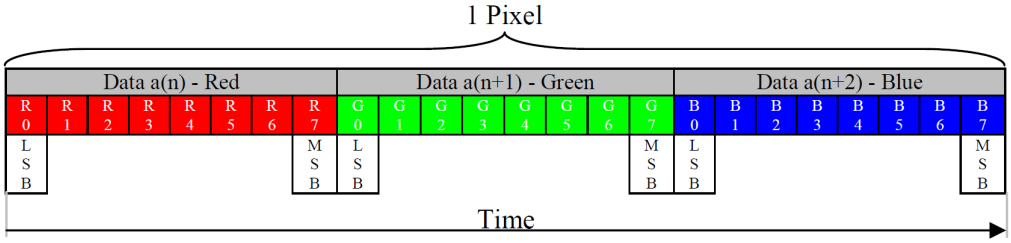


Figure 104: One Pixel Bit and Color Write Orders

The MPU can send the following packet to the display module.

Note 1 DCS (Data 0) can also be "Memory Write" (2Ch) command.

Note 2 1. DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch).
2. Previous data byte is R [0:4] G [0:2].

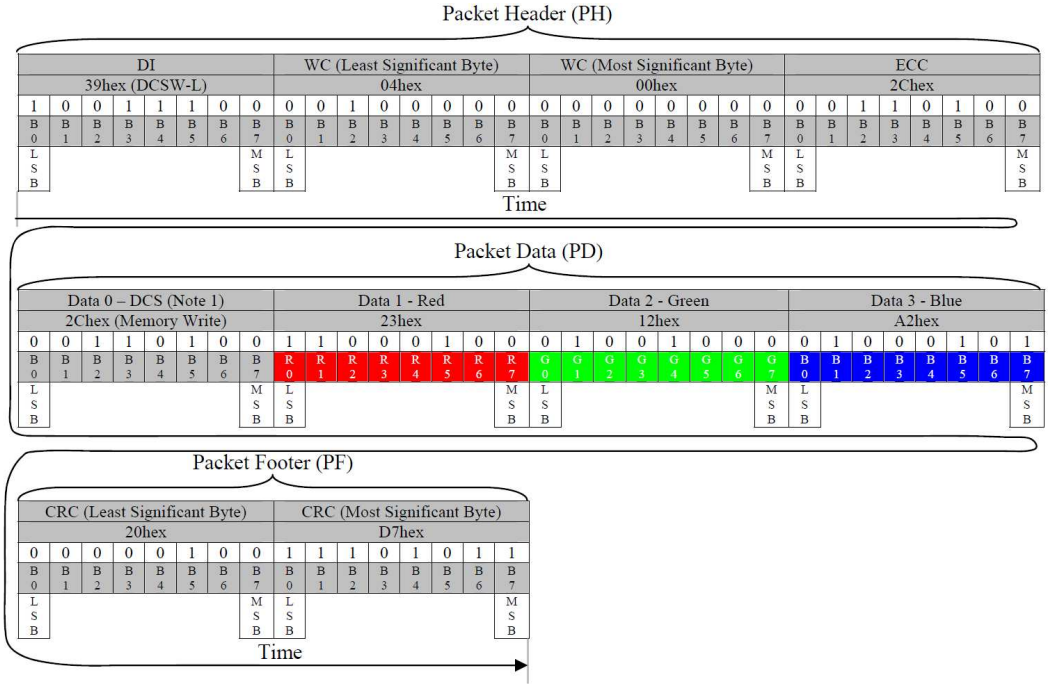


Figure 105: One Pixel Write (DCSW-L) – Example[Note]

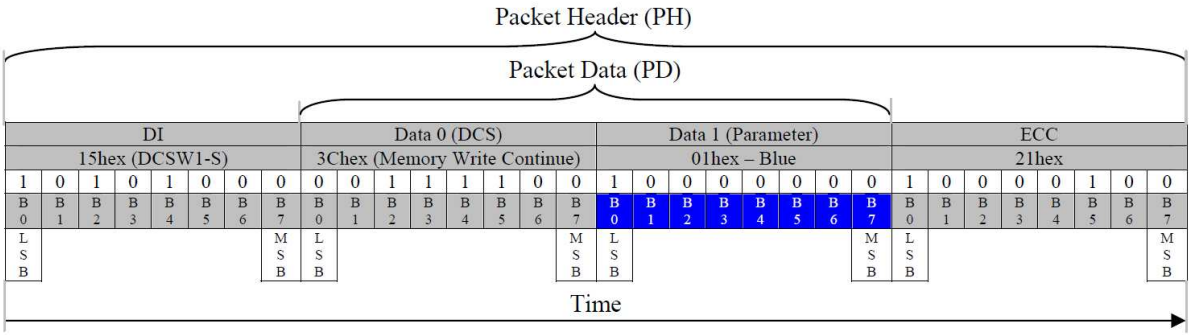


Figure 106: Blue Subpixel Write (DCSW1-S) – Example 2

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch)
2. Previous data byte is G [0:7].

Note 1. DCS (Data 0) can be Memory Write (2Ch) or Memory Write Continue (3Ch) command.
2. It is possible that one pixel information is split in two or three different packets which end and start as follows:
- *R – GB (2 packets)*
- *RG – B (2 packets)*
- *R – G – B (3 packets)*

3. A packet can include several pixels (not just one pixel as in this example).

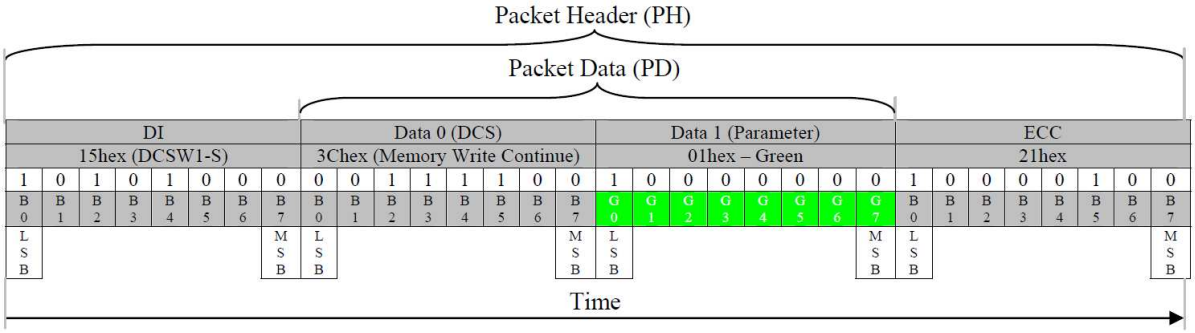


Figure 107: Green Subpixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be “Memory Write” (2Ch) command. It must always be “Memory Write Continue” (3Ch)
2. Previous data byte is R [0:7].

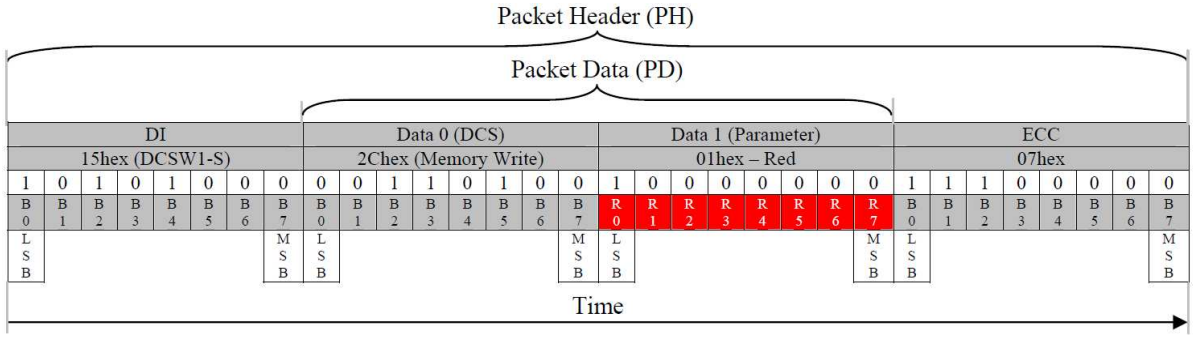


Figure 108: Red Subpixel Write (DCSW1-S) – Example 4

Notes:

1. DCS (Data 0) can also be “Memory Write Continue” (3Ch) command.
2. Previous data byte is B [0:7].

3.12.60. 24 bit/pixel Reading

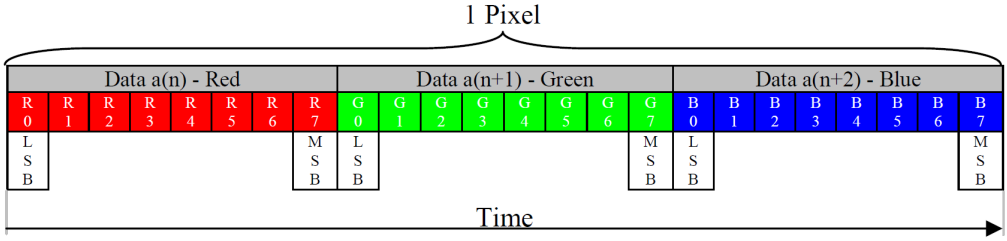


Figure 109: One Pixel Bit and Color Read Order

The display module can send following packets to the MPU after the MPU has sent a read command “Memory Read (2Eh)” or “Memory Read Continue (3Eh)”.

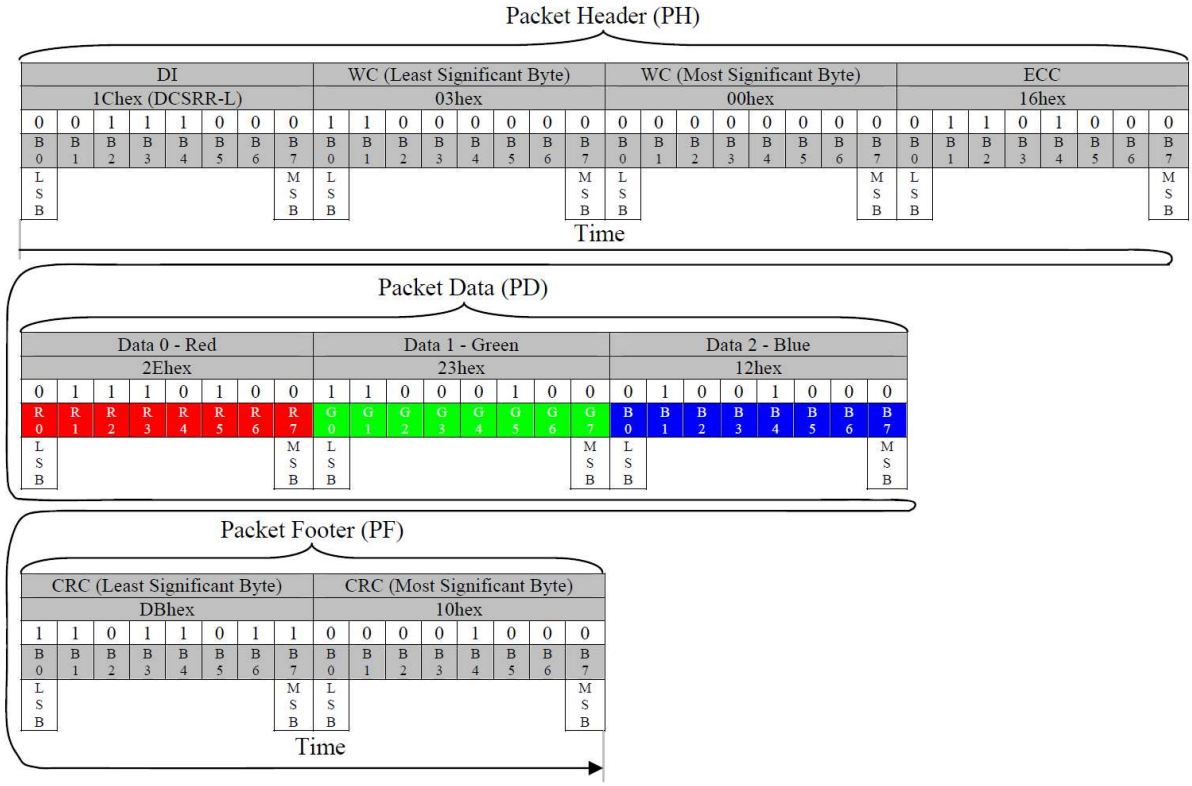


Figure 110: One Pixel Read Response (DCSRR-L) – Example 1

Note: It is possible that one pixel information is split in two or three different packets:

- R – GB (2 packets)
- RG – B (2 packets)
- R – G – B (3 packets)

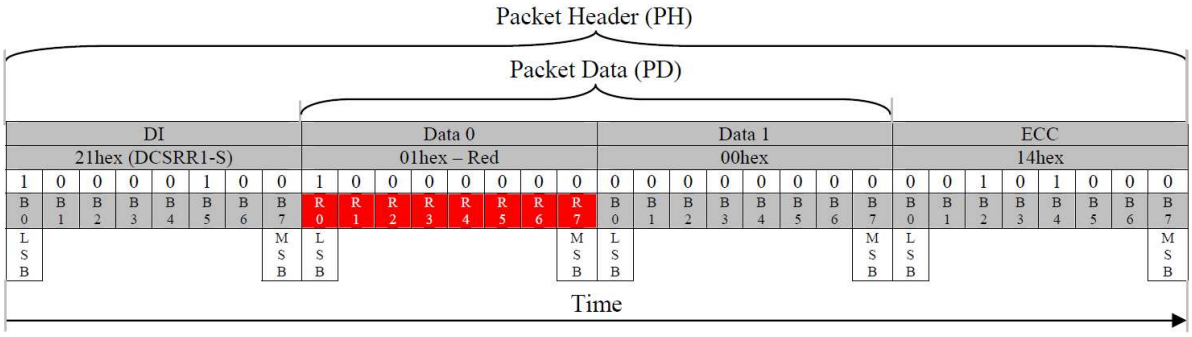


Figure 111: Red Subpixel Response (DCSRR1-S) – Example 2

Notes:

1. Data 1 is always 00h.
2. Previous data byte is B [0:7].

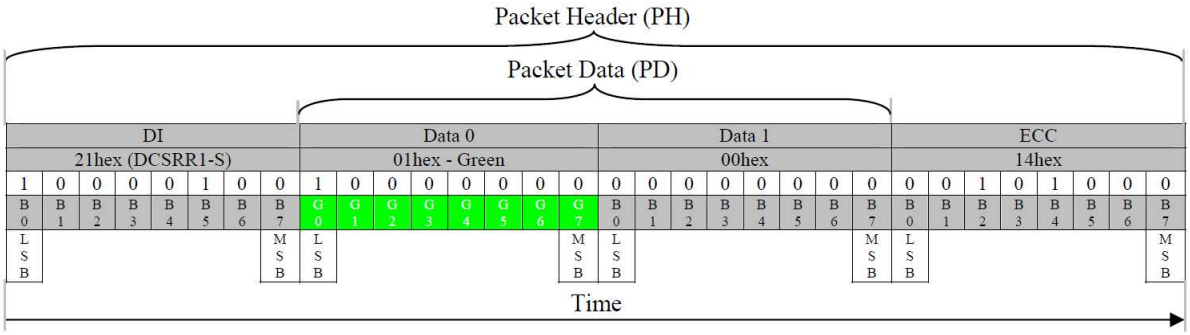


Figure 112: Green Subpixel Response (DCSRR1-S) – Example 3

Notes:

1. Data 1 is always 00h.
2. Previous data byte is R [0:7].

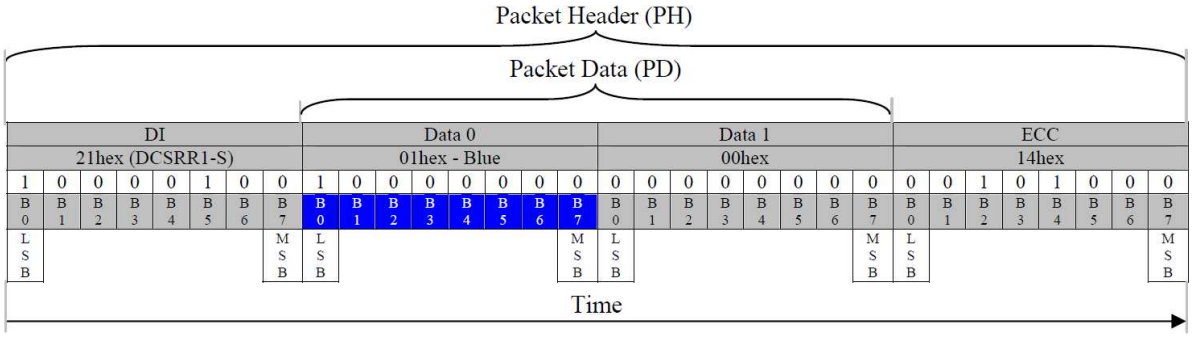


Figure 113: Blue Subpixel Response (DCSRR1-S) – Example 4

Notes:

1. Data 1 is always 00h.
2. Previous data byte is G [0:7].

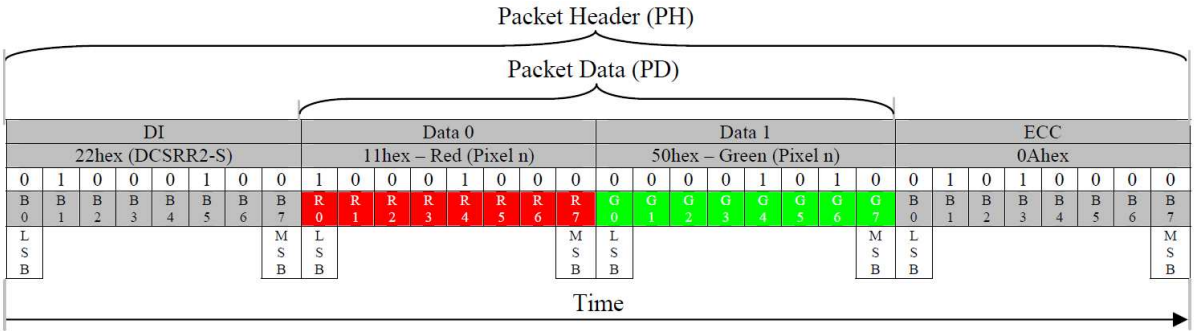


Figure 114: Red and Green Subpixels Response (DCSRR2-S) – Example 5

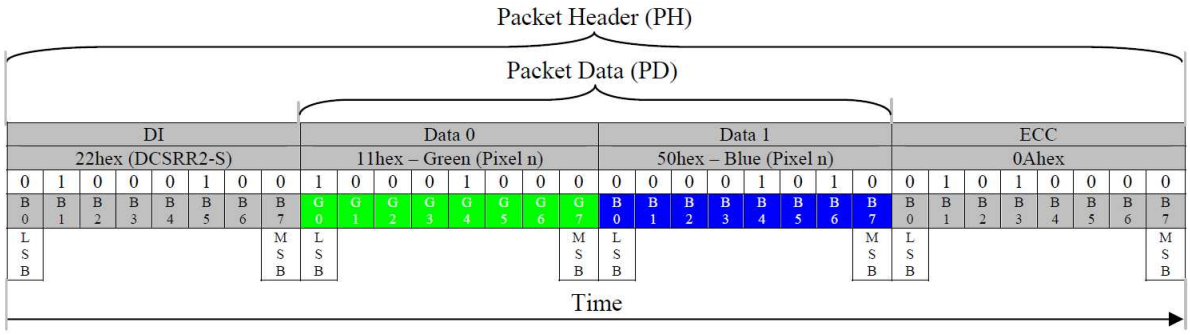


Figure 115: Green and Blue Subpixels Response (DCSRR2-S) – Example 6

Note: Previous data byte is R [0:7].

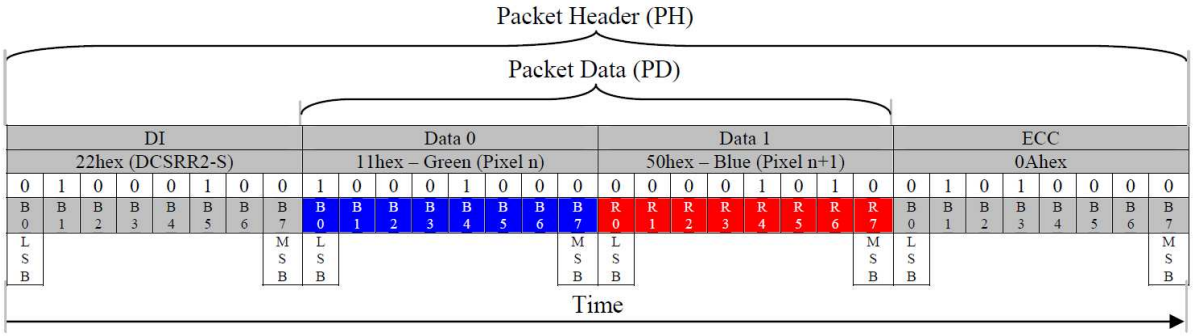


Figure 116: Blue and Red Subpixels Response (DCSRR2-S) – Example 7

Note: Previous data byte is G [0:7].

3.13. MDDI (Mobile Display Digital Interface)

MDDI (Mobile Display Digital Interface) is a differential small amplitude serial interface for high-speed data transfer via 4 lines: Stb+/- (HS_CP, HS_CN), Data+/- (D_P, D_N). The specifications of MDDI supported by the ILI9806 are compatible to the MDDI specifications disclosed by Video Electronics Standards Association (VESA). The MDDI specifications of the ILI9806 are listed below[Note].

ILI9806 MDDI Specifications

- MDDI specification version V1.2 , support Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data0+/- lines
- MDDI client: the ILI9806 enables direct connection to the Base Band (BB) chip without bridge chip
- Cost/performance optimized interface for mobile display systems:
  1. Only internal mode (one client) and Forward Link are supported
  2. Hibernation mode to save power consumption
  3. Tearing-free moving picture display via TE/VSYNC interface
  4. Moving picture display with low power consumption, realized by the features 2 ~ 3
  5. Shutdown mode for saving power consumption in the standby state

Incorporates an output port for sub-display interface or peripheral control providing single-chip solution for MDDI mobile display systems

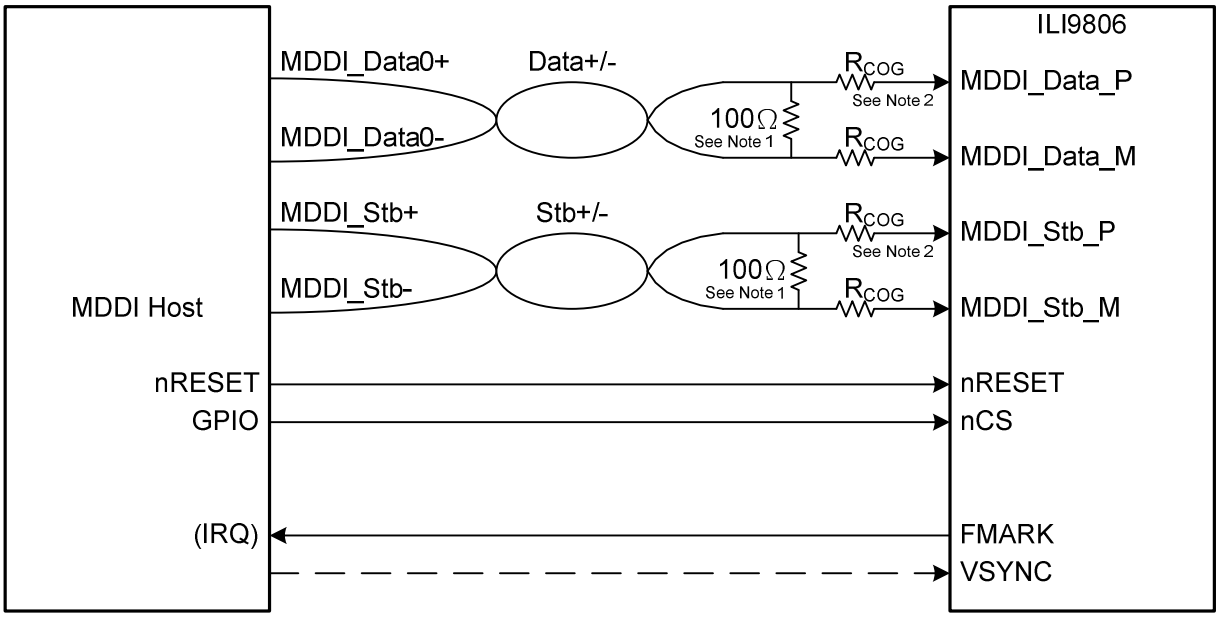


Figure 117: Physical Connection of Host and ILI9806, Type 1 External Mode Minimum Configuration

Note 1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines.

2. Make the COG wiring resistances of Data+/- and Stb+/- lines as small as possible (RCOG < 10 ohm).

MDDI Link Protocol (Packets Supported by the ILI9806)

The MDDI Link Protocol of the ILI9806 is compliant with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ILI9806 are listed in Table 40.

Note: DO NOT send packets which are not supported by the ILI9806.

For the MDDI packet structure, a sub-frame header packet is placed in front of a sub-frame, and some sub-frames together construct a media-frame. The Table 40 describes nine types of packets supported in the ILI9806.

Table 40: List of Supported MDDI Packets

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

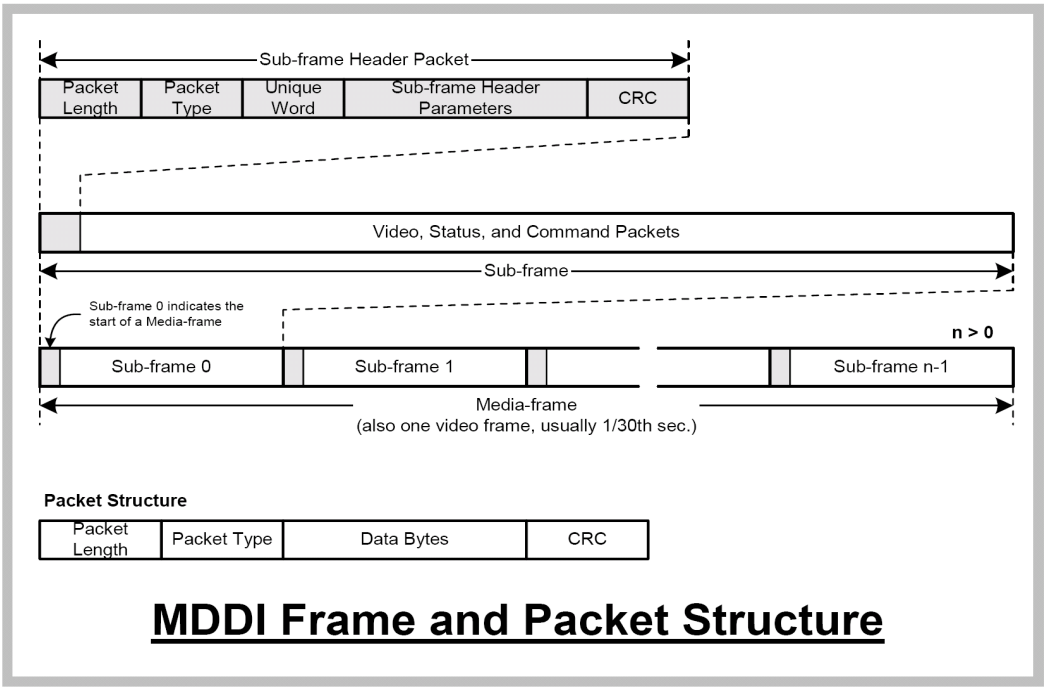


Figure 118: Forward Link Structure

Sub-frame Header Packet

The Sub-Frame Header Packet is the first packet of every sub-frame.

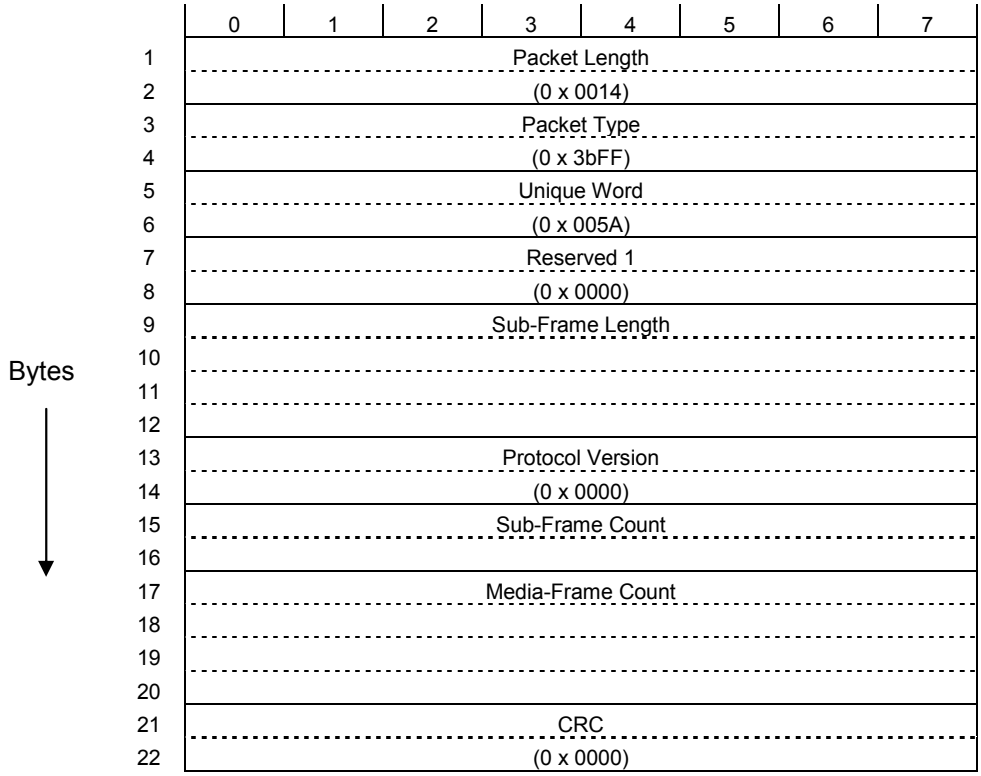
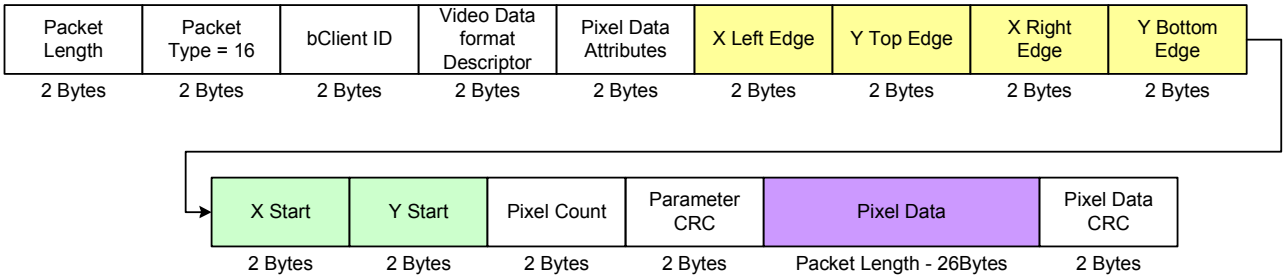


Figure 119: Sub-Frame Header Packet

Video Stream Packet

The ILI9806 writes image data to the RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.



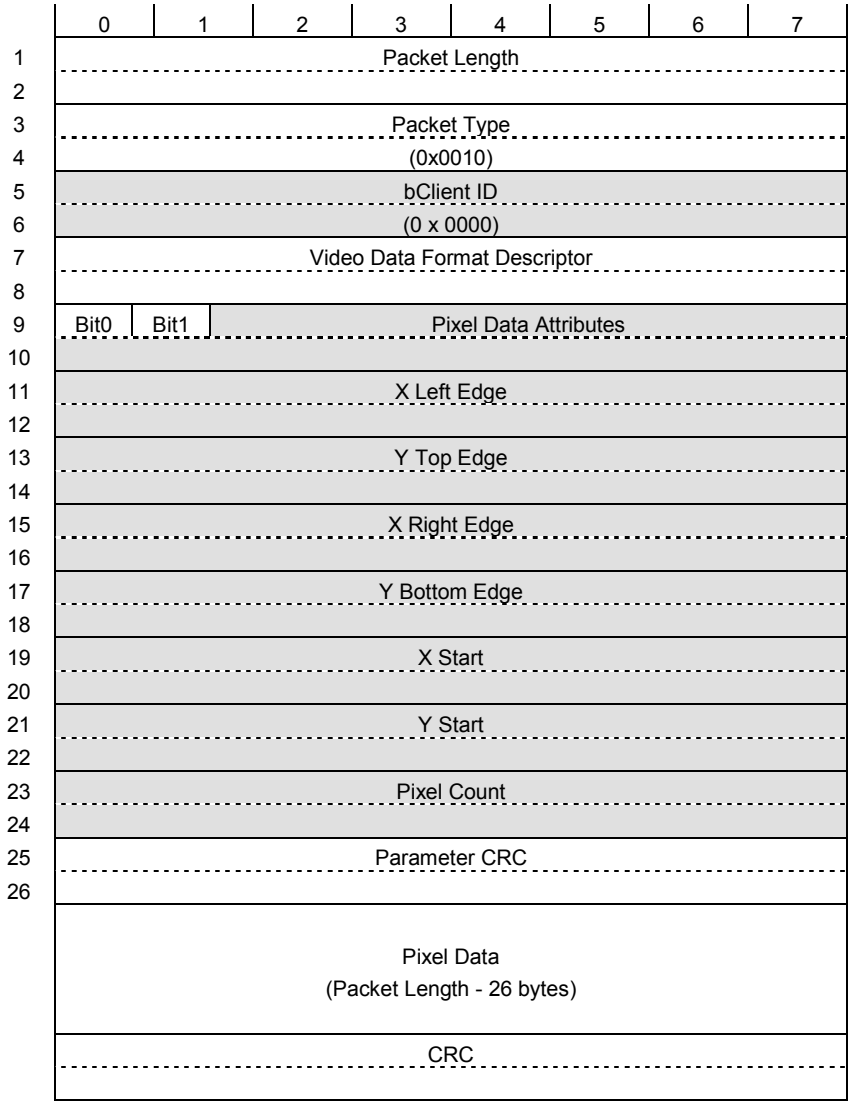


Figure 120: Example of Video Stream Packet Fields[Note]

Note *The parameters colored in gray are not supported by the ILI9806.*

Video Data Format Descriptor: This sets the pixel data format. The ILI9806 supports only the following format. Set the same pixel format (bpp) as selected by DSS [1:0] in Video Data Format Descriptor.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B = 5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B = 6:6:6)
010	1	0x8	0x8	0x8	Packed 24bpp RGB format (R:G:B = 8:8:8)
Others					Setting disabled

	MDDI Bytes n								MDDI Bytes (n+1)								MDDI Bytes (n+2)							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
16bpp	Pixel 1 Blue					Pixel 1 Green						Pixel 1 Red					Pixel 2 Blue					Pixel 2		
Packet	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
18bpp	Pixel 2 Blue						Pixel 2 Green						Pixel 2 Red				Pixel 2 Blue							
Packet	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
24bpp	Pixel 1 Blue								Pixel 1 Green								Pixel 1 Red							

Figure 121: Video Data Format

Pixel Data Attributes: The image data sent via Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Table 41: Pixel Data Attributes

Pixel Data Attributes	Bits [1:0]	Description
0 x 0000	00	The ILI9806 does not support the sub-panel display.
0 x 0001	01	Setting disabled
0 x 0002	10	Setting disabled
0 x 0003	11	The Video Stream Packet data is recognized as the data written in the ILI9806. The Video Stream Packet data is written in the ILI9806 and not outputted via a sub-display interface.
Others	-	-

Register Access Packet

The Register Access Packet is used when setting instructions to the ILI9806.

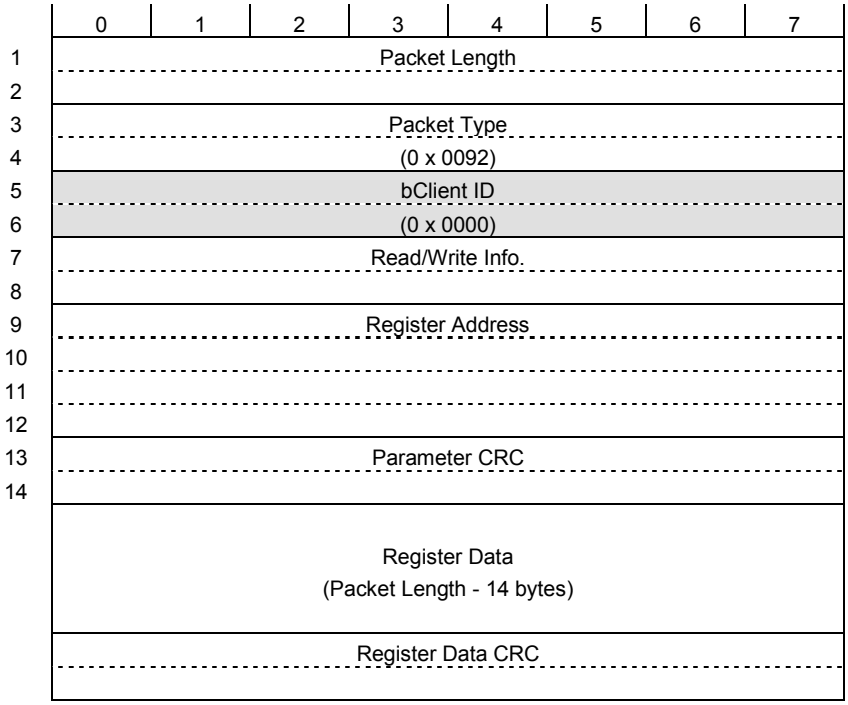


Figure 122: Register Access Packet[Note]

Read/Write Info: Read or Write information in register access. The following access setting is supported.

Bits [15:14]	Bits [13:00]	Description
2'b00	0 x n	Write one register by register access packet
2'b01	0 x n	Reserved
2'b10	0 x n	Read one register by register access packet
2'b11	0 x n	Response to read

Register Address: The index of the register to be accessed is set in the Register Address area, and the Register Address Packet is directed to the ILI9806, or the sub display as determined by the setting in the Register Address area.

Bits [31:16]	Description
16'h0000	The Register Access Packet is directed to the ILI9806 via the main-display interface.
16'h0001 ~ 16'h7FFF	Setting disabled

Bits [15:0]	Description
16'h0000~16'h FFFF	Bits [15:0] are used as index [15:0].

Register Data: The data for register access is written in the Register Data area. The length of the Register Data Packet depends on the parameter length of the command.

Note *The parameters colored in gray are not supported by the ILI9806.*

	0	1	2	3	4	5	6	7
1	Packet Length					(0 x 16)		
2						(0 x 00)		
3	Packet Type					(0 x 92)		
4						(0 x 00)		
5	bClient ID					(0 x 00)		
6						(0 x 00)		
7	Read/Write Info.					(0 x 01)		
8						(0 x 00)		
9	Register Address					(index ID [7:0])		
10						(index ID [15:8])		
11						(0 x 00) → Main Panel (ILI9806)		
12						(0 x 00)		
13	Parameter CRC							
14								
15	Register Data List (Various Length)					1st Parameter		
16						0 x 00		
17						0 x 00		
18						0 x 00		
19						2nd Parameter		
20						0 x 00		
21						0 x 00		
22						0 x 00		
23	Parameter CRC							
24								

Figure 123: Example of Register Access Packet (write to the ILI9806)[Note]

Register Access Packet Restrictions

The internal RAM of the ILI9806 is accessible via the Video Stream Packet. RAM access data is not included in the Register Access Packet.

Note *The parameters colored in gray are not supported by the ILI9806.*