Project Delta
An Interactive FPGA Circuit Simulator

Specification

Developers:
Robert Duncan – rad55@cam.ac.uk
Justus Matthiesen – jm614@cam.ac.uk
David Weston – djw83@cam.ac.uk
Christopher Wilson – cw397@cam.ac.uk
Rubin Xu – rx201@cam.ac.uk

Client:
Steven Gilham
steven.gilham@citrix.com

January 18, 2009

Contents

1 Project Description

It would be useful if a first year computer scientist could rapidly prototype a circuit on an Altera DE2 FPGA board without using a hardware description language. The user interface might be presented as a graphical circuit entry system allowing the user to select components from a library (including, 2- and 3-input NOR and NAND gates, RS-latch and D flip-flop) and place them on the screen. Additional components like RAMs and ROMs would be desirable. Switches and LEDs that are present on the DE2 board should be present in the graphical environment to allow circuits to be interfaced to them. Saving and loading of circuits is desirable. Circuits created should be simulated on the DE2 board. The transfer of the circuit to the FPGA simulation might happen in real-time (i.e. any change in the circuit is reflected "instantly" in the simulation). The simulation might be performed in software by a soft processor on the FPGA. For a high performance implementation, the graphical circuit might also be written out as Verilog and then synthesised for direct implementation on the FPGA.

2 Proposal

We propose to create a Java based GUI that allows the user, in this case a first year computer scientist, to design a simple circuit using a drag-and-drop interface. The application will allow the user to send their design to the Altera DE2 board for simulation using a Java-based processor. What follows is a description of the required features and our plan to implement them within the time restriction given.

3 Major Planned Features

(a) Tri-state wires: with `0`,`1`, and `X` which represents a disconnection.

(b) A component library containing:

- (i) NOR gate (2/3 input).
- (ii) NAND gate (2/3 input).
- (iii) AND gate (2/3 input).
- (iv) OR gate (2/3 input).
- (v) XOR gate (2/3 input).
- (vi) XNOR gate (2/3 input).
- (vii) RS latch.
- ($viii$) D flip flop.
- (ix) limited size RAM.

(x) limited size ROM.

(c) The ability to "connect" circuit to built-in LEDs, toggle switches, and push buttons on DE2 boards.

(d) The ability to group and ungroup components into a single composite component.

(e) Reasonably accurate simulation of circuit on DE2 board, not withstanding variable gate and wire delay (i.e. only have fixed gate delay equal across all components).

(f) Single clock with variable frequency.

(g) An intuitive GUI with:

  (i) Drag-and-drop component placing and wiring.
  (ii) Flexible wiring with the ability to split wires.
  (iii) Undo/redo.
  (iv) Zooming.
  (v) Document loading/saving.
  (vi) Component loading/saving.

(h) Capability to export to verilog to be implemented directly onto the FPGA.

(i) Fast transfer of designed circuit to DE2 board to be simulated.

4 Acceptance Criteria

Even though we will endeavour to complete all the major features listed in section 3, we may find it necessary to make variations during development of the project. The final project must satisfy the following criteria:

(a) Core GUI.

(b) Loading/saving of circuits.

(c) At least switch/button/LED connection along with NAND and NOR gates (2/3 input), RS latches and D flip flops.

(d) Simulation of circuit on DE2 board.

(e) Clock frequency control.

5 Distribution of Responsibility

The rôles defined here are temporary assignments.

Robert Duncan	Data Structure & Integration
Justus Matthiesen	Simulator
David Weston	GUI
Chrisopher Wilson	GUI
Rubin Xu	Hardware