

Lab2 Report  
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**Microbenchmark:**

Here is the microbenchmark used to verify the 2-level branch predictor:

```
int a = 0;
for(int i = 0; i < 1000000; i++){
    for(int j = 0; j < 7; j++){ // 8 branches with pattern: TTTTTTTN
        a++;
    }
    for(int j = 0; j < 3; j++){ // 4 branches with pattern: TTTN
        a++;
    }
}
```

The branch outcome pattern for one loop is T TTTTTTTN TTTN\*. The history table has 6 bits per entry. Considering all the 6-bit patterns, there is only one pattern (TTTTTT) that yields two possible outcomes. So, there should be 1 misprediction for each loop.

The number of mispredictions should be  $1 * 1000000 = \mathbf{1000000}$  since there are 1000000

iterations. The MPKI should be  $1/51 * 1000 = \mathbf{19.608}$  since there are 51 instructions per loop.

The reported results are NUM\_MISPREDICTION = **1001848**, MPKI = **19.601**, which are close to what we predict. To see the assembly code, refer to mb.c and **-O0 compilation flag** is used.

**Branch predictor performance:**

Benchmark	2-bit saturating		2-level		open-ended	
	Mispredictions	MPKI	Mispredictions	MPKI	Mispredictions	MPKI
astar	3695830	24.639	1785464	11.903	798843	5.326
bwaves	1182969	7.886	1071909	7.146	832175	5.548
bzip2	1224967	8.166	1297677	8.651	1120811	7.472
gcc	3161868	21.079	2223671	14.824	1118817	7.459
gromacs	1363248	9.088	1122586	7.484	769478	5.130
hmmer	2035080	13.567	2230774	14.872	1775925	11.839
mcf	3657986	24.387	2024172	13.494	1552188	10.348
soplex	1065988	7.107	1022869	6.819	808722	5.391

**open-ended branch predictor implementation:**

The open-ended branch predictor is a hybrid predictor consisting of a GAP and a PAp. We use a chooser to select between the two.

The PAp has a private prediction table with 512 entries. Each entry has 11 bits, and they are used to index into the row of the branch prediction table. There are 8 branch prediction tables selected by the last 3 bits of PC. Each row of the branch prediction table is a 4-bit counter indicating the prediction result.

The GAP has a global predictor table and 8 private branch prediction tables selected by the last 3 bits of PC. The global predictor table is used to select the row of the private branch prediction table. Each entry of the private branch prediction table is a 4-bit counter.

The selector is a 4-bit counter. It is used to select between the GAP and the PAp.

**Size:**

GAp:  $9 + 8 \times 512 \times 4 = 16393$

PAP:  $512 \times 11 + 8 \times 2048 \times 4 = 71168$

Selector:  $512 \times 4 = 2048$

Total: 89609bits = 87.5Kbits

**Area, access latency, and leakage power:**

Assume: For RAMs, block size is rounded up to byte and the total size is calculated based on the rounded-up block size

Note: the access latency is calculated based on whether the access is parallel or sequential

**Two-level:**

	Configuration	Area (mm <sup>2</sup> )	Access latency (ns)	Leakage power (mW)
BHT 2level-bpred-1.cfg	Type: RAM Size: 512 bytes Block size: 1 byte	0.0391054 x 0.0269215	0.163585	0.195006
PHT 2level-bpred-2.cfg	Type: RAM Size: 128 bytes Block size: 2 bytes	0.022907 x 0.0145202	0.143854	0.0535953
Total	Sequential access	1.38539 x 10 <sup>-3</sup>	0.307439	0.2486013

**Open-ended:**

Note: the global history register is ignored since it is insignificant compared to other data and the access latency is calculated based on whether the access is parallel or sequential storage.

	Configuration	Area (mm <sup>2</sup> )	Access latency (ns)	Leakage power (mW)
GAp (PHT) open-ended-bpred-1. cfg	Type: RAM Size: 2048 bytes Block size: 4 bytes	0.0700302 x 0.0515418	0.206091	0.833957
PAP (BHT) open-ended-bpred-2. cfg	Type: Cache Size: 704 bytes Tag size: 11bits	0.00188529	0.179111	0.375048
PAP (PHT) open-ended-bpred-3. cfg	Type: RAM Size: 8192 bytes Block size: 4 bytes	0.133416 x 0.0953244	0.279886	2.87418
Selector Open-ended-bpred-4 .cfg	Type: Cache Size: 256 bytes Tag size: 4	0.000325773	0.146414	0.057681
Total	Parallel access	0.01853834571	0.458997	4.140866

**Work Distribution:**

Tianyi Xu: implemented part 1, part2, part3 parameter tuning, wrote report, CACTI configuration

Wang Hao: implemented part 3