Research on Electrical Characteristics of 1200V SiC Trench MOSFET with Periodic Arrangement of 3D P-shield Structure

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Abstract

In this study, we developed a 1200V SiC trench gate MOSFET device by utilizing ion implantation to create periodic P-type shielding structure in the trench, this approach significantly reduces the electric field stress on the trench gate oxide layer, with a peak electric field below 2MV/cm under a blocking voltage of 1200V. Additionally, we examined the effects of the H_2 annealing process on trench sidewall roughness and the restoration of lattice damage at SiC/SiO_2 interfaces through high-temperature annealing. By optimizing the process, we attained a sidewall roughness of 0.11nm and a channel field-effect mobility of 51.6$cm^2/V{\cdot}s$, thereby enhancing the device's dynamic-static and robustness trade-off. Ultimately, utilizing L5 series packaging, we assessed the chip's performance, achieving a R_{DSON} of less than 10mΩ and an E_{SC} over 13J.

1 Introduction

Compared to planar MOSFETs, trench MOSFETs can reduce cell-pitch and enhance current density, earning them increasing favor[1]. However, in SiC trench MOSFETs, the wide band-gap significantly increases the electric field stress in the gate oxide layer. Therefore, these devices require P-type doping, also known as a shielding structure, to terminate electric field lines and ensure long-term reliability. Moreover, the shielding structure significantly affects the chip's dynamic-static performance and robustness, making trench shielding technology been the core of trench SiC MOSFET technology[2-3].

Currently, SiC trench MOSFETs in the industry primarily feature the "Semi-Enclosed" and "Double-Trench" structures, as depicted in Figures 1 and 2[4-6]. The "Semi-Enclosed" structure allows conduction through only one side of the channel, thereby sacrificing partial current capacity; the "Double-Trench" structure forms deeper source trenches on either side of the gate trench, followed by ion implantation to create a shielding structure, this results in reduced contact areas for source P+ and N+ regions, elevates process capability requirements, and hinders further cell-pitch reduction.

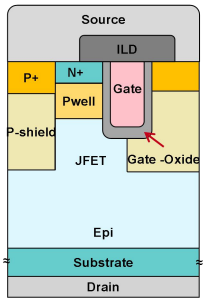

Fig.1 “Semi-Enclosed” structure

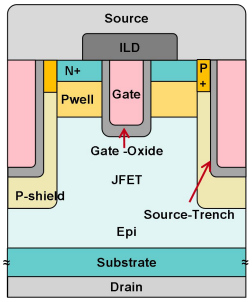

Fig.2 "Double-Trench" structure

Based on this, this paper developed a 1200V trench MOSFET featuring a periodic P-type shielding structure in three dimensions(3D P-shield). By utilizing the three-dimensional expansion, the cell-pitch is further reduced, and optimizations have been made to the trench morphology, roughness, and channel mobility. The current capacity is significantly enhanced, and exhibits outstanding robustness.

2 Structure Design

The top and cross-sectional views of the 3D P-shield SiC Trench MOSFET are shown in Figures 3 and 4. A periodic P-shield structure is created along the three-dimensional (CC') direction through ion implantation within the trench. When the device is turned on, channels form on both sides of the trench in region AA', with the N+ area supplying electrons for conduction. In the reverse bias state, the P-shield structure depletes within the epitaxial layer, reducing electric field stress concentration at the trench bottom's gate oxide layer, achieving an electric field of less than 2MV/cm at 1200V to ensure long-term reliability. It should be noted that the ion implantation window and angle for the P-shield structure significantly impact its effectiveness, necessitating continuous design optimization.

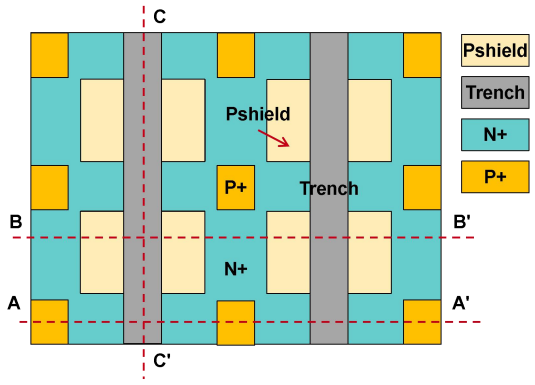

Fig.3 Vertical view of 3D P-shield SiC trench MOSFET

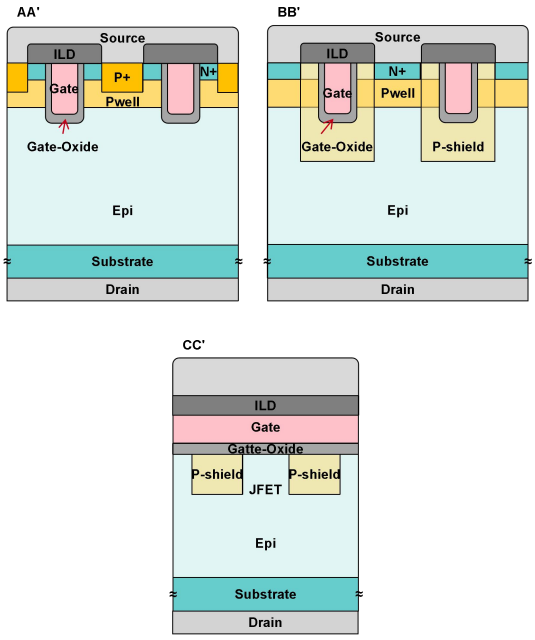

Fig.6 Cross section of the direction AA', BB' and CC'

In contrast to traditional SiC trench MOSFETs, the 3D P-shield SiC trench MOSFET features its parasitic JFET region along the CC' direction, enhancing flexibility in N+ and P+ dimensions and layout designs, facilitating a better trade-off performance of the device's dynamic-static performance and robustness.

3 Critical process

Besides reducing cell-pitch, SiC trench MOSFETs benefit from having their channels located on vertical crystal planes like the a-face and m-face, which offer higher channel mobility than the horizontal Si-face, enabling a relatively lower channel resistance. However, the etching and post-processing techniques

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for silicon carbide trenches significantly impact the device's electrical performance.

Figures 5 and 6 depict the trench morphology under various process conditions, the experiments revealed that with an increase in H_2 annealing temperature, the trench curvature enlarges. Moreover, as the H_2 flow rate rises, the roughness of the trench sidewalls initially increases and then decreases. By continuously optimizing, a roughness of 0.11 nm on the trench sidewalls was achieved, mitigating the scattering effects of surface roughness.

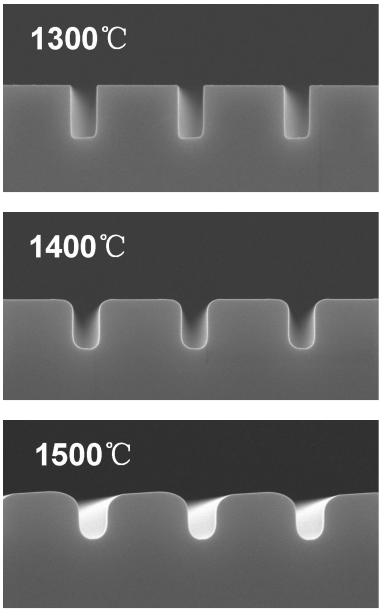
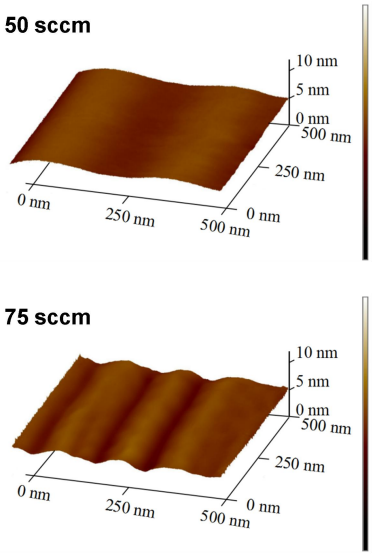


Fig.5 Trench appearance after different H_2 annealing temperatures (1300℃,1400℃, 1500℃)



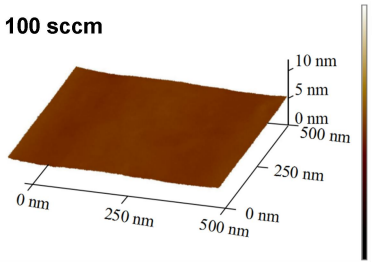


Fig.6 Trench side-wall roughness under different H_2 flow rate (50 sccm, 75 sccm, 100 sccm)

Additionally, lattice defects generated during the trench etching process can reduce channel mobility, high-temperature annealing processes have effectively repaired lattice damage, as illustrated in Figure 7. These two approaches have led to a channel mobility of 51.6 $cm^2/V{\cdot}s$, as shown in Figure 8, which substantially reduces the device's channel resistance.

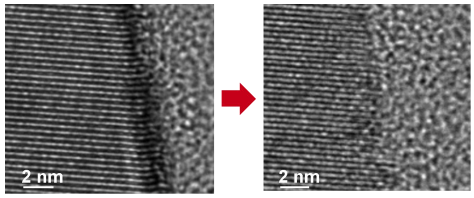


Fig.7 Effect of lattice repair after high-temperature annealing

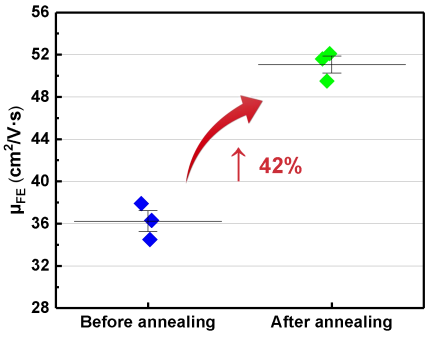


Fig.8 Field-effect mobility before and after process optimization

4 Electrical Characteristics

The 3D P-sheild SiC trench MOSFET chip was packaged using the L5 series format (8 chips in parallel), and its electrical characteristics, including dynamic-static performance and robustness, were evaluated.

Figure 9 and Figure 10 present the transfer and output

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characteristic curves, respectively. The temperature coefficient of the trench gate's resistance is higher than that of the traditional planar gate MOSFET, attributed to the reduced proportion of channel resistance in the trench gate devices, channel resistance exhibits a negative correlation with temperature, while the remaining resistances show a positive correlation. Additionally, the superior shielding effect results in a leakage current of only 0.3μA at 1200V.

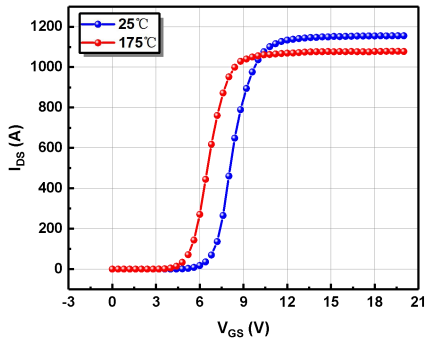

Fig.9 Transfer characteristic

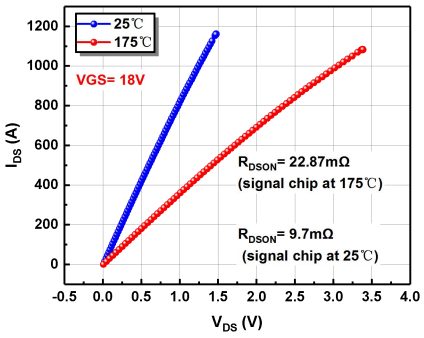

Fig.10 Output characteristic

Figure 11 is the capacitance characteristic curve, which deeply influences the device's switching process, thus, the design process involved detailed optimization of key parameters such as the junction depth of N-type dopping, shielding structure dimensions and JFET width, achieving a reverse tansfer capacitance (Crss) of 8.7pF and a gate-source input capacitance (Ciss)/Crss ratio exceeding 700, this enables faster switching speeds and reduced switching losses with smaller gate resistors.

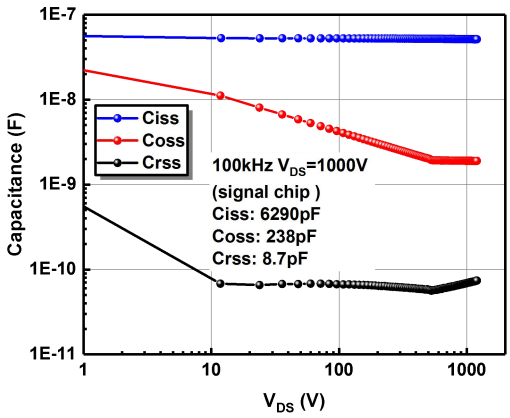

Fig.11 Capacitance characteristic

Figure 12, Figure 13, and Figure 14 illustrate the turn-off, turn-on, and reverse recovery waveforms, with the turn-on, turn-off, and reverse recovery losses being 60.75mJ, 44.93mJ, and 6.42mJ, respectively. The crosstalk voltage during turn-off remains between -5.25V to -2.32V, yet the Vrm during turn-on is higher due to the rapid carrier extraction in the body region during the reverse recovery process, leading to a large dirr/dt and severe voltage overshoot, which constrains further increases in turn-on speed.

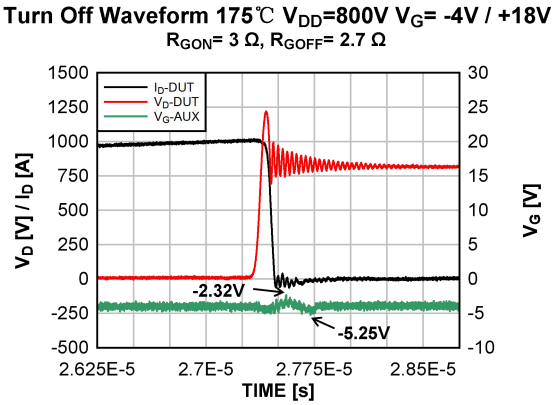

Fig.12 Turn-off waveform

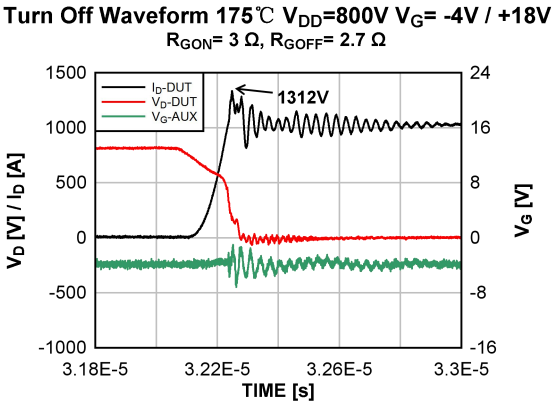

Fig.13 Turn-on waveform

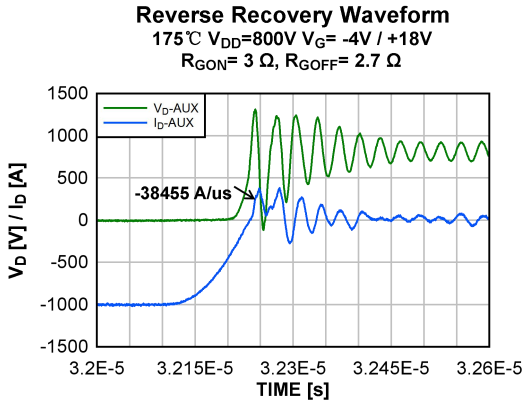

Fig.14 Reverse recovery waveform

Figure 15 displays the short-circuit capability. The enhanced channel mobility enables the design of longer channel lengths in trench gate devices, leading to reduced saturation currents. Additionally, the 3D P-shield structure introduced in this study further reduces the device's saturation current, thanks to its high doping concentration and junction depth, achieving a short-circuit withstand of 3μs and a short-circuit energy (ESC) of 13J

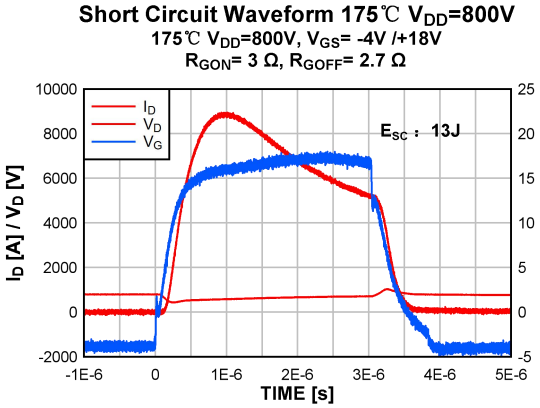

Fig.15 Short-circuit capability

5 Conclusion

The 3D P-shield structure allows SiC trench MOSFET to overcome the cell-pitch constraints in two dimensions, when combined with process optimization, this enhances the device's trade-off between dynamic-static performance and robustness, thus broadening its potential applications.

6 References

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