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Dynamic Current Balancing Optimization of Cu Clip-Bonded SiC power module Based on Layout-Dominated Parasitic Inductance

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Abstract

Cu clip-bonding has lower resistance and lower inductance than wire-bonding, but unbalanced dynamic current still exists between paralleled silicon carbide (SiC) MOSFETs, limiting the available current capacity of Cu clip-bonded SiC power modules. This paper presents a parasitic inductance equivalent circuit model at switching transients, and a dynamic current balancing optimization guideline based on self- and mutual inductance of main current path segments is determined. The mismatch of the equivalent power source parasitic inductances is reduced by adjusting the bonding positions and shape parameters of Cu clips. Simulation results show that the dynamic current sharing performance is greatly improved.

1 Introduction

For high-capacity power electronic converter applications, such as electric vehicles, electric aircraft, and photovoltaic inverters, SiC MOSFETs are the most promising alternative to Si IGBTs due to their high blocking voltage, low ON-resistance, high switching frequency, and high operating temperature [1]. However, existing power module packaging technologies limit the full utilization of the performance of SiC MOSFETs, especially Al wire-bonding. In contrast, Cu clip-bonding has lower parasitic resistance and inductance due to the high electrical conductivity of copper and large cross-sectional area of Cu clips, which contributes to lower switching loss and voltage overshoot, and provides an extra heat dissipation path due to the high thermal conductivity and large soldering area of Cu clips, which contributes to the power module's heat dissipation capability [2].

Since the rated current of a single SiC chip is limited, parallel operation of SiC MOSFETs is the simplest and most practical way to increase the current capacity of power modules. However, if the bonding wires are simply replaced with Cu clips, the unbalanced current between paralleled SiC MOSFETs will still affect the stable operation of the power module. Static current of paralleled SiC MOSFETs can be self-balanced due to the positive temperature coefficient of ON-resistance, but dynamic current isn't self-balanced and requires additional balancing measures. In [3], it is noted that unbalanced dynamic current is closely related to the mismatch of the power source inductances, chip characteristic parameters and temperature. Some researchers proposed circular or elliptical symmetric DBC layout to suppress the mismatch of power source inductances, but due to the inflexible shape and position of terminals, it is difficult to generalize them for application [4], [5]. In [6], the bonding wire position is optimized to adjust the power source inductances, but the effect of mutual inductance is neglected and the parasitic inductance introduced by long bonding wire is relatively large. There are also some researches focusing on active gate drivers to suppress the unbalanced dynamic current by adjusting the gate driver voltage amplitude and delay [7], [8]. However, the current sensing and signal processing in a very short period of time make the driver circuit too complicated.

To address the above issues, a layout-dominated parasitic inductance equivalent circuit model at switching transients considering mutual inductance is established, and an optimization guideline for the equivalent power source parasitic inductances to achieve dynamic current balancing is derived. On this basis, the bonding positions and shape parameters of the paralleled dies' Cu clips are adjusted to reduce the mismatch of the equivalent power source parasitic inductances because the Cu clips' parasitic inductance is easy to adjust. And Kelvin-source connection is used to decouple the power network and drive network, eliminating the influence of common source inductance [9]. The rest of this paper is organized as follows. Section II introduces the baseline Cu clip-bonded SiC

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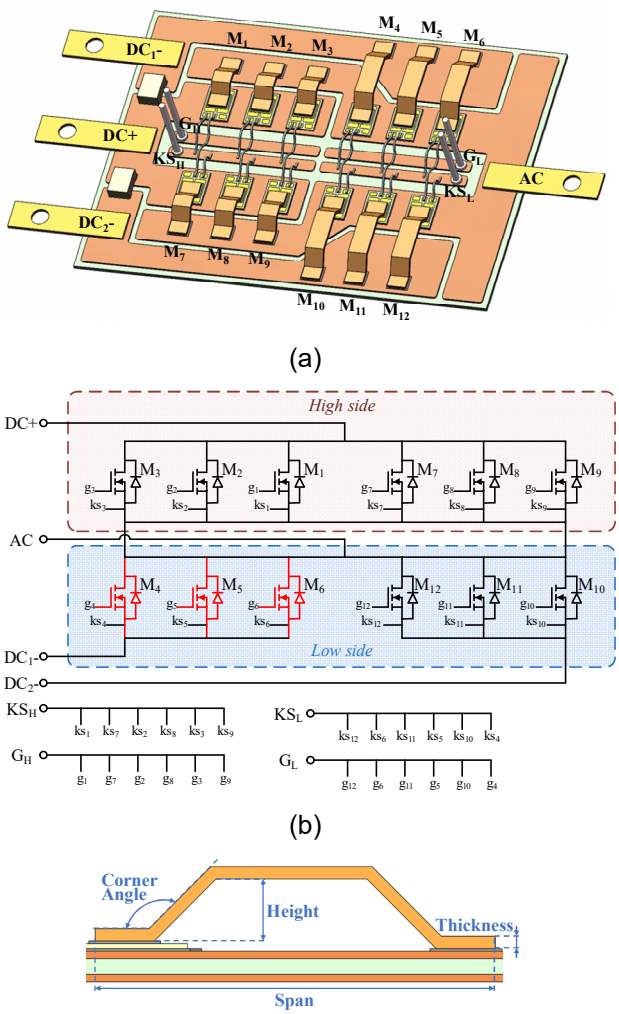


Fig. 1. Schematic of the baseline Cu clip-bonded SiC power module. (a) DBC Layout. (b) DBC topology. (c) Structural parameters of Cu clip.

power module and derives the optimization guideline. In Section III, the DBC layout is optimized by shaping the Cu clips and the simulation verification results of dynamic current balancing optimization is presented. Finally, the conclusion is given in Section IV.

2 Layout-Dominated Parasitic Inductance Equivalent Circuit Model

2.1 Baseline Cu Clip-Bonded SiC Power Module: DBC Layout and topology

The schematic of the baseline Cu clip-bonded SiC power module is shown in Fig.1, whose DBC layout is commonly used in commercial wire-bonded power modules. As shown in Fig.1(b), each side switch consists of six paralleled SiC MOSFET dies with Kelvin-source connection, and dies M_1-M_6 are symmetrically located with dies M_7-M_{12}. Due to the symmetry of the

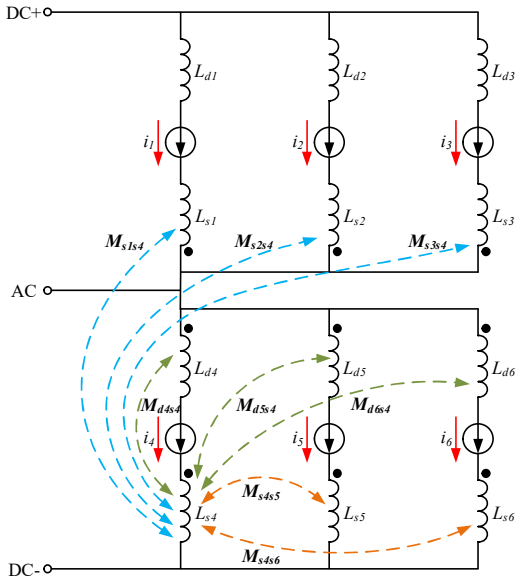


Fig. 2. Parasitic inductance equivalent circuit model at switching transients.

overall layout, this article only discusses the unbalanced dynamic current among low side dies M_4-M_6, and thus evaluates the overall current sharing performance of the multichip power module. As shown in Fig.1(c), the main structural parameters of Cu clip include span, height, thickness, and corner angle, which affect the numerical value of parasitic inductance of Cu clip.

2.2 Optimization Guideline

Considering the effect of magnetic coupling between different current path segments, the parasitic inductance equivalent circuit model of M_4 at switching transients is shown in Fig. 2, where L_x and M_x refer to the parasitic self-inductance of each current path segment and parasitic mutual inductance between each two current path segments. According to the DBC layout of the baseline Cu clip-bonded SiC power module, the mutual inductance of the M_4 power source path segment can be divided into three main types based on the criterion of tight magnetic coupling, which are the mutual inductance between the M_4 power source path segment and the M_1-M_3 power source path segments M_{sis4} (i= 1, 2, 3), the mutual inductance between the M_4 power source path segment and the M_4-M_6 drain path segments M_{dis4} (i= 4, 5, 6), the mutual inductance between the M_4 power source path segment and the M_5-M_6 power source path segments M_{s4si} (i= 5, 6), respectively. The parasitic inductance equivalent circuit models of M_5 and M_6 at switching transients are similar and will not be repeated here.

The parasitic inductance of dies M_4-M_6 can be represented with inductance matrices $\boldsymbol{L_1}$ and $\boldsymbol{L_2}$:

$$\boldsymbol{L_1} = \begin{bmatrix} M_{s1s4} & M_{s2s4} & M_{s3s4} \\ M_{s1s5} & M_{s2s5} & M_{s3s5} \\ M_{s1s6} & M_{s2s6} & M_{s3s6} \end{bmatrix} \quad (1)$$

$$\boldsymbol{L_2} = \begin{bmatrix} L_{s4}+M_{d4s4} & M_{d5s4}+M_{s4s5} & M_{d6s4}+M_{s4s6} \\ M_{d4s5}+M_{s4s5} & L_{s5}+M_{d5s5} & M_{d6s5}+M_{s5s6} \\ M_{d4s6}+M_{s4s6} & M_{d5s6}+M_{s5s6} & L_{s6}+M_{d6s6} \end{bmatrix} \quad (2)$$

Where $\boldsymbol{L_1}$ consists of mutual inductance M_{sisn} (n= 4, 5, 6), $\boldsymbol{L_2}$ consists of self-inductance L_{sn} (n= 4, 5, 6) and the other two types of mutual inductance (M_{disn} and M_{snsi}, n= 4, 5, 6).

According to the parasitic inductance equivalent circuit models, the induced voltage drops on M_4-M_6 power source path segments can be written as

$$\boldsymbol{v_{Ls}} = \begin{bmatrix} -\boldsymbol{L_1} & \boldsymbol{L_2} \end{bmatrix} \frac{d\boldsymbol{i}}{dt} \quad (3)$$

where $\boldsymbol{v_{Ls}} = \begin{bmatrix} v_{Ls4} & v_{Ls5} & v_{Ls6} \end{bmatrix}^T$, $\boldsymbol{i} = \begin{bmatrix} i_1 & i_2 & i_3 & i_4 & i_5 & i_6 \end{bmatrix}^T$.

The induced voltage difference between M_4-M_6 power source path segments at switching transients because of the different parasitic self- and mutual inductance will cause circulations in the power and driver loops, resulting in an unbalanced dynamic current [10]. Therefore, balanced dynamic current among paralleled dies M_4-M_6 means that

$$v_{Ls4} = v_{Ls5} = v_{Ls6} = v_{Ls}' \quad (4)$$

$$\frac{di_1}{dt} = \frac{di_2}{dt} = \frac{di_3}{dt} = \frac{di_4}{dt} = \frac{di_5}{dt} = \frac{di_6}{dt} = \frac{di'}{dt} \quad (5)$$

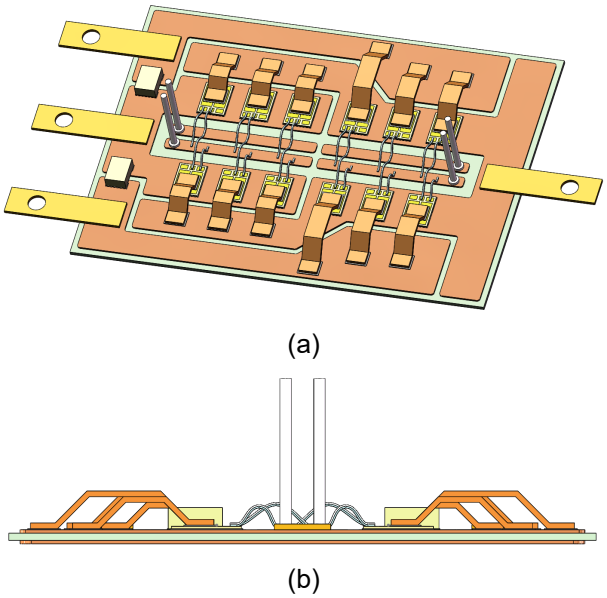
Take (4) and (5) into (3), it can be derived that

$$\begin{bmatrix} v_{Ls}' \\ v_{Ls}' \\ v_{Ls}' \end{bmatrix} = -\begin{bmatrix} M_{s1s4}+M_{s2s4}+M_{s3s4} \\ M_{s1s5}+M_{s2s5}+M_{s3s5} \\ M_{s1s6}+M_{s2s6}+M_{s3s6} \end{bmatrix} \frac{di'}{dt} + \begin{bmatrix} L_{s4}+M_{d4s4}+M_{d5s4}+M_{s4s5}+M_{d6s4}+M_{s4s6} \\ M_{d4s5}+M_{s4s5}+L_{s5}+M_{d5s5}+M_{d6s5}+M_{s5s6} \\ M_{d4s6}+M_{s4s6}+M_{d5s6}+M_{s5s6}+L_{s6}+M_{d6s6} \end{bmatrix} \frac{di'}{dt} = \boldsymbol{L_e} \frac{di'}{dt} \quad (6)$$

Where $\boldsymbol{L_e} = \begin{bmatrix} L_{e4} & L_{e5} & L_{e6} \end{bmatrix}^T$, representing the equivalent power source parasitic inductances of dies M_4-M_6. In order to satisfy (6), the equivalent power source inductances should be equal, which is also the optimization guideline for the baseline clip-bonded SiC power module to achieve balanced dynamic current. Since the parasitic inductances come from Cu clips and copper traces, the difference between the equivalent power source parasitic inductances can be reduced by adjusting the bonding position and the shape parameters of Cu clips.

TABLE I
VALUE OF EQUIVALENT POWER SOURCE PARASITIC INDUCTANCES

	Initial	Optimized
L_{e4}/nH	22.55	22.82
L_{e5}/nH	24.64	23.42
L_{e6}/nH	25.22	23.86



(a)

(b)

Fig. 3. The DBC layout of the optimized Cu clip-bonded SiC power module. (a) Overall view. (b) Side view.

3 DBC Layout Optimization of Cu Clip-Bonded SiC Power Module and Simulation Verification

3.1 DBC Layout Optimization

Before optimizing the Cu clip-bonded SiC Power Module, the self- and mutual inductance of the initial baseline power module are firstly extracted by ANSYS Q3D, and the equivalent power source parasitic inductances calculated based on the extraction results are given in Table I. According to the relative magnitude of the initial equivalent power source parasitic inductances, the spans, heights, thicknesses and corner angles of the Cu clips of dies M_4-M_6 are rationally adjusted to increase L_{e4} and decrease L_{e5} and L_{e6} as shown in Fig.3, and the optimized results are also given in Table I. The main structural parameters of Cu clips of dies M_4-M_6 are given in Table II. According to the results in Table I, the equivalent power source parasitic inductance imbalance degree before and after optimization is 11.06% and 4.45%, respectively, and the maximum equivalent power source parasitic inductance is reduced by 1.36 nH.

TABLE II
THE MAIN STRUCTURAL PARAMETERS OF CU CLIPS

Die	Span	Height	Thickness	Corner angle
M_4	16mm	2.5mm	0.5mm	135°
M_5	13mm	2mm	0.5mm	135°
M_6	12.5mm	2mm	0.5mm	135°

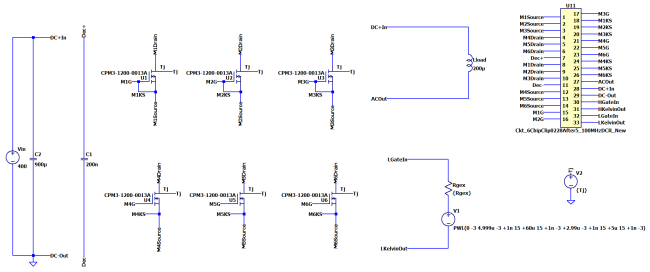


Fig. 4. The double pulse test circuit built in LTspice.

3.2 Simulation Verification

Firstly, the parasitic parameter multiport network models of the power module before and after optimization are derived from ANSYS Q3D simulation respectively, which includes parasitic inductances and ESRs, and then double pulse test circuits are built in LTspice to verify the optimization effect, in which M_4-M_6 are used as the active switches. As shown in Fig. 4, the double pulse test circuit built in LTspice includes the DC voltage source (400 V), bus capacitance (900 μF), decoupling capacitance (200 nF), load inductor (200 μH), gate resistance (10 Ω), gate drive voltage source (+15 V/ -3 V). The simulation waveforms of M_4-M_6 drain current at switching transients are shown in Fig. 5. In Fig. 5(b), the maximum initial turn-on peak current difference is 10.30 A with an imbalance degree of 18.77%. After optimization, the maximum turn-on peak current difference is 1.54 A and the imbalance degree is as low as 2.81%. Similarly, the current difference at turn-off also decreases after optimization. Therefore, it can be demonstrated that the current sharing performance of paralleled SiC dies in the optimized Cu clip-bonded SiC power module is greatly improved.

4 Conclusion

This article presents an optimization method for dynamic current balancing of paralleled dies in Cu clip-bonded SiC power module. Particularly, based on the self- and mutual inductance of several main current path segments dominated by layout, a parasitic inductance equivalent circuit model at switching transients is established, and a dynamic current balancing

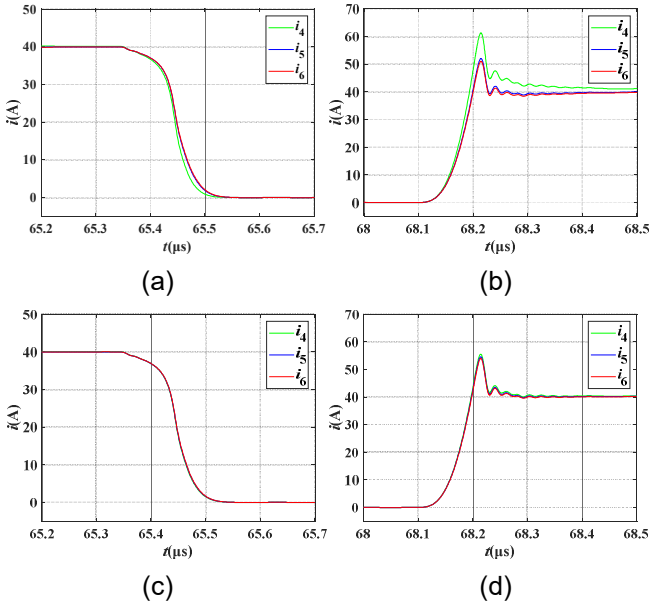


Fig. 5. Simulation waveforms of M_4-M_6 drain current at switching transients. (a) Initial turn-off. (b) Initial turn-on. (c) Optimized turn-off. (b) Optimized turn-on.

guideline is determined. The equivalent power source parasitic inductances are optimized by adjusting the bonding positions and shape parameters of Cu clips. The simulation results demonstrate that the optimized power module has a balanced switching current with an imbalance degree of 2.81% at turn-on (18.77% before optimization), which verifies the effectiveness of the proposed model and optimization method. Future work will mainly focus on improving the reliability of Cu clip-bonding in SiC power module.

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