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Compensation of Inconsistencies in Junction Temperature Deviation during Power Cycling Tests

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Abstract

In Power Cycling Tests (PCT), same device under identical testing conditions may exhibit different junction temperature deviation ΔT_{vj} which would affect the assessment of the device. This article analyzed the inconsistency in ΔT_{vj} among devices in serial power cycling topology. Subsequently, a compensation method based on adjusting the gate voltage through iterative fitting is proposed to address this imbalance. Then this paper analyzed the method's impact on junction temperature (T_{vj}) measurements and proved its robustness through experimentation. Finally, compensation on the junction temperature deviation was conducted on different power modules in PCT to validate the feasibility of the method.

1 Introduction

With the rapid development of the power electronics technology, semiconductor devices serving as pivotal components are encountering significant reliability challenges across various harsh application scenarios [1]. The failure of power semiconductor devices can lead to substantial losses and even casualties. With the raising demands of the reliability of the power devices in various application, the assessment of the power device's lifespan is increasingly paramount [2].

Power cycling test as the most important test of evaluating the device's lifespan and degradation mechanism can simulate the junction temperature deviation (ΔT_{vj}) of the device by controlling the amplitude of load current and the time applied to the device [3]. Though accelerated aging test, power cycling test applies thermal stress to the power device for verifying the reliability of the device package [4]. Fig. 1 illustrates the schematic diagram of junction temperature change of the power device. During the heating time t_{on}, load current will be applied to the Device Under Test (DUT). During the cooling time t_{off}, the device will be cooled through the cooling system. The summation of t_{on} and t_{off} constitutes a cycle, which will repeated until the DUT fails.

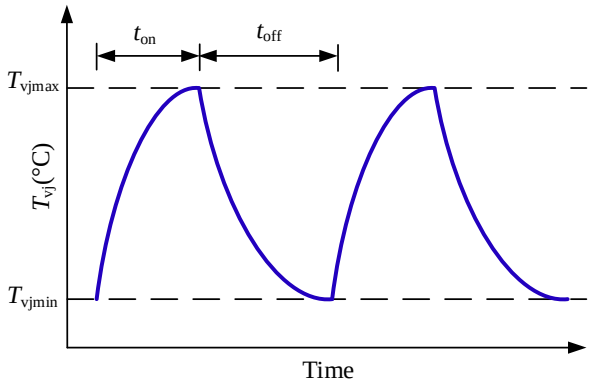

Fig. 1. The junction temperature fluctuation in the PCT

However, under the same testing condition, power device may exhibit varying ΔT_{vj}. Fig. 2 illustrates the temperature rise of each device in the serial power cycling testing of six devices within two three-phase IGBT power modules at the 45th cycle. The designed ΔT_{vj} for thermal stress of the devices is set at 100K, with all other testing conditions being identical. It is observed that the ΔT_{vj} of Device 1 is significantly lower than that of the other devices within the same test condition.

This inconsistency in ΔT_{vj} poses challenges in setting the parameters before power cycling tests. Furthermore, in cases like that depicted in Fig. 2, where such disparities are substantial, significant errors in estimating the lifespan of the tested components may occur.

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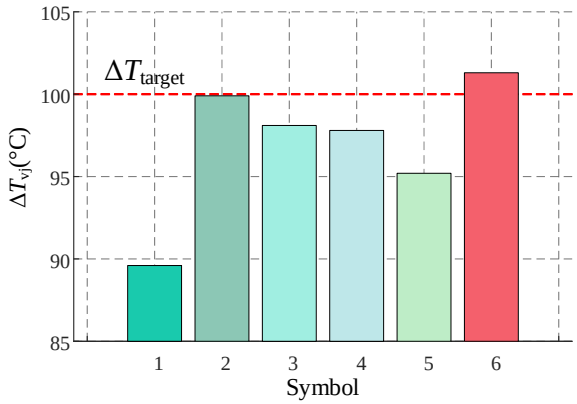


Fig. 2. The ΔT_{vj} of devices under same test condition

Chen analyzed the physical significance and averaging mechanism of chip junction temperature, indicating that the virtual junction temperature is a value associated with the measurement current [5]. Serval authors has compared the relationship between various temperature measurement methods and the temperature of IGBT chips, indicating a small difference between the average device temperature and the virtual junction temperature [6]. However, existing studies mainly focuses on junction temperature measurement, power cycling test topologies and control methods.

This study mainly focuses on the issue of inconsistency in ΔT_{vj} during the power cycling tests. A method has been proposed to compensate this problem and its robustness is analyzed and verified regarding its impact on junction temperature measurement. Finally, the compensation effect was validated through experiments involving multiple power modules of different companies and topologies.

2 Methodology

2.1 Analysis of Inconsistencies in Junction Temperature Deviation

In the power cycling test, the main factors that influencing the lifespan of a device are the maximum junction temperature and the fluctuation of junction temperature [7]. Fig. 3 shows the maximum and minimum junction temperature observed within the initial 45 cycles of the power cycling test.

The ΔT_{vj} of the power device is mainly determined by the amplitude of the load current and the turn-on time of the load current while the minimum and maximum junction temperatures of the device are determined by the cooling water temperature and flow rate of the cooling system during the power cycling test [8].

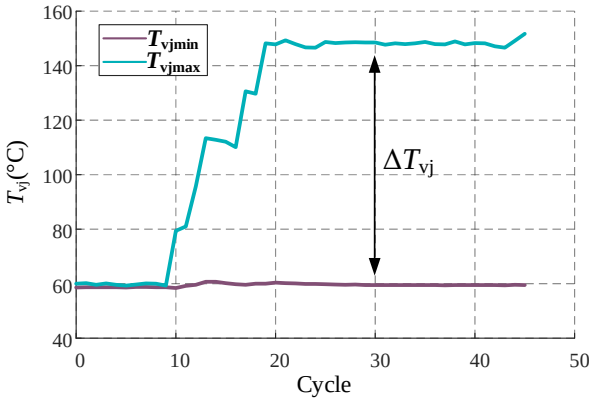
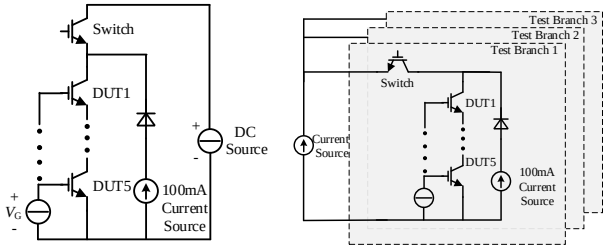


Fig. 3. Maximum and minimum junction temperature in the PCT

As a means of assessing the longevity of devices, PCT often necessitates a prolonged testing duration. To enhance testing efficiency, a common approach involves serially connecting DUTs into the testing circuit. Illustrated in Fig. 4 (a), several DUTs are serially connected to a DC power source via a control switch, enabling the injection of current into the DUT circuitry by alternately controlling the switch. Furthermore, in the pursuit of further augmenting testing efficiency while mitigating potential damage to testing equipment arising from frequent alternation of current output by the DC power source, a hybrid serial-parallel testing methodology is proposed. As depicted in Fig. 4 (b), several serially connected testing branches are paralleled at the current source, with several control switches facilitating the connection between the current source and testing branches. Consequently, prevalent power cycling testing equipment predominantly adopts such hybrid serial-parallel testing circuits.



(a) Series type (b) Serial-parallel type

Fig. 4. The circuit diagram of PCT

Therefore, in such topologies, adjustments can only be made to the total current. Hence, it is not possible to independently adjust the load current to change the ΔT_{vj} of a single device. Additionally, since each DUT shares the same cooling equipment, the temperature and flow rate of the cooling liquid are also nearly identical for all devices.

The difference in ΔT_{vj} of power devices mainly stems from variances in module thermal resistance and on-state voltage. Research indicates that the cell layout of power modules is one of the factors affecting device on-state voltage drop [9]. Additionally, the thickness, area,

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and thermal conductivity of different layers within the chip and module can also affect the device's on-state characteristics and thermal resistance. In the soldering process of power devices, the thickness of the solder layer and the void ratio are also important factors affecting the overall thermal resistance of the device [10].

This study conducted power cycling tests on power modules with different topologies from various companies. Tab. 1 presents the testing parameters which utilized in power cycling tests.

Tab. 1. Power cycling test condition

Parameter		Value
On-time of the load current	t_{on}	20s
Off-time of the load current	t_{off}	40s
Value of load current	I_L	300A
Gate voltage	V_G	15V
Coolant temperature	T_{cool}	60°C
Coolant flow rate	Q_{cool}	8L/min

Tab. 2 presents the variances and ranges of data from different test groups, serving to characterize the degree of dispersion in ΔT_{vj}. The first group of data corresponds to the situation depicted in the above Fig. 2. In the same testing equipment, different groups of power modules sharing the same testing parameter exhibit varying degrees of dispersion in their ΔT_{vj}. Therefore, the design and manufacturing processes of the chips are among the factors contributing to this situation.

Tab. 2. Variance and range of data from different test groups

Group	Topology	Variance(K)	Range(K)
1	Six-Pack	14.6	11.3
2	Six-Pack	9.1	8.2
3	Six-Pack	16.3	10.0
4	Half-Bridge	10.4	8.7

Additionally, the position of devices within the water channels may also contribute to this phenomenon. Fig. 5 depicts the cooling channel diagram of the power cycling equipment, wherein water at a constant temperature is injected into the channels via a water chiller. Modules located farther from the outlet of the water chiller has a higher thermal resistance in their cooling circuits compared to those closer to the water chiller.

The relationship between chip junction temperature and thermal resistance is described by the following Equation (1), where T_{vj} is the junction temperature of the device, R_{th} represents the total thermal resistance in the heat dissipation circuit, P is the power dissipation on the device and T_{water_system} is the temperature at the outlet of the water chiller. Both T_{water_system} and I_L remain constant throughout the testing process. Consequently, the junction temperature of the DUT increases with the increase in thermal resistance in the cooling circuit [11].

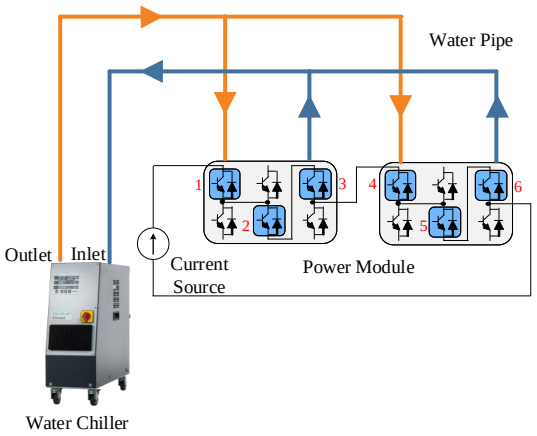

Fig. 5. The water channel diagram of the power cycling equipment

$$T_{vj}=R_{th}\times P+T_{water\_system}=R_{th}\times V_{DUT}\times I_L+T_{water\_system} \quad (1)$$

Meanwhile, the series-connected cooling water pipes may also be affected by the junction temperature fluctuations of the preceding devices, leading to an increase in the coolant temperature and the change in the thermal resistance. Wu conducted research on the estimation of IGBT device junction temperature and cooling liquid temperature based on a thermal model. The issue of thermal coupling in the cooling system has been modeled and discussed. Accuracy of the model has been verified through IR camera validation [12].

To evaluate the impact of the placement position of the tested component in the equipment on ΔT_{vj}, a comparison has been made between the ΔT_{vj} of DUT 6 which is the furthest module from the cooling system outlet and DUT 1 which is less affected by temperature rises from other components. A temperature rises of 2.3K has been found in the comparison. Thus, the temperature rises due to the difference in thermal resistance of the cooling system, as compared in Tab. 2, is not the most significant factor for the inconsistency in ΔT_{vj}, yet it remains an unneglectable factor.

2.2 Compensation Method for the Inconsistency

To compensate for the inconsistency of ΔT_{vj} in devices, increasing the power dissipation on the devices is a feasible approach. Equation (2) represents the on-state power of an IGBT device whose gate voltage exceeds the threshold voltage.

$$P=V_{CE}\times I_L=(V_{PiN}+V_{MOSFET})\times I_L \quad (2)$$

Where, V_{PiN} represents the voltage drop across the PiN junction in the IGBT structure and the V_{MOSFET} represents the voltage drop across the MOSFET in the IGBT celling structure.

As I_L remains constant in the serial structure of power cycling tests, the desired alteration in the device's junction temperature variation can only be achieved by modifying the voltage drop across the device in its on-

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state. Equation (3) represents the formula for the on-state voltage drop of a MOSFET structure. It is evident that the magnitude of the gate voltage can influence the channel resistance, thereby affecting the on-state voltage drop.

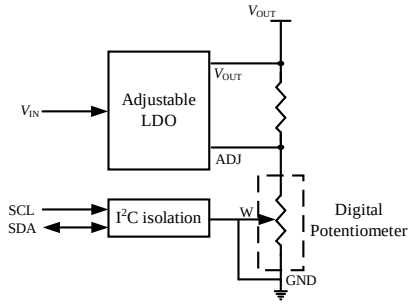
$$V_{\mathrm{MOSFET}} = I_{\mathrm{L}} \times R_{\mathrm{channel}} = I_{\mathrm{L}} \times \left(\frac{L_{\mathrm{channel}}}{Z\mu_{\mathrm{ni}} C_{\mathrm{ox}} (V_{\mathrm{G}} - V_{\mathrm{th}})}\right) \quad (3)$$

Where L_{channel} is the channel length, Z is the channel width orthogonal to the cross section, μ_{ni} is the inversion layer mobility for electrons, C_{ox} is the gate oxide capacitance.

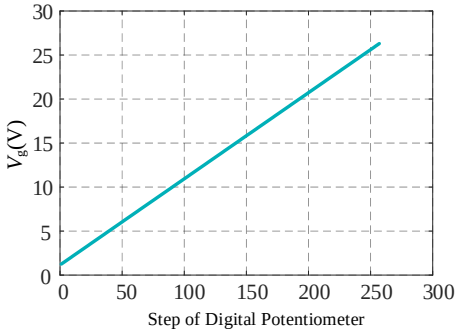
Therefore, whether for IGBT or MOSFET devices, compensating for the inconsistency in junction temperature can be achieved by adjusting their gate voltages.

2.3 Compensating Procedure

The circuit shown in the Fig. 6 (a) is designed to regulate the drive voltage to achieve the adjustment of gate voltage and ultimately ensure the desired ΔT_{vj} of DUT. The digital potentiometer on the feedback pin of the adjustable low dropout regulator (LDO) is controlled via IIC communication to change its resistance, thereby altering the output voltage. The input of the LDO comes from a 24V output of power block and a linear digital potentiometer with a resolution of 256 bits are selected to achieve high-precision and wide-range adjustment of the drive voltage. The output range is as shown in the Fig. 6 (b).



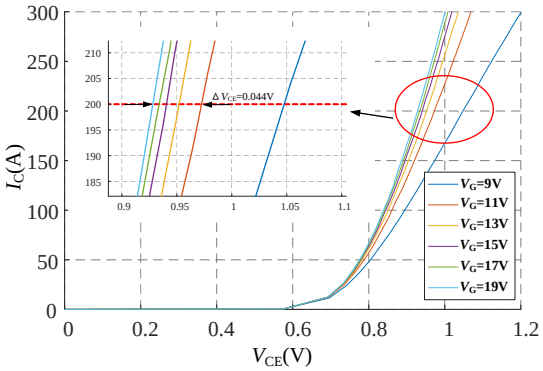
(a) Diagram of voltage adjustment circuit



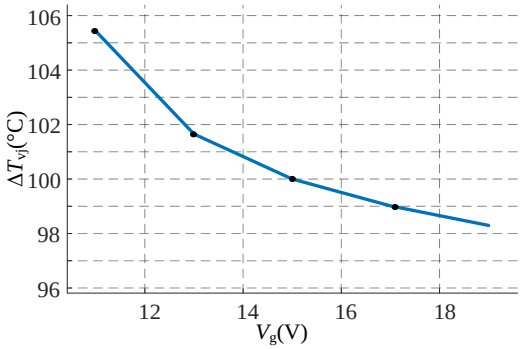
(b) Voltage adjustment range

Fig. 6. The diagram of gate voltage adjustment method

Furthermore, the influence of gate voltage adjustment on the ΔT_{vj} can be analyzed based on the output characteristic of power module. The Fig. 7 (a) shows the output characteristic curves of a IGBT power module under different gate voltages. The ΔT_{vj} at different gate voltages is calculated by multiplying load current with saturation voltage, and then multiplied by the measured thermal resistance. The ΔT_{vj} has been estimated based on the difference in the saturation voltages between different gate voltages. Results are as shown in Fig. 7 (b). For the tested module, when the gate voltage ranges from 11V to 19V, the change in ΔT_{vj} by approximately 7K. Comparing this compensation amount with the range of ΔT_{vj} in the Tab. 2, the method meets the requirements for junction temperature compensation.



(a) Output characteristic under different gate voltages



(b) Estimation of ΔT_{vj} under different gate voltages

Fig. 7. Effect of gate voltage on ΔT_{vj} estimation

In order to achieve the target ΔT_{vj}, it is necessary to determine a compensatory gate voltage for each DUT. As mentioned above, estimating ΔT_{vj} based on output characteristic curves is a feasible approach. Meanwhile, research indicates that base on the calibration of the relationship between voltage, current, and temperature, solving nonlinear equations though the saturation voltage under different current can obtain the junction temperature [9]. However, if these methods are applied to estimate ΔT_{vj} before power cycling, calibration of model parameters for the DUT and multiple measurements of saturation voltage at different currents are required each time before testing for different modules. This may significantly impact testing efficiency.

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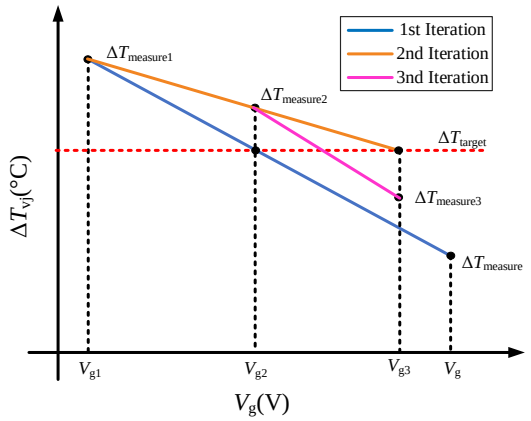
Due to the inherent variability in ΔT_{vj} within each cycle, there isn't a stringent requirement for accuracy in ΔT_{vj} during the parameter tuning stage of power cycling tests. Therefore, to maintain testing efficiency while adjusting gate voltage to achieve the desired ΔT_{vj}, this paper proposes an iterative fitting method. This method does not require modeling for each tested module, reducing the workload of parameter tuning in the initial stage. By fitting the junction temperature fluctuation curve based on ΔT_{vj} at different gate voltages and iterating multiple times, the method obtains a fitting curve near the target junction temperature fluctuation, thereby determining the gate voltage value for compensation.

Method diagram is shown in the Fig. 8(a), where the $\Delta T_{measureN}$ means the result of ΔT_{vj} in the Nth iteration, V_{gN} means the gate voltage used in the Nth iteration and the ΔT_{target} means the target junction temperature fluctuation.

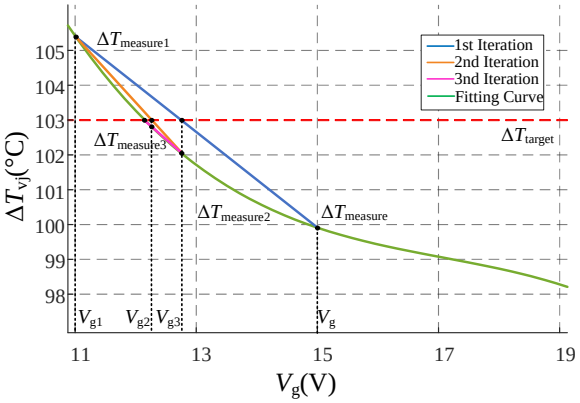
First, measure the $\Delta T_{measure}$ at the standard gate voltage and if the compensation is needed, proceed with the first iteration. In the first iteration, a lower gate voltage V_{g1} will be chosen and measure its $\Delta T_{measure1}$, then form the first iteration fitting curve with the $\Delta T_{measure1}$ and $\Delta T_{measure}$. It's worth noting that excessively low gate voltage power may lead to excessively high power dissipation and subsequent failure. Based on the output characteristic curve from Fig. 7, adjusting within a range of 11V to 19V can bring about a temperature variation of approximately 7K which is within a safe adjustment range. After obtaining the first fitting curve, the gate voltage V_{g2} corresponding to the ΔT_{target} on this curve is selected as the gate voltage for the second iteration, and its measurement result $\Delta T_{measure2}$ and $\Delta T_{measure1}$ will be used to fit the second curve. Then, the iterative steps will repeated until $\Delta T_{measureN}$ hits the ΔT_{target}.

The method has been validated in Fig. 8 (b). In the figure, the relationship between the estimated ΔT_{vj} and V_g based on the output characteristic will be plotted as a curve and compared with the curve iteratively fitted by the gate adjustment method proposed in this paper. After three iterations, a higher similarity is found between the two curves, and a error of 8mV in gate voltage results obtained by the two approaches is calculated. Therefore, the iterative fitting method achieves a higher accuracy while saving parameter calibration time.

The ECPE testing standard AQG324 stipulates that prior to commencing power cycling tests, various parameters must be determined, including the apply time of the load current, the amplitude of the load current, the amplitude of the gate voltage and the flow rate of the cooling liquid [14]. Furthermore, the standard indicates that these testing parameters should not be adjusted midway through the testing process.



(a) Iterative fitting gate voltage adjustment diagram



(b) The result of the iterative fitting method

Fig. 8. Gate voltage adjustment through iterative fitting

Based on the above analysis, a compensation procedure before the PCT for ΔT_{vj} is proposed. The flowchart is shown in the Fig. 9.

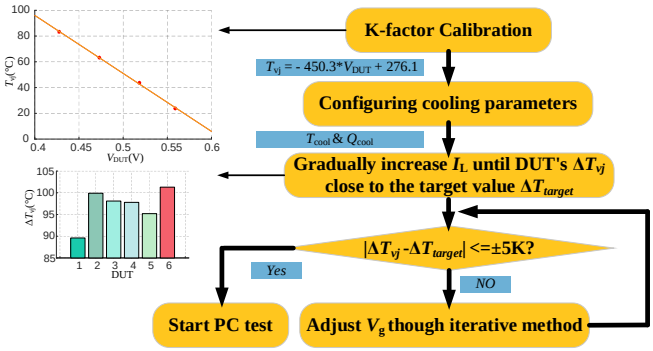


Fig. 9. Junction temperature compensation procedure

First, calibrate the K factor for each DUT to measure the junction temperature. After determining the cooling system parameters, gradually increase the current to ensure that the ΔT_{vj} of each DUT are close to the target ΔT_{vj}. Subsequently, for DUT with significant offsets, adjust their gate voltage though the iterative fitting method to modify the ΔT_{vj} and repeat the iterative steps until the ΔT_{vj} is within the target range. Finally, conduct formal PCT using the adjusted parameters.

3 Validation

3.1 Robustness Analysis

In the process of compensating for the inconsistency in ΔT_{vj}, it is imperative to ensure that the compensation method does not affect the assessment of device lifespan. Furthermore, other functionalities of the power cycling test equipment should not be impeded.

In power cycling tests, it is crucial to measure the junction temperature of the DUT. Accurate measurement of junction temperature is a key aspect of power cycling tests.

3.1.1 Junction temperature measurement method

The recommended method for measuring junction temperature, as outlined in standard AQG324 and commonly used in power cycling tests, is the V_{CE}(T) method [14]. The circuit diagram for this method is depicted in Fig. 10. In the case of IGBT devices where the collector-emitter current is small, the saturation voltage drop across the device primarily occurs across the PN junction within the device. The conduction voltage drop across the PN junction exhibits a linear relationship with temperature. Therefore, to determine the junction temperature of an IGBT device, it is necessary to establish the relationship between the voltage drop across the device at low currents and temperature. Subsequently, the device's junction temperature can be obtained by measuring its voltage drop.

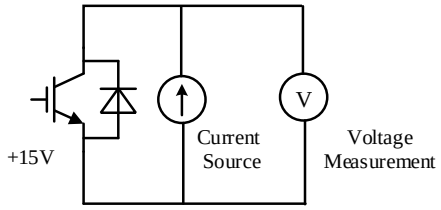


Fig. 10. The circuit diagram for measuring junction temperature

The method of obtaining junction temperature of a chip through electrical parameters is commonly referred to as the thermosensitive electrical parameters measurement method. Prior to junction temperature measurement, the temperature of the DUT is uniformly altered using a temperature-variable device. Once stabilized, the device's junction temperature is assumed to be equal to the external case temperature. Then a small current is injected into the conducting device and its saturation voltage drop will be measured. This process is repeated multiple times at different temperatures and ultimately, a curve representing the relationship between the device's junction temperature and saturation voltage drop is fitted. This process is also known as K-factor calibration.

3.1.2 Influence on the junction temperature measurement

Before conducting power cycling tests, it is necessary to perform K-factor calibration for the DUT. Prior to testing, K-factor calibration is based on standard gate voltage values. However, the junction temperature measured after lowering the gate voltage is still calculated based on the K-factor obtained under the standard gate voltage. Therefore, it is essential to verify whether the gate voltage affects the linear relationship between junction temperature and V_{DUT}.

Referring to Equation (4), the conduction voltage drop of an IGBT device is composed of the voltage drop across the internal PN junction of the device, the base region voltage drop and the voltage drop across the MOSFET structure.

$$V_{CE}=V_{PN}+V_n+V_{MOSFET}=V_{PN}+I_C\times R_n+I_C\times R_{channel} \quad (4)$$

Where, V_{PN} is the voltage drop on the PN junction, IC represents the collector current, V_n is the voltage drop across the base region and R_n represents the base region resistance.

The linear relationship between V_{CE} and device junction temperature originates from the linear relationship between the voltage drop across the PN junction and temperature. Consequently, increases in collector current and channel resistance lead to a higher proportion of nonlinearity in V_{CE}, thereby rendering the relationship between device junction temperature and voltage drop nonlinear. As analyzed in the preceding section, there exists an inverse relationship between the resistance on the channel and the difference between the gate voltage and threshold voltage. This implies that reducing the gate voltage leads to an increase in channel resistance. Consequently, it is evident that decreasing the gate voltage and increasing measure current may both result in the nonlinearity between V_{CE} and device junction temperature.

Therefore, there are three issues that need to be verified whether the method this paper proposed may have an impact on using the VCE(T) method for junction temperature measurement. First issue which needs to verify is whether the linear relationship between the saturation voltage drop and temperature can be maintained after reducing the gate voltage under a measurement current of conventional 100mA. Secondly, it is necessary to assess the influence of lowering the gate voltage on junction temperature measurement under higher measurement current conditions. Finally, whether the relationship calibrated under standard gate voltage can still be used for junction temperature calculation after lowering the gate voltage needs verification.

Fig. 11 illustrates the linear relationship between the on-state voltage drop and junction temperature under three different gate voltages with different measurement current, validating that under the premise of conventional

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testing current of 100mA, the linear relationship between the on-state voltage drop and junction temperature can still be maintained under lower gate voltages. And it verifies that at a bigger testing current of 250mA, reducing the gate voltage does not alter the linear relationship between the on-state voltage drop and junction temperature. However, under larger test current conditions, such as 250mA, an unneglectable impact on the junction temperature measurement results will occur. Therefore, adjustment should be exercised in such scenarios.

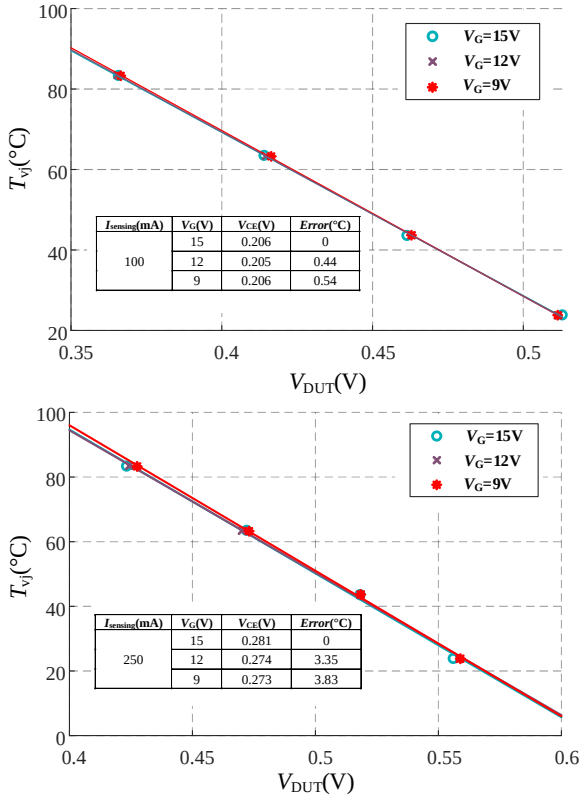

Fig. 11. The linear relationship between on-state voltage drop and junction temperature under different gate voltages

3.2 Experimental Results

In response to the situation depicted in Fig. 2 above, the test parameter was adjusted according to the compensation procedure outlined in this article.

After adjusting the cooling system parameters, a load current of 243A was determined and passed through the test circuit. Upon stabilization of the junction temperature, a significant offset was identified. Consequently, adjustments were made to the gate voltage for these DUT.

The adjusted gate voltage and its corresponding ΔT_{vj} are shown in the following Fig. 12.

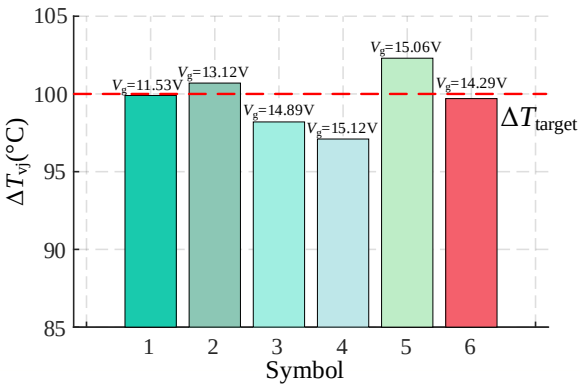

Fig. 12. Consistency of ΔT_{vj} after adjustment

Furthermore, compensation was applied for the testing of modules with different packages from different companies, as depicted in TAB. 2 above. The variance and range of the ΔT_{vj} after compensation are shown in the following TAB. 3.

Tab. 3. Comparison of Data Dispersion Before and After Compensation

Group	Before		After	
	Variance (K)	Range (K)	Variance (K)	Range (K)
1	14.6	11.3	2.77	8.8
2	9.1	8.2	3.11	7.9
3	16.3	13.1	3.43	9.4
4	10.4	9.4	3.03	7.5

It can be observed that the ΔT_{vj} after compensation are all maintained within an acceptable range and there is a noticeable improvement in dispersion.

4 Conclusions

The paper initially analyzed the causes of inconsistency in ΔT_{vj} during PCT and evaluates the impact of thermal resistance differences introduced by device test positions on ΔT_{vj}. Subsequently, a compensation method targeting this inconsistency is proposed, which involves adjusting the gate voltage of the device to modify the ΔT_{vj}. Unlike the limitations imposed by test equipment and topology on load current and cooling conditions, gate voltage can be easily and independently adjusted, making it a low-cost and efficient solution. Additionally, an iterative fitting method is proposed to accurately determine the gate voltage under the target junction temperature fluctuation. Robustness analysis of the compensation method's impact on junction temperature measurement is conducted and the experimental validation demonstrates that the errors remain within acceptable limits.

It is worth noting that this study only validated the effectiveness of reducing gate voltage in adjusting ΔT_{vj} and confirmed its operation when reduced to 9V. If the gate voltage is lowered to an even lower level, it may affect the accurate measurement of chip junction temperature.

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Additionally, when the gate voltage of the chip is close to the threshold voltage, the thermomechanical stress may become concentrated in the channel region, thereby affecting the mechanism of failure. Therefore, the range of gate voltage adjustment in this method still warrants further research. However, as motion above a gate voltage range from 11V to 19V may leads 7K of T_{vj} offset which can meets the requirements in the compensation of the inconsistencies.

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