

# Direct Model Predictive Control of a Five-Level ANPC Inverter with an Adaptive Linear Neuron-based Impedance Estimator

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## Abstract

The paper proposes a direct model predictive control (MPC) method for a five-level active neutral point clamped (5L-ANPC) inverter which includes an online impedance identification through an adaptive linear neuron (ADALINE) estimator. This is adopted to improve the robustness of the underlying MPC against load parameters uncertainty and wear-out, i.e., minimizing model mismatches, while keeping the computational complexity at bay. To this aim, the formulation of a single-layer neural network and the related online training for the application at hand is derived. The MPC optimization problem is designed such that the current reference tracking and the balancing of either the flying capacitors voltages and the neutral point voltage are addressed altogether. The presented results verify the effectiveness of the proposed strategy and demonstrate the performance benefits against impedance variations.

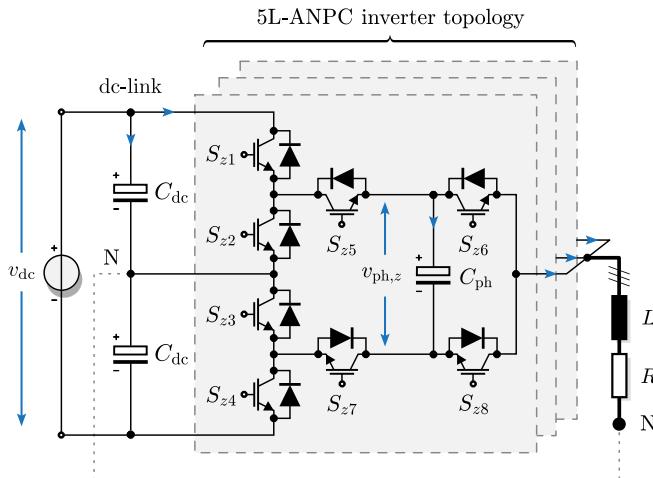
## 1 Introduction

Nowadays multilevel inverter topologies have become the standard in high power<sup>1</sup> and high performance applications [1]. The increasing demand of *load-friendly* inverter solutions poses particular attention to topologies able to produce a high number of voltage levels. Although an higher switching device count results, this facilitate the reduction of voltage and current harmonic distortions and the adoption of semiconductors with lower (voltage) ratings. This paper adopts the 5L-ANPC topology proposed in [2] and [3], which have been emerging as an extension of the conventional three-level neutral point clamped (3L-NPC) one. The neutral point diodes are replaced by active switches and flying capacitors are added to each phase. The circuit of one phase leg is shown in Fig. 1. As a result, the reliability of the 3L-NPC topology is enhanced with the versatility given by the floating phase capacitors. Nevertheless, regulating the load currents while balancing the four internal converter voltages (i.e., the neutral point potential and the three phase capacitors) around their references, proves to be a challenging control problem, particularly when the phase capacitors are small, see e.g., [4]. Indeed, these control objectives must be achieved within the switching frequency constraints of the semiconductor devices and the output harmonic distortion limits of the driven load<sup>2</sup>. Due to its ability to handle multiple system dynamics altogether, its ability to impose explicit constraints, and its very fast transient response, *direct* MPC—also called finite control set MPC (FCS-MPC)—is adopted to address the control and modulation problem of the

5L-ANPC inverter in one computational stage (i.e., without employing a modulator). This results in a significant performance advantage as discussed in [4]. Considering model-based predictions of the future system dynamics, the solution of the FCS-MPC optimization problem relates to the optimal switching sequence which minimize an objective function that resembles the desired output behavior. Multiple examples of such control approach are provided in literature. For instance, [3], [4], and [5] introduced the main direct MPC framework for medium-voltage (MV) drives. For low-voltage (LV) loads, a similar principle was adopted in [6] to minimize the common-mode voltage while achieving a natural balancing of the voltages across the phase capacitors and neutral point potential. The computational effort associated to the FCS-MPC for such kind of inverter topology has been discussed in [7], and an enhanced solving method proposed. For a recent perspective on MPC for power electronic-based control problems, see [1], [8] and the references therein (also including its *indirect* derivation [9]). Since FCS-MPC requires an accurate model of the system to predict its future dynamics, an impedance variation (e.g., due to components aging/stress, overload and saturation conditions) can significantly compromise the controller performance. Thus, an online estimation of the line/load impedance could be used to improve the robustness of the underlying MPC, i.e., minimizing model mismatches. In literature, this framework is sometimes referred to as *adaptive* MPC (either direct or indirect type). Several impedance estimation strategies have been proposed in literature such as the usage of an extended kalman filter (EKF), a model reference adaptive system (MRAS) or a gradient descendant optimization (GDO) algorithm denoted in [10], [11] and [12].

<sup>1</sup>i.e., with power ratings above 500 kW

<sup>2</sup>Along with acceptable  $dv/dt$  and common mode voltages.

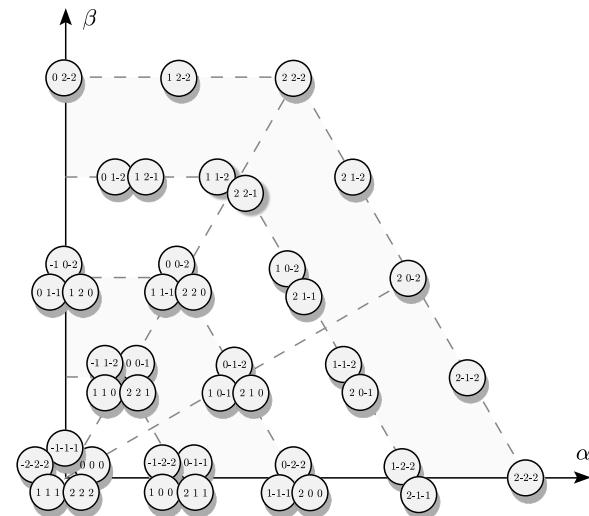


**Fig. 1:** Simplified circuit of a 5L-ANPC inverter (with focus on phase leg  $z$ ) driving an  $RL$  load

Methods based on artificial neural networks (ANN) have also been proposed [13] and gaining considerable attention in the power electronics field. Nevertheless, a significant drawback of these methods is that they typically require an offline training stage for which limited datasets concerning the system are usually available, thus, not covering all parameters variations. Conversely, the ADALINE approach is based on a simple single-layer neural network that is trained online. Furthermore, according to [13] and [14], an ADALINE-based estimator typically requires a lower computational effort and present faster convergence than EKF and MRAS solutions. These aspects turn the ADALINE method into a promising computationally-efficient solution to be used with control approaches that already presents a notable computational burden, which is precisely the case of FCS-MPC. Given the above, this paper proposes an FCS-MPC algorithm which include an ADALINE-based estimator to improve the robustness against parameters uncertainty of the line/load impedance, while keeping the computational complexity at bay. To this aim, the formulation of a single-layer neural network and the related online training for the application at hand is derived. The MPC optimization problem is designed such that the current reference tracking and the balancing of either the flying capacitors voltages and the neutral point voltage are addressed altogether. To simplify the mathematical derivation (without loss of generality), a MV 5L-ANPC inverter connected to an equivalent  $RL$  load is considered as case study. Simulation results would verify the effectiveness of the proposed strategy at steady-state and demonstrate the performance benefits against resistive/inductive variations.

## 2 5L-ANPC Inverter System

Consider the 5L-ANPC inverter topology connected to an  $RL$  load depicted in Fig. 1. The dc-link is divided into an upper and a lower half with the two dc-link capacitors  $C_{dc}$ . Each phase  $z$ , with  $z \in \{a, b, c\}$ , consists of eight switches  $S_{z1}$  to  $S_{z8}$ , with a flying capacitor  $C_{ph}$  placed between the outer pairs of switches. Namely,  $S_{z1} - S_{z4}$



**Fig. 2:** Voltage vectors  $v_{abc}$  produced by a 5L-ANPC topology in the  $\alpha\beta$ -plane along with the phase levels  $u_{abc}$  (only the first quadrant is shown)

refer to the ANPC-group of switches while  $S_{z5} - S_{z8}$  to the flying capacitor (FC)-group of switches in phase  $z$ . Let the voltages across the phase capacitors be denoted by  $v_{ph,z}$ . As described in [4], by imposing  $v_{ph,z} = v_{dc}/4$ , all switches are rated for the same blocking voltage, and the 5L-ANPC topology produces five phase-to-neutral voltages  $\{-v_{dc}/2, -v_{dc}/4, 0, v_{dc}/4, v_{dc}/2\}$  at each phase. These levels can be described by the integer variables  $u_a$ ,  $u_b$ , and  $u_c$ , with  $u_z \in \mathcal{U} = \{-2, -1, 0, 1, 2\}$ , to which we refer as *phase levels*. The latter can be synthesized through the integer variables  $s_a$ ,  $s_b$ , and  $s_c$ , with  $s_z \in \mathcal{S} = \{0, 1, \dots, 7\}$ , to which we refer as *switch positions*. Table 1 details the mathematical correspondence among the introduced operators. Then, the phase voltage  $v_z$  is defined with respect to the dc-link midpoint N such as

$$v_z = \frac{v_{dc}}{4} u_z, \quad (1)$$

provided that the fluctuations on the neutral point potential and the phase capacitor voltages are small<sup>3</sup>. Given that  $v_{abc} = [v_a \ v_b \ v_c]^T$ , the phase voltage vector in the  $\alpha\beta$ -plane—with  $v_{\alpha\beta} = [v_\alpha \ v_\beta]^T$ —is defined<sup>4</sup> by

$$v_{\alpha\beta} = \widetilde{\mathbf{K}} v_{abc} = \frac{v_{dc}}{4} \widetilde{\mathbf{K}} u_{abc} = \frac{v_{dc}}{4} u_{\alpha\beta}. \quad (2)$$

It can be deduced that (2) results in 61 different voltage vectors synthesized by  $\{-2, -1, 0, 1, 2\}^3 = 5^3 = 125$  phase levels  $u_{abc} = [u_a \ u_b \ u_c]^T \in \mathcal{U} = \mathcal{U}^3$ , which in are established based on  $\{0, 1, \dots, 7\}^3 = 8^3 = 512$  distinct switch positions  $s_{abc} = [s_a \ s_b \ s_c]^T \in \mathcal{S} = \mathcal{S}^3$ . Hence, the voltage vector  $v_{abc}$  can be described either in terms of  $u_{abc}$  or  $s_{abc}$ , i.e.,

$$v_{abc} (v_{dc}, u_{abc}) \Leftrightarrow v_{abc} (v_{dc}, s_{abc}). \quad (3)$$

<sup>3</sup>The time dependency ( $t$ ) is dropped from (1). This holds for the remaining of the paper unless otherwise stated.

<sup>4</sup>All variables given in  $abc$  coordinates  $\xi_{abc} = [\xi_a \ \xi_b \ \xi_c]^T$  are mapped into  $\xi_{\alpha\beta} = [\xi_\alpha \ \xi_\beta]^T$  via the reduced Clarke transformation matrix  $\widetilde{\mathbf{K}}$ , see e.g., [5].

**Tab. 1:** Relationship among the phase switch positions  $s_z$ , the phase levels  $u_z$ , the phase voltages  $v_z$ , and the switching states  $S_{z1} - S_{z8}$  for phase  $z$  with  $z \in \{a, b, c\}$

| switch position<br>$s_z$ | phase level<br>$u_z$ | phase voltage |                   | synthesis               | switching state |          |          |          |          |          |          | influence on |        |        |
|--------------------------|----------------------|---------------|-------------------|-------------------------|-----------------|----------|----------|----------|----------|----------|----------|--------------|--------|--------|
|                          |                      | $v_z$         | $\Leftrightarrow$ |                         | $S_{z1}$        | $S_{z2}$ | $S_{z3}$ | $S_{z4}$ | $S_{z5}$ | $S_{z6}$ | $S_{z7}$ | $v_{ph,z}$   | $v_n$  |        |
| 7                        | 2                    | $v_{dc}/2$    | $\Leftrightarrow$ | $v_{dc,up}$             | 1               | 0        | 1        | 0        | 1        | 1        | 0        | 0            | 0      | 0      |
| 6                        | 1                    | $v_{dc}/4$    | $\Leftrightarrow$ | $v_{dc,up} - v_{ph,z}$  | 1               | 0        | 1        | 0        | 1        | 0        | 0        | 1            | $i_z$  | 0      |
| 5                        | 1                    | $v_{dc}/4$    | $\Leftrightarrow$ | $v_{ph,z}$              | 1               | 0        | 1        | 0        | 0        | 1        | 1        | 0            | $-i_z$ | $-i_z$ |
| 4                        | 0                    | 0             | $\Leftrightarrow$ | 0                       | 1               | 0        | 1        | 0        | 0        | 0        | 1        | 1            | 0      | $-i_z$ |
| 3                        | 0                    | 0             | $\Leftrightarrow$ | 0                       | 0               | 1        | 0        | 1        | 1        | 1        | 0        | 0            | 0      | $-i_z$ |
| 2                        | -1                   | $-v_{dc}/4$   | $\Leftrightarrow$ | $-v_{ph,z}$             | 0               | 1        | 0        | 1        | 1        | 0        | 0        | 1            | $i_z$  | $-i_z$ |
| 1                        | -1                   | $-v_{dc}/4$   | $\Leftrightarrow$ | $-v_{dc,lo} + v_{ph,z}$ | 0               | 1        | 0        | 1        | 0        | 1        | 1        | 0            | $-i_z$ | 0      |
| 0                        | -2                   | $-v_{dc}/2$   | $\Leftrightarrow$ | $-v_{dc,lo}$            | 0               | 1        | 0        | 1        | 0        | 0        | 1        | 1            | 0      | 0      |

As well detailed in [5], the 5L-ANPC topology contains both single-phase and three-phase redundancies. In particular, the single-phase redundancy exists among the single-phase switch positions. Indeed, the phase levels  $-1, 0$  and  $1$  can each be obtained by two different  $s_z$ . According to Table 1,  $u_z = 1$  can be generated either by implementing the FC switch configuration  $S_{z5} = 1$ ,  $S_{z6} = 0$ ,  $S_{z7} = 0$  and  $S_{z8} = 1$ —related to  $s_z = 5$ —or with  $S_{z5} = 0$ ,  $S_{z6} = 1$ ,  $S_{z7} = 1$  and  $S_{z8} = 0$ —related to  $s_z = 6$ . The other switches are in both cases set to  $S_{z1} = 1$ ,  $S_{z2} = 0$ ,  $S_{z3} = 1$  and  $S_{z4} = 0$ , thus, no *switch-on* transitions occur in the ANPC part. Both  $s_z = 5$  and  $s_z = 6$  produce the same voltage at the phase terminals, i.e.,  $v_z = v_{dc}/4$ . This redundancy can be used to regulate  $v_{ph,z}$ . However,  $s_z = 5$  and  $s_z = 6$  differently affect the neutral point potential. In addition to the above, Fig. 2 provides a visual example of three-phase redundancy, with  $\mathbf{v}_{abc}$  produced by multiple phase levels  $\mathbf{u}_{abc}$ . For more details on redundancy and switching constraints, the reader is referred to [4] and the reference therein.

## 2.1 Dynamics of the Internal Voltages

The potential of the neutral point N is defined by

$$v_n = \frac{1}{2}(v_{dc,lo} - v_{dc,up}), \quad (4)$$

with  $v_{dc,lo}$  and  $v_{dc,up}$  denoting the voltages over the lower and the upper dc-link half, respectively, i.e.,  $v_{dc} = v_{dc,lo} + v_{dc,up}$ , see Fig. 1. According to [5], the dynamic of the neutral point potential is given by

$$\frac{dv_n}{dt} = -\frac{1}{2C_{dc}}(i_{n,a} + i_{n,b} + i_{n,c}), \quad (5)$$

with  $i_{nz}$  denoting the current drawn from the neutral point such that

$$i_{n,z} = \begin{cases} i_z, & \text{if } s_z \in \{2, 3, 4, 5\} \\ 0, & \text{if } s_z \in \{0, 1, 6, 7\} \end{cases}. \quad (6)$$

Note that (5) depends on all three switch positions and all three phase currents. The dynamic of the capacitor voltage in phase  $z$  is described by

$$\frac{dv_{ph,z}}{dt} = \frac{1}{C_{ph}} \begin{cases} i_z, & \text{if } s_z \in \{2, 6\} \\ -i_z, & \text{if } s_z \in \{1, 5\} \\ 0, & \text{if } s_z \in \{0, 3, 4, 7\} \end{cases}. \quad (7)$$

which depends on the switch position and phase current of phase  $z$  only. According to Table 1, let the auxiliary logic variable  $\delta_{ph,z}$  be defined as

$$\delta_{ph,z} = \begin{cases} 1, & \text{if } s_z \in \{2, 6\} \\ -1, & \text{if } s_z \in \{1, 5\} \\ 0, & \text{if } s_z \in \{0, 3, 4, 7\} \end{cases}. \quad (8)$$

This allows us to rewrite (7) in the compact form

$$\frac{dv_{ph,z}}{dt} = \frac{1}{C_{ph}} \delta_{ph,z} i_z. \quad (9)$$

Similarly, we introduce the three logic variables

$$\delta_{n,z} = \begin{cases} 1, & \text{if } s_z \in \{2, 3, 4, 5\} \\ 0, & \text{if } s_z \in \{0, 1, 6, 7\} \end{cases}, \quad (10)$$

which allow to rewrite (5) such that

$$\frac{dv_n}{dt} = -\frac{1}{2C_{dc}}(\delta_{n,a} i_{n,a} + \delta_{n,b} i_{n,b} + \delta_{n,c} i_{n,c}). \quad (11)$$

Further modeling details can be found in [2], [3] and [4].

## 2.2 Load Dynamics

As shown in Fig. 1, an  $RL$  load is connected between the phase legs terminals and the neutral point potential N. Let the phase current by denoted by  $i_z$ , we define the three-phase current vector  $\mathbf{i}_{abc} = [i_a \ i_b \ i_c]^T$ . As for (2), the dynamic model of the load is derived in the  $\alpha\beta$ -plane considering  $\mathbf{i}_{\alpha\beta} = [i_\alpha \ i_\beta]^T$  as state variable. This yields

$$\frac{d\mathbf{i}_{\alpha\beta}}{dt} = -\frac{R}{L}\mathbf{i}_{\alpha\beta} + \frac{1}{L}\widetilde{\mathbf{K}}\mathbf{v}_{abc}(v_{dc}, \mathbf{s}_{abc}), \quad (12)$$

where  $R$  and  $L$  are the equivalent line/load resistance and inductance, respectively.

## 3 Direct MPC with ADALINE-based Impedance Estimator

The proposed FCS-MPC framework is graphically represented in Fig. 3. The optimal switching actions to be applied to the 5L-ANPC inverter are obtained by solving

within each sampling interval  $T_s$  an (integer-valued) optimization problem based on the dynamic model of the controlled system. This is achieved by resembling the equations described in Sec. 2 in the discrete-time domain. To improve the robustness of the underlying MPC, the ADALINE-based estimator is implemented to minimize model mismatches concerning the line impedance.

### 3.1 Controller Model

We define the state vector (in  $\alpha\beta$ -plane)

$$\mathbf{x} = [i_\alpha \ i_\beta \ v_{ph,a} \ v_{ph,b} \ v_{ph,c} \ v_n]^T \in \mathbb{R}^6, \quad (13)$$

and the output vector  $\mathbf{y} = \mathbf{x} \in \mathbb{R}^6$ . As input vector, we choose the three-phase switch position, recalling

$$\mathbf{s}_{abc} = [s_a \ s_b \ s_c]^T \in \mathcal{S} = \mathcal{S}^3 = \{0, 1, \dots, 7\}^3. \quad (14)$$

This choice allows to formulate an MPC problem which takes into consideration both kinds of single- and three-phase topological redundancies when applying a given combination, see Sec. 2. As denoted in (2), the three-phase voltage  $v_{abc}$  can be computed as a function of  $\mathbf{s}_{abc}$ . Nevertheless, since different  $\mathbf{s}_{abc}$  values can produce the same  $v_{abc}$ , the effect of  $\mathbf{s}_{abc}$  on  $v_{ph,z}$  and  $v_n$  must be considered. By assuming a constant dc-link voltage  $v_{dc} = V_{dc}$ —i.e., drooping it from the list of arguments—we introduce the simplified notation

$$v_{abc}(\mathbf{s}_{abc}, \mathbf{x}). \quad (15)$$

which uses the state  $\mathbf{x}$  to map the beyond effect of a three-phase voltage and thus translating Table 1. Combining (9), (11), and (12), the evolution of the system dynamics is described by the following continuous-time state-space model

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{F}(\mathbf{s}_{abc}(t)) \mathbf{x}(t) + \mathbf{G}\mathbf{v}_{abc}(\mathbf{s}_{abc}(t), \mathbf{x}(t)) \quad (16)$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t), \quad (17)$$

where the matrix  $\mathbf{F}(\mathbf{s}_{abc}) \in \mathbb{R}^{6 \times 6}$  and  $\mathbf{G} \in \mathbb{R}^{6 \times 3}$  are

$$\mathbf{F}(\mathbf{s}_{abc}) = \begin{bmatrix} -I_2 \frac{R}{L} & \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} & \mathbf{0}_{2 \times 1} \\ \mathbf{0}_{1 \times 2} & \frac{\delta_{ph,a}}{C_{ph}} & 0 & 0 & 0 \\ \mathbf{0}_{1 \times 2} & 0 & \frac{\delta_{ph,b}}{C_{ph}} & 0 & 0 \\ \mathbf{0}_{1 \times 2} & 0 & 0 & \frac{\delta_{ph,c}}{C_{ph}} & 0 \\ \mathbf{0}_{1 \times 2} & -\frac{\delta_{n,a}}{2C_{dc}} & -\frac{\delta_{n,b}}{2C_{dc}} & -\frac{\delta_{n,c}}{2C_{dc}} & 0 \end{bmatrix} \quad (18)$$

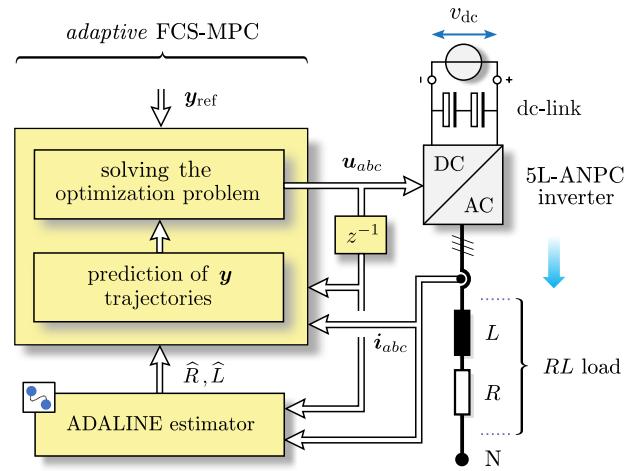
$$\mathbf{G} = [I_2 \frac{1}{L} \ \mathbf{0}_{2 \times 4}]^T \widetilde{\mathbf{K}}. \quad (19)$$

Note that,  $\mathbf{F}(\mathbf{s}_{abc})$  is function of the auxiliary logic variables  $\delta_{ph,z}$  and  $\delta_{n,z}$ , which in turn depend on the three-phase switch position  $\mathbf{s}_{abc}$ . We derive the discrete-time representation of the system by integrating (16) from  $t = kT_s$  to  $t = (k+1)T_s$  using the forward Euler discretization method within  $T_s$ . This leads to the discrete-time state-space model

$$\mathbf{x}(k+1) = \mathbf{A}(\mathbf{s}_{abc}(k)) \mathbf{x}(k) + \mathbf{B}\mathbf{v}_{abc}(\mathbf{s}_{abc}(k), \mathbf{x}(k)) \quad (20)$$

$$\mathbf{y}(k) = \mathbf{C}\mathbf{x}(k), \quad (21)$$

with  $\mathbf{A}(\mathbf{s}_{abc}) = \mathbf{I}_6 + \mathbf{F}(\mathbf{s}_{abc})T_s$  and  $\mathbf{B} = \mathbf{G}T_s$ .



**Fig. 3:** Block scheme of the proposed direct MPC with the ADALINE estimator for the line/load impedance

### 3.2 FCS-MPC Problem Formulation

The direct MPC aims to regulate the load currents while balancing either the flying capacitors voltages and the neutral point voltage. The output vector  $\mathbf{y} = \mathbf{x}$  in (13) must follow its reference  $\mathbf{y}_{ref} \in \mathbb{R}^6$ , i.e.,

$$\mathbf{y}_{ref} = [i_{\alpha\beta,\text{ref}} \ v_{ph,a,\text{ref}} \ v_{ph,b,\text{ref}} \ v_{ph,c,\text{ref}} \ v_{n,\text{ref}}]^T, \quad (22)$$

to minimize the current total harmonic distortion (THD), i.e.,  $I_{\text{THD}}$ . The reference  $i_{\alpha\beta,\text{ref}} = [i_{\alpha,\text{ref}} \ i_{\beta,\text{ref}}]^T$  can be computed according to a phasor analysis [9] or second-order extrapolation, while the phase capacitor voltage and the neutral point potential are set to  $v_{n,\text{ref}} = 0$  and  $v_{ph,z,\text{ref}} = v_{dc}/4$ , respectively. For a one-step prediction horizon— $N_p = 1$ —the designed objective function is

$$J(k) = \|\mathbf{y}_{ref}(k+1) - \mathbf{y}(k+1)\|_Q^2 + \lambda_u \|\Delta\mathbf{s}_{abc}(k)\|_2^2. \quad (23)$$

The first term of (23) penalizes the output vector deviation by weighting it with the matrix<sup>5</sup>

$$\mathbf{Q} = \begin{bmatrix} I_2 q_i & \mathbf{0}_{2 \times 3} & \mathbf{0}_{2 \times 1} \\ \mathbf{0}_{3 \times 2} & I_3 q_{v_{ph}} & \mathbf{0}_{3 \times 1} \\ \mathbf{0}_{1 \times 2} & \mathbf{0}_{1 \times 3} & q_{v_n} \end{bmatrix}. \quad (24)$$

The diagonal entries of  $\mathbf{Q} \in \mathbb{R}^{6 \times 6}$ , i.e.,  $q_i, q_{v_{ph}}, q_{v_n}$ , may differ from each other to prioritize the tracking accuracy among the different entries of  $\mathbf{y}$  [15]. The second term of (23) penalizes the switching effort

$$\Delta\mathbf{s}_{abc}(k) = \mathbf{s}_{abc}(k) - \mathbf{s}_{abc}(k-1), \quad (25)$$

by counting the number of switch-on transitions per each phase for a given commutation from  $\mathbf{s}_{abc}(k-1)$  to  $\mathbf{s}_{abc}(k)$ . The weighting factor  $\lambda_u \in \mathbb{R}^+$  is introduced to penalize  $\Delta\mathbf{s}_{abc}$  and indirectly regulate the inverter average switching frequency  $f_{sw,\text{avg}}$  to a desired target value. Indeed,  $\Delta\mathbf{s}_{abc}$  influence the calculation of  $f_{sw,\text{avg}}$  such that

$$f_{sw,\text{avg}} = \lim_{N_w \rightarrow \infty} \frac{1}{24N_w T_s} \sum_{\ell=0}^{N_w-1} \|\Delta\mathbf{s}_{abc}(k)\|_1, \quad (26)$$

<sup>5</sup>with  $\mathbf{Q}$  being a positive semidefinite matrix, i.e.,  $\mathbf{Q} \succeq 0$

where  $N_w$  denotes a generic time interval within which the averaging (among  $8 \times 3 = 24$  active switches) is performed<sup>6</sup>. Note that, following (26), different commutation paths from  $s_{abc}(k-1)$  to  $s_{abc}(k)$  may lead to different value of  $f_{sw,avg}$ , thus, different switching losses.

To compute the optimal control input  $s_{abc}^*$  which minimizes (23), the following integer quadratic program (IQP) needs to be solved in real time

$$s_{abc}^*(k) = \arg \underset{s_{abc}(k) \in \mathcal{S}}{\text{minimize}} J(k) \quad (27)$$

$$\text{subject to } \mathbf{x}(k+1) = \mathbf{A}(s_{abc}(k)) \mathbf{x}(k) + \mathbf{B} \mathbf{v}_{abc}(s_{abc}(k), \mathbf{x}(k)) \quad (28)$$

$$\mathbf{y}(k+1) = \mathbf{C} \mathbf{x}(k+1) \quad (29)$$

$$s_{abc}(k) \in \mathcal{S} = \{0, 1, \dots, 7\}^3. \quad (30)$$

The dynamic evolution of the system is predicted for one time step ahead in time—i.e.,  $\mathbf{x}(k+1)$  and  $\mathbf{y}(k+1)$ —by applying each combination of  $s_{abc}$ . The optimal solution  $s_{abc}^*$  is found by (brute-force) exhaustive enumerating all feasible  $s_{abc}$  and choosing the one which leads to the minimal  $J$ —i.e., the one that achieves the best output reference tracking. It is worth recalling that different combinations of  $s_{abc}$  can produce the same voltage  $\mathbf{v}_{abc}$  that is considered in (28) to calculate  $\mathbf{x}(k+1)$ . Hence, evaluating the effect of  $s_{abc}$  on  $v_{ph,z}$  and  $v_n$  via (15) is fundamental to select the optimal switch positions. In this regards, the modeling proposed in Sec. 2 is beneficial. Indeed, the deviation of the phase capacitor voltage and the neutral point potential from their reference values are explicitly calculated in  $J$  as function of  $s_{abc}$ . This address an inherent balancing mechanism as previously stated. Different balancing techniques may be also utilized, see Appendix. At the next control iteration, the optimization procedure is repeated at  $k+1$  based on an updated state information over a shifted prediction horizon [1].

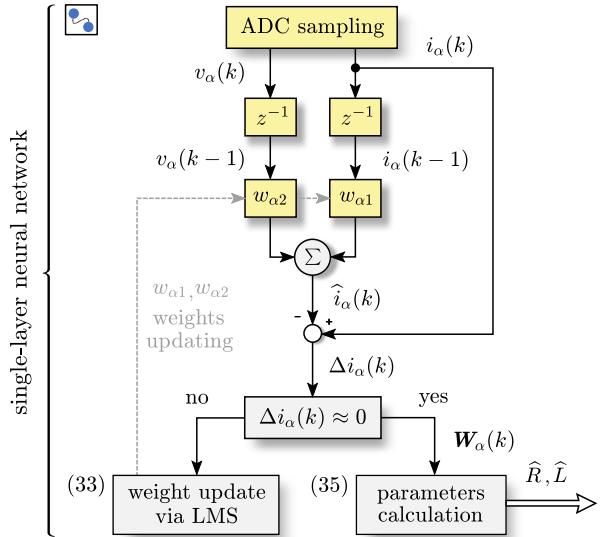
### 3.3 ADALINE-based Estimator

The  $RL$  load values both influence  $\mathbf{F}(s_{abc})$  and  $\mathbf{G}$  in (18)-(19), thus, the state-update predictions  $\mathbf{x}(k+1)$  computed in (28). Due to that, the controller model adopted by the FCS-MPC is refined with an online update of the resistance  $R$  and inductance  $L$ . This is achieved by designing an ADALINE estimator. Given (20), the load current predictions can be isolated and resembled within the time interval from  $k-1$  to  $k$ , i.e.,

$$\mathbf{i}_{\alpha\beta}(k) = \left(1 - \frac{RT_s}{L}\right) \mathbf{i}_{\alpha\beta}(k-1) + \left(\frac{T_s}{L}\right) \mathbf{v}_{\alpha\beta}(k-1) \quad (31)$$

where  $\mathbf{v}_{\alpha\beta} = \widetilde{\mathbf{K}} \mathbf{v}_{abc}$  and  $\mathbf{v}_{abc}(s_{abc}(k-1), \mathbf{x}(k-1))$  hold. The ADALINE structure performs a parameter estimation through a single-layer neural network which

<sup>6</sup>It is common to consider a value of  $N_w$  which allows to cover at least 10-20 periods of  $T_s$ . Moreover, it is worth mentioning that, intrinsically, the FC switches carry the majority of the switching burden and thus constitute the limiting factor in terms of maximal switching losses. This is masked by the proposed averaging calculation in (26), see [2] and [4].



**Fig. 4:** Graphical representation of the ADALINE-based estimation principle for the  $\alpha$ -component (hybrid flowchart)

is mathematically represented by a linear function. The latter is synthesized by combining a set of state/input variables with a set of adaptive weights. According to (31) and recalling that  $\mathbf{i}_{\alpha\beta} = [i_\alpha \ i_\beta]^T$  while  $\mathbf{v}_{\alpha\beta} = \widetilde{\mathbf{K}} \mathbf{v}_{abc}$ , the proposed candidate specific for the  $\alpha$ -component is

$$\hat{i}_\alpha(k) = \underbrace{w_{\alpha 1}(k) i_\alpha(k-1)}_{\text{weight 1}} + \underbrace{w_{\alpha 2}(k) v_\alpha(k-1)}_{\text{weight 2}}, \quad (32)$$

where  $\hat{i}_\alpha$  is the component-wise estimated load current, and  $w_{\alpha 1}, w_{\alpha 2}$  are adaptive weighting factors. The estimated value is compared with the respective measured one. The resulting estimation error, defined as

$$\Delta i_\alpha(k) = i_\alpha(k) - \hat{i}_\alpha(k), \quad (33)$$

is used as the input of an online *weight adaptation* algorithm. Specifically, the baseline principle of the ADALINE estimator is the adoption of a least mean square (LMS) method to minimize  $\Delta i_\alpha$ . This translates into recursively adjusting the adaptive weights  $w_{\alpha 1}$  and  $w_{\alpha 2}$  at every  $T_s$  through the following rule [14]

$$\mathbf{W}_\alpha(k+1) = \mathbf{W}_\alpha(k) + \frac{\eta \Delta i_\alpha(k) \boldsymbol{\gamma}_\alpha(k-1)}{1 + \boldsymbol{\gamma}_\alpha^T(k-1) \boldsymbol{\gamma}_\alpha(k-1)}, \quad (34)$$

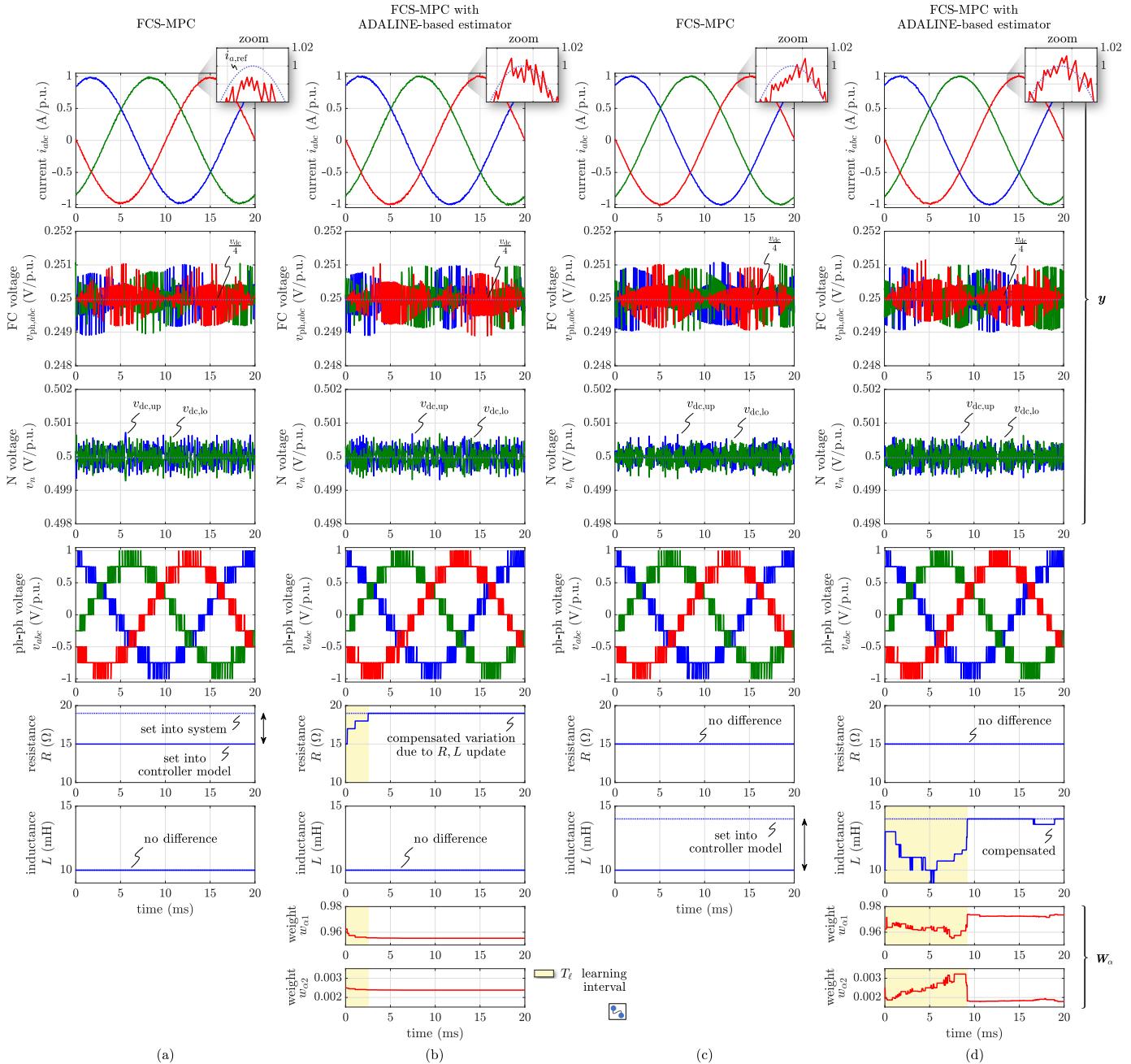
with  $\mathbf{W}_\alpha = [w_{\alpha 1} \ w_{\alpha 2}]^T$  being the adaptive weights vector. The compact notation<sup>7</sup> in (34) also adopts the vector

$$\boldsymbol{\gamma}_\alpha(k-1) = [i_\alpha(k-1) \ v_\alpha(k-1)]^T \in \mathbb{R}^2, \quad (35)$$

while  $\eta$  is the *learning rate*<sup>8</sup> which defines the learning time interval  $T_\ell$ . Since a new ADALINE iteration takes place at every  $T_s$ , the latter would be a multiple of  $T_s$ , i.e.,  $T_\ell \approx \nu T_s$  with integer  $\nu \in \mathbb{N}$ . By constantly adjusting the weights over  $T_\ell$ , at steady-state  $w_{\alpha 1}$  and  $w_{\alpha 2}$  should converge to approximately constant values.

<sup>7</sup>Note that a positive coefficient  $\xi$  may be included to scale the denominator, which becomes  $1 + \xi \boldsymbol{\gamma}_\alpha^T(k-1) \boldsymbol{\gamma}_\alpha(k-1)$ .

<sup>8</sup>The value of  $\eta$  is a design choice. In general, the larger  $\eta$  is, the quicker the parameters estimation is performed.



**Fig. 5:** Steady-state simulated waveforms in p.u. during (a) line resistance variation and (c) line inductance mismatches for a conventional FCS-MPC. The same parameter variations hold in (b) and (d), respectively, for the proposed FCS-MPC with an ADALINE-based estimator. The set  $\eta = 0.0001$ ,  $w_{\alpha 1}(0) = 0.97$  and  $w_{\alpha 2}(0) = 0.0025$  is chosen and applied in both test cases, with  $T_\ell \ll T_1 = 20$  ms, while  $\lambda_u$  is adjusted to achieve the same  $f_{sw} \approx 4$  kHz.

For instance, if  $\Delta i_\alpha \approx 0$ , the base parameters of the line/load impedance<sup>9</sup> are estimated such that

$$\hat{R} \approx 1 - \frac{w_{\alpha 1}(k)}{w_{\alpha 2}(k)} \quad \hat{L} \approx \frac{T_s}{w_{\alpha 2}(k)}, \quad (36)$$

with  $\mathbf{W}_\alpha(k+1) \approx \mathbf{W}_\alpha(k)$ . Such estimated values are then considered to update the controller model of the FCS-MPC. Such update is performed at every  $T_s$ . Note that, assuming a balanced symmetrical three-phase system, performing the component-wise calculation (either in  $\alpha$  or  $\beta$ ) in (36) is sufficient to estimate the  $RL$  load. Nevertheless, to address unsymmetrical load and/or different components wear-out between phases, (31) can be easily derived in  $abc$  coordinates and the calculation

steps (31)-(36) repeated for each individual phase  $z$ . A graphical representation of the ADALINE estimation steps is provided in Fig. 4 as hybrid flowchart. Compared to other estimation methods, the adoption of a single-layer neural network with a LMS minimization method results in a low computational complexity, being an attractive features for embedded implementation either combined with such MPC framework or standalone.

## 4 Performance Evaluation

The effectiveness of the proposed direct MPC combined with an ADALINE-based estimator are evaluated through MATLAB/Simulink simulations. The 5L-ANPC converter denoted in Fig. 1 is fed by a constant dc-link voltage of 7.2 kV, with equal dc-link capacitors

<sup>9</sup>For a constant angular frequency, it follows  $\hat{Z} = \hat{R} + \omega_1 \hat{L}$

$C_{dc} = 1 \text{ mF}$  and a flying capacitor  $C_{ph} = 1 \text{ mF}$ , respectively. The  $RL$  load is characterised by  $R = 15 \Omega$  and  $L = 10 \text{ mH}$  as rated values. The controller is operated with a sampling interval of  $T_s = 25 \mu\text{s}$  with the goal of managing a power transfer from the dc to ac side subject to a rated current of 180 A. The tracking of  $i_z$ ,  $v_{ph,z}$  and  $v_n$  is equally prioritized, i.e.,  $Q = I_6$ , while  $\lambda_u$  is adjusted between the various simulation tests such that a  $f_{sw,\text{avg}} \approx 4 \text{ kHz}$  results in all cases. The closed-loop behaviour of the system is examined while being controlled with the direct MPC scheme *with or without* the ADALINE-based estimator.

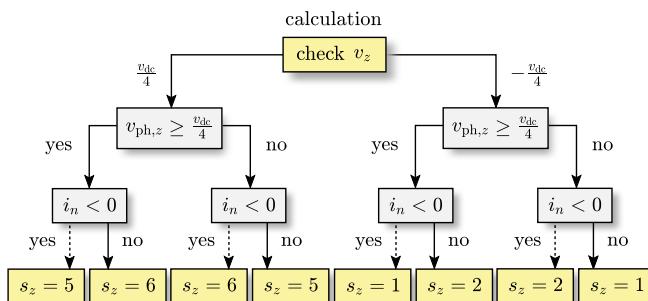
Different steady-state results are shown in Fig. 5, where all quantities are given in per unit (p.u.)<sup>10</sup> over one fundamental period with a line/load frequency of  $f_1 = 50 \text{ Hz}$  (i.e.,  $T_1 = 1/50 \text{ Hz} = 20 \text{ ms}$ ). Fig. 5(a) and (b) show the effects of a +26% resistive load mismatch between the  $R$  value adopted into the controller model—i.e., the rated value  $R = 15 \Omega$ —and the one effectively present in the system—i.e.,  $R = 15 \Omega + 26\% = 19 \Omega$ . The inductance value  $L$  is not affected (i.e., a constant  $L = 10 \text{ mH}$  is considered). In particular, Fig. 5(a) denotes the response of the FCS-MPC without the ADALINE-based estimator. The currents  $i_{abc}$  do not track their reference values accurately, producing a notable offset at their peak values, e.g., see the zoom given in the upper-right part of the figure. On the contrary, this inaccuracy is solved by adopting the ADALINE-based estimator as shown in Fig. 5(b). The recursive calculation of  $\hat{R}$  starts at  $t = 0$  updating the controller model with a refined value of  $\hat{R}$  at every  $T_s$ . This leads to effectively compensate the load mismatch and improve the reference tracking performance at same  $f_{sw,\text{avg}}$ . The learning rate  $\eta$  is set such that a learning interval  $T_\ell \ll T_1 = 20 \text{ ms}$  results, i.e., an accurate estimation of  $\hat{R}$  and the following parameter updating is performed way within a fundamental period. The voltages  $v_{ph,z}$  and  $v_n$  track their reference values with good accuracy both in Fig. 5(a) and (b). Since these quantities are mostly related to the capacitors  $C_{dc}$  and  $C_{ph}$  variation, the effect provided by the resistance variation is minor (despite being physically present through  $i_z$ , see (5)-(11)). Similar results are achieved in Fig. 5(c) and (d) concerning a +40% line/load inductance mismatch between the  $L$  value adopted into the controller model—i.e., the rated value  $L = 10 \text{ mH}$ —and the one effectively present in the system—i.e.,  $L = 10 \text{ mH} + 40\% = 14 \text{ mH}$ . The resistance value  $R$  is not affected (i.e., a constant  $R = 15 \Omega$  is considered). Compared to Fig. 5(c), the results of the FCS-MPC with the ADALINE-based estimator leads to compensate the current tracking inaccuracy through the recursive parameter update as shown in Fig. 5(d). Despite the bigger numerical mismatch (in percentage) compared to the resistive test, the ADALINE-based estimator accurately calculate  $\hat{L}$  within a fundamental period. The previous considerations on  $v_{ph,z}$  and  $v_n$  dynamics hold also for this case. Overall, the simulation results shown in Fig. 5(b) and (d) demonstrate the

performance benefits against impedance variations (either resistive and inductive) provided by the ADALINE framework along with the capability of simultaneously tracking the load currents and the inverter voltages. Regarding the design of the ADALINE-based estimator, note that the choice of the starting value (at  $t = 0$ ) for  $w_{\alpha 1}$  and  $w_{\alpha 2}$  combined with the value of  $\eta$  determine the interval  $T_\ell$ . Specifically, the same set of  $\eta$ ,  $w_{\alpha 1}(0)$  and  $w_{\alpha 2}(0)$  has been applied for both the test cases. Therefore, despite being lower than  $T_1$ , the resulting  $T_\ell$  achieved for the resistive mismatch case differs from the one resulting for the inductive case, which is longer due to the larger difference in the inductance mismatch. This is clearly visible comparing the last rows of Fig. 5(b) and (d) (yellow area). Given that, it is intuitive to state that the final numerical value of  $w_{\alpha 1}$ —theoretically defined such that  $w_{\alpha 1}(\infty)$  for  $t \rightarrow \infty$ —and  $w_{\alpha 2}$  calculated from (34) for the resistive mismatch will be different from the ones resulting for the inductive mismatch. This is evident by comparing the steady-state values of  $w_{\alpha 1}$  and  $w_{\alpha 2}$  in Fig. 5(b) and (d). Nevertheless, the ADALINE framework relies into an automated recursive process, thus, inherently addressing those calculations. This represents a key benefit of the proposed online training. According to the considerations above, a set of  $\eta$ ,  $w_{\alpha 1}(0)$  and  $w_{\alpha 2}(0)$  have been chosen such that the calculation time required to achieve a  $\hat{L}$  estimation (i.e., the most demanding one among the two) within a 1% tolerance compared to its rated values would not exceed one fundamental period. The values are denoted in Fig. 5. Concerning the algorithm scheduling, the estimator calculations runs in parallel to the FCS-MPC ones. It might be beneficial to define a *stopping criteria* for the ADALINE framework which avoids excessive calculations nor continuous update of the controller model. For instance, without loss of generality, a stopping criteria can be implemented by producing a trigger when the estimation error is within 1% tolerance.

## 5 Conclusion

This paper presented a strategy to improve the robustness of a direct MPC against load parameters uncertainty and wear-out, i.e., minimizing model mismatches, while keeping the computational complexity low. This is achieved by adopting an online impedance identification method based on an ADALINE estimator, which exploits a simple single-layer neural network that is trained online. This typically requires a lower computational effort and present faster convergence than more conventional methods, being a promising computationally-efficient solution to be used with control approaches that already presents a notable computational burden, which is precisely the case of FCS-MPC. A 5L-ANPC inverter driving an  $RL$  load is considered as case study. The multi-objective optimization problem concerning MPC has been formulated along with the single-layer neural network and the related online training for the application at hand. Simulation results shown the effectiveness

<sup>10</sup>See e.g., [5] and [9] for an overview of the p.u. derivation and definition of the base values starting from the rated ones.



**Fig. 6:** Switch position  $s_z$  selection based on  $v_z$  (via  $u_z$ ) implementing a balancing mechanism for phase  $z$

of the proposed method in presence of either resistive and inductive mismatches. Therefore, the proposed approach is particularly suitable when a limited datasets concerning the system characteristic occur. Design guidelines for both the FCS-MPC and ADALINE-based estimator have been provided, highlighting the possibility of further improvements.

## 6 Appendix

As defined in Sec. 2, the 61 voltage vectors of the 5L-ANPC topology can be synthesized by considering the phase level, i.e.,  $u_{abc} = [u_a \ u_b \ u_c]^T \in \{-2, -1, 0, 1, 2\}^3$  ( $5^3 = 125$  combinations) or the switch position which establish the phase levels, i.e.,  $s_{abc} = [s_a \ s_b \ s_c]^T \in \{0, 1, \dots, 7\}^3$  ( $8^3 = 512$  combinations). The FCS-MPC optimization problem defined in (27) considers  $s_{abc}$  as the optimization variable, thus, exploring 512 candidates at every control cycle. The calculation effort is a quite important aspect of MPC [16]. To reduce such exhaustive search iterations to compute the optimal solution, the phase level  $u_{abc}$  can be adopted instead, i.e., calculating  $u_{abc}^*$ . Nevertheless, such approach cut-loose the single-phase redundancy among the switch position which has to be re-established. This can be done in different ways, e.g., adopting the evaluation algorithm described in [7] and [17] and graphically represented (in a simplified manner) in Fig. 6.

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