Current Sharing Issues of Paralleled SiC MOSFET

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Abstract

For paralleling SiC MOSFET, there are many technical challenges including current imbalance, different thermal performance and over voltage. In this paper, theoretical analysis and mathematical calculation of different circuit parameters' effect on current sharing of paralleled SiC MOSFET is presented. Simetrix simulation based on SPICE model is proposed to investigate the influence of different parameters on current sharing. Driver circuit design suggestions and gate resistance design method are provided. Based on the theoretical analysis, gate loop design method can improve the imbalance due to circuit and device parameters mismatch.

1 Introduction

With the development of market and application, high-power rating and high-power density are more and more essential. Nowadays, silicon carbide (SiC) MOSFET has many advantages compared to IGBT in different applications due to its characteristics: low Rdson especially on light load, low switching loss, high thermal conductivity [1]. In electric vehicle (EV), EV charger, solar and ESS applications, SiC MOSFET is widely used [2].

Advanced semiconductor manufacturers, like Infineon, could provide wide SiC MOSFET module portfolio to meet the high-power demands and enlarge SiC MOSFETs' application range. Meanwhile, paralleling discrete SiC MOSFET is also very commonly used because of its flexibility. And the positive temperature coefficient of ON-resistance R_{dson} helps mitigate the static current sharing for SiC MOSFET to work in parallel [3].

Although positive temperature coefficient exists, when SiC MOSFETs are paralleled, current imbalance is still the main challenge. There are two kinds of imbalance: ON-state current imbalance and dynamic current imbalance. To achieve high reliability, operation derating of the MOSFETs is usually required, which will lead to additional cost and comparing to the ideal case, require oversized chip or more in parallel. It is the difference of parameters(mismatch/delta) and the asymmetry (unmatched) of the layout which are all important for paralleling. Circuit parameters mainly come from the PCB layout or busbar build process.

In this paper, theoretical analysis and mathematical calculation of different circuit parameters' effect on current sharing of paralleled SiC MOSFET is presented. SPICE simulation results are shown to verify the theoretical analysis. According to mathematical calculation and qualitative analysis, driver circuit design suggestions and gate resistance design method are provided to improve the SiC MOSFET parallel performance.

2 Theoretical Analysis and Calculation

Mismatched device parameters of SiC MOSFET and power circuit parameters both have impact on the current sharing performance of SiC MOSFET paralleling [4,5]. This section provides the theoretical analysis of different parameters' influence on current sharing. And qualitative analysis can be seen from the calculation process. Tab. 1 lists the parameters which have effect on the current sharing of paralleled SiC MOSFET, differentiating between semiconductor and circuit parameters. However, in this paper we will focus on the latter.

Tab. 1. Effective parameters for current sharing

	Semiconductor parameter	**Circuit parameter**
ON-state current sharing	ON resistance R_{dson}	Power loop stray inductance L_{sp}
Dynamic current sharing	Threshold voltage $V_{gs\text{-}th}$	Driver stray inductance L_{sg}
	Device capacitance	Source stray inductance L_s
	transconductance g_{fs}	
	Internal gate resistance $R_{g\text{-}in}$	

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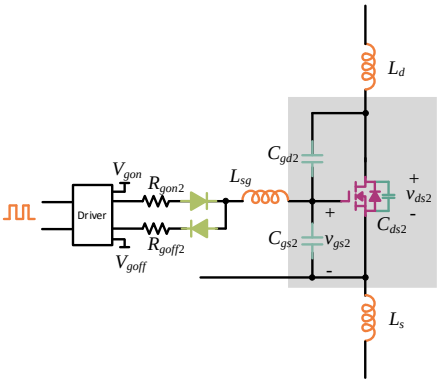
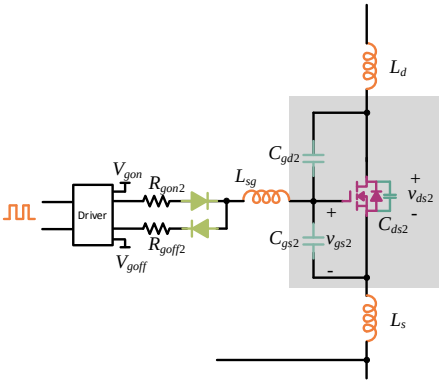
2.1 ON-state Current Sharing

Current sharing can be divided into ON-state current sharing and dynamic current sharing. Dynamic current sharing is focused on switching process and ON-state current sharing is mainly for ON state.



a. 4 pin stray parameters



b. 3 pin stray parameters

Fig. 1. Drain stray inductance L_d, source stray inductance L_s and driver stray inductance L_{sg} in circuit

2.1.1 Rdson

SiC MOSFET ON-resistance R_{dson} is the direct factor for ON-state current sharing. However, the positive temperature coefficient of R_{dson} can improve the initial ON-state current difference to some extent.

2.1.2 Power Loop Stray Inductance

In practical application, inductive loads are usually connected, like boost converter. There is a certain slope of quiescent current, the current of device is changing. So power loop stray inductance would have influence on the current sharing. The impact will sustain even under steady ON state since the i_{ce} is not a stable value, like inductive loads or resonant converter, e.g. LLC converter.

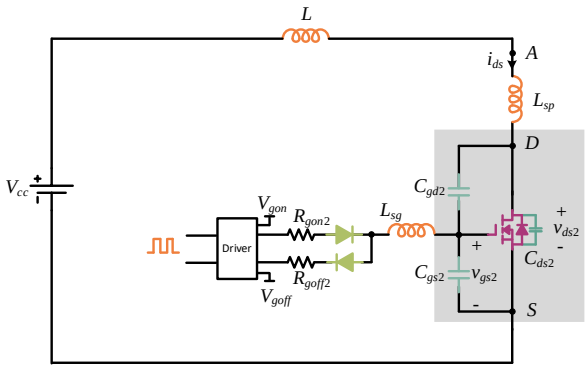


Fig. 2. Schematic for power loop stray inductance impact

Power loop stray inductance consist of drain stray inductance L_d and source stray inductance L_s in Fig. 1. Take the power loop stray inductance as L_{sp} as in Fig. 2, the influence can be expressed as below:

$$V_{as}(t) = R_{dson} \times i_{ds}(t) + L_{sp}\frac{di_{ds}(t)}{dt} \tag{1}$$

Assuming the circuit is boost topology, voltage source is V_{cc} and inductor is L, R_{dson} for two paralleling devices are same, power loop stray inductance is L_{sp1} and L_{sp2} separately, the circuit initial current is I_o, the current sum of device 1 and 2 is:

$$i_{sum}(t) = I_o + \frac{V_{cc}}{L}t \tag{2}$$

then the current of device 1 from two paralelling device is:

$$i_{ds1}(t) = C \times e^{-\frac{2R_{dson}t}{L_{sp1}+L_{sp2}}} + \frac{LR_{dson}I_o + L_{sp2}V_{cc}}{2L \times R_{dson}} + \frac{V_{cc}}{2L}\left(t - \frac{L_{sp1}+L_{sp2}}{2R_{dson}}\right) \tag{3}$$

The parameter C is:

$$C = \frac{I_o}{2} + \frac{L_{sp1}V_{cc} - L_{sp2}V_{cc}}{4LR_{dson}} \tag{4}$$

From equation (3) and (4), we can see the current of device 1 is also influenced by the power loop stray inductance. The more difference of L_{sp1} and L_{sp2}, there will be higher current difference between i_{ce1}(t) and i_{ce2}(t). The simulation result would be shown in next section for a more intuitive presentation.

2.2 Dynamic Current Sharing

Dynamic current sharing is influenced by device parameters and circuit parameters. Threshold voltage $V_{gs\text{-}th}$, internal gate resistance $R_{g\text{-}in}$, capacitance of device like C_{iss}, C_{rss} and C_{oss}, transconductance g_{fs} are all effective on current sharing. Stray inductance, including power loop stray inductance L_{sp} and driver loop stray inductance L_{sg}, all have direct impact on dynamic current sharing. Power loop inductance L_{sp} includes drain stray inductance L_d and source stray inductance L_s. PCB layout, device installation, even spatial position would

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cause different stray inductance in power loop and driver loop.

The stray parameters extraction method and stray parameter analysis during transient process are very important for parallel application.

2.2.1 Power Loop Stray Inductance

The switching speed during dynamic current change process is much higher than steady ON-state, including di/dt and dv/dt value. So, the inductance impact is more important even than 2.1.2 part.

The equation of power loop stray inductance's impact on dynamic process is neglected here since the principle is similar with 2.1.2.

2.2.2 Driver Stray Inductance

For paralleling devices, single high current driver IC is usually used to drive two or even more devices. For simplify, two devices are considered here for theoretical analysis.

From Fig. 1, driver stray inductance in gate loop L_{sg} has obvious impact on both 3pin and 4pin discrete. During gate voltage charging or discharging process, the driver circuit can be seen as a R-L-C resonant circuit as below.

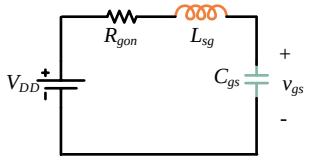


Fig. 3. Equivalent circuit of driver circuit with stray inductance during turn on

If $R_{gon} > 2\sqrt{\frac{L_{sg}}{C_{gs}}}$, initial voltage of v_{gs} is V_{goff}, and the voltage between Gate and Source v_{gs} is changed over time and can be expressed as:

$$v_{gs}(t) = A_1 \times e^{\left(-\frac{R_{gson}}{2L_{sg}} + \sqrt{\frac{R_{gson}^2}{2L_{sg}} - \frac{1}{L_{sg}C_{gs}}}\right)t} + A_2 \times e^{\left(-\frac{R_{gson}}{2L_{sg}} - \sqrt{\frac{R_{gson}^2}{2L_{sg}} - \frac{1}{L_{sg}C_{gs}}}\right)t} \quad (5)$$

The parameters A_1 and A_2 is:

$$A_1 = \frac{V_{goff} - V_{gon}}{2} \times \left(\frac{\frac{R_{gson}}{2L_{sg}}}{\sqrt{\frac{R_{gson}^2}{2L_{sg}} - \frac{1}{L_{sg}C_{gs}}}} + 1\right) \quad (6)$$

$$A_2 = \frac{V_{goff} - V_{gon}}{2} \times \left(-\frac{\frac{R_{gson}}{2L_{sg}}}{\sqrt{\frac{R_{gson}^2}{2L_{sg}} - \frac{1}{L_{sg}C_{gs}}}} + 1\right) \quad (7)$$

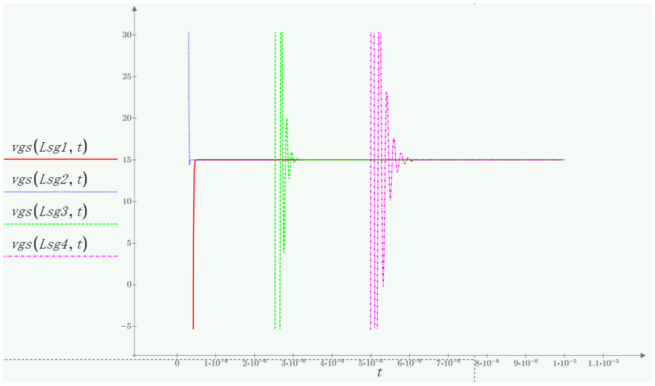


Fig. 4. Curve of gate voltage v_{gs} vs L_{sg}: L_{sg1}=2nH, L_{sg2}=20nH, L_{sg3}=200nH, L_{sg4}=400nH, R_{gon}=5ohm, C_{gs}=2.1nF

From Fig. 4, it's shown that as the L_{sg} increases, the current oscillation is getting worse and turn on delay time is getting longer. The practice results of the trends depend on specific parameters value range.

For paralleled device, switching waveform and time plot depends a lot on the driver stray inductance. different L_{sg} causes early or later turn on and turn off behavior.

2.2.3 Source Stray Inductance

Source stray inductance L_s will participate the gate driver charging and discharging process and what's more important, this inductance can couple the di_{ds}/dt from power loop to driver loop in 3pin device as shown in Fig. 1 b.

For example, when SiC MOSFET is turned on, the i_{ds} is increasing and di_{ds}/dt can build a voltage v_s on L_s, which acts as a changing DC voltage source in Fig. 5.

$$v_s(t) = L_s \frac{di_{ds}(t)}{dt} \quad (8)$$

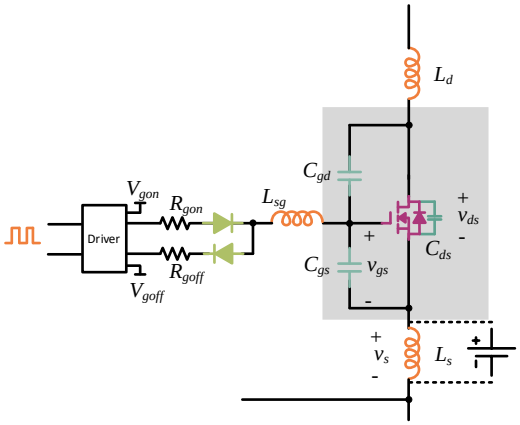


Fig. 5. Source stray inductance effect during turn on process in 3pin device

During turn on process, the voltage source v_s will decrease the gate voltage v_{gs} as equation 9. Therefore, the turn on speed is slowed down. The turn off process is opposite, and the principle is same.

$$V_{gs}(t) = V_{gon} - R_{gon} \times i_{gs}(t) - L_s \frac{di_{ds}(t)}{dt} \quad (9)$$

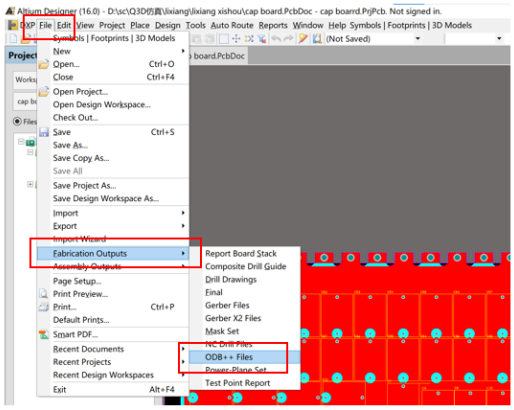
Source stray inductance's impact can be avoided in 4pin device. Since the impact is strong for high switching speed device like SiC MSOFET, it's recommended to use 4pin package.

2.2.4 Stray Parameters Extraction

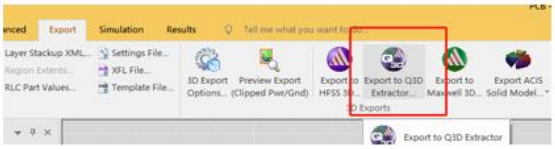
To extract the stray parameters and achieve better performance of paralleling devices, finite element simulation can be done to check the PCB layout situation after intimal design.

The common method is to use the Ansys-Q3D, Ansys is a powerful tool to offer a comprehensive software suite that spans the entire range of physics, providing access to virtually any field of engineering simulation. Before practical testing, the simulation can help engineer optimize the PCB layout and build their own design principle.

It's convenient to export an ODB++ file from Altium Designer as Fig. 6 a and import the ODB++ file through the Ansys-SIwave and then transfer to Ansys-Q3D. in Q3D, the process is just normal setup, details are not given here.



a. Export ODB++file from Altium designer



b. Transfer the PCB file to Ansys-Q3D

Fig. 6. FE simulation for PCB stray parameters extraction

3 SPICE Simulation

SPICE model can simulate the behavior of power semiconductor, help to estimate the SiC device transient performance. It's suitable to do the dynamic current sharing simulation.

From Infineon's website, SPICE model can be divided into L1(level 1), L2(level 2) and L3(level 3). L1 is the behavioral modelling approach, L2 is physics-based modelling approach and L3 is coupled electro-thermal modelling. Level 1 models provide faster computation speed and reasonable accuracy within the calibrated range. Level 2 models provide a more precise representation of the switching transients over a wide range of operating points, but these can result in slower simulation times and convergence instability. The simulation result from L1 and L2 model comparing with measurement is shown in Fig. 7 [6].

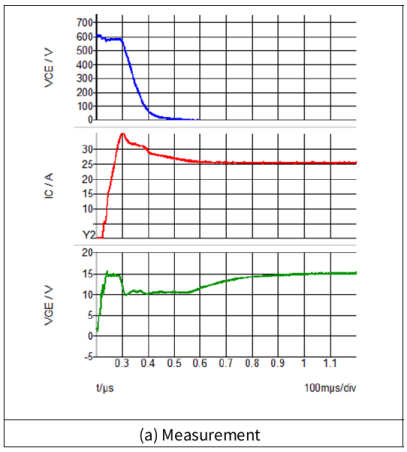


Fig. 7. L1 and L2 SPICE model simulation results

Using Infineon's IMZ120R030M1H L3 SPICE model to simulate the SiC MOSFET parallel application, double pulse electrical parameters are shown as Tab. 2 and Fig. 8.

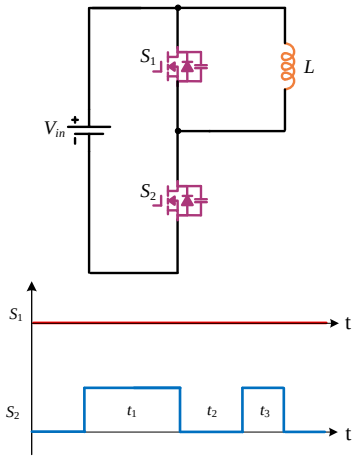
Tab. 2. double pulse test parameters

	value	**unit**
Voltage	800	V
Inductance	200	uH
t1	6.5	us
t2	3.5	us
t3	2	us

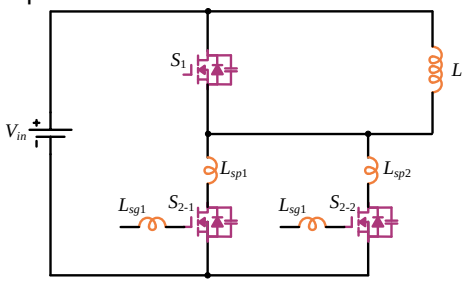
L_{sp} is the stray inductance in power loop and L_{sg} is the stray inductance in driver loop. If the symmetry of paralleled SiC MOSFET PCB layout is not perfect, stray

inductance L_{sp1}/L_{sp2} or L_{sg1}/L_{sg2} would have some difference. Since IMZ120R030M1H is 4 pin package and L_{sp} here is stand for drain stray inductance.

The L_{sp1} for $S_{2\text{-}1}$ is 5nH and L_{sp2} for $S_{2\text{-}2}$ is 10nH. L_{sp} would decrease the oscillation frequency and largen the oscillation amplitude. Excessive inductance L_{sp} causes V_{ds} drops sharply when the switches are turned on. With the increase of L_{sp} mismatch, the ON-state current sharing shows problem, unbalance current increases. From Fig. 9 a, the unbalance current is obvious, while the purple line is I_{ds} for $S_{2\text{-}1}$ and green line is I_{ds} for $S_{2\text{-}2}$. Dash line between them is the average current. L_{sg} difference would influence the gate voltage waveform as Fig. 9 b shows. The current sharing unbalance depends on the waveform performance.

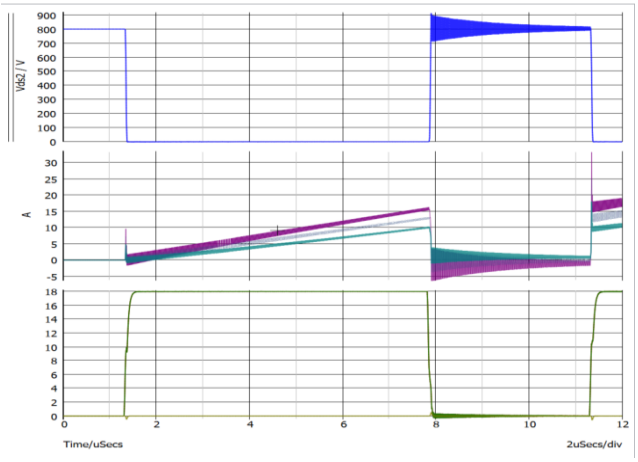


a. double pulse test

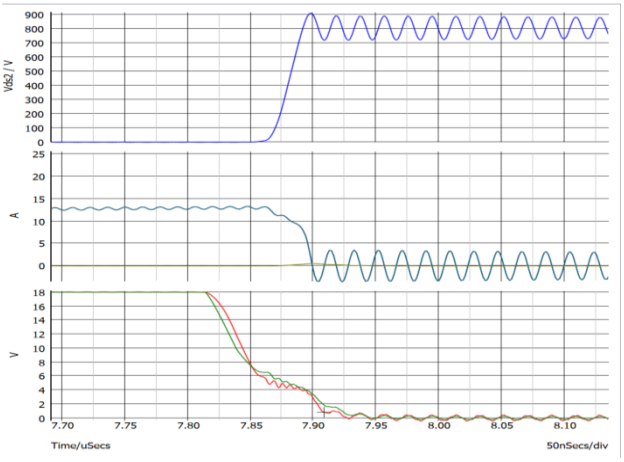


b. stray inductance in SiC MOSFET paralleling application.

Fig. 8. double pulse test description and stray inductance



a. L_{sp1}=5nH L_{sp2}=10nH



b. L_{sg1}=5nH L_{sg2}=50nH

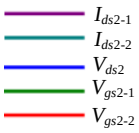


Fig. 9. Simetrix simulation results using SPICE model.

4 Driver Circuit Design

Apart from the parameter mismatch, coupling between unbalanced devices also amplify the imbalance issue. this section provides two method to limit the coupling impact from each paralleled devices.

4.1 Coupling from Stray Parameters

Single driver IC is usually used to drive two paralleled devices. As Fig. 10 shows, grey part means one SiC MOSFET device, S_1 and S_2 are paralleled together. It's hard to design the PCB layout very symmetrically in practical application, L_{sg1} is not equal to L_{sg2}. Assuming L_{sg2} is larger than L_{sg1}, S_1 would turn on first. Due to the current changing in S_1 driver loop, there is a changing voltage source on $L_{sg\text{-}c}$, which further slows down the S_2 turn on process.

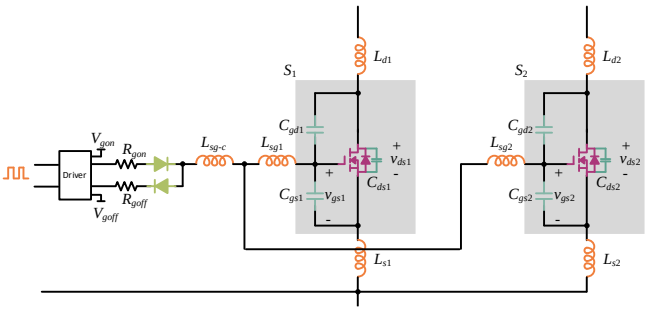


Fig. 10. Gate coupling between two paralleling SiC MOSFET

Due to the uncontrollable result of stray parameters, it's recommended to optimize PCB layout and achieve symmetric driver loop and power loop design.

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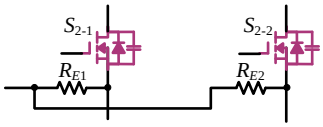
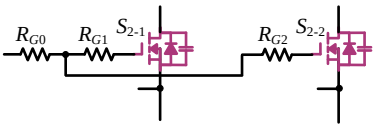
4.2 Coupling from Device Parameters

What's more, if the device's parameters are inconsistent, there would be more problem and severe oscillation conditions.

To improve the parallel performance, two method of driver circuit design is shown in Fig. 11, mutual interference can be optimized.



a. method I



b. method II

Fig. 11. two driver circuit design suggestions

4.2.1 Method I

When two 4pin SiC MOSFET are paralleled directly, the KS and S are connected separately and there will be a small source loop between L_{s1} and L_{s2} as blue loop in Fig. 12.

Due to the power loop current changing, di_{ds}/dt will build a voltage source on L_{s1}/L_{s2} as equation 10.

$$v_{s1/2}(t) = L_{s1/2}\frac{di_{ds1/2}(t)}{dt} \tag{10}$$

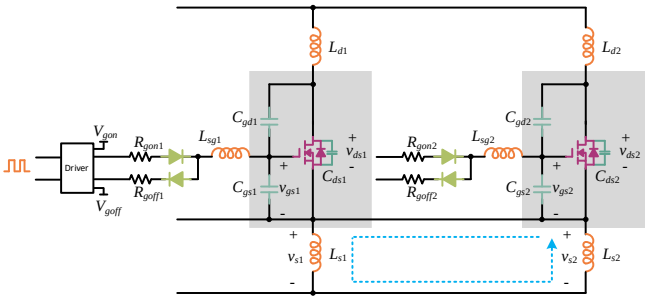


Fig. 12. Source loop induced current due to L_s

Due to the current unbalancing or device parameters mismatching like L_s, the v_{s1} would be different from v_{s2}, which would cause a voltage difference source in this loop. Due to the very small size of loop, the resistance and inductance of this loop is small and high current will gain from even a small voltage source.

Fig.11 a shows method I, which can limit the current in source loop as Fig. 13. the high current in small source loop is under control. Oscillation and EMI issue caused by the loop current can be avoided. Using method I, the gate resistor can be separated into R_g and R_E, the driver performance remains same. As a rule of thumb, the R_E/R_g ratio is between 1/5 and 1/10. In order to achieve proper current limiting function, R_E should be selected more than 0.5 Ω.

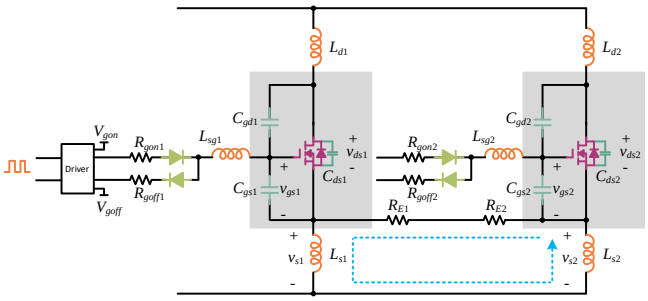
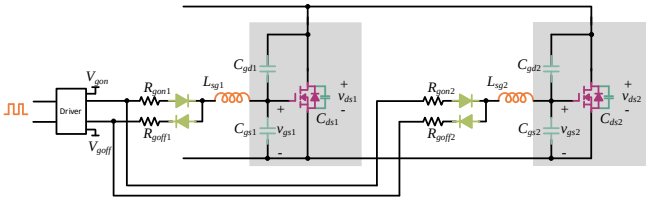


Fig. 13. R_{E1} and R_{E2} add extra resistance in source loop

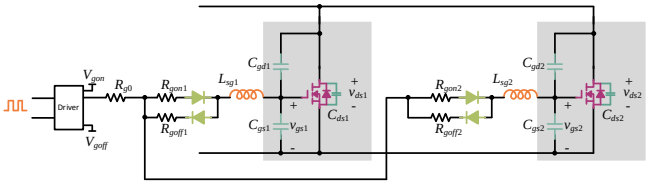
4.2.2 Method II

Inside the gate loop, turn on and turn off process can be seen as a capacitor charging and discharging process. If the gate loop stray inductance L_{sg} or gate driver resistor R_{gon} and R_{goff} are not exactly the same, or the SiC MOSFET parameters are mismatched between paralleling devices, like C_{gs}.

For example, if the C_{gs1} is larger than C_{gs2}, the traditional connection method in Fig. 14 a is shown and higher C_{gs1} will slow down S_1 and make S_1 turn on/off later.



a. The traditional gate connection for paralleled device



b. Gate loop connection for paralleled device using method II

Fig. 14. Method II for C_{gs} mismatch in paralleled devices

$$v_{gs}(t) = V_{gon} + (V_{goff} - V_{gon}) \times e^{-\frac{t}{C_{gs}R_g}} \tag{11}$$

$$i_{gs}(t) = \frac{(V_{gon} - V_{goff}) \times e^{-\frac{t}{C_{gs}R_g}}}{R_g} \tag{12}$$

Using method II as Fig. 11 b shows, higher C_{gs1} produces higher gate current as equation 11 and 12. So as in Fig. 14 b, higher gate current builds a higher voltage on R_{g0}, which will slow down both S_1 and S_2. Adding R_{g0}, the imbalance can get smaller.

5 Conclusion

Paralleling SiC MOSFET is an essential trend in today's application. Mismatch of device parameters and inequality of circuit parameters all have impact on the paralleling performance. The theoretical analysis and SPICE simulation is presented to show the circuit parameters' influence on operation. From simulation result, L_{sg} difference would change the V_{ge} waveform and L_{sp} difference causes the ON-state current difference. Two circuit design point is shown for better paralleling performance.

6 References

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