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Comprehensive Board Level Temperature Cycling Lifetime Projection of WLCSP GaN Power Devices

Siddhesh Gajare[1], Duanhui Li[1], Shengke Zhang[1]
[1] Efficient Power Conversion, United States

Corresponding author: Shengke Zhang, Shengke.Zhang@epc-co.com
Speaker: Shengke Zhang, Shengke.Zhang@epc-co.com

Abstract

Wafer level chip scale packaged (WLCSP) gallium nitride (GaN) power devices have been deployed in increasingly advanced applications that demand high board-level temperature cycling (TC) reliability. In this study, a comprehensive TC lifetime model is developed, accounting for different device sizes and varying land grid array (LGA) solder bump dimensions. COMSOL finite element analysis (FEA) simulations were conducted to model the characteristic TC lifetime based on solder fatigue wear-out mechanism. The simulated results agree with the experimental data, validating the proposed TC lifetime model.

1 Introduction

Temperature cycling (TC) lifetime with respect to the die size is typically modeled by the classic Coffin-Mansion relation, where the devices under test (DUT) are usually symmetrical in x and y directions [1]. In addition, most of the solder joints presented in those studies are ball grid array (BGA), and all the bumps have identical shape. Thus, distance-to-neutral point-based TC lifetime models are frequently adopted and proven effective [2]. However, there is a lack of TC lifetime models that account for both asymmetrical die size and varying solder bump shapes with land grid array (LGA) solder bump implementation [3]

In this work, a suite of wafer level chip scale package (WLCSP) GaN devices with different die size and bump shapes are studied under a consistent assembly and TC testing condition. TC lifetime model that includes all die sizes and bump shapes was developed and an excellent fit was empirically achieved.

After the development of the comprehensive TC lifetime model, COMSOL [4] finite element analysis (FEA) simulations were carried out based on the 3D geometry of the GaN transistors, bump dimensions, and assembly build-up. An excellent agreement was achieved between the experimental data and the simulations.

2 TC Wear-out Mechanism

The main failure mode under temperature cycling (TC) stress is identified as solder joint cracking [5,6]. The coefficient of thermal expansion (CTE) of a typical FR4 PCB is ~18 ppm/°C [7], but the CTE of a wafer level chip scale package (WLCSP) GaN device is ~4 ppm/°C [8]. The CTE of SAC305 solder connecting the GaN device and the PCB is ~23 ppm/°C [9]. The CTE mismatch between the device, solder and PCB is attributed as the fundamental wear-out mechanism responsible for the TC failures. Fig.1 illustrates the resulting stress caused by CTE mismatch during temperature cycling testing.

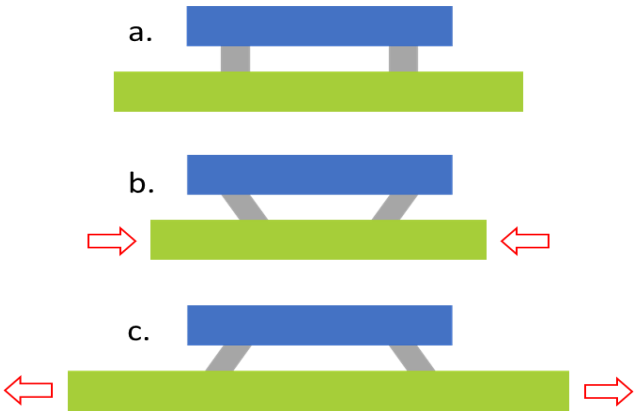

Fig. 1. (a) Neutral stress-free condition; (b) Contraction during low temperature point; (c) Expansion during high temperature point.

Fig.1 (a) shows the solder joint between the device and PCB in a neutral thermal stress position. As the temperature is lowered shown in Fig. 1 (b), the PCB which has the higher CTE value contracts more than the device, exerting compressive strain on the solder joints. Similarly, when the temperature increases in Fig. 1 (c), the PCB undergoes more expansion than the device, applying tensile strain on the solder joints.

3 Experiment

A suite of WLCSP GaN transistors with various dimensions are evaluated for temperature cycling performance, including EPC2206 [10], EPC2071 [11], EPC2069 [12], EPC2218 [13] and EPC2204 [14] shown in Fig. 2.

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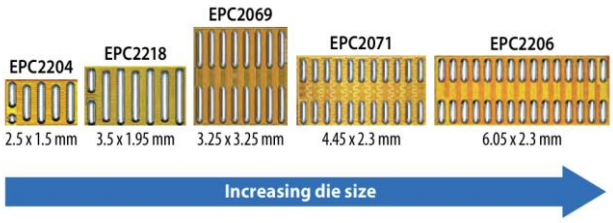

Fig. 2. Five GaN devices tested including EPC2206, EPC2071, EPC2069, EPC2218 and EPC2204.

The temperature cycling experiment was constructed to ensure that the only variables are the device dimensions and bump shape. These devices were mounted on identical test PCB boards using identical solder (SAC305). The PCB boards consist of 2-layer Cu, 1.6-mm thick, FR4 board. The standoff height i.e. the solder height of ~130 µm was maintained during the assembly process. This was verified by performing physical cross-section of the assembled boards.

The temperature cycle range was from -40°C to 125°C, with a ramp rate of 15°C/min and soak time of 10 minutes at the end points following industry standard JESD22-A104F [15]. A group of 88 devices were tested for each WLCSP device. After every temperature cycling interval of ~200 cycles, an electrical screening was performed, where an increase in $R_{DS(on)}$ exceeding datasheet limits was used to determine failures. Test-to-fail approach was adopted, where the devices are tested till 50% failure rate was achieved.

4 Results and Discussions

4.1 Weibull Analysis

The gate solder joint cracking was found to be the single failure mode throughout all failures analyzed by physical cross-sectioning and SEM inspection Fig. 3. Thus, establishing that failure of the smallest solder bump is the limiting factor for TC lifetime.

Mean-time-to-fail (MTTF) was analyzed using a two-parameter Weibull distribution for each device using maximum likelihood estimation (MLE) [16]. The resulting Weibull fits are indicated by solid lines in Fig. 4 and the Weibull characteristics are summarized in Table 1.

Device	k	λ	MTTF (cycles)
EPC2206	5.6	797	737
EPC2071	5.6	1416	1309
EPC2218	5.6	1764	1630
EPC2069	5.6	1880	1737
EPC2204	5.6	2389	2208

Table. 1. Weibull characteristics for experimental TC.

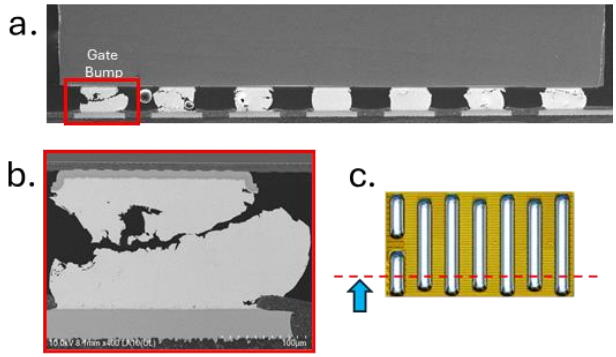

Fig. 3. (a) Cross-section of an EPC2218 TC failure; (b) worst solder joint cracking observed in corner gate bump; (c) direction of the cross-section view.

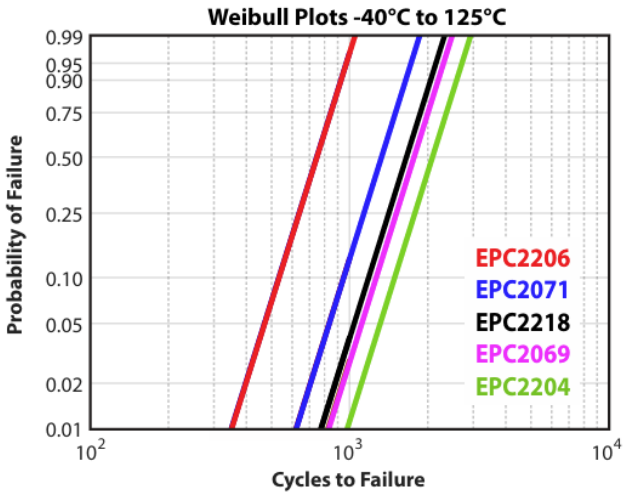

Fig. 4. Weibull distribution plot for experimental TC data.

4.2 Discussions

During TC stress, the center point of the device experiences the least stress compared to the extremities, as illustrated in Fig. 1. This is confirmed by the cross-sectional results of Fig. 3, in which the corner gate bump showed the worst solder cracking, but the center bump exhibited very little cracking. Therefore, the concept of "Maximum Distance from Neutral point (DNP^{max})" [17] is introduced in Fig. 5, where the center point is defined as the neutral point and the distance from the neutral point to the farthest solder bump is defined as DNP^{max}.

Weibull analysis in Fig. 4 shows a general trend of decreasing MTTF with increasing die size and DNP^{max}. However, it is noted that EPC2069 and EPC2071, which have similar die size of ~10 mm^2 and DNP^{max} (2.3 mm vs. 2.5 mm), showed significant difference in MTTF. Thus, some other factors other than the size or DNP^{max} must be responsible for the TC lifetime discrepancy observed.

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Failure analysis has established the gate solder joint cracking at the device corner as the limiting factor in TC. A longer gate bump indicates a longer time of failure under TC stress and vice versa. Fig. 2 shows that different devices under test (DUTs) have varying length of the gate solder bump sizes. Therefore, the corner gate bump shape should also be accounted for along with the DNP^{max} for a more accurate TC lifetime model development. As the gate bump width is similar for all devices studied, the bump length, denoted as L in Fig. 5, is the primary parameter that is included in the following discussions.

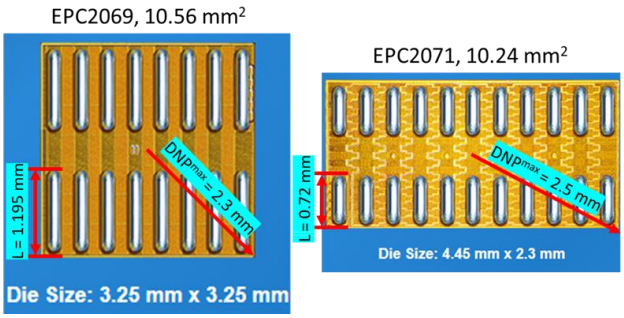

Fig. 5. Example of gate length, L and DNP^{max}.

The length of solder bump "L" is factored into DNP^{max}, and "Effective DNP (DNP^{eff})" is introduced Eq. (1).

$$\mathrm{DNP^{eff}} = \mathrm{DNP^{Max}} + \mathrm{a} \times \mathrm{L} \qquad \mathrm{Eq.\,(1)}$$

where a is a dimensionless coefficient that is determined by the best empirical fit. Eq. (2) is proposed to correlate the measured MTTF with the effective DNP (DNP^{eff}), where a good fit was found with a R^2 of 0.99, shown in Fig. 6.

$$\mathrm{MTTF} = \mathrm{A}\left(\mathrm{DNP^{eff}}\right)^{-\mathrm{n}} = \mathrm{A}(\mathrm{DNP^{Max}} + \mathrm{a} \times \mathrm{L})^{-\mathrm{n}} \qquad \mathrm{Eq.\,(2)}$$

where A is a constant, and the coefficient a is determined to be -0.65 based on the best fit, and the power exponent, n is found to be -1.4. The fitted n is consistent with literature reported values, which are typically found to be between -2 and -1 for SAC305 solder joint cracking under similar TC test conditions [18,19].

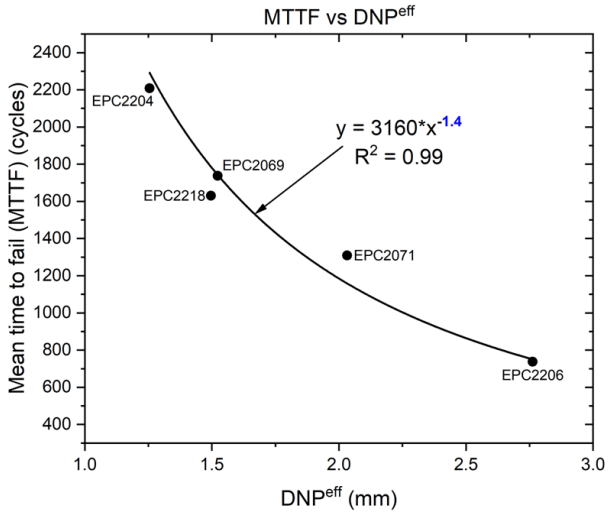

Fig. 6. Mean-Time-To-Fail with respect to effective DNP (DNP^{eff}).

5 FEA Simulations

COMSOL finite element analysis (FEA) simulations were carried out to validate the TC lifetime model presented in Eq. (2). Anand viscoplasticity model for the SAC305 solder was implemented in COMSOL, simulating solder's plasticity and creep behavior during temperature cycling [20,21]. Hence, the energy dissipation density of the solder bumps can be calculated based on the area of stress-strain hysteresis loops, denoted as ΔW. Deveraux's energy-based fatigue model was subsequently used to calculate the MTTF, quantifying when the solder joint cracking initiates and eventually propagates through the entirety of the gate bump length, L, shown in Eq. (3) [22,23].

$$\mathrm{MTTF} = \mathrm{K_1}\Delta\mathrm{W^{K_2}} + \frac{\mathrm{L}}{\mathrm{K_3}/\Delta\mathrm{W^{K_4}}} \qquad \mathrm{Eq.\,(3)}$$

where the first term, $\mathrm{K_1}\Delta\mathrm{W^{K_2}}$, represents the crack initiation lifetime and the second term, $\frac{\mathrm{L}}{\mathrm{K_3}/\Delta\mathrm{W^{K_4}}}$, models the crack growth lifetime. K_1, K_2, K_3, K_4 are fitting coefficients.

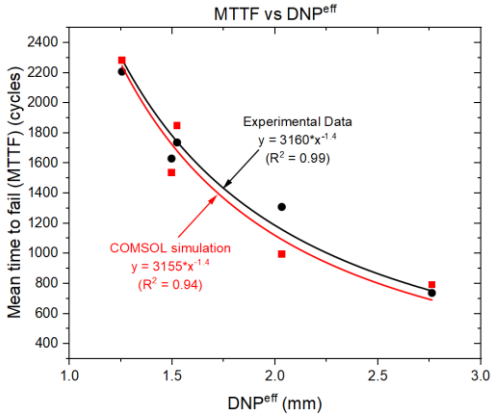

Fig. 7. Comparing MTTF from TC experimental data (black) and COMSOL FEA simulation results (red).

Fitting the COMSOL simulated MTTF of different devices yielded the red trendline in Fig. 7, where an excellent agreement was found between the simulation and experiment. It is noted that the fitted power exponent (n) based on the simulation results was also determined to be -1.4, matching precisely the one obtained from the experimental data. This further validates the effectiveness of the proposed TC lifetime model in Eq. (2) that includes device dimensions (DNP^{Max}) and the critical corner gate bump length (L).

6 Conclusions

A TC lifetime model is proposed considering the device size and corner gate bump shape,

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$$N = A \cdot \left(DNP^{eff}\right)^{-n} \quad \text{Eq. (4)}$$

where

$$DNP^{eff} = DNP^{max} - 0.65 \cdot L \quad \text{Eq. (5)}$$

In conclusion, the authors establish a comprehensive TC lifetime model, accounting for all device dimensions with varying LGA solder bumps. A good agreement between the experimental results and COMSOL FEA simulations is achieved, demonstrating the validity of the TC lifetime model.

7 References

[1] R. Ghaffarian: Accelerated thermal cycling and failure mechanisms for BGA and CSP assemblies. J. Electron. Packag. 122.4 2000, 335-340.

[2] B. Han, G. Yifan: Determination of an effective coefficient of thermal expansion of electronic packaging components: A whole-field approach. IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A 19.2 1996, 240-247.

[3] D. Barbini, M. Meilunas: Reliability of lead-free LGAs and BGAs: Effects of solder joint size, cyclic strain and microstructure. SMTA International Proceedings, Fort Worth, Texas 292 2011.

[4] COMSOL Multiphysics Reference Manual, version 6.1, COMSOL, Inc, www.comsol.com

[5] CONVERSION, EFFICIENT POWER. GaN Reliability and Lifetime Projections: Phase 15.

[6] A. Lidow, GaN Power Devices and Applications, El Segundo, CA, USA: PCP Press, 2021.

[7] J. Coonrod: Understanding when to use FR-4 or high frequency laminates. OnBoard Technology 2011, 26-30.

[8] S. Michaelides, S. Sitaraman: Die cracking and reliable die design for flip-chip assemblies. IEEE Transactions on Advanced Packaging 22.4 1999, 602-613.

[9] B. Wu, et al.: Measurement of anisotropic coefficients of thermal expansion of SAC305 solder using surface strains of single grain with arbitrary orientation. Acta Materialia 156 2018, 196-204.

[10] EPC2206 – Enhancement-mode power transistor, EPC2206 datasheet, Efficient Power Conversion

[11] EPC2071 – Enhancement-mode power transistor, EPC2071 datasheet, Efficient Power Conversion

[12] EPC2069 – Enhancement-mode power transistor, EPC2069 datasheet, Efficient Power Conversion

[13] EPC2218 – Enhancement-mode power transistor, EPC2218 datasheet, Efficient Power Conversion

[14] EPC2204 – Enhancement-mode power transistor, EPC2204 datasheet, Efficient Power Conversion

[15] JEDEC Standard: Temperature Cycling, Test Method JESD22-A104F, November 2020

[16] H. Cramér: Mathematical methods of statistics. Vol. 26. Princeton university press, 1999.

[17] J. Clech: Board, package and die thickness effects under thermal cycling conditions. Proceedings of SMTA International. 2015.

[18] R. Darveaux: Robert. Effect of assembly stiffness and solder properties on thermal cycle acceleration factors, THERMINIC 2005. TIMA Editions, 2005.

[19] T. Tee et al.: Comprehensive board-level solder joint reliability modeling and testing of QFN and PowerQFN packages, Microelectronics Reliability 43.8 2003, 1329-1338.

[20] J. Clech: The combined effect of assembly pitch and distance to neutral point on solder joint thermal cycling life, Proceedings of SMTA International.

[21] M. Motalab et al.: Determination of Anand constants for SAC solders using stress-strain or creep data, 13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems. IEEE, 2012.

[22] M. Motalab et al.: Correlation of reliability models including aging effects with thermal cycling reliability data. 2013 IEEE 63rd Electronic Components and Technology Conference. IEEE, 2013.

[23] R. Darveaux: Effect of simulation methodology on solder joint crack growth correlation and fatigue life prediction, J. Electron. Packag. 124.3 2002, 147-154.