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Optimized Switching Behavior in a 3L-ANPC-Topology with Paralleled IGBTs for Renewable Energy Applications

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Abstract

Today, converter design for renewable energy applications is getting more challenging due to various power capacity range demands coupled with increasingly limited time for the design-cycle. Focusing on the converter design, the IGBT module paralleling technology and the 3L-ANPC application technology are essential to achieve higher power capacity. For the design cycle, a qualified standard commutation loop platform would help designers simply the expansion of the power capacity of a converter set. This paper describes a design approach to support a three-level Active-Neutral-Point-Clamped (3L-ANPC) topology with paralleled IGBTss, using the SCALE-iFlex LT NTC gate driver unit from Power Intergrations. The proposed gate driver system will optimize the switching behavior in the commutation cell, which will create a platform that can be adopted for different converter sets while retaining a similar level of performance. This will reduce design requirements.

1 Introduction

There are two main approaches to increasing the power capacity in power electronics applications. Thefirst choice is to increase current capacity, which can be either achieved by adding more IGBT modules in parallel, or select an IGBT module that supports higher collector current. A new dual IGBT package is becoming popular in the market and helps designers to find a good compromise between the number of parallel modules and the need to meet increased output current per device. The other approach to realize a more powerful converter is to increase the DC-Link voltage. This could be easily realized by selecting a higher collector-emitter voltage IGBT module or by choosing the 3L-ANPC topology to achieve a higher DC-link voltage while using conventional (lower) voltage IGBT modules.

An easy-to-scale paralleling solution [1] which mainly focuses on 2L topology applications has already been introduced. It shows good paralleling behavior, including synchronization of voltage and current sharing among the IGBTs. In this paper, a systemic design approach will be introduced to show how to derive a solution for a 3L topology with paralleled IGBTs from a qualified 2L parallel design. The fundamental factor in the success of this approach is the use of a mature, scalable, reliable gate driver solution which ensures the key switching behavior is controllable even if some converter level parameters are changed - such as they type pf IGBT, number of parallel modules, and topology.

2 Switching behavior in a 2L topology with paralleled IGBTs

This section provides a quick review of the paralleling performance in a 2L topology based on an indirect gate driver solution [2].

In this solution, the main board is the Integrated master Control (IMC), the peripheral boards are plug-and-play circuits –Module Adapted gate Drivers (MAG). The IMC board receives switching signals and then sends them to the parallel MAG boards to switch each IGBT. Fig. 1 shows the electrical structure for one channel with n IGBTs in a parallel configuration.

This structure gives good freedom for the mechanical design of the power loop, which plays an essential factor in optimization of paralleling performance.

In short, the paralleled AC terminal busbar has a significant impact on static current balance. The paralleled DC gate voltage will have a significant impact on the dynamic current balance.

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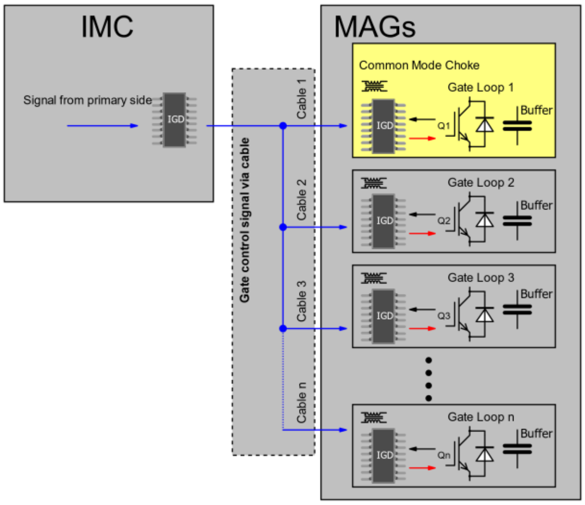

Fig. 1 An Indirect gate driver solution

After optimization of the setup, good parallel performance for 6 IGBTs in the 2L topology can be achieved.

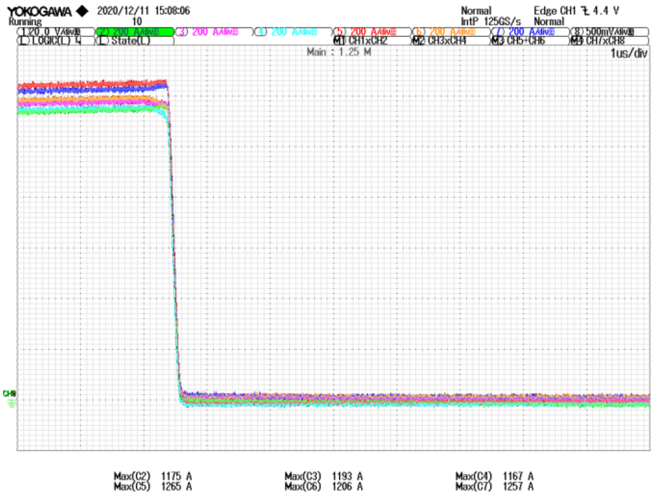

Fig. 2 Current Sharing, Turn-Off, 6 IGBTs in parallel

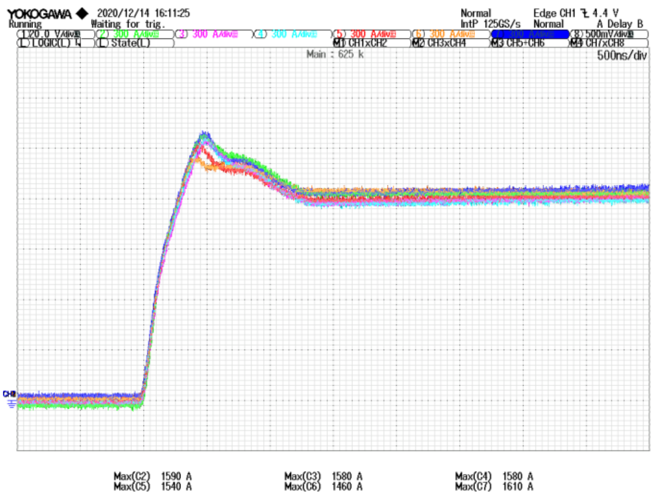

Fig. 3 Current Sharing, Turn-On, 6 IGBTs in parallel

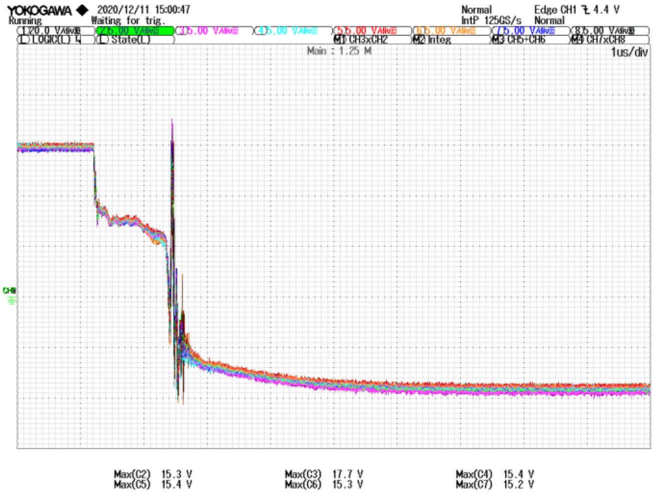

Fig. 4 Gate Voltage Comparison, 6 IGBTs in parallel.

As shown in Fig. 2 and Fig. 3, the static current balancing is less than 5%, before turn-off switching and after turn-on switching. The dynamic current sharing at both switching transitions is extremely good, as shown by the gate voltage waveform in Fig. 4.

3 Optimized switching behavior in a 3L-ANPC topology with paralleled IGBTs

This section will present a system design approach for a 3L solution with parallel IGBTs derived from the 2L topology presented in Section 2, and keeping the switching behavior at the same level with minimum changes to the design.

The switching behavior was optimized according to the new mechanical structure and the performance presented in the section 2 was achieved. The block diagram for the 2L solution is shown in Fig. 5. It consists of one IMC board and three MAG boards, since half-bridge IGBT modules are readily available.

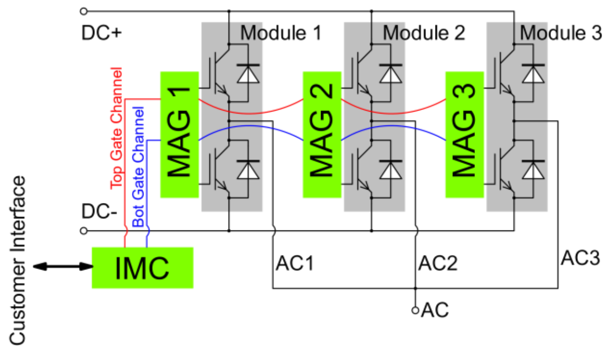

Fig. 5 A 2L topology with 3 IGBTs in parallel

The IMC provides the customer interface to the main control and provides the isolation barrier between the two channels. The MAGs supervise the switching of each half-bridge IGBT module.

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To build a 3L topology converter for renewable applications, the most practical way is to use 3 half-bridge IGBT modules for one 3L bridge with three MAGs (MAG 1-1, MAG 2-1, MAG 3-1) and three IMCs (IMC 1, IMC 2, IMC 3). In Fig. 6 the block diagram of a two-in-parallel solution in a 3L topology is shown.

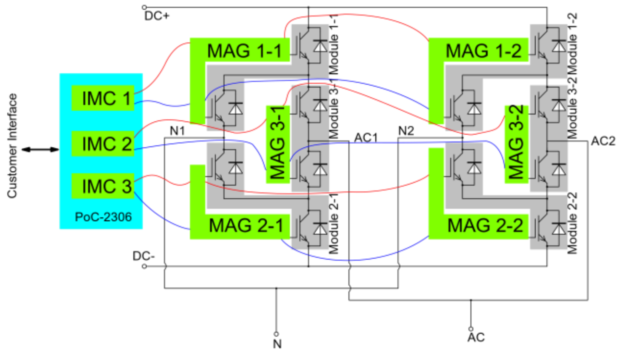

Fig. 6 A 3L topology with 2 IGBTs in parallel

In this way, it is easy for the designer to scale the power stack by employing one qualified gate driver solution for different mechanical structures. Although the different topologies will bring different design challenges, a qualified gate driver solution as a performance reference which is very important when converting a design concept into a real product.

For 3L topology in renewable energy applications, there are three major design challenges:-

1. The first one is that the commutation loop for each switch is more complex than for a 2L topology. Depending on specific control strategies, there could be 2 or commutation loops. With more paralleled IGBT, more design details need to be considered.

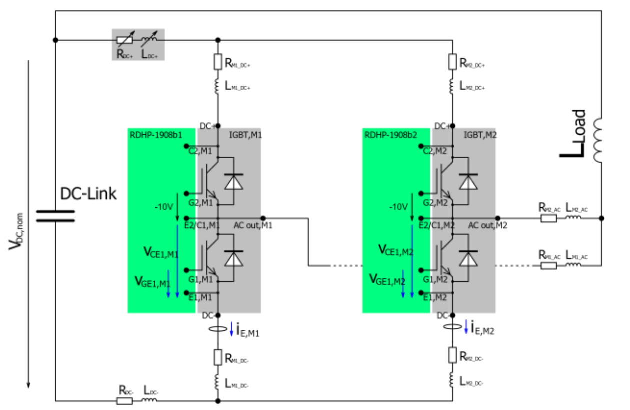

Fig. 7 Parasitic parameter for commutation loop

In order to simplify this topic, a typical equivalent circuit of 2 IGBTs in parallel is presented in Fig. 7. Each of the different mechanical structures can be converted into different combinations of parasitic inductance and parasitic resistance for each commutation loop. For each commutation loop, the basic key factors of the switching behavior are always the same and have been addressed in Section 2.

2. Communication between all six gate driver channels in a fault-tripping case. This is dependent on the control strategy. Instead of the simple interlock seen or a 2L topology, a 3L topology needs to strictly follow the turn-off sequence of IGBTs to shut down the system safely. This requires flexibility of the gate driver solution to deal with different signal processing requirements.
3. Precise temperature monitoring of the paralleled IGBTs is important for applications with high power density. Therefore the provision of an isolated IGBT temperature measurement interface is an important added feature for every power electronic converter system.

The following section will present how to perform further optimization based on the existing solution.

3.1 Overvoltage protection for 3L-ANPC topology

With respect to overvoltage spikes the most critical communication loop in a 3L topology is realized via T5 and T2 as presented in Fig. 8. This loop has the largest stray inductance in the system, here L_{stray}= 150nH. For every design, the commutation loop with the highest stray inductance has to be identified and a double pulse test, especially for the turn-off behavior, must be performed.

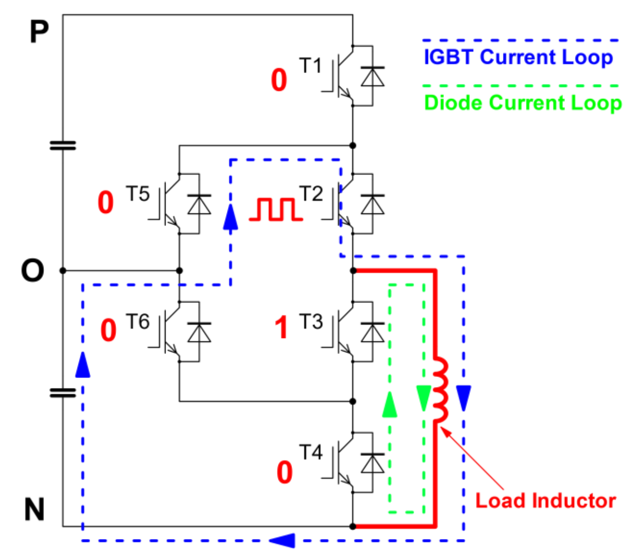

Fig. 8 Critical Commutation loops in a 3L topology

As long as one set of parameters of the gate loop for this condition is validated, the converter system will work safely for all conditions - even for parallel operation. If needed, the proposed gate driver solution will provide overvoltage-protection for each IGBT.

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A verification test has been performed for a 3L-ANPC topology using 2.3kV IGBT module, the equivalent DC link is 1800V, and the stray inductance is approximately 150nH. This is the most critical working condition for the overvoltage evaluation since it has the maximum DC link value, turn-off current, and stray inductance. The goal is to limit the $V_{CE,MAX}$ < 2200V. As shown in Fig. 9, the peak voltage of V_{CE} has been limited to 2118V. In this case, the gate resistor value was high enough to limit the overvoltage spike.

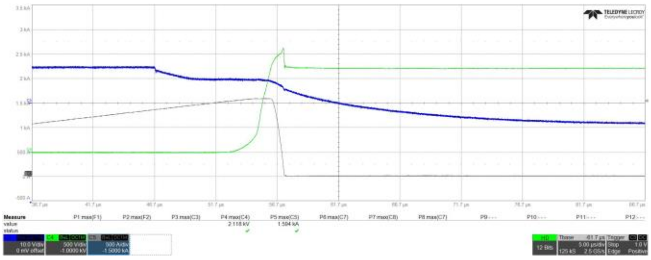

Fig. 9 T2, Turn-Off, I_c =1600A, $V_{DC\text{-}link}$=1800V, L_{stray}= 150nH

The next step is to implement this set of gate parameters, including gate resistance and overvoltage protection level, into all other MAGs, that see a similar commutation loop or for paralleled IGBTs. the overvoltage protection performance will be kept the same to ensure system safety.

Further optimization can be performed for a smaller commutation loop in the 3L topology (L_{stray}= 30nH), which has less overvoltage stress. In this case, the set of gate driver parameters can be optimized to switch faster to reduce switching losses.

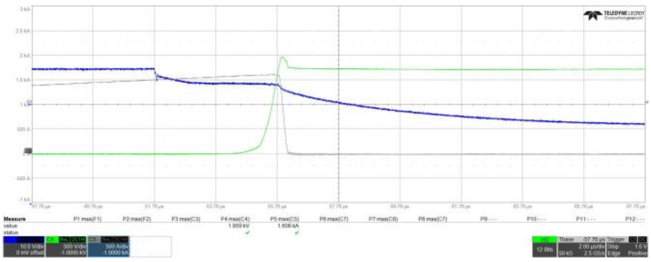

Fig. 10 T1, Turn-Off, I_c =1600A, $V_{DC\text{-}link}$=1800V, L_{stray}= 30nH

The result of this verification has been shown in Fig. 10 where overvoltage has been limited to 1959V even with a smaller gate resistance., tThe turn-off loss for 30nH is about 772mJ, which is one-third that of the losses for a 150nH loop inductance. This will provide signifcant value when the converter is deployed because this commutation loop switches more often than the inner loop.

3.2 Customized Customer Interface for 3L-ANPC Topology

In a design for a 3L topology, a common interface between the gate driver unit and the main control system is always preferred, in this case, a Proof-of-Concept design (PoC-2306) was made to provide an interface between the IMC and the main control. The blocking diagram is presented in Fig. 11.

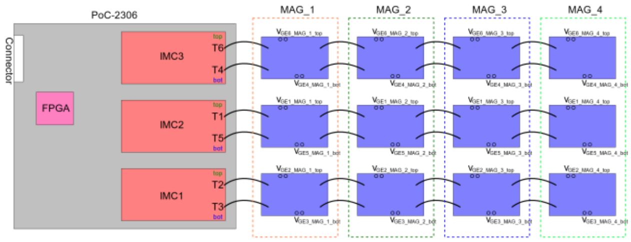

Fig. 11 Blocking diagram with PoC-2306 and SCALE-iFlex LT NTC

The PoC-2306 integrated three IMCs onto one PCB, providing six isolated gate driver channels for the 3L topology with only one primary side interface connector for receiving PWM commands and returning feedback signals. The FPGA component, positioned on the primary side will provide the necessary design freedom to adapt to different interface or communication protocols required for different projects.

On the secondary side, MAGs(in blue) can be connected according to the topology requirement. Here a 3L-ANPC topology with 3 paralleled IGBTs are represented. The cable connection among MAGs could easily adapted to match either water-cooling solution or an air-cooling solution, as long as the paralleled IGBTs stay close to each other.

A verification test was performed in a 3L-ANPC topology with 3 paralleled 1.7kV IGBTs by means of a double-pulse test, to confirm switching behavior. The equivalent DC link voltage is 1050V.

The test result is shown in Fig. 12 and Fig. 13. The dynamic current balance shows similar performance to that of 2L topology(Fig. 2 and Fig. 3).

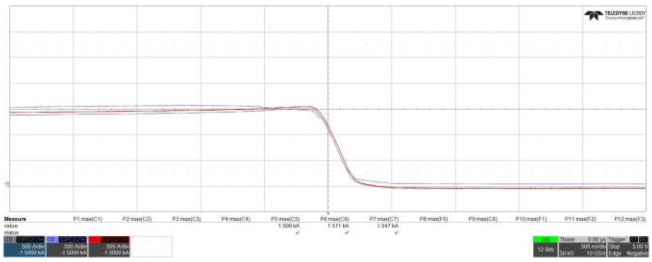

Fig. 12 Turn-off, 3 IGBTs in parallel, 3L-ANPC

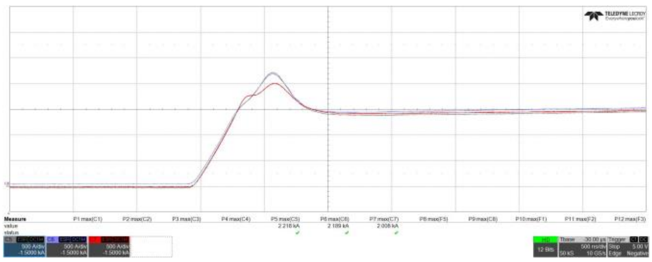

Fig. 13 Turn-on, 3 IGBTs in parallel, 3L-ANPC

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All paralleled gate voltages were tested confirm gate behavior during the same working conditions. The test results have are shown in Fig. 14 and Fig. 15. The waveforms show perfect synchronization on gate voltages, which mirrored the performance of the 2L topology.

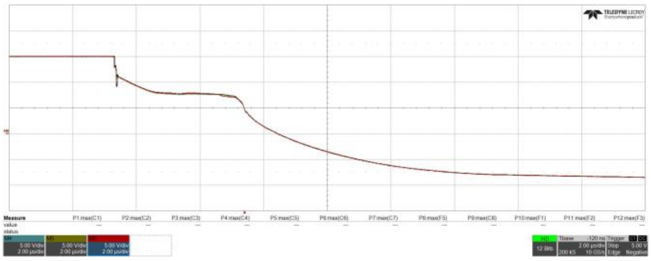

Fig. 14 Gate Voltages, Turn-off, 3 IGBTs in parallel

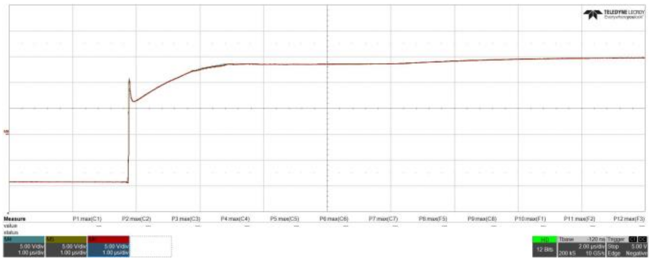

Fig. 15 Gate Voltages, Turn-on, 3 IGBTs in parallel

4 Conclusion

The paper presented a systemic design approach based on Power Integrations' SCALEiFlex-LT NTC gate driver family. The approach provides excellent flexibility to support different mechanical design control signal requirements.

Excellent switching performance for a 2L topology with 6 paralleled IGBTs has been presented, and a similar switching performance of a 3L-ANPC topology with 3 paralleled IGBTs was also verified. The result showed that the IMC+MAGs structure can optimize the switching performance for completely different machinal designs, as long as the commutation loop verification is done appropriately. This is also valid for overvoltage protection performance.

The d PoC-2306 will allow this gate driver solution to be quickly adapted to different control strategies for different applications. The most value for system designers is that parallel performance will be always the same, which will reduce the hardware qualification period significantly.

5 References

[1] H. W. K. F. Jianlong Chen, Easy-to-Scale Paralleling Solution for IGBTs in Renewable Engergy Application, 2021.

[2] Power Integrations. SCALE-iFlex LT NTC Gate Driver Family Data Sheet.

