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Research of Three-Level ANPC Converter Based on Si/SiC Hybrid Switches

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Abstract

Compared to two-level converters, Three-level converters feature higher efficiency and smoother output waveform. To further reduce cost and increase the power conversion efficiency, this paper presents a three-level Active Neutral Point Clamped converter using Si/SiC hybrid switches. It consists of four Si/SiC hybrid switches and two Si IGBT. A control method based on the optimal turn-off delay time is proposed for hybrid Si/SiC switches inside. Both the performance of the proposed ANPC converter and its control strategy is investigated and validated by experiment. Results indicate that the proposed ANPC converter exhibits a higher efficiency compared with other similar ANPC converters. The proposed ANPC converter exhibits a higher efficiency compared to all Silicon IGBT based ANPC converter, all SiC MOSFET based ANPC converter, and the four Si/SiC hybrid switches converter based on fixed turn-off delay time control method. In addition, the switches cost of the proposed converter is greatly cut down when compared to all SiC MOSFET based ANPC converter.

1 Introduction

Along with iterative technological advancements, industries such as aerospace, photovoltaic (PV), and electric vehicles are placing higher demands on power electronics systems. Taking the inverter as an example, as the power of the system continues to increase, converter losses will also be increased. The size and cost of auxiliary systems such as heat sinks and power supplies are increasing accordingly. Therefore, improving the efficiency and power density of energy conversion systems become the focus for both current and future power electronics research[1].

Three-level topologies have been widely used in industrial inverters to realize high power conversion[2]. Compared to the two-level inverter, the advantages of the three-level inverter are lower harmonic content in the output current waveform(filter can be designed smaller), reduced switching loss and reduced electromagnetic interference[3][4]. The neutral point clamped (NPC) circuit is a typical three-level converter. In this topology, the power devices need to bear only half of the input dc bus voltage[5]. However, it has the disadvantage that the power loss distribution of each power device is uneven[6][7]. In order to solve this problem, the three-level active neutral point clamped (ANPC) circuits are proposed in [8] and [9]. The clamp diodes of NPC circuit are replaced by active devices, which adds a part of redundant switching states to the circuit that can be flexibly configured to balance power device losses[10].

In order to improve the power conversion efficiency of the ANPC circuit, a converter consisting of four Si active switches and only two SiC MOSFETs is proposed in [11]. The converter has achieved 99% peak efficiency at the 45kHz switching frequency and with 650V dc bus voltage. However, the cost of SiC devices is still significantly larger than Si devices for the same rated voltage and rated current. The SiC MOSFET costs around six to eight times higher than the Si IGBT in the high current range[12]. The converter cost will be reduced by using hybrid switch consisting of a high current rated Si and a low current rated SiC compared to using a single high current rated SiC MOSFET. Besides, due to the conductivity modulation effect in Si IGBT within the Si/SiC hybrid switches, the conduction loss is also reduced at high current [13].

This paper presents a high-efficiency and low-cost three level Active Neutral Point Clamped inverter using hybrid Si/SiC switches for the high frequency switching devices and Si IGBTs for the low frequency switching devices[14]. The characteristics of Si/SiC hybrid switches are evaluated by the double-pulse testing firstly, a control method that the turn-off delay time of the Si/SiC hybrid switches varies with the load current is subsequently proposed to improve the converter efficiency.

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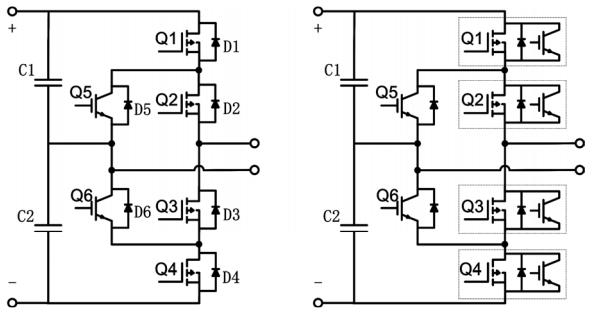
The structure of this paper is arranged as follows. In Section Ⅱ, the working principle and control strategy of ANPC converter are introduced. The third section introduce the Si/SiC hybrid devices and its control method. The Si/SiC hybrid turn-off delay time changed along with the load current control method. In Section IV, the three-level ANPC converter basis on the Si/SiC hybrid switches is built and its experimental performances are analyzed in detail. Finally, Section V summarizes this paper.

2 Proposed anpc converter and Its control strategy

2.1 Introduction of proposed topology

The topology proposed in this paper is shown in **Fig. 1**. b. Q5 and Q6 use Si IGBT for the low frequency switches in order to achieve low cost and low conduction loss. Compare to traditional hybrid ANPC converter (see **Fig. 1**. a), hybrid switches, consisting of high current rated Si IGBT and low current rated SiC MOSFET, are used for Q1-Q4 in order to reduce cost and conduction loss.



(a)Tradition topology (b) Proposed topology

Fig. 1. Topology of ANPC.

Tab. 1. Switching States of the Proposed ANPC Converter

States	Q1	Q2	Q3	Q4	Q5	Q6	Voltage
P	1	1	0	0	0	0/1	$V_{DC}/2$
OU	0	1	0	1	1	0	0
OUL	0	1	1	1	1	0	0
OL	1	0	1	0	0	1	0
N	0	0	1	1	0/1	0	$-V_{DC}/2$

Table. 1. lists the switching status and output status of ANPC converter. The ANPC converter output three different levels: *P*, *N*, *O*. There are three redundant *O* states: *OU*(upper arm carries current); *OUL*(upper and lower arm carry current); *OL*(lower arm carries current). The output status and corresponding switch states are listed in **Tab. 1**.

2.2 Control strategy

For the proposed ANPC converter, the control strategy shown in **Fig. 2**. It can be seen that the Si/SiC hybrid switches (Q1, Q2, Q3 and Q4) operate in high frequency state and bear most of the switching losses. While other Si switches (Q5 and Q6) operate in the line frequency(50Hz) state, their power losses are mainly conduction losses, and switching losses are almost negligible. Therefore, all switching events are moved to the four Si/SiC hybrid switches.

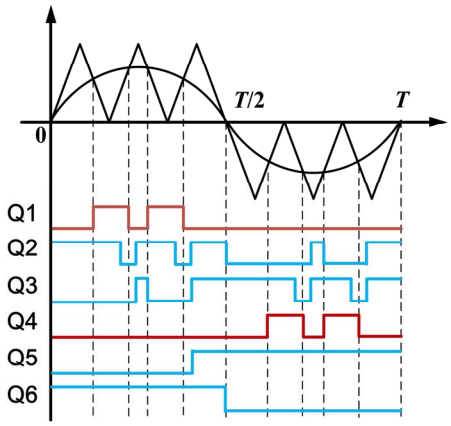


Fig. 2. Waveform of the control strategy

Using the optimal turn-off delay time control method (discussed in Section 3), the power losses of the hybrid switch are minimized, and the efficiency of the converter is thus much improved.

2.3 Commutation analysis

Taking tradition topology configuration as an example(Because the proposed topology configuration has essentially the same commutation process as the tradition configuration, except that the Si IGBT in the hybrid switches should be turned off prematurely), When the inductor current is positive, the commutation process is demonstrated in **Fig. 3** and introduced below.

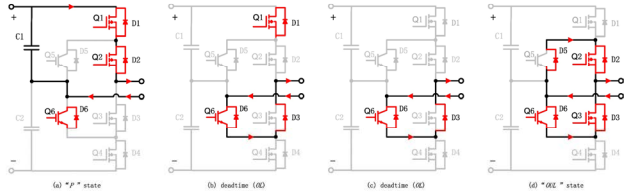


Fig. 3. The commutation process of the positive half cycle

1)During the "*P*" state, Q1, Q2 and Q6 are turned on, the load current flows through Q1 and Q2, and the output voltage is $V_{dc}/2$, as shown in **Fig. 3**. (a). Q6 is

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turned on to clamp the blocking voltage of Q3 and Q4 to $V_{dc}/2$.

2)During the dead time (*OL*) state, the Q2 is turned off firstly, forcing the main current to reverse to Q6 and D3, as shown in **Fig. 3**. (b). Then Q1 is turned off, the current distribution is unchanged.

3)During the "*OUL*" state, the Q2 and Q3 are turned on, the current flows through two parallel paths D5, Q2 and Q6, Q3, as shown in **Fig. 3**. (d).

3 The constitute of hybrid devices and the optimal turn-off delay time

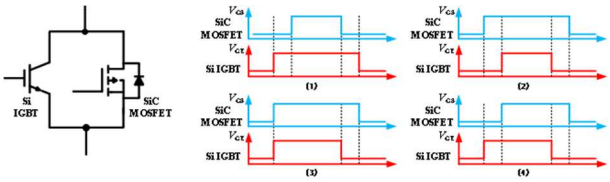
Nowadays, the price of SiC MOSFETs with high current ratings is very high. So, using high current rated Si and low current rated SiC hybrid switches to replace high current rated SiC is a feasible way. The **Tab. 2**. shows the rated voltage, rated current and price of SiC and Si devices selected for this paper. The prices are obtained from MAOZE website.

Tab. 2. main parameters and cost of Selected devices

Device	Model	Rated voltage	Rated current	Cost
Si IGBT	IXDH30N120D1	1200V	60A	¥86.32
SiC MOS	C2M0080120D	1200V	36A	¥237.82
Hybrid Si/SiC	Si:IXGH20N120A3	1200V	40A	¥62.16
	SiC:C2M0280120D	1200V	11A	¥66.23

It can be seen that using 1200V Si IGBT IXGH20N120A3 and 1200V SiC MOSFET C2M0280120D hybrid switches to replace 1200V SiC MOSFET C2M0080120D can reduce the switches cost.

The schematic diagram of the Si/SiC hybrid switches is shown in **Fig. 4**. a while the possible gate control sequence of hybrid switches is shown in **Fig. 4**. b. There are four control options. These options differ from each other in the relative turn on and turn off timing of the Si IGBT and the SiC MOSFET. The loss of hybrid switches is different when choosing different control options.[15-17]indicate that selecting (3) can achieve the lowest loss.



(a)Schematic of hybrid switches (b)Control method of hybrid switches

Fig. 4. Schematic and gate sequence control of hybrid switches

The relationship between switching loss and turn-off delay time is investigated by double-pulse circuit. The turn-off loss of hybrid switches (E_{off}) can be expressed by Eq. (1):

$$E_{\text{off}} = E_{loss\_IGBT} + E_{loss\_MOS} \quad (1)$$

Where E_{loss_IGBT} is donated as the the turn-off loss of IGBT, and E_{loss_MOS} is the turn-off loss of MOSFET. The E_{loss_IGBT} in Eq.(1) can be given by Eq.(2):

$$E_{\text{loss\_IGBT}} = \int_{T_{start\_IGBT}}^{T_{soft\_IGBT}} E_{soft\_IGBT}\,dt + \int_{T_{start\_MOS}}^{T_{off\_IGBT}} E_{res\_IGBT}\,dt \quad (2)$$

Where, E_{soft_IGBT} is the zero-voltage turn-off loss of IGBT; E_{res_IGBT} is the IGBT losses due to the carrier recombination; T_{start_IGBT} is the time point when IGBT starts to be turned off; T_{soft_IGBT} is the end time when soft turn-off of IGBT is completed; T_{statr_MOS} is the time point when MOSFET starts its turn-off process; T_{off_IGBT} represents the end time when the recombination of the access carrier inside IGBT is completed The E_{loss_MOS} can be calculated by Eq.(3):

$$E_{\text{loss\_MOS}} = \int_{T_{start\_IGBT}}^{T_{start\_MOS}} E_{con\_MOS}\,dt + \int_{T_{start\_MOS}}^{T_{off\_MOS}} E_{hard\_MOS}\,dt \quad (3)$$

Where, E_{con_MOS} is the conduction loss of MOSFET during the T_{off_delay} period; E_{hard_MOS} is the hard-switching turn-off loss of MOSFET; T_{off_MOS} is the time point when the turning off the MOSFET ends.

Figure 5 shows measured hybrid switches total turn-off current waveform, hybrid switch internal IGBT and MOSFET turn-off current waveform at a positive turn-off gate signal's delay time $T_{off\ delay}$ =0. 5μs in a double-pulse circuit with a dc-link voltage of 400 V and a load current of 15 A at room temperature.

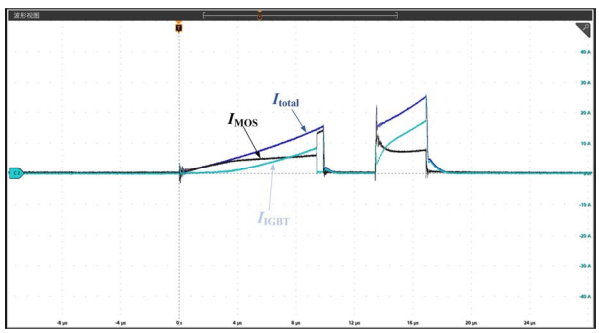


Fig. 5. Turn-off current waveforms of hybrid switch with $T_{off\ delay}$ =0. 5μs.

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Figure 6 shows the turn-off loss comparison between hybrid switch, hybrid switch internal Si IGBT, and hybrid switch internal SiC MOSFET with different turn-off delay time in a double-pulse circuit.

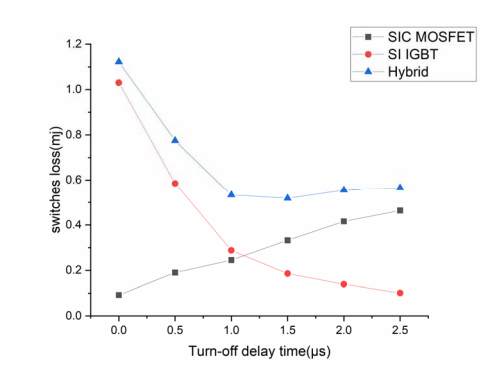

Fig. 6. The relationship between switches loss and turn-off delay time

From **Fig. 6**, it can be seen that as the increase of turn-off delay time, the energy loss of hybrid switch internal Si IGBT switch decreases, the energy loss of hybrid switches internal SiC MOSFET switch increases, and the hybrid switches loss first decreases and then increases. There exists a minimum value of the loss. The delay time corresponding to the minimum value of the total switching loss is the optimal turn-off delay time. Figure 7 shows the relationship between hybrid switches loss and turn-off delay time at varied load currents. It can be seen that the optimal delay time is different for different load currents, and the optimal delay time decreases with the increase of load current.

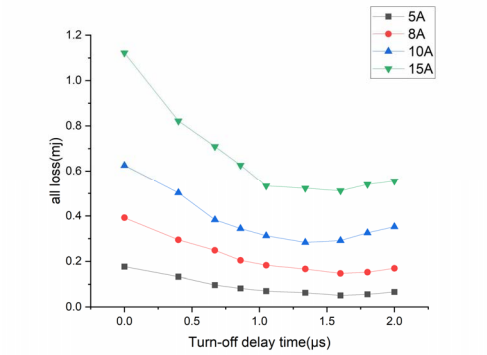

Fig. 7. The relationship between switches loss and turn-off delay time under different load current.

Following principle of achieving the lowest power loss, the optimal turn-off delay time at different load currents can be obtained. These results are shown in **Tab. 3**.

Tab. 3. The optimal turn-off delay time under different load current

Load current(A)	5	8	10	15
The optimal delay time(μs)	1. 55	1. 49	1. 46	1. 30

The curve obtained by curve fitting is also plotted in the **Fig. 8.**

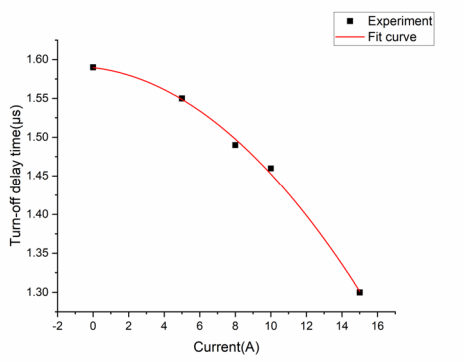

Fig. 8. Fitting curve of the optimal turn-off delay time under different load current

The calculated equation obtained from the fitting is given as follows:

$$T_{off\_delay}=1.\ 589-0.\ 0026*I-0.\ 0011*I2 \qquad (4)$$

4 Experimental Results

4.1 Building the prototype

A single-phase three-level ANPC prototype is built to verify the feasibility of the hybrid switches the optimal turn-off delay time control method for hybrid switches. The experimental platform is shown in **Fig. 9**,while the specifications of the converter adopted for this test are all listed in **Tab. 4**.

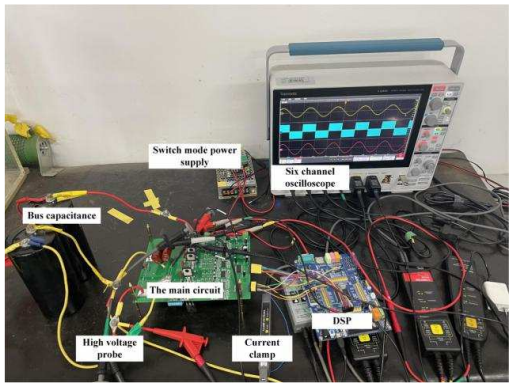

Fig. 9. Experimental platform

In order to prevent the abnormal operation of the device caused by high dv/dt, the 2ED020IL2-F2 driver chip with functions such as Miller clamp and V_{ce} over protection is used to build the driver circuit.

Tab. 4. Circuit parameters

Rated output power P_{max}	0. 91kW
DC-link voltage U_{dc}	400V
Hybrid Switches frequency	20kHz
Load Resistance R	40/3Ω
Filter inductor L	700uH
Filter capacitor C	9uF
DC capacitance C_{dc}	1000uF*2

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Figure 10 shows the voltage waveform of two bus capacitors when the converter is running normally. Figure 11. a shows the output waveform before and after the filter in the converter. Figure 11. b shows the output voltage and output current waveform. It can be seen that the voltage distribution on the bus capacitor is balanced, and the output voltage and output current of the converter are both standard power frequency sine waves, there is no obvious distortion at the zero crossing point, and the ripple is also very small. Figure 12 shows the enlarged image for driving waveform of hybrid switches at 5A and 8A.

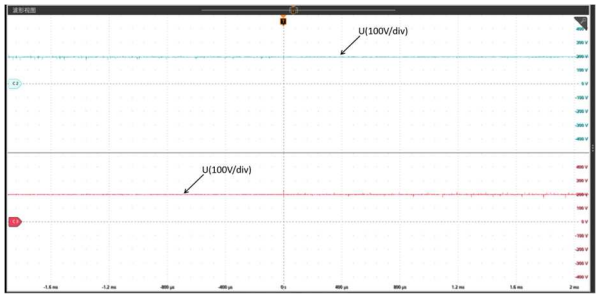
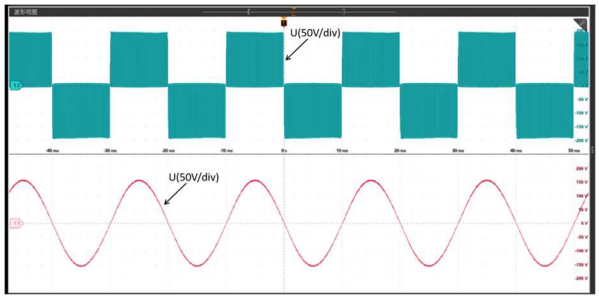
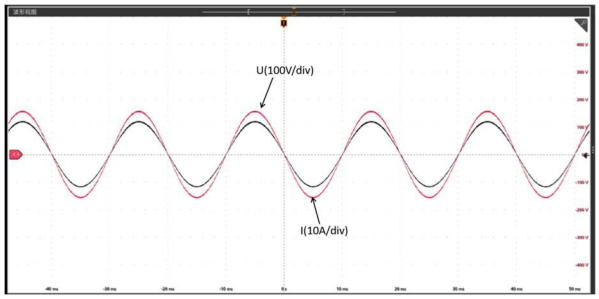


Fig. 10. Voltage waveform of bus capacitors.

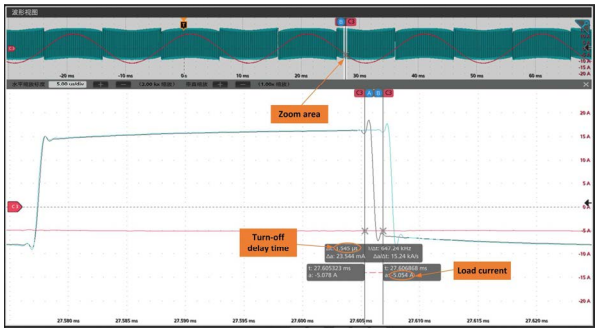


(a) Output voltage before and after filter.

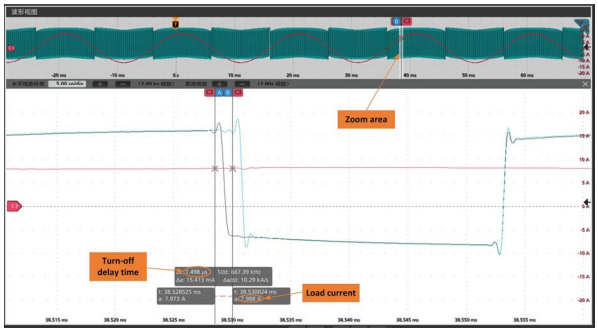


(b) Output voltage and output current at 0. 91kW

Fig. 11. Output waveform



(a) 5A



(b) 8A

Fig. 12. Driving waveform of hybrid switches

It can be seen that at a load current of 5A, the turn-off delay time is 1.545μs; at a load current of 8A, the turn-off delay time is 1.498μs,the turn-off delay time of the hybrid switches is set to be basically consistent with the fitted curve shown in **Fig. 8.**

4.2 Efficiency performance and comparison

The efficiency of converter is changed with turn-off delay time in fixed turn-off delay time control method. Figure 13 shows the relationship between turn-off delay time and efficiency for the fixed turn-off delay time control method.

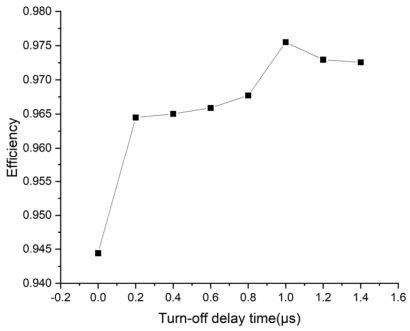


Fig. 13. Converter efficiency under different turn-off delay time

The converter achieves a maximum efficiency of 97. 55% as shown in **Fig. 13**.

The efficiency of four different configurations or control strategy of ANPC converter are compared. Include: 4 Si/SiC hybrid switches using fixed turn-off delay time control method, 4 Si/SiC hybrid switches using the optimal turn-off delay time control method, all-SiC MOSFET switches configurations and all-Si IGBT switches configurations. The selected comparison condition is shown in the **Tab. 4**.

Table. 5 lists the efficiency of four situations. From **Tab. 5**, it can be seen that the power conversion efficiency of the ANPC converter using the optimal turn-off delay time is the highest, and its efficiency is 0. 59% higher than that of using a fixed delay time method.

Tab. 5. Comparison of efficiency in four situations

Types of converters	Efficiency
Fixed turn-off delay time	97. 55%
The optimal turn-off delay time	98. 14%
All SiC MOSFET	97. 38%
All Si IGBT	95. 66%

5 Conclusions

In this paper, a Three-Level Active NPC Converter bases on hybrid switches is proposed to decrease switches cost. From the experiment results obtained from a double-pulse testing, it is found that the minimum loss of the hybrid switch can be achieved by properly setting the turn-off delay time of the hybrid switch at varied the load currents. So, the control method of hybrid switches turn-off delay time changed along with the load current is proposed. The experimental results confirm that the proposed control method can get higher power conversion efficiency than all Si IGBT converter, all SiC MOSFET converter and fixed turn-off delay time control method.

6 References

[1] D. Woldegiorgis, Y. Wu, Y. Wei and H. A. Mantooth, "A High Efficiency and Low Cost ANPC Inverter Using Hybrid Si/SiC Switches, " in IEEE Open Journal of Industry Applications, vol. 2, pp. 154-167, 2021, doi: 10.1109/OJIA.2021.3091549.

[2] H. Liu and T. Zhao, "Performance Evaluation of Si/SiC Hybrid Switch-Based Three-Level Active NPC Converter, " 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), Phoenix, AZ, USA, 2021, pp. 2058-2064, doi: 10.1109/APEC42165.2021.9487399.

[3] M. Schweizer, T. Friedli and J. W. Kolar, "Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies Against Two-Level Systems, " in IEEE Transactions on Industrial Electronics, vol. 60, no. 12, pp. 5515-5527, Dec. 2013, doi: 10.1109/TIE.2012.2233698.

[4] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications, " in IEEE Transactions on Industry Applications, vol. 41, no. 3, pp. 855-865, May-June 2005, doi: 10.1109/TIA.2005.847285.

[5] Y. Zhou, Y. Zhang, P. Du and H. Yang, "Research and Application of Hybrid ANPC Control Strategy, " 2022 IEEE 5th International Electrical and Energy Conference (CIEEC), Nangjing, China, 2022, pp. 4645-4649, doi:10.1109/CIEEC54735.2022.9846596.

[6] T. Bruckner, S. Bernet and H. Guldner, "The active NPC converter and its loss-balancing control, " in IEEE Transactions on Industrial Electronics, vol. 52, no. 3, pp. 855-868, June 2005, doi: 10.1109/TIE.2005.847586.

[7] L. Ma, T. Kerekes, P. Rodriguez, X. Jin, R. Teodorescu and M. Liserre, "A New PWM Strategy for Grid-Connected Half-Bridge Active NPC Converters With Losses Distribution Balancing Mechanism, " in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 5331-5340, Sept. 2015, doi: 10.1109/TPEL.2014.2387152.

[8] G. Zhang, Y. Yang, F. Iannuzzo, K. Li, F. Blaabjerg and H. Xu, "Loss distribution analysis of three-level active neutral-point-clamped (3L-ANPC) converter with different PWM strategies, " 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand,2016, pp. 1-6,doi: 10.1109/SPEC.2016.7846157.

[9] D. Zhang, J. He and S. Madhusoodhanan, "Three-level two-stage decoupled active NPC converter with Si IGBT and SiC MOSFET, " 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 2017, pp. 5671-5678, doi: 10.1109/ECCE.2017.8096943.

[10] Y. Deng, J. Li, K. H. Shin, T. Viitanen, M. Saeedifard and R. G. Harley, "Improved Modulation Scheme for Loss Balancing of Three-Level Active NPC Converters, " in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2521-2532, April 2017, doi: 10.1109/TPEL.2016.2573823.

[11] Q. -X. Guan et al. , "An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages, " in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8341-8352, Oct. 2018, doi: 10.1109/TPEL.2017.2784821.

[12] T. Xia, Q. Wang, H. Yang, C. Li, W. Li and X. He, "Investigation of Hybrid Three-Level Hybrid Device (Hybrid2) Active Neutral-Point-Clamped Converter, " 2022 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific), Haining, China, 2022, pp. 1-5, doi:10.1109/ITECAsiaPacific56316.2022.9941815.

[13] H. Liu, T. Zhao and X. Wu, "Efficiency Improvement Evaluation and Loss Modeling of a Hybrid Switch-Based T-NPC Inverter, " 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Raleigh, NC, USA, 2019, pp. 6-11, doi: 10.1109/WiPDA46397.2019.8998807.

[14] D. Woldegiorgis, M. M. Hossain, Y. Wei, H. Mhiesan and A. Mantooth, "A High Efficiency Three-level Active Neutral Point Clamped Inverter Using

Hybrid Si/SiC Switches, " 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 2020, pp. 284-289, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9368234.

[15] Z. Li et al., "Active Gate Delay Time Control of Si/SiC Hybrid Switch for Junction Temperature Balance Over a Wide Power Range," in IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 5354-5365, May 2020, doi: 10.1109/TPEL.2019.2942044.

[16] Z. Li, J. Wang, B. Ji and Z. J. Shen, "Power Loss Model and Device Sizing Optimization of Si/SiC Hybrid Switches," in IEEE Transactions on Power Electronics, vol. 35, no. 8, pp. 8512-8523, Aug. 2020, doi: 10.1109/TPEL.2019.2954288.

[17] H. Qin, R. Wang, Q. Xun, W. Chen and S. Xie, "Switching Time Delay Optimization for “SiC+Si” Hybrid Device in a Phase-Leg Configuration," in IEEE Access, vol. 9, pp. 37542-37556, 2021, doi: 10.1109/ACCESS.2021.3055244.