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The third generation SiC MOSFET with low on-state resistance and ultra-high reliability

Pengxiang Wang[1,2], Chengzhan Li[1,2],Yao Yao[1,2], Yafei Wang[1,2], Jieqin Ding[2], Haihui Luo[1,2]

[1] Zhuzhou CRRC Times Semiconductor Co., LTD, Tianxin High-tech Park, Shifeng District, Zhuzhou, Hunan, P.R.China

[2] State Key Laboratory of Power Semiconductor and Integration Technology, Tianxin High-tech Park, Shifeng District, Zhuzhou, Hunan, P.R.China

Corresponding author: Pengxiang Wang,wangpx1@csrzic.com

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Abstract

In this paper, we introduce the new generation of 1200V fine planar-gate SiC MOSFET,which has excellent low specific resistance of 2.7 mΩ*cm^2 by adjusting the cell structure and low switching loss by optimizing the radio of Ciss/Cgd. Furthermore, the device has also demonstrated ultra-high reliability with narrower termination compared with last generation planar-gate SiC MOSFET, as shown by no failures after stressing at +23/-10V HTGB test for 1000 hours at 175℃ or 1300V HTRB test for 1000 hours at 175℃.

1 Instruction

In recent years, SiC MOSFET (silicon carbide metal oxide semiconductor field effect transistor) has garnered significant attention and widespread adoption in the realm of new energy electric vehicles. Its outstanding performance has prompted numerous automakers to transition from traditional Si IGBT (silicon insulated gate bipolar transistors) to SiC MOSFET in order to enhance driving range and expedite charging rates.

Tesla, pioneering the industry, was the first automaker to adopt SiC MOSFET in lieu of Si IGBT. According to their report, the implementation of SiC MOSFET has led to a 6% increase in vehicle power utilization.[1] Following this trend, Nio, Geely, Xiaomi, and other prominent companies have also integrated the SiC MOSFET power module as the primary drive inverter, with the objective of bolstering the overall performance of their vehicles.[2]

The 800V new energy electric vehicle platform, incorporating 1200V SiC MOSFET chips, has emerged as a preferred choice for numerous companies across all voltage levels. This technology is being promoted to customers as a core competitive advantage of these products.[3]

To further enhance the utilization of SiC MOSFET in automotive applications, elevate the safety and acceleration capabilities of new energy electric vehicles, and mitigate electric drive losses to improve driving range, CRRC has introduced the next-generation G3 SiC MOSFET. This innovation has achieved a notable reduction in losses, approximately 35% lower than its predecessor, while fully adhering to the reliability standards mandated by the AECQ101 vehicle reliability qualification.

2 Characterization of 1200V G3 SiC MOSFET

2.1 Low specific resistance

To achieve a low specific resistance, we put a lot of effort to optimize the cell structure. Figure 1 shows the schematic cross section of G3 1.2kV SiC MOSFET and previous generation SiC MOSFET.

As shown in figure 1, the cell pitch of CRRC G3 SiC MOSFET has been reduced to 4μm, which is less than the most of commercial planar-gate SiC MOSFET. This advancement led to a significant increasing in the number of cells, thereby achieving a substantial reduction in channel resistance of approximately 14%.

Furthermore, the G3 SiC MOSFET incorporates the carrier spreading layer(CSL), which significantly improves the doping concentration at the JFET area and effectively facilitates the expansion of current in the drift area. By precisely control the CSL concentration and thickness, the breakdown voltage of the chip remains constant at 1500V, while the JFET and drift resistance are reduced by approximately 11%.

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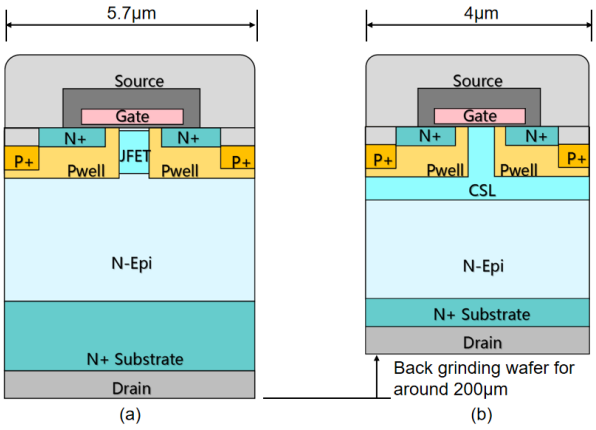

Fig. 1. Cross section of (a)previous generation SiC MOSFET and (b)new generation SiC MOSFET

Last, the application of the back grinding technique resulted in obvious reduction of the substrate thickness to 140um, thereby decreasing the substrate resistance by approximately 2mΩ.

Through those way, CRRC G3 SiC MOSFET achieved a 30% reduction in DC on-state resistance compared to previous generation, the radio of resistance is shown in figure 2.

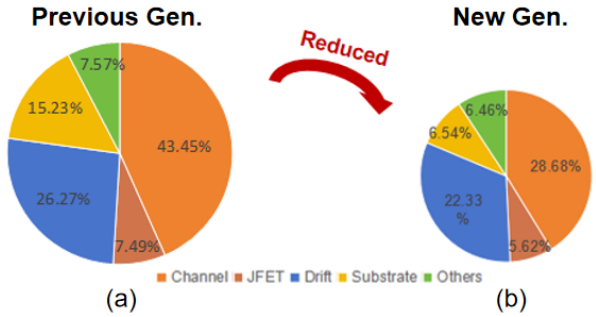

Fig. 2. Resistance ratio of (a)Previous generation SiC MOSFET and (b)CRRC new generation SiC MOSFET. The number of resistance has been normalized.

The DC on-state of 1200V G3 SiC MOSFET at 25˚C, and 175˚C is shown in figure 3. The MOSFET has +18V gate voltage (VGS) recommended DC operating maximum, and +23V overshoot maximum in dynamic switching.Maximum junction temperature(Tj) is 175˚C. From the output characteristics in Fig. 3, the DC on-state resistance is 13mΩ at the room temperature with a typical threshold voltage of 2.75V at 25°C.It means the specific resistance of this SiC MOSFET is around 2.7 mΩ*cm^2

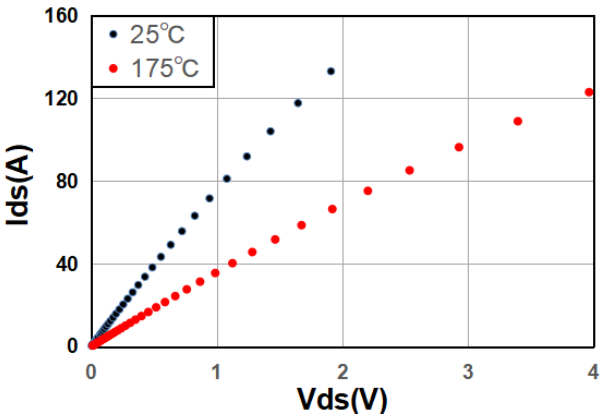

Fig. 3. DC output characteristics of 1200V 13mΩ SiC MOSFET at 25°C and 175°C temperature. The DC operating point of the gate voltage is +18V, with a typical threshold voltage of 2.75V at 25°C

2.2 Low Switching loss by suppressed crosstalk

Fast switching speed is one of the best qualities among SiC MOSFET. This makes it a common component in high-power applications. However, the SiC MOSFET bridge circuit will experience significant phase-leg crosstalk because of the greater di/dt and dv/dt during the switching operation as well as the combined influence of parasitic characteristics.

The most conventional way to reduce crosstalk is increasing the driving resistance, but this will greatly increase the switching loss of the chip.

In addition to increasing the driving resistance, we find that adjust the Ciss/Cgd in SiC MOSFET can also suppressed the crosstalk among chips. As shown in figure 4,by adjusting the Ciss/Cgd, the switching during the turn-on transient reduced around 20%.

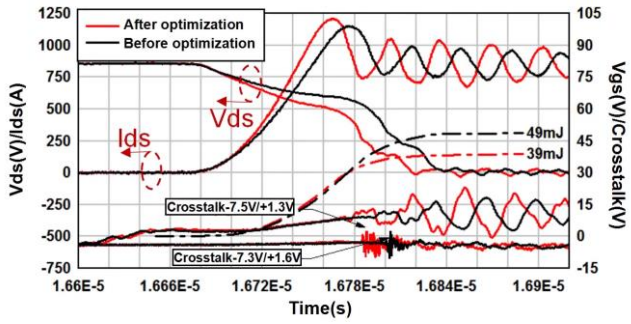

Fig. 4 Crosstalk of the G3 SiC MOSFET before/after optimization

In G3 SiC MOSFET, Ciss/Cgd is increased by adding poly layer on the gate pad, and increasing the overlap between poly and P+ doping in G3 SiC MOSFET as shown in figure 5 and figure 6. After optimization, the radio of Ciss/Cgd has reached ~850, and.the cross talk

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has also been significantly suppressed, which allows the chip to be used at a higher switching speed and significantly reduces switching loss.

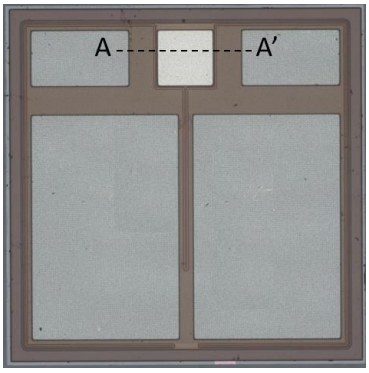

Fig. 5. The locatoin of cross section

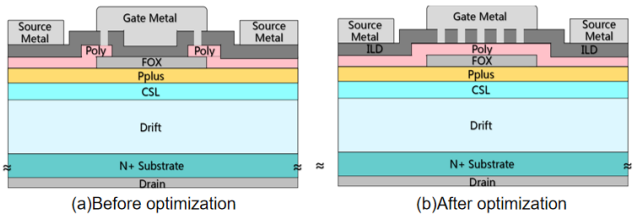

Fig. 6. Cross section of G3 SiC MOSFET from A to A'.(a)before optimization,(b)after optimization

3 Ultra high reliability of G3 SiC MOSFET

The G3 SiC MOSFET has successfully passed AEC-Q101 reliability verification,that means it could be used in automotive main drive inverters and OBC safely.

3.1 High HTRB and HTGB reliability

In this paper, we enhance the stability of the space between guard ring by introducing auxiliary guard rings as hown in figure 7. And improve doping concentration at the surface of terminal to cut off channel caused by interface state, resulting in a significant improvement in HTRB capability. Above all, the terminal of G3 SiC MOSFET is much smaller than previous generation by optimizing the space and width of guard rings, the efficiency of terminal has improved around 20%. It means the resistance of chip could be further reduced. Currently, the G3 SiC MOSFET chip has passed a 1000-hour 1300V 175°C HTRB test, demonstrating long-term stable source-drain blocking capability.

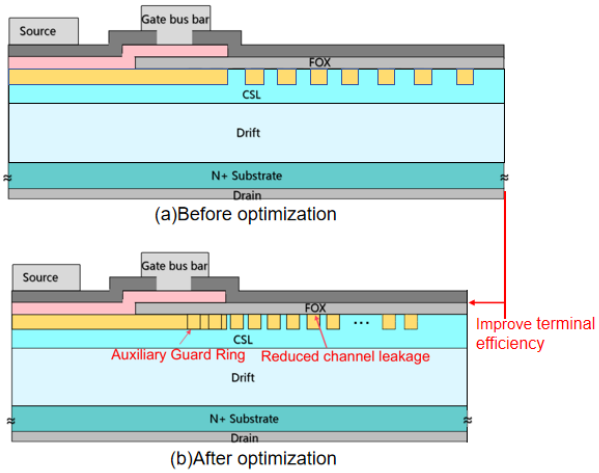

Fig.7 Terminal structure of G3 SiC MOSFET (a)before/(b)after optimization

The threshold voltage shift, after +23/-10V HTGB, is shown in the figure 8. By controlling the density of interface states at the channel, the stability of gate oxygen is greatly improved, the G3 SiC MOSFET has passed +23/-10V HTGB test, which allows the chip can be used faster than before,futher reduce the switching loss of SiC MOSFET.

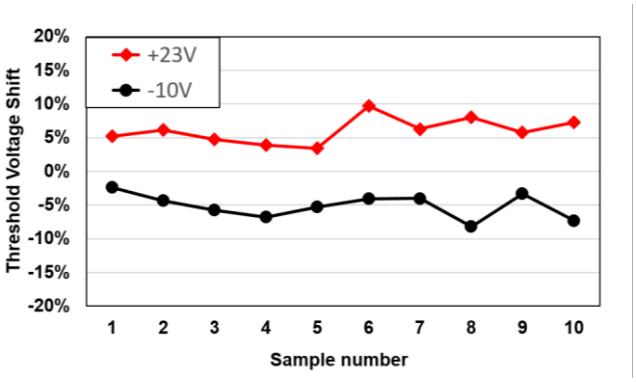

Fig.8 Threshold-Voltage shift of G3 SiC MOSFET after stressing of +23/-10V HTGB test for 1000 hours at 175℃

4 Conclusion

The new generation of 1200V SiC MOSFET reaches specific resistance of 2.7 mΩ*cm^2 due to smaller cell pitch, thinner substrate thickness and current spreading layer technology. Thus we have also adjust the radio of Ciss/Cgd to suppress the crosstalk of the chips, which has reduced the switching loss of the device.Those works make the G3 SiC MOSFET could be used in automotive main drive inverter or photovoltaic inverter more effectively,

Above all, The chip also meets the reliability requirements of AEC-Q101, which means it can be used in new energy electric vehicle.

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Furthermore, the chip has passed the +23/-10V HTGB test for 1000 hours at 175℃ and 1300V HTRB test for 1000 hours at 175℃, which allows the G3 SiC MOSFET can be used faster to reduce the switching loss, increase the cruising range of automobiles.

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