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Comparisons of Board-Side and Back-side Thermal Management Techniques for eGAN® FETs in a Half-Bridge Configuration.

Adolfo R. Herrera[1], Michael A. de Rooij[1]
[1] Efficient Power Conversion, U.S.A.

Corresponding author: Adolfo R. Herrera, adolfo.herrera@epc-co.com
Speaker: Adolfo R. Herrera, adolfo.herrera@epc-co.com

Abstract

GaN FET characteristics offer converter high power-density capabilities with fast switching and low on-resistance, however, they are physically smaller, and come in alternative package offerings, than their silicon counterparts. When employed in applications the result is higher heat flux density that limits the power processing capabilities of the converters. Various thermal strategies are necessary to leverage the potential of GaN FETs by lowering the thermal resistances both in a printed circuit board (PCB) and through external heat sinking. Configuration options using thermal vias, heat spreaders, heatsinks on either side of a PCB, and high-performance thermal interface materials (TIM) are investigated. Implementing these techniques can reduce thermal resistance from the junction to ambient ($R_{\theta JA}$) by 30% without a heatsink and by over 60% with a heatsink.

1 Introduction

Enhancement-mode gallium nitride eGaN FETs offer high power-density capabilities with ultra-fast switching and low on-resistance, all in a compact form factor [1]. However, the achievable power levels are limited by the thermal system capability in conjunction with high heat-flux densities. If not managed properly, the generated heat can result in excessive self-heating and elevated temperatures that compromise reliability and performance. Thermal techniques that manage the temperatures of the heat-generating parts on the board are required to keep operating temperatures within safe levels. Design choices within the structure of the PCB itself as well as external components such as heatsinks and thermal interface materials (TIM) can all be leveraged to keep device temperatures low.

Power electronic devices in operation dissipate energy causing self-heating. The heat generated flows from the heat source, referred to as the device junction, towards cooler bodies through two main parallel paths – to the printed circuit board (PCB) and to the case or back-side of the device. The heat flux for each path is a result of the temperature difference and the thermal resistances encountered along the path, as shown in Eq. (1).

$$R_{\theta JX} = \frac{T_J - T_X}{P_V} \quad (1)$$

Where $R_{\theta JX}$ is the thermal resistance from the junction to a reference location X; T_J is the device junction temperature in steady state conditions; T_X is the temperature at reference location X; and P is the power dissipated in the device. The reference location commonly refers to the ambient environment (A), the board (B), or the back-side of the device (C). $R_{\theta JA}$ is the combined equivalent resistance from the junction to ambient, which includes the thermal resistance of the whole system encompassing the various paths. The thermal resistances that are not intrinsic to the device junction, are generally the ones that can be improved on and are calculated with a general equation, instead using two different reference points that approximate the heat path. Some of these thermal resistances will be introduced in the following section.

This paper details thermal management guidelines when designing high power applications with GaN devices by using elements of the PCB to reduce thermal resistance both with and without heatsinking. Different PCB parameters are simulated in CFD to determine the effect on thermal resistance; the PCB parameters were then experimentally tested to validate the CFD simulation results. A few heatsink attachment variations are also introduced, evaluated in CFD simulation, and experimentally verified to identify effective ways of cooling devices in high power applications.

2 Baseline and Methods

2.1 Thermal Resistance Network

Modeling the heat transfer characteristics of a PCB is complicated as conduction, convection, and radiation all combine thus affecting the various thermal paths on

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the board and any devices. However, because radiation is intrinsically the least effective thermal path and can only be realistically affected by significantly increasing the effective surface area of the PCB with a heatsink, only conduction and convection are modeled in the PCB thermal resistance network. The first thermal resistance network will be modeled for two FETs in a half-bridge configuration with no heatsink attached. This network approximates the thermal path from the device junction through the PCB and to the surrounding environment. The second thermal resistance network will build upon the first by attaching a heatsink to the bottom of the board, and the final network will instead attach the heatsink to the back side of the devices.

The PCB-only cooling resistance network is shown in Fig. 1. In a cooling application with no heatsink attached, the heat dissipated from the transistor to ambient is minimal due to the small area such as in EPC2619, EPC2057, and EPC2218 [2, 3, 4]. As such, the main heat dissipation path from the transistor is through the PCB [5]. Once heat flows through the device to the board ($R_{\theta JB}$), heat can then spread transversely through the top layer and transfer to ambient; represented by $R_{PCBT\text{-}A}$. The heat can also flow laterally through the PCB with thermal resistance $R_{Z,PCB}$ before transferring from the bottom layer to ambient with $R_{PCBB\text{-}A}$. $R_{12,}$ for both the top and bottom of the board, represents the coupling thermal resistance between the two devices.

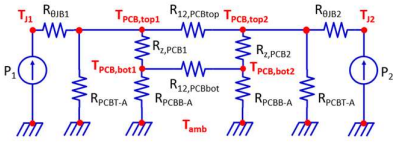

Fig. 1 Simplified PCB only thermal resistance network for a half-bridge without heatsink attached.

Figure 2 updates the thermal network of Figure 1 when adding a heatsink to the bottom of the PCB. The thermal resistance network is almost identical to that of the PCB-only cooling network, with added heat path from the bottom layer to ambient through $R_{PCBB\text{-}A}$. In this case heat flux now will transfer through the heatsink. R_{TIM} is the thermal resistance through the TIM that lies between the board and the heatsink. $R_{\theta SA}$ is the thermal resistance of the heatsink.

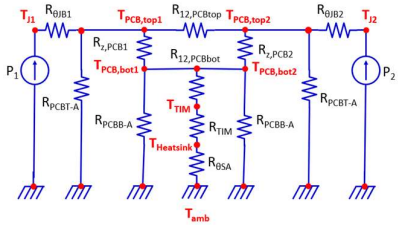

Fig. 2 Simplified thermal resistance network for a half-bridge configuration with a heatsink attached to the bottom side of the PCB.

The final cooling configuration that is presented in this paper attaches a heatsink to the back-side of the devices. The thermal resistance network is shown in Fig. 3. $R_{\theta JC}$ (thermal resistance from the junction of the back-side case) is now included in this network as there will be significant heat flow through the case of the device to the heatsink. In this case, R_{TIM} is specific to the TIM applied on top of the transistors while $R_{G.F.}$ represents any contact of the TIM between the board, the side walls of the transistors, and the heatsink.

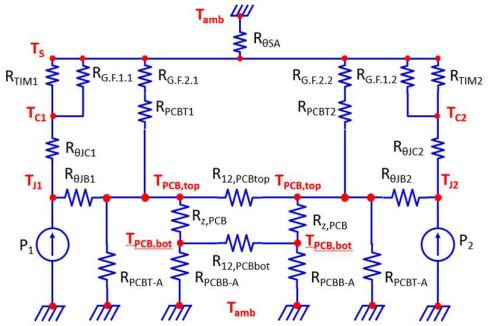

Fig. 3 Simplified thermal resistance network for a half-bridge with a heatsink attached to the back-side of the transistors.

2.2 Typical Board Design Baseline

The thermal management strategies for PCB-only cooling, bottom-side heatsink cooling, and back-side heatsink cooling in the following sections relies on a baseline standard 50 mm x 50 mm PCB of 4-layers. The PCB-only cooling case heavily depends on the copper mass and design traces within the board. The copper thicknesses used for the conductive layers in the board will vary between 0.5 oz, 1 oz, 1.5 oz, 2 oz, and 3 oz. Note that 3 oz copper is only studied in simulation due to PCB manufacturing cost and feature size manufacturability limitations. The use of vias will range from under the device, adjacent to the device to very few or none at all. Increasing the capability for heat spreading by thoughtfully designing the copper in the PCB should lower overall thermal resistance for low power applications.

The bottom-side heatsink approach will evaluate different heatsinks with base areas of 3 cm^2, 12 cm^2, and 25 cm^2 that are attached to the bottom of the PCB and their effect on overall thermal resistance. There will also be a discussion on TIM selection for this thermal solution approach. Bottom-side heatsinking should reduce the thermal resistance more than PCB cooling does as the added surface area allows for more convection and radiation to occur in the full system.

The back-side heatsink approach will evaluate the efficacy of attaching the heatsink directly to the back of the devices and evaluate if there is improvement over the bottom-side heatsink approach. The heatsink used for the back-side cooling evaluation is an aluminium

heatsink with a 10 cm^2 base area. This approach is expected to deliver even further improvements in overall thermal resistance over the bottom-side heatsinking approach due to the more direct thermal path from the junction to the heatsink.

2.3 FEA Approach

In this study, different PCB and heatsink designs were simulated in 6SigmaET version 16.3, also known as CelsiusEC [6]. 6SigmaET is a finite element analysis software specifically designed for simulations of thermal performance in electronic systems. The simulations are set up so that the heat-generating FETs are each given a power dissipation number in watts so that a steady state temperature can be reached. This temperature along with the given power dissipation numbers are plugged into Eq. (1) to obtain $R_{\theta JA}$.

3 Effects of PCB Design Parameters

3.1 PCB Cooling Motivation

There are several ways to improve the conduction heat paths within the PCB before adding external components to improve cooling. These improvements to the PCB may still even provide benefits for lowering thermal resistance when additional cooling methods such as heatsinks and forced air convection are considered. The PCB design parameters that will be examined include the board area, copper layer thickness, thermal vias, and optimized component layout.

3.2 Board Area

The effectiveness of cooling parts on a PCB depends on the area of the board. To increase cooling, it is important to increase that effective area of heat spreading away from the parts and into the environment. Increasing the area of the PCB decreases the total thermal resistance from device junction to ambient, but the magnitude of that decrease is less impactful as the board continues to increase in size as shown in Fig. 4. This is because in a case where the power dissipation and size of the parts is kept the same then the extra area in the board that is further away from these parts does not have much heat spread all the way to those fringes, making the actual effective area of convection between the PCB and the environment smaller than the total area of the PCB. The very thin copper layers are responsible for the bulk of the heat conduction away from the parts, and there is very limited copper volume in these layers directly surrounding the parts to make a large enough impact to the outer edges of a large PCB.

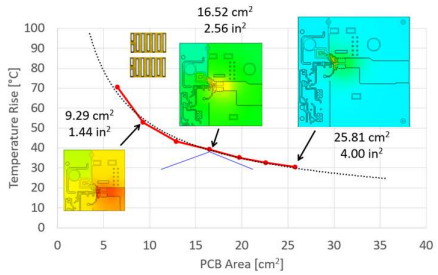

Fig. 4 Effect of board size on temperature rise.

3.3 Copper Thickness

The most important structure of a PCB with a low thermally conductivity dielectric is the copper. The top layer is particularly important as it is the primary heat flux exchange mechanism on the board itself [7]. Designing thicker copper traces can help maximize the heat spreading benefits of the relatively thin copper layers in the PCB. Table 1 shows the simulation results for different copper layer thicknesses in a 4-layer PCB. Copper layer thicknesses exceeding 2 oz can challenge manufacturability due to etching of fine features required for the GaN devices, while also yielding diminishing returns to reducing maximum temperature. The buried layers also have little impact on convection to the ambient environment and act as very small heatsinking components.

Table 1 Temperature rise for different copper layer thicknesses under two cooling conditions using baseline PCB.

Thickness	*ΔT Still Air [°C]*	*ΔT 400 LFM [°C]*
1oz Cu	64	42
1.5oz Cu	57 (-13%)	39.5 (-6%)
2oz Cu	53 (-21%)	37.5 (-12%)
3oz Cu	51 (-25%)	35.5 (-18%)

3.4 Vias

As previously mentioned, the two outer layers are the most impactful layers for reducing temperatures as they have the largest area in contact with the ambient environment. However, it is difficult for heat to spread away from the parts to the bottom layer of the PCB through the much thicker and less thermally conductive dielectric layers. To compensate for this, thermal vias can be implemented in the PCB to act as “heat pipes” to transfer the heat from the top layer to the bottom layer of the board. In cases where the vias are in the bump under the device, IPC4761 Type VII vias must be used. These vias are tended over on both sides of the board, contain a non-conductive fill, and are plated over to seal them [8]. The non-conductive fill helps to reduce the effects of thermal cycling on the reliability of the board by having a better match between the coefficient of thermal

expansion (CTE) of the via fill and the FR4 in the board [9]. The thin copper plating around the vias is sufficient to transfer heat. In cases where the vias are adjacent to devices, the vias only require tenting to prevent solder wicking; this means that the Type VII vias in pad are not necessary, allowing for a less expensive approach. Figure 5 shows the results of including these types of vias near the devices, with reductions in thermal resistance as high as 30%.

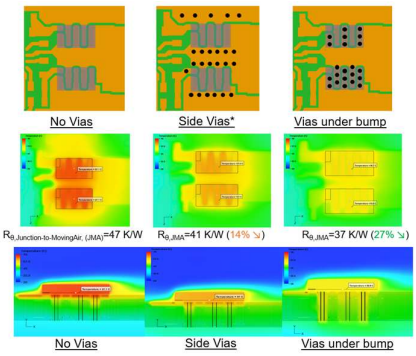

Fig. 5 Via location configurations and their effect on thermal resistance.

3.5 Device separation

Typical GaN FET layouts [10, 11] require close proximity between the two devices in a half bridge configuration to ensure lowest loop inductance [12]. Heat-generating components on a PCB heat each other when placed in proximity with each other. Due to this, two FETs in a half-bridge configuration will co-exchange heat flux which increases $R_{\theta JA}$ for each device. To approximate the effects of co-heating between two heat sources, a simple superposition can be used to analyze the combined effects of their temperature rise [13]. Reconfiguring the layout by separating the devices apart and relocating the critical bus capacitor to between the devices can reduce the effect of co-heating which in turn reduces $R_{\theta JA}$ without any penalty in loop inductance [11]. Figure 6 shows that separating the parts can reduce $R_{\theta JA}$ by about 5% for both FETs.

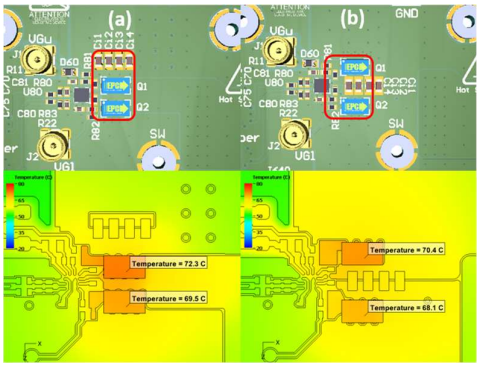

Fig. 6 FEA simulation temperature results for (a) adjacent bus capacitor temperatures, (b) center bus capacitor temperatures.

3.6 Combined Thermal Effectiveness

Combining all these PCB cooling techniques results in about a 35% decrease in $R_{\theta JA}$ with little to no additional cost in manufacturing the PCB as shown in Fig. 7 [7]. These techniques will be built upon in the following section when a heatsink is added to the design for a complete thermal solution.

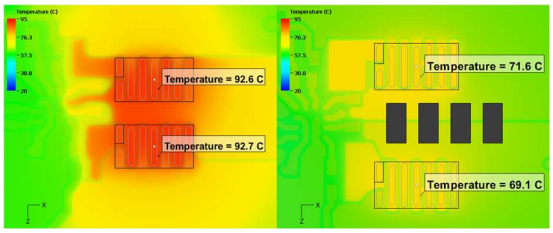

Fig. 7 (a): Result with no PCB only thermal techniques used. (b): Result with all possible thermal techniques used

4 Effects of Bottom-side Cooling

4.1 Bottom-side Heatsinking Motivation

Bottom-side cooling involves attaching a large metal, normally aluminum but potentially copper, heatsink to the bottom layer of the PCB. This approach to cooling the parts can be favored for several reasons including simplicity of attachment when there are little to no components on the bottom side of the board and the necessity for external cooling components when reaching higher powers for specific applications. Attaching a heatsink to the bottom of the PCB does not induce mechanical stress on the devices. Adding a heatsink increases the effective area of both convection and radiation on the full thermal system, allowing for even further reductions in thermal resistance beyond what is possible on the PCB alone.

4.2 Heatsink Design Considerations

There are different design considerations to be evaluated when using a heatsink. For the purposes of this investigation, an extruded fin aluminium heatsink will be studied. The heatsink fin design must be considered as different fin shapes and densities have very different performance results depending on the environment they are surrounded in. In a natural convection environment, heatsinks with sparser fin patterns will outperform heatsinks with dense fin patterns as the thermal resistance to ambient is strongly related to the air flow generated by the thermal gradient along the length of each fin. Having dense fins may trap heat between each fin, resulting in worse performance [14]. The increased surface area of a dense fin pattern will be more desirable in forced convection cooling systems as there will be little to no heat trapping effect. The following sim-

ulation studies consider a bottom-side heatsink in natural convection with tall, thick, extruded fins in a sparse pattern.

4.3 TIM Design Considerations

A heatsink cannot simply be attached to a PCB without any interface between them. As such, thermal interface materials (TIM) with good thermal conductivity are used to mate the thermal surfaces of the board or device and the heatsink. Different considerations need to be made with TIM selection such as low thermal resistance, electrical isolation, and mechanical compliance [1]. Decreasing the thickness of the TIM, whether it is a pad or a gel, often increases the performance thermally as shown in Fig. 8 but can result in tradeoffs with mechanical force exerted on the device and manufacturing tolerances.

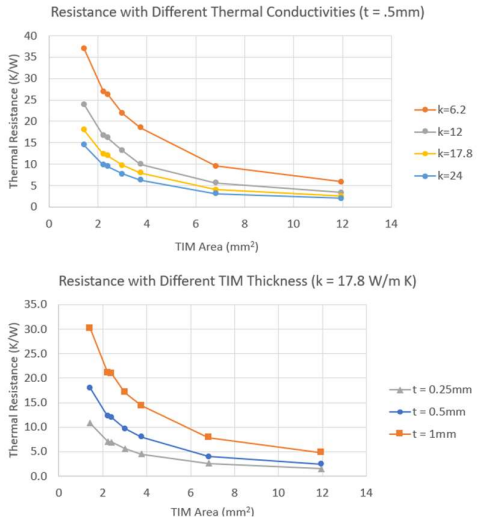

Fig. 8 Effect of TIM thickness, area, and thermal conductivity on the thermal resistance from junction to heatsink ($R_{\theta JSA}$).

Figure 8 also shows that increasing the TIM area or thermal conductivity will lower thermal resistance but that may come with significant cost tradeoffs. The thermal resistances shown in Fig. 8 were obtained via FEA simulation and are the thermal resistance between the heat source of 1 W and the very bottom of an ideal cold plate with a TIM in between. Much like with PCB area, there are diminishing returns with having too much TIM area between the mating surfaces; in addition, TIM thermal conductivity makes little difference in the thermal resistance between the mating surfaces when TIM area is large enough.

4.4 Simulation Results

Three different bottom-side heatsinks were designed to evaluate the total thermal resistance to ambient in comparison to the PCB cooling best-case scenario. Heatsinks with areas of 3, 12, and 25 cm^2 were centered around the eGaN FETs on the bottom side of the PCB with a thermal conductivity (κ) of 6 W/m·K TIM with 1 mm thickness between them. The TIM area was the same as the heatsink base area in each case. The PCBs used are the same as done in the PCB cooling investigation, with all thermal techniques used. Figure 9 shows the effect of heatsink area on $R_{\theta JA}$ for the bottom-side heatsink configurations. A similar trend of reduced effectiveness as the upper ends of area as the PCB area investigation can be seen here, indicating that making a heatsink too large not only adds substantial costs but gives very little returns. In the natural convection case, the $R_{\theta JA}$ value of 31 K/W with the largest heatsink shows a 30% improvement to the PCB cooling best-case without a heatsink. In forced air convection, this improvement is closer to 40%, due in part to the increased effectiveness of the top layer cooling as well as through the heatsink. Very similar results can be achieved with a heatsink with half the base area.

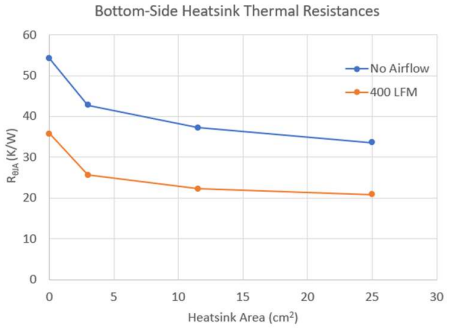

Fig. 9 Thermal resistance to ambient for different heatsink sizes attached to the bottom of the PCB with κ = 6 W/m·K TIM.

One major drawback of the bottom-side heatsinking approach is that it is heavily dependent on how effective heat spreads from the heat sources at the top layer to the bottom layer of the PCB. This not only includes higher thermal resistances in that heat path, but also makes the design of the PCB integral to the efficacy of the whole thermal solution. Figure 10 shows the bottom-side heatsinking approach with the 25 cm^2 heatsink in two cases. One includes the PCB cooling thermal techniques mentioned earlier, while the other has no vias and very thin copper layers. Both cases are for natural convection. In the case where no PCB cooling thermal techniques are used, the maximum temperature is only 4°C cooler than the case in Fig. 7(a) where there is no heatsink attached. This is because very little heat flux flows to the bottom of the board where heat can then transfer to the heatsink, so nearly all the convection is happening at the top layer of the board. Another drawback is that if there are components on the bottom side of the board, a pocket must be machined into the heatsink to avoid contact with them, which reduces the efficacy of the heatsink itself.

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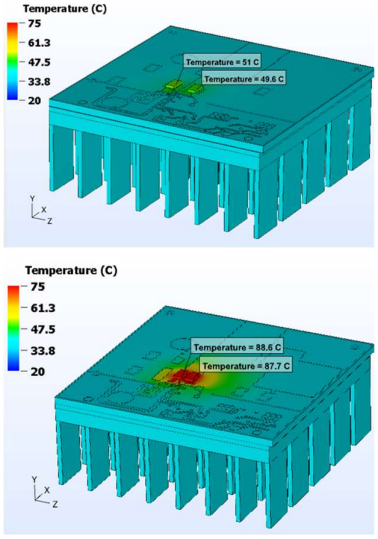

Fig. 10 Comparison of bottom-side cooling heatsink for (a) PCB with vias and (b) PCB with no vias.

5 Device Back-side Cooling

5.1 Back-side Heatsinking Motivation

Another method of using a heatsink to cool devices in a half-bridge is to attach the heatsink directly to the back of the devices. This is a more direct path than going through the board, so it presents an opportunity to lower thermal resistance significantly over using the bottom-side heatsink approach. eGaN FETs tend to have lower $R_{\theta JC}$ values than $R_{\theta JB}$ values [2]. However, there are some additional engineering challenges that come with attaching a heatsink directly to the top side of the device. A more complicated thermal stack up will include needing to account for mechanical tolerances, spacing, and higher potential for stresses that can damage the components on the PCB.

5.2 Mechanical Design Considerations

The TIM for a back-side heatsink fulfills the same purpose as it does for a bottom-side heatsink but there are minor differences in how one can select the appropriate material. For a back-side heatsink attach and because the thermal path from the junction is much shorter and the area of the devices is smaller, a much smaller TIM area can be used to mate the surfaces of the device to the heatsink. As such, a much higher conductivity TIM can be used as there is little impact to overall cost associated with making the TIM area as large as possible. However, there is a much larger constraint on how thin the selected TIM can be due to the contact pressures associated with the devices. Using a solid TIM thinner than a millimeter can result in high contact pressures on the devices for the desired TIM deflection . In a TIM pad with 0.5 mm thickness, deflections above 15% can result in contact pressures greater than 50 psi (345 kPa) [15]. It can also be very difficult to ensure that the TIM adequately covers the devices and separates them from the base of the heatsink when liquid or gel TIMs are used.

5.3 Simulation Results

The back-side heatsink cooling capability was examined in FEA simulation to compare against the bottom-side cooling approach. A TIM with κ = 17.8 W/m·K and thickness of 0.5 mm was placed over each FET, then the aluminum heatsink with a base area of 10 cm^2 is placed over the TIM. The simulation assumed 400 LFM forced air convection. The results of the simulation are shown in Fig. 11.

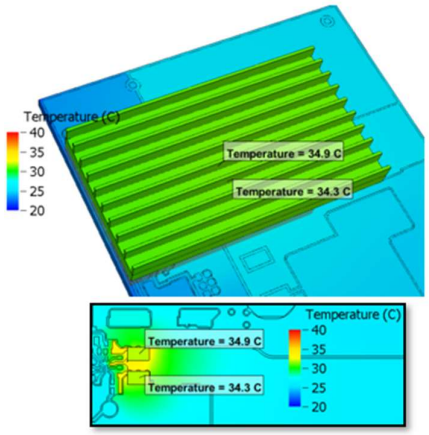

Fig. 11 Maximum temperature for back-side heatsink solution.

The back-side cooling setup results in a thermal resistance to ambient of 14.9 K/W, which is a 32% improvement over the 12 cm^2 bottom-side heatsink under 400 LFM that is shown in Fig. 9. Using a thinner TIM or one that is more thermally conductive can lower the overall thermal resistance even more, as well as optimizing the heatsink for the forced airflow condition [14].

6 Experimental Results

6.1 Experimental Test Setup

To validate the thermal resistance numbers obtained from the FEA simulations, the simulation setups were also run experimentally using the same board characteristics. For the configurations without heatsinks, the boards featured a half-bridge running the FETs activated in reverse- bias to allow for the current and power dissipation across the FETs to be accurately controlled. The power dissipation is calculated for each individual FET by multiplying the measured voltage across the part by the current running through the parts. The temperatures of the devices were measured both by a fiber

optic thermal sensor beneath the die and with an IR camera. The dies were painted black to increase emissivity. For board configurations with heatsinks, a data acquisition lab setup (DAQ) was used to measure the temperature and power dissipations of the devices accurately. All boards can be measured both in still air and with accurately controlled airflow. The measured device temperature and calculated power dissipation are then input into Eq. (1) to calculate the thermal resistance of the part in the given board setup.

The cooling conditions used to validate the results of the simulations will be the PCB only cooling and the back-side cooling cases. The FET used matches the one used in the simulations, EPC2619 [2]. The test boards are mounted on a motherboard which provides signal and power connections, power supply, and electronic load connections. The motherboard is placed in a forced-cooling test chamber. An F200 anemometer is placed upstream to measure air speed measurements. Thermocouples and fiber optic cables can be used to measure temperatures on the devices. Figures 12 shows pictures of the demo board used, the test setup, as well as how the OpSense® OTG-F sensor is fed through drill holes in the board to measure the die.

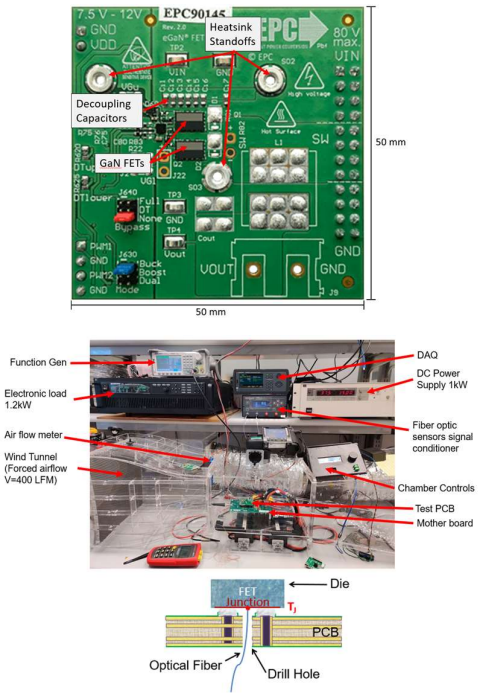

Fig. 12 (Top): PCB image showing GaN FETs and heatsink standoff locations. (Middle): Test setup with instrumentation. (Bottom): Optical sensor measurement diagram.

6.2 PCB Only Cooling

The different PCB design techniques that maximize thermal performance without a heatsink were experimentally tested to verify the accuracy of the FEA simulations. Each board was tested with a constant reverse current of 0.75 A with temperature measurements being made five minutes after activating the FETs. Figure 13(a) shows the results comparing a board with minimal thermal techniques used and Fig. 13(b) shows the results with all the thermal techniques being used. The experimental result shows high agreement with the simulation results shown in Fig. 8. The effectiveness of the heat spreading in Fig. 13(b) is evident compared to that in Fig. 13(a), where the outer edges of the board are still relatively cool compared to the pad. The results show a satisfactory agreement with the FEA simulations and the efficacy of these PCB design techniques in reducing $R_{\theta JA}$. Validation errors in the results could arise because of the difference in power dissipation between the simulations and the experiments. In the simulations each FET is dissipating exactly one watt while in the experiments the two FETs will each have a different power dissipation. This results in one FET contributing more to the heating of the pad and causing an imbalance between the two. More specific experimental results are given in a previous study [4].

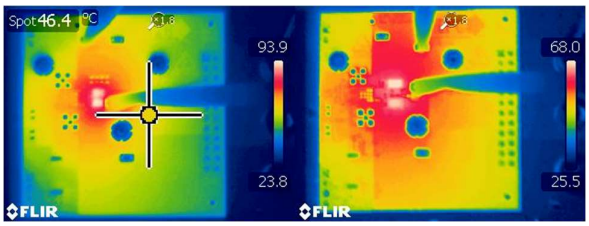

Fig. 13 (a) Experimental result with 0.5 oz Cu, minimal vias, and adjacent FETs; (b) Result with 2 oz Cu, vias under the FET, and separated FETs.

6.3 Heatsink Cooling

The simulated heatsink used in Fig. 11 was attached to the back-side of the die with the same stack up as simulated and described. The results of the tests are shown in Table 2. The 400 LFM case shows agreement with the 14.9 K/W resistance that was simulated, with error in the simulation of about 5%. The simulated result was also an underestimate of the result shown in the experiment. This could be for several reasons, including assuming the TIM has the ideal thermal conductivity that is specified in the datasheet when used in simulation. The bulk conductivity that is reported will be larger than what the conductivity is in practice on a board. There were also non-ideal conditions in the wind tunnel such as wires and the motherboard that could have changed the airflow experienced over the board.

Table 2 Thermal resistance with back-side cooling solution for different airflow speeds.

Airflow	*Power Loss[W]*	$R_{\theta JA}$ *[K/W]*
200 LFM	2.91	21.06
400 LFM	2.89	17.20
600 LFM	2.92	15.92

7 Conclusion

7.1 Observations

The different thermal techniques presented in this work show different capable power dissipations before reaching the maximum rated temperature of the devices in steady state. In a PCB only cooling case, the parts can potentially reach 2 W dissipated each without airflow, and 3 W each with airflow. The bottom-side cooling case without airflow can reach a total power dissipation of about 4 W depending on the size of the heatsink. With airflow that total amount can go up to about 6 W. The most effective cooling solution is backside cooling, which with airflow included can reach a total power dissipation of over 8 W in steady state with even an unoptimized solution. Higher airflow speeds; more carefully designed heatsinks for a specific application; and different forced convection cooling methods can all be used to increase the power dissipation further.

7.2 Conclusions

A study and evaluation on best thermal practices to cool GaN FETs in different thermal environments was presented. The approach begins with reducing the thermal resistances in the PCB without external parts by increasing copper thickness, including thermal vias, and separating the heat generating components. Then two different heatsinking approaches are examined to evaluate the impact on $R_{\theta JA}$, one focusing on board-side thermal resistance by attaching to the bottom of the PCB and the other focusing on the thermal resistance through the case by attaching to the top of the GaN FETs. The PCB-cooling baseline without a heatsink reduces $R_{\theta JA}$ by 30% with little to no additional cost in the manufacture of the PCB itself. Attaching a bottom-side heatsink with a high-performance TIM reduces $R_{\theta JA}$ by an additional 30% over this improved baseline. A backside heatsink stackup with a high-performance TIM reduces $R_{\theta JA}$ by about 60% over the improved PCB-only baseline.

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