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Evaluation and Efficiency Study of High Current Class Discrete IGBTs-based Converter Systems

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Abstract

The most recent generation technologies of discrete insulated gate bipolar transistor (IGBT) could boost the power density and efficiency of converter systems significantly. This paper investigates the performance and consequences of single 140 A discrete IGBT-based converter systems, including a comprehensive comparison to state-of-the-art systems with 75 A devices in parallel and silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET)-based converters. This study evaluates the improvements in the converter system by using the commercially available 1200 V IGBTs from different technologies in 140 A (G1) and 75 A (G2 and G3) in TO247 PLUS packages and 1200 V SiC MOSFET in 14 mΩ (G4) in TO247 package. To comprehend the performance and viability of discrete IGBTs in a power electronics system, dynamic and static measurements were conducted, followed by an application measurement test in a three-level T-type clamped neutral point topology inverter. In this investigation, we acquire an in-depth understanding of the various test combinations of discrete IGBT-based converter systems, ultimately achieving an efficiency of 97.5% with 1 x G1 in comparison to a state-of-the-art system with 2 x G2 with an efficiency of 97%. In addition, the adaptability of new-generation IGBT characteristics demonstrated that Si IGBTs can occasionally substitute SiC MOSFETs.

1 Introduction

Most modern inverter systems utilize wide band gap devices – SiC MOSFETs in their inverter system design to achieve higher efficiency and power density as a result of the material's superior advantages over silicon IGBTs [1]. IGBTs, on the other hand, are still evolving with their technology designs (square cell design and stripe cell design) to maintain their positions in power electronic systems in order to attain higher system performance. Today, IGBTs are frequently designed with micropattern trench (MPT) cell technology to achieve higher power density devices, and several studies demonstrate and highlight the important characteristics and performance of the recent generation IGBTs based on MPT technology [2] [3]. It has been observed that the stripe cell design technology facilitates the goal of higher current density devices, allowing for more efficient use of silicon area, with a consequent advantage on maximum current rating devices in TO247 packages. Several studies have demonstrated the superior advantages of SiC MOSFETs over IGBTs [4] [5]. However, there is a dearth of research comparing the electrical and thermal behaviour of SiC MOSFETs and IGBT devices with high current class in grid-connected systems. In addition, grid-connected industrial applications are more and more demanding for compact, reliable, and cost-effective high-power converter systems. To achieve high system output power, parallel connections of devices are typically required, due to the limited current handling capacity of the devices. Several studies indicate that disparities in key device parameters, which can lead to current mismatching and uneven temperature distribution; Consequently, this can lead to device degradation over time, and potential early failure [6] [7].

The objective of this study is to compare the key characteristics of G1 in a converter system to a state-of-the-art system with two G2 devices operating in parallel and to enlighten the power electronics designers on the benefits of new discrete high-current class discrete IGBTs. The efficiency and thermal performance of the devices in a t-type inverter system have been experimentally analysed. Additionally, a comparison between the most recent iteration of discrete IGBTs and SiC MOSFETs has also been studied.

2 Device Parameter Comparison

The evaluation utilizes multiple IGBTs co-packed with a freewheeling diode from G1, G2, and G3. The study concentrates on the inverter system design utilizing a single G1 device in comparison to the current state-of-the-art system solution using two G2 devices in parallel. In paralleling operations, a careful choice of the pack-

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age is a crucial aspect for the design of an inverter system, as its parasitic inductance, which influences the switching losses of the device, and its thermal resistance, which in turn affects performance and heat sink design of the inverter system [8]. In addition, Table 1 illustrates the device parameters of the G1, G2, and G3 devices required for paralleling operation. In order to improve the accuracy of the analysis, devices with no short circuit capability withstand time are chosen for comparison.

Table 1. Comparison of electrical parameters of IGBT

Technology	**G1**	**G2**	**G3**
	Micropattern Trench	**Field Stop Trench**	**Micropattern Trench**
Nominal collector current, (IC, A)	140 A	75 A	75 A
Gate charge, (QG, nC) @ Inom	970	399	518
Turn-on time, (tdon, ns) @ Inom, 175°C	63	56	52
Turn-off time, (tdoff, ns) @ Inom, 175°C	619	364	545
IGBT Thermal resistance, (Rth(J-c), K/W)	0.16	0.19	0.27

3 Electrical Measurements

To select the optimal combination of paralleled devices for application measurement in order to avoid current imbalance during turn-on and turn-off events, a comprehensive electrical characterization of the devices was conducted, with a focus on the dynamic and static losses. The conventional analogy curve tracer is used to measure the static losses - Vce(sat) of the IGBTs by applying a constant current while the gate is swept; for the application, since the conduction losses in the t-type are lower compared to the other topologies, the nominal devices are chosen, and on the other hand, for the switching loss calculation, a standard double pulse setup is utilized as described in [9], Fig. 1(a) and Fig. 1(b) shows the turn-on and turn-off losses and switching waveforms of G1, G2, and G3, while the switching waveform evidently demonstrates the advantages of the feedback inductance effect when paralleling two G2 and two G3 devices versus a single G1 device in the test.

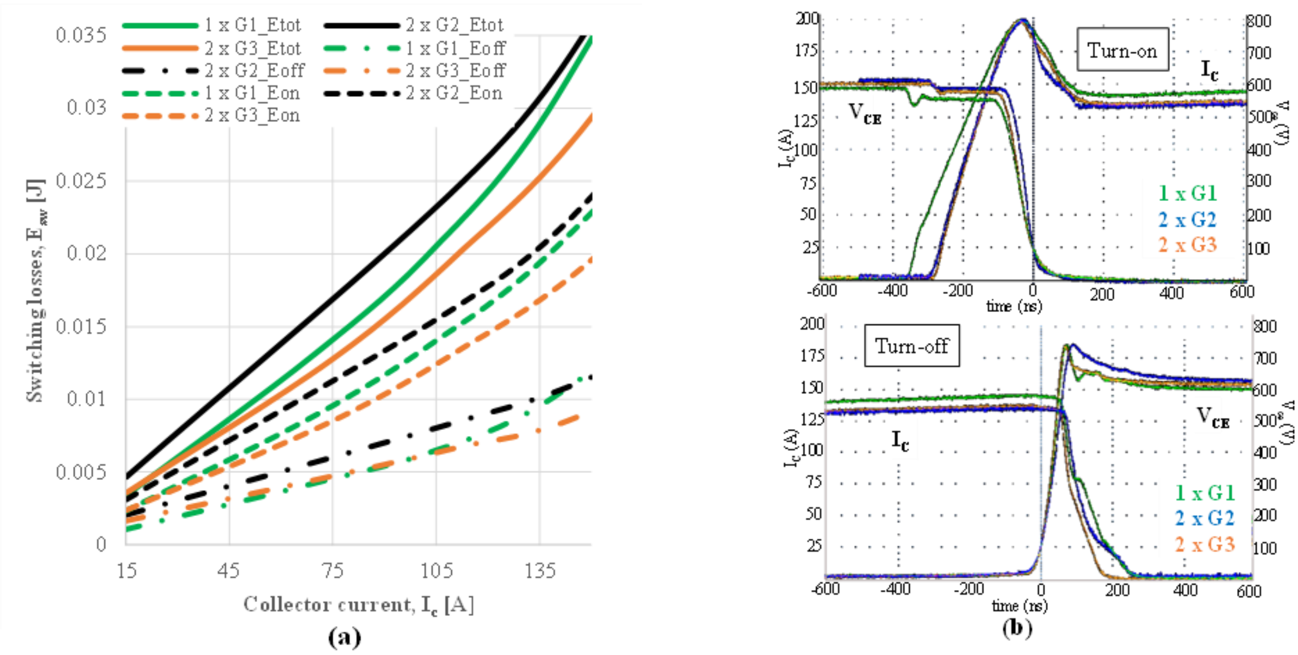

Fig. 1. switching losses of IGBTs at 600 V, 140 A, 175°C, Rg(on) and Rg(off) - 5.2Ω, (b) turn-on and turn-off waveforms of IGBTs at 600 V, 140 A, 175°C, Rg(on) and Rg(off) - 5.2Ω.

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4 Application Measurements

Figure 2 (b) depicts the experimental test arrangement used to analyse the electrical and thermal performance of the various test configurations of discrete devices. Due to the limited experimental system, a 4.5 kW AC electronic load with a 3-level T-type inverter board in a single phase is used. To ensure a uniform evaluation of different 1200 V IGBT devices with a high current class, the 650 V devices utilized in the T-type neutral-point-clamped (TNPC) inverter remain unchanged across all test configurations. In order to test the efficiency of the G1, G2, and G3 devices, the output load current is varied at a constant switching frequency of 33kHz using the application test platform. Due to the technology benefits, it is evident from Figure 2(a) that the converter system with a single G1 device was 0.5% more efficient than the state-of-the-art inverter system with two G2 devices in parallel. However, when comparing the performance of G1 and G3 devices, the G1 and G3 device has similar efficiency, whereas the G3 device has a performance advantage in terms of thermal performance due to current sharing in paralleling.

In addition, a high current class discrete IGBT (G1) is compared to a SiC MOSFET (G4), and the output demonstrates that the G1 could replace the G4 up to 40 kHz switching frequency. In contrast, the characteristics of the SiC semiconductor become evident when G1 and G4 devices are operated at switching frequencies greater than 40 kHz.

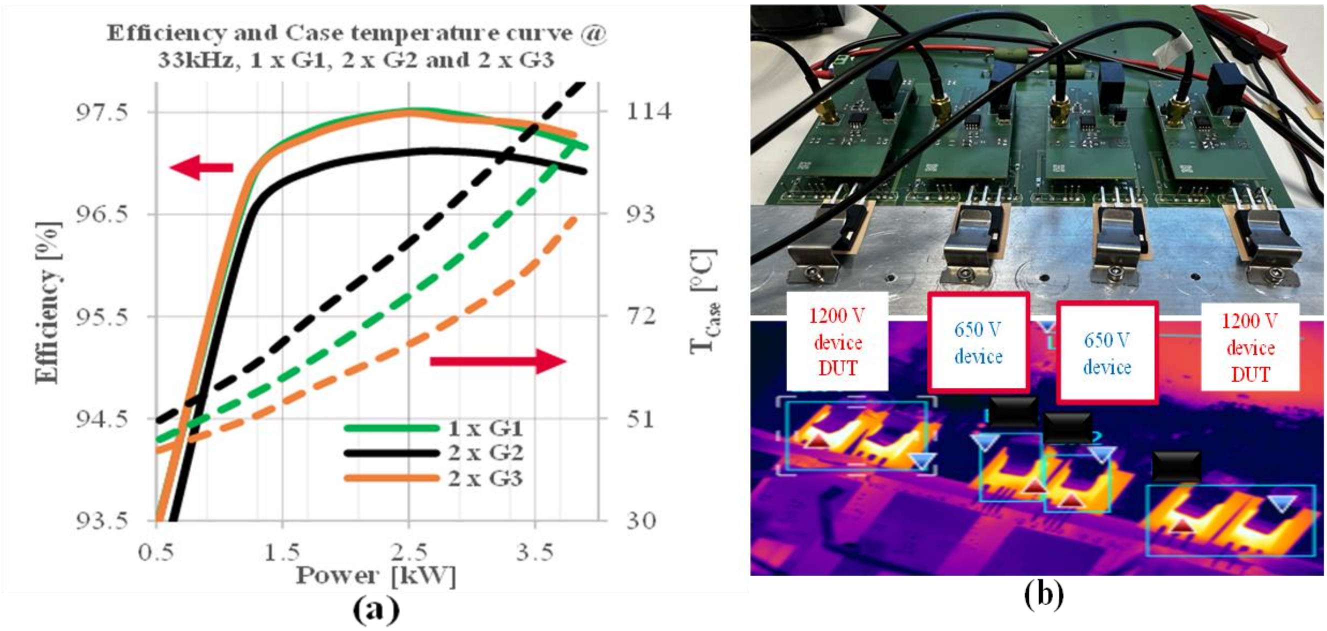

Figure 2. (a)Efficiency and case temperature performance in 3-level TNPC inverter with 1 x G1, 2 x G2 and 2 x G3 devices (b)Test setup of 3- level TNPC inverter and thermal image with 2 x G2 devices.

5 Conclusion and Future Work

This paper quantifies the comparator system with a single 140 A device to an equivalent state-of-the-art system with parallel-connected 75 A devices. Dynamic, static, and application measurements indicate that the paralleling of devices to attain higher system levels can be replaced with a single 140 A device to avoid paralleling's attributed design risks. On the other hand, it is possible to replace SiC MOSFETs up to 40kHz with minimal design compromise. Future research will concentrate on the influence of the TO247 PLUS 4-pin packages, as well as the influence of various test configurations of discrete IGBT and SiC MOSFET in a 3-level T-type inverter system.

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