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High Density USB-PD ZVS Flyback Converter Based on Seconary Side Control

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Abstract

This paper presents a zero-voltage-switching (ZVS) USB-PD Flyback converter with a secondary control method for variable output voltage and loading. The PD chip at secondary side integrates both primary PWM and Synchronous Rectifier (SR) control function to achieve ZVS of primary main power switch, which simplifies the circuit and reduces the switching losses. Comparing to the based primary ZVS technique, the secondary control method eliminates the auxiliary winding and ZVS switch at primary side and prevents the synchronous rectification MOSFETs' gate driver from being falsely triggered. Due to ZVS, high switching frequency can be enabled to use smaller size transformer and capacitor to get high power density for PD charger together with GAN switch. The detailed operation principle and design considerations are presented. Performance of the proposed control method is validated by the experimental results from a 5-20V/3.25A prototype.

1 Introduction

Flyback topology is widely used, especially for lower to medium power application as in phone chargers and adapters, due to its simplicity, low cost and flexibility to wide input voltage variations [1][2]. As the fast charging and USB-PD standards with wide output voltage variations are widely and rapidly adopted and the miniaturization is the trend of the mobile power supplies, there is a growing demand for significant power density improvement for USB-PD chargers and adapters [3]. Any size reduction of the USB-PD chargers and adapters while maintaining better thermal performance must be accompanied by some efficiency improvement as well as a switching frequency increase for smaller size of the magnetic and capacitive storage elements. To meet these requirements, a novel Flyback design with ZVS was developed [4]. In most applications, the Flyback with ZVS bases on primary side control. Like Flyback-Mode current injection ZVS, it needs auxiliary winding and ZVS switch at primary side and has a risk, that the SR MOSFETs' gate driver may be falsely triggered. Like Forward-Mode current injection ZVS, it solves falsely trigger SR issue, but still requires auxiliary winding and ZVS switch at primary side. Another popular topology-ACF, it can recover the leakage inductance energy and implement ZVS, but additional high side switch and diver are essential [5]. All those solutions bring good performance, but they also increase system cost and complexity of implementation.

This paper proposes a secondary side-controlled ZVS Flyback topology, which is well suited to address the challenges by providing SI or GAN driver and high switching frequency of up to 300kHz to meet smaller form factor. And the controller at secondary side integrates SR control and PD control to avoid SR false trigger and implement ZVS of primary main power switch, which accomplishes soft switching and reduces the switching losses. Additionally, the chip also does not need additional auxiliary winding and ZVS switch, see Fig. 1, which simplifies the circuit and reduces the Bom cost. Its high integration, simplicity, low cost, high density is best-in-class supplier of USB-PD solutions for the charger and adapter market with class-leading efficiency and BOM.

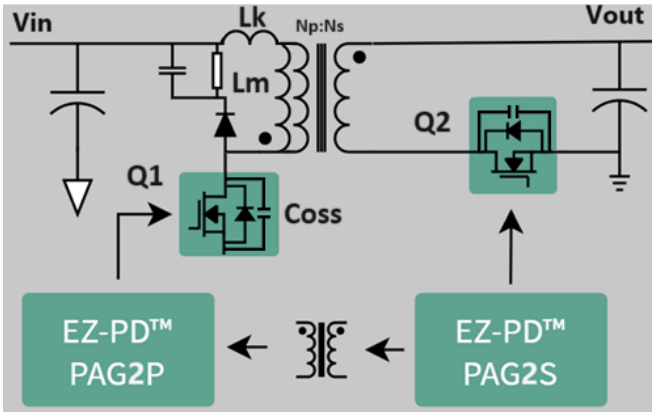

Fig. 1. Topology of the ZVS Flyback converter secondary side ZVS control method

2 Secondary Side Control Principle

Fig.1 illustrates the circuit diagram of the secondary side control ZVS Flyback converter with SR [6]. Secondary side generates all PWM, SR control, ZVS implementation and transfers PWM to primary side. Q1 is the primary switch, and Q2 is the output synchronous rectifier. Lm is the transformer magnetizing inductance and Lk is the transformer leakage inductance. The transformer turn ratio is Np:Ns. Coss is primary Si or GAN MOSFET parasitic capacitor between drain and source.

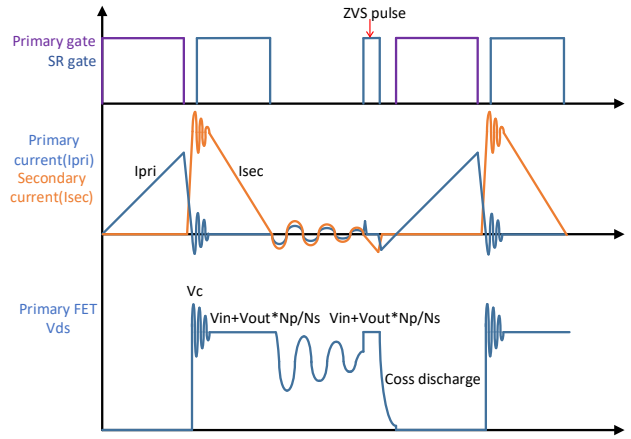

Fig. 2. Steady state waveforms of the secondary side control ZVS Flyback converter

Fig.2 shows the steady state waveforms of the secondary side control ZVS Flyback converter. Based on the waveforms, there are three main operating stage during one switching cycle. And there also are some parasitic resonance mode at the moment of Q1 switching off, Q1 switching on and entering into DCM. Below show the equivalent circuits for three main operating stage of the ZVS Flyback converter during one switching cycle.

2.1 Primary Energy Storage Stage

In this mode, primary side switch Q1 switches on and secondary side switch Q2 switches off. The output capacitor supplies power for load (Fig.3) [7].

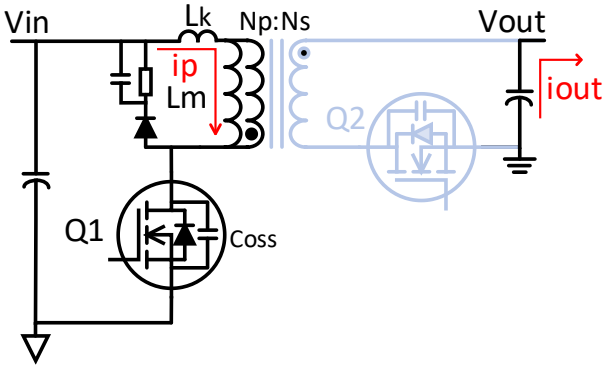

Fig. 3. Equivalent circuit in Primary Energy Storage Stage

From the waveform at the primary energy storage mode, the primary side magnetizing current Ip increases linearly to Ipk. The energy is stored in the magnetizing inductor Lm and leakage inductor Lk, which is the same as the conventional Flyback converter, as depicted in Fig.4.

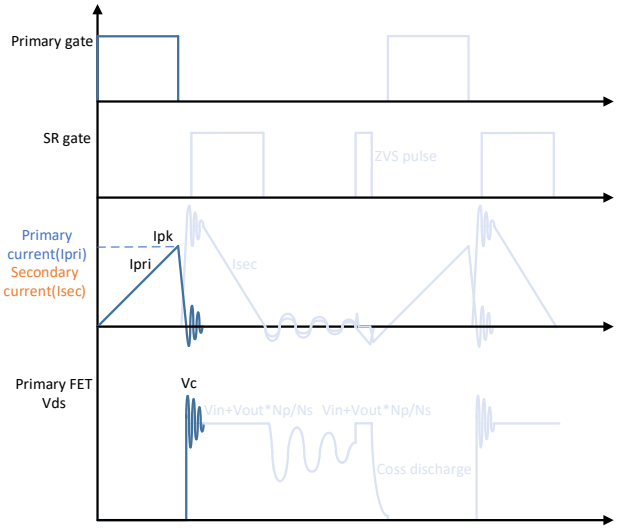

Fig. 4. Waveforms in Primary Energy Storage Stage

At the end of the mode, Q1 switches off and leakage inductance Lk energy cannot transfer to secondary side, so leakage inductance Lk and Coss will resonate, Lk current will charge Coss, RCD snubber circuit clamps the Max Vds to Vc [8].

2.2 Secondary Energy Delivery Stage

After primary energy store, the converter enters into secondary stage-energy delivery stage. Q1 switches off, the SR sense circuit detects and triggers the load current threshold, and Q2 switches on. Here the SR sense circuit and driver feature decide the turn on delay time (Fig.5).

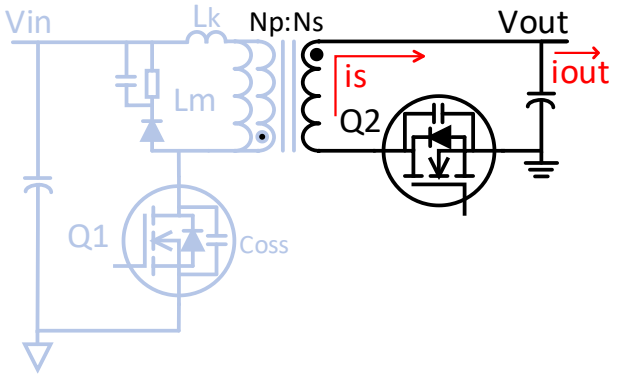

Fig. 5. Equivalent circuit in Secondary Energy Delivery Stage

The primary magnetizing energy is delivered to the secondary side and the secondary demagnetizing current Is decreases linearly. Is charges output capacitor and supplies power for load.

Primary side magnetizing inductance Lm voltage is clamped to Vout/Ns*Np, so Vds of Q1 also is clamped to Vin + Vout/Ns*Np until Is decreases to zero as shown in Fig.6.

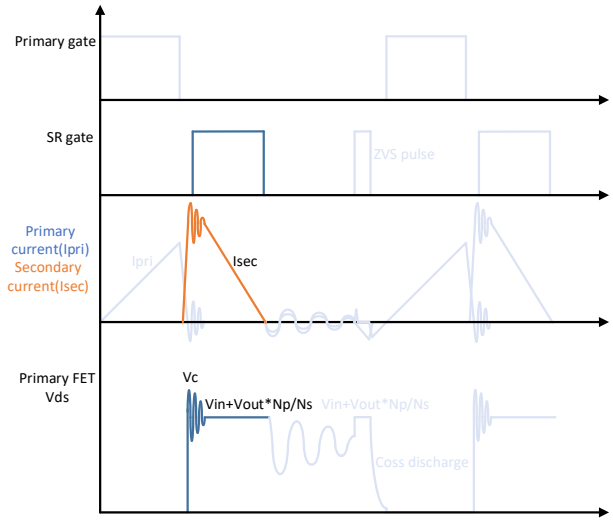

Fig. 6. Waveforms in Secondary Energy Delivery Stage

After Is deceases to zero, the converter enters into next cycle or DCM. If in DCM mode, Q1 and Q2 both switch off, Coss will discharge to primary inductance Lm and Lk, Coss, Lm and Lk form resonance until ZVS pulse switches on (Fig.7).

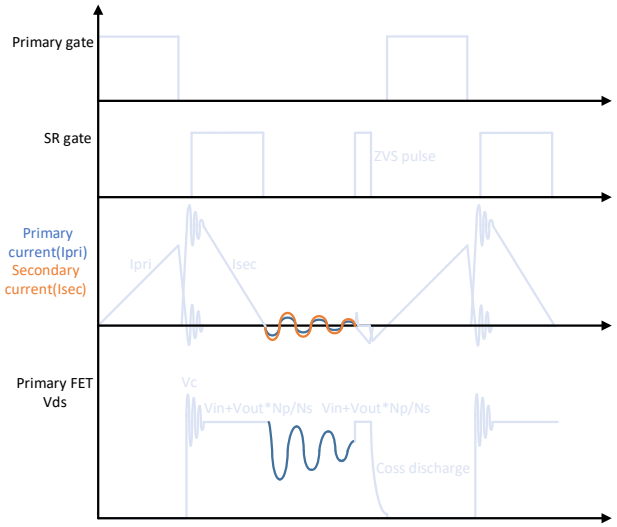

Fig. 7. Waveforms after secondary current falls to zero

2.3 ZVS Implementation Stage

ZVS is actualized by turning on secondary synchronous rectifier switch for a short interval to reversely magnetize secondary inductance and then SR switch turns off, primary inductance Lm deliveries energy to discharge Coss voltage down to 0V.

As can be seen in Fig.8, at the ZVS implementation stage, Q2 turns on again before primary switch Q1 turns on. The current Is through secondary winding increases reversely and linearly to Ipk1.

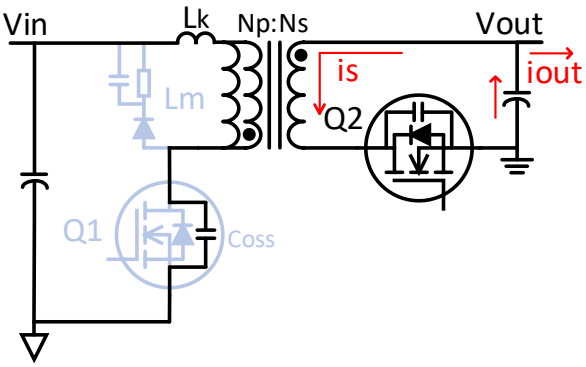

Fig. 8. Equivalent circuit in ZVS pulse

The negative current Ipk1 is proportional with SR turn on time. The negative current is used to magnetize secondary inductor. The voltage across the magnetizing inductance Lm is clamped to –Vout*Np/Ns, and drain to source voltage of Q1 is clamped to Vin+Vout*Np/Ns (Fig.9).

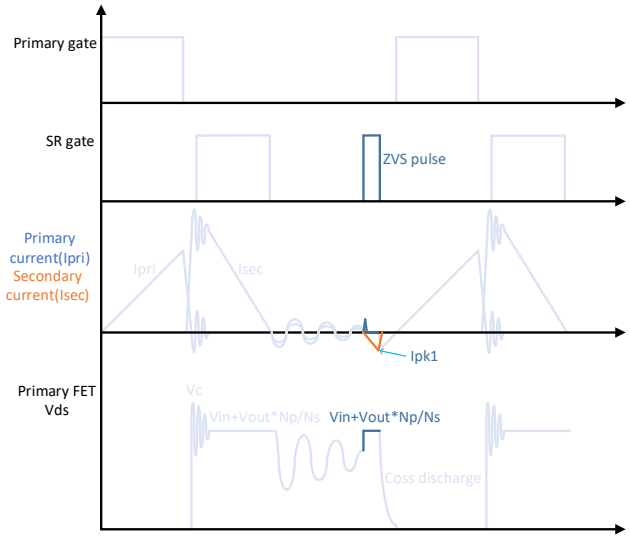

Fig. 9. Waveforms during ZVS pulse

Fig.10 show that after ZVS pulse, SR switches off. The secondary inductance magnetizing energy is transferred to primary side and primary inductance demagnetizes to generate primary negative current and to discharge Coss of primary switch Q1.

The magnetizing energy stored in secondary inductance by the negative current must be more enough to discharge Coss from Vin+Vout*Np/Ns down to zero to implement ZVS in the all input voltage range [9].

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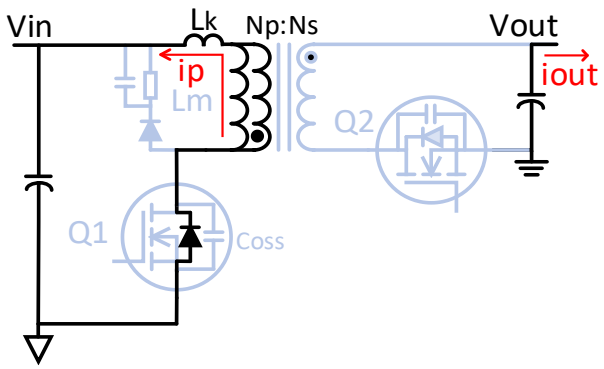

Fig. 10. Equivalent circuit in primary ZVS implementation stage

Fig.11 depicts the parasitic Coss voltage decreases until the anti-parallel body diode of primary switch Q1 forwards bias. Before Q1 turns on again in next cycle, the Vds of Q1 discharges to zero, zero voltage switching of primary switch is fulfilled and Coss energy transfer to bulk capacitor, that can improve efficiency [10].

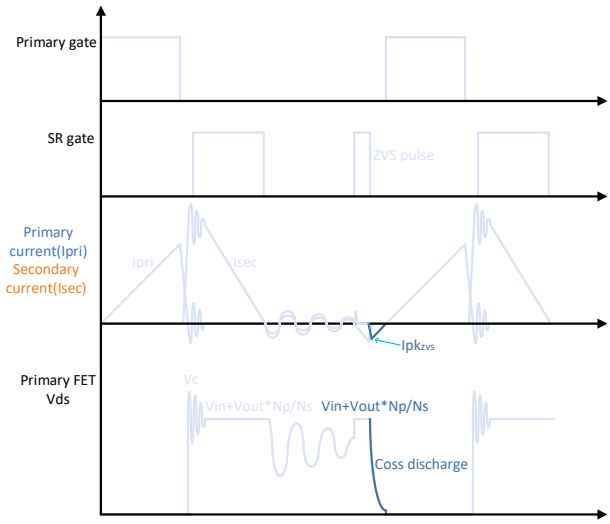

Fig. 11. Waveforms in primary ZVS implementation stage

3 DESIGN CONSIDERATIONS

From above circuit, principle and waveforms description, the most are same with conventional Flyback converter, but ZVS operation. There is an additional reverse power delivery period through the SR switch Q2 turning on for an interval PWM pulse before primary switch Q1 switches on.

Exactly the PWM pulse is extremely short, and the reverse power also is pretty little, which almost do not affect the output. But ZVS operation is critical to affect the efficiency. So some design details about ZVS implementation must be considered, like ZVS pulse width, deadtime after ZVS pulse, SR turn on moment, which are elaborated here.

3.1 ZVS turn on pulse width

If ZVS pulse is too short, the reverse power is not enough to discharge total parasitic capacitor, total charge cannot fully be transferred back to input bulk capacitor, ZVS cannot be implemented well [11]. If ZVS pulse is too long, the reverse negative current rises too high, and output capacitor voltage Vout will drop more, that also cause more loss and efficiency lower. Base on the energy conservation, the minimum ZVS pulse width can be expressed as:

$$E_{tot} = \frac{1}{2} * C_{tot} * \left(Vin + Vout * \frac{Np}{Ns}\right)^2 \quad (1)$$

$$Ton_{zvs\_tot} = \frac{Ls * Ipk_{zvs} * \frac{Np}{Ns}}{Vout} = \frac{Lm * Ipk_{zvs}}{Vout * \frac{Np}{Ns}} \quad (2)$$

$$Ton_{zvs} > Ton_{zvs\_tot} \quad (3)$$

where

$$C_{tot} = Coss + Cpar \qquad Ipk_{zvs} = \sqrt{2 * \frac{E_{tot}}{Lm}}$$

$Coss$ is primary switch Q1 parasitic capacitor, $Cpar$ is PCB and transformer parasitic capacitor, C_{tot} is total parasitic capacitor, E_{tot} is total parasitic capacitor store energy, Ipk_{zvs} is primary reverse peak demagnetizing current. Ton_{zvs_tot} is ZVS pulse width calculated value. Ton_{zvs} is ZVS pulse width time the system should set.

3.2 Deadtime after ZVS pulse

During ZVS pulse, primary total parasitic capacitor C_{tot} is charged to Vin+Vout*Np/Ns. After ZVS pulse, need enough deadtime to discharge the Coss to input bulk capacitor as can be shown in Fig.12. If the dead time is not enough, the Coss voltage cannot decrease to zero, ZVS cannot be reached. If the dead time is too long, primary switch cannot turn on in time, the secondary side voltage will fall more to not have enough energy to power supply for load.

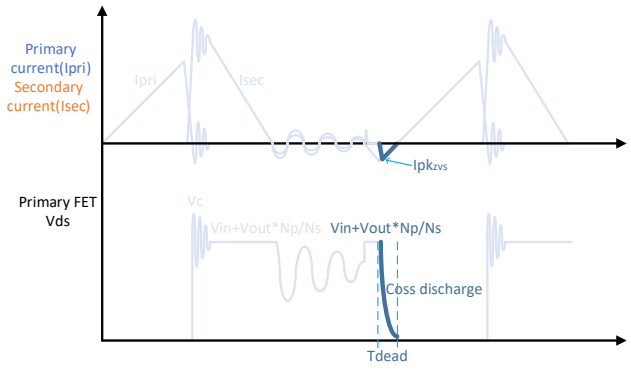

Fig. 12. Primary Coss discharge waveforms

$$T_{tot} = \frac{2 * C_{tot} * (Vin + Vout * \frac{Np}{Ns})}{Ipk_{zvs}} \quad (4)$$

$$Tdead > T_{tot} \quad (5)$$

The minimum dead time can be designed in (4)(5). Where T_{tot} is the calculated dead time. $Tdead$ is the dead time the system should set.

3.3 SR turn-on moment for ZVS

When SR switch Q2 turns on for ZVS is also very critical. If ZVS pulse starts at t1 or t5 point, spike voltage on Q1 is the lowest as given in (6), that can cause less loss to be dissipated in RCD snubber circuit [12]. Meanwhile, Q2 Vds resonate to valley and it is easier to generate a negative secondary current. If ZVS pulse starts at valley t3 point, the spike on Q1 is the highest, that can cause higher stress on primary switch and more loss (Fig.13).

$$Vds_{Q1}(t) = Vin + Vout * \frac{Np}{Ns} * e^{-\frac{t}{2\tau}} * \cos(\omega t) \quad (6)$$

where

$$\tau = 2\pi * \sqrt{(Lm + Lk) * Ctot}$$

$$\omega = \sqrt{\frac{1}{(Lm + Lk) * Ctot}}$$

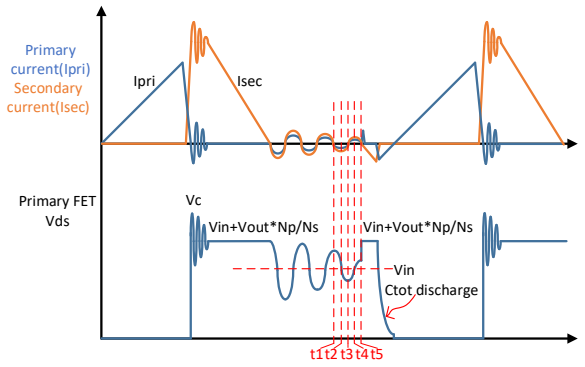

Fig. 13. DCM resonance waveforms after Secondary Energy Delivery Stage

Accordingly, consider the switch stress, loss and ZVS current building, ZVS pulse should start at primary peak t1 or t5, secondary side is at valley, that is better for efficiency and stress (Fig.14). The controller bases at secondary side, and secondary valley is detected very easily with valley detect sensing.

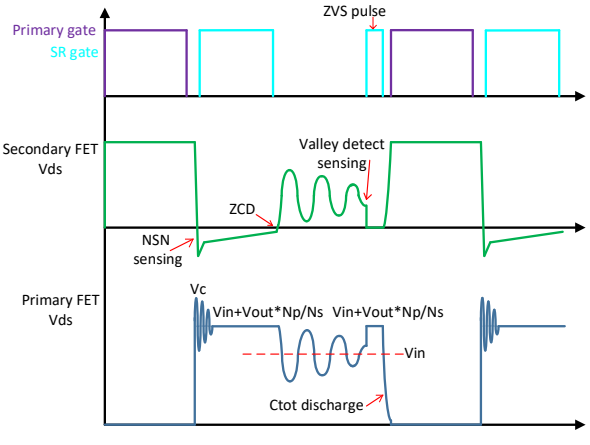

Fig. 14. ZVS pulse switch on waveforms

4 Experiment Results

To experimentally characterize the secondary side control ZVS Flyback converter performance, a 65W demo was constructed to the specifications listed below:

- AC input voltage: 90~264Vac
- USB PD output:
  5V3A,9V3A,15V3A,20V3.25A PDO,
  3.3~21V3.25A PPS
- Transformer
  Core: ECW23.7F/12.8 DMR96
  Inductance Lm: 210uH
  Np: 18T 0.1*20
  Ns: 3T 0.1*80
  Lk: 3uH
- Q1: CoolGaN IGLD60R190D1AUMA1
  Vds:600V
  Rdson: 190mΩ
  Coss: 32.5pF
  Qg: 3.2nC
- Q2: OptiMOS™ 5 BSC050N10NS5
  Vds:100V
  Rdson: 5mΩ
  Coss: 490pF
  Qg: 49nC
- Controller: CYPAP212A1, CYPAS211A1

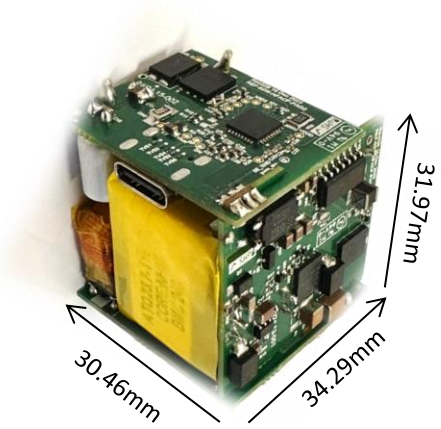

Fig. 15. View of the secondary side-controlled ZVS Flyback board

The secondary side-controlled ZVS Flyback demo board for 65W USB-PD charger is showed in Fig.15. The size is 30.46mm*34.29mm*31.97mm. Power density is 31.89 W/in^3.

Primary gate PWM signal, Q1 drain to source voltage waveform, secondary SR gate PWM signal, Q2 drain to source voltage waveform can be seen in Fig. 16. Before primary Q1 switches on, the ZVS pulse switch on to implement ZVS.

The Q1 can switch on with zero Vds due to ZVS implementation as shown in Fig. 17, that discharges the Coss and Ccapr to zero before Q1 switches on in next duty cycle. In addition, SR drain to source voltage can be charged to Vin/Np*Ns+Vout without spike in advance,

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that is due to the ZVS without resonance. Consequently, SR RC snubber can be diminished or eliminated, that can reduce components and improve efficiency.

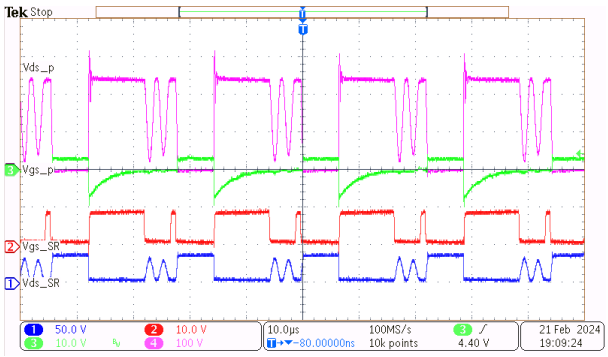

Fig. 16. Primary and secondary Vds and Gate waveform of secondary side-controlled ZVS Flyback prototype

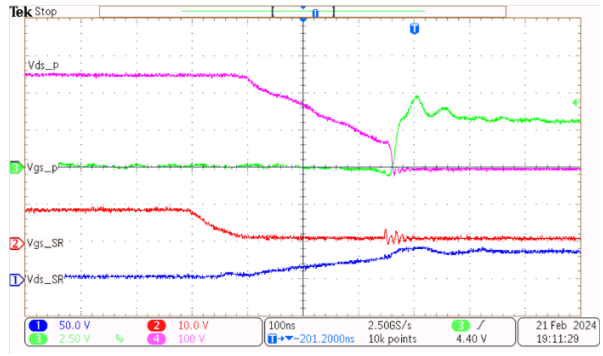

Fig. 17. Primary side GAN zero-voltage switching waveform of secondary side-controlled ZVS Flyback prototype

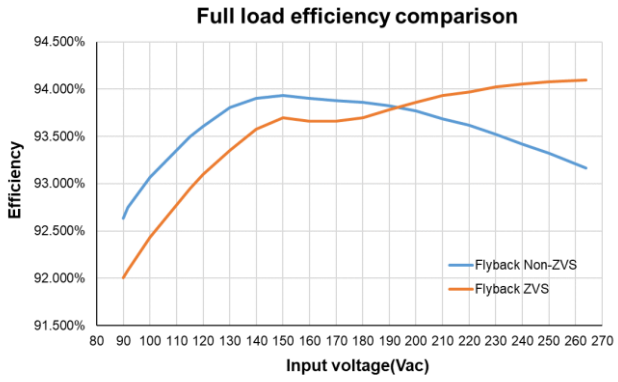

Fig. 18. Full load efficiency comparison between ZVS and Non ZVS of the prototype

Fig. 18 compares the measured full load 65W efficiency of the demo with ZVS and Non ZVS. At high line the ZVS can improve the efficiency by up to 1%, but at low line ZVS cannot bring better efficiency. At low line, the converter works in QR mode, Vds valley is inherently quite low, SR ZVS pulse will cause more loss during the energy transfer from secondary side to primary side.

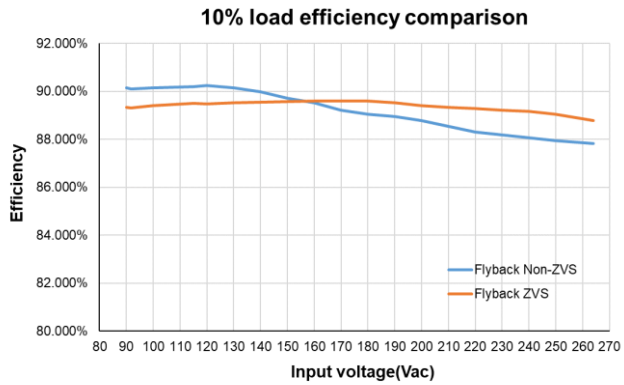

Fig. 19. 10% load efficiency comparison between ZVS and Non ZVS of the prototype

Fig. 19 shows the measured light load 10% efficiency of the demo with ZVS and Non ZVS. At high line the ZVS can improve the efficiency about 1%, but at low line ZVS cannot bring better efficiency.

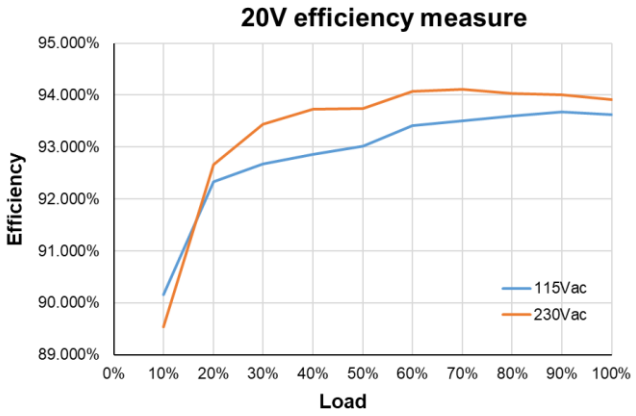

Fig. 20. 20V efficiency measure with ZVS at high line and Non-ZVS at low line

From the comparison measured efficiency, the secondary side control ZVS Flyback converter has more impact on the efficiency at high line and light load conditions. Thanks to the programmable feature, the converter can disable ZVS at low line and enable ZVS at high line, that can result in higher efficiency at all range line voltage.

The 20V efficiency with different load is summarized in Fig. 20. The firmware disables ZVS at low line and enables ZVS at high line, the best efficiency can be realized over the entire range from low line to high line.

5 Conclusion

USB-PD applications like the charger and adapter especially benefit from the simplicity and low cost of Flyback converter. To meet smaller form factor and higher power density, high switching frequency and GAN with better frequency performance are an increasing need to decrease transformer and capacitor size. Here the

more switching losses and thermal issue due to conventional hard switching with high switching frequency is hard to be avoided.

The new Flyback converter technology with ZVS control brings soft switching into convention Flyback with a superior switching performance. The ZVS Flyback is specifically optimized for up to 300kHz high switching frequency and zero voltage switching performance to meet high power density charger or adapter.

The remarkable feature is that all control base on secondary side, like PWM generator, SR control, PD controller, ZVS implementation, that is better to detect Vout variation, monitor output current change, control primary and SR switching without false triggering.

Programmability is another important feature, as present in above critical considerations, it is flexible to implement best ZVS condition by the programmable parameters. And SR and PD control performance also can be optimized to the best through tuning firmware parameters.

The significantly improved secondary control ZVS technology for high frequency application does not enable an increase in the number of devices required. Moreover, its compatible driver for GAN is best solution for high frequency and high efficiency need, without having a negative impact on the temperature of the devices. This provides not only an advantage in terms of bill-of-materials (BOM) cost, but also a chance for a further optimization at the system design level, which is expected to further boost efficiency, reduce the converter size and increase the power density.

Furthermore, designing new demo with planar transformer to run higher frequency 250kHz is ongoing, its higher switching frequency performance and efficiency will be verified, higher power density for PD-USB solution will be validated.

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