An Automatic Optimization Algorithm of SiC MOSFET Power Cycling Test parameters Based on the Device Thermal Networks

Hao Jin[1,2], Jin Zhang[1], Xinyu Zou[1,2], Yao Yan[1,2]

[1] Institute of Electrical Engineering of the Chinese Academy of Sciences, China

[2] University of Chinese Academy of Sciences, China

Corresponding author: Jin Zhang, ejzhang@mail.iee.ac.cn

Speaker: Hao Jin, jinhao97@mail.iee.ac.cn

Abstract

Power cycling (PC) is one of the most important tests for power semiconductor reliability since it is particularly effective in verifying the reliability of chip bond-wire and chip solder layer. The target experimental parameters of PC test are junction temperature (T_j) fluctuation and the maximum T_j (T_{j_max}). Most of the current PC equipments operate by manual adjustment of test parameters in order to keep the experimental conditions as close as possible to the target values. In this paper, a novel computing method of SiC MOSFET power cycling test parameters was introduced. The proposed method extracted Foster model thermal network parameters based on the cooling curve of SiC MOSFET, and then calculated the most suitable heating time, heating power and cooling plate temperature for the devices under test (DUTs) based on the thermal network. Experimental results showed that the proposed method greatly improved the test efficiency and junction temperature measurement accuracy.

Keywords: SiC MOSFET, power cycling test, thermal network, automatic optimization

1 Introduction

With the development of power electronics technology, the wide band-gap semiconductor devices represented by SiC(silicon carbide) MOSFETs (metal oxide semiconductor field-effect transistors) have gradually entered the electric vehicle industry. Compared with traditional Si IGBTs (insulated-gate bipolar transistor), SiC MOSFETs have the advantages of high voltage, low loss, high thermal conductivity and high switching frequency.

However, due to the defects of the materials and the immaturity of the manufacturing process, there is still a gap in reliability between SiC devices and Si devices.PC is an important part of power devices reliability test.The traditional PC equipment needs to manually select the experimental conditions of PC test to meet the temperature requirements of the experiment, which will occupy a lot of time of the experimental personnel and may cause low temperature accuracy. In this paper, a novel computing method of power cycling test parameters was proposed.

2 Device Thermal Network Parameter Extraction Algorithm

The AQG324 standard clearly states that thermal resistance needs to be measured without removing the device, and a 20% increase in thermal resistance is used as the failure criterion. Therefore, it is necessary to integrate the thermal resistance measurement function into the system. Most of the existing commercial PC test equipment does not have thermal resistance test function, and only takes 20% increase in the fluctuation of T_j(ΔT_j) as the failure criterion. PC test equipment with integrated thermal resistance test function can only calculate the thermal resistance from junction to ambience, or use the heatsink temperature as the case temperature to calculate the junction to case thermal resistance, which causes inaccuracy to determine the aging state of the device connection interface. During the PC test, the thermal grease ageing often occurs, which reduces the heat dissipation performance from the device substrate to the heatsink, and externally manifests itself as an increase in the thermal resistance of the thermal grease layer, but in reality, the device itself is not degenerating. In this paper, we proposed a novel algorithm in the PC test system to identify the 8th order Foster and Cauer thermal network model without removing the devices, and extract the junction to case thermal resistance for the determination of thermal resistance failure and subsequent implementation of the junction temperature active optimization function.

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2.1 Thermoelectric Comparison Theory

In the thermoelectric comparison theory, current corresponds to heat power, voltage difference is analogous to temperature difference, resistance corresponds to thermal resistance, and capacitance is equivalent to thermal capacity.[1][2] The heat dissipation pattern of most power electronic devices with single-path heat dissipation can be characterized using the Cauer model[3], whose thermal network model can be represented by Fig.1.

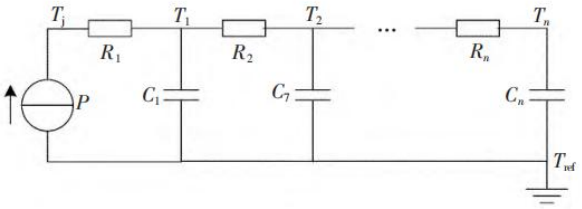

Fig.1. Cauer thermal network equivalent thermal circuit diagram

The general SiC MOSFET module heat dissipation structure from junction to case is SiC chip, chip solder layer, DBC (upper copper, ceramic plate, lower copper), base plate solder layer and lastly the base plate, i.e. the case. After the device is installed on a heat sink, thermal grease and heat sink will also be added to the heat transfer path. In Cauer model each geometric layer corresponds to one order of the RC thermal network. In general, the structure from the chip to the heat sink will not exceed 8 layers, so the thermal network parameters was calculated based on the 8th order thermal network model.

The Cauer model is a simplification based on actual physical theory and has actual physical meaning. The thermal resistance in each layer of the RC network is to the same reference point thermal resistance, which leads to the device cooling curve, i.e., the zero-input response curve expressed in terms of the Cauer model parameters is very complex both from the time and frequency domains, so it is very impractical to calculate the Cauer model thermal network directly from the device junction temperature cooling curve.

As shown in Fig.2, the Foster model consists of n-order RC parallel structures connected in series, which makes the calculation very easy. The drawbacks of the Foster thermal network model are also obvious, as it has no real physical meaning and it is not possible to calculate the temperatures of each layer since each layer of its RC parallel structure does not correspond to the actual structure. Despite the limitations, the Foster model is identical to the Cauer model for the calculation of junction temperatures and can be used to simplify the thermal networks fitting.

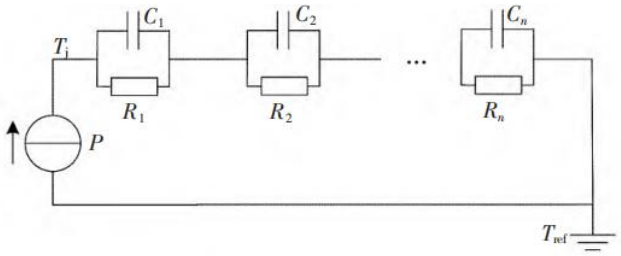

Fig.2. Foster thermal network equivalent thermal circuit diagram.

2.2 Algorithm for Extracting Thermal Network Parameters

As a conventional method, the structure function was commonly used for extracting the thermal network parameters based on the device cooling curve. The concept of structure function was first proposed by V. Szekely et al[4]. This method is based on a series of mathematical operations on the transient thermal response curve, and ultimately obtains a structure function that contains the thermal parameters of each layer of the power device. The whole process of calculating the thermal network model using the structure function method mainly includes four steps: measurement of the thermal transient response curve, deconvolution operation, discretization of the time constant spectrum, and conversion of the Foster and Cauer network mode[5], as shown in Fig.3.

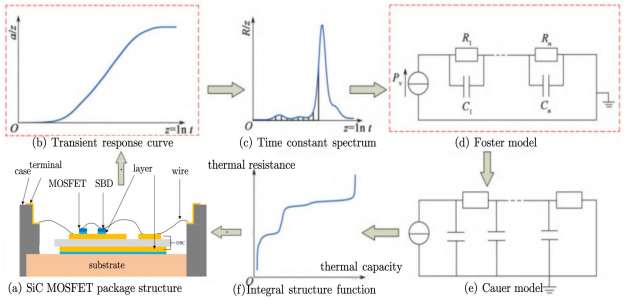

Fig.3. Analysis of thermal network models of device using the structure function method

This calculation process is cumbersome and the result is an integral structure function as shown in Fig.3(f), which cannot identify the thermal resistance of each layer. In order to determine the thermal resistance of the crust, the double interface method is generally used to test and the structure function method is used to calculate.

The dual-interface method needs to change the thermal structure of the device by adding and removing thermal grease when mounting the device, and the integral structure function is calculated by the structure function method for two different heat dissipation conditions. Then the separation point of the two structure function curves is used to determine the thermal resistance. Since it is clearly stated in the AQG324 standard that the device cannot be removed

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for thermal resistance measurement, the dual-interface method is obviously not permissible for PC testing.

In this paper, we use MATLAB's built-in nonlinear fitting function “1sqcurvefit” to fit the relevant parameters of Foster thermal network, and the advantage of this method is that it can directly identify the parameters of the thermal network at each layer.

$$T(t) = P\sum_{i=1}^{n} R_{th,i}\left(1 - e^{\frac{-t}{\tau_i}}\right) \quad (a)$$

$$Z_{th}(t) = \sum_{i=1}^{n} R_{th,i}\left(1 - e^{\frac{-t}{\tau_i}}\right) \quad (b)$$

A heating current I_{load} is first injected into the device to heat the device to steady state. After switching off I_{load}, the T_j cooling curve is measured by a small current body diode voltage as TSP(Temperature sensitive parameter). The extracted temperature drop curve conforms to the transient response of the heat source temperature expressed by equation(a). Equation(a) shows the thermal response of the equivalent thermal circuit of the Foster model to the heating power excitation of the device, and the transient thermal resistance of the corresponding thermal network of the Foster model can be expressed by equation(b), where $R_{th,i}$ is the thermal resistance of each layer of the Foster network, τ_i is the time constant of each layer of the RC network, and P is the heating power. In this paper, the iterative fitting of the Foster thermal network was carried out directly using MATLAB's built-in nonlinear fitting function “1sqcurvefit”, which is essentially a nonlinear curve fitting solved by the least square method. In order to obtain the thermal network model parameters with practical physical significance, it is necessary to calculate the Cauer network model parameters.

The whole process of using “1sqcurvefit” function to calculate the thermal network model of the device mainly includes four steps as shown in Fig.4: measuring the thermal transient response to the cooling curve, using the $\sqrt{t}$ method to fit the front end of the cooling curve, using “1sqcurvefit” function to fit the Foster thermal network and conversion from the Foster model to the Cauer model.

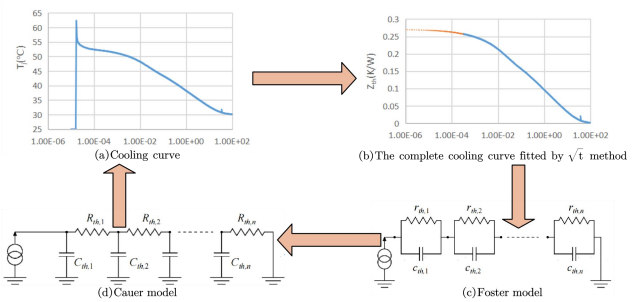

Fig.4. Analysis of thermal network models of device using the “1sqcurvefit” function

The specific steps are as follows:

(1) Measure the device cooling curve with a temperature rise of not less than 50°C.

(2) Fit the cooling curve by $\sqrt{t}$ method. In the case of Si devices, the recommended fitting interval is 500μs to 1000μs, but in the case of SiC devices, the recommended fitting interval is 200μs to 600μs.

(3) The fitted complete cooling curve is symmetric with the ramp-up curve shown in equation(a) based on the average junction temperature, and the zero-input response pair of the cooling curve complies with equation (c):

$$T(t) = P\sum_{i=1}^{n} R_{th,i}e^{\frac{-t}{\tau_i}} \quad (c)$$

(4) Given that the lower limit of all parameters is 0 and the upper limit of all thermal resistances is $R_{th,j\text{-}s}$, the iterative initial value of the thermal resistance of each layer of the device is set to $R_{th,j\text{-}s}/8$. According to many tests the Foster model thermal capacity of the internal structure of the device is below 10, so one is used as the initial value. The number of iterations is set to 1000, and the relevant parameters of the Foster thermal network are fitted using the nonlinear fitting function “1sqcurvefit”.

(5) To facilitate the Foster to Cauer model conversion, the discrete Cauer thermal network model of the device is first obtained by performing the Laplace transform of the time-domain analytical equation of the Foster thermal network, and then applying the polynomial division alternating between the numerator and the denominator, and the transformation result is in the form of equation(d).

$$Z(s) = \sum_{i=1}^{n} \frac{r_i}{1+s\tau_i} \quad (d)$$

(6) Derivation of equation(d) into the form of equation(e) by multiple polynomial divisions.The obtained R_i and C_i are the parameters of each layer of the Cauer model thermal network.

$$Z(s) = \frac{p_{n-1}s^{n-1}+p_{n-2}s^{n-2}+\ldots+p_0}{q_n s^n+q_{n-1}s^{n-1}+\ldots+q_1 s+q_0}$$

$$Z(s) = \cfrac{1}{(q_n/p_{n-1})s+\cfrac{q^*_{n-1}s^{n-1}+\ldots+q^*_1 s+q^*_0}{p_{n-1}s^{n-1}+p_{n-2}s^{n-2}+\ldots+p_0}}$$

$$Z(s) = \cfrac{1}{(q_n/p_{n-1})s+\cfrac{1}{p_{n-1}/q^*_{n-1}+\cfrac{p^*_{n-2}s^{n-2}+p^*_{n-3}s^{n-3}+\ldots+p^*_0}{q^*_{n-1}s^{n-1}+\ldots+q^*_1 s+q^*_0}}}$$

$$Z(s) = \cfrac{1}{C_1 s+\cfrac{1}{R_1+\cfrac{1}{C_2 s+\cfrac{1}{R_2+\cfrac{1}{\ldots \\ C_n s+\cfrac{1}{R_n}}}}}} \quad (e)$$

Taking an Infineon FF6MR12KM1 SiC MOSFET module as as an example, the 4th order Foster model transient thermal impedance given in the technical specification for this module is shown in Fig.5.

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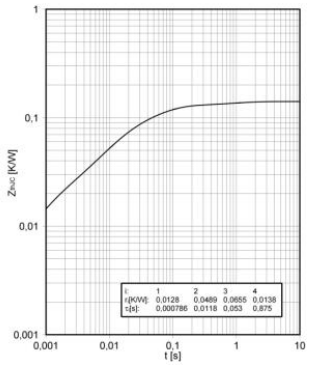

Fig.5. Transient thermal impedance of FF6MR12KM1

The calculation results of the 8th order Foster thermal network model using the proposed method are shown in Table1.

Table1 FF6MR12KM1 Foster thermal network model calculation results

Order i	r_i	τ_i
1	6.04E-02	2.87E-02
2	4.92E-02	6.54
3	3.49E-02	7.90E-01
4	2.79E-02	4.69E-03
5	1.93E-02	1.38E-01
6	9.03E-03	2.64E-04
7	5.61E-03	9.16
8	2.08E-03	1.82E-07

As shown in Figure 6, the calculated parameters of Foster model were put into equation (c) to obtain the theoretical junction temperature cooling curve.

As can be seen from the figure, the zero-input response of the fitted Foster model thermal network parameters matches very well with the original measured data and can be used as a basis for calculating the Cauer model parameters and for subsequent implementation of the junction temperature auto-optimization function.

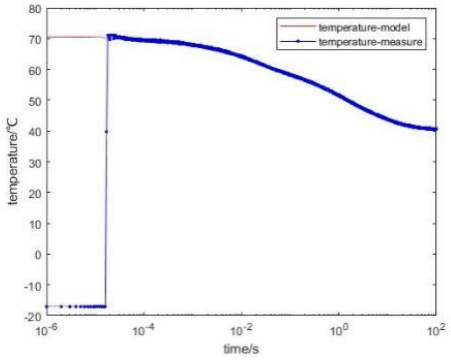

Fig.6. Zero input response of Foster thermal network model compared with measured data

Afterwards, the Foster-Cauer thermal network parameters are transformed using step (6), and Table 2 shows the calculated results of the transformed Cauer thermal network model.

Table2 FF6MR12KM1 Cauer thermal network model calculation results

Order i	R_i	C_i
1	2.10E-03	8.70E-05
2	1.37E-02	2.35E-02
3	4.69E-02	1.09E-01
4	3.85E-02	4.89E-01
5	2.58E-02	7.10E+00
6	3.19E-02	2.10E+01
7	3.89E-02	1.39E+02
8	3.46E-04	2.58E+04

Fig.7 shows the differential structure function curves calculated using the traditional structure function method. The red dashed line is the thermal resistance boundary of each layer structure calculated by this method. The junction to case thermal resistance calculated by dual interface method is 0.125K/W. It can be seen from the Table 2 that the thermal resistance value calculated using the proposed method is 0.127 K/W as of layer 5 and the calculation error of the two methods is less than 10%.Therefore, the method proposed in this paper can be used to perform PC testing without removing the device to identify the junction-to-case thermal resistance.

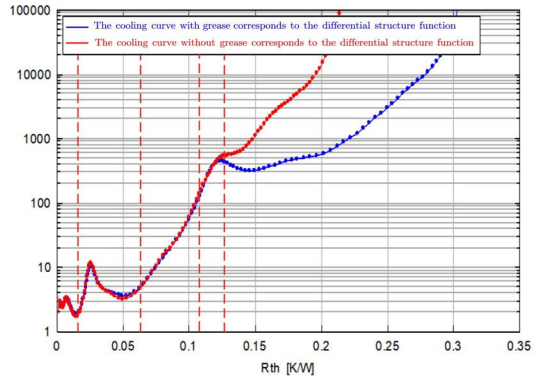

Fig.7. Differential structure function curves

The shortcoming of the proposed method is that it is impossible to accurately determine how many orders of thermal networks correspond to the junction-to-case thermal resistance. The feasible solution given in this paper is to measure the thermal resistance of the device by the dual interface method before the PC test. After starting the test, we can observe the Cauer model thermal network calculated by the system at which order is the closest to the result calculated by the dual-interface method to judge the

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structure of the device and provide a reference for the identification of thermal resistance during the subsequent PC test.

3 Automatic Optimization Strategy of Junction Temperature

The main target experiment parameters of PC test are the maximum and difference of junction temperature. The experiment parameters that can be controlled are heating time, cooling time, aging current and temperature of cooling plate. Currently, most commercial PC test equipment needs the operator to adjust controllable parameters manually to make the experiment condition approach the target parameters as close as possible. This process is highly dependent on the experience and ability of the testers. For an experienced operator, the time of adjusting is about 20~30 minutes. At the same time, manual adjustment still cannot achieve high accuracy. In actual operation, the accuracy of manually adjusted junction temperature is about ±5°C. Though ±5°C do not have much influence on aging test, higher precision of junction temperature adjusting is beneficial for the standardization of the experiment and may promoting the development of testing standard. What's more, manual adjustment can't guarantee the PC cycle period is theoretical minimum, which increase the total time and decreases the efficiency of experiment. This article realized the computation of the best testing cycle of DUTs basing on the above mentioned Foster thermal network extracting algorithm.

3.1 Basic Principle of the Computation

The typical temperature change during the PC test is shown in Fig. 8.

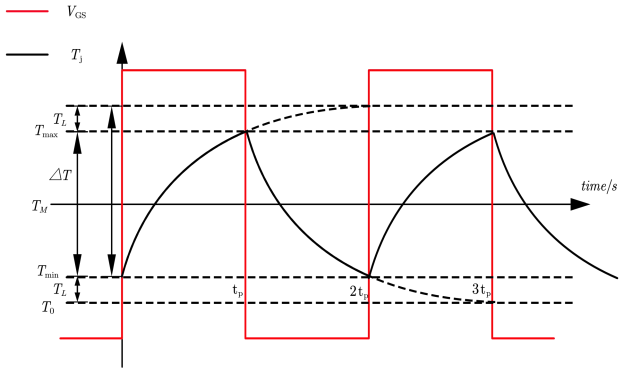

Fig. 8. Temperature change during PC test

The red line in Fig. 8 denotes the gate bias. When V_{GS}>0, the DUT is turned on and the heating current flows into the DUT. When V_{GS}<0, the DUT is turned off and the DUT cools down. The black solid line represents the practical fluctuation of T_j. The black dotted curve shows how the T_j of device changes till steady state when heating or cooling without switching conditions. While the black dotted straight line is the steady-state value of T_j without switching conditions. The controllable conditions in the test contain heat sink temperature T_0, heating power P and heating/cooling pulse width time t_p. Target conditions are T_{jmax} and the fluctuating value of T_j (ΔT_j). The controlling strategy is minimizing the pulse width time t_p with target conditions satisfied to improve the efficiency of experiment. In addition, T_M denotes the average of T_j, T_{min} represents the minimum of T_j and T_L denotes the difference of steady-states values of T_j either switching circuit conditions or not.

The heat dissipation path of device can be seen as a Foster thermal network model where 8-order RC parallel structures connect in series. According to the rules of RC oscillating circuit, the heating curve and the cooling curve are symmetrical on the average T_j. The temperature change of each layer accords with Fig. 8 as well, and its structure is simple RC parallel structure. The total change of T_j is the accumulation of the actual temperature change of each layer. Hence, when each layer is seen as object of study, its temperature fluctuation is shown as follows. The thermal network parameters r_i、τ_i in the process of computing are both based on Foster model.

$$T_{maxi} = T_{Li} + (\Delta T_i + T_{Li})(1 - e^{-\frac{t_p}{\tau_i}}) + T_{0i}$$

and

$$Pr_i = \Delta T_i + 2T_{Li}$$

$$T_{maxi} = T_{Li} + (Pr_i - T_{Li})(1 - e^{-\frac{t_p}{\tau_i}}) + T_{0i}$$

$$T_{maxi} = T_{Li}e^{-\frac{t_p}{\tau_i}} + Pr_i(1 - e^{-\frac{t_p}{\tau_i}}) + T_{0i}$$

$$T_{maxi} = T_{Li}e^{-\frac{t_p}{\tau_i}} + 2 \times \frac{1}{2}Pr_i(1 - e^{-\frac{t_p}{\tau_i}}) + T_{0i}$$

$$T_{maxi} = T_{Li}e^{-\frac{t_p}{\tau_i}} + \frac{1}{2}Pr_i(1 - e^{-\frac{t_p}{\tau_i}}) + \frac{1}{2}(T_{maxi} + T_{Li} - T_{0i})(1 - e^{-\frac{t_p}{\tau_i}}) + T_{0i}$$

$$(\frac{1}{2} + \frac{1}{2}e^{-\frac{t_p}{\tau_i}})T_{maxi} - (\frac{1}{2} + \frac{1}{2}e^{-\frac{t_p}{\tau_i}})T_{Li} - (\frac{1}{2} + \frac{1}{2}e^{-\frac{t_p}{\tau_i}})T_{0i} = \frac{1}{2}Pr_i(1 - e^{-\frac{t_p}{\tau_i}})$$

$$(1 + e^{-\frac{t_p}{\tau_i}})\Delta T_i = Pr_i(1 - e^{-\frac{t_p}{\tau_i}})$$

Total fluctuation of T_j is the accumulation of the temperature fluctuation of each layer, as shown in equation (f):

$$\Delta T_i = Pr_i \frac{1 - e^{-\frac{t_p}{\tau_i}}}{1 + e^{-\frac{t_p}{\tau_i}}} \quad (f)$$

The maximum of T_j is shown as follows:

$$T_{jmax} = T_M + \frac{1}{2}\Delta T_j$$

$$T_{jmax} = T_0 + \frac{1}{2}P\sum_{i=1}^{n} r_i + 1/2\Delta T_j$$

The cumulative thermal resistance of each layer is

the thermal resistance from junction to environment $R_{th,j\text{-}s}$.

$$T_{jmax} = T_0 + \frac{1}{2}PR_{th,j-s} + \frac{1}{2}\Delta T_j \qquad (g)$$

In the PC test system, the pulse width t_p can be calculated by equation (f) according to the power P, the thermal resistance of the Foster model calculated in section 2 and the target junction temperature fluctuation, and then the cooling water temperature T_0 can be calculated by equation(g).

3.2 Automatic Optimization Procedures

Before starting to adjust the junction temperature, the rated current of the device, the minimum pulse duration time of the PC, the target ΔT_j, and the target T_{jmax} should be conformed.

To calculate the experimental parameters, the Foster thermal network model of the device should be calculated first.

The cooling water temperature is adjusted to room temperature, such as 20°C, and the device is heated with 75% of the device's rated current as I_{load}. This current value is the system default, and the heating current can be manually adjusted according to the device. The purpose of the heating current setting is that the steady-state junction temperature of the device cannot exceed the set maximum junction temperature and the temperature rise is greater than 60°C. After heating the device for 100 seconds, the circuit is switched to cooling for 2 seconds, and the cooling curve is measured at the same time. The heating time and cooling time can also be manually adjusted, but it needs to be long enough to make the device junction temperature stable. After the data acquisition is completed, the $\sqrt{t}$ method is used to fit the front end of the cooling curve, and the non-fitting part is filtered with 100Hz point-by-point low-pass filtering to make the curve smoother.

Due to the influence of temperature on heat capacity, the measured thermal network model cannot accurately meet the heat network corresponding to the maximum junction temperature of the PC test. Therefore, in this paper, the maximum junction temperature adaptation function is added to the calculation procedure of the thermal network, and the maximum junction temperature when calculating the thermal network meets the set value by gradually adjusting the heating current.

The second step is measuring the heating power of the device at I_{load} and T_{jmax}. The water temperature is adjusted to T_{jmin} and the device is heated with the current I_{load}. At this time, the device is heated to pulse mode. That is, after 200 ms heating, the circuit is switched to a cooling state for 5ms to measure the real-time junction temperature. At the cycle when the junction temperature has just risen to the maximum junction temperature, the heating power P is calculated by the voltage drop at both ends of the DUT during heating and the I_{load}.

The third step is to calculate the test pulse width t_p and cooling water temperature T_0 corresponding to the current experimental conditions by equation (g), and compare the calculation results of the junction temperature with the set minimum pulse width time of PC test.

If the calculation result is greater than or equal to the set minimum pulse width time of the PC, set the pulse duration of the PC test to t_p. If the calculation result is less than the set minimum pulse width time of PC test, the second and third steps are repeated until the calculated result is greater than or equal to the set minimum pulse width time of the PC test.

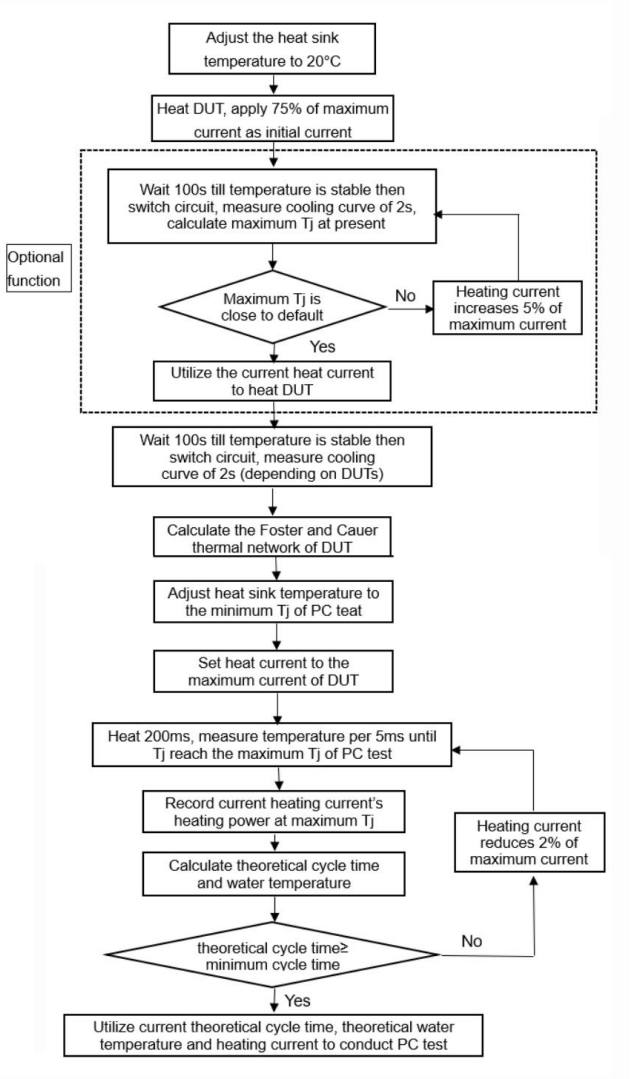

Fig. 9 The automatic adjustment process

At this time, the heating current, pulse width time, and cooling water temperature are the experimental conditions for the formal PC test.

The individual difference of SiC MOSFET devices is greater than that of Si IGBT, there may be some devices with slight deviation from the actual junction temperature set value.However the thermal network

parameters of the same batch of devices are generally consistent.
In this case, by appropriately adjusting the gate voltage of the corresponding device, according to equation (h),

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{OX}(V_G - V_{th})} \quad \text{(h)}$$

By decreasing the gate voltage, the channel resistance of the device increases, and then the drain-source on-state resistance and the heating power increase. After adjusting the gate voltage to ensure that the junction temperature of all devices meets the test requirements, the PC test begins. As a general rule, you cannot change the test conditions after the test has started. Fig.9 shows the whole procedures of automatic optimization and adjustment process.

3.3 Experimental Results

The Wolfspeed SiC MOSFET modules WAB300M12BM3 were used to validate the effect of the proposed automatic optimization strategy for PC test parameters, and the experimental results are shown in Table 3. After setting a series of preset conditions, the system automatically completes the calculation, and the error of T_j was within ±2°C. If the time spent waiting for the cooling plate temperature to stabilize was not taken into account, the automatic optimization and adjustment process of the junction temperature only took 5 minutes. Experimental results showed that the algorithm had good results and the accuracy met the requirements of PC testing.

Table 3 Objective and result of automatic optimization of junction temperature

parameter	set value	real value
maximum T_j	150°C	151.8°C
minimum T_j	70°C	69.11°C
aging current	≤300A	283A
cycle time	≥2s	2s
T of cooling water	none	34°C

Moreover , unlike the manual adjusting of the t_{on} step time of 1s, the automatic optimization strategy in this paper can adjust the t_{on} to the accuracy of 0.1s, which minimizes the time of each cycle and increase testing efficiency. For example, if the maximum aging current was adjusted to 270A, the calculated PC test cycle was 2.3s and the aging current was 270A. However, if manually adjusted, the testing cycle would usually be set to 4s and the heating current can only reach 250A. The experimental results proved that the calculating the PC test conditions by the automatic optimization strategy in this paper can maximize the overall PC test efficiency.

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