

Design of a High-Efficiency Single-Stage Series Resonant Micro-Inverter

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Abstract

This paper shares the design of a high-efficiency single-stage series resonant micro inverter used for domestic photovoltaic (PV) systems. The First Harmonic Analysis (FHA) model of the system is first established. An analytical modulation scheme of small root-mean-square resonant current, reliable full-range Zero Voltage Switching (ZVS), and small switching frequency variation range is proposed. Design indexes are proposed to further guide the selection of hardware parameters. By calculating the CEC weighted average of different indexes under different hardware parameters, the optimal hardware parameters are selected for optimal design. A loss estimation is conducted accordingly. Finally, a prototype is built and experimentally verified, exhibiting a peak efficiency of 96.23%, a CEC efficiency of 95.12%, and a power density of 34W/in³.

1 Introduction

Single-stage topologies are regarded as a promising solution for low-power microinverters for their lower cost, higher efficiency, and higher compactness. The High-Frequency-Link (HFL) type single-stage microinverter has the potential for a wide soft-switching range, high transformer utilization rate, and bidirectional power transfer. Therefore, HFL microinverter is gaining wide interest from both industry and academia[1], [2], [3], [4].

There's a series of variations of HFL microinverter. The two most distinctive differences among the variations are the grid side bridge type and passive components. For an HFL microinverter with an H-bridge on the grid side[5], 12 power switches are needed, making it too costly for a real product. However, if a half-bridge[6] is used instead, the switch count is reduced to eight, which greatly reduces the cost and improves the density. For a single inductor type HFL microinverter, ZVS is hard to achieve in all working conditions[7]. However, for a resonant type, full-range ZVS is possible in all working conditions with proper modulation[8]. Therefore, as shown in Fig.1., this paper focuses on the series resonant HFL microinverter with a half-bridge on the grid side. The resonant capacitor is integrated into the capacitor bridge.

Due to high control degrees of freedom, the inner behavior of a HFL converter is greatly affected by its modulation. Therefore, a proper design of the HFL microinverter is usually connected with its modulation. For the HFL DCDC converter, analytical modulation strate-

gies[9] can be used with clear expression and easy implementation. However, for resonant HFL inverters, due to high complexity, there's no analytical modulation yet, and the existing researches on the design of HFL micro inverters are mainly numerical modulation methods[8], [10], which relies heavily on precise hardware numeric and offline calculation, resulting in limited engineering deployment capability. Moreover, these researches mainly focus on optimizing the performance of a single or a few specific working points, which is unsuitable for microinverters, whose whole load-range performance (CEC efficiency, for example.) is regarded as more important than a single point's best performance.

Therefore, this paper proposes an analytical modulation strategy and proposes its hardware design method for a series resonant microinverter.

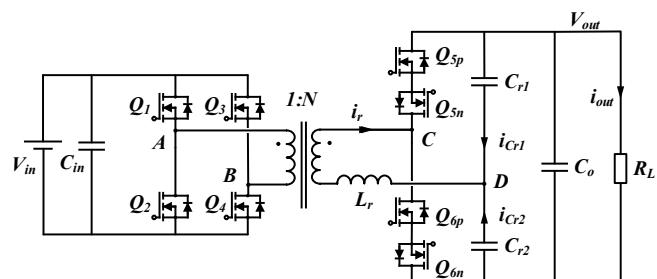


Fig. 1. The topology of the microinverter

2 System Modelling

As shown in Fig.1., the research subject of this paper is a single-stage series resonant microinverter. The input

is a 16~60V DC from the PV panels. The full power input voltage range is set as 36~45V. The output connects a 220V~240V 50Hz/60Hz AC for the grid through an EMI filter (not included in the figure, since it is not the concentration of this paper). The switches at the secondary side are the integration of a half-bridge and an unfolder. Q_{5p} and Q_{6p} work complementary in PWM mode when the output is positive, and remain on when the output is negative. Q_{5n} and Q_{6n} work similarly but oppositely. Fig.2. (a) shows the equivalent resonant circuit, where V_{X1} is the voltage of V_{AB} reflected at the secondary side, V_{X2} is the equivalent waveform of the secondary bridge after the split resonant capacitor is viewed as one, and $C_{r1}=C_{r2}=1/2C_r$. As shown in Fig.2. (b), the analysis based on the power flow can be done under First Harmonic Analysis (FHA).

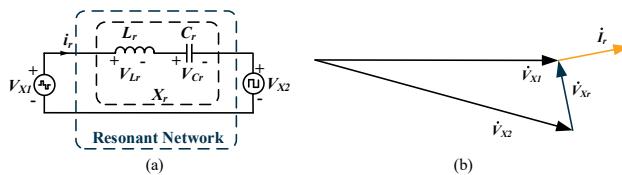


Fig. 2. (a) equivalent resonant circuit, and (b) phasor diagram

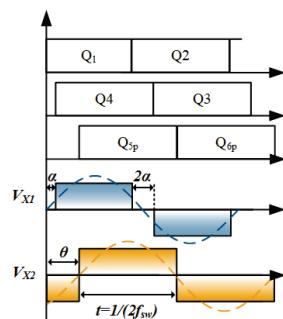


Fig. 3. Critical waves and the definition of the three control variables α , θ , f_{sw}

Therefore, after calculating the system parameters by circuit equations under FHA, the system can be modeled as Equation (1)~(11). The critical waves and the definition of the three control variables α , θ , and f_{sw} are shown in Fig.3.

$$M = \frac{\text{Amplitude}(V_{X2})}{\text{Amplitude}(V_{X1})} = \frac{V_{out}}{2NV_{in}} \quad (1)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (2)$$

$$V_{X1}(\omega t) = \frac{4V_{in}N}{\pi} \cos \alpha \sin \omega t \quad (3)$$

$$V_{X2}(\omega t) = \frac{4MV_{in}N}{\pi} \sin(\omega t - \theta) \quad (4)$$

$$f_{p.u.} = \frac{f_{sw}}{f_r} \quad (5)$$

$$X_r = \sqrt{\frac{L}{C}} (f_{p.u.} - 1/f_{p.u.}) \quad (6)$$

$$I_r(\omega t) = \frac{4V_{in}N}{\pi X_r} (-\cos \alpha \cos \omega t + M \cos(\omega t - \theta)) \quad (7)$$

$$P = \frac{8MV_{in}^2 N^2}{X_r \pi^2} \cos \alpha \sin \theta \quad (8)$$

$$P = \frac{V_{out}^2}{R_L} = \frac{4M^2 N^2 V_{in}^2}{R_L} \quad (9)$$

$$Q_z = \sqrt{\frac{L_r}{C_r}} / R_L \quad (10)$$

$$M = \frac{2}{\pi^2 Q_z (f_{p.u.} - 1/f_{p.u.})} \cos \alpha \sin \theta \quad (11)$$

$$I_{r_rms} = I_o \frac{\pi}{\sqrt{2}} \frac{\sqrt{M^2 - 2M \cos \alpha \cos \theta + \cos^2 \alpha}}{\cos \alpha \sin \theta} \quad (12)$$

3 Modulation Design

An analytical modulation was proposed by [11] for a DCDC series resonant DAB with an H-bridge on the second side. Similarly, to reduce the H-bridge scenario to a half-bridge one as (12), it can still achieve minimum reactive power (satisfies the minimum reactive power restriction, (13)) at below-unity system gain M and full range ZVS (satisfies the ZVS restriction, (14), which can be simplified as (15)) and minimum resonant current (satisfies the minimum current restriction, (16), which can be simplified as (17)) at any system gain M .

$$\begin{cases} \varphi = \begin{cases} \arccos(\sqrt{M}), & M \leq 1 \\ \arccos(\frac{1}{M}), & M > 1 \end{cases} \\ \alpha = \begin{cases} \varphi, & M \leq 1 \\ 0, & M > 1 \end{cases} \\ \theta = \begin{cases} \varphi, & M > 1.02 \text{ or } M < 0.96 \\ \arccos(\sqrt{0.96}), & 0.96 < M \leq 1.02 \end{cases} \end{cases} \quad (12)$$

$$Y = \frac{2}{\pi^2 M Q_z} \cos \alpha \sin \theta$$

$$f_{p.u.} = \frac{Y + \sqrt{Y^2 + 4}}{2}$$

$$\alpha \rightarrow \theta \quad (13)$$

$$\begin{cases} I_{r(\omega t=\alpha)} = \frac{4V_{in}N}{\pi X}(-\cos^2 \alpha + M \cos(\alpha - \theta)) \leq 0 \\ I_{r(\omega t=-\alpha)} = \frac{4V_{in}N}{\pi X}(-\cos^2 \alpha + M \cos(\alpha + \theta)) \leq 0 \\ I_{r(\omega t=\theta)} = \frac{4V_{in}N}{\pi X}(-\cos \alpha \cos \theta + M) \geq 0 \end{cases} \quad (14)$$

$$\begin{cases} \cos \alpha \geq \sqrt{M \cos(\alpha - \theta)} \\ \cos \alpha \cos \theta \leq M \end{cases} \quad (15)$$

$$\begin{cases} \frac{\partial I_{r_rms}}{\partial \alpha} = 0 \\ \frac{\partial I_{r_rms}}{\partial \theta} = 0 \end{cases} \quad (16)$$

$$\theta = \begin{cases} \arccos\left(\frac{M}{\cos \alpha}\right), M \leq 1 \\ \arccos\left(\frac{\cos \alpha}{M}\right), M > 1 \end{cases} \quad (17)$$

Therefore, modulation strategy (12) seems to have great potential to be used on the series resonant microinverter of this paper.

However, under such modulation, the converter works close to the ZVS boundary, making it hard to achieve reliable ZVS under real applications. Moreover, the variable switching frequency will become extremely large when the system gain is low and/or load low, making the modulation strategy impossible to work in AC conditions. To solve these problems, this paper proposes a modulation with two improvements. A margin angle is proposed to ensure reliable ZVS and a frequency limit strategy is proposed to have a lower switching frequency range.

$$\begin{cases} \varphi = \begin{cases} \arccos(\sqrt{M}), M \leq 1 \\ \arccos\left(\frac{1}{M}\right), M > 1 \end{cases} \\ \delta \text{ is a small angle, } \delta \in (0, 0.5\pi) \\ \alpha = \begin{cases} \varphi - \delta, \varphi > \delta \text{ and } M \leq 1 \\ 0, \varphi \leq \delta \text{ or } M > 1 \end{cases} \\ \theta = \begin{cases} \varphi + \delta, M > 1.02 \text{ or } M < 0.96 \\ \arccos(\sqrt{0.96}) + \delta, 0.96 < M \leq 1.02 \end{cases} \end{cases} \quad (18)$$

$$\begin{cases} Y = \frac{2}{\pi^2 M Q_z} \cos \alpha \sin \theta \\ f_{p.u.} = \frac{Y + \sqrt{Y^2 + 4}}{2} \end{cases} \quad (19)$$

$$f_{p.u.} = \begin{cases} f_{H_p.u.}, \text{ if } f_{p.u.} > f_{H_p.u.} \\ f_{L_p.u.}, \text{ if } f_{p.u.} < f_{L_p.u.} \\ f_{p.u.}, \text{ else} \end{cases} \quad (20)$$

$$\begin{cases} \gamma = \arcsin \frac{M \pi^2 Q_z (f_{p.u.} - 1/f_{p.u.})}{2 \cos \alpha} \\ \theta_{f_{lim}} = \begin{cases} \gamma, \gamma \geq \varphi + \delta \\ \pi - \gamma, \gamma < \varphi + \delta \end{cases} \end{cases} \quad (21)$$

A $f_{H_p.u}$ of 2.2 and $f_{L_p.u}$ of 1.1 is selected for calculation. According to (18)~(21), the relationship between control variables α , θ , $f_{p.u.}$ and working parameters Q_z and M can be illustrated in Fig. 4.

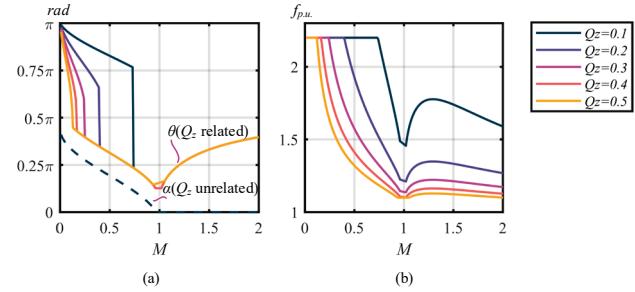


Fig. 4. The relationships for $\delta=0.2$ under different Q_z :
(a) α , θ and M , (b) $f_{p.u.}$ and M .

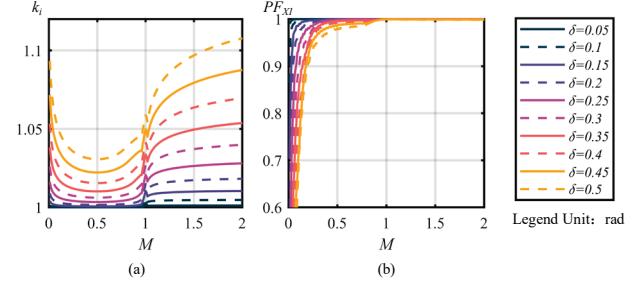


Fig. 5. The relationship between (a) k_i and M , and (b) PF_{X1} and M , under different values of δ .

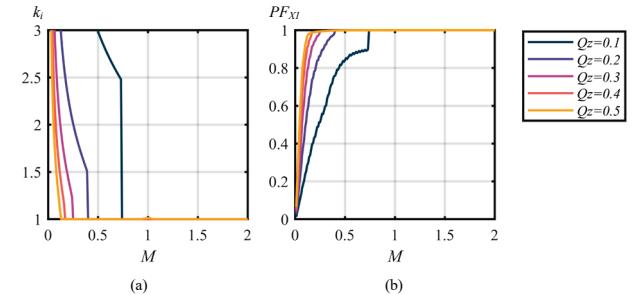


Fig. 6. When $\delta=0.2$, the relationship between (a) k_i and M , and (b) PF_{X1} and M , under different values of Q_z .

Define the coefficient k_i as the ratio of the resonant current RMS value after implementing the improvements to that of (12), and the power factor of the primary port of the resonant network PF_{X1} . Fig. 5. illustrates the relationship between k_i and M , and PF_{X1} and M , under different values of δ . Fig. 5. (a) reveals that when δ is relatively small, its impact on k_i is not significant. Fig. 5. (b) shows that when M approaches zero, the reactive power ratio introduced by δ increases, and the larger the δ , the greater the reactive power ratio. Similarly, Fig. 6. illustrates the relationship between k_i and M , and PF_{X1} and M , under different values of Q_z . It reflects that

the frequency limit strategy mainly worsens the circuit in light loads and small gains. It can be seen that it is a trade-off to accept higher-rms-current-caused loss to avoid non-ZVS loss and extremely-high-frequency-caused losses. Moreover, since the system power is small at a small M , the hardware, whose power capacity is designed for full power, will not have a lower utility rate. Therefore, the proposed modulation strategy is beneficial for the high-efficiency running and design of the proposed topology.

4 Hardware Design

4.1 Design Target

This paper uses the target in Table 1 as an example to better demonstrate the design process.

Table 1. Design Target

Target Name	Value
Full load input voltage	36V~45V
Rated input voltage	40V
Rated output voltage	240V 60Hz
Rated power	500W
CEC efficiency	≥95%
Power density	≥20W/in ³

4.2 Design Index

Define the primary current coefficient $k_{i_pri.}$, as (22), and the secondary current coefficient $k_{i_sec.}$, as (23), to evaluate the RMS values of the primary current I_{pri_rms} and the secondary current I_{sec_rms} in one fundamental cycle relative to the corresponding output current RMS value under each Q_z and N . Small $k_{i_pri.}$ and $k_{i_sec.}$ are needed for a good hardware design.

$$k_{i_pri.(Qz,N)} = I_{pri_rms(Qz,N)} / I_{o_rms(Qz)} \quad (22)$$

$$k_{i_sec.(Qz,N)} = I_{sec_rms(Qz,N)} / I_{o_rms(Qz)} \quad (23)$$

Define the frequency limiting coefficient $k_{f_lim.}$, as (24), which represents the proportion of the total duration t_{f_lim} in the frequency limiting region within one grid frequency cycle. Small $k_{i_pri.}$ and $k_{i_sec.}$ are needed for a good hardware design.

$$k_{f_lim.(Qz,N)} = t_{f_lim(Qz,N)} / T_{grid} \quad (24)$$

The voltage stress on the input and output filter capacitors is determined by operational conditions. The selection of capacitor models should be based on appropriate voltage ratings considering safety margins. The maximum capacitor voltage stress can be expressed as (25).

$$\begin{aligned} V_{C_max(N,Qz\max)} &= \\ \begin{cases} (\frac{1}{2} + \pi Q_{z\max}) V_{out_peak}, M_{peak_max} \leq 1 \\ (\frac{1}{2} + \pi Q_{z\max} M_{peak}) V_{out_peak}, M_{peak_max} > 1 \end{cases} \end{aligned} \quad (25)$$

in which $M_{peak_max} = V_{out_max} / V_{in_min}$

4.3 Design Process

According to the above analysis, a δ of 0.2, $f_{H_p.u.}$ of 2.2, and $f_{L_p.u.}$ of 1.1 are selected for reliable ZVS and reasonable switching frequency range.

The optimization analysis contains two parts. The first part is to calculate the target and limit values at any given N and Q_z for a whole base period. The calculation method divides the entire base frequency into multiple uniformly distributed calculation time points (e.g., 500 points). Between each calculation time point, all base frequency values can be treated as constant, while multiple switching periods occur between each time point. After collecting parameters at each time point, convert them to the base period value.

Table 2. CEC load weights corresponding to Q_z

m	$Q_{z[m]} (Q_{zmax}\%)$	$W_{z[m]}$
1	10	0.04
2	20	0.05
3	30	0.12
4	50	0.21
5	75	0.53
6	100	0.05

Table 3. CEC load weights corresponding to V_{in}

n	$V_{in[n]}$	$W_{V[n]}$
1	Full load minimum input voltage V_{in_min}	33.3%
2	Full load nominal input voltage V_{in_norm}	33.3%
3	Full load maximum input voltage V_{in_max}	33.3%

The second part is to calculate the CEC value of target values since the paper aims at microinverters for PV applications. For any given N and Q_{zmax} , 18 CEC calculation points (6 load points* 3 different input voltages) can be determined. By using the first part's methods, values of each point can be obtained. Average the value of different points at their corresponding CEC weight, the overall CEC value can be obtained. CEC values of k_{is} , k_{ip} , and k_f can be expressed as (26)~(28), respectively. The CEC points and weights are given in Tables 2 and 3.

$$k_{i_pri_CEC(Qz\max,N)} = \sum_{n=1}^{n=3} [W_{V[n]} (\sum_{m=1}^{m=6} W_{[m]} k_{i_pri.(Qz[m],N)}) @ V_{[n]}] \quad (26)$$

$$k_{i_sec_CEC(Qz\max,N)} = \sum_{n=1}^{n=3} [W_{V[n]} (\sum_{m=1}^{m=6} W_{[m]} k_{i_sec.(Qz[m],N)}) @ V_{[n]}] \quad (27)$$

$$k_{f_lim_CEC(Qz\max,N)} = \sum_{n=1}^{n=3} [W_{V[n]} (\sum_{m=1}^{m=6} W_{[m]} k_{f_lim.(Qz[m],N)}) @ V_{[n]}] \quad (28)$$

According to (25)~(28) and the design process, the system characteristics for each combination of $N \in [0 \sim 5]$, $Q_{z\max} \in [0 \sim 0.75]$ can be computed. The results are depicted in Fig. 7.

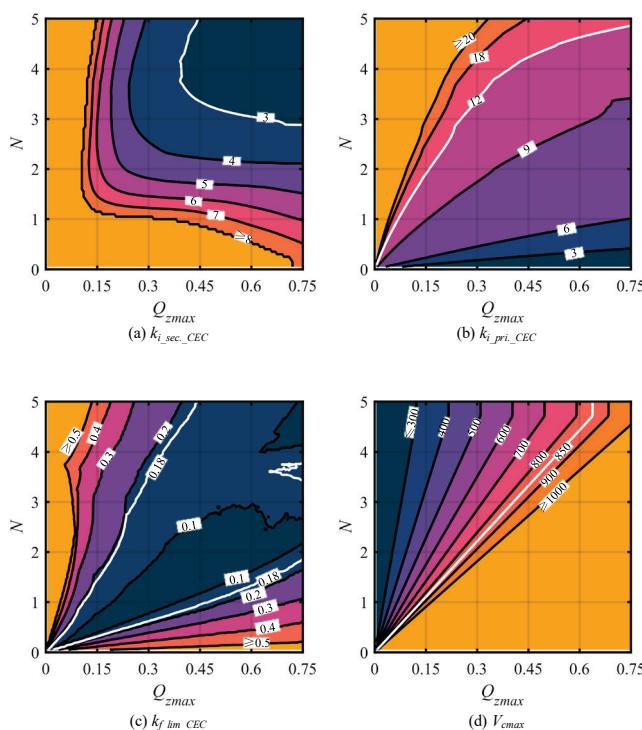


Fig. 7. (a) Secondary current coefficient, (b) Primary current coefficient, (c) Frequency limiting coefficient, (d) Voltage stress, under different N and $Q_{z\max}$.

Analyzing the results shown in Fig. 7., it is evident that different design indexes exhibit varying trends toward achieving optimal performance. Therefore, there is no single optimal N and $Q_{z\max}$ combination that simultaneously optimizes every design index. Thus, a balanced selection approach should be adopted, setting desired boundaries for each index. All combinations (N , $Q_{z\max}$) that surpass these boundaries collectively define the expected range for each index. By intersecting all expected ranges, a comprehensive optimization interval can be determined. Choosing a design point within this interval ensures that all objectives are optimized as expected.

The secondary side current target k_{is} is selected to be less than 3. The primary side current target k_{ip} is selected to be less than 12. The frequency limit ratio is k_f selected to be less than 0.18. The capacitor voltage stress is selected to be less than 850 Volts.

Therefore, different limit lines of the aforementioned target values can be drawn in a common N and Q_z graph as Fig. 8. The only region that satisfies all the targets is the white region. This paper chooses an N of 4 and a $Q_{z\max}$ of 0.4 as the final optimal design value.

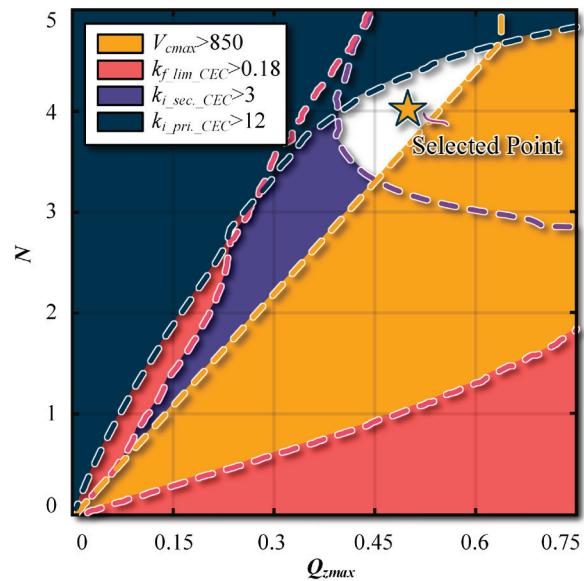


Fig. 8. Optimization result

Note that there are two important considerations in this process. Firstly, due to the proportional relationship between primary-side CEC current coefficient $k_{i_pri_CEC}$ and secondary-side CEC current coefficient $k_{i_sec_CEC}$, the desired boundaries for $k_{i_pri_CEC}$ and $k_{i_sec_CEC}$ should be chosen to maintain the turns ratio relationship at an equal optimization level. Secondly, not all arbitrarily specified expected ranges necessarily intersect. Therefore, the entire optimization process typically involves iterative adjustments to achieve a final and reasonable optimization outcome.

After the determination of N and $Q_{z\max}$, the real components can be designed. Considering the ability of magnetic materials 3C95, the lowest switching frequency limit f_L is selected as 100kHz. Therefore, according to a $f_{L_p.u}$ of 1.1, the resonant frequency f_r is 90.9 kHz. Combining f_r with the definition of Q_z (as in (12)) and the load at rated power, a C_r of 30 nF and L_r of 100 nH can be determined. Accordingly, the transformer and the inductor can be designed under the AP method, and switches can be selected for their current stress. EPC 2302 is selected for the primary side and GS66508T is selected for the secondary side.

5 Loss Analysis

An assessment of system losses is required to ensure that the hardware design and component selection meet the efficiency requirements outlined in Table 1. The basic approach for loss assessment aligns with the design process. The entire fundamental frequency is divided into multiple uniformly distributed calculation points (e.g., 500 points), with multiple switching cycles between each time point. By computing the losses at each time point and averaging them over the entire fundamental period, the overall system losses can be determined. This method[12] offers higher accuracy for nonlinear systems compared to conventional RMS estimation methods and ensures rapid and batch computation capabilities compared to calculations based on switch-level simulation software such as Spice.

Five different types of losses are considered. Due to the full range ZVS, turn-off loss, and conduction loss are considered in the type of switch loss (Sw. Loss). Core loss and copper loss are considered in the type of inductor loss (Ind. Loss) and the type of transformer loss (Trans. Loss). ESR loss of the input capacitor, which provides the second-harmonic energy for the inverter, is considered in the capacitor loss (Cap. Loss). An estimation of 2.5W is considered for the auxiliary circuits' loss (Aux. Loss). The calculated results are shown in Fig. 9. The efficiency satisfies the requirement.

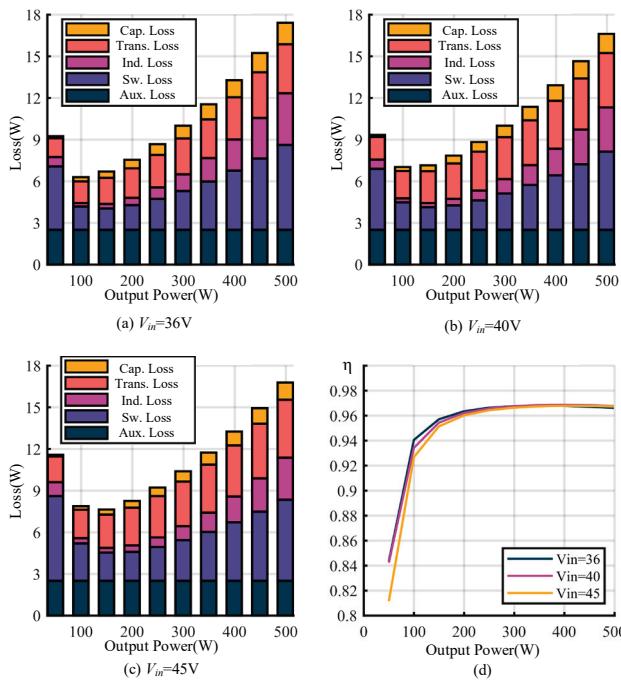


Fig. 9. Loss calculation result (a)36Vin, (b)40Vin, (c)45Vin, (d) Efficiency Curve

6 Prototype and Experiment

As shown in Fig. 10., a 500W prototype is built according to the design with a power density of 34W/in³.

Off-grid tests under different loads and different input voltages are made. The key waveforms are presented in Fig. 11 and Fig. 12. Full-range working is achieved, and all working conditions satisfy the ZVS restrictions (14). As Fig. 13., a peak efficiency of 96.23% and CEC efficiency of 95.12% is achieved. The test results verify the design of the series resonant microinverter.

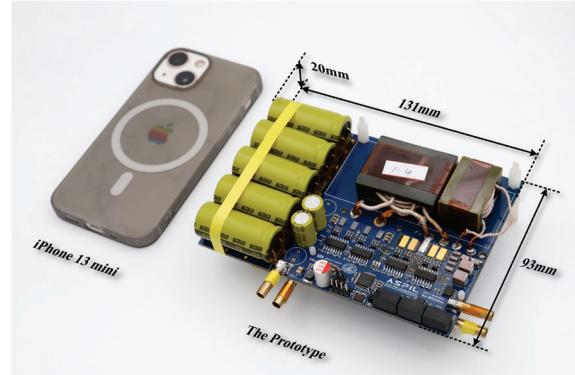


Fig. 10. The 500W Prototype

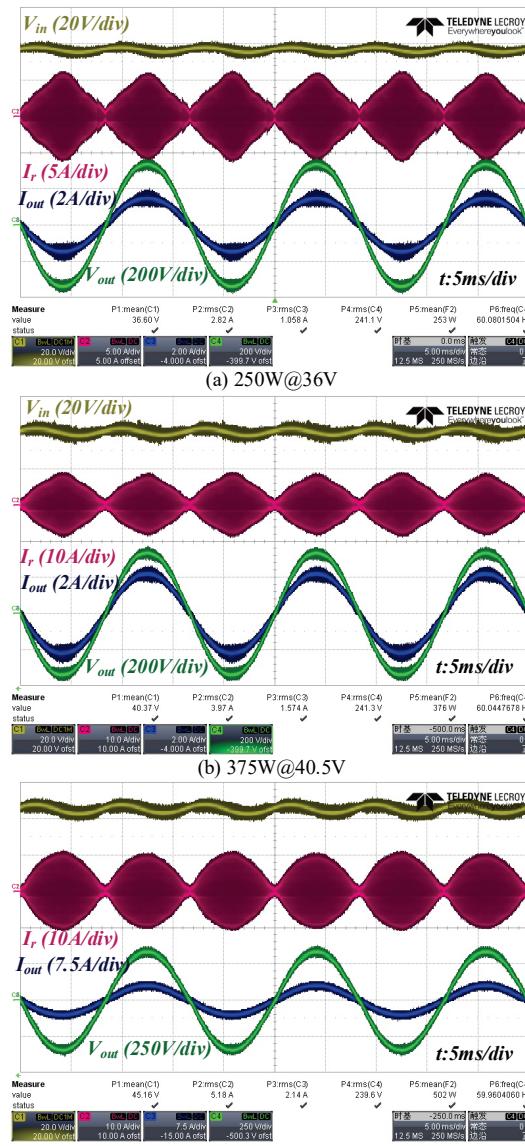


Fig. 11. Key Waveforms

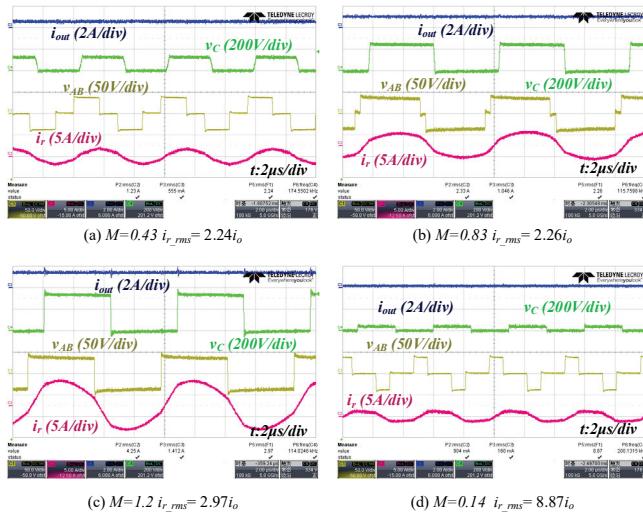


Fig. 12. Key waveforms of the resonant network and ratio of instantaneous currents under different M

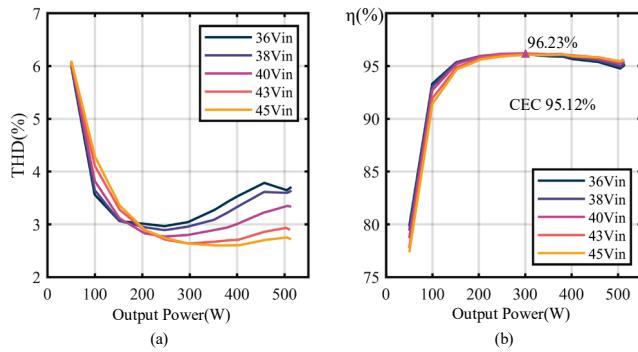


Fig. 13. Test Results (a) Voltage THD, (b) Efficiency

7 Conclusions

This paper shares the design of a single-stage series resonant microinverter. The model of the converter is first established under FHA. An analytical modulation strategy is proposed for full-range ZVS, small rms current, and low switching frequency variation range. Design indexes are analyzed and proposed for CEC conditions. Accordingly, hardware parameters of the best set of design indexes are determined and hardware is designed. After loss estimation, a 500W prototype of 34W/in^3 power density is built with a peak efficiency of 96.23% and CEC efficiency of 95.12%.

8 References

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