Gen.4 Trench SiC-MOSFET for Automotive Applications

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Abstract

This paper presents Gen.4 trench SiC-MOSFET for automotive applications. This structure is characterized by three injection layers.:the first is the protection of the trench Bottom P-well Region (BPW), the second is the sidewall connection region (SC) between p-well (PW) and BPW, and the third is the suppression of JFET Doping region (JD). With these new technologies, the Gen.4 trench SiC-MOSFET (Gen.4) achieves a remarkably low specific on-resistance (Ron,sp) of 1.9mΩcm^2.It achieves about 49% improvement in Ron,sp than conventional planar SiC-MOSFET. When we evaluated the power module with Gen.4, we confirmed that a power loss improvement of about 10% and the output capability of 350 kW or more could be obtained with multiple chips in parallel. These results show the Gen.4 is a suitable device for EV inverter, which require low loss and high output.

1 Introduction

In recent years, due to stricter automobile emission regulations and the introduction of preferential measures for eco-friendly vehicles, xEVs have gained significant popularity in the market. In this market environment, power modules used for electrification are increasingly required to be smaller in size and have larger capacity [1,2,3]. A good option to meet those demands is silicon carbide (SiC), which has remarkably superior characteristics as a power device, such as a wider band gap and higher breakdown electric field than conventional silicon (Si). We have been developing and mass-producing SiC-MOSFET and SiC-SBDs, and have supplied them into the market with a wide range of breakdown voltage levels, from 600 V for home appliance applications to 3.3 kV for electric railway applications[4]. The SiC-MOSFET are mainly classified into two types: trench type and planar type. Our planar SiC-MOSFET are characterized by lower loss than our competitors' planar products, but we will promote the development of a trench type that can be mounted with high integration to further improve performance.

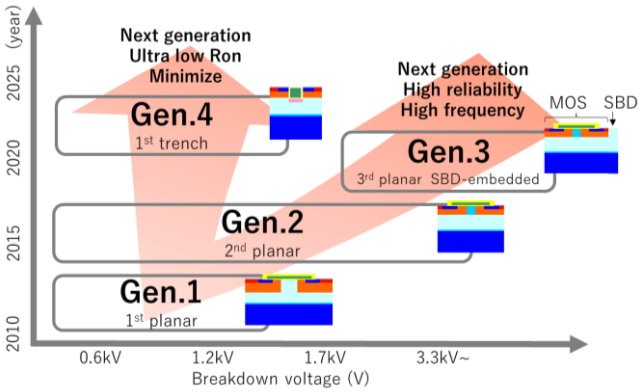
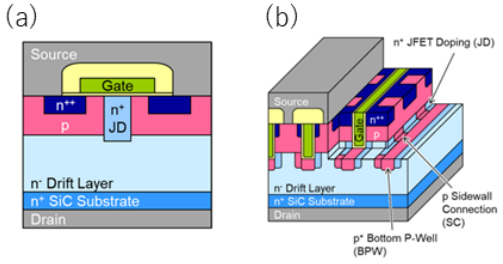


Fig. 1: Mitsubishi SiC-MOSFET technology

2 Chip technology

A structural comparison of the Gen.2 planar SiC-MOSFET (Gen.2) and Gen.4 is shown in **Fig. 2**. The trench-type structure enables narrower cell widths and denser cell layouts, but the risk of gate dielectric breakdown when high voltages are applied is higher than that of the planar type. In particular, strong electric field are concentrated at the corners of the trench bottom, causing breakdowns, so protection of the trench bottom gate dielectric is necessary to ensure high reliability. To solve this problem, we have developed Gen.4 which is characterized by mainly three injection layers is shown in **Fig. 3**. The three injection layers consist of a trench bottom p-type protection layer region (BPW), a sidewall connection region (SC), and a side JFET doping region (JD). BPW has the effect of mitigating the high electric field applied to the bottom of the trench. SC has the effect of discharging the charge accumulated in the electric mitigation layer to the source electrode. JD has the effect of setting up a high concentration layer on the side face of the trench that can easily be energized. In addition, Gen.4 uses a proprietary technology called tiled ion implantation, which allows it to be fabricated using a relatively simple process[5]. In the next chapter, we present the characteristics comparison of Gen2 and Gen4 which are evaluated with the chips.



(a) planar-MOSFET (b) trench-MOSFET

Fig. 2: Schamatic diagrams

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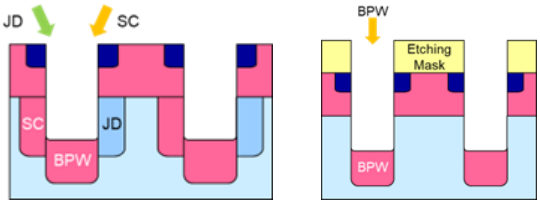


Fig. 3: The three injection layers

3 Chip Evaluation Result

3.1 Static Characteristic Result

A comparison of the V_{DS} (on) characteristics between Gen.2 and Gen.4 is shown in **Fig.4**. Gen.4 achieves a remarkably low specific on-resistance (Ron,sp) of 1.9mΩcm^2. It was confirmed that both at room temperature and high temperature, Gen.4 had lower Ron.sp than Gen.2. At room temperature, Gen.4 improved Ron,sp by about 49%, and at high temperature, Ron,sp was improved by about 30%.

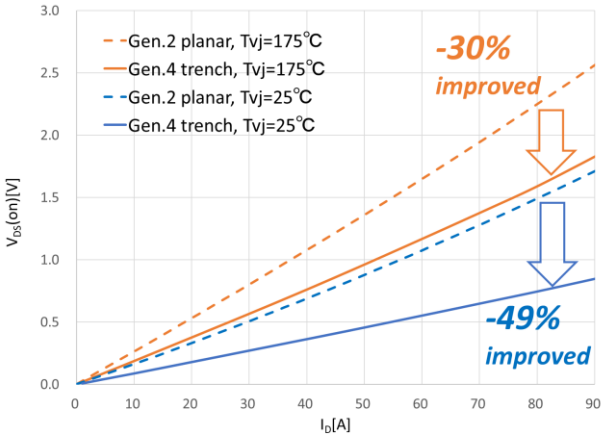


Fig. 4: V_{DS} (on) characterristics (R.T, 175℃)

3.2 Dynamic Characteristics Result

Table.1 compares the dynamic characteristics of the Gen.2 and the Gen.4. These characteristics are evaluated in specific condition Turn-ON at same di/dt_on(max) and Turn-OFF at same V_{DS} peak. Where the characteristics of Gen.4 is 29% increase than Gen.2. In the next chapter, we will investigate how the reduction of static characteristics and the increase of dynamic characteristics affect the actual operation of the EV inverter.

Table. 1: Dynamic Loss Results

Item	Unit	Planar-MOS	Trench-MOS
Turn-On			
didt(on)_max	[kA/μs]	3.7	3.7
Eon	[mJ/pulse]	2.5	3.5
Turn-Off			
Vdspeak	[V]	1014	1014
Eoff	[mJ/pulse]	0.6	0.9
Eon＋Eoff	[mJ/pulse]	3.1	4.4

4 Power Module Evaluation Result

4.1 Waveform and Loss Characteristics

Chapter 3 introduced the chip performance of Gen.4. In Chapter 4, we present the experimental results assuming actual inverter operation for EV inverter. The characteristics were evaluated using a power module with multiple Gen.4 mounted in parallel in a prototype package. Typical switching waveform (Tvj= 175°C) (**Fig. 5**), and loss characteristics (**Fig. 6**) are shown below.

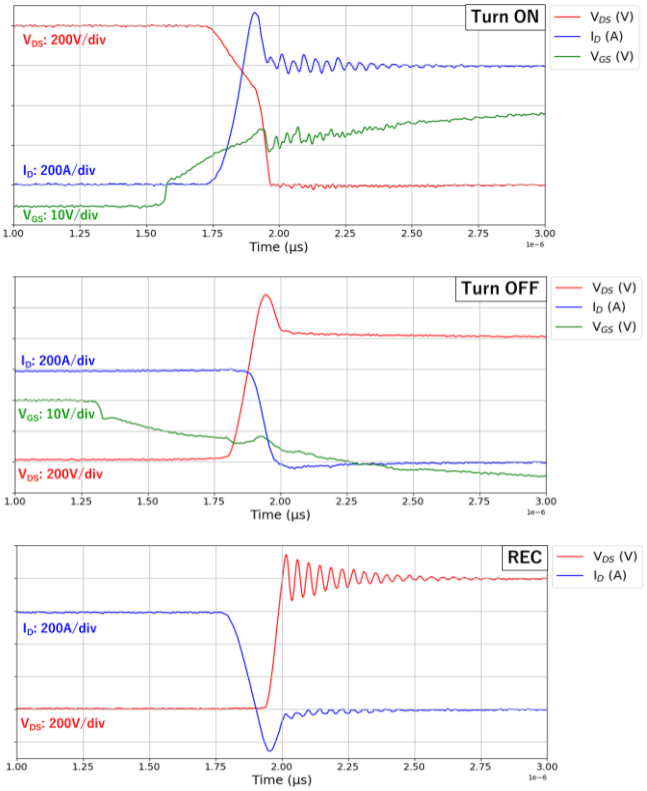


Fig. 5: Typical switching waveform (800V/600A,V_{GS} =20/-5V,T_{vj}= 175°C)

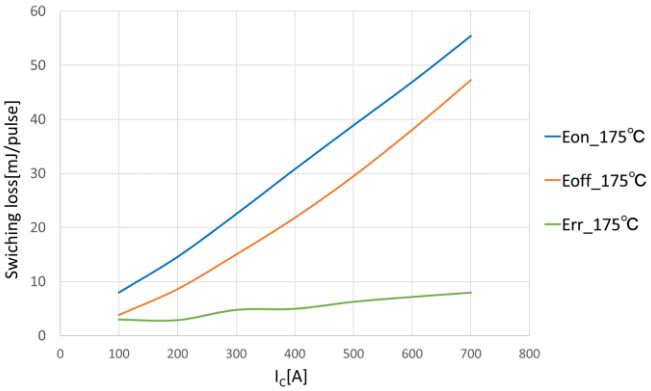
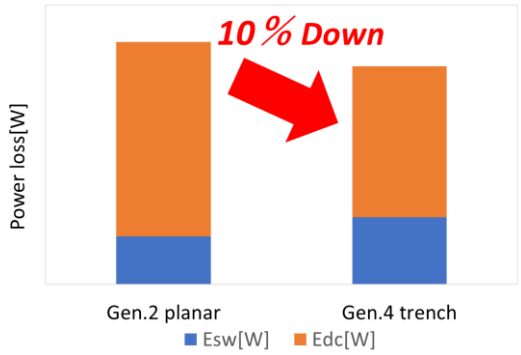


Fig. 6 Switching loss (V_{CC} =800V, V_{GS} =20V/-5V, T_{vj}= 175°C)

4.2 Comparison of Gen.4 and Gen.2

Compare the losses of Gen.4 and Gen.2 for EV inverter operation by simulation. When compared at 8 kHz, the carrier frequency most commonly used in automotive EV inverter, Gen.4 achieved a 10% loss reduction compared to Gen.2 (**Fig. 7**).



Vcc[V]	800
Irms[A]	700
Carrier Frequency[kHz]	8.0
Modulation Rate	1.0
Power Factor	0.85

Fig. 7: Gen.4 vs. Gen.2 power loss comparison

Next, we calculated the power loss for each carrier frequency to determine where the loss cross-point is for Gen.4 and Gen.2. A graph of the relationship between carrier frequency and power loss for Gen.4 and Gen.2 is shown in **Fig. 8**. The carrier frequency crosspoint was confirmed to be at 18 kHz. Gen.2 is used for applications in the high frequency range, such as OBC and boosters, while Gen.4 is used in the low frequency range, such as EV inverter. This differentiation of use based on the cross-point will enable product design with lower power loss.

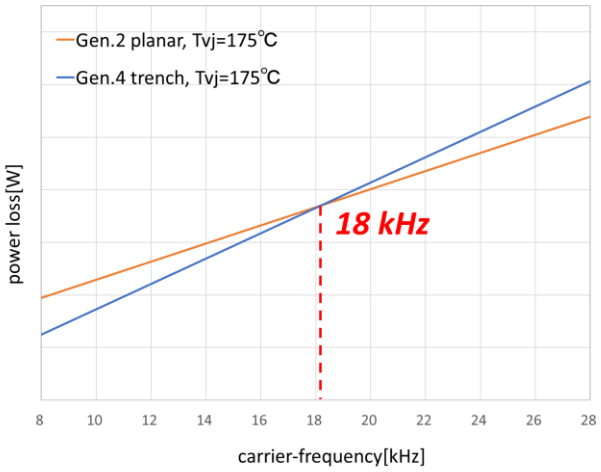


Fig. 8: Carrier frequency vs. power loss

4.3 Power module output capacity

The Power module with trench SiC-MOSFET was verified for its output capability when used as EV inverter. Inverter loss simulation was performed based on the characteristic results in Chapters 4.1 and 4.2, using the power module loss conditions at 175℃. **Fig. 9** shows the graph of output current vs. Tvj for each carrier frequency (fc=6kHz, 8kHz, 10kHz). The output is considered to be 350 kW at 700 Arms, although it depends on the operating environment of the motor. Therefore,the graph in **Fig. 9** shows that an output capacity of 350 kW or more can be obtained with multiple chips in parallel. The high current-carrying capability of trench SiC-MOSFET was also demonstrated.

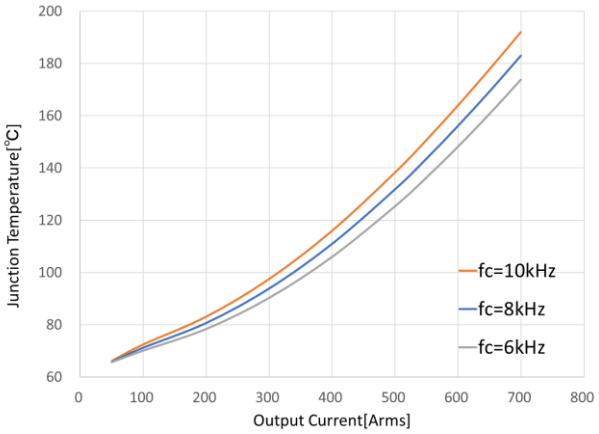


Fig. 9: Output current vs. Tvj (fc=6kHz,8kHz,10kHz)

5 Conclusion

New Gen.4 Trench SiC-MOSFET for Automotive Applications have been developed to meet the requirements of the evolving automotive market.

Gen.4 offer better Ron,sp than conventional Gen.2 and solve trench-specific challenges with three proprietary technologies: BPW, SC, and JD.

Since trench SiC-MOSFET have superior DC loss due to its superior Ron and sp, Gen.4 is best suited for low-frequency applications such as EV inverter. On the other hand, planar SiC-MOSFET with superior switching loss is best suited for high-frequency applications such as OBC and boosters.

When we evaluated the power module with Gen.4, we confirmed that a power loss improvement of about 10% and the output capability of 350 kW or more could be obtained with multiple chips in parallel.

The improvement in power loss from Gen.2 to Gen.4 can be allocated to chip size reduction, contributing to downsizing and cost reduction of inverters for xEVs.

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