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Validating Duty Cycle-Based Repetitive Gate and Drain Transient Overvoltage Specifications for GaN HEMTs

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Abstract

Repetitive transient overvoltage ringing is a switching characteristic that is commonly seen in GaN-based high slew-rate and high frequency applications. Thus, an application driven repetitive transient overvoltage specification is highly desirable. In this work, a 1% duty cycle-based overvoltage specification was developed from resistive-load hard switching test biased at 120% of maximum drain-source voltage ($V_{DS,Max}$). To validate the 1% duty cycle factor (DC_{Factor}), an unclamped inductive switching (UIS) test circuit featuring *in-situ* $R_{DS(on)}$ monitoring was implemented to emulate the resonance-like overvoltage ringing during drain turn-off transients in applications. The dynamic $R_{DS(on)}$ shift for voltages under 120 $V_{DS,Peak}$ from UIS is projected to be less than 10% after 25 years of continuous operation, which validates the 1% DC_{Factor} specification proposed. The 1% DC_{Factor} with 7 V gate-source voltage is also applicable to gate overvoltage transients, demonstrating the excellent overvoltage robustness of pGaN gate in GaN HEMTs.

1 Introduction

Gallium nitride (GaN) high-mobility-electron transistors (HEMTs) have revolutionized power conversion industries owing to GaN's superior material properties. In recent decades, GaN has been increasingly deployed in advanced applications, such as light detection and ranging (lidar) for autonomous and commercial vehicles, rooftop solar panels, DC-DC converters for AI servers and data centers, drones, e-bikes, humanoid robots, and satellites [1]. The rapid adoption of GaN technology in such diverse applications calls for extreme reliability and user-friendly product datasheet specifications that are tailored to address the switching characteristics of GaN-based converters.

GaN HEMTs are not well suited to operation in avalanche due to the lateral device architecture as compared to the vertically constructed silicon counterparts [2]. Therefore, the drain transient overvoltage margin under high slew-rate fast switching applications is useful for GaN HEMTs. To address this, most of the GaN suppliers provided some forms of transient off-state drain-source voltage specifications in datasheets as a reliability robustness indicator [3]. However, majority of the existing transient voltage ratings on product datasheets do not specify it as a repetitive or cycle-by-cycle specification [3].

In this study, a duty cycle-based repetitive transient overvoltage specification is proposed and validated. Fig. 1 illustrates a simplified gate-source voltage turn-on transient or drain-source voltage turn-off transient, where t_1 is the repetitive transient overvoltage duration within every switching period, t_S. The duty cycle-based repetitive transient overvoltage specification is defined by the ratio of t_1 over t_S.

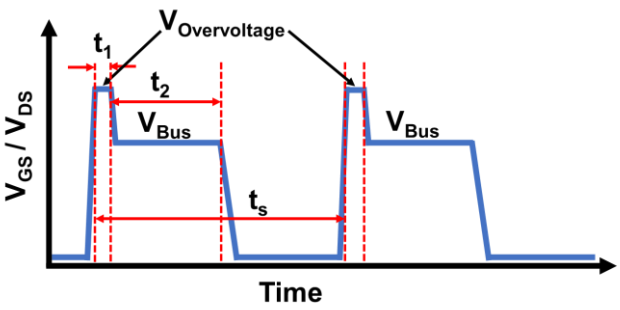

Fig. 1. An illustration of a simplified transient waveform. t_1 is the duration of the overvoltage period; t_2 is the nominal bus voltage bias duration; t_S is the switching period that is the inverse of the switching frequency.

Following the definition of the duty cycle-based transient overvoltage specifications, a method is developed to estimate the overall lifetime by accounting for various stress conditions during the mission, including repetitive transient overvoltage and nominal operation bias. Accurate lifetime projections at different stress conditions are enabled by the development of physics-based lifetime models for gate stress and drain stress, based on the understanding of the fundamental failure mechanisms [4,5].

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2 Drain Overvoltage Specification

This section explains how the duty cycle-based transient overvoltage specification is developed and validated for the drain of GaN HEMTs.

2.1 Developing 1% DC_{Factor} for Drain

Drain transient overvoltage specification is derived by testing a suite of 100 V maximum rated ($V_{DS,Max}$) GaN devices under test (DUTs) with a resistive load hard-switching circuit at the target overvoltage of 120 V_{DS}. Fig. 2 (a) shows the hard switching test circuit equipped with *in-situ* dynamic $R_{DS(on)}$ measurement. Fig. 2 (b) presents the measured drain voltage waveform, where the drain is biased at 120% of the $V_{DS,Max}$ (100 V) with 85% of the time under 100 kHz switching frequency. During the remaining 15% within each switching cycle, the DUTs are turned on, during which the $R_{DS(on)}$ of the DUT is measured.

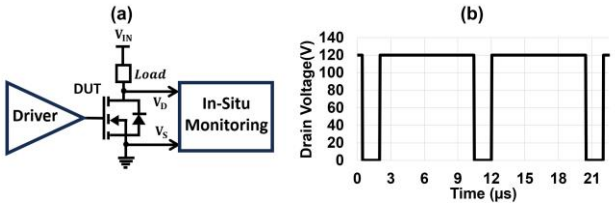

Fig. 2. (a) Schematics of the resistive load hard switching circuit with *in-situ* $R_{DS(on)}$ monitoring; (b) measured drain voltage waveform during switching with 85% of the time V_{DS} = 120 V.

Fig. 3 shows the measurement results of four different 100 V rated GaN transistor types under resistive load hard switching test, where 20% dynamic $R_{DS(on)}$ shift is used as the failure criteria. As shown in Fig. 3, a minimum of 2 x 10^5 minutes is found by projecting when the dynamic $R_{DS(on)}$ shifts more than 20% to their first values. The lifetime projection for drain stress is based on the hot carrier trapping wear-out mechanism [4-6]. The time evolution of dynamic $R_{DS(on)}$ shift can be modeled by a logarithmic-time relation [4-6].

Because the 120 V drain bias is applied 85% of the time, 85% is factored in to calculate the actual lifetime, in which the overvoltage stress is applied continuously, yielding 1.7 x 10^5 minutes. Comparing 1.7 x 10^5 minutes with 25 years expected lifespan (1.3 x 10^7 minutes) leads to 1.3%. To add more margin, the number is reduced to 1%, becoming the proposed duty cycle-based transient drain overvoltage specification.

This total time-based specification can be scaled to a shorter duration that occurs repetitively. Eq. (1) specifies the proposed 1% duty cycle factor (DC_{Factor}) for datasheet specification.

$$\text{Overvoltage } DC_{Factor} = t_1/t_S \leq 1\% \qquad \text{Eq. (1)}$$

where t_1 is the transient overvoltage period where V_{DS} equals to 120 V (120% of $V_{DS,Max}$); t_S is the switching period that is the inverse of switching frequency. Both parameters are specified in Fig. 1.

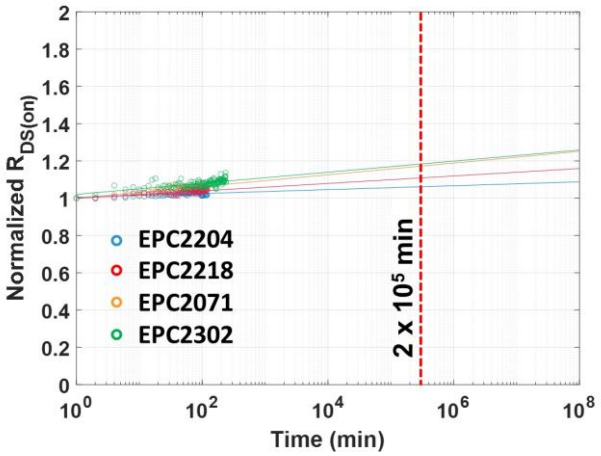

Fig. 3. Evolution of $R_{DS(on)}$ of a representative EPC2204 [7], EPC2218 [8], EPC2071 [9], and EPC2302 [10] 100V-rated GaN transistors. A minimum of 3 devices from each product number was tested and all parts showed similar lifetime projection, where the lifetime projection is estimated to carry a ±10% of confidence level by earlier studies [11].

2.2 Validating 1% DC_{Factor} for Drain

To further validate the proposed 1% duty cycle-based overvoltage specification, an unclamped inductive switching (UIS) circuit was developed featuring *in-situ* $R_{DS(on)}$ monitoring. Fig. 4 (a) shows the schematics of the UIS test circuit with *in-situ* $R_{DS(on)}$ measurement capability. During the operation of the UIS test system, the DUT is first turned on, during which the current is rising linearly, and the energy is stored in the inductor (L). The DUT is then switched off, where the energy stored in the inductor surges into the output capacitor (C_{OSS}) of the DUT, leading to a transient drain overvoltage owing to the resonance between the L and C_{OSS}. Fig. 4 (b) shows the resulting half-sinusoidal overvoltage waveform with a peak drain-source voltage ($V_{DS,Peak}$) of 120 V.

Earlier publication by the authors has demonstrated that UIS testing triggers the same wear-out mechanism [6] causing dynamic $R_{DS(on)}$ drift as the resistive load hard switching test, from which the 1% duty cycle transient overvoltage specification was developed. Therefore, the UIS test circuit is deployed in this study because the resonant-like overvoltage spike shown in Fig. 4 (b) better emulates the transient overvoltage ringing phenomena that are commonly seen in real-world GaN-based applications [12].

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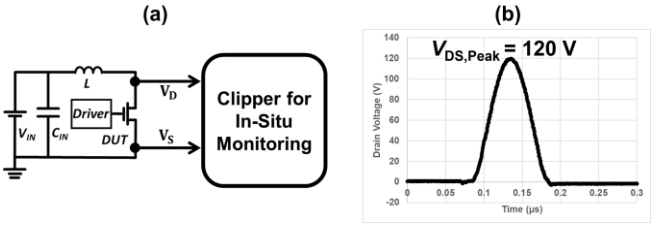

Fig. 4. (a) Schematics of the unclamped inductive switching circuit with *in-situ* $R_{DS(on)}$ monitoring; (b) the measured drain overvoltage waveform with a $V_{DS,Peak}$ of 120 V.

Fig. 5 shows the measured results of a representative EPC2218 (100 V-rate GaN transistor) from three different wafer lots that were tested to over 1.5 billion of switching cycles under 120 $V_{DS,Peak}$ at 75°C junction temperature, showing very small dynamic $R_{DS(on)}$ shift. The logarithmic time-based lifetime model is applied to project the lifetime in 25 years ($1.3x10^7$ minutes). The dynamic $R_{DS(on)}$ shift is expected to be less than 10% and well below the maximum datasheet limit.

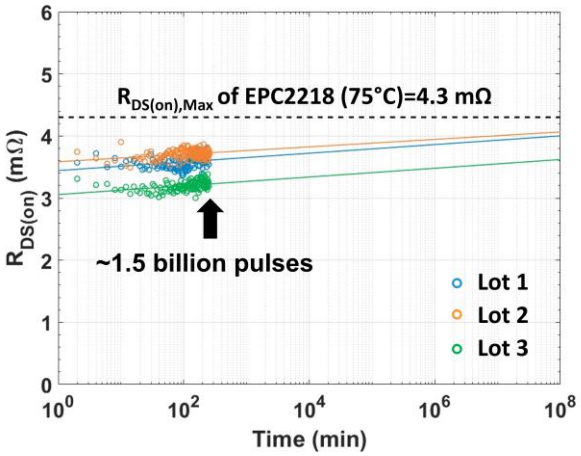

Fig. 5. Evolution of dynamic $R_{DS(on)}$ of a representative EPC2218 DUTs from three different wafer lots under 120 $V_{DS,Peak}$ and 75 °C UIS testing.

Two more 100 V-rated GaN transistors, EPC2204 and EPC2302 were tested under 120 $V_{DS,Peak}$ by UIS at 25°C. Because the hot carrier trapping wear-out mechanism is more pronounced at lower temperature due to the longer mean free path [1,4], 25°C is a more stringent test condition than previously used 75°C. As shown in Fig. 6. They were stressed for more than 6 and 10 billion pulses, respectively, where small dynamic $R_{DS(on)}$ drifts were measured. When projected to 25 years (1.3×10^7 minutes) and beyond, the dynamic $R_{DS(on)}$ of the DUTs are expected to be well below the maximum datasheet limit.

The results in Fig. 5 and 6 showed excellent drain overvoltage robustness of GaN transistors, confirming the applicability of the proposed 1% duty cycle-based repetitive transient overvoltage specification.

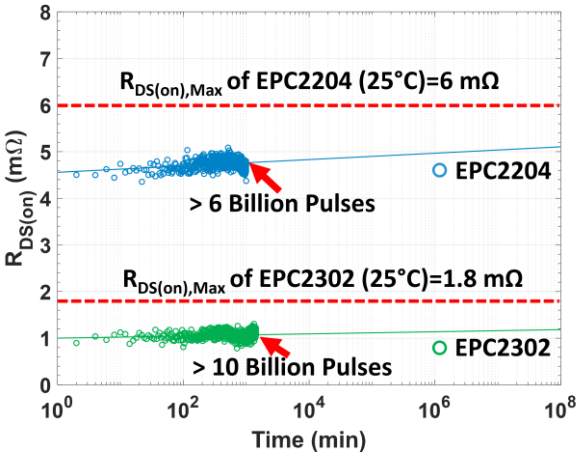

Fig. 6. Evolution of $R_{DS(on)}$ shift of a representative EPC2204 and EPC2302 DUTs under 120 $V_{DS,Peak}$ UIS testing.

3 Gate Overvoltage Specification

The relatively small margin between the maximum rated gate voltage ($V_{GS,Max}$) and typical recommended operating gate voltage has become a concern for GaN HEMTs [13]. Therefore, it is highly desirable to develop a repetitive transient gate overvoltage specification for GaN. This section shows that the 1% duty cycle developed from drain stress can also apply to gate overvoltage.

3.1 Developing 1% DC_{Factor} for Gate

Accelerated gate reliability testing beyond $V_{GS,Max}$ was performed and generated gate failures well above the rated maximum operating conditions. Failure analyses were conducted and found that impact ionization in the pGaN gate under forward gate bias is the underlying wear-out mechanism [1,5]. Thus, another physics-based lifetime model for gate stress was developed from first principles [1,5].

Fig. 7 shows the measured mean-time-to-fail (MTTF) at various gate biases. The solid blue line is the fitted lifetime model based on the impact ionization wear-out mechanism, where the model agrees with the measurements. The lifetime projection is then extrapolated to lower failure rates such as 100 ppm, 10 ppm and 1 ppm shown in Fig. 7.

In Fig. 7, the time-to-fail at 7 V_{GS} constant DC bias is projected to be ~$1x10^{12}$ seconds at MTTF (50% failure rate) and ~$5x10^6$ seconds at 100 ppm failure rate. By scaling them with the 1% duty cycle, the total lifetimes with 1% duty cycle of 7 V transient overvoltage are calculated to be ~$1x10^{14}$ seconds at MTTF and ~$5x10^8$ seconds at 100 ppm, which are equal to ~31,700 years (MTTF) and ~16 years (100 ppm), respectively. The estimated results show the validity of the 1% duty cycle-based gate overvoltage specification.

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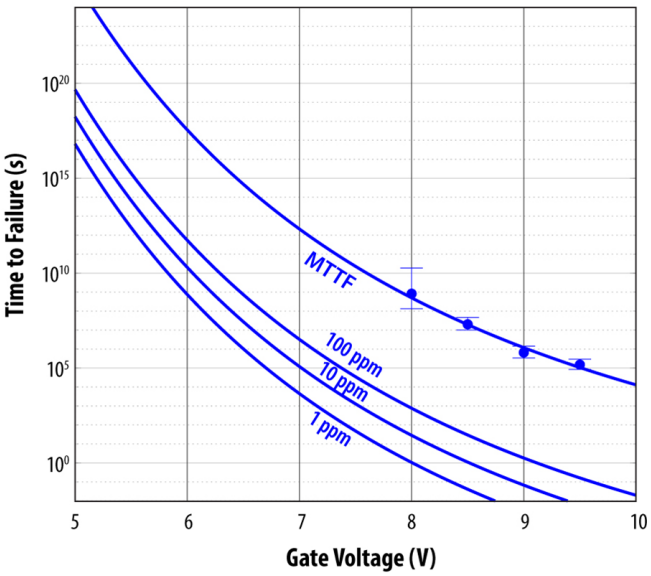

Fig. 7. Time to failure vs. gate bias at 25°C. MTTF (and error bars) are shown for four different voltage legs. The solid line corresponds to the impact ionization lifetime model at different failure rates, including MTTF (50%), 100 ppm, 10 ppm, and 1 ppm.

3.2 Validating 1% DC_{Factor} for Gate

To further validate the proposed 1% duty cycle-based transient gate overvoltage at 7 V, a gate specific UIS test circuit is developed. The schematics of the gate UIS system are shown in Fig. 8 (a), where the EPC2252 GaN transistor [14] is first turned on, allowing the inductor (L) to charge up. When EPC2252 is turned off, the resonance between inductance and parasitic capacitance triggers an overvoltage spike that is applied to the gate of the DUT. Fig. 8 (b) illustrates the gate overvoltage spike waveform with a $V_{GS,Peak}$ of 7 V that is measured on the gate of the DUT.

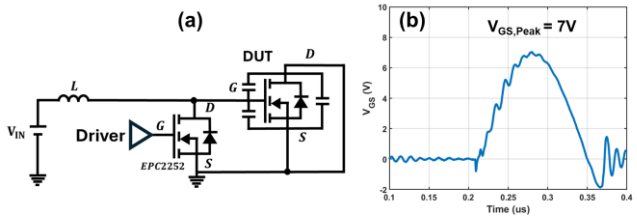

Fig. 8. (a) Schematics of the gate UIS test circuit; (b) the measured gate overvoltage waveform with a $V_{GS,Peak}$ of 7 V.

Three representative EPC2057 GaN transistors [14] were stressed under the 7 $V_{GS,Peak}$ under 3 MHz for more than a trillion ($1x10^{12}$) cycles. As shown in Fig. 9, no measurable degradation in $V_{GS,Peak}$ was seen on the continuously monitored gate waveforms over the course of 1 trillion cycles, suggesting the DUTs can survive such nearly repetitive gate transient overvoltage stresses. Fig. 10 shows the electrical measurements including $R_{DS(on)}$ and threshold voltage (V_{TH}) before and after the 1 trillion cycles of 7 V gate overvoltage spikes, where no significant parameter shifts were detected.

Fig. 9 and 10 show the excellent overvoltage robustness of the pGaN gate in GaN HEMTs, which also validates the applicability of the 1% duty cycle-based repetitive transient overvoltage specification for the gate.

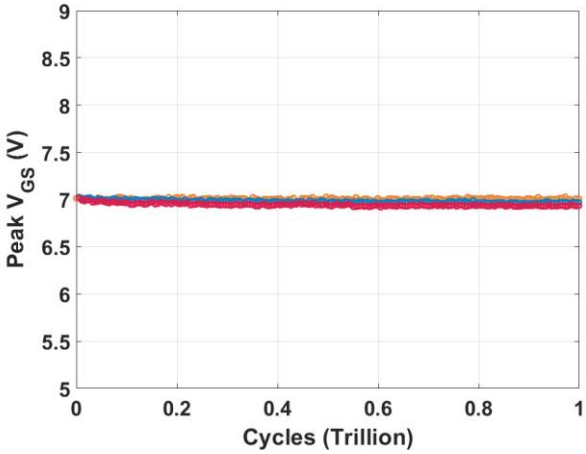

Fig. 9. *In-situ* 7 $V_{DS,Peak}$ monitoring during 1 trillion overvoltage pulses of three EPC2057 GaN transistors, where no measurable $V_{GS,Peak}$ degradation is seen.

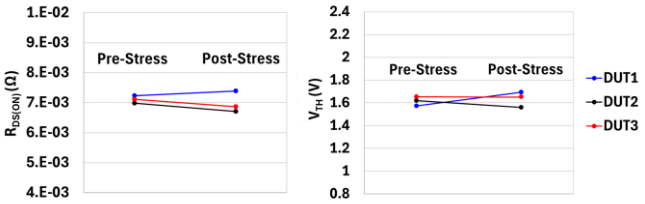

Fig. 10. Pre- and post-electrical measurements ($R_{DS(on)}$ and V_{TH}) of the three EPC2057 GaN transistors, showing insignificant parameter shift.

4 How to Use the 1% DC_{Factor}

A comprehensive lifetime equation was developed and shown in Eq. (2), accounting for various lifetimes under different stress conditions [4,15].

$$\frac{1}{LT_{Total}} = \frac{a}{LT_a} + \frac{b}{LT_b} + \cdots + \frac{i}{LT_i} \qquad \text{Eq. (2)}$$

where LT_{Total} is the total lifetime and LT_i is the projected lifetime under individual stress condition. Eq. (2) shows that the harshest stress condition, which also yields the shortest lifetime, dominates the total lifetime.

a, b, …, i are the duty cycle-based lifetime percentages, defined by Eq. (3).

$$i = t_i/t_S \qquad \text{Eq. (3)}$$

where t_i is the time interval during which a specific gate or drain bias is applied within a switch cycle; t_S is the switching period, inversely proportional of the switching frequency. The variable i is equal to DC_{Factor} when t_i is the overvoltage period, specified by Eq. (1). The sum of *a, b, …, i* is 100%, denoted by Eq. (4).

$$a + b + \ldots + i = 100\% \qquad \text{Eq. (4)}$$

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How do the engineers use this 1% DC_{Factor} when designing GaN-based converters?

For instance, an LLC converter that uses 100 V-rated GaN transistors on the primary side operates at 1 MHz switching frequency (t_S=1 µs). Due to parasitic inductance in the circuit, the drain of the GaN FETs is subjected to a repetitive 120 V overvoltage spike with a duration of ~5 ns. Scaling 5 ns overvoltage duration to 1 µs switching period yields 0.5%, less than the 1% DC_{Factor} specified by datasheet overvoltage rating. Hence, there should be no reliability risk expected.

If the same LLC converter had a high gate loop inductance, causing a 6.5 V gate overvoltage spike during turn-on transients repetitively with a measured duration of 10 ns, how do the customers evaluate the reliability risk? First, 10 ns is 1% of 1 µs at 6.5 V_{GS}, which still satisfied the 7 V 1% DC_{Factor} specification. As shown in Fig. 7, the time-to-failure at 6.5 V with 10 ppm failure rate is approximately $1.6x10^7$ seconds. After scaling with 1% DC_{Factor}, the total lifetime is expected to be $1.6x10^9$ seconds based on Eq. (2), which is longer than 50 years. Therefore, greater than 50 years of gate lifetime with 10 ppm failure rate are predicted under such gate stress conditions.

5 Conclusions

Repetitive transient overvoltage ringing is a common switching characteristic for wide bandgap power converters operating at high frequencies. A 1% duty cycle-based repetitive overvoltage specification was developed and validated for drain turn-off as well as gate turn-on transients. Such application-driven repetitive transient overvoltage specifications are critical for facilitating the adoption of GaN technology in increasingly diverse and advanced power applications.

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