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New Power MOSFET Technology for High Efficient Motor Drives

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Abstract

This work introduces the characteristics and properties of the latest trench MOSFET technology for high power density motor drive applications. A revolutionary new cell design is combined with the benefits of an advanced manufacturing technology, bringing benefits of low conduction and switching losses with good ruggedness, excellent body diode properties and an extremely tight threshold voltage spread. These features result in a well-balanced all-round performer that will bring significant improvements to e-scooters, microEVs, forklifts, golf carts, light electric aircraft, and other battery-powered motor drive applications, which require an easy paralleling of many devices. The presented results focus on the use of the new devices in such applications.

1 Introduction

The power source of e-scooters, microEVs, forklifts, golf carts or light electric aircraft usually use low-voltage lithium-ion batteries. Therefore, MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) are mainly used in inverters on these applications. The peak power delivered from the inverters can easily reach several ten Kilowatts, the inverter output current is up to hundreds of amps. In order to configure a switch in a three-phase inverter shown in Fig. 1, paralleling of MOSFETs is a common and practical approach for high current applications because of limited current capability on a single discrete MOSFET. Since multiple MOSFETs are connected in parallel to handle enough current for the motor, the discrete MOSFET-based inverters require low conduction and switching losses with extremely tight threshold voltage spread on every discrete MOSFET. This eases the challenge to realize a uniform current distribution and stray inductance of the metal PCB on parallel connection of MOSFET-based inverter.

Trench MOSFET technologies have always been noted as excellent candidates to be used as switches in power inverter circuits, starting in the late 1980s with the appearance of the first trench gate MOSFETs (Fig. 2a). This marked a milestone for the broad adoption of field-effect transistors in the power electronics industry [1]-[3]. Moving the channel to the vertical direction, the device concept virtually removed the JFET region and reduced the on-state resistance. However, the remarkable increase in cell density has also brought to light significant disadvantages. The gate-drain capacitance and gate-source capacitance both increase linearly with the number of trenches, i.e. with the cell density. Since the MOSFET is uniquely controlled through its gate terminal, the gate driver circuitry has to provide the total gate charge Q_G required to turn on the transistor. In the case of paralleling of MOSFET applications, as found for power inverter, the lowest gate charge is desirable since it proportionally reduces the gate-driving losses. A part of the total gate charge is associated with the gate-to-drain charge Q_{GD}, which governs the drain voltage transient. Larger values of Q_{GD} impact the transient speed, result in an increase of the switching losses, and additionally force the use of longer dead-times on the inverters. Additionally, another constraint is imposed by the Miller charge ratio: Q_{GD}/Q_{TH} must be lower than one. This is needed in order to ensure an intrinsic robustness against parasitic turn-on of the MOSFET under fast drain voltage transients [4].

The introduction of charge-compensated structures, exploiting the same principle as super junction devices, marked the beginning of a new era. The introduction of

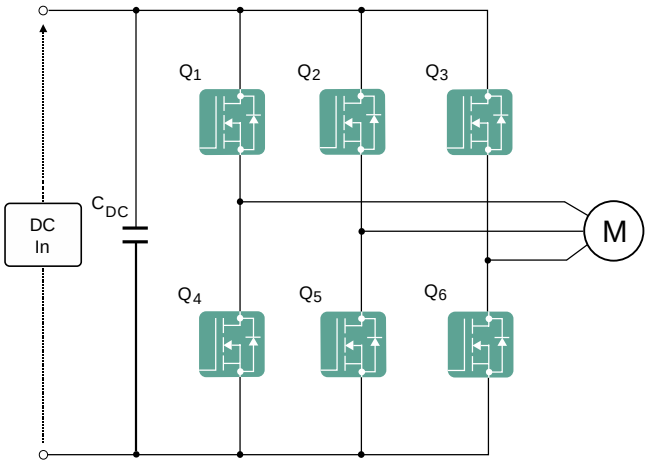

Fig. 1: Basic schematic of the B6 inverter

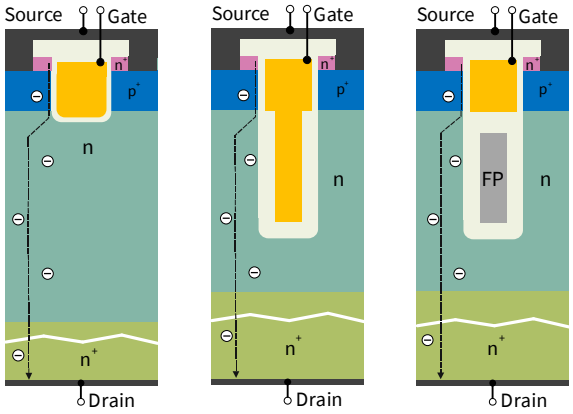

Fig. 2a-c: Exemplary device structures depicting the evolution of power MOSFETs:

a) Trench MOSFET structure with vertical channel

b) Trench MOSFET with lateral charge-compensation by a gate-connected field plate

c) Trench MOSFET with lateral charge-compensation by an insulated field plate connected to source

devices employing an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Fig. 2b) [5]. The lateral depletion alters the electric field distribution throughout the structure, and it is possible to block the same voltage within a shorter length. In turn, the electric field can now be supported by a thinner and more heavily doped drift region, which leads to a substantial reduction in the on-state resistance. Unfortunately, the field plate as an extension of the gate electrode leads to a significant increase of the gate-drain capacitance C_{GD} (hence also Q_{GD} and Q_G) and a nonlinear dependence on the drain voltage.

Isolating the field plate from the gate and instead connecting it to the source (Fig. 2c) resolves this issue. While the charge compensation principle operates as before, the now buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{GD} and related charges. At the time of their introduction, these devices delivered best-in-class performance [6]. While the presence of the field plate comes with the disadvantage of an increased output capacitance C_{OSS} and output charge Q_{OSS} (a consequence of the lateral charge-compensation), a careful device optimization enabled field plate-based power technologies with $FOM_{OSS} = R_{DS(on)} \times Q_{OSS}$ comparable to those of the standard trench MOSFET [7],[8].

2 Novel Device Concept

New MOSFET devices are required to provide improvements across all figures of merit. To meet these requirements, a novel cell-design approach is developed, which explores a true three-dimensional charge compensation. Today's state-of-the-art MOSFET technologies use an insulated deep field plate underneath and separated from the gate electrode and employ a stripe layout as depicted in Fig. 3. The new generation separates the field plate trench, which is now formed with a needle-like structure, from a grid-like gate trench that surrounds the needles [9], as shown in Fig. 4. This chip structure increases the silicon area available for current conduction, allowing for a further reduction in the overall on-resistance [9]. In order to further reduce the $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ values, the gate trench underwent a complete redesign to minimize its lateral extension.

The distribution of the field plate resistance across the chip for the new grid-like device is completely flat due to the trench electrodes acting as field plates connected directly to the source metal. This is improved from the chip with a stripe layout, where the local resistance increases with distance from the source runner in the center of the chip. Hence this new layout is expected to switch extremely homogeneously, supporting fast transitions between the on- and off-state. It is beneficial for achieving a high avalanche ruggedness, as

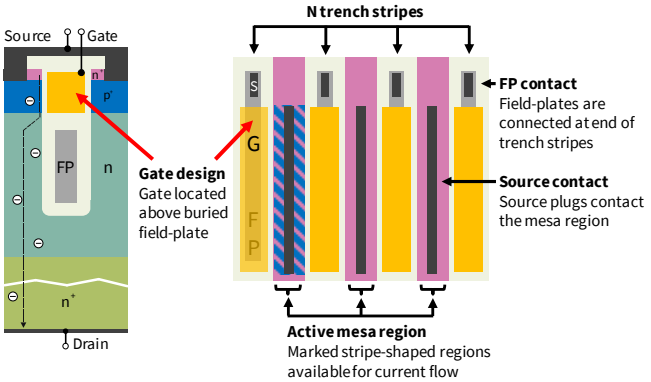

Fig. 3: Typical Trench MOSFET structure with lateral charge-compensation by an insulated field plate connected to source (left) and commonly employed stripe layout approach in the chip design (right)

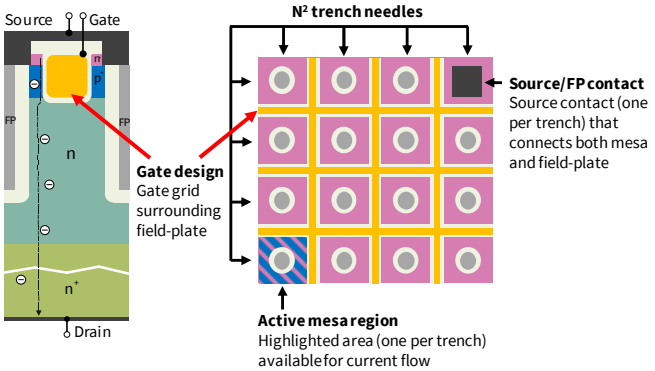

Fig. 4: Trench MOSFET structure with lateral charge-compensation by an insulated field plate and separated gate trench (left) and the new grid-like layout approach in the improved chip design (right)

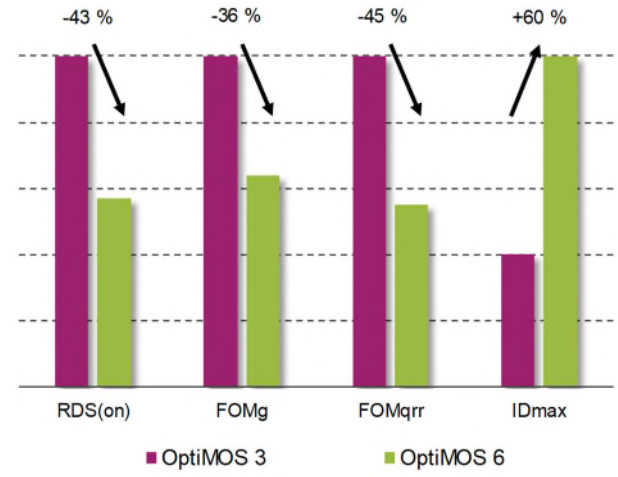

Fig. 5: Improvement in device performance for best-in-class 200 V devices in TO-263 (D²PAK) package

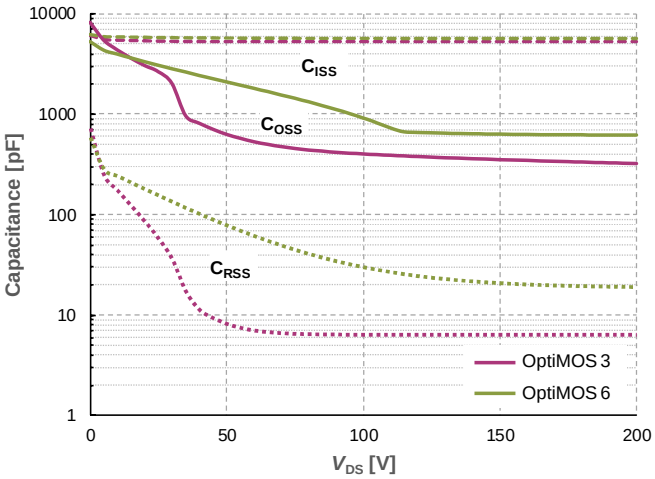

Fig. 7: Comparison of capacitances for best-in-class 200 V devices in TO-263 (D²PAK) package

an increased local field-plate potential may alter the local breakdown voltage [10] and can lead to an inhomogeneous power dissipation over the chip area. In addition, the direct connection between the source and the field plate practically eliminates any resistance in series with the output capacitance, which minimizes conduction losses during charging and discharging of the output capacitance.

In the case of the stripe design, the local gate resistance rises along the length of the stripe, with the lowest values at the gate runners and the gate pad. The use of a gate grid-like layout results in a much more even distribution of the gate resistance across the chip. This strongly improved homogeneity is further advantageous for device robustness, for example avalanche ruggedness, by reducing the probability that a part of the chip is affected by gate signal delays [11] or parasitic turn-on. In former transistor generations, both gate signal delay and parasitic turn-on degrade the device ruggedness as power dissipation is limited to just a part of the chip.

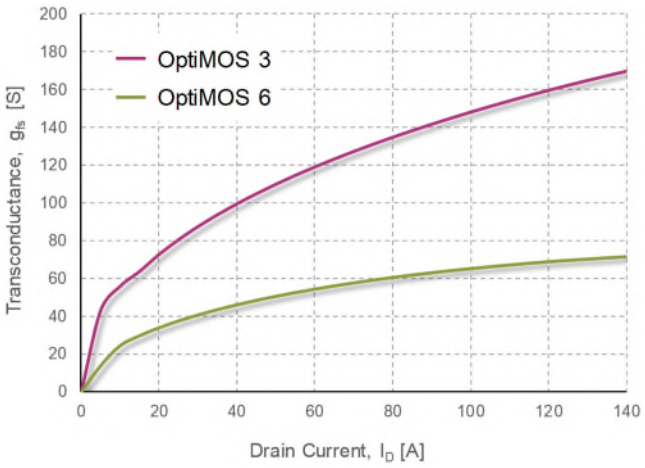

Fig. 6: Comparison of transfer characteristics for best-in-class 200 V devices in TO-263 (D²PAK) package

Fig. 5 indicates the realized parameter improvements for the new OptiMOS™ 6 200 V technology based on the introduced grid-like layout with trench needles over the predecessor technology OptiMOS™ 3 200 V. Here, it was especially important to further reduce the reverse-recovery charge with respect to the previous technology generation with a fast diode [12]. This is not only important for a further reduction of switching losses, but also improves the EMI behavior and ensures a high commutation ruggedness [13]. Thanks to the new advanced cell design, the on-resistance of the device is greatly reduced, enabling a remarkable 60 % increase of the drain current capability in the same package footprint.

Due to the required output power in motor-drive applications, it is often necessary to parallel devices. This is often a challenging task, as the designs need to ensure a good static and dynamic current sharing between the devices. The new OptiMOS™ 6 devices offer several advantages here. A lowered gate threshold voltage spread of 1.5 V instead of 2.0 V as in case for the predecessor technology, and a lowered transconductance as depicted in Fig. 6 improve dynamic current sharing when paralleling MOSFETs. This leads to more evenly spread device temperatures, ultimately improving reliability, or reducing the number of paralleled MOSFETs.

In addition, the linearity of the device capacitances for the new devices is also improved, which is achieved even despite the realized FOM improvements. Fig. 7 shows the comparison for best-in-class devices of the predecessor OptiMOS™ 3 and the latest OptiMOS™ 6 200 V technology. The improved linearity of both output capacitance C_{OSS} and reverse capacitance C_{RSS} reduces oscillations during switching and causes a lower voltage overshoot and less switching losses.

Overall, the use of a gate grid and the direct connection of the field plates to the source metal realizes a very attractive device setup. This new device structure not only ensures a very fast and homogeneous transition at turn-on and turn-off to minimize switching losses, but

also reduces the risk of an unwanted, dV/dt induced parasitic turn-on of the MOSFET.

3 Performance in Motor Drives

3.1 Bench test on single device

This investigation focuses on the comparison of the new OptiMOS™ 6 200 V devices with its direct predecessor technology. The comparison uses best-in-class devices, which have approximately the same die area. The new OptiMOS™ 6 devices come with an on-resistance of 6.8 mΩ, while the predecessor OptiMOS™ 3 devices [12] have an on-resistance of 11.7 mΩ. The device performance in the application is studied using a 3-phase motor drive inverter test platform. The inverter test board, a single layer insulated metal substrate (IMS) board with aluminum core, uses a single MOSFET per switch in a standard TO-263-3 package. Fig. 8 shows the board design.

In the measurements, the switching frequency of the inverter is 10 kHz with sinusoidal SVM modulation, and a single-phase current of 33 Arms at a DC bus voltage of 144 V. The dead time is set to 600 ns. To enable the loss calculations, the measured values, among others, include low-side MOSFET current, low-side drain-to-source voltage and the phase current. All measurements extended over one complete electrical period of the motor.

The first investigation determined the inverter losses on MOSFETs. The results are shown in Fig. 9. The comparison includes the overall mean losses per MOSFET as well as the separate conduction and switching losses. The overall loss reduction amounts to a remarkable 45.5 %. It is also worth mentioning that

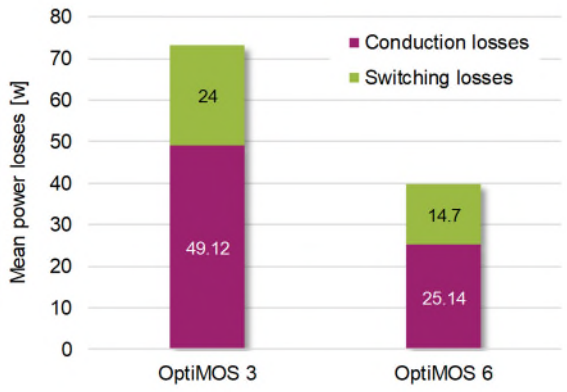

Fig. 9: Comparison of the MOSFET power losses for both generations in the B6 inverter equipped with a single device per power switch position

the new OptiMOS™ 6 200 V devices achieve a reduction in all of the loss contributors.

Fig. 10 compares the switching behavior using predecessor and new technology devices. The new OptiMOS™ 6 waveforms reveal a cleaner and more linear turn-on and turn-off, translating into lower switching losses. The total power losses are reduced by 45%, with 39% less switching losses and 49% less conduction losses.

In consequence, the new devices remain much cooler with 63.6°C compared to 95.8°C of the predecessor device, as indicated by the thermal images in Fig. 11. This enables a significant increase of the output power. For the same device temperature, the current per phase can be increased by impressive 38 %, supporting higher inverter power densities.

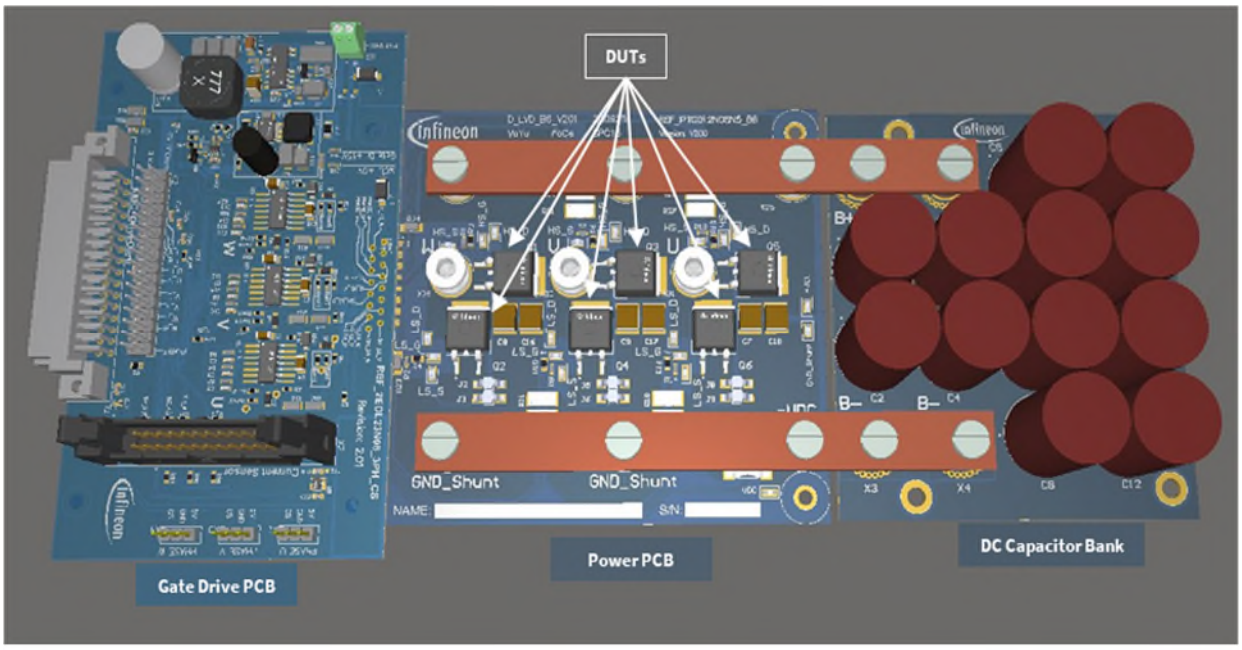

Fig. 8: 3-phase motor-drive inverter test platform

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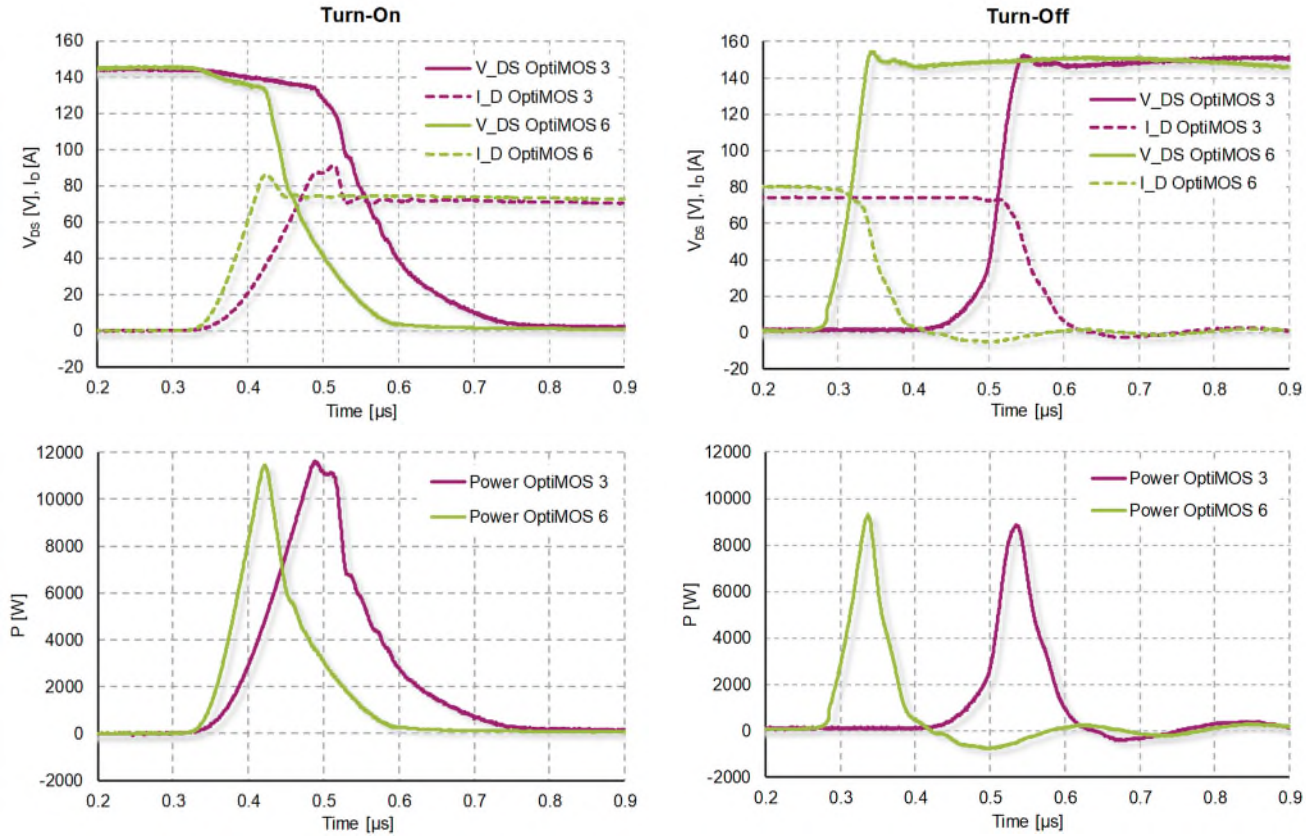

Fig. 10: Comparison of switching waveforms (left) and instantaneous power (right) between the new OptiMOS™ 6 and the predecessor OptiMOS™ 3 technology (I_D = 75 A)

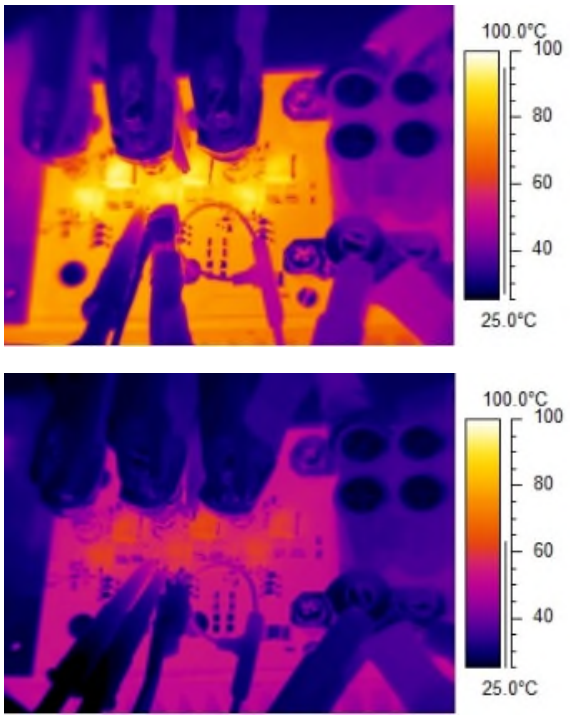

Fig. 11: Comparison of device temperature at identical power output between OptiMOS™ 3 (top) with 95.8°C and the new OptiMOS™ 6 (bottom) with 63.6°C

3.2 Test on commercial inverter under paralleling

This section compares the performance of the same new OptiMOS™ 6 and the predecessor OptiMOS™ 3 devices on a commercially available inverter [14] which employs a common B6 topology as depicted in Fig. 1, with a nominal input voltage of 144 V, an average current output of 135 Arms and a short-term peak current output of 500 Arms. The rated power of the inverter is 65 kW. The power board contains 96 MOSFETs overall, with 16 devices paralleled in each leg for applications like microcars or e-forklift motor drives. The switching frequency is adjustable between 8 kHz and 16 kHz, with a dead time of approximately 1 µs. The inverter uses devices in standard TO-263-3 packages, making it relatively easy to modify the original devices and to replace them by the devices of interest.

The first investigation determined the mean losses per MOSFET. The results are shown in Fig. 12. The comparison includes the overall mean losses per MOSFET as well as the separate conduction, turn-on and turn-off losses. The overall loss reduction ammounts to a remarkable 36 %. The results are coherent to the previous section.

Beside a reduction of the losses, it is important that the devices provide a clean switching behavior. Switching waveforms are measured at a single MOSFET.

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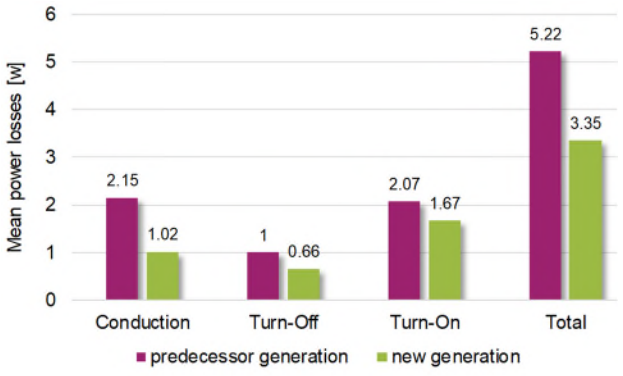

Fig. 12: Comparison of mean power losses for each MOSFET

Fig. 13 gives an overview on the investigated device parameters, and at which positions of the circuitry these values are measured. All gate-to-source and drain-to-source voltages are calculated from two separate measurements, taken from the respective electrode to ground. The current through the MOSFET is measured by a Rogowski coil at the source of a low-side device.

Fig. 14 shows the switching waveforms of the new generation devices when the high-side switch is turned-on. Fig. 15 depicts the transients for the turn-off of the high-side switch, with the low-side MOSFET operating in synchronous rectification mode.

In both cases, the use of the OptiMOS™ 6 devices results in clean waveforms. There is no visible ringing, and the slew rates are rather linear which is an advantage for the EMI behavior. This implies that the performance improvement of the new device does not degrade the EMI behavior. This is confirmed by the comparison of the radiated emission between the two technology generations shown in Figs. 16 & 17. The radiated emission measurements were done in accordance with the applicable standard EN 12895.

4 Conclusion

This work introduces our latest power MOSFET technology family that delivers improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance.

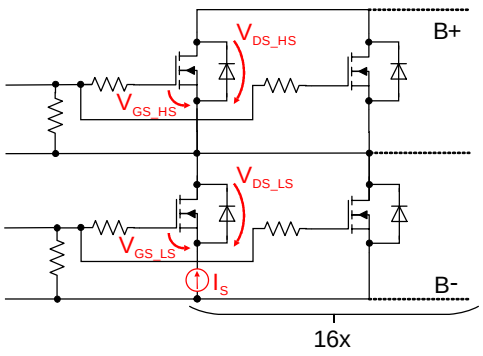

Fig. 13: Indication of test points for the waveform measurements

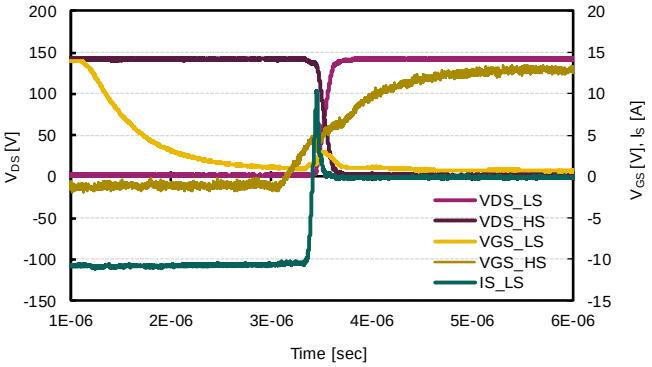

Fig. 14: Switching waveforms at turn-on of the high-side switch

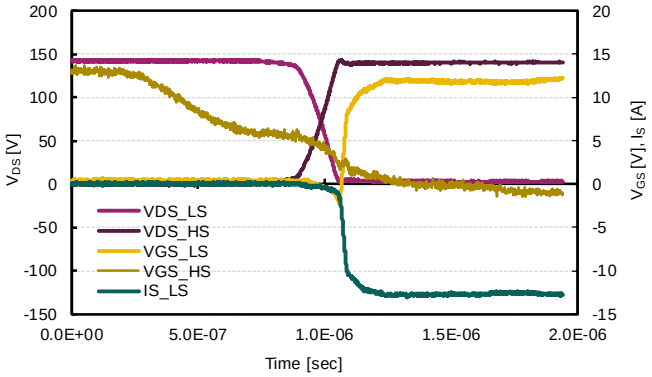

Fig. 15: Switching waveforms at turn-off of the high-side switch

The remarkable progress in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ three-dimensional charge compensation combined with a gate grid in a trench power MOSFET. The new design provides a so-far unmatched homogeneity of the gate and field plate resistance across the chip. The reduction achieved in the on-resistance and the competitive FOM together with a low output and reverse-recovery charge, result in lower conduction and switching losses. Motor-control applications will greatly benefit from these improved properties. The improved switching homogeneity across the device area further enhances the system efficiency. The devices can be massively paralleled and still achieve clean switching waveforms. The good switching properties are also confirmed by radiated emission measurements, which stay well within the required limits.

The significantly improved device performance also allows a reduction in the number of devices required, or alternatively the use of smaller footprints, without having a negative impact on the temperature of the devices. This not only provides an advantage in terms of bill-of-materials (BOM) costs, but also the chance to save actual space on the PCB. This provides a chance for further optimization at the level of system design, which is expected to enhance system efficiency, minimize the motor inverter size and increase the power density.

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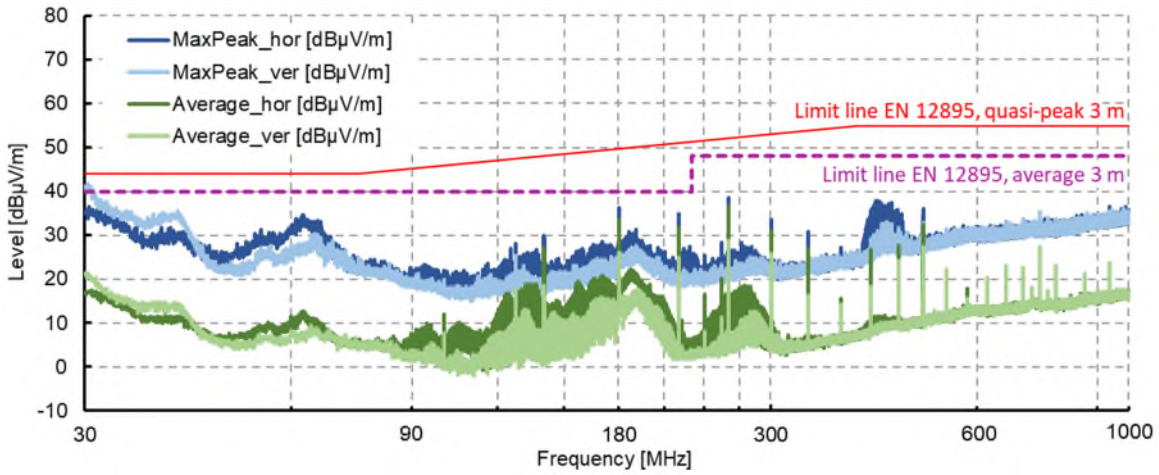

Fig. 16: Measurement of radiated emission in the application using the predecessor device generation

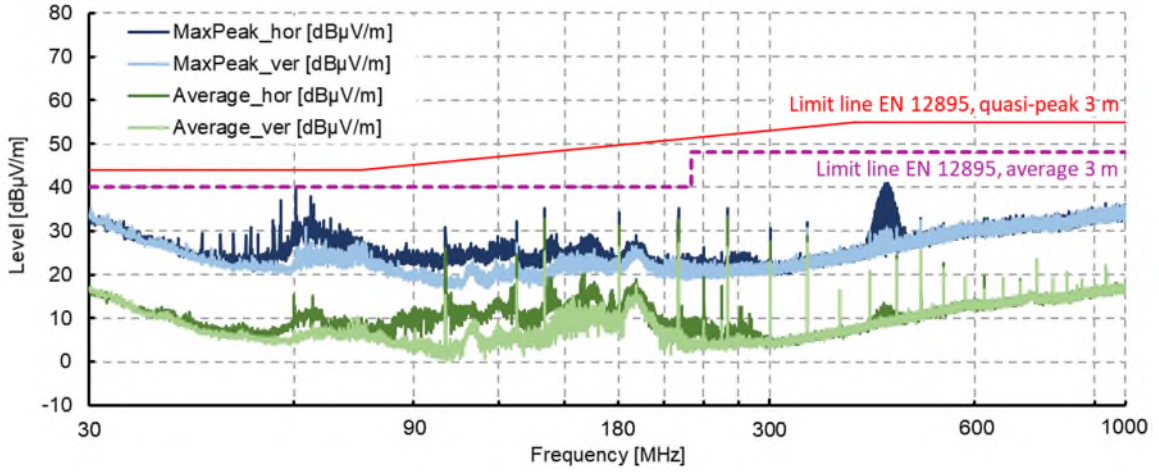

Fig. 17: Measurement of radiated emission in the application using the new device generation

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