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A Harmonic Current Suppression Method for PMSM Based on Model Predictive Current Control

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Abstract

This paper introduces a harmonic current suppression (HCS) strategy utilizing dual-vector model predictive current control (DV-MPCC) to mitigate the issue of elevated harmonic currents resulting from a reduced switching frequency in permanent magnet synchronous motors (PMSMs). First, the number of switching actions of the inverter at future moments is evaluated and limited to reduce the switching frequency of the inverter. Second, by employing a simple calculation method, the harmonic components induced by the reduced switching frequency are separated from the predicted current. These components are then embedded as one of the performance indicators in the cost function so that high-performance predictive control can be achieved even with reduced switching frequency. Finally, the effectiveness of the proposed method is validated through simulation experiments.

1 Introduction

Permanent magnet synchronous motors (PMSMs) are widely used in industrial and electric vehicle applications due to their small size, high torque, high power density, and high efficiency [1-3]. The traditional and classical control methods for PMSMs are field-oriented control (FOC) and direct torque control (DTC). However, FOC and DTC have certain drawbacks in terms of dynamic and steady-state performance, and they cannot meet the performance requirements of motor control systems under various operating conditions [4-5].

In recent years, the finite control set model predictive control (FCS-MPC) method has gained popularity due to its elimination of the need for a modulator and its ability to efficiently manage multi-objective nonlinear problems [6-7]. At the same time, with the improvement of digital processing chip technology, MPC has been further promoted and applied in practical industrial applications. In the development process of MPC, to further improve its control accuracy, many scholars have started by increasing the number of voltage vectors (VVs) acting within one control cycle or by improving the control frequency [8-10]. However, these two methods, while effectively improving the system's control accuracy, bring about significant losses and heat generation [11-12]. This undoubtedly increases the workload of the inverter and reduces its service life. Especially in many high-power applications, the switching frequency needs to be lowered to reduce loss and heat generation. It should be noted that lowering the switching frequency inevitably generates harmonic currents. These harmonic currents, through the sampling channel, are incorporated into the computation of the prediction model, which undoubtedly leads to deviations between the prediction model and the actual system behavior, directly affecting the stability of the system [13-14].

To address this challenge, this paper proposes a harmonic current suppression method based on model predictive current control (MPCC) considering switching frequency limitations (HCS-SFL-MPCC). First, the switching frequency is reduced by rationally designing the cost function. Then, the harmonic currents generated in the predicted currents due to the reduced switching frequency are extracted and embedded in the cost function as an index for system performance control, in order to balance the relationship between switching frequency and harmonic currents. Ultimately, the proposed HCS-SFL-MPCC method can effectively suppress the harmonic components caused by the reduction of switching frequency, thereby reducing the impact of harmonic components on the system and improving the system control performance.

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The main structure of this paper can be divided as follows: Section II introduces the conventional DV-MPCC. Next, Section III elaborates on the core idea and control strategy of the proposed HCS-SFL-MPCC. Then, Section IV verifies the effectiveness of the proposed HCS-SFL-MPCC method through simulation. Finally, Section V provides the conclusion.

2 Mathematical Model of PMSM

The controlled surface mounted PMSM (SPMSM) in the paper is realized by utilizing a two-level voltage source inverter (2L-VSI), and the topology is depicted in Fig. 1.

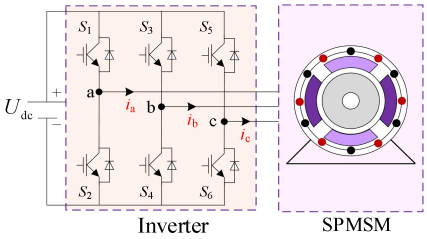

Fig. 1. Topology of SPMSM system.

The mathematical model of SPMSM under dq-axes can be represented as

$$\begin{cases} \dfrac{\mathrm{d}i_\mathrm{d}}{\mathrm{d}t} = \dfrac{1}{L_\mathrm{d}}(u_\mathrm{d} - Ri_\mathrm{d} + \omega L_\mathrm{q} i_\mathrm{q}) \\ \dfrac{\mathrm{d}i_\mathrm{q}}{\mathrm{d}t} = \dfrac{1}{L_\mathrm{q}}(u_\mathrm{q} - Ri_\mathrm{q} - \omega L_\mathrm{d} i_\mathrm{d} - \omega\psi_\mathrm{f}) \end{cases} \tag{1}$$

where i_d and i_q represent the current of dq-axes, respectively. R, L, ψ_f and ω_e represent resistance, stator inductance, flux-linkage and electrical angular velocity, respectively.

Furthermore, the switching states produced by the 2L-VSI can be portrayed as

$$S = [S_{\mathrm{a1}} \quad S_{\mathrm{b1}} \quad S_{\mathrm{c1}}]^{\mathrm{T}} \tag{2}$$

where S_{a1}, S_{b1}, S_{c1} denote the phase change state of each phase in the three upper bridge arms of the inverter, respectively. And the correlation between the switching state and VV is depicted in Fig. 2.

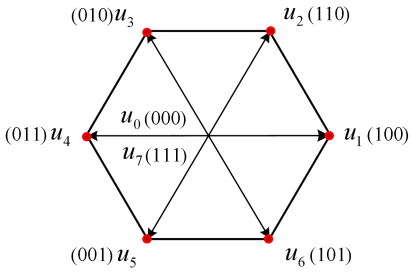

Fig. 2. The correlation between switching state and VV in 2L-VSI.

Immediately after that, an Eulerian discretization of (1) yields the predicted current at (k+1)$^{\mathrm{th}}$ instant.

$$\begin{cases} i_\mathrm{d}^\mathrm{p}(k+1) = Mi_\mathrm{d}(k) + Nu_\mathrm{d}(k) + T\omega_\mathrm{e} i_\mathrm{q}(k) \\ i_\mathrm{q}^\mathrm{p}(k+1) = Mi_\mathrm{q}(k) + Nu_\mathrm{q}(k) - T\omega_\mathrm{e} i_\mathrm{d}(k) - N\omega_\mathrm{e}\psi_\mathrm{f} \end{cases} \tag{3}$$

where M=(1-TR/L), N=T/L.

3 Traditional DV-MPCC

The traditional DV-MPCC (T-DV-MPCC) selects two VVs in one cycle and pre-allocates the time of the two VVs at the same time, and finally selects the optimal combination of VVs to be applied to the inverter. The control block diagram of the T-DV-MPCC with one-step delay compensation is shown in Fig. 3.

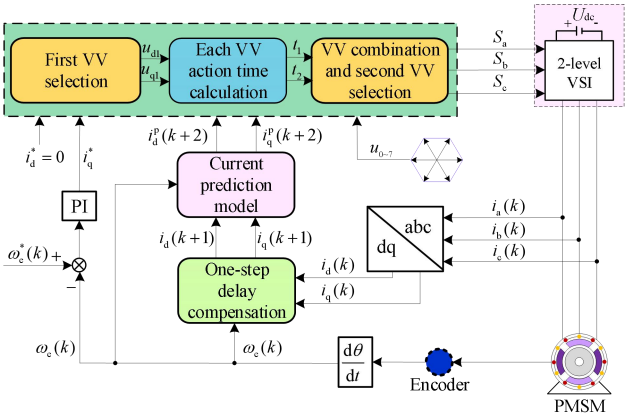

Fig. 3. Control schematic diagram of T-DV-MPCC.

In T-DV-MPCC, the first and second VVs are selected in the same way as traditional single vectors, based on cost minimization. After determining the first VV, each of the eight VVs is combined with the first VV and time is allocated to obtain the optimal VV combination. The synthesized VV can be denoted as

$$u_\mathrm{s}^\mathrm{s}(k) = \frac{t_1 u_{\mathrm{s}1}(k) + t_2 u_{\mathrm{s}2}(k)}{T} \tag{4}$$

$$t_2 = T - t_1 \tag{5}$$

where t_1, t_2 represent the durations for which the first and second optimal VVs are applied, respectively. The calculation of the operation times of these VVs within a single sampling period is derived from the deadbeat control principle for the dq-axes currents [15], namely,

$$i_\mathrm{q}(k+1) = i_\mathrm{q}(k) + S_{\mathrm{q}1} t_1 + S_{\mathrm{q}2} t_2 = i_\mathrm{q}^* \tag{6}$$

where i_q^* denotes the reference current of q-axis. $S_{\mathrm{q}1}$ and $S_{\mathrm{q}2}$ denote the current slopes of q-axis generated by the effect of the two VVs [16].

According to (6) , the action time of the first optimal VV can be represented as

$$t_1 = \frac{\left[i_\mathrm{q}^* - i_\mathrm{q}(k) - s_{\mathrm{q}2} \cdot T_\mathrm{s}\right]\left(s_{\mathrm{q}1} - s_{\mathrm{q}2}\right)}{\left(s_{\mathrm{q}1} - s_{\mathrm{q}2}\right)^2}. \tag{7}$$

After accounting for the one-step delay compensation, the predicted currents under the synthesized VVs are input into the cost function (8) for optimization. The combination of VVs that minimizes the value of the cost function is then selected for operation with the inverter.

$$J=\left[i_{\mathrm{d}}^{*}-i_{\mathrm{d}}^{\mathrm{p}}(k+2)\right]^{2}+\left[i_{\mathrm{q}}^{*}-i_{\mathrm{q}}^{\mathrm{p}}(k+2)\right]^{2}. \quad (8)$$

4 Proposed HCS-SFL-MPCC Method

This section proposes a method for harmonic current suppression aimed at reducing the switching frequency. First, the switching frequency of the inverter is reduced by limiting its switching states at future time steps. Next, harmonic currents present in the predicted current are extracted and suppressed to mitigate the negative impact of reduced switching frequency on the system.

4.1 Switching Frequency Limitation

First, to reduce the switching frequency between neighboring VVs in a dual-vector, the following function is designed

$$f_1=\left|S_{\mathrm{abc}}^{2}(k-1)-S_{\mathrm{abc}}^{1}(k)\right| \quad (9)$$

$$f_2=\left|S_{\mathrm{abc}}^{1}(k)-S_{\mathrm{abc}}^{2}(k)\right| \quad (10)$$

where f_1 denotes count of switching operations between the second VV at the (k-1)$^{\mathrm{th}}$ instant and the first VV at the k^{th} instant. f_2 denotes the count of switching operations between the two adjacent VVs during the sampling period at k^{th} instant.

According to the T-DV-MPCC method, the selection of the first and second VVs is still based on minimizing the cost function. Additionally, the switching states between adjacent VVs need to be considered as a constraint. Therefore, the cost function for selecting the first and second optimal VVs can be designed as

$$J_1=\left[i_{\mathrm{d}}^{*}-i_{\mathrm{d1}}^{\mathrm{p}}(k+1)\right]^{2}+\left[i_{\mathrm{q}}^{*}-i_{\mathrm{q1}}^{\mathrm{p}}(k+1)\right]^{2}+H_1 f_1 \quad (11)$$

$$J_2=\left[i_{\mathrm{d}}^{*}-i_{\mathrm{d2}}^{\mathrm{p}}(k+1)\right]^{2}+\left[i_{\mathrm{q}}^{*}-i_{\mathrm{q2}}^{\mathrm{p}}(k+1)\right]^{2}+H_2 f_2 \quad (12)$$

where H_1 and H_2 denotes the weighting factor between current difference and number of switches. Since both H_1 and H_2 in J_1 and J_2 are designed to balance the order-of-magnitude relationship between the current and the quantity of switching actions, it can be assumed that H_1=H_2=H.

4.2 Harmonic Current Suppression

It should be noted that when the switching frequency constraint is applied to reduce the inverter's switching frequency, errors occur between the synthesized VV and the exact synthesized VV, leading to degraded system control performance and a significant increase in harmonic current components. To address this issue, this paper first uses a low-pass filter to separate harmonic currents from the predicted currents. Then, the harmonic components are directly embedded as one of the performance indicators in the cost function for constraint. The specific steps are as follows.

Firstly, using a low-pass filter to isolate the fundamental component from the predicted currents under the action of the eight synthesized VVs, denoted as

$$i_{\mathrm{sf}}^{\mathrm{p}}(k+1)=\gamma\cdot i_{\mathrm{sf}}^{\mathrm{p}}(k)+(1-\gamma)\cdot i_{s2}^{\mathrm{p}}(k+1) \quad (13)$$

where $i_{\mathrm{sf}}^{\mathrm{p}}(k+1)$, $i_{\mathrm{sf}}^{\mathrm{p}}(k)$ denotes the fundamental wave current component of the predicted current at (k+1)$^{\mathrm{th}}$ instant and k^{th} instant, respectively. And the coefficients of the filter are set to $\gamma=0.9$.

Then, the harmonic current in the predicted current is determined by the discrepancy between the predicted current $i_{\mathrm{s2}}^{\mathrm{p}}(k+1)$ and the fundamental current $i_{\mathrm{sf}}^{\mathrm{p}}(k+1)$, denoted as

$$i_{\mathrm{sh}}^{\mathrm{p}}(k+1)=i_{\mathrm{s2}}^{\mathrm{p}}(k+1)-i_{\mathrm{sf}}^{\mathrm{p}}(k+1) \quad (14)$$

Finally, the obtained harmonic current components are introduced into equation (12) to reduce the harmonic currents generated when the switching frequency is reduced. Therefore, equation (12) is extended to

$$\begin{aligned}J_2=&\left[i_{\mathrm{d}}^{*}-i_{\mathrm{d2}}^{\mathrm{p}}(k+1)\right]^{2}+\left[i_{\mathrm{q}}^{*}-i_{\mathrm{q2}}^{\mathrm{p}}(k+1)\right]^{2}+H_2 f_2\\&+X\left[\left(i_{\mathrm{dh}}^{\mathrm{p}}(k+1)-0\right)^{2}+\left(i_{\mathrm{qh}}^{\mathrm{p}}(k+1)-0\right)^{2}\right]\end{aligned} \quad (15)$$

where X denotes the value of the weighting factor among the current derivative and the harmonic currents, and X is set to 1. The core idea control graph of the proposed HCS-SFL-MPCC methodology is shown in Fig. 4.

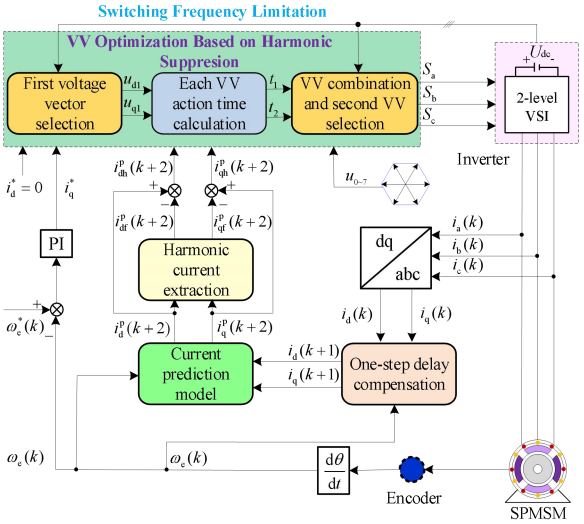

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Fig. 4. Control schematic diagram of the proposed HCS-SFL-MPCC method.

5 Simulation Experiment

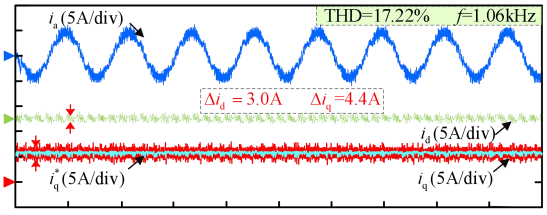
To verify the effectiveness of the proposed HCS-SFL-MPCC method in this paper, this section designs relevant simulation experiments. The parameters of the controlled system are displayed in Table 1. Additionally, for clarity in subsequent discussions, this paper will refer to the method of restricting switching frequency using T-DV-MPCC alone as Method-I. Method-II, which incorporates harmonic suppression (i.e., the proposed HCS-SFL-MPCC method), builds upon Method-I. It should be noted that the coefficients for the switching frequency constraint is the identical for either method, with H_1 = H_2 =H =1.5.

TABLE I

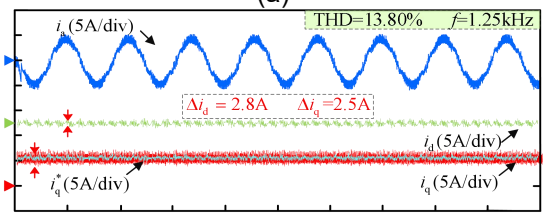
PARAMETERS OF SPMSM

Symbol	Value	Symbol	Value
U_{dc} (V)	310	P_N (kW)	1.25
R (Ω)	3.18	T_N (N-m)	5
L (mH)	8.5	n_N (r/min)	2000
ψ_f (Wb)	0.325	p	2

Firstly, the steady-state performances of the two methods are evaluated and compared at rated torque and different speed conditions, as depicted in Figs. 5-6.

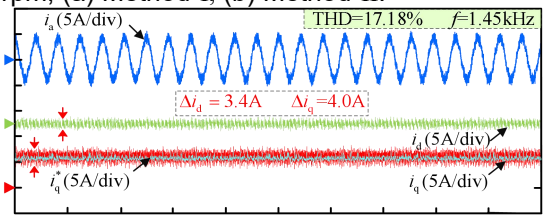


(a)

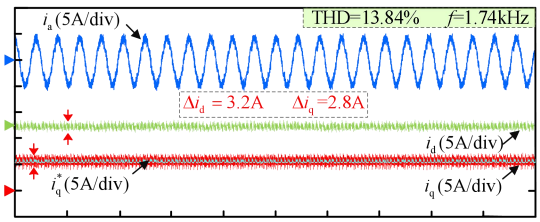


(b)

Fig. 5. Simulation results at rated load and speed of 500 rpm, (a) Method-I, (b) Method-II.



(a)

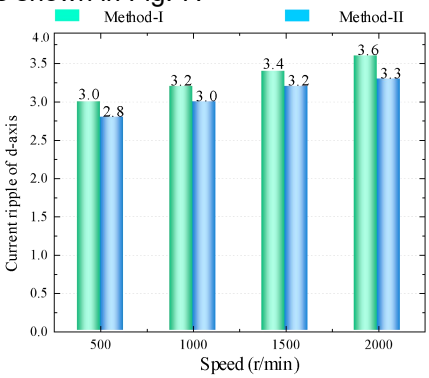


(b)

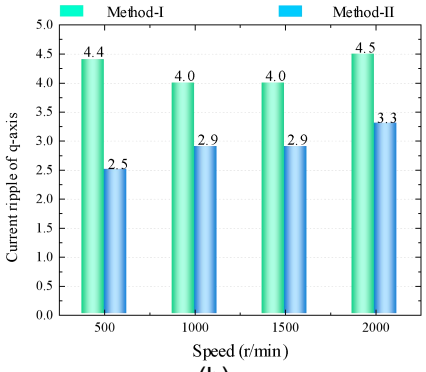
Fig. 6. Simulation results at rated load and speed of 1500 rpm, (a) Method-I, (b) Method-II.

When the switching frequency is reduced, the total harmonic distortion (THD) of the currents in Method-I is 17.22% at 500 rpm and 17.18% at 1500 rpm, accompanied by significant dq-axes current ripple. However, Method-II effectively mitigates the negative impact of reduced switching frequency on the system. It reduces the THD of Method-I to 13.80% and 13.84% at 500 rpm and 1500 rpm, respectively. Similarly, the dq-axes current ripple is also reduced.

To prove more about the advantages of the proposed method in harmonic suppression, this paper also compares the dq-axes current ripple of the two methods across the full speed range under rated torque, as shown in Fig. 7.



(a)



(b)

Fig. 7. Comparison plot of current ripple between Method-I and Method-II across full speed range. (a) d-axis. (b)q-axis.

The information in Fig. 7 exhibits that the dq-axes current of Method-I maintains a large current ripple in the full speed range. However, compared to Method-I, Method-II reduces the d-axis current ripple by 0.2 A, 0.2 A, 0.2 A, and 0.3 A, and the q-axis current ripple

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by 1.9 A, 1.1 A, 1.1 A, and 1.2 A at 500 rpm, 1000 rpm, 1500 rpm, and 2000 rpm, respectively.

Secondly, when the speed is kept at 2000 rpm and the torque is changing, the steady-state performance of the two methods is depicted in Fig. 8-9.

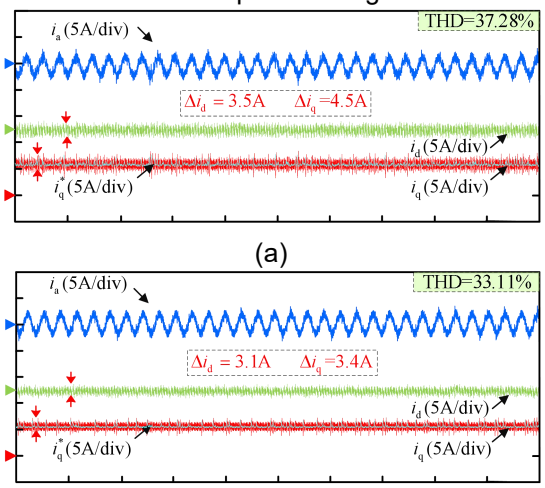

Fig. 8. Simulation results for a speed of 2000 rpm and a torque of 2 N-m. (a) Method-I, (b) Method-II.

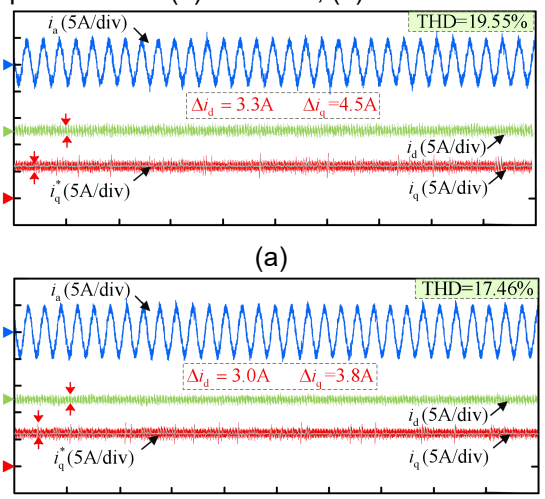

Fig. 9. Simulation results for a speed of 2000 rpm and a torque of 4 N-m. (a) Method-I, (b) Method-II.

Similarly, it can be seen from Figs. 8-9 that the phase current THD and dq-axes current ripple of Method-II are still better than that of Method-I under rated speed and different torque conditions. This indicates that the proposed harmonic suppression method remains effective under various rated torque conditions.

6 Conclusions

To mitigate the harmonic current components caused by reduced switching frequency in the T-DV-MPCC, this paper proposes a harmonic current suppression MPCC method applied to switching frequency limitations. This method achieves reduced switching frequency by restricting the conduction states of the inverter at different instances. Simultaneously, it predicts and extracts the harmonic current components corresponding to each inverter switching state. These harmonic currents are then introduced into the cost function as one of the performance indicators for the entire system, facilitating rolling optimization. This method equalizes the relationship among switching frequency and harmonic currents. Finally, simulation results validate the effectiveness of the proposed method.

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