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Fusion switch concept addresses the cost-performance dilemma in EV powertrains

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Abstract

This paper introduces a simplified approach for a parallel operation of Si IGBTs and SiC MOSFETs in an automotive traction inverter. The so called “Fusion switch” thereby uses one common gate driver and therefore simultaneous switching. In order to achieve a safe but near efficiency optimal operation special requirements have to be fulfilled by the devices to enable this ease of use. The theoretic idea behind this concept is validated in this paper by measurements using well matched EDT3 IGBT/Diode chips with CoolSiC™ SiC MOSFETs in a HybridPACK™ Drive prototype power module. Double pulse measurements confirm the ultra-high switching speed with smooth switching transients. Inverter thermal IR testing demonstrates the pursued current sharing in both, light and full load, inverter operation conditions. Finally, inverter calorimetric tests in comparison to state-of-the-art solutions verify the power loss reduction provided by this Fusion concept in the typical WLTP and CLTC-P drive cycle relevant operation area.

1 Introduction & Motivation Fusion Switch

While market share of electric vehicles has continuously grown in the last decade, the majority of cars sold worldwide are still powered by internal combustion engines. It is beyond all question, that electric powertrains are able to win customers due to their high performance and quiet driving. By employing sufficient battery capacity even long-distance travelling is enabled. In order to offer even longer distance, inverter efficiency is increased by replacing IGBTs with SiC MOSFET. However, to maintain peak performance a lot of expensive SiC chip area is needed, which increases inverter cost. Especially in the high-volume segment, the cheaper silicon IGBT/Diodes solutions are still used due to the cost pressure. The idea to manage peak performance, efficiency and cost by combining Si IGBT and SiC MOSFET has sparked R&D activities for many years. Using both chip technologies in a parallel operation was already investigated in the year 1993 with encouraging results in terms of efficiency gain [1]. Over the last 25 years, research work was published with the focus of a most optimal control of these paralleled devices [2],[3],[4]. The hard & software complexity for optimal control patterns and especially the responsibility for applying patterns, which do not exceed the device ratings, prevented the application in automotive traction inverters.

This paper focus on the so-called “Fusion” concept, which uses one common gate drive for simultaneous switching. The complexity at the customer side is avoided, however special care is now required to design the chipset and power module. On the one hand the target is to achieve a near optimal operation of the devices with respect to efficiency. On the other hand, the parts have to be designed also in a way that extreme conditions like overload, active short circuit and short circuit is not causing critical situations for the devices.

The basic concept of driving the Fusion switch is introduced in section 1.1. The special requirements to the switching devices to enable this ease of use is explained in section 1.2. Chapter 2 discusses the static and dynamic behavior of a prototype close to final application. Chapter 3 demonstrates the performance based on inverter thermal IR camera test bench results. The efficiency gain by means of power loss reduction in the inverter

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system is verified in a calorimetric inverter test in chapter 4.

1.1 Single Gate Drive Fusion Switch

The investigations of this paper are related to a configuration, where one common gate driver is applied to drive simultaneously the SiC MOSFET and the Si IGBT. In modern automotive gate drivers, a dedicated turn-on path with R_{gon} resistor and a turn-off path with R_{goff} is available. For extreme overload conditions these gate drivers have implemented a 3rd path with a dedicated $R_{gsoft(off)}$. For functional safety reasons gate monitoring functions are typically applied, which read the status of the gate voltage and provides active miller clamp during the off-periods. Due to the short circuit ruggedness of the implemented chipset standard DESAT detection feature can be used for short circuit protection. The device temperature is readable via integrated on-die temperature sensor diodes in the power devices. Precise 200 µA current sources and ADC converters implemented on the high voltage side of the gate drivers simplify the readout of these signals in the inverter system. The serial resistor R_s of typical 1 kΩ can protect both, the gate driver and the on-die temperature sensor diodes, from transient current spikes.

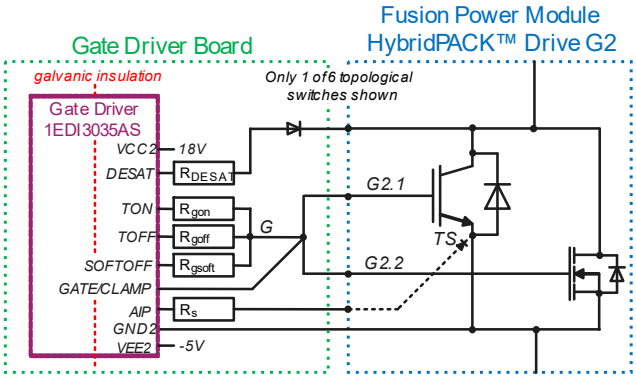

Fig. 1 Fusion switch configuration with one common gate driver for simultaneous switching.

1.2 Requirements for a Fusion Switch

The main inverter working voltages of the actual electric vehicles in development can be classified mainly in 470 V and 850 V power nets [5], where the majority of the cost sensitive high-volume projects still mainly uses the 470 V domain, which will be the focus of this paper. Reviewing the inverter current demand during WLTP class 3 and also the latest CLTC-P [6] drive cycle of a standard size SUV vehicle, about 150 A_{rms} can be seen as a common operation point (see Fig. 2), where efficiency is key to achieve a high driving range from a given battery size. In this efficiency demanding operation around 150 A_{rms}, it is intended to conduct and switch near entirely with the SiC MOSFETs. This assumption is supported by the studies in [8], where the cost optimal solution with latest SiC MOSFET technologies is in a narrow area between 60 and 80mm² chip area per topological switch, well suited to drive the 150 A_{rms} inverter currents efficiently.

For vehicle acceleration events the currents may increase up to 750 A_{rms}, where a Full SiC MOSFET inverter would require a total chip size of about 180 mm² per switch. But in order to avoid the cost of SiC MOSFETs for conditions, which are not frequent occurring, the idea is to utilize the lower cost Si IGBT/Diodes with an area of about 160 mm² and 60 mm² respectively.

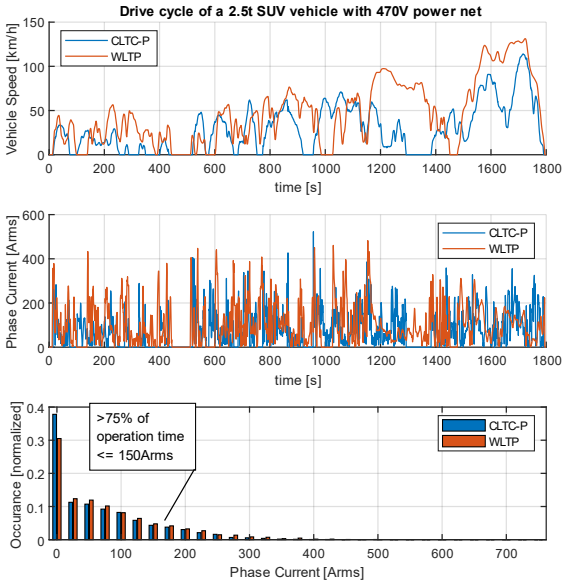

Fig. 2 Comparison of drive cycles CLTC-P and WLTP class 3.

Table 1 Chip utilization requirements for an efficient and safe inverter operation

Operating Mode	Chip Utilization		
	SiC MOSFET	Si IGBT	Si Diode
Light load (0.. 250A_{rms})	Full	**Minimum**	Minimum
Peak load turn-on (500..750A_{rms})	Full (1/3 of total current)	**Full (2/3 of total current)**	Medium to Full
Active Short Circuit	Full	Medium	Full
Short Circuit	Full	Full	n.a.

The main challenge in a Fusion switch using one common gate driver is the fact that during light load the SiC MOSFET current share rate has to be

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maximized and in full load situation it needs to be limited to approximately 1/3 of the total current. This limitation is crucial as the full load current with 1000 A_{peak} over the sinusoidal output would exceed the current density capability of the small MOSFET die area. This maximizing/limiting task seems to be in contradiction with a single gate drive. However, matching chip technologies can automatically fulfill this task as discussed in next chapters.

2 Fusion Switch Characteristics

2.1 Static Characteristics

The Fusion switch combines the output characteristics of an IGBT with a MOSFET. Fig. 3 show with dashed lines the characteristics of both devices' individual. The solid lines are the combination in parallel configuration. It can be clearly seen that the drive cycle relevant area, with 150 A_{rms}, is dominated by the SiC MOSFET characteristics with the near ohmic behavior. The power losses from the IGBT pn-junction drop of about 0.8V (at room temperature) is avoided due to this parallel operation leading to a conduction loss reduction of more than 50% in this important light load area. At high load, the IGBT characteristics support most of the current and the SiC MOSFET only contributes with a decreasing share rate.

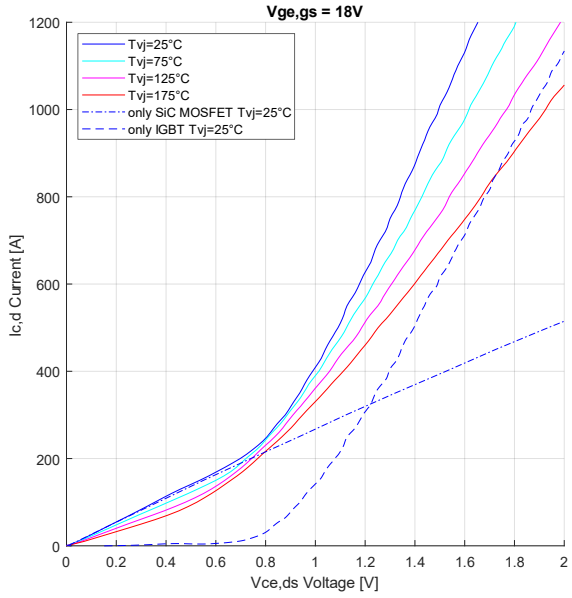

Fig. 3 Output Characterisitcs of the Fusion switch with contribution from SiC MOSFET and Si IGBT

In the rectification mode the SiC MOSFET shares the current with the Si diodes. Due to the high pn-junction drop of the Si diodes the MOSFET dominates the conduction in active freewheeling up to nearly 300 A and the conduction losses in the 150 A_{rms} load point are reduced by more than 75%. At high load currents the Si diodes support the MOSFETs, which is also needed in order to achieve a datasheet specified I^2t capability of 14.5 kA^2s (i.e. 1700 A peak current at a 10 ms half sine pulse event) at $T_{vj,max}$. This robust I^2t behaviour ensures that customers can achieve a safe state in system failure conditions, which require active short circuit of the motor windings [11].

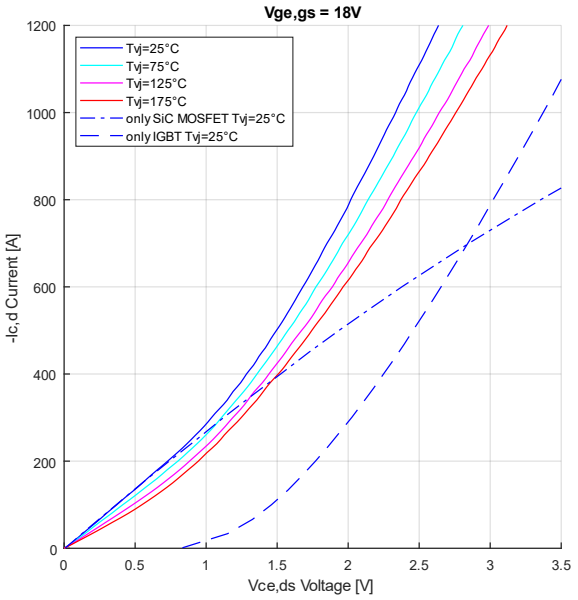

Fig. 4 3rd quadrant output characterisitcs of the Fusion switch with contribution from SiC MOSFET and Si Diode in active rectification

2.2 Dynamic Characteristics

2.2.1 Turn-on

Fig. 5 shows the turn-on switching waveforms of the Fusion switch. In the light load area (represented by a switching waveform with 400 V, 150 A) the switch shows a smooth fast turn-on waveform. The 150 A current is fully provided by the SiC MOSFETs and also after the turn-on event the current remains mainly in the SiC MOSFETs as the forward voltage drop does not reach the knee-voltage of the IGBT.

At full load (represented by a 400 V 900 A switching waveform in Figure 5) it can be clearly seen that a second di/dt slope becomes visible at about half of the turn-on current. The IGBT starts the turn-on event later than the SiC MOSFET, but provides the faster turn-on slope and takes the major-

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ity share rate of the total switched current. The optimal switch utilization stated in Table 1 is given at both, light load and full load condition, despite just having one simple gate drive command in simultaneous switching. It has to be clearly noted that this switching behavior is not possible with most of the available IGBT technologies, but the EDT3 technology [9] is specifically designed for high current densities and fast turn-on switching speed, which is in this use-case of the Fusion switch a mandatory requirement to match with the SiC MOSFET.

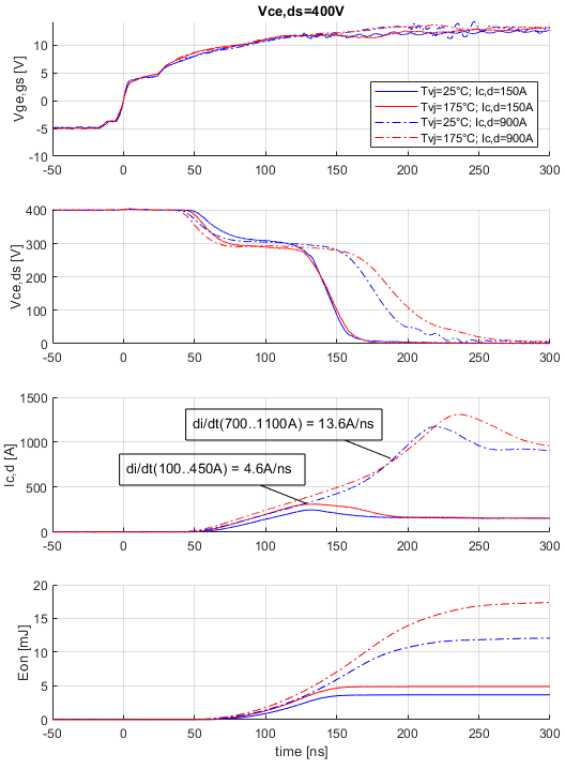

Fig. 5 Turn-on switching waveforms at 400 V for 150 A and 900 A at 25°C and 175°C

2.2.2 Turn-off

Fig. 6 show the turn-off switching waveforms at the same conditions as the turn-on in the previous section. A design critical item for Fusion switch is the fact that the small SiC MOSFETs die areas will not be able to handle the full inverter currents. In order to prevent excessive currents from the SiC MOSFET and risk of damage over lifetime it is important that the MOSFET is not turning off too late with respect to the IGBT. The EDT3 IGBTs and SiC MOSFETs were designed in this Fusion switch in such way that the IGBT in all conditions takes the full turn-off currents. This might look contradicting with studies in the past like [1]-[4], but due to the extreme short conduction times of less than 150 ns, the EDT3 IGBT will not show the classical turn-off losses – it is similar to the case where ZVT switching is provided, but without having the risk of transient overload currents in the small SiC MOSFET dies. In the switching waveforms of Fig. 6 a very minor increase in the $V_{ce,ds}$ voltage at 120 ns can be seen, which is exactly the event where the MOSFET turns-off and shifts the currents for the remaining about 100..150 ns in the IGBT. This switching mode leads to ultra-low switching energies, especially in the light load conditions, which become visible in the 3D mesh diagram of Fig. 7.

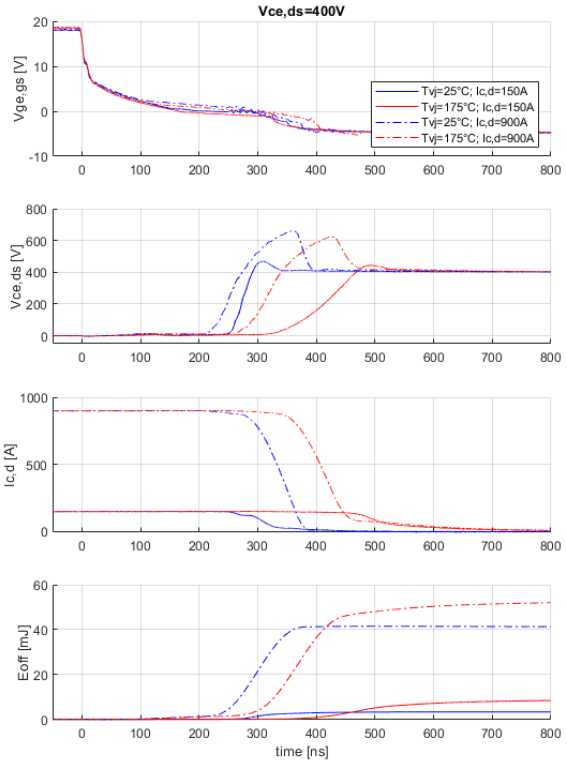

Fig. 6 Turn-off switching waveforms at 400 V for 150 A and 900 A at 25°C and 175°C.

The Fusion switch does not anymore follow the near linear dependency of $E_{off}(I_{c,d})$, which improves the drive cycle efficiency but brings challenges for behavioural models, which in most cases assume linear or 2nd order polynomial functions of $E_{off}(I_{c,d},V_{ce,ds})$ [10] for loss calculations. Therefore, special requirements to the system simulation tools arises from this new behaviour, which will be focused in future publications. Also, it has to be clearly mentioned that studies with testing only low currents [12] and extrapolation to 5-10 times of the measured currents will likely lead to wrong (i.e. too

optimistic low losses) conclusions. For high current automotive traction inverters, it is mandatory to use test devices and packages similar to the final application.

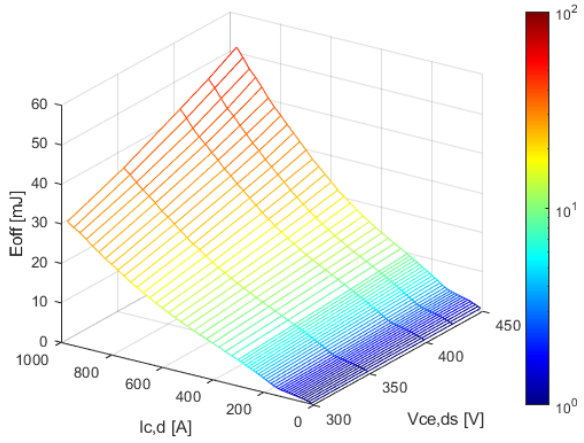

Fig. 7 Turn-off energies measured in small steps from 300..450 V and 0..1000 A at T_{vj}=25°C.

2.2.3 Active rectification Diode turn-off

In contrast to classical Si IGBT/Diode power modules the Fusion switch with additional SiC MOSFETs provides synchronous rectification capability during the freewheeling periods. Fig. 8 shows the active rectification Diode turn-off event at the same conditions as for the turn-on/off events from previous sections. Before 0 ns the MOSFET channel contributed to the conduction of the freewheeling current. A smooth transition without any spikes is observed when the SiC MOSFET gate is turned-off and thus the MOSFET body diode together with the Si diode take the currents. At higher currents (in the plot 900 A condition is shown) the missing active rectification can be seen by already minor increase of the switching energy. The final commutation of the diodes due to complementary switch turn-on command is fast and ultra-smooth in comparison with full SiC MOSFET solutions, which show typical major oscillations at such slopes (see also comparison of waveforms in [7]). Due to the absence of critical voltage overshoots it is possible to turn-on the switches as fast as shown in the section 2.2.1.

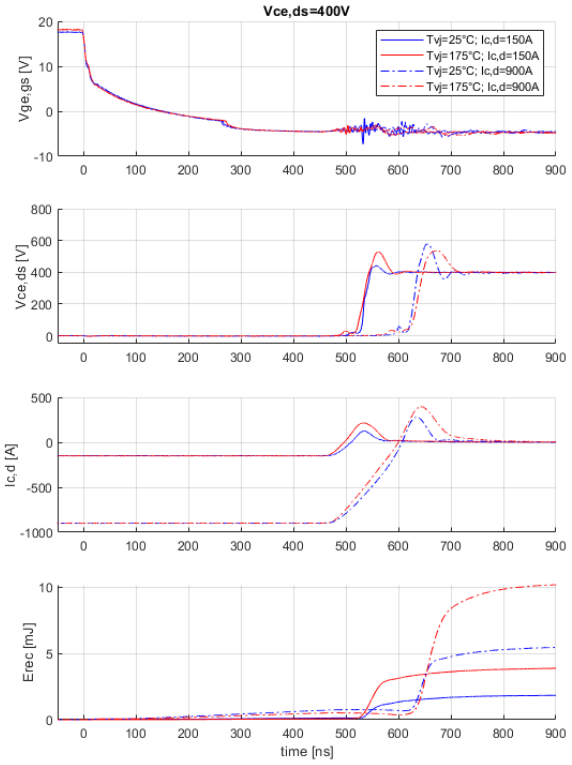

Fig. 8 Active rectifier and Diode turn-off switching waveforms at 400 V 150 A and 900 A at 25°C and 175°C.

2.2.4 Signal dead times for active rectification

All the waveforms in this chapter are plotted with time axis 0 ns at the point where the gate voltage command from the gate driver starts. At turn-off, the longest delay from gate command to switching event occur at light load. At turn-on the shortest delay is observed also at light load. Similar to classical power modules, the minimal signal deadtimes can be characterized at zero load condition. In the experimental tests, 300 ns signal deadtime is the optimal case. The inverter tests in the following chapter are performed with conservative constant 500 ns. A more detailed optimization of the deadtime similar to research studies in [13] is planned in future publications.

3 Inverter Thermal IR measurements

In order to verify the outstanding static and dynamic behaviour results from the curve tracer and double pulse testbench, a prototype Fusion power module is tested also in an inverter thermal IR camera testbench with an inductive load. Fig. 9 shows on the left area an open power module with

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the chip locations. In order not to disturb the switching behaviour a gate driver board was designed in such way that the SiC MOSFETs are directly visible during the operation from top view. The IGBT temperature can be monitored directly via the on-chip temperature sensor diodes. It is possible to monitor the IGBT temperatures via IR camera, which has to be placed in a front view with a pitch angle (see bottom right in Fig. 9). With this setup it is ensured that the devices under test behave identical to real inverter application in contrast to setups where the device under test is connected via coax-cables or rigid-flex adapter PCBs. The thermal IR pictures are done with black painted power modules at high emission rates of 0.95, but for illustration the power modules are shown before the colouring preparation.

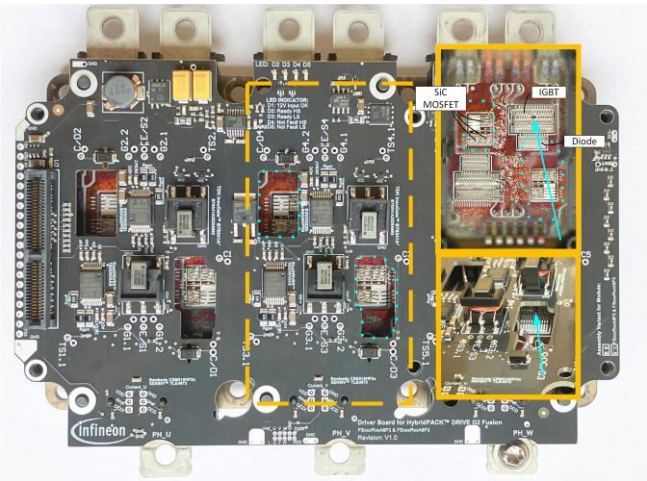

Fig. 9 Fusion power module in the inverter testbench. The gate driver board was designed with board-cutouts for thermal IR camera measurements during the operation.

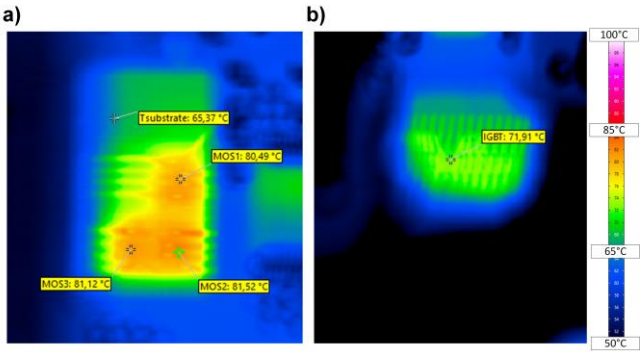

Fig. 10 Thermal IR pictures during the inverter operation of 150 A_{rms}.

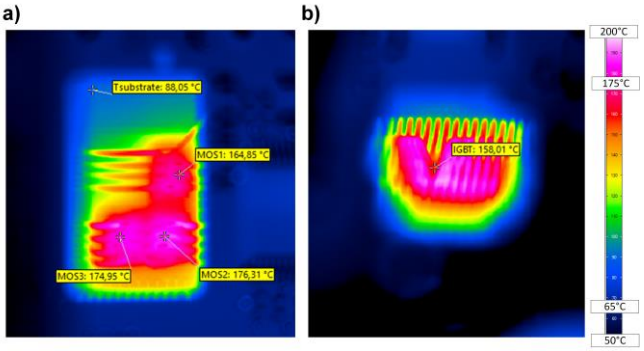

Fig. 11 Thermal IR pictures during the inverter operation of 725 A_{rms}.

Fig. 10 and Fig. 11 show the resulting IR camera pictures of the SiC MOSFET and IGBT/Diode chipset at light load 150 A_{rms} and high load 725 A_{rms}. The inlet fluid temperature is constant 65°C at a flow rate of 8 L/min. The switching frequency is constant 10 kHz at 400 Vdc at the DC-link capacitor. The pictures are from the hottest topological switch close to the fluid outlet.

In the 150 A_{rms} light load operation of Fig. 10, the IGBT has a temperature delta of $\Delta T = T_{vj} - T_{fluid} \approx 7K$. At the same time the SiC MOSFET showed a $\Delta T \approx 16K$, which is twice as high as for the IGBT. As intended in Table 1, light load is dominated by operation of the SiC MOSFETs.

In the high load operation point of Fig. 11, the Si IGBT and SIC MOSFET show a much more homogenous temperature with 10% difference as the IGBT takes most of the high current share rate. A potential thermal improvement can be also derived from the thermal IR pictures. The three SiC MOSFET dies were placed in a L shape, where the two dies next to each other have a high thermal coupling. It is subject for future improvement to place the dies in a straight row with balanced thermal stress. Nevertheless, the prototype clearly shows the light load efficiency improvements and demonstrate the high peak power performance with respect to the small implemented total die area.

4 Inverter Calorimetric Test Results

The Fusion power module prototype as well as latest IGBT power module FS1150R08A8P3 power module as well as 1 mOhm full SiC MOSFET power module FS01MR08A8MA2 (all DUTs implement the latest released automotive chip technologies in HybridPACK™ Drive G2 package) are

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tested on an adiabatic calorimetric inverter testbench. The method is explained in detail in [14] with discussion of the accuracy advantages compared to classical electric input/output measurements via power analyzer. In brief the method is performed as follows: The entire inverter is placed in a near ideal thermal isolated environment (i.e. no fluid cooling and minimized free air convection due to thermal packing in thermal isolation material). In a first step the inverter is fed with DC power losses, which can be accurately measured electrically. Due to the thermally isolated setup the power losses are stored as heat in the thermal capacitances of the inverter stack. The elapsed time to increase the power module temperature from e.g. 50°C to 100°C, correlate with the total power losses of the inverter system. In the test of the Fusion prototype inverter the following correlation was measured:

$$P_{\mathrm{loss}} = \ 5139 \cdot t_{\mathrm{r}}(50..100°C)^{-0.7107}$$

It has to be noted that this correlation is accurate only for the exact identical setup. As soon as any part in the setup like DC-link capacitor, thermally isolated cooler jacket, load terminal busbar, the power module itself, etc. is changed a new calibration is mandatory.

In the second phase the inverter is operated in the exact identical setup but is now modulated to output sinusoidal currents at 10 kHz switching frequency. The total power losses can now be obtained by measurement of the temperature rise time. Another advantage of this method is the fact that it includes all losses in the inverter system, not only the chip related power losses.

The test results are depicted in Fig. 13. At ultra-light load of 25 A_{rms}, the Fusion prototype power module reduced the total inverter power losses by 1/3 compared to the IGBT power module. At 150 A_{rms} more than 300 W power losses were avoided. The power module with full SiC MOSFET chip content still provides the benchmark lowest total power losses, but it comes with the penalty of significant higher power module cost. In this context of cost/performance a new benchmark value for Fusion power modules is proposed with following nomenclature:

$$\text{"Efficiency Gain"} = \frac{P_{\mathrm{loss,Fusion}} - P_{\mathrm{loss,IGBT}}}{P_{\mathrm{loss,SiC}} - P_{\mathrm{loss,IGBT}}}$$

Using only 30% of the expensive SiC MOSFET die area in the Fusion power module already more than 70% of the efficiency gain of the full SiC MOSFET was achieved in average over the WLTP and also the CLTC-P drive cycle.

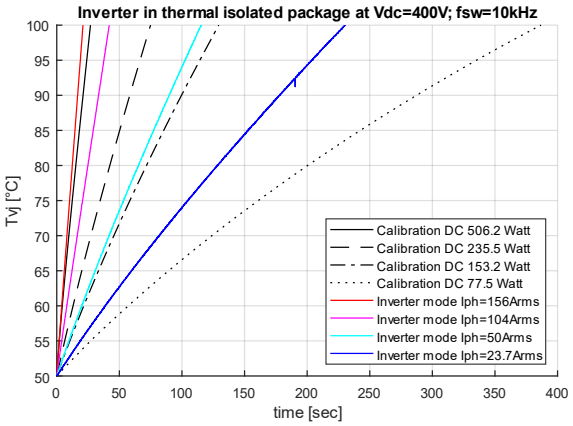

Fig. 12 Calorimetric inverter test with the Fusion prototype power module in a thermally isolated package.

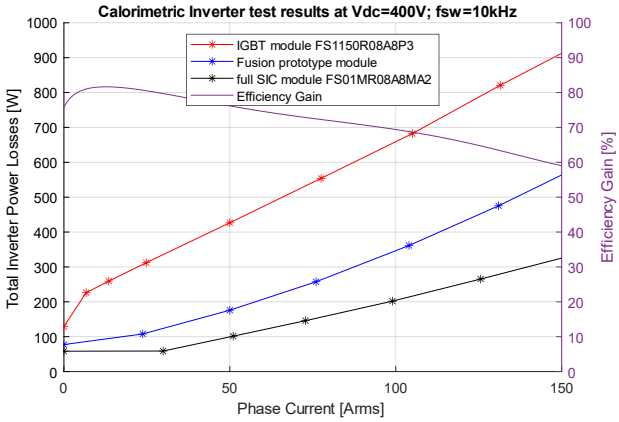

Fig. 13 Calorimetric inverter test results of IGBT, full SiC MOSFET and Fusion power module with latest chip technologies.

5 Summary and Outlook

This paper introduces the Fusion switch concept with simultaneous gate drive of the paralleled Si IGBT and SiC MOSFET switching devices. Despite losing the ability of individual control of the two devices the paper shows the possibility of an efficient inverter operation by means of matching IGBT and SiC MOSFETs characteristics. At light load the operation is dominated by the efficient SiC MOSFETs and at high load the cheaper and larger die area of the Si IGBT/Diode supports most of the current. Using only 30% of the expensive SiC MOSFET die area in the Fusion power module already more than 70% of the efficiency gain of the full SiC MOSFET power module was achieved for both profiles, the WLTP and also the CLTC-P. The results are validated by double pulse tests, in-

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verter thermal IR tests and also by calorimetric inverter tests. Due to ease of use the concept is ready for high volume automotive projects, which requires the contradicting topics low cost and high efficiency at the same time.

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7 Appendix

All tests for the paper were done with the following settings and the 1EDI3035AS Gate Driver:

VCC2 = 18 V

VEE2 = -5 V

R_{gon} = 1.27 Ω

R_{goff} = 1.0 Ω

R_{gsoft} = 22 Ω

R_s = 1 kΩ

R_{DESAT} = 3.3 kΩ

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