A 150 & 200mm engineered substrate increasing SiC power device current density up to 30%

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Abstract

The Smart Cut™ technology enables the integration of high quality SiC layer transfer for device yield optimization, combined with a low resistivity handle wafer (below 5mOhm.cm) to lower device conduction and/or switching losses both for 150mm and 200mm wafers diameter. Based on material characterisation, we anticipate a benefit of up to 15% or 30% in terms of RDSon for state of the art 1200V SiC MOSFET and JFET. 1200V SiC diodes and MOSFETs have been fabricated by Fraunhofer IISB. 1200V diodes (JBS and MPS) with voltage drop improvement by 12% at rated current have been demonstrated.

1 Introduction

Silicon Carbide (SiC) technology has emerged as a crucial component in the realm of power electronics, playing a pivotal role in propelling electric mobility forward and enhancing the harnessing of renewable energy sources. The surging demand for SiC in the market has placed significant pressure on power semiconductor companies to rapidly scale up their production capabilities. Despite notable advancements in the quality and availability of 4H-SiC material, the quest for low defect density wafers to ensure high yields persists as a main challenge.

In response to this pressing need, a groundbreaking SiC engineered substrate has been introduced to address the industry's requirements [1-4].

2 Substrate description

The Smart Cut™ technology (fig.1) is a significant advancement in the field of semiconductor manufacturing, particularly for Silicon Carbide (SiC) devices. Here's a detailed breakdown of its features and benefits:

1.High-Quality SiC Layer Transfer: The technology enables the integration of high-quality SiC layer transfer, which is crucial for optimizing device yield.

2.Low Resistivity Handle Wafer: By incorporating a low resistivity handle wafer with a resistivity of less than 5mOhm.cm, the technology enhances device conduction and/or reduces switching losses. This feature is essential for improving the overall efficiency and performance of SiC-based devices.

3.Compatibility with Different Wafer Diameters: The Smart Cut™ technology is scalable to both 150mm and 200mm wafer diameters, providing flexibility in manufacturing processes and meeting various application requirements.

4.SmartSiC™ Engineered Substrate Composition (fig.2): The engineered substrate consists of a thin layer (400 to 800nm) of high-quality 4H-SiC bonded on top of a 350µm thick polycrystalline SiC (pSiC) handle wafer. This composition ensures structural integrity and performance while contributing to the reliability and efficiency of SiC devices.

5.Efficient Utilization of SiC Boule Materials: The reusability of initial single crystal donor wafers significantly enhances the efficiency of SiC boule material usage. Compared to conventional wafering technology, which typically yields a maximum of 50 wafers per boule, the Smart Cut™ technology enables the preparation of up to 500 wafers from the same boule. This substantial increase in yield represents a significant cost-saving and resource-efficient solution for SiC device fabrication.

Overall, the Smart Cut™ technology offers a comprehensive solution for optimizing SiC device manufacturing processes, enhancing device performance, and maximizing the utilization of SiC boule materials. These benefits make it a valuable

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advancement in semiconductor technology, particularly for applications requiring high-performance SiC devices.

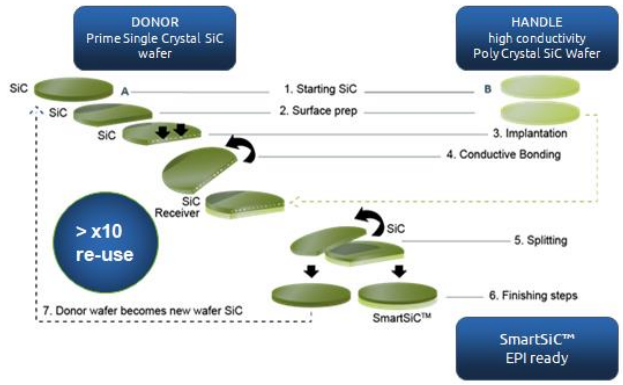

Fig. 1. Smart Cut™ technology adapted to silicon carbide

Fig. 2. 150mm & 200mm SmartSiC™ substrate ready for SiC drift epitaxy

Through the utilization of high material doping, the electrical resistivity of the pSiC substrate is significantly reduced by a factor of at least 4, up to 10, in comparison to conventional single crystal SiC (mSiC) wafers. It guarantees an electrical resistivity of less than 5 mOhm.cm, with typical values falling within the range of 1 to 2 mOhm.cm. Employing CVD technology ensures consistent performance across wafers for substrate diameters of both 150mm and 200mm. This uniformity can be replicated using various material sources, which is a critical aspect for industrial applications, as depicted in figure 3.

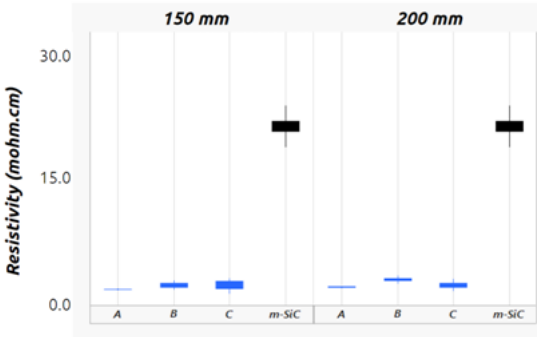

Fig. 3. Electrical resistivity distribution of pSiC (A, B, C sources) compared to mSiC substrate.

The electrical conductivity achieved through high material doping remains consistent from room temperature (25°C) to the maximum operating temperature of devices (175°C), as indicated in Table 1. This table compares the electrical resistivity of single crystal SiC, pSiC, and the SmartSiC™ wafer bonding interface across the entire temperature range [5].

Temperature	25°C	175°C
4H-SiC bulk [mOhm.cm]	15 – 25	15 – 25
Bonding Interface [mOhm.cm²]	0.003 – 0.006	0.002 – 0.006
Handle pSiC bulk [mOhm.cm]	1.5 – 2.2	1.7 – 2.5

Table 1: Electrical resistivity for each SmartSiC layer, from 25°C to 175°C

Polycrystalline SiC handle wafers are prepared through the chemical vapor deposition (CVD) technique. This process is much more energy-efficient than the conventional physical vapor transport (PVT) used to manufacture mSiC wafers, cutting CO_2 emissions of the final SmartSiC™ product by at least 70% compared to conventional single crystal SiC.

3 Device experimental conditions

The fabrication of 0.09mm² 1200V JBS diodes and MPS diodes (with areas of 2.5 and 6.12mm²: see figure 4) has been performed in collaboration with Fraunhofer IISB. In parallel 1200V SiC planar MOSFETs are also being fabricated.

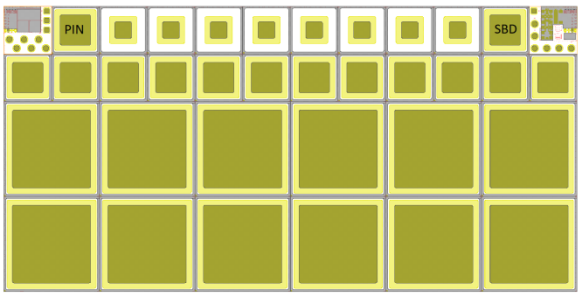

Fig. 4. Test mask for SiC diodes fabrication.

Diode devices were fabricated with both commercial 150 mm 4H-SiC wafers and 150mm SmartSiC™

engineered substrate processed in parallel for both epitaxy and device fabrications. The drift layer is an n-type epitaxial layer of 11µm thickness and $1.10^{16}cm^{-3}$ doping concentration. This epitaxial layer is designed for a 1200 V blocking capability. The die thickness was reduced down to 340µm. The rated current ranges from 1A for 0.09mm² JBS diodes, 4A and 9A for respectively 1.6x1.6mm and 2.5x2.5mm MPS diodes. P+ doped layers are 500nm deep with a width of 2.5µm and 2.0µm respectively for JBS and MPS diodes.

For the front side metallization (fig.5), we deposited (through evaporation) 80 nm Ti and 300 nm Al on the p+-regions and annealed via RTP (980°C during 2min under Argon). On top (and on the n- region) we sputtered the power metal (50 nm Ti, 3500 nm Al and 20 nm Ti), which also builds the Schottky contact on the not-implanted epi layer.

For the back side metallization, we deposited (through sputtering) 60 nm $NiAl_{2.6\%}$ and use laser annealing on 4H-SiC to create the ohmic contact, on top of that we sputter 2000 nm Al and then evaporate the solder stack – 100 nm Cr, 1000 nm Ni and 1000 nm Ag. For the SmartSiC substrate, no laser annealing was performed.

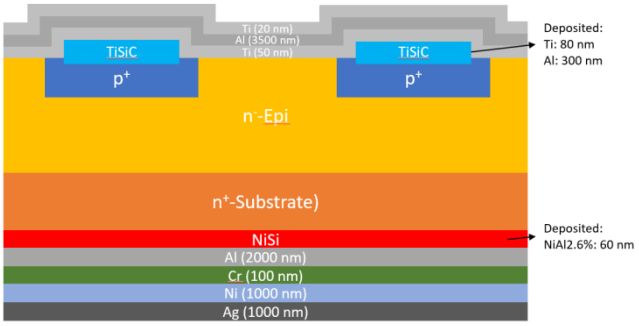

FIG. 5. METAL STACKS FOR FRONT AND BACK SIDE.

4 Device results

4.1 JBS diodes

For 1200V JBS diodes, we have performed wafer-level 300x300µm² forward (see fig.6) and reverse characteristics (see fig.7). No critical change in the reverse characteristics is observed. Forward characterization shows a forward voltage drop lowering at the rated voltage.

Reverse I-V characteristics of JBS diodes manufactures on SmartSiC™ substrates are shown in Fig. 8. Despite some device failures below the targeted voltage, the tested diodes reached the targeted voltage with a current leakage below the specifications.

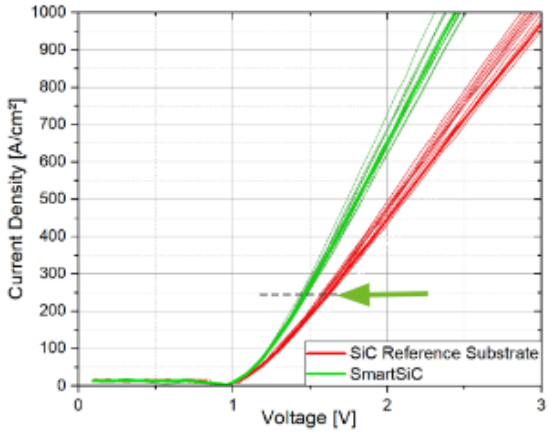

Fig. 6. Forward characteristics of JBS diodes manufactured on mSiC (red lines) and SmartSiC™ substrates (green lines).

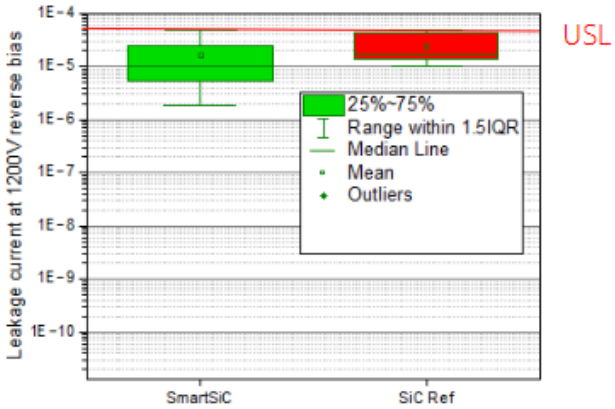

Fig. 7. Leakage current at a reverse bias of 1200V for the JBS diodes manufactured on mSiC (red box) and SmartSiC™ substrates (green box).

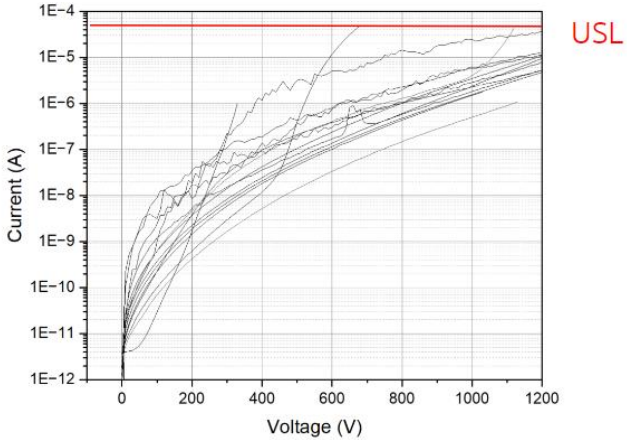

Fig. 8. Reverse current of JBS diodes made on SmartSiC™ substrates.

4.2 MPS diodes

For 1200V MPS diodes, we first report wafer-level forward characteristics. Voltage drop lowering at the respectively rated currents of 4 and 9A for 1.6x1.6mm² (see Fig.9) and 2.5x2.5mm² (see Fig.10) MPS diodes,

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is around 12%. A first extraction of the dynamic resistance of the forward regime (2 to 10A) of the MPS diodes leads to a benefit (linked to SmartSiC™ transition) of around 0.9mOhm.cm². This is even beyond the expected gain linked to the improved material resistivity: around 0.77 mOhm.cm². This further gain is supposed to be linked to the lower contact resistance of the back side contact coming from the high level of doping in the pSiC [3].

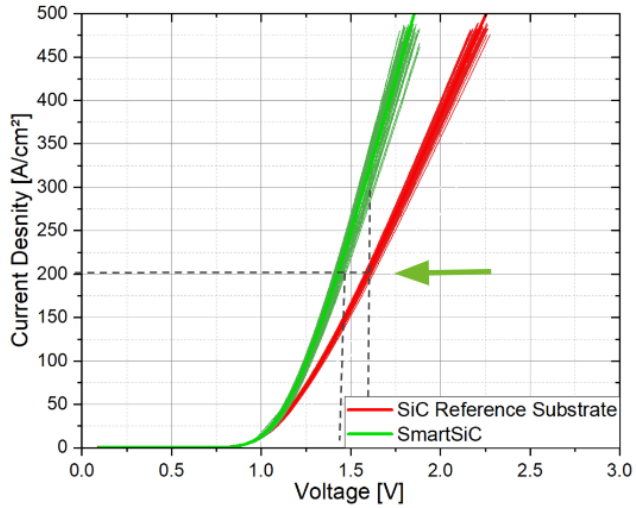

Fig. 9. Forward characteristics of MPS diodes manufactured on mSiC (red lines) and SmartSiC™ substrates (green lines). 1.6x1.6mm², 6A rated MPS diodes.

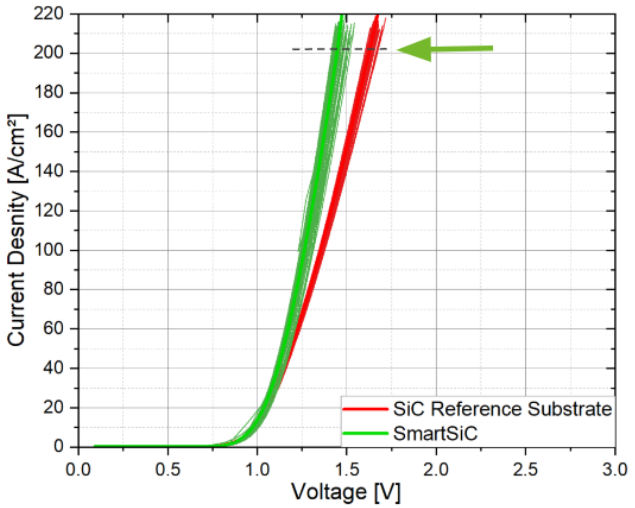

Fig. 10. Forward characteristics of MPS diodes manufactured on mSiC (red lines) and SmartSiC™ substrates (green lines). 2.5x2.5mm² 10A rated MPS diodes.

Reverse bias leakage at 1200V (see Fig.11) is slightly higher for the SmartSiC™ samples. This is attributed to the 20% higher doping level which lowers the breakdown voltage.

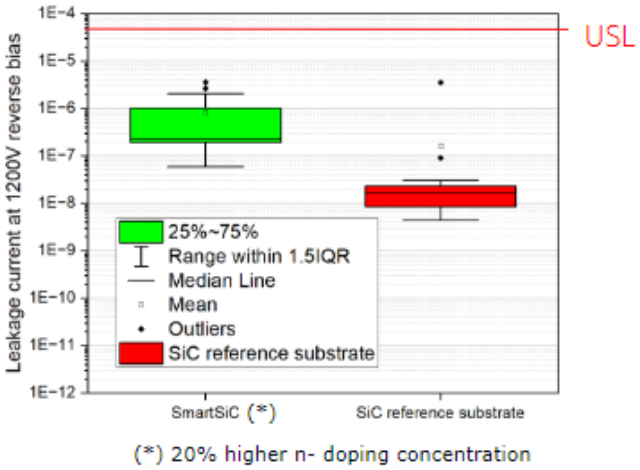

Fig. 11. Leakage current at a reverse bias of 1200V for the MPS diodes manufactured on mSiC (red box) and SmartSiC™ substrates (green box).

Reverse I-V characteristics of PIN diodes made on SmartSiC™ substrates are shown in Fig. 12. Again, despite some device failures below the targeted voltage, the tested diodes reached the targeted voltage with a current leakage below the specifications. This is showing that SmartSiC™ engineered substrate is fully compatible with SiC power device fabrication and reaches the targeted device leakage levels.

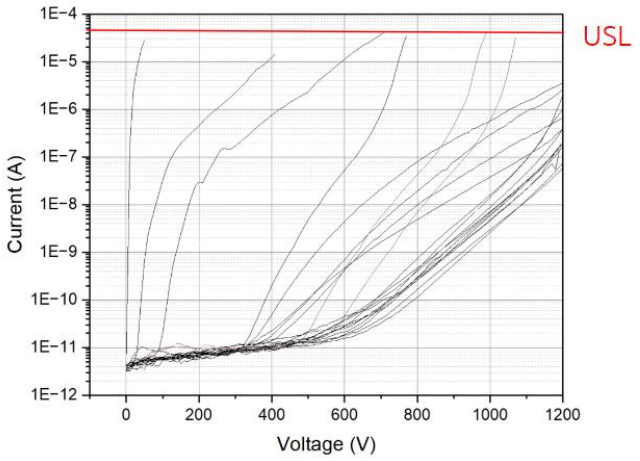

Fig. 12. Reverse current of PiN diodes made on SmartSiC™ substrates.

5 Device performance perspectives

SmartSiC™ enables an increase of the current density at the device level thanks to both the polycrystalline SiC material's low resistivity and the lowered back side contact resistance. Compared to standard single crystal SiC substrate with a material electrical resistivity around 20mOhm.cm, the polycrystalline SiC material

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can reach material resistivity as low as 2mOhm.cm. In parallel, thanks to the high doping level of polycrystalline SiC, the contact resistance is lowered around 10-50 µOhm.cm². Associated with substrate selection and/or specific surface preparation prior to Smart Cut™ that will guarantee the best yield, the technology will enable a lowering of the total cost of ownership of power devices.

To investigate the advantages of SmartSiC™ engineered substrates versus standard single-crystal 4H-SiC wafers, n-type, 13mOhm / 650V Gen2 planar SiC MOSFETs were manufactured on both types of substrates and processed simultaneously as a single batch by ST Microelectronics in the framework of the EU funded program Transform.

The comparison of device's RDSon shows an average reduction of the on-resistance of around 24% favorable to the SmartSiC™ substrates [6]. This improvement is due to the much lower resistivity of the poly-SiC handle wafer of SmartSiC™ substrates, as well as its capacity to make much lower resistivity metal contacts (back-side drain contact in this case).

Such a strong reduction of RDSon (~24%) is close to what it can be expected during the transition from a given device generation to the next one.

Now to anticipate the benefits awaited for various 1200V MOSFETs designs of available and foreseen products, we calculated the benefit of the electrical parameters as a function of device specific resistance (Ron.A) at room temperature and die thickness. We clearly see that for Ron.A improvement up to 15% for state of the art 1200V SiC MOSFETs and up to 18% for next generation 1200V SiC MOSFETs, can be envisioned (see fig.13). Considering ultimate SiC MOSFET or state of the art JFET, improvement up to 30% is anticipated.

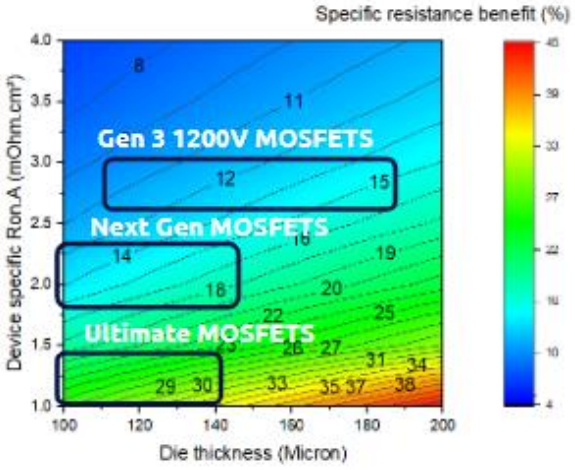

Fig. 13. Ron.A reduction enabled by the use of SmartSiC™ substrates for 1200V SiC FETs.

6 Bipolar degradation benefits of SmartSiC™ material

Bipolar degradation of post epitaxy SiC substrates without diode processing was carried out on reference and engineered SiC substrates using the E-V-C technique developed by ITES, Co. (Japan) [8]. The results suggest that the SmartSiC™ design possesses an inherent advantage over bulk material in terms of robustness against bipolar degradation. This characteristic was previously evaluated through a forward-current stress test conducted on a 4H-SiC epitaxial layer subjected to proton irradiation [7]. It appears that both the number of SSFs and their typical size are lower in the case of SmartSiC™ compared to bulk. We are currently assessing the above characterized MPS diodes under high current density with short pulses to directly check the bipolar degradation [9].

7 Conclusion

In conclusion, we are demonstrating that the SmartSiC™ engineered substrate solution available in 150 and 200mm diameters will bring a higher current density (up to 30%) both for state of the art SiC MPS diodes and MOSFETs (either planar or vertical). Besides modeling, SiC devices have been fabricated and diodes (JBS and MPS) with voltage drop improvement by 12% at rated current have been demonstrated. Finally we have demonstrated post epitaxy robustness with regards to bipolar degradation. This will be further assessed at device level.

Acknowledgements

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