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Tuning the parasitic JFET resistance for low on-state 1.2kV SiC power MOSFETs

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Abstract

This paper presents a method for extracting the channel and parasitic resistances of small pitch planar 1.2 kV SiC power MOSFETs. In addition, the influence of channel width, cell pitch and JFET doping on the overall device performance is presented. By optimizing the device design and layout, excellent static and dynamic performance is achieved. Test substrates are used for static and dynamic characterization.

1 Introduction

While the commercialization of low-voltage silicon carbide power MOSFETs is taking place in many applications, some fundamental shortcomings in terms of device performance have not yet been addressed. Besides the typical reliability and robustness challenges, it is the comparatively poor performance of the inversion channel that leads to significant on-state losses. Recently, numerous approaches to improve the inversion channel have been reported. While a minimum channel length must be maintained to ensure device blocking capability, increasing the carrier density by reducing the oxide thickness or replacing silicon dioxide with high-k materials is the most promising. Thinner gate dielectrics and new materials in the most critical area of the device raise new questions about long-term reliability and robustness. However, the most common approach is to overcome poor channel performance by scaling device spacing and widths, as reliability is usually maintained [1-3]. A minimum JFET spacing between the active cells must be maintained [4-6]. In this paper, a design study is presented to understand the resistance contributions of the top cell layout and finally achieve maximum performance by scaling the cell spacing, device width and channel length using state-of-the-art techniques.

2 Experimental

Several designs of vertical power MOSFETs with pitches from 5.4 um to 6.4 um were fabricated on 1.2 kV SiC epi wafers. The drift epitaxial layer was chosen rather conservatively with a large margin for blocking. To investigate the influence of scaling on the different parasitic contributions, different design variants were focused on: Three different dosages of the JFET compensation implant were investigated (low/medium/high), while the device spacing was scaled from 6.4 um (p6.4) to 5.4 um cell spacing (p5.4). In addition, two different versions of p-well were used (strong p-well) that interfere with the JFET compensation implant. The cells are arranged in both a stripe and hexagonal layout, shown schematically in Fig.1. All designs were combined with 300 nm and 400 nm physical channel length. In addition to scaling the cell spacing, the gate width was also increased by implementing a cell design. Table 1 gives an overview of the proposed designs.

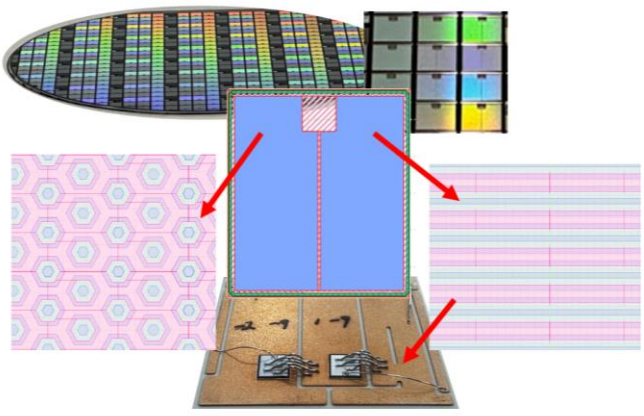

Fig. 1. Overview of the fabricated MOSFET layout and design of experiment. Each pitch and layout were combined with two channel length (300nm / 400nm), 3 variants of JFET compensation and Pwell configuration

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Device type	Pitch (um)	Channel length (nm)	JFET compensation	P- well configuration
A	5.4 stripe	300 / 400	Low / Medium / High	Strong / baseline
B	6.4 stripe			
C	6.4 hex			

Table 1. Design overview of investigated MOSFET layout

3 Results

3.1 Parameter extraction

Fig. 2 shows an exemplary blocking curve that illustrates the blocking behavior at room temperature with V_G = 0 V for the two cell pitches of 6.4 um and 5.4 um. Both designs reach 1600 V, with the leakage rising slightly above 1000 V for the wider pitch. Obviously, the wider cell pitch leads to higher electric fields reaching the channel area from the drain side and thus increasing the blocking leakage. Since the pitch of 6.4 um is the largest in this study, the blocking capability is considered sufficient for all designs used in this work.

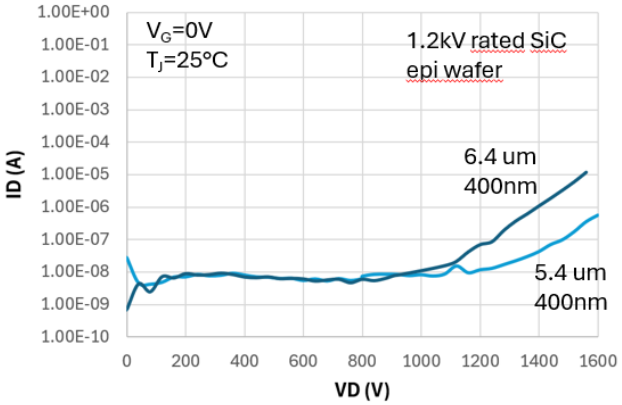

Fig. 2. Exemplary blocking curve of a pitch 5.4 um and 6.4um device with 400 nm channel length at V_G =0 V. The graph shows reasonable blocking capability with a lot of margins over the targeted 1200 V

Fig. 3 shows the method for extracting the parasitic resistance and the effective channel length using the example of a component with 5.4 um spacing. The extracted $R_{DS,on}$ was plotted against the physical channel length for different gate overdrives (V_{ov}). The extrapolation of the corresponding gate overdrive for each channel length crosses at one point and results in the effective channel length difference (ΔL_G) and the parasitic resistance (R_{par}). As can be seen in the graph, a significant reduction in the physical channel length of >150 nm and a parasitic resistance of about 10 mOhm was observed for this device. The parasitic resistance is comprised of all channel-independent resistances such as substrate, contact resistance and the JFET resistance.

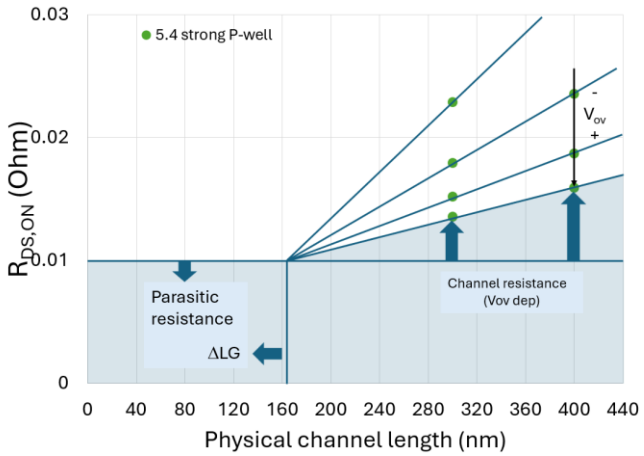

Fig. 3. Extracted exemplary total on resistance ($R_{DS,ON}$) versus the physical channel length for a 5.4 um pitch device with strong p-well layout for various gate overdrive at room temperature. The conjunction point of the extrapolated lines indicates the parasitic resistance at the y-axis intercept as well as the effective reduction of the channel length due to the JFET implant ant process variations (ΔLG).

Fig. 4 summarizes the extracted R_{par} versus ΔL_G for all devices. Increasing the JFET implant reduces R_{par} along with ΔL_G, although it tends to saturate at higher JFET implant dose. As expected, increased channel width (5.4 um & hex) efficiently reduces R_{par}. Interestingly, the p-well design further reduces the effective channel length by >50 nm. Obviously, besides the pure JFET region, the effective channel length is also affected. In addition, the minimum R_{par} seems to be further reduced with a stronger p-well design. While the effect of the channel itself is taken out by the method, a shorter effective channel length effectively leads to a wider JFET region as the JFET spacing was physically maintained. Interestingly, the wider JFET range of the hex6.4 did not lead to a significant improvement in R_{par}. Fig. 5 right shows the extracted specific channel resistance (Rsp) per nanometer gate length at highest gate overdrive compared to the extracted ΔL_G for all device designs. It can be seen from the diagram that, as expected, reducing the effective channel length for a particular design has no effect on Rsp. Only the increased channel width reduces Rsp significantly, as shown for hex6.4.

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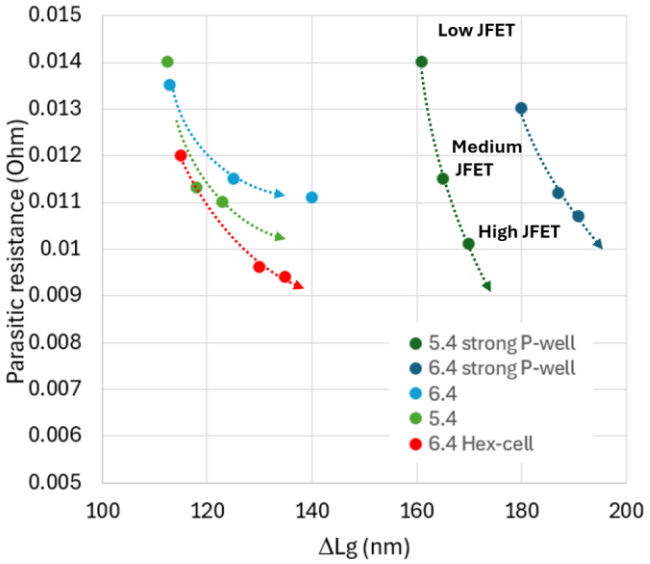

Fig. 4. Extracted parasitic resistance versus channel length reduction ΔL_G for all proposed designs. The different colour indicates the different device type. Each group of points corresponds to low, medium, and high JFET compensation. The guide to the eye line points towards higher compensation implant

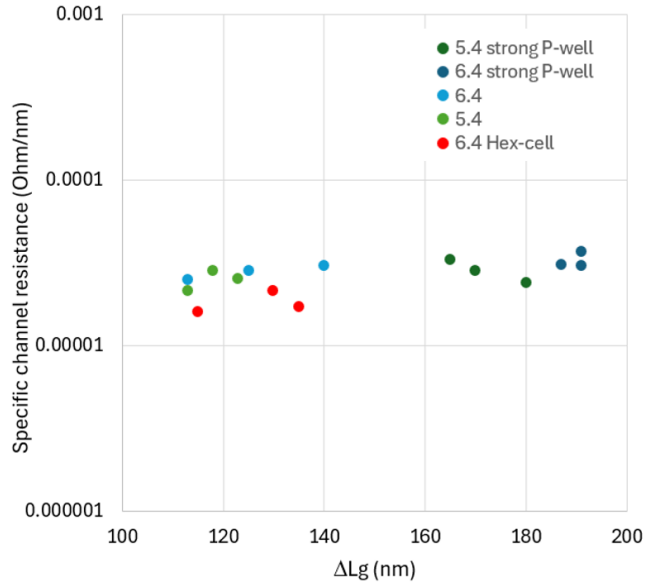

Fig. 5. Extracted specific channel resistance from the smallest slope of Fig 3 extracted at the largest gate overdrive, versus ΔL_G. Each group of points indicate the specific cell layout for all three JFET compensation.

3.2 Static performance

Fig. 6 shows the substrate assembly of selected splits on a test carrier with one MOSFET on the low side (LS) and one on the high side (HS). The selected splits were a medium and a high JFET for pitch 5.4 and a medium JFET for hex6.4. The devices were soldered and wire bonded to ensure the best possible thermal and electrical contact. The on-resistance ($R_{DS,on}$) was extracted for V_G =18 V and T_J from 25°C, 125°C to 175°C. As can be seen in the graph, the temperature coefficient is stronger for medium JFETs than for high JFETs. As expected, the hex cells have the lowest Ron. In addition, the smaller JFET contribution due to the the wider spacing of the hex cells compared to the 5.4 um stripe layouts seems to increase with temperature. At high temperatures, the medium JFETs of hex6.4 even show a lower $R_{DS,on}$ than the p5.4 with high JFET doping. For comparison, three commercially available SiC MOSFETs with comparable chip size were plotted in the diagram (grey dash). The designs used in this study compare very well with the performance, especially at high temperatures. The temperature coefficient was adjusted to have a low Ron at higher temperatures while keeping the Vth as large as possible for all splits. This optimization results in a flatter temperature response.

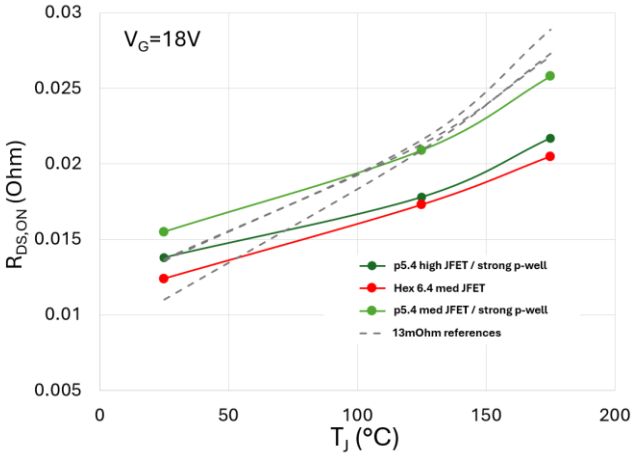

Fig. 6. Temperature dependent on-resistance of selected designs, measured on test substrates for application near parameter characterization, at V_G = 18 V and L_G = 300 nm.

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3.3 Dynamic characterization

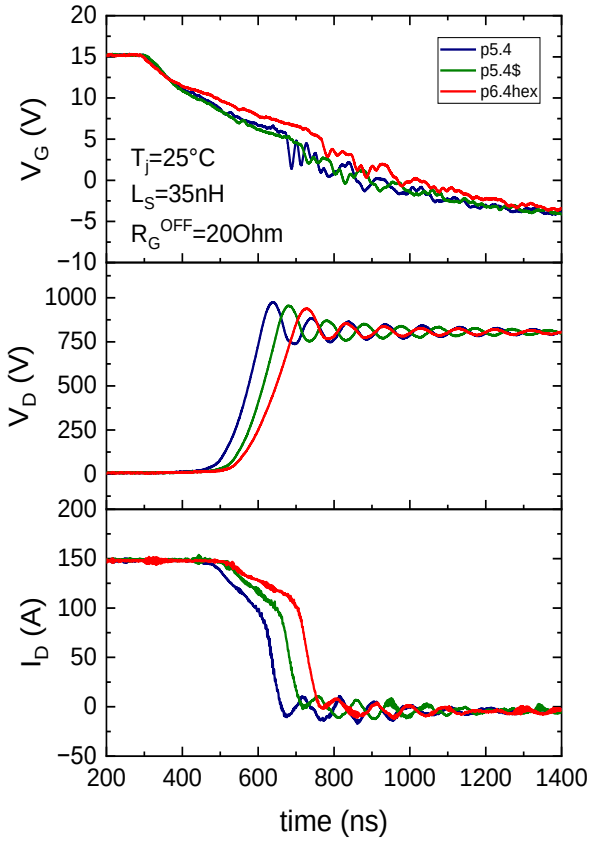

Fig. 7. Turn-off wave forms of a test substrate using one MOSFET on the high side and one MOSFET on the low side with R_G^{OFF} = 20 Ohm and L_S = 35 nH at room temperature. The LS turn-off of a pitch 5.4 device with strong and standard p-well, high JFET and 300nm channel length compared to a hex6.4 med JFET is shown

The dynamic performance was analyzed with the same module as in section 3.2. The substrate layout was designed to ensure fast switching with low stray inductance (LS), which mimics the switching of the module. No auxiliary diodes were fitted as the MOSFET body diode was used during the freewheeling phase. Fig. 7 shows the turn-off waveforms of selected splits at nominal switching conditions. All components show stable switch-off behavior. No strong over-voltages or gate oscillations were observed in any of the splits. Obviously, the hex6.4 shows the slowest turn-off behavior, as the drain voltage and current have a significant delay compared to their stripe counterparts. Considering the higher channel width, this behavior can be explained and is to be expected due to the higher input capacitance C_{iss} and the fixed external gate resistor R_G^{ext}.

Fig. 8 shows the switch-on waveforms of the same devices as shown in Fig. 7. As commonly observed with dynamic switching of SiC MOSFETs, the gate signal suffers from minor oscillations during the turn-on process. It is generally assumed that these oscillations are caused by the body diode turn-on. It is worth noting that the amplitude of these oscillations is not critical, the observed gate voltage remains well within the device limits and in this case remains below V_G = 15V. Similar to the turn-off waveform, the designs show different turn-on behavior. Again, the hex design shows the lowest dV/dt. The p5.4 design with standard p-well has the longest delay time due to a slightly higher Vth, but the dV/dt is only slightly lower than for p5.4 with strong p-well.

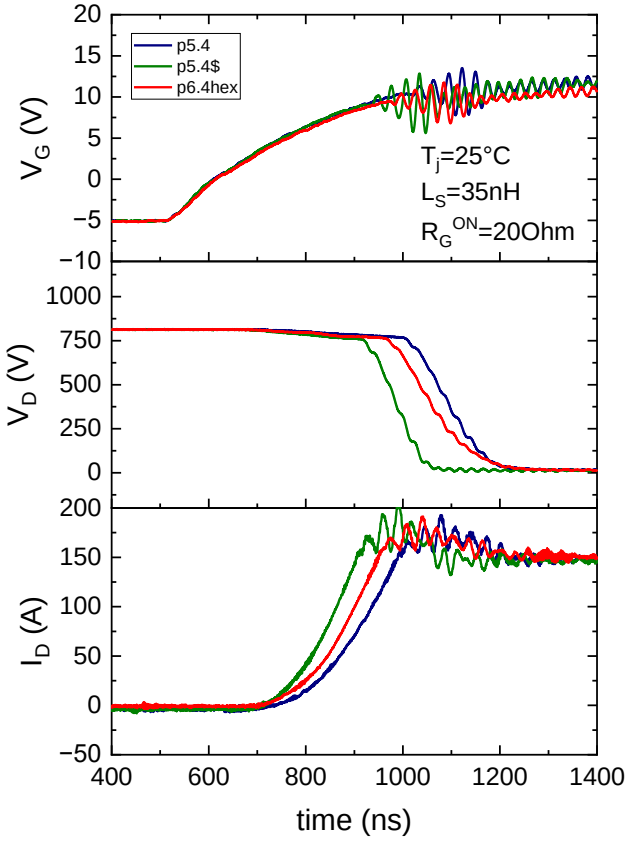

Fig. 8. Turn-on wave forms of a test substrate using one MOSFET on the high side and one MOSFET on the low side with R_G^{ON}=20 Ohm and L_S = 35 nH at room temperature. The turn-on of the same devices as in Fig. 7 is shown

Fig. 9 shows the extracted switching energy of the same designs as a function of different R_G. Good controllability can be observed for both the turn-on and turn-off cases. In particular, the R_G dependence in the case of turn-off is approximately linear. During tun-on, the R_G dependency is weaker and doubles the Eon with an R_G^{ext} approximately 4x greater. As expected from the switching curves, the turn-off energy of the hex6.4 has the strongest R_G^{ext} dependence. Within the stripe designs, the strong p-well has the lowest Eoff energy, although all designs perform relatively similarly. The hex design also shows the strongest R_G^{ext} dependence

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for the switch-on energy (Eon). Remarkably, the two stripe designs with strong p-well show the smallest Eon. In addition, the JFET compensation implant has only a very small influence on Eon.

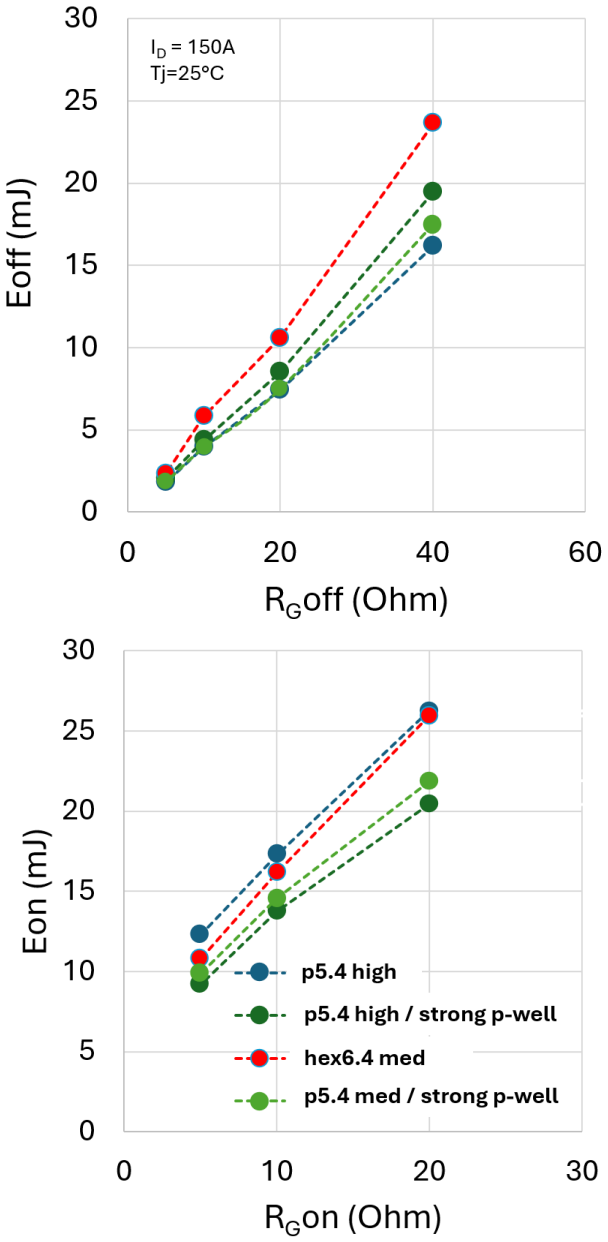

Fig. 9. Extracted switching energy of selected splits versus external gate resistor R_G

The short-circuit drain current at room temperature for the same splits at V_D = 800V is shown in Fig. 10. The turn-on pulse time is between 2us and 3us, which results in an SC current of about 950A to 1050A. It is noteworthy that the p5.4 and the p5.4 mid JFET / strong p-well survive the 3us SC pulse. The hex6.4 and the p5.4 p5.4 high JFET / strong p-well withstand the 2us pulse but fail after the 3us switch-off pulse in thermal runaway. When comparing the drain current, only a slight increase can be observed, which means that the current of 950 A for 3us is close to the thermal limit of the component. An energy of 1.5 J was observed in the last pass.

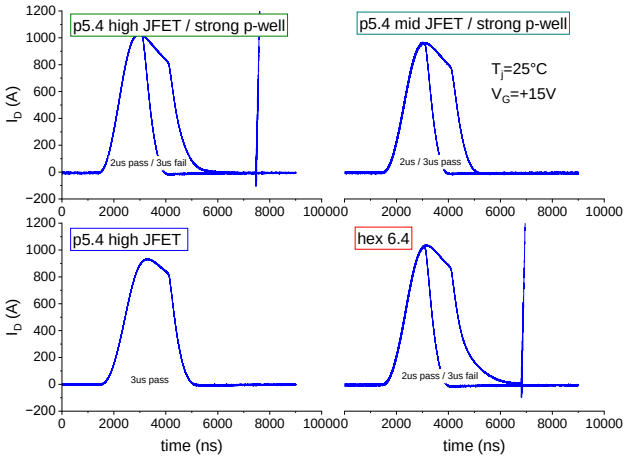

Fig. 10. Short circuit wave forms (type I) of p5.4 and hex selected splits. Pulse test was performed using 2us and 3 us respectively. Remarkably two p5.4 designs can handle up to 3us. The hex and aggressive p5.4 with high JFET still handle 2us in this test.

4 Conclusion

The aggressive scaling of 1.2kV SiC MOSFETs was presented and the design aspects to reduce the parasitic JFET resistance were analyzed. It was shown that with the right design, a very competitive device can be produced even with state-of-the-art processes and conventional designs. A flat temperature behavior with optimized Vth could be achieved. A high SC capability of up to <3us could be demonstrated, so that the expected SC capability of the hex6.4 is <2.8us.

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5 References

[1] K. Han and B. J. Baliga, "Comparison of Four Cell Topologies for 1.2-kV Accumulation- and Inversion-Channel 4H-SiC MOSFETs: Analysis and Experimental Results," in *IEEE Transactions on Electron Devices*, vol. 66, no. 5, pp. 2321-2326, May 2019, doi: 10.1109/TED.2019.2905736

[2] S. Zhu *et al*., "A New Cell Topology for 4H-SiC Planar Power MOSFETs and Comparison with Hexagonal and Octagonal Cell Topologies," *2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, Redondo Beach, CA, USA, 2022, pp. 7-10, doi: 10.1109/WiPDA56483.2022.9955263.

[3] L. Knoll *et al*., "Planar 1.2kV SiC MOSFETs with retrograde channel profile for enhanced ruggedness," *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Shanghai, China, 2019, pp. 211-214, doi: 10.1109/ISPSD.2019.8757648.

[4] D. Kim, N. Yun, A. J. Morgan and W. Sung, "The Effect of Deep JFET and P-Well Implant of 1.2kV 4H-SiC MOSFETs," in *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 989-995, 2022, doi: 10.1109/JEDS.2022.3218689.

[5] K. Tachiki, T. Ono, T. Kobayashi and T. Kimoto, "Short-Channel Effects in SiC MOSFETs Based on Analyses of Saturation Drain Current," in *IEEE Transactions on Electron Devices*, vol. 68, no. 3, pp. 1382-1384, March 2021, doi: 10.1109/TED.2021.3053518.

[6] M. Zhu, L. Wang, H. Li, C. Yang, D. Ma and F. Yang, "Characteristics of SiC MOSFET in a Wide Temperature Range," *2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, Wuhan, China, 2021, pp. 79-82, doi: 10.1109/WiPDAAsia51810.2021.9656056.

