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Adaptive Efficiency Optimization for the High-Step-Up Boost Converter Based on the Loss Analysis Model

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Abstract

In this paper, an adaptive-step-size frequency optimization algorithm (ASSFO) is used for tracking the maximum efficiency point of the high-step-up boost converter under variable conditions. Based on the analysis of losses of the converter, the desired switching frequency is selected depend upon input current value. The ASSFO function results in improved adaptive controller convergence speed, convergences error and stability. This algorithm is implemented in a prototype where converter continuously maintains the optimal switching frequency under varying load current. A 1-kW prototype is implemented to verify the proposed controller performance and proposed algorithm is verified successfully.

1 Introduction

DC-DC converters with high voltage gain are applied widely in the academic and industrial power electronics field [1]-[3], especially in the new energy industry.

Solar energy is popular green energy source, which can be converted into electricity by photovoltaic (PV) systems. In these systems, the output voltage generated by the PV panels is usually at a low level (less than 50V). Therefore, the low level DC voltage from the PV arrays needs to be boosted to meet the input voltage requirement (400V) of the inverter [4]. These converters are two types, isolated and non-isolated converters. In isolated structure, adjustable high gain can be generated by utilizing transformers. However, isolated structures are larger, less efficient and more complex to design as compared to non-isolated topologies.

In non-isolated step-up applications, the classical boost converter with simple structure is normally applied. However, using the boost converter can be disadvantageous due to the low system efficiency in applications requiring high step-up ratio [5]. Tapped inductors provide high step-up ratios without the need for isolation, which represents a simple, effective and promising alternative to achieve wide voltage conversion ratios [6].

There is a requirement of optimum selection of several parameters, in order to achieve an improved efficiency. The design of these parameters for particular components, output and input, load, and operating temperature is might enhance efficiency, however it will not track maximum efficiency for change conditions [7]-[8].

One important parameter in a non-isolated DC-DC converter that needs to be optimized to improve efficiency is the switching frequency of the main switch of the converter. The higher the switching frequency, the smaller the RMS current of each component. The conduction loss is reduced but more switching loss is introduced.

In previous studies [9], fixed step sizes (decreasing and increasing auto-tuning variable values) were used to implement the proposed algorithm. In this case, the designer can choose a smaller step size, which increases the convergence time of the controller, but with higher accuracy to achieve the optimal frequency value, or a larger step size, which shortens the convergence time of the controller. For adaptive frequency control, convergence speed is critical because it needs to keep up with the adjustments that produce new optimal parameters and affect the power conversion output at different times during the converter process. To solve this problem, adaptive efficiency optimization for buck converters is proposed [10]. A new control scheme, based on variable switching frequency and duty cycle, is introduced for the Single Active Bridge converter [11].

In this paper, an adaptive-step-size frequency optimization algorithm (ASSFO) is used for tracking the maximum efficiency point of the tapped-inductor boost converter. The algorithm tracks the operating frequency with minimum power loss and maximum efficiency by tracking the minimum value of the input current. The ASSFO function results in improved adaptive controller convergence speed, convergences error and stability. This algorithm is implemented in a prototype where converter continuously maintains the optimal switching frequency under varying load.

2 High-Step-Up Boost Converter

2.1 Topology of the Converter

The tapped-inductor boost converter is shown in Fig.1. The circuit components include MOSFET SW_1, power

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diode D_1, tapped-coupled inductors L_1 and L_2, output filter capacitor C, and load resistance R. Compared with the traditional boost converter circuit uses a tapped coupled inductor instead of a tapless inductor. The switch is connected to the tapping point of the inductor rather than to one of the extremities of the inductor, which makes the turns of the inductor in the magnetizing circuit and the demagnetizing circuit is different, so that the inductance is different.

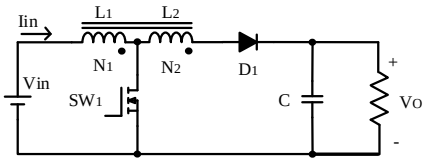


Fig. 1. Tapped-Inductor Boost Converter [12].

2.2 Operation of the Converter

When the switch SW_1 is on (Fig.2.a): the diode D_1 is not conducting, due to the polarity of the magnetic element, the tapped inductor L_1(corresponding to the coil N_1) is charged through the loop formed by SW_1 and V_{in}, the current of L_1 rises, and the inductor L_2 has no current. The output filter capacitor C supplies power to the load.

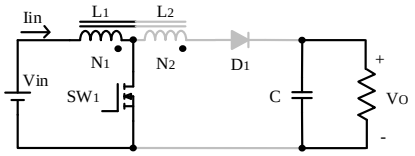
When the switch SW_1 is off (Fig.2.b): the diode D_1 is conducting, and the magnetic element is being discharged through the loop formed by the equivalent inductance of L_1 and L_2, the diode D_1, the output load and Vin. The current of L drops, and the currents of L_1 and L_2 are equal. The input source V_{in} and the tapped inductance jointly supply power to the load.

The two subcircuits of the converter are determined by the main switch, these subcircuits are shown in Fig.2. The high boosting capability is because the discharging process of the magnetic element.

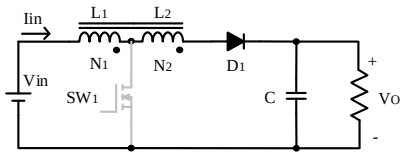
The voltage gain can be obtained as:

$$\frac{V_o}{V_{in}} = \frac{1+nkD}{1-D} \tag{1}$$

Fig.3 illustrates the curves of the voltage gain as a function of the duty cycle D when the turns ratio n is different. When n=0, the tapped-coupled boost converter is reduced to a conventional boost converter, which has a voltage gain of $V_o/V_{in}=1/(1-D)$. Obviously, the tapped-inductor boost converter can obtain high step-up ratios with low duty ratio. Such as, voltage gain of 10 is achieved by the tapped-inductor boost converter with a duty ratio of 0.45 and turns of 10, but with a duty ratio of 0.9 by the conventional boost converter.



a. SW_1 on.



b. SW_1 off.

Fig. 2. Subcircuits of Tapped-Inductor Boost Converter.

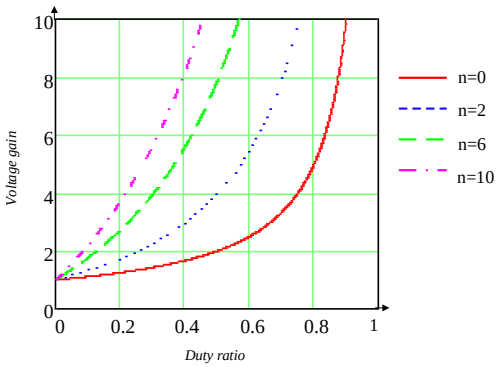


Fig. 3. Voltage gain versus duty ratio D.

2.3 Frequency Effect on Losses

The expression for RMS current of L_1, C, SW_1 and D_1 can obtained as:

$$I_{L1rms} = I_{inrms} = \sqrt{\left\{\left(\left(\frac{1+nk}{1-D}\right)I_{o,ave}\right)^2 D\times\left[1+\frac{1}{3}\left(\frac{\Delta i'_{L_1,pk-pk}}{2\left(\frac{1+nk}{1-D}\right)I_{o,ave}}\right)^2\right] + \left(\frac{I_{o,ave}}{(1-D)}\right)^2(1-D)\times\left[1+\frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{I_{o,ave}}{(1-D)}\right)}\right)^2\right]\right\}} \tag{2}$$

$$I_{crms} = \sqrt{\left\{\left(I_{o,ave}\right)^2 D + \left(\frac{DI_{o,ave}}{(1-D)}\right)^2(1-D)\times\left[1+\frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{DI_{o,ave}}{(1-D)}\right)}\right)^2\right]\right\}} \tag{3}$$

$$I_{srms} = \sqrt{\left\{\left(\left(\frac{1+nk}{1-D}\right)I_{o,ave}\right)^2 D\times\left[1+\frac{1}{3}\left(\frac{\Delta i_{L1,pk-pk}}{2\left(\frac{1+nk}{1-D}\right)I_{o,ave}}\right)^2\right]\right\}} \tag{4}$$

$$I_{Drms} = I_{L2rms} = \sqrt{\left\{\left(\frac{I_{o,ave}}{(1-D)}\right)^2(1-D)\times\left[1+\frac{1}{3}\left(\frac{\Delta i_{L2,pk-pk}}{2\left(\frac{I_{o,ave}}{(1-D)}\right)}\right)^2\right]\right\}} \tag{5}$$

The tapped-inductor boost converter total power loss is the sum of three types of power losses as follow.

1) Conduction power losses.

$$\begin{aligned} P_{\text{loss\_conduction}} &= P_{\text{loss\_mos}} + P_{\text{loss\_Diode}} + P_{\text{loss\_cu}} \\ &= I_{srms}^2 \cdot R_{DS\_MOS} + I_{Drms} \cdot V_{\text{fwd}} + I_{L1rms}^2 \cdot R_{L1} + I_{L2rms}^2 \cdot R_{L2} \end{aligned} \tag{6}$$

where R_{DS_MOS} is the turn-on resistance of MOSFET that can be obtained from the datasheet diagram, R_{L1} is the resistance of the primary winding and R_{L2} is the

resistance of secondary winding of the inductor. V_{fwd} is the forward voltage drop of the diode.

They are a function of RMS currents in different components and traces. According to the analysis of the RMS values of the currents of the coupled inductance, the active switch and the diode, these values are related to the switching frequency f_{sw}.

Fig.4 shows the switching frequency effect on the total conduction losses at output current I_o=2.5A based on (6).

2) Switching power losses.

$$\begin{aligned} P_{\text{loss\_switch}} &= P_{\text{mos\_on}} + P_{\text{mos\_off}} + P_{\text{Diode-on}} + P_{\text{Diode-off}} \\ &= f_{sw} \times \int V_{DS\_on}(t) \cdot I_{DS\_on}(t)dt + f_{sw} \times \int V_{DS\_off}(t) \cdot I_{DS\_off}(t)dt \\ &+ \frac{1}{2} \cdot V_{fp} \cdot I_{fp} \cdot t_{fr} \cdot f_{sw} + \frac{1}{2} \cdot V_{rp} \cdot I_{rp} \cdot t_f \cdot f_{sw} \end{aligned} \quad (7)$$

where V_{fr} is the forward recovery voltage, and t_{fr} is the turn-on recovery time. And V_{rp} is the reverse voltage of the diode, t_f is the reverse recovery time.

Switching losses are related to the parasitic parameters of the switching device. Fig.5 shows the switching losses, which is a function of the switching frequency.

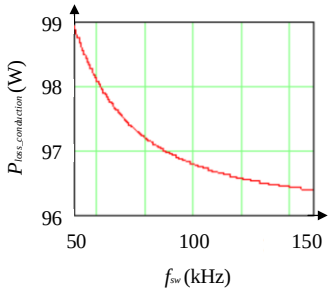


Fig.4. Conduction losses versus switching frequency.

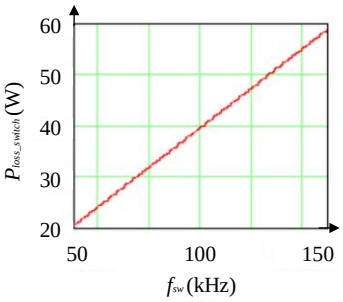


Fig.5. Switching losses versus switching frequency.

3) Gate-drive power loss.

$$P_{gs} = V_{gs} \cdot Q_g \cdot f_{sw} \quad (8)$$

where Q_g is the gate charge value, V_{gs} is the gate-drive voltage.

These losses are the energy required to drive the gate of the MOSFET.

4) Transformer core loss.

The core losses of magnetic can be calculated using the Steinmetz equation.

$$P_c = k f_s^{\alpha} B^{\beta} V_e \quad (9)$$

where k, α, β are constant which are related to the material, and Ve represents the core volume.

The maximum magnetic flux density of the transformer can be calculated as:

$$B_{Tr} = \frac{V_{L1rms}}{4 f_s A_{e-Tr} N} \quad (10)$$

where $A_{e\text{-}Tr}$ is the effective cross-sectional area of the transformer and N is the number of turns of the excitation coil.

Based on (9) and (10), higher switching frequency results in lower flux density. The influence of flux density is greater than that of switching frequency for core loss. So, P_c decrease while switching frequency increases respectively.

$$P_{total} = P_{\text{loss\_conduction}} + P_{\text{loss\_switch}} + P_{gs} + P_c \quad (11)$$

The higher the switching frequency, the smaller the RMS current of each component. The conduction loss is reduced but at the same time, more switching loss is introduced. Fig.6 shows all the key components power losses of the converter at output current I_o=2.5A.

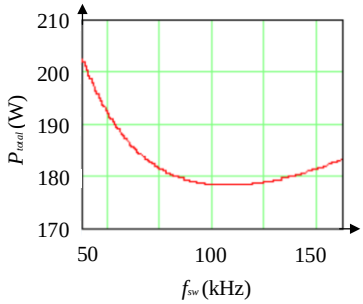


Fig. 6. Total losses as a function of switching frequency.

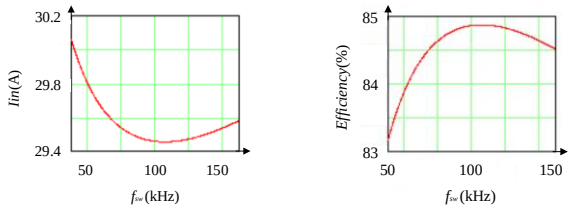
The efficiency of the tapped-inductor boost converter can be stated as:

$$\eta = \frac{V_o I_o}{V_o I_o + P_{total}} = \frac{V_o I_o}{V_{in} I_{in}} \quad (12)$$

Thus, there is an optimum switching frequency value which will result in a minimum total power loss as one of the losses increases and the other decreases when the switching frequency is varied. Lower total power loss results in lower input power and therefore lower input current which leads to higher power conversion efficiency. This behavior results in the curves shown in Fig.7, that is, the input current and input power as a function of the switching frequency have a curve with minimum.

Since the change in the input current is higher for the same change in frequency, the gradient is higher. The high gain characteristics of the boost topology make its losses sensitive to the switching frequency, reacting to

the input power and to the input current with a constant input voltage and a constant output power.

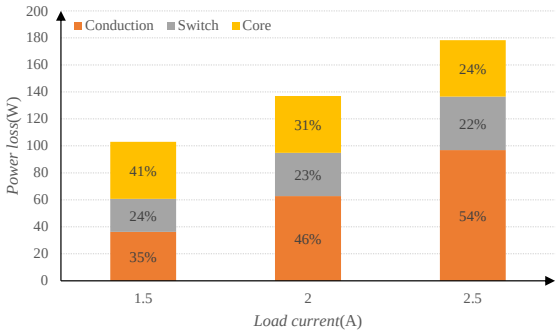


a. input current **b.** efficiency

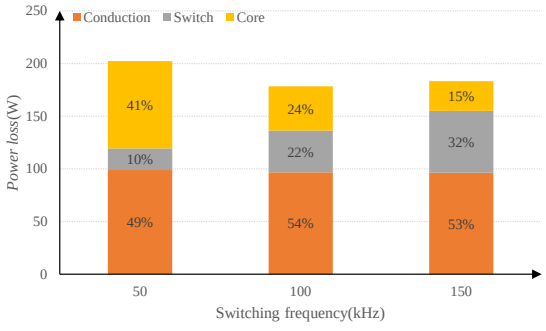
Fig. 7. Input current and efficiency curves as a function of the switching frequency.

The power losses and distribution of the tapped-inductor boost converter at different loads are shown in Fig.8.a It shows that the losses of magnetic core make up 41% of total losses at output current Io=1.5A, and conduction losses are dominated at full load. Fig.8.b shows the distribution at different switching frequencies, and it illustrates that magnetic core loss decreases with increasing switching frequency, while the switching loss behaves in the opposite way.

According to the above analysis, the power losses of the converter is related to both the load and the switching frequency. The losses are minimized by a trade-off between conduction losses, switching losses and core losses.



a. at different loads at 100kHz



b. at different switching frequency at I_o=2.5A

Fig. 8. Power losses distribution

Based on (12), Fig.9 shows 3-D surface plots of efficiency versus frequency versus load current. And the optimum frequencies to maximize the efficiency of the converter at different loads is marked with black dots. It is noted that different loads correspond to different optimal switching frequencies, so an adaptive optimization algorithm needs to be designed to track the frequency that maximizes efficiency.

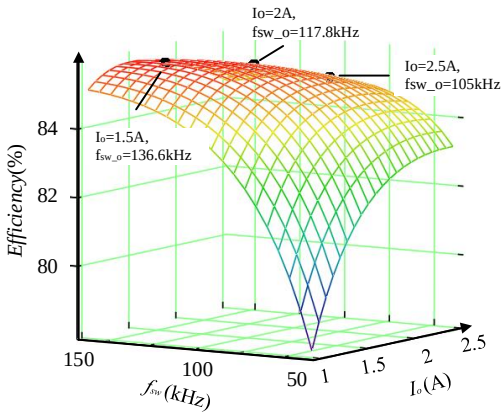


Fig. 9. Converter efficiency as a function of switching frequency and load current.

3 Adaptive-Step-Size Frequency Optimization Algorithm

This method tracks efficiency of power circuits, and adaptively optimizes control system parameters to maximize efficiency. An adaptive frequency optimization controller is a controller that can modify its behavior after changes in the controlled plant.

3.1 Control System

Fig.10 shows a tapped-inductor boost converter and the control system, which will be taken as an example with ASSFO to be applied to it to optimize its frequency, the voltage loop collects the output voltage to compensate the output voltage when the switching frequency is changed to keep the output voltage constant.

Calculating the efficiency of a converter requires sampling the input current, input voltage, output current, and output voltage and then multiplying them three times. Due to the inductive and proportional amplification of the sampling circuits, this process not only requires a certain amount of controller resources, but also has a large number of possible computational errors.

Combining this with the analysis of Section 2, when the input voltage is constant and the output power is also constant, the magnitude of the input current characterizes the magnitude of the input power which means that the maximum efficiency occurs at the minimum point of the input current.

And, collecting the input current, which can be used as a characterization of the input power when the input voltage is constant, and the input power is minimized

when the converter loss is minimized, that is, when the input current is minimized.

3.2 Performance of the Algorithm

The steps of the proposed algorithm are shown in Fig.11.

(1) The input current at fixed input voltages is captured by the ADC and averaged to obtain $I_{in}(n)$;

(2) The ASSFO algorithm calculates the difference between the current and previous values of the input current frequencies;

(3) A check will be performed to see if ΔI_{in} has sufficient value to update f_{sw} or not. This difference is compared with the selected I_e;

   a) if the condition is satisfied to update f_{sw} and the program proceeds to the next step;

   b) Otherwise, keep the current stable working state, and wait for the next command;

(4) The gradient value of the input current is obtained using the two differences obtained in (3);

(5) Calculate the step size based on the gradient value of the input current;

(6) As the curves shown in Fig.7,

   a) If the signs of the values obtained from the above two equations are similar, it means that f_{sw} should decrease f_{sw_step} to move toward the maximum efficiency point;

   b) Otherwise, f_{sw} should increase f_{sw_step};

(7) After M switching cycles (needed to allow the circuit to reach steady state under the control of a voltage closed-loop controller), sample again and repeat the ASSFO process;

Until the accuracy requirements are met, end the cycle.

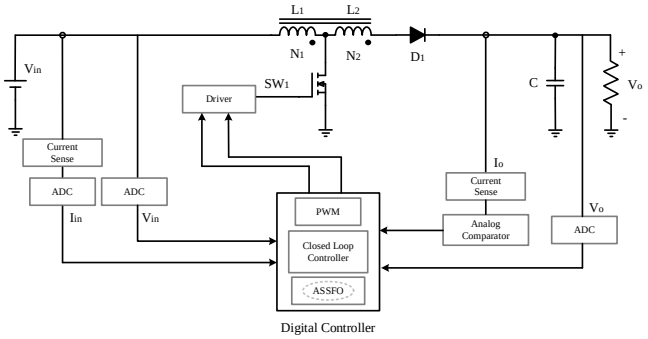


Fig. 10. The tapped-inductor boost converter with control system.

4 Experimental Work

A prototype of the tapped-inductor boost converter was chosen as a power stage in this experimental work to implement ASSFO in order to select the operating frequency that maximizes its efficiency.

The tapped-inductor boost converter was with 400V/2.5A output, 40V input voltage, output current ripple of 25% and the output power regulation was achieved using a conventional closed-loop compensator. Switching frequency varies from 50k Hz to 150k Hz.

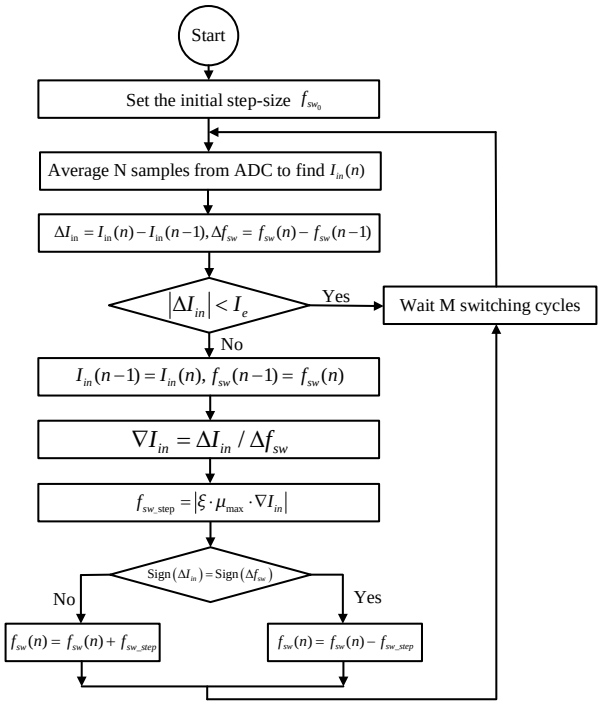


Fig. 11. ASSFO controller flowchart [10].

4.1 Active Switch Selection

Based on the analysis of the operation of the circuit in Section 2.2, the MOSFET is selected by considering the blocking voltage V_{ds} when SW_1 is not conducting and the peak switching current $i_{s,pk}$ when SW_1 is conducting.

When SW_1 is not conducting,

$$V_{ds} = V_{in} - V_{L1} \tag{13}$$

According to the coupling coefficient k and turns ratio n of the coupled inductor,

$$V_{ds} = V_{in} - \frac{\left\{V_{in} - V_o - i_L\left(r_{L_1} + r_{L_2}\right)\right\}(1+nk)}{1+2nk+n^2} \tag{14}$$

The voltage blocked by the switch when it is not conducting, is,

$$V_{ds} = \frac{V_{in}\left(nk+n^2\right)+\left(V_o + i_L\left(r_{L_1}+r_{L_2}\right)\right)(1+nk)}{1+2nk+n^2} = 70.12\text{V} \tag{15}$$

$$i_L = i_{in} \tag{16}$$

When SW_1 is conducting , the peak current of the MOSFET is,

$$i_{s,pk}=\left(\frac{1+nk}{1-D}\right)I_{o,ave}+\frac{1}{2}\left(\frac{\left(v_{in}-i_{L1}r_{L_1}\right)DT_{sw}}{L_1}\right)=52.57\text{A} \quad (17)$$

As Fig.2.a, the blocking voltage of output diode V_D is determined by considering the voltage across the diode when the active switch is on,

$$V_D=\left(i_{ds}r_{ds(on)}+nk\left(V_{in}-i_{L1}r_{ds,on}-i_{L1}r_{L1}\right)+V_{\text{out}}\right)=777.86\text{V} \quad (18)$$

Based on (4) and Fig.2.b, the peak current of diode D_1 is determined when the active switch is off,

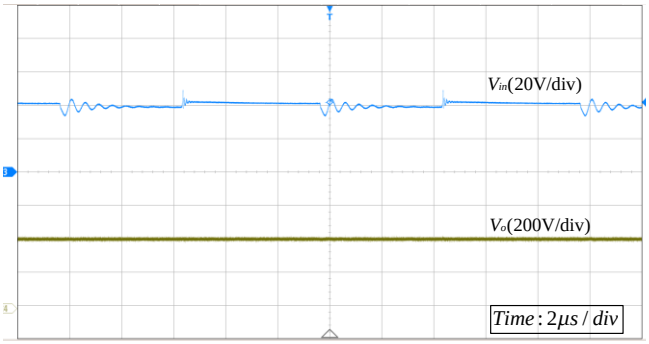
$$i_{D,pk}=\frac{I_{o,ave}}{(1-D)}+\frac{1}{2}\left(\frac{n\left(V_{in}-V_o-i_L\left(r_{L_1}+r_{L_2}\right)\right)(1-D)T_{sw}}{(n+1)L_2}\right)=4.56\text{A} \quad (19)$$

Table 1. Specifications of the Converter

Item	Symbol	Value
Input Voltage	V_{in}	40V
Output Voltage	V_o	400V
Output Current	I_o	2.5A
Turns Ratio	n	10
Magnetic Inductor	L_1	30μH
Coupling Coefficient	k	0.98
MOSFET	SW_1	IRFB4115PBF
Rectifier Diode	D_1	STTH810FP
Output Capacitor	C	200μF

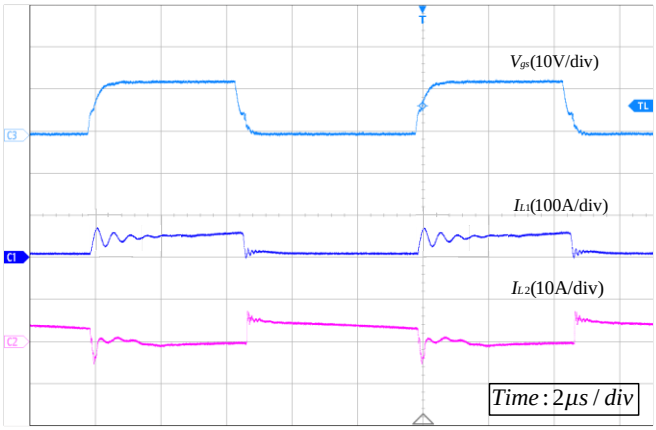
4.2 Experimental Results

At a frequency of 100k Hz, the experimental key waveforms of the tapped-inductor boost converter when the output voltage is 40V and the output is 400V is shown in Fig.12. Fig.12.a shows that the voltage gain of the topology achieves 10 when the duty cycle D is 0.5. And Fig.12.b verifies the operation of the converter in Section 2.2.



a. Voltage waveforms.

This experimental result shown in Fig.13 proved the theoretical analysis of Section2.2. Lower total power loss (higher efficiency) results in lower input power and therefore lower input current which leads to higher power conversion efficiency.



b. Current waveforms.

Fig.12 The experimental key waveforms of the tapped-inductor boost converter.

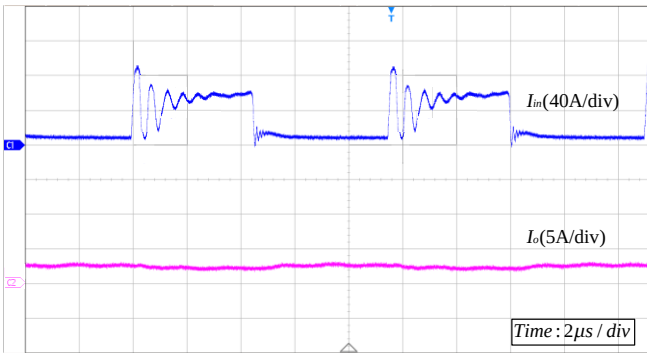


Fig. 13 Waveforms of input and output currents at a frequency of 105k Hz

In this paper, the Gradient Descent Method is used for optimization, which starts with a step size f_{sw_0} of 1 kHz.

$$\begin{aligned}\nabla I_{\text{in}}(n)&=\frac{I_{\text{in}}\left(f_{\text{sw-start-max}}\right)-I_{\text{in}}\left(f_{\text{sw}-o}\right)}{f_{\text{sw-start-max}}-f_{\text{sw-o}}}\\&=\frac{29.581-29.455}{150000-105000}\\&=2.8\times10^{-6}\end{aligned} \quad (20)$$

This $\nabla I_{\text{in}}(n)$ value represents a line slope approximation of curve which is connected between the approximated optimum switching frequencies and the farthest switching frequency that the controller is allowed to operate.

According,

$$\frac{dI_{\text{in}}}{df_{\text{sw}}}=2\lambda\cdot\left(f_{\text{sw}}-f_{\text{SW}-O}\right) \quad (21)$$

$$f_{\text{sw}_{(k+1)}}=f_{\text{sw}_{(k)}}+\mu\cdot\left(-\nabla_{(k)}\right) \quad (22)$$

Then,

$$f_{(n)}=f_{\text{sw}-o}+(1-2\mu\lambda)^k\cdot\left(f_{\text{sw}_{(0)}}-f_{\text{sw}-o}\right). \quad (23)$$

the iterative process will be stable if the following condition is satisfied,

$$|r| = |1 - 2\mu\lambda| < 1. \quad (24)$$

This condition can be also expressed as,

$$0 < \mu < \frac{1}{\lambda} \quad (25)$$

In this prototype experiment,

$$2.8\times10^{-6} = 2\lambda\cdot(150000-105000) \Rightarrow \lambda = 3.11\times10^{-11} \quad (26)$$

$$0 < \mu < \frac{1}{\lambda} \Rightarrow \mu < 3.21\times10^{10} \quad (27)$$

This value represents the maximum value for above which, the adaptive loop may not converge.

For this experimental work, select $\mu = 3\times10^{10}$, $\xi = 0.04$, which starts with a step size f_{sw_0} of 1 kHz.

Then the gradient $\nabla I_{\text{in}}(n)$ can be approximated as,

$$\nabla I_{\text{in}}(n) = \frac{I_{\text{in}}(n) - I_{\text{in}}(n-1)}{f_n - f_{n-1}} = \frac{29.581 - 29.576}{150000 - 149000} = 5\times10^{-6} \quad (28)$$

$$f_{\text{sw\_step}} = \left|\xi\cdot\mu_{\max}\cdot\nabla I_{\text{in}}\right| = \left|0.04\times3\times10^{10}\times5\times10^{-6}\right| = 6000Hz \quad (29)$$

The next iteration new approximated switching frequency value is $149000 - 6000 = 143000\text{Hz}$. By repeating the same process, the next step-sizes and gradient values can be estimated and used as design guidance for the experimental adaptive loop design.

Fig.14 shows the optimum switching frequency under different loads, it shows more clearly that, the optimum switching frequency follows the change of circuit operating state. As shown in Fig.15, for this prototype, an efficiency gain of up 5% is observed at I_o=0.5A, which is due to the optimum frequency to maximize converter efficiency at light loads is far from the fixed frequency. It should be noted that the potential efficiency gain may vary when load and components changing.

Table 2 demonstrates the data from the experimental results comparing the fixed step size algorithm with the adaptive step size algorithm proposed in this paper and the effect of different zeta values on convergence speed and accuracy.

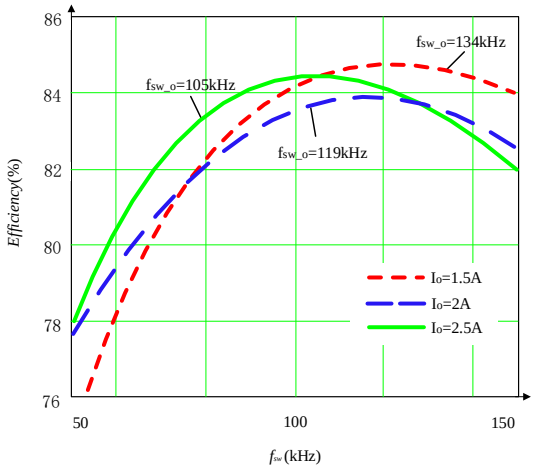


Fig. 14. Optimal switching frequency for different loads

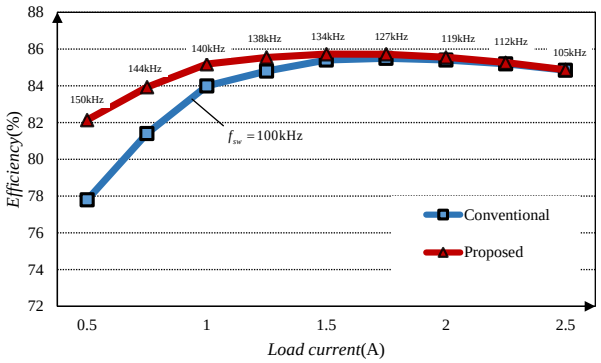


Fig. 15. Efficiency curves of conventional fixed-frequency and the proposed control method.

Table 2. Summary And Comparison of The Experimental Results

Load/ Optimum Frequency	Criteria	Fixed-Step-Size			Adaptive-Step-Size	
		10 kHz	5 kHz	1 kHz	ξ=0.08	ξ=0.04
2.5A/105kHz	Iterations	5	10	46	8	16
	~% Error in f_{sw-o}	4.76 (110kHz)	0 (105kHz)	0 (105kHz)	1.71 (106.8kHz)	1.24 (106.3kHz)
2A/116kHz	Iterations	4	8	35	8	17
	~% Error in f_{sw-o}	3.45 (120kHz)	0.86 (115kHz)	0 (116kHz)	1.38 (117.6kHz)	0.43 (116.5kHz)
1.5A/134kHz	Iterations	3	4	17	5	11
	~% Error in f_{sw-o}	2.99 (130kHz)	0.75 (135kHz)	0 (134kHz)	1.04 (135.4kHz)	0.07 (134.1kHz)

5 Conclusion

This paper presents an adaptive-step-size frequency optimization algorithm for high-step-up boost converter. Based on the analysis of losses of the tapped inductor boost converter, the power losses of the converter are related to both the load and the switching frequency. The losses are minimized by a trade-off between conduction losses, switching losses and core losses.

The algorithm tracks the operating frequency with minimum power loss and maximum efficiency by tracking the minimum value of the input current.

The ASSFO algorithm is discussed, the theoretical analysis and design equations of ASSFO are established, and the experimental results verify the operation and analysis of the proposed algorithm.

The algorithm works well with different input power supplies and output loads when the parameters are properly selected.

6 References

[1] C. Lee and Q. Zhao, “High-Efficiency, high step-up DC-DC converters,” IEEE Trans. Power Electron., Vol. 18, No.1, pp.65-73, Jan. 2003.

[2] A. Emadi and S. S. Williamson. “Fuel cell vehicles: opportunities and challenges,” IEEE Power Engineering Society General Meeting., Vol. 2, pp.1640-1645, Jun. 2004.

[3] K. C. Tseng and T. J. Liang, “Novel high-efficiency step-up converter,” IEE Proc.-Electr. Power Appl., Vol. 151, No. 2, pp.182-190, Mar. 2004.

[4] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti and F. Blaabjerg, "High-Efficiency High Step-Up DC–DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," in IEEE Transactions on Power Electronics, vol. 33, no. 7, pp. 5967-5982, July 2018.

[5] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, “Step-up switching-mode converter with high voltage gain using a switched- capacitor circuit,” IEEE Trans. Syst. I, Fundam. Theory Appl., vol. 50, no. 8, pp. 1098–1102, Aug. 2003.

[6] Michael, Njoroge, Gitau, et al. “Analysis and Design of a Single-Phase Tapped-Coupled-Inductor Boost DC–DC Converter,” Journal of Power Electronics, 2013.

[7] J. Abu-Qahouq, H. Mao, H. Al-Atrash, and I. Batarseh, “Maximum efficiency point tracking (MEPT) method and dead-time control,” IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1273-1281, Sep. 2006.

[8] W. Al-Hoor, J. Abu-Qahouq, L. Huang, and I. Batarseh, “Adaptive variable switching frequency digital controller algorithm to optimize efficiency,” in Proc. IEEE Int. Symp. Circuits Syst., 2007, pp. 781-784.

[9] J. Klien, “Synchronous buck MOSFET loss calculations with Excel model,” Fairchild Semiconductor Application Notes AN-6005, 2006.

[10] Al-Hoor, Wisam, "Adaptive Efficiency Optimization For Digitally Controlled Dc-dc Converters" (2009). Electronic Theses and Dissertations. 4006.

[11] A. A. Gómez, A. Rodríguez, M. M. Hernando, A. Vázquez, J. Giles and J. Sebastián, "Variable switching frequency and duty cycle control strategy for the Single Active Bridge," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-8.

[12] N. Vasquez, L. Estrada, C. Hernandez, and E. Rodriguez, “The tapped inductor boost converter,” in Proc. IEEE Conf. Ind. Electron., (ISIE'07) ,Vigo, Spain, June, 2007, pp. 538 - 543.