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Design and Implementation of 3.3kV Hybrid SiC Three-level AC/DC Converter

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Abstract

Due to the requirements of high efficiency, high power density and lower cost for railway traction converter, the multilevel converter technology has received increasing attention in recent years. Considering reliability of railway traction system,current research mainly focuses on three-level converter technology. For three-level converters, employing hybrid silicon carbide (SiC) solutions allows for achieving performance characteristics nearly equivalent full SiC solutions and significantly reduce costs. In this paper, the design guideline and experiment test of 3.3kV hybrid SiC three level AC/DC converter are given.

1 Introduction

With the advancement of silicon carbide power semiconductor technology, hybrid silicon carbide (SiC) solutions have emerged as an ideal choice for high-voltage three level Active Neutral Point (ANPC) converter due to its superior attributes such as high breakdown voltage, low on-state resistance,and fast switching ability[1]-[3]. Howerver, for these solutions in 3.3kV power electronic systems, low stray inductance design is a significant challenge of performance and reliability[4]-[5]. Thus, the strategies to suppress stray inductance and designs of low-inductance busbars play important roles in hybrid SiC application and significantly enhancing the efficiency and reliability of converters.

To meet the demands of high power applications, it is common practice to employ power semiconductor devices in parallel configuration. The current distribution of SiC MOSFETs in parallel application should be considered to avoid excessive junction temperature differences. To illustrate the solutions of these problems, a design example and experiment test of three-level converts are shown as follow.

2 Principle and design example

As shown in fig1, there is an example of hybrid SiC three-level converter used in the context of the railway traction application. In such railway traction converters, the power rate of four-quadrant converter usually in falls between around 1800kW to 2000kW. Thus, the outer switches and clamping switches of this practical hybrid SiC three-level converter employ 3300V/2400A IGBT. On the other hand,the inner switches are configured as three paralleled 3300V/750A SiC MOSFETs.

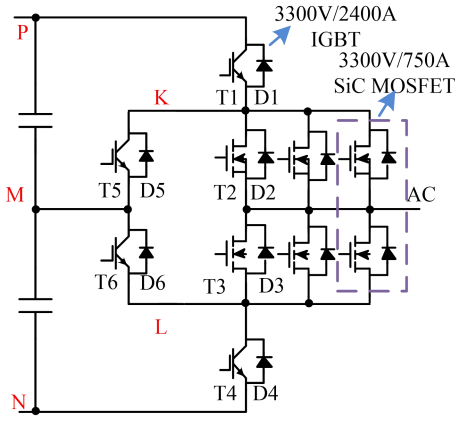

Fig. 1. Diagram of hybrid-SiC three-level converter

2.1 Main circuit layout design

During high frequency switching operations of SiC devices, stray inductance will translate into transient voltages and generate voltage spikes that threaten the reliability and efficiency of SiC devices. The Implementation of Low-Inductance device layouts and busbar design are shown as follow. In this solution, since the commutation loop is mainly consist of T1-T2-T3-T6 switches. During the device layouts design, special emphasis is given to the arrangement of this commutation loop. Moreover, in order to ensure uniform current distribution among the connecting terminals of the IGBT modules, it is necessary to keep the relative distance difference between the IGBT

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module connecting terminals and current paths within the converter as well as possible.

Because of the parallel applications of hybrid SiC devices, busbar design uniformity directly affects the current distribution among the switches. An optimally designed low-inductance busbar should be complemented by advanced current sharing control schemes, ensuring all paralleled switches share currents evenly under any operating condition. Following the above principles, the device layouts and busbar design are shown in fig2.

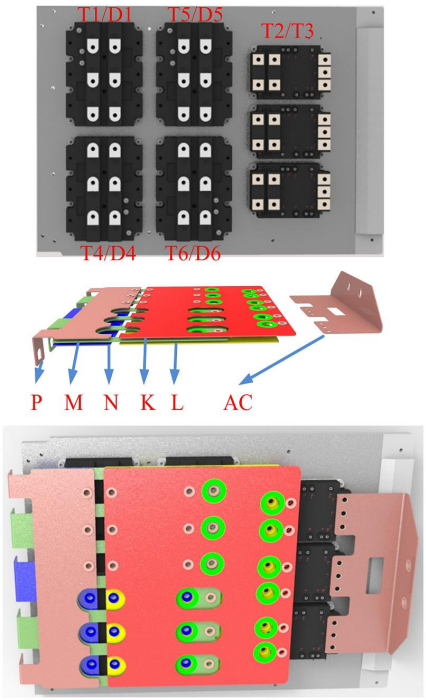

Fig. 2. Device layouts and busbar of hybrid-SiC three-level converter

In Figure 2, the layout has been arranged to optimize in the commutation paths of both the upper and lower bridge arms. On the one hand, the outer switch is placed on the left, and the inner switch is placed on the right, with the clamp switch settled in between them.On the other hand, to balance the current flow across all terminals of the IGBT module, a special consideration has been given to their placement. Each IGBT is situated in proximity current paths, ensuring an equitable distribution of current and enhancing device performance and reliability.

2.2 Commutation loop analysis

After completing the layout of power semiconductor modules and the design of stacked busbars, it is essential to analysis the commutation loops with consideration for the operation principles and modulation strategies of the hybrid SiC three-level topology. In Figure3, the operation principle of the hybrid SiC three-level topology is given. The inner switches T2/T3 switch at high frequency by using SiC modules. The outer and clamping switches T1/T4 T5/T6 switch at line frequency. Under these conditions, particular attention should be paid to switching process of the inner switches. Furthermore, because of the presented design employing three SiC MOSFETs in parallel, the current sharing characteristics among these SiC MOSFETs should be considered.

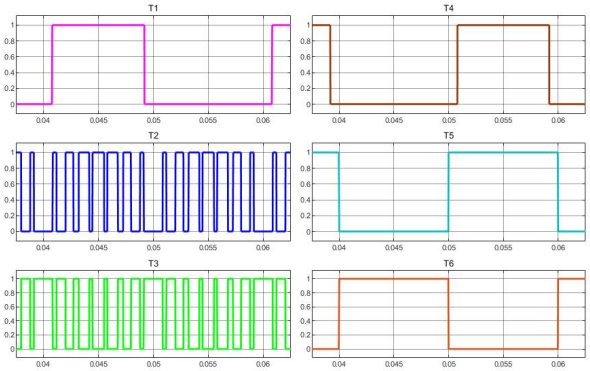

Fig. 3. Modulation strategies of the hybrid SiC three-level topology

As shown in fig4, the commutation loop of switch T2 is given. Firstly, switch T1 and T6 remain in the on state and switch T4 and T5 remain in the off state during the switching process of switch T2. Then, when the switch T2 is turned on, current flows through the positive terminal of busbar, switches T1,T2 and the neutral point of busbar. Finally, when the switch T2 is turned off, current flows through the AC terminal of busbar and switches T3,T6. Therefore, the commutation loop of switch T2 comprises the positive busbar, the upper capacitor, the neutral point busbar and switches T1,T2,T3 and T6, as shown on the right side of figure4.

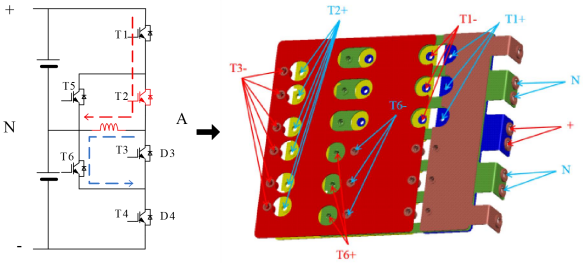

Fig. 4. Commutation loop of T2

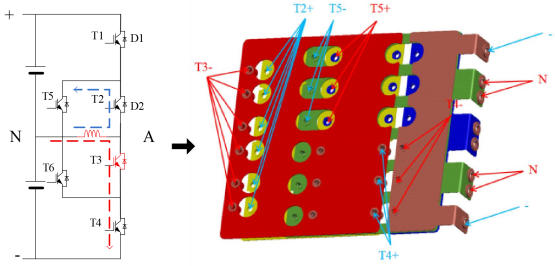

Fig. 5. Commutation loop of T2

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The commutation loop for switch T3 is similar to that of switch T2, comprising the neutral point busbar, the lower capacitor, negative busbar and switches T2,T3,T4 and T5, as shown on the right side of figure5.

3 Experiment

In order to verify the impact of device layouts and busbar design on the stray inductance and the current distribution among switches, the double pulse test has been conducted. In presented topology, there is primary focus on the switching dynamics of the inner switches. Therefore, the test results of inner switches are shown as follow.

As shown in figure6, The stray inductance of the inner switches can be calculated by the waveform of switches turning off process, the calculation results of T2 and T3 are 267nH and 243nH,respectively. These results include inductance of DC link capacitor, stacked busbar, and switches in the commutation loops.

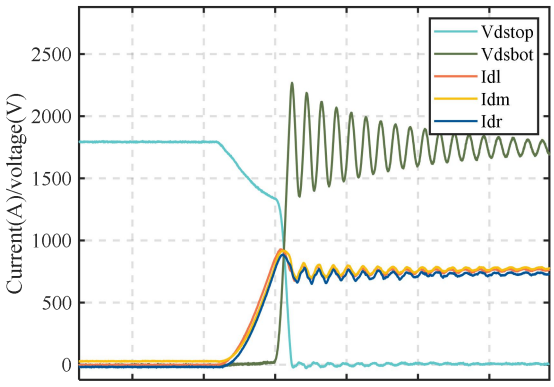

Fig. 6 Waveform of inner switches turning off process

The double pulse test waveforms of T2 and T3 are shown in figure7 and figure8. The maximum drain source voltage for T2 and T3 are respectively 2222V and 2157V. The test results shows that the turn-on energy is close to the value in the data sheet. But in order to reduce the voltage during turn-off process, the turn-off energy has reached approximately three times the values in the data sheet.

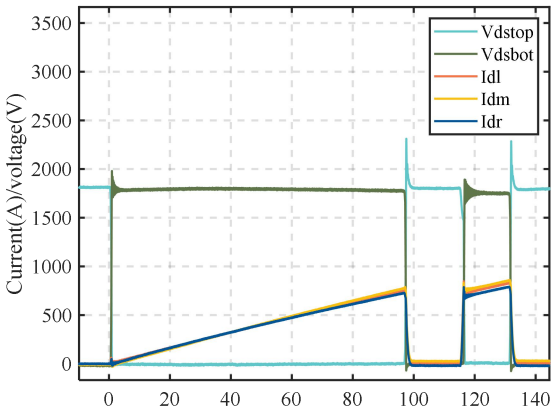

Fig. 7 Waveform of T2 switching process

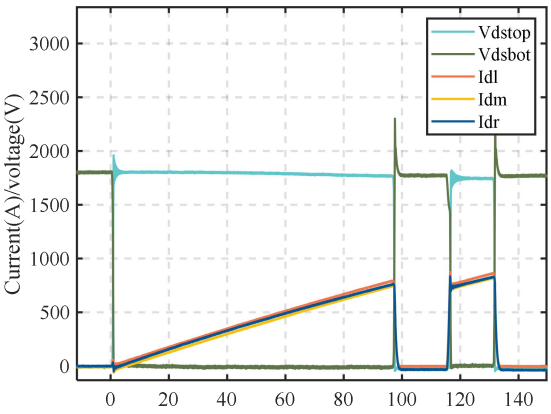

Fig. 8 Waveform of T3 switching process

The Figure9 presents the detailed waveform of the current sharing test for three parallel SiC MOSFETs. The static current sharing degree can reach 97%, while dynamic current sharing degree can reach 94%.

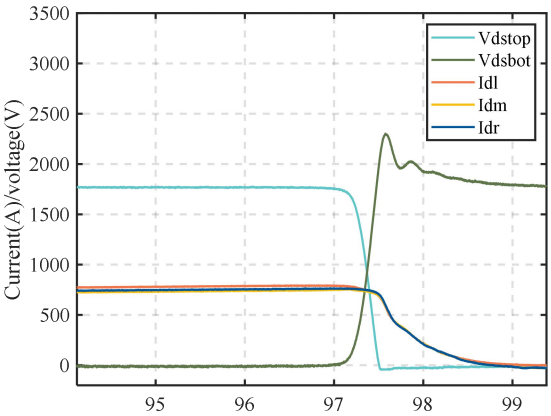

Fig. 9 Waveform of current distribution of three SiC modules

The results of the double pulse test are presented, the experiment results indicate that under the current design scheme, the current-sharing degree among SiC MOSFETs can reach 94%. However, due to the large commutation loop, to suppress voltage spikes during turn-off, it has resulted in higher turn-off losses for the SiC MOSFETs.

4 Conclusion

The design and implementation of 3.3kV hybrid SiC application in three-level ANPC converters are the fundamental for realizing compact and lightweight high-power, high-voltage converters. In this paper, a practical design of hybrid SiC three level converter is given. And the experiment results verify the design principles well. As SiC technology continues to mature, the attentions will increasingly be on the fine-grained control of stray inductance and paralleled application

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of switches to meet higher voltage levels and larger-scale power demands in the future.

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