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Optimized Driving Conditions for Enhanced Switching Performance with SiC-MOSFETs

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Abstract

Silicon carbide (SiC) based power converters are becoming increasingly popular in power electronics due to their high efficiency and power density, which are critical factors for environmental and energy cost considerations. SiC devices possess higher dielectric breakdown strength, energy bandgap, and thermal conductivity than silicon, allowing for the creation of more efficient and compact power converters [1].

Key parameters such as low $R_{DS(on)}$ and body diode reverse recovery charge play pivotal roles in minimizing losses during operation. These characteristics significantly contribute to the reduction of conduction and switching losses, thereby enhancing overall efficiency. Additionally, SiC devices enable faster switching speeds and higher operating frequencies, resulting in space-saving designs, reduced heat dissipation, and lighter power converters. This paper presents an in-depth investigation into the effects of various drive conditions on the losses and performance characteristics of onsemi 1200 V SiC MOSFET technology (M3S).

By examining parameters such as gate drive voltage, switching frequency, and temperature, this study provides valuable insights for optimizing the switching performance and efficiency of SiC-based power converters. The findings demonstrate how careful adjustment of drive conditions can minimize energy losses, improve thermal management, and extend the operational lifetime of power electronic systems. Consequently, this research contributes to the advancement of SiC technology in modern power electronics applications, highlighting its potential to meet the growing demands for sustainable and efficient power conversion solutions.

1 Introduction

1.1 M3S Technology

EliteSiC MOSFET technology has progressed through three generations at onsemi (Figure 1). The onsemi Elite SiC MOSFET technology has evolved over three generations: M1, M2, and M3. M1 introduced the company to SiC MOSFETs with a classic planar DMOS structure. M2 saw significant improvements with a shift to an elongated hexagon layout and a 70% reduction in substrate thickness, resulting in a 20% decrease in specific on-resistance (RSP).

M3 introduced a stripe design, further reducing unit cell pitch and achieving an additional 30% reduction in RSP compared to M2[2].

This technology is divided into two products: M3T for motor control and M3S, which boasts ultra-low RSP and superior switching losses, making it ideal for high-speed applications like EV applications.

M3S technology is optimized for high-frequency switching applications in electric vehicles, such as on-board chargers (OBC) and high-voltage DC/DC converters.

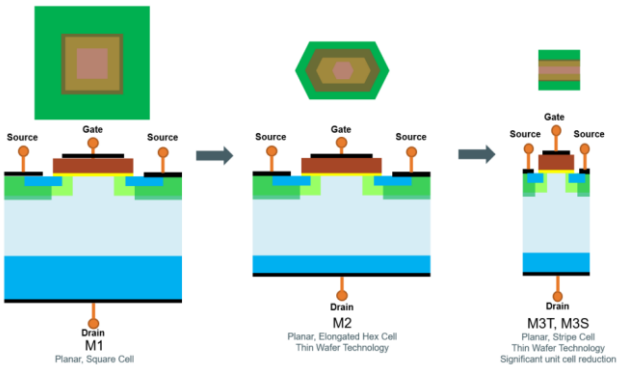

Fig 1. Technology Evolution of EliteSiC MOSFET

These MOSFETs balance conduction and switching losses, making them ideal for hard-switching applications like Power Factor Correction (PFC). Additionally, their low RDS(on) values make them suitable for soft-

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switching applications, where circuit topology minimizes switching losses, making conduction losses the primary concern.

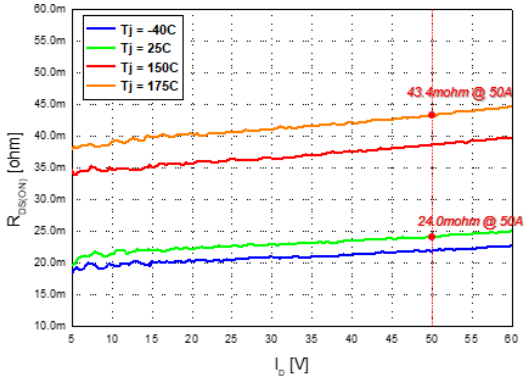
2 Electrical Characterization Findings

This section of the paper focuses on comparing onsemi M3S family member, NVH4L022N120M3S.

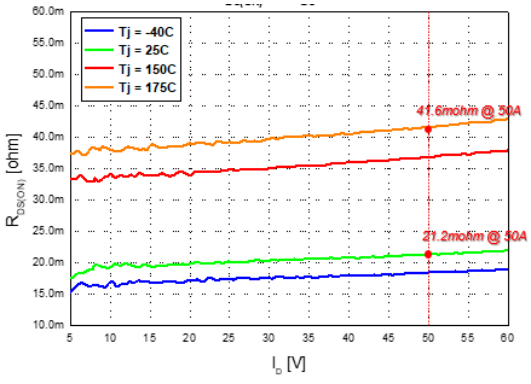
SiC MOSFETs are packaged in TO247−4L packages. Through dynamic characterization tests conducted under various conditions using a double−pulse test setup, I analyze and compare the static and dynamic parameters of the two devices.

2.1 Static Parameters – $R_{DS(on)}$

The crucial static parameters of SiC include $R_{DS(on)}$ and V_F (body diode voltage drop). Consequently, we analyze and characterize the $R_{DS(on)}$ and VSD parameters for two devices across different test scenarios. Specifically, Figure .1 presents a difference of the $R_{DS(on)}$ between V_{GS+} = 15V and V_{GS+} = 18V.



(a) $R_{DS(ON)}$@V_{GS+}=15V



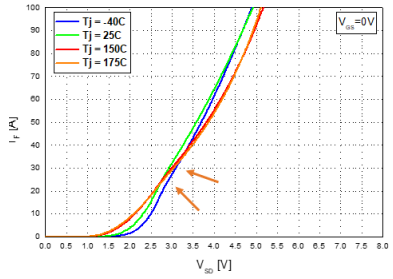
(b) $R_{DS(ON)}$@V_{GS+}=15V

Fig. 2. $R_{DS(ON)}$ value by Junction Temperature and Gate Voltage

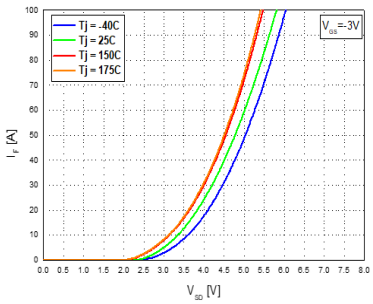
As indicated by the data presented in the above figure, there is a noticeable discrepancy of 2.8 mΩ in Rdson values observed at a temperature of 25 degrees. This underscores the importance of selecting the appropriate gate voltage tailored to the specific characteristics of each topology. It becomes possible to mitigate power losses to the greatest extent feasible, thus optimizing the overall performance of the system.

2.2 Static Parameters – V_F

As demonstrated in both Figure .2 and Table. 1, it is evident that the forward voltage (V_F) of the SiC MOSFET exhibits an increase with the application of a negative bias. Therefore, when formulating system designs, it is essential to take into consideration the influence of negative bias. As seen in Fig. 2 (a), the forward voltage (V_F) characteristic at V_{GS} = 0 V represents a combination of body diode conduction and channel leakage. As the junction temperature (T_J) increases, the threshold voltage (V_{th}) decreases, resulting in increased channel leakage. This phenomenon is observed as a deviation in the V_F characteristic compared to V_{GS} = -3 V, where channel leakage is entirely suppressed. In the above experimental results, it is observed that the forward voltage (V_F) of SiC exhibits a significant difference compared to other freewheeling diodes. This discrepancy arises due to the Modulation Index (MI) when driving a three-phase inverter using SiC MOSFETs, resulting in notable variations in diode power losses. Consequently, when employing SiC MOSFETs in a three-phase inverter, the diode losses also significantly influence the overall system power losses.



(a) V_{GS}=0V



(b) V_{GS}=-3V

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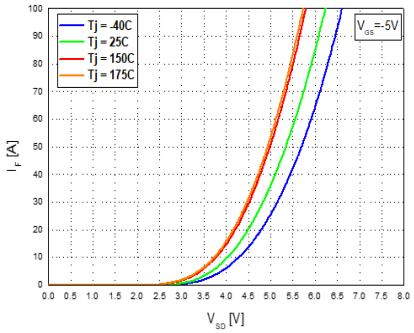


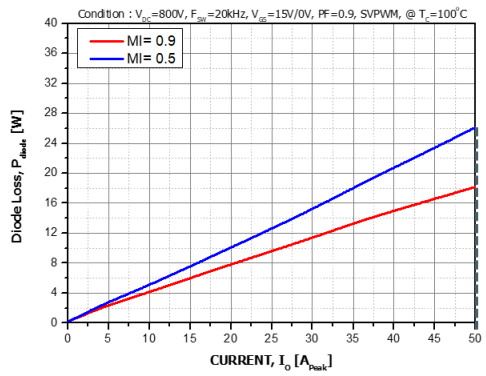
(c) V_{GS}=-5V

Fig. 2. Diode Forward Voltage (V_F) by Gate Voltage

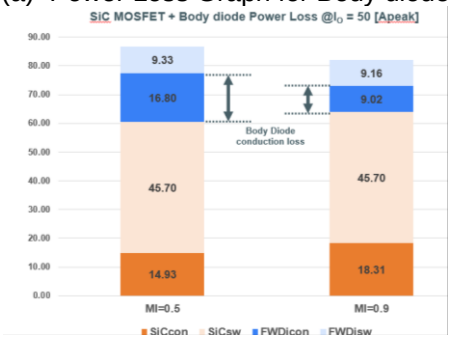
Table.1 Diode Forward Voltage (V_F) at 50A by Gate Voltage

Condition	V_F [V] @ 50A		
	T_J= -40℃	T_J = 25℃	T_J = 175℃
V_{GS}=0V	4.90	4.93	5.12
V_{GS}=-3V	6.05	5.85	5.42
V_{GS}=-5V	6.61	6.24	5.74

As shown in Figure .3 below, a discernible trend emerges diode power losses exhibit variance dependent on the Miller effect (MI). Remarkably, as MI approaches unity, a notable reduction in diode power losses becomes apparent, showcasing the intricate relationship between MI and power dissipation [4].



(a) Power Loss Graph for Body diode



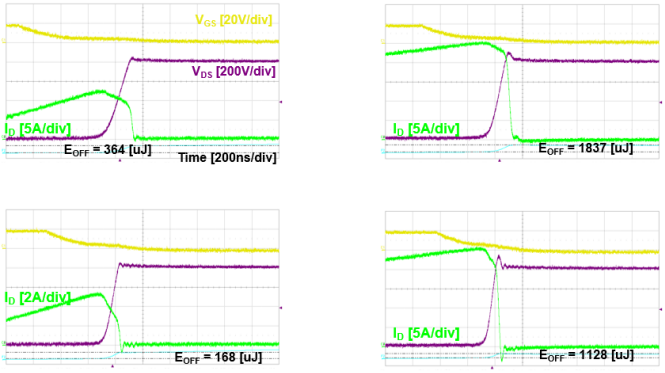
(b) Power Loss distribution

Fig. 3. Power Loss Simulation Result by MI

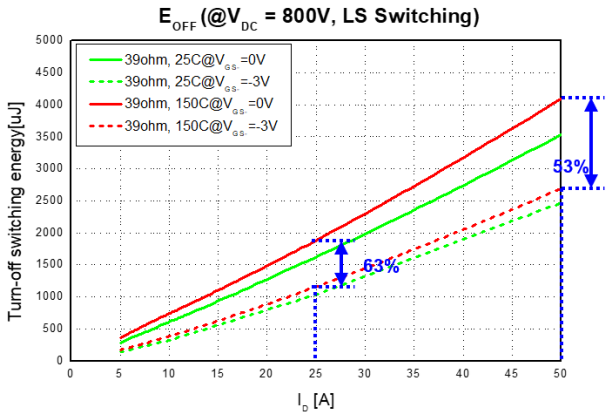
2.3 Dynamic Parameter

Among the dynamic parameters, it is noteworthy that Eoff varies significantly with negative bias during turn-off. This parameter can be determined by system designers and is crucial to consider during design due to its substantial impact on overall performance and system cost. The SiC MOSFET generates overvoltage (di/dt) and overcurrent (dv/dt) owing to rapid switching speeds and parasitic components [3].

As shown in Figure .3 below, Eoff exhibits a 63% difference at 25A. Therefore, ensuring system stability requires careful determination of appropriate gate resistance and bias.



(a) waveform



(b) Turn-off energy

Fig. 3. Turn Off waveform by Negative Gate Voltage

The switching speed is determined by the gate resistance, and a lower gate resistance results in increased dv/dt. As shown in Figure .4, this dv/dt can sometimes create unwanted gate voltage through Cgd, leading to malfunctions. Typically, such malfunctions are caused by three main factors.

- R_{G_OFF}: R_{G_OFF} is increased → Increasing V_{GS}
- R_{G_ON}: R_{G_ON} is decreased → Increasing dv/dt
- T_J: T_J is increased → Decreasing V_{th}

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Based on experimental results, it appears appropriate to use R_{G_ON} of 10 ohms and R_{G_OFF} of 2 ohms for achieving stable operation when employing zero voltage. However, it is essential to note that these values may vary depending on experimental conditions and gate driving circuitry. Therefore, users should select suitable resistances to prevent malfunctions.

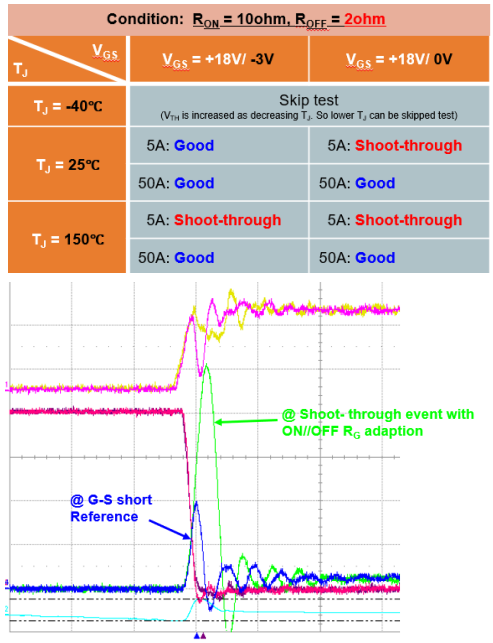

Fig. 4. Test result Malfunction Waveform by Cdvdt event

3 Conclusion

In conclusion, this study's thorough analysis of SiC-based power converters and inverters has provided valuable insights into key parameters affecting system performance. By examining static and dynamic parameters such as $R_{DS(on)}$, V_F, Eoff, and gate resistance, we've highlighted the importance of selecting appropriate gate voltages and resistances to optimize switching speed and minimize power losses. Additionally, our findings underscore the significance of considering modulation index (MI) effects on diode power losses in three-phase inverter applications. Moving forward, further research should validate these insights under real-world conditions to drive efficiency and performance improvements in SiC-based power electronics.

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