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Optimizing Turn-off Controllability of Micropattern Trench IGBTs for 900 A ED Type Modules

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Abstract

Low voltage trench isolated gate bipolar transistors (trench IGBTs), ranging from voltages of 750 V to 1700 V, are widely used in power electronics applications such as e-mobility, industrial and renewable energy. For the optimization of the power device, the chip must be designed according to the target application, each of which presents their own requirements regarding the switching frequency, power factor, stray inductance, and modulation strategy. This presents a significant challenge since the device is expected to perform well for different applications.

In this paper, an in-depth analysis of the effects of various design parameters on the IGBTs performance is demonstrated with experimental data. Finally, a conclusion is drawn on how to achieve the most optimized device design for a given application. Optimized solutions for a widely used package type (ED type) with state-of-the-art current density are presented.

1 Introduction

Key performance figures of IGBTs indicated in the datasheet are conduction loss ($V_{ce,sat}$) and turn-off loss (E_{off}) which determines the power dissipation in the IGBT, and therefore, the maximum effective current the device is able to switch at a given junction temperature (T_{vj}). Additionally, the safe operating area (SOA) is often indicated for short-circuit (SCSOA) and elevated current levels (RBSOA). This is needed for system designers to define the safety margins and maximum allowable voltage/current levels. Also the switching delay times ($t_{d,off}$ and $t_{d,on}$) are given by the semiconductor supplier for the programming and tuning of the gate-units.

Other less well-known metrics can also be very important for the performance of a device, such as behavior at elevated stray inductances, peak voltage slopes (dV/dt), peak overvoltage ($V_{ce,max}$), turn-off and turn-on controllability. For the purpose of this work turn-off controllability, understood as how well the switching parameters can be influenced by the external gate resistor $R_{G,off}$.

1.1 Turn-off controllability

When operating an IGBT in application, care must be taken to limit the peak overvoltage ($V_{CE,max}$) below the allowable limit under all possible switching conditions. The peak overvoltage of a certain IGBT design is a complicated function of junction temperature (T_{vj}), current and voltage levels, stray inductance (L_σ), and gate resistor ($R_{G,off}$) and capacitor (C_{GE}). This function is also highly dependent on the design parameters of the device [1], which will be shown in chapter 3.

If an IGBT exhibits excessive overvoltage at desired switching conditions, either the voltage or current levels must be derated, or the gate conditions can be changed, usually by increasing $R_{G,off}$ or C_{GE} . Slowing down switching speed however presents the drawback of increasing E_{off} and $t_{d,off}$ [1-3]. Especially for applications with increased L_σ (e.g. three-level inverters for wind and solar power) keeping the overvoltage below the rated value is a key constraint, which must be addressed on device level to achieve best performance.

1.2 Carrier confinement

Carrier confinement describes the concentration of excess charge carriers at the emitter-side of the device in the conducting state. Several factors can be used to influence the effective carrier confinement, such as an n-enhancement layer, the geometry and mesa of the active trenches [4], and the arrangement of active vs inactive trenches. Higher carrier confinement significantly improves the on-state performance, but can degrade RBSOA, SCSOA and the turn-off controllability [1], especially with higher n-enhancement doses. However, there are some results indicating that by scaling the mesa the negative effects of the n-enhancement layer can be largely avoided, while still achieving the desired reduction in $V_{CE,sat}$ [5].

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2 Experimental study

2.1 Description of samples

For this study, 1200 V IGBTs with different designs resulting in different levels of carrier confinement, as well as different anode and buffer doses were manufactured. **Table 1** shows an overview of the tested samples. The combination of anode dose and buffer dose determines the anode efficiency of the device. The anode efficiency can be freely tuned to move the IGBT along the technology curve, since more plasma injection leads to lower $V_{CE,sat}$ but conversely higher turn-off losses. For layouts 1A, 1B and 1C the drift layer thickness is increased by 10 µm to recover the blocking capability lost by reducing the field-stop layer.

A key element of this experiment is the shape of excess carrier concentration within the drift region of the IGBT under conduction, which depends on the anode efficiency and the carrier confinement. The anode efficiency determines the concentration of holes injected into the device from the backside, whereas the carrier confinement determines the efficiency of plasma extraction on the frontside. **Fig. 1** shows the simulated concentration of excess charge carriers along a vertical cutline of the devices during current conduction.

The next-gen devices differ from the rest of the samples as they are designed and produced with a much more advanced technology platform, allowing for aggressive scaling of trench mesa and active cell pitch. A side-by-side comparison of the active cell of current-gen and next-gen devices is shown in **Fig. 2**. The aspect ratio of the trenches is roughly doubled, whereas the mesa is halved in the next-gen device. Additionally, the total trench density is increased almost threefold. The next-gen optimized device is identical to the baseline next-gen, except for increased active channel density. This is not expected to affect the turn-off characteristics.

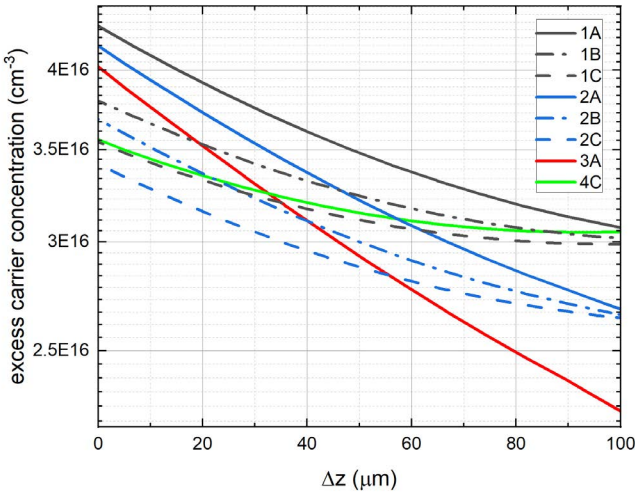

Fig. 1: Simulated excess carrier concentration along a vertical cutline at T_{vj} = 175 °C, J = J_{nom}. The emitter side of the device is at z = 0.

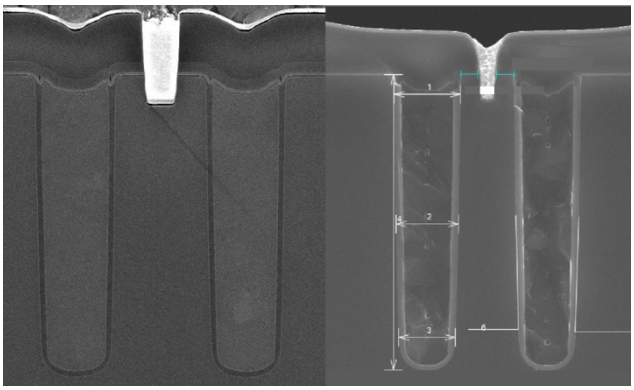

Fig. 2: SEM images of the cross-sections in the active regions of the fabricated devices. Left: current-gen, right: next-gen. The two images are shown in the same scale.

Table 1: Overview of tested samples.

					Max DS ratings	
Device	**Anode dose**	**Buffer dose**	**Thickness**	**Carrier confinement**	**Peak current density (A/cm²)**	**SC time @ 175 °C (µs)**
1A	Mid	Low	+10 µm	High	300	8
1B	Mid	Low	+10 µm	Mid	300	10
1C	Mid	Low	+10 µm	Low	300	≥10
2A	Mid	High	Std	High	300	8
2B	Mid	High	Std	Mid	300	10
2C	Mid	High	Std	Low	300	≥10
3A	Low	High	Std	High	300	8
4C	High	High	Std	Low	300	≥10
next-gen	Mid	High	Std	Low	360	≥10
next-gen optimized	Mid	High	Std	Low	360	6

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3 Results

3.1 Experimental setup

The IGBTs are assembled on test substrates, and subsequently measured both statically and dynamically. Standard double pulse tests, and tests with increased voltage and current conditions are undertaken. Finally, the samples are checked for their short-circuit withstand capabilities. For direct comparison all measurements for the technology curve and turn-off controllability follow the same current density J_{nom}.

3.2 Technology curve

Fig. 3 shows the measured technology curve at nominal current level and high temperature. The anode efficiency, determined by the anode and buffer doses, moves the devices along the technology curve. Reduction of carrier confinement leads to a significant increase in $V_{CE,sat}$, indicated by the straight arrows in the graph.

By reducing active cell pitch and trench mesa, the conduction losses can be recovered even at low carrier confinement, as can be seen in the next-gen device. The next-gen optimized device with higher SC current is improved in on-state by an additional 85 mV.

Devices 1A, 1B, and 1C are on a slightly worse technology curve compared to the other devices with the same level of carrier confinement, since the drift region is 10 µm thicker to recover the necessary blocking voltage.

3.3 Turn-off controllability

The samples were tested at elevated voltage levels of 750 V and double nominal current density, inducing overvoltage conditions. The test was repeated at a range of $R_{G,off}$ values and the resulting $V_{CE,max}$ is plotted against $t_{d,off}$ in **Fig. 4**. In this case, the device is called *more controllable* if the peak overvoltage decreases more rapidly with increasing delay times.

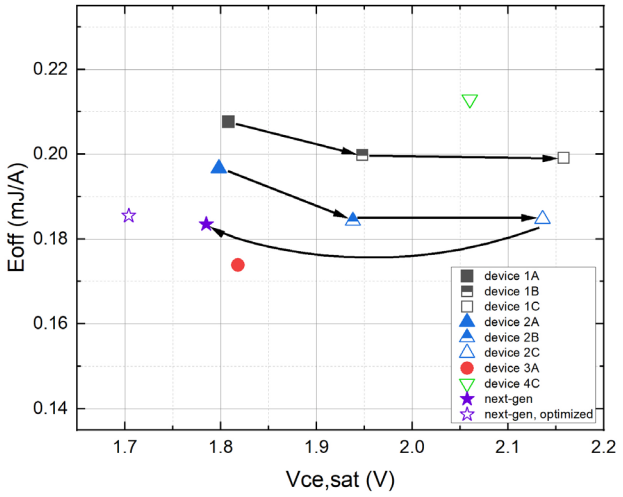

Fig. 3: Technology curve measured at T_{vj} = 175 °C, V_{CC} = 600 V, L_s = 32000 nH*A, J = J_{nom}.

Higher anode efficiency tends to decrease the peak overvoltage across all tested conditions, but the controllability is not significantly improved with higher anode efficiencies. Conversely, decreasing the carrier confinement leads to an increase of the worst-case overvoltage, but better behavior at higher delay times. This can be observed when comparing device 1A and 1C, or 2A and 2C. Devices 1C and 2C are more controllable. But devices 1A, 1B and 1C are always overall softer switching compared with their lower anode efficiency counterparts 2A, 2B and 2C. Considering **Fig. 3** and **Fig. 4**, a clear tradeoff between controllability and losses emerges. With the next-gen device, the tech curve can be recovered or improved while keeping high turn-off controllability. No significant difference in turn-off controllability is observed between the next-gen and the next-gen optimized devices.

Fig. 5 shows turn-off waveforms at the corresponding points of **Fig. 4** for selected devices. Higher anode efficiencies decrease the overvoltage and especially the snap-off, which occurs when the current vanishes abruptly, causing a high negative dV/dt which induces undesirable oscillations. Lower carrier confinement and higher anode efficiency, which causes a “flat” excess carrier distribution, offers by far the best dI/dt and dV/dt control, allowing for soft switching with acceptable delay times and turn-off losses even at harsh switching conditions.

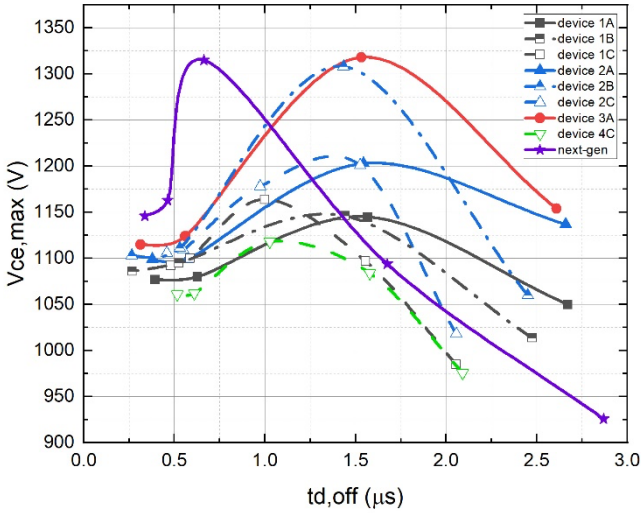

Fig. 4: Peak overvoltage vs turn-off delay time measured at T_{vj} = 25 °C, V_{CC} = 750 V, L_s = 64000 nH*A, J = 2xJ_{nom}.

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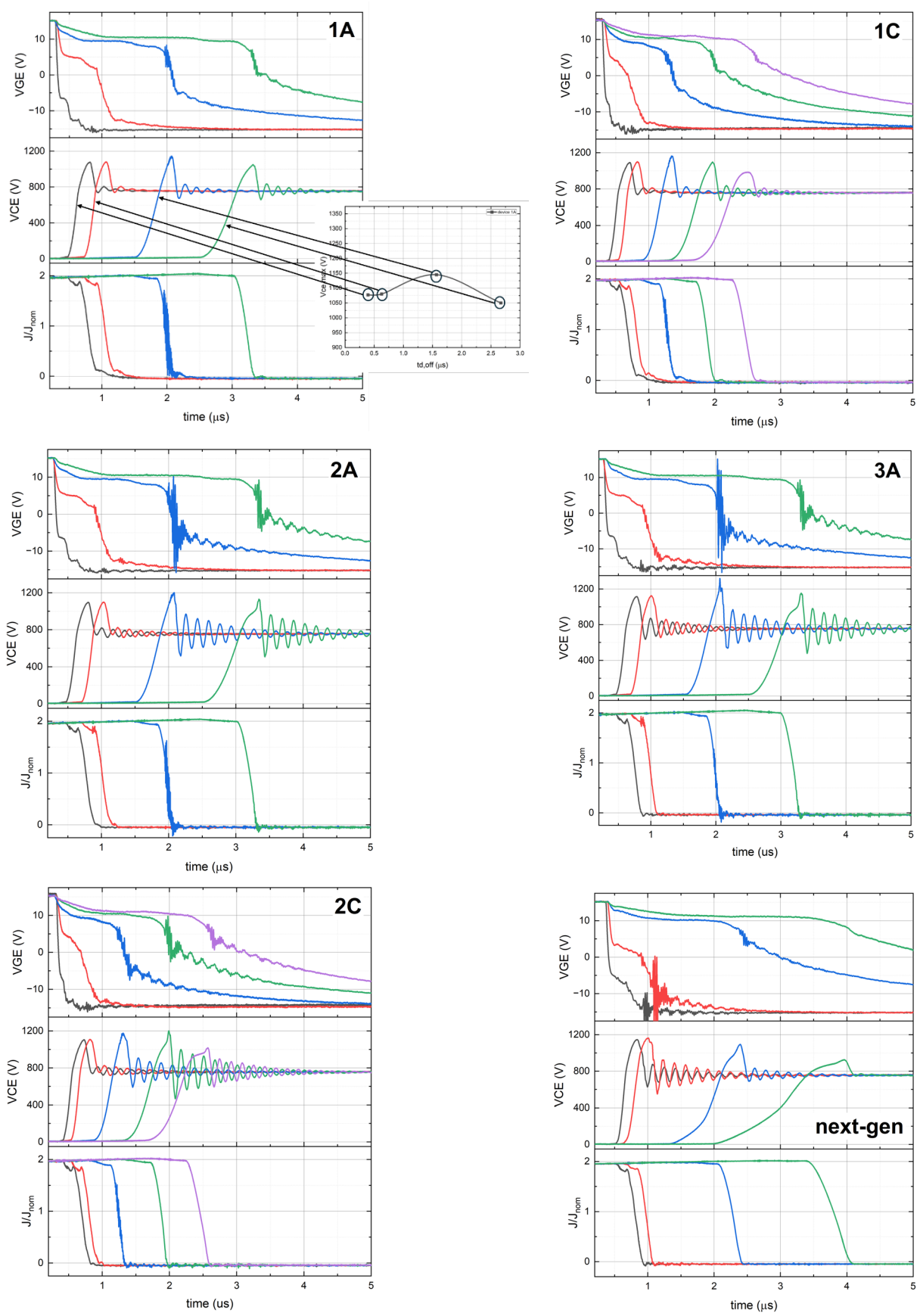

Fig. 5: Measured turn-off waveforms at T_{vj} = 25 °C, V_{CC} = 750 V, L_s = 64000 nH*A, J = 2xJ_{nom} and different $R_{G,off}$ values. Top left: layout 1A, top right: device 1C, middle left: device 2A, middle right: device 3A, bottom left: device 2C bottom right: next-gen.

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3.4 SCSOA

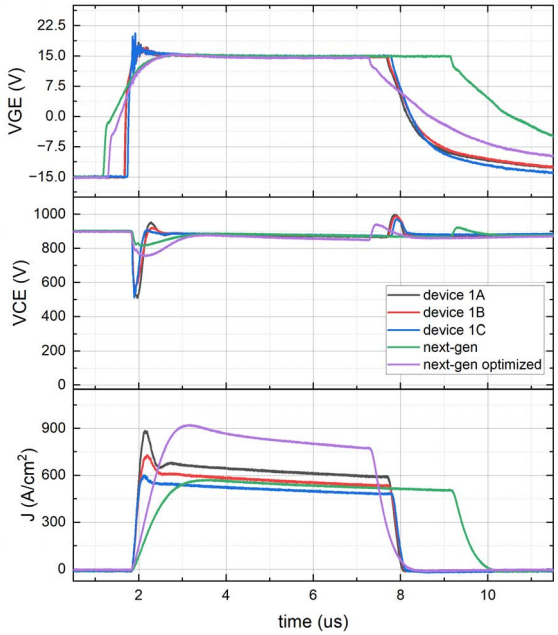

Fig. 6: Measured SCSOA waveforms at T_{vj} = 175 °C, V_{CC} = 900 V, V_{GE} = 15 V, $t_{p,sc}$ = 6 µs (8 µs for next-gen).

Fig. 6 shows the SCSOA waveforms of selected samples. The anode efficiency has less impact on the short-circuit current than the carrier confinement. It can be clearly seen that the level of carrier confinement with the same backside correlates directly with the short-circuit current. The next-gen device shows a similar level of SC-current as device 1C, but with an improvement of roughly 500 mV in $V_{ce,sat}$. This is achieved by the combination of higher active cell density and the much narrower trench mesa compared to the current generation IGBT, shown in **Fig. 2**. Considering current market demands, the SCSOA withstand time of the next-generation device can be reduced from over 10 µs to 6 µs by increasing the n-source ratio, thereby gaining an additional ~85 mV on-state reduction, without compromising the turn-off controllability.

3.5 RBSOA

Device 1A and the next gen chip were assembled in standard industrial modules (ED-type, **Fig. 7**) with a current rating of 600 A and 900 A, respectively. For the ED-type module, the current density of the next-gen chip is uprated by a factor of 1.25 compared to the current device. This is justified by the significant improvement in technology curve and excellent soft-switching behavior. To verify the current rating the modules were tested at V_{CC} = 900 V, T_{vj} = 175 °C and I_{CE} = 1200 A and 1800 A, respectively. **Fig. 8** shows the waveforms of the RBSOA tests. Both device 1A as well as the next-gen platform are able to withstand two times rated current at V_{CC} = 900 V and T_{vj} = $T_{vj,max}$.

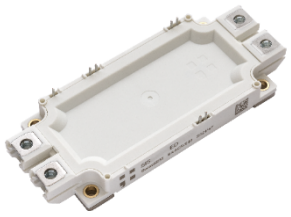

Fig. 7: SwissSEM ED-type power module.

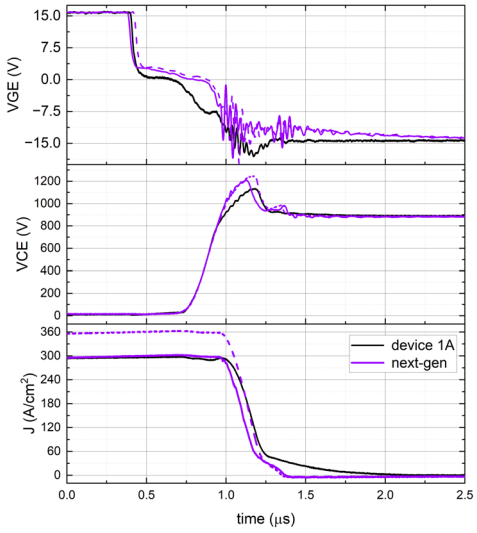

Fig. 8: Measured RBSOA waveforms at T_{vj} = 175 °C, V_{CC} = 900 V, L_s = 35 nH, I_{CE} = 1200 A for device 1A ; I_{CE} = 1500 (solid line) and 1800 A (dashed line) for the next-gen device.

4 Conclusion

Different IGBT designs have been assembled and tested under various conditions. For applications with high L_σ, such as three-level inverters, layout 1A provides the most optimized performance as the device can be operated at low gate resistance While still achieving low $V_{CE,max}$. The increased E_{off} shown by this device is less of an issue at these conditions since these inverters typically operate at lower switching frequencies [6]. While reducing carrier confinement on its own benefits controllability, the increase in $V_{CE,sat}$ does not justify the benefit. Conversely, the next-gen device performs well at low stray inductances and can be switched to perform well at higher stray inductances, without showing excessive switching times. Therefore, the next-gen device is more suitable for a broader application range. Additionally, the next-gen device allows for a higher peak current density while maintaining RBSOA capabilities. The tests on module level showed SCSOA capabilities which matched the DS conditions. The modules assembled with device 1A have low voltage overshoot at comparably much lower switching times, allowing for increased performance at high stray inductance. The next-gen device offers state of the art current density and performs very well at both high and low stray inductance applications.

5 References

[1] R. Baburske, F. Pfirsch, J. Hänsel and K. Waschneck, "Si IGBT and SiC MOSFET – Potentials and Limitations of Plasma Shaping versus Unipolar Switching in Medium Power Applications," 2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Hong Kong, 2023, pp. 159-162

[2] W. Saito and S. -i. Nishizawa, "High Switching Controllability Trench Gate Design in Si-IGBTs," 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020, pp. 447-450

[3] A. K. Pulikkathodi, V. Suresh, Shao-Ming Yang and G. Sheu, "Investigation in characteristics of 1200V vertical IGBT for different trench designs," 2013 IEEE International Conference of Electron Devices and Solid-state Circuits, Hong Kong, China, 2013, pp. 1-2

[4] M. Rahimo, “Future trends in high-power bipolar metal-oxide semi-conductor controlled power semi-conductors,” IET Circuits Devices Syst., 2014, 8: 155-167.

[5] E. Buitrago, M. Antoniou, N. Schneider, E. Bianda, L. De-Michielis, C. Chorvasce and F. Udrea, "Experimental Demonstration of Point-Injection Trench IGBT Concept," 2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Hong Kong, 2023, pp. 179-182

[6] Y. Liu, Y. Zhang, P. Wu and J. Li, "Development review and market research of IGBT devices for PV inverter and Wind power converter," 2020 17th China International Forum on Solid State Lighting & 2020 International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS), Shenzhen, China, 2020, pp. 30-33

