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Balancing Switching Transient of Paralleled SiC-MOSFETs by Using Adaptive Gate Current Shaping

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Abstract

In high power applications, SiC-MOSFETs are often connected in parallel to increase RMS current rating of the system. However, this normally leads to unbalanced current sharing, especially during switching transients, resulting in uneven system aging and long-term reliability issues. This study proposes a new gate drive methodology utilizing an advanced gate driver IC. The proposed gate drive method can adjust the gate drive strength individually to each gate loop of the paralleled SiC-MOSFETs based on their actual gate charge characteristics, resulting in a more balanced dynamic-stress distribution for the system.

1 Introduction

Advancements in power electronics technologies have significantly increased the need for power devices that support higher current and voltage, leading to greater power densities accompanied by improved efficiency [1], [2]. Silicon carbide MOSFETs (SiC-MOSFETs) are becoming the key solution to these requirements. Compared to silicon (Si) insulated gate bipolar transistors (IGBTs), SiC-MOSFETs feature several superiorities, including fast switching speed, high operating temperatures, high breakdown voltage, lower switching loss.

Despite these superiorities, SiC-MOSFET device still have relatively low current rating at the current stage of development [2]. To reach higher current ratings, it is a common practice in power-electronic system design to connect multiple discrete devices or bare dies of power module in parallel. However, this parallel configuration introduces the major challenges of current imbalance, which can be classified into two categories :

- Static imbalance: occurring in steady state, primarily arises from mismatches in on-state resistance (R_{DSon}).
- Dynamic imbalance: occurring in switching transients, due to various factors such as mismatched parameters in gate drive circuits (e.g., gate resistance R_g, gate inductance L_g), power device parameters (e.g., threshold voltage Vth, transconductance g_m) and power circuit layout (e.g., source resistance R_s, source inductance L_s, commonly named as parasitics).

While static imbalance is inherently self-limited due to the positive temperature coefficient of R_{dson} in most commercially available SiC-MOSFETs, dynamic imbalance is more challenging to eliminate due to the short duration of switching events [3]. Unbalanced current distribution results in uneven stress conditions, influencing the aging and consequently rises some drawbacks such as requiring safety margin in the design or long-term de-rating of power module, thereby prevent the power module from being utilized to its full performance potential.

To address current imbalance in paralleled devices, various methods have been developed, broadly classified into passive and active approaches.

Passive methods focus on minimizing the impact of mismatched electrical parameters by optimizing package or circuit layout, or through preselection. These methods, however, are typically expensive, time-consuming, and unable to adapt to changing operating conditions.

Active methods use auxiliary circuits or components to achieve drain current balancing, including external passive components and external active components. External passive components methodologies can adjust the current distribution via adding passive components in the gate loop or power loop. For example, adding series resistors or inductances in the high current paths is a possible method to achieve current sharing [4], [5]. However, this can lead to additional losses, reduced switching speed, and increased stress on components, resulting in decreased efficiency.

Generally, the inflexibility and limitation of the two methods mentioned above make them unsuitable for all operating conditions, as circuit layout or passive

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components cannot be altered during operation. Therefore, active methods with active components, namely active gate drivers (AGDs), are desired, which focus on adapting the gate drive of each MOSFET individually according to the working conditions. In [6], an AGD is presented, which generates different delays on the gate drive signal applied to each MOSFET in range of picosecond, adjusting the time each MOSFET starts conducting. However, the method to calculate suitable delay values is not presented. Another digital AGD is proposed in [7], which can synchronize the drain current edges and slopes of paralleled SiC-MOSFETs. Nevertheless, it has a complex control circuit and requires several switching cycles to achieve the current balancing.

To overcome the disadvantages mentioned above, a novel AGD method is proposed for dynamic current balancing of paralleled SiC-MOSFETs. This new gate drive concept utilizes an advanced gate driver IC, designed by Robert Bosch GmbH, which can generate individual gate drive strengths for each SiC-MOSFET based on their actual characteristics. The modulation of gate drive strength is achieved through the adjustment of gate current across several time-based segments.

The whole work described in this article is organized as follows: In Section 2, the mechanism of dynamic current imbalance is analyzed. Based on these fundamentals, Section 3 presents the strategy of gate current shaping for the AGD. After that, Section 4 details the hardware setup used to evaluate the effectiveness of this concept, followed by an analysis of the experimental results. Finally, Section 5 provides the outlook and conclusions of the study.

2 Dynamic current imbalance mechanism

Dynamic imbalance in parallel-connected MOSFETs occurs when there are mismatches in drain current transition during switching events. Generally, the dynamic imbalance can be considered as a combination of two special cases of asynchronization:

a) Current edges asynchronization: The drain currents of the paralleled MOSFETs commutate at different time points but with the same slew rates.
b) Current slopes asynchronization: The drain currents of the paralleled MOSFETs starts to commutate at the same time point but with different slew rates.

Figure 1 illustrates these two conditions by a turn-on transition of two paralleled MOSFETs.

Current edges asynchronization occurs when two MOSFETs reach their threshold voltage V_{th} at different times. Similarly, the current slopes asynchronization is determined by the time each MOSFET takes to transit from threshold voltage V_{th} to plateau voltage V_{pl}. These

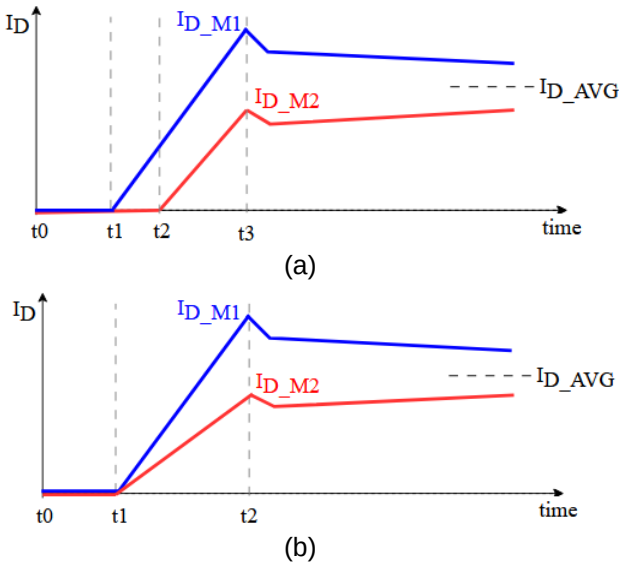

Fig. 1. Turn-on process of the two special cases of dynamic current imbalance in paralleled MOSFETs. (a) Current edges asynchronization (b) Current slopes asynchronization

time deviations are typically caused by gate driver propagation delay, mismatched gate resistance and inductance, and by variations in MOSFET characteristics, such as different V_{th} and V_{pl} values between the two MOSFETs.

Given that the drain-source voltage V_{DS} of parallel-connected MOSFETs is nearly identical, the distribution of switching loss and stress is primarily influenced by the drain current I_D. In an extreme scenario of a turn-on transition, one MOSFET switches significantly earlier than the other and ends up carrying the entire load current and with it the switching losses. Conversely, the other MOSFET then operates in an almost zero-load switching mode, experiencing minimal stress.

A similar analysis applies to the turn-off transition. If one MOSFET begins to switch off earlier than the other, the load current will transfer to the MOSFET with later switch-off time, which is depicted in Figure 2. It is noteworthy that if a MOSFET withstands higher current stress during turn-on process due to its lower V_{th} and V_{pl}, it will also face higher stress during turn-off because it will switch off later than the other MOSFET. This worsens the stress imbalance, leading to one MOSFET consistently experiencing higher stress.

3 Concept of proposed AGD

The proposed AGD leverages a gate driver developed by Robert Bosch GmbH. This gate driver enables the programming of gate drive strength via gate current modulation over time-based segments. The programming can be independently configured for both turn-on and turn-off phases. Notably, these gate current profiles can be adjusted dynamically during operation of the gate driver. The gate current can be set with a current resolution of 9.8mA and a timing resolution of

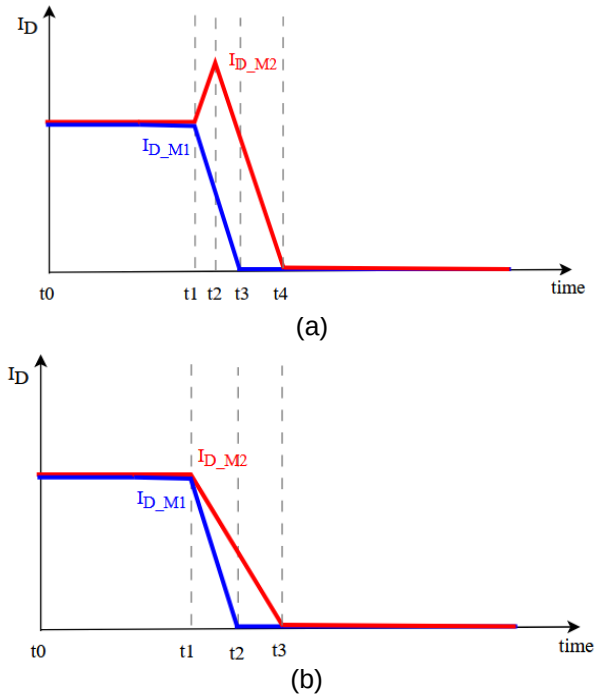

Fig. 2. Turn-off process off the two special cases of dynamic current imbalance in paralleled MOSFETs. (a) Current edges asynchronization (b) Current slopes asynchronization

1.66ns. The gate driver features four parallel channels, allowing individual connection and driving of each MOSFET's gate terminal.

An advantage of current-source gate driver is its ability to set different gate currents, thus actively controlling the amount of electric charge flowing into or out of the gate terminal. This is unlike conventional voltage-source gate driver with fixed gate resistors, in which gate current varies according to the voltage drop over this resistor, making it very difficult to monitor the gate charge during these switching events. Based on this feature, the dynamic synchronization of paralleled MOSFETs could be achieved by aligning the time that each MOSFET reaches their respective gate charge points throughout the switching process.

3.1 MOSFET Gate Charge

The switching process of MOSFET can be divided into four phases [8]. Figure 3 illustrates an inductive turn-on event, depicting the associated charge points and charge amount for each of these phases during the turn-on process.

During phase 1, the gate-source voltage V_{GS} transitions from the off-state voltage $V_{gs,off}$ to the threshold voltage V_{th}, where the drain current I_D starts to commutate. The gate charge at this phase is accumulated from 0 to Q_{th}. In phase 2, between V_{th} and the start of Miller plateau V_{pl}, respectively the gate charge point Q_{pl}, the drain current continues to rise and reaches to switching current. These two phases are crucial for current balancing strategies as they determine the current edges and current slopes of the MOSFET, which directly affect the imbalance mechanism as discussed in Section 2.

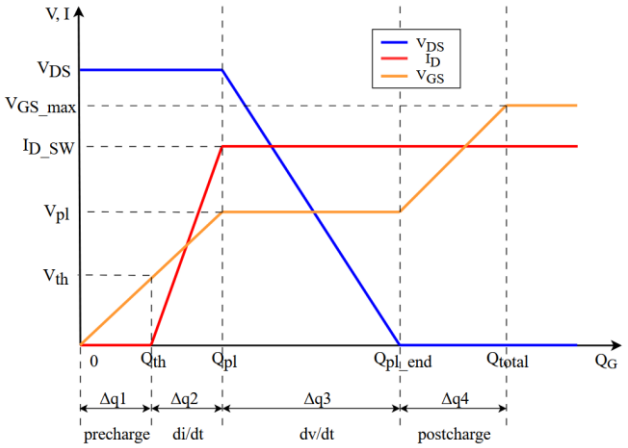

Fig. 3. Turn-on process with gate charge characteristics

Phase 3 and phase 4 are for the voltage commutation and settling of channel resistance R_{ds}. The gate charge points associated with these two phases are denoted as Q_{pl_end} and Q_{tot}, respectively. In these phases, the transition of R_{DS} until it reaches its settled value, R_{DSon}, also influences the dynamic current sharing ratio. However, the impact of this transition is not as critical as those observed in phase 1 and 2. This is due to the fact that V_{ds} decreases to nearly 0V after phase 3, significantly reducing the power dissipation.

During turn-off, these phases occur in reverse order.

3.2 Gate Current Shaping Strategy

As outlined in Section 3.1, the switching process of an individual MOSFET can be controlled by a positive and a negative charge flow in the gate terminals. Additionally, with the capability of the novel gate driver to feature segmented gate current profiles, it becomes feasible to independently control each phase in the switching process.

The strategy for achieving current balancing through gate current shaping is the step-by-step synchronization of current edges and slopes. To achieve this, each MOSFET needs to be controlled individually in a way that all MOSFETs reach their respective V_{th} and V_{pl} values at the same time. To implement this strategy, it is also required to have a reference transition that all MOSFETs should follow. This reference could be derived from the average transition length among all MOSFETs, or directly from one of the MOSFETs, such as the slowest or fastest one.

Figure 4 illustrates the step-by-step synchronization between two paralleled MOSFETs during a turn-on event, with the assumption that they have differences in

their gate charge characteristics. In this scenario, MOSFET 1 (M1) is designated as the reference and is driven with constant gate current. Meanwhile, MOSFET 2 (M2) is adapted to match the drain current I_D of M1. It is crucial to note that during the synchronization process as shown in Figure 4 and Figure 5, each MOSFET is switched independently from the other by individual gate-driver output stages. This ensures the synchronization of the drain current transitions for both MOSFETs before they are connected to work in parallel. When having the same constant gate drive current, M1 and M2 show asynchronization in current edges and current slopes due to deviations in their V_{th} and V_{pl}. M2 has higher V_{th} and V_{pl} values, so that it needs to be charged with higher gate current to reach V_{th} and V_{pl} simultaneously with M1.

The same strategy applies for turn-off process, as depicted in Figure 5. It is noted that there is a small dip in drain current before the actual di/dt phase happens. This is because the channel resistance R_{DS} starts increasing with the reducing of gate-source voltage V_{gs}.

For each charging segment, since the segment time is identical for both MOSFETs, the ratio of gate charge amount is also the ratio of gate current:

$$\frac{Q_{Gi\_M2}}{Q_{Gi\_M1}} = \frac{I_{Gi\_M2}.t_i}{I_{Gi\_M1}.t_i} = \frac{I_{Gi\_M2}}{I_{Gi\_M1}} \quad (1)$$

Here Q_{Gi}, I_{Gi} and t_i denote the gate charge amount, gate current and time duration of segment i. This equation can be generalized for more paralleled MOSFETs:

$$\frac{Q_{Gi\_n}}{Q_{Gi\_ref}} = \frac{I_{Gi\_n}}{I_{Gi\_ref}} \quad (2)$$

Which leads to:

$$I_{Gi\_n} = \frac{Q_{Gi\_n}}{Q_{Gi\_ref}}.I_{Gi\_ref} \quad (3)$$

, where notation n and ref denote the values belonging to the n-th MOSFET and reference MOSFET, respectively. According to equation 3, the gate current of segment i can be calculated based on the reference gate current of the same segment and the actual gate charge of each MOSFET. This calculation is applicable for both turn-on and turn-off. Additionally, the reference gate current I_{gi_M1}, or the general I_{gi_ref}, can be chosen or calculated using some strategies, such as those proposed strategies in

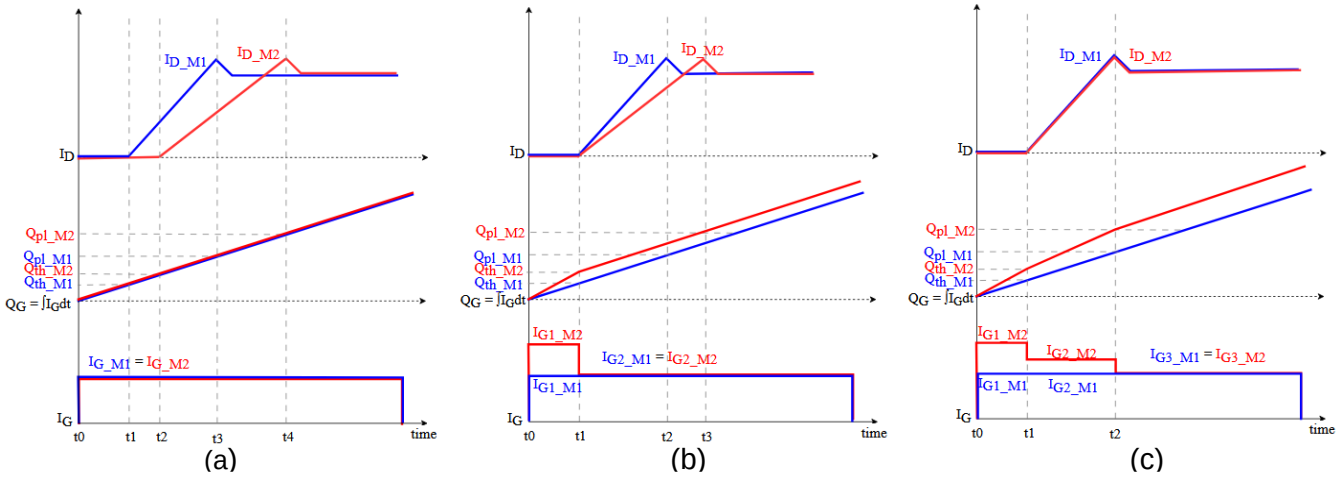

Fig. 4. Step-by-step current balancing strategy for turn-on process. (a) No synchronization (b) With current edges synchronization (c) With current edges and slopes synchronization

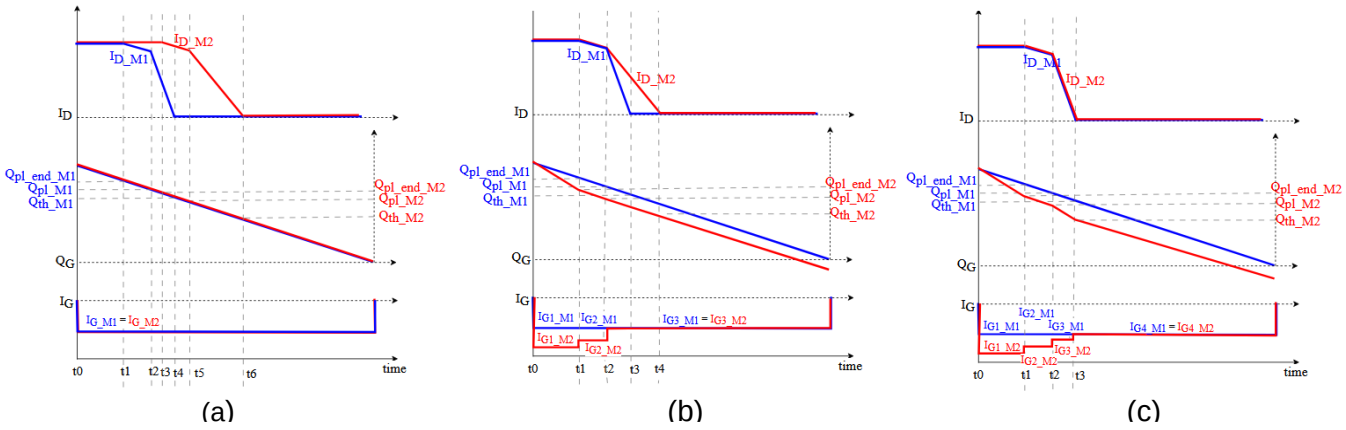

Fig. 5. Step-by-step current balancing strategy for turn-off process. (a) No synchronization (b) With current edges synchronization (c) With current edges and slopes synchronization

[9], [10]. Generally, when choosing gate current I_{gi_ref}, a trade-off between overall switching loss and system reliability should be considered. If I_{gi_ref} is too high, the switching process can be significantly accelerated, resulting in low switching loss but also posing risks such as high overshoots or increased electro-magnetic emission. On the other hand, if I_{gi_ref} is too low, it will unnecessarily slow down the switching event, causing worsened power dissipation and thermal stress.

Additionally, the segment time t_i also needs to be calculated based on the gate charge characteristics of the reference MOSFET using equation 4:

$$t_i = \frac{Q_{Gi\_ref}}{I_{Gi\_ref}} \quad (4)$$

Furthermore, the gate charge characteristics of a single MOSFET depends on its operating conditions. Therefore, there is no universal gate-shape that fits optimally under all conditions. Indeed, for each range of working conditions, a specific gate-shape needs to be calculated based on the actual gate charge characteristics. This proposed AGD concept is thus an operation point based method.

4 Experimental Verification

4.1 Test Setup

To evaluate the effectiveness of proposed AGD concept, a double pulse test setup is used. This double pulse setup relies on a half-bridge power module developed by Robert Bosch GmbH, along with the gate driver mentioned in Section 3. The half-bridge power module has a rated continuous drain current of 315A and a maximum drain-source voltage of 1200V. Each high-side and low-side consist of two paralleled MOSFETs, each with intentionally different gate charge characteristics. In this setup, the low-side MOSFETs are devices under test and are used as the active switching device, while the high-side MOSFETs are always turned-off and act like freewheeling diodes. The schematic of the test setup is shown in Figure 6.

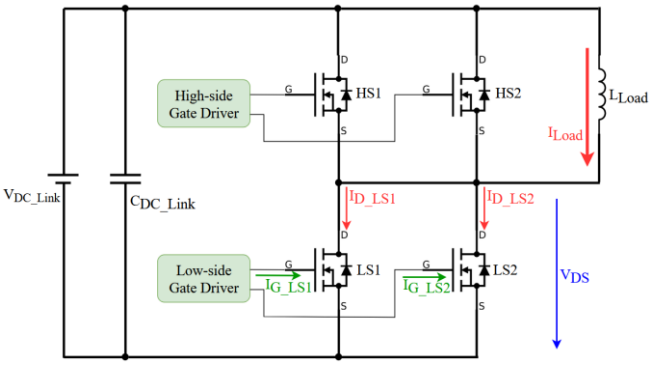

Fig. 6. Schematic of double pulse test setup

To validate the proposed concept, a double pulse test is carried out at two different operating points of V_{DC_Link} with the same I_{sw} and room temperature:

1) 400V, 100A
2) 600V, 100A

At each of these working points, the actual gate charge characteristics of each MOSFET in the low-side are measured. Based on these measurements, the gate shape is calculated for low-side MOSFET 2 (LS2), while the low-side MOSFET 1 (LS1) is taken as reference. For simplicity, the gate current of LS1 is set as constant value, and thus, the gate current shaping is only applied to LS2. However, the small V_{DS} deviation due to different power loop inductances between each MOSFET is also neglected, the V_{DS} is assumed to be identical for both MOSFETs.

The performance of the proposed AGD concept is then compared with the case when both MOSFETs are driven with the same constant gate current.

4.2 Result and Evaluation

First, the gate charge characteristics at two working points are measured separately for each MOSFET using the same test setup. To do this, the MOSFET that is being measured is turned-on, while the other MOSFET is turned-off. The measurement results are presented in Table 1.

	400V		600V	
	LS1	LS2	LS1	LS2
Q_{th} (nC)	49.76	50.27	52.90	56.73
Q_{pl} (nC)	81.25	88.19	81.28	86.61
Q_{pl_end} (nC)	102.802	110.44	106.86	110.54
Q_{tot} (nC)	195.93	191.02	205.41	198.16

Table 1. Gate charge measurements at 400V and 600V

After that, the reference constant gate current is experimentally chosen for LS1, which is 98mA. This value ensures acceptable overshoots of the MOSFETs during double pulse test. Based on the reference gate current of LS1, the current profiles are calculated and applied to LS2. It could be seen that there are some differences in the gate charge of two MOSFETs at two different V_{DC_Link}. This is due to the C_{iss} versus V_{DS} dependency of MOSFET. These variations in gate charge affect the gate shape calculation, resulting in two different gate shapes of LS2, despite the reference gate current from LS1 being consistent at 98mA for both test conditions. Table 2 and Table 3 present the calculated turn-on and turn-off gate shape for LS1 and LS2 at 400V-100A and 600V-100A. Note that the presented values are already rounded according to internal resolutions of the gate driver IC. Besides, the last segments of turn-on and turn-off do not have the time settings, because their current values are kept infinitely until the switching process is done.

Phase	I_{G_LS1} (mA)	I_{G_LS2} (mA)	Time (ns)
Turn on			
Pre-charge	98	98	508
di/dt	98	118	320
dv/dt	98	98	53
Post-charge	98	108	--
Turn off			
Pre-discharge	98	88	951
dv/dt	98	98	221
di/dt	98	118	322
Post-discharge	98	98	--

Table 2. Gate shape values calculated for 400V, 100A

Phase	I_{G_LS1}(mA)	I_{G_LS2} (mA)	Time (ns)
Turn on			
Pre-charge	98	108	540
di/dt	98	108	289
dv/dt	98	88	53
Post-charge	98	88	--
Turn off			
Pre-discharge	98	88	1006
dv/dt	98	88	261
di/dt	98	108	289
Post-discharge	98	108	--

Table 3. Gate shape values calculated for 600V, 100A

The results for both turn-on and turn-off processes are summarized in Table 4. The degree of imbalance is quantified as the switching loss deviation relative to the total switching loss:

$$DoI = \frac{|E_{LS1} - E_{LS2}|}{E_{total}} = \frac{|\Delta E|}{E_{total}} \quad (5)$$

The closer this DoI value comes to 0% indicates a better balancing. Additionally, the measured I_D and V_{DS} waveforms, along with power dissipation at 600V, are depicted in Figure 7 and 8.

During turn-on, the original mismatch between LS1 and LS2 is relatively small due to their close Q_{th} and Q_{pl} values. As shown in Figure 7.a), when having same drive strength, LS1 and LS2 start the current commutation nearly simultaneously. However, LS1 has lower Q_{pl} value, therefore its drain current commutates with higher slew rate. Upon applying the adapted gate shape on LS2, its current slew rate now matches to LS1. Consequently, the imbalance of the peak current is mitigated and the distribution of the power dissipation between LS1 and LS2 improves. At 400V, the rebalancing reduces the loss deviation from 27.7% to just 0.7%. This re-balancing does not affect the total

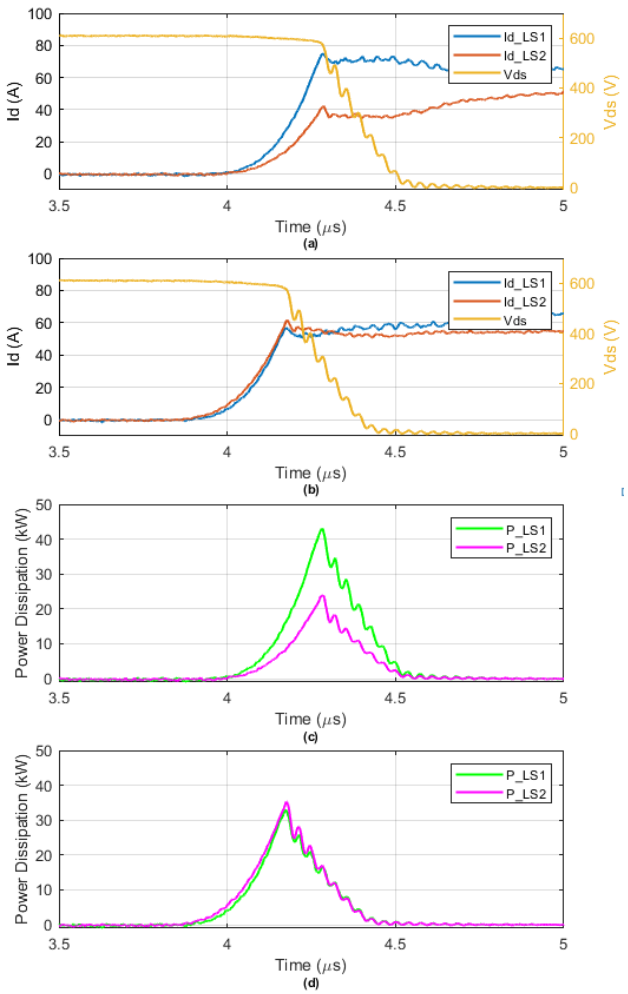

Fig. 7. Verification of the AGD at turn-on, 600V 100A. (a) Turn-on waveforms without AGD. (b) Turn-on waveforms with AGD. (c) Turn-on power dissipation without AGD. (d) Turn-on power dissipation with AGD.

switching losses, if not even reduce them, as shown in the column E_{total} of Table 4. The experiments show consistent results over two working points of 400V and 600V.

For turn-off, the unbalance is more noticeable at first. This is because of big mismatch of two MOSFETs regarding the charge amounts between their Q_{pl} and Q_{tot}. Initially, LS2 turns off much sooner than LS1. So LS1 undergoes the majority of turn-off losse. However, with the implementation of gate shaping on M2, the turn-off start- and end-times of both MOSFETs are more aligned. Consequently, the turn-off losses are balanced from 67.6% to 3% in the test with 600V V_{DC_Link}. However, it is observed that the turn-off result at 400V still exhibits some remaining imbalance, as shown Table 4. This is mostly due to the inaccuracies in gate charge measurement at each working point.

5 Outlook and Conclusions

In this work, a gate driver has been presented, which allows to balance the switching losses of paralleled SiC-

		400V 100A				600V 100A			
		E_{LS1} (mJ)	E_{LS2} (mJ)	E_{total} (mJ)	$\|\Delta E\|/E_{total}$	E_{LS1} (mJ)	E_{LS2} (mJ)	E_{total} (mJ)	$\|\Delta E\|/E_{total}$
Without AGD	Turn on	4.62	2.61	7.23	27.8%	8.83	4.62	13.45	31.3%
	Turn off	6.03	1.30	7.33	64.4%	14.02	2.71	16.73	67.6%
With AGD	Turn on	3.29	3.24	6.53	0.7%	6.45	6.91	13.36	3.42%
	Turn off	4.38	2.55	6.93	26.3%	7.22	6.80	14.02	3.0%

Table 4. Experimental result summary

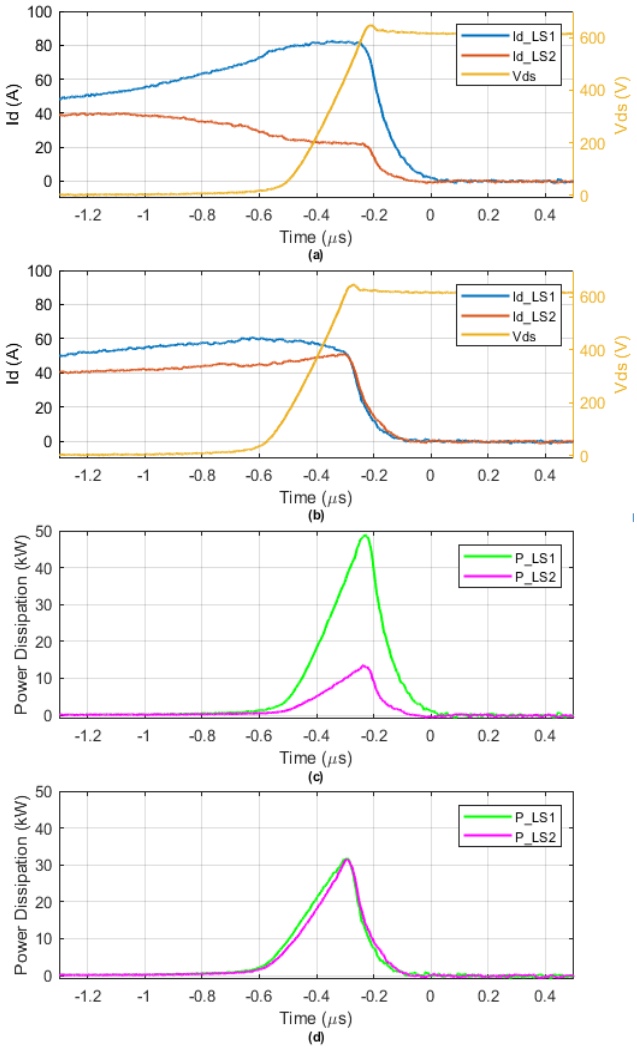

Fig. 8. Verification of the AGD at turn-off, 600V 100A. (a) Turn-off waveforms without AGD. (b) Turn- off waveforms with AGD. (c) Instantaneous turn- off power without AGD. (d) Instantaneous turn-off power with AGD.

MOSFETs. Firstly, the fundamental principles and concept behind the gate driver have been explained. Subsequently, measurement results in two different working points have been shown. The impact of the new gate drive method on switching transient waveforms and losses is assessed. The findings demonstrate the potential of the gate driver to mitigate mismatches in switching losses between paralleled MOSFETs, and slightly increase overall system efficiency.

Further investigations on the proposed AGD are necessary. Within the scope of this paper, the reference gate profile used for LS1 is a constant current profile. Exploration into gates shapes as reference profiles for M1 could offer potential reductions in overall switching losses. Besides, the measurement of gate charge characteristics can be utilized from the on-chip sensor of the same gate driver IC from Robert Bosch GmbH, instead of measuring it with off-board methods which makes the complete concept suitable for integrating into an embedded system. Finally, the gate driver should be evaluated whether it could actively control the ratio of power losses distribution, which is useful in the context of hybrid switch applications where SiC-MOSFETs are used in parallel to Si-IGBTs to reduce the overall cost of inverter applications and systems.

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