SPICE Modeling and Experimental Validation of the Active Short Circuit (ASC) Test with Silicon Carbide Power MOSFETs

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Abstract

A new SPICE model for SiC MOSFETs to be used in ASC test simulations has been developed. This model accurately reproduces the behavior of the device at extreme conditions, such as high temperature, high current, and high drain-source voltage, typical for this kind of test. The ASC test has been simulated and the results have been compared with experimental measurements to validate the methodology.

1 Introduction

New energy vehicles today play a key role in the development of resource-saving mobility and the reduction of green-house gas emissions. Three-phase traction inverters in hybrid and full electric propulsion units need to be compact, light, inexpensive, and reliable over the expected lifetime, and operate in extreme electrothermal conditions at increasingly higher power levels. In particular, overload capability requirements for power devices are becoming increasingly stringent, as in case of active short-circuit (ASC). ASC is a protection measure adopted in automotive applications to safeguard the driver and is a common abnormal mode of operation in new energy vehicles. It is referred to as “active” because it is triggered intentionally in response to certain other detected fault conditions. Testing in such condition is required because, if we consider the example of three-phase inverters in this mode of operation, as shown in Fig. 1, the motor turns into a generator: the energy stored in it before the SC causes the rise in high sinusoidal currents to be dumped, along with pulsating torque, which may introduce dangerous electrothermal stress in power devices and the whole propulsion unit. It therefore plays a key role in the protection of power circuits in the presence of overloads or short-circuits, and is used in electric traction, especially when abrupt interruptions generate dangerous back-EMF or currents capable of damaging the electric machinery or batteries [1]. During an active short-circuit, the gate voltage of the power device is held to the conduction state value (V_{GS}=18 V for SiC MOSFETs) and a very high current flows.

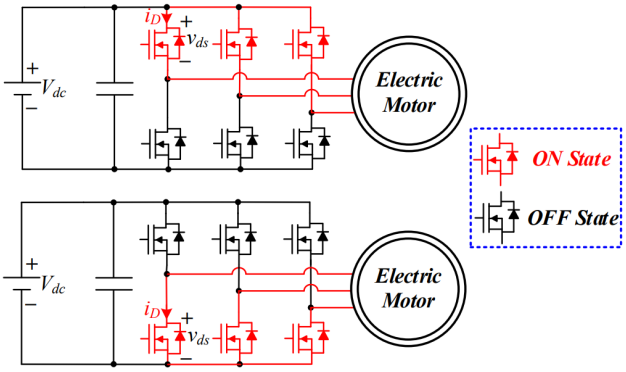

Fig. 1: Active Short Circuit in three-phase motor drive.

The associated power is naturally very high and the temperature increases, with output characteristics falling with temperature change.

2 Device modeling for ASC test simulation

The developed SPICE model includes several mathematical formulas that can accurately reproduce the behavior of the device subject to high temperature, high current, and high drain-source voltage conditions. Moreover, the model is self-heating [2], including the thermal impedance of the device reported in Fig. 2, so during any transient, the internal temperature changes and all the electrical parameters change accordingly. This model therefore allows the prediction of the internal temperature T_j of a device during any test, including ASC, through simulation, which is often very complicated or not possible experimentally.

The self-heating capabilities are obtained consider-

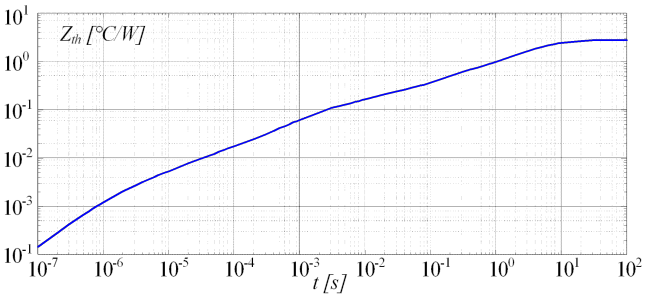

Fig. 2: Thermal impedance profile of the DUT.

ing the thermal impedance of all the layers present in the device by an electrical representation through an equivalent RC thermal network (Cauer or Foster), in which there are the T_{case} pin for the external temperature setting, and the T_j pin for evaluation of the internal temperature (Fig. 3).

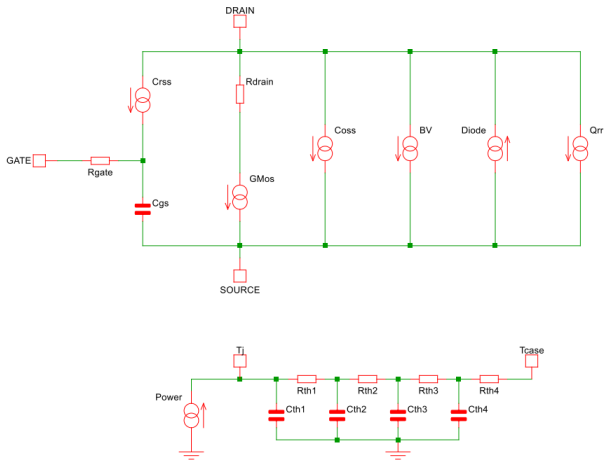

Fig. 3: Self-heating SPICE block diagram.

In the SPICE model of the device, several Gvalue components are included to reproduce the SiC MOSFET resistive contributions and to simulate the output characteristics at different temperatures. The variables used to retrieve T_j are the instantaneous power losses $P_d(t)$, the thermal impedance junction-to-case $Z_{th}(t)$, and the case temperature T_{case}.

$$T_j(t) = P_d(t) \cdot Z_{th}(t) + T_{case} \tag{1}$$

The on-state of the MOSFET is modelled by the two blocks, Rdrain and GMos, using voltage-controlled current sources, as shown in Fig. 3, whose resultant trans conductance does not exclusively depend on the temperature T_j [2].

$$R_{DSON}(T_j) = x_2 T_j^2 + x_1 T_j^2 + x_0 \tag{2}$$

$$g(u, w, T) = f(u, w, \alpha_1(T_j - T_0) + \alpha_2(T_j - T_0)^2 + \alpha_3(T_j - T_0)^3) \cdot (1 + \lambda y) \tag{3}$$

The effect of the temperature on the output current is modeled by the Eq. (2) in the linear region and by a function of the form of Eq. (3) in the saturation region, in which u and w are the V_{DS} and the V_{GS}, and T_j is the temperature. In the functions, there are second-degree and third-degree polynomials, in which the parameters x_0, x_1, x_2, α_1, α_2 and α_3 allow accurate control of the effect of the temperature on the output waveforms. A comparison between measurements and model behavior is reported in Fig. 4.

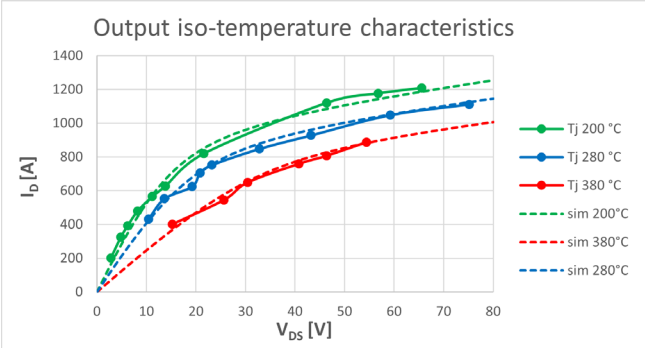

Fig. 4: Simulated and measured output iso-temperature characteristics.

3 Experimental setup

An active short-circuit test has been performed on a 750 V, 120 A SiC power MOSFETs, whose specifications are listed in table 1.

V_{BDSS} (V_{GS}=0 V)	750 V
R_{DSON}@ (V_{GS}=18 V,I_{DS}=150 A)	15.7435 mΩ (Typ) @ 200 °C
I_{DS} @ 200 °C	150 A

Tab. 1: Specification of the DUT

To perform the test, two ASC dumped sinusoidal currents with 300 A and 340 A peak, respectively, have been experimentally reproduced. Each ASC current has been approximated as the sum of two current contributions i_{R1L1C1} and i_{R2L2}, obtained by appropriately setting the RLC circuits reported in Fig. 5.

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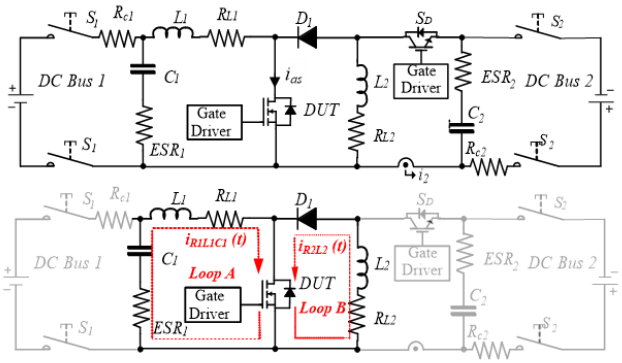

Fig. 5: Schematic of the proposed test bench for the analysis of SiC power devices.

$$i_{\text{asref}}(t) \approx i_{\text{as}}(t) = i_{\text{R1L1C1}}(t) + i_{\text{R2L2}}(t) \quad (4)$$

$$i_{\text{as}}(t) = A_1 \exp \alpha t \sin \omega t + A_2 e^{-\frac{t}{\tau}} \quad (5)$$

The ASC current transient can be approximated in the first fundamental cycles with the current generated by the test bench of Figure 5, following the steps described below. Initially, the capacitors C_1 and C_2 are charged at the voltages VC1(0) and VC2(0), respectively, by closing the two electromechanical power switches, S1 and S2. Soon after, S1 and S2 are opened. The SD switch can then be closed. A current i_2 will start to flow in the loop, including C_2 and the inductance L_2. When i_2 reaches the desired starting value of the ASC current (A2), the power device under test (DUT) is turned on, and the SD switch is turned off. The equivalent electrical circuits shown in Fig. 5 include the equivalent series resistances (ESR) of the capacitors and equivalent series resistances R_L of the inductors. The low on-state resistance of new generation of SiC allows decoupling of the two discharging loops: A and B. The RLC parameters allowing fitting to the target current have been determined and are listed in table 2. In this test bench, a 1200 V 300 A IGBT has been used as SD, and a 1000 V 150 A diode as D1. The total ASC current on the DUT is measured through a Hall effect current probe. The drain-to-source and gate-to-source voltages V_{DS} and V_{GS} are measured with high-voltage differential probes.

4 Simulation Results

In a SPICE environment, the simulation of the ASC test is performed using the schematic reported in Fig. 6, in which the pseudo-damped sinusoidal currents with 300 A and 340 A peak, coming from the measurements, are forced in the drain of the MOSFET, U1, by the current generator, I1. The device is in the on-state set by the V1 generator, while V2 defines the external temperature.

Parameters	Values
C_1	260 μV
ESR_1	5.44 mΩ
L_1	1.2 mH
R_{L1}	1.85 mΩ
C_2	3.1 mV
ESR_2	16 mΩ
L_2	3.62 mH
R_{L2}	190 mΩ
R_{D1} @ 125 °C	2.45 mΩ
ω	1790 rad/s
ω_{02}	298 rad/s

Tab. 2: Main circuit parameters.

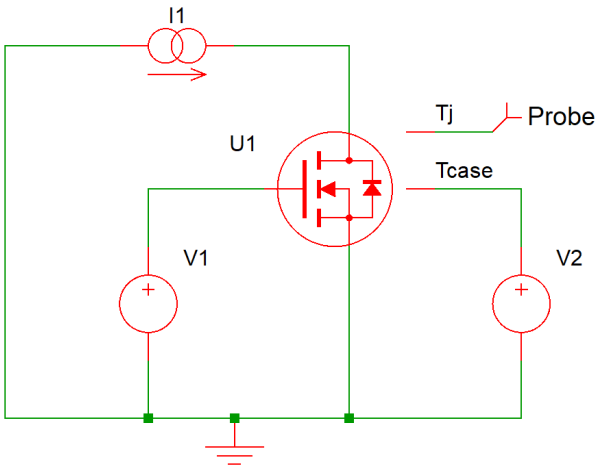

Fig. 6: Simulation schematic.

The simulated V_{DS} is compared with the measured one for each case as reported in Fig. 7 and Fig. 8. As the tested and simulated V_{DS} match very closely, we can conclude that the methodology is effective and it is therefore possible to evaluate the internal temperature using a voltage probe on the pin T_j, where 1 V represents 1 °C (Fig. 9).

5 Conclusion

Starting from the measured output iso-temperature characteristics and the thermal impedance of the device, a new SPICE model has been developed to allow the simulation of various tests at extreme conditions in terms of temperature, current, and drain-source voltage, estimating the internal temperature

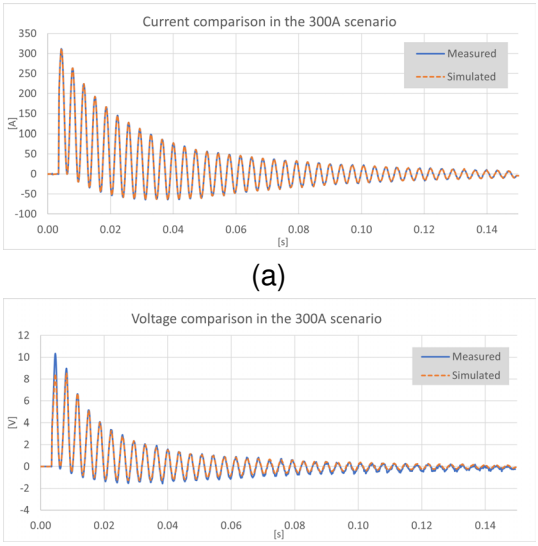

Fig. 7: Comparison of measured and simulated data at 300A.

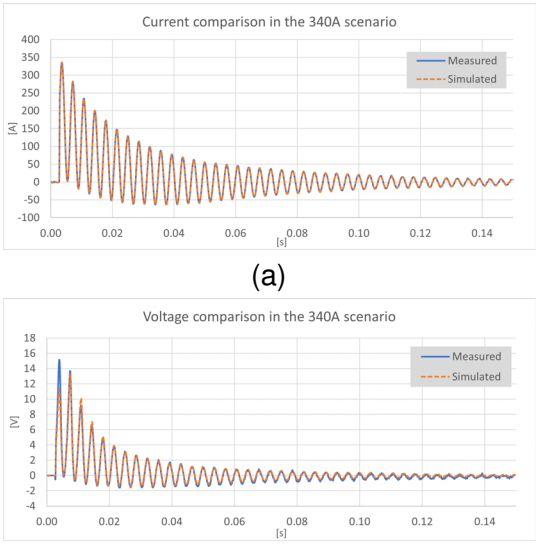

Fig. 8: Comparison of measured and simulated data at 340A.

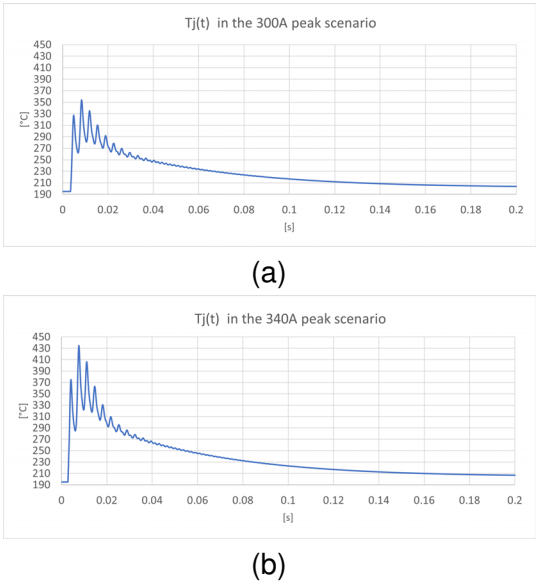

Fig. 9: Simulated temperature profiles.

and thereby evaluating whether or not the power device is able to withstand specific conditions, as well as its overall reliability [3]. The effectiveness of the methodology has been verified experimentally with a specific ASC current transient on a 750 V 150 A SiC MOSFET.

References

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