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New 15 V silicon trench MOSFET technology optimized for high frequency switching buck converters at low input voltages

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Abstract

Driven by emerging technologies such as AI, blockchain, 5G and virtual reality global servers, power consumption has increased by >250 % since 2017 [1]. In this context, a 48 V power distribution architecture has been proposed by leading tech companies [2]. This also anticipates stricter environmental regulations [3] and enables further capacity upscaling.

Infineon's newly introduced 15 V trench power MOSFET plays a key role in converting the 48 V to a CPU/GPU supply voltage level thanks to significantly improved device characteristics. This paper presents benchmark results for the discrete MOSFET generations as well as for a fully integrated power stage operating up to 2 MHz.

1 Introduction

The emerging 48 V power distribution architecture in high performance computing and data centers requires for new DCDC conversion concepts (Fig. 1). A two stage conversion approach from 48 V to a CPU/GPU supply voltage level requires discrete power MOSFETs on the 1st stage to generate the intermediate bus voltage. The 2nd stage consists of a fully integrated power stage. Instead of 48V, 54V can be used producing 6-6.75V V_{in} for the 2nd stage respectively at 8:1 voltage conversion of the first stage. We developed the new OptiMOS™ 7 15 V technology with the intention of addressing the needs of the 2nd stage in this conversion cascade as well as for direct 48:1 conversion.

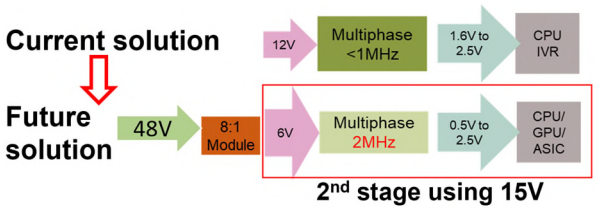

Fig. 1 Schematic diagram comparing the well established 12V power distribution architecture with the emerging 48V based rail supply showing a two stage power conversion based on a 6V intermediate bus conversion voltage

2 Device & Product Properties

The latest Infineon trench MOSFET technology node available in integrated powerstages was adapted for a 15V blocking voltage. To optimize the field plate trench (Fig. 2) for buck converters with a low 6 - 6.75 V input voltage, in particular the trench depth and drift zone were shrunk to enable a lower RonA and $FOMQ_{oss}$ (=Q_{oss} x Rds_{on}). At the same time the field plate resistance along the trenches had to be kept at a well-balanced level to allow for a fast reaction to rapid turn-on and turn-off events. This is a particular challenge in mass production due to the extremely small dimensions of low volt field plate MOSFETs.

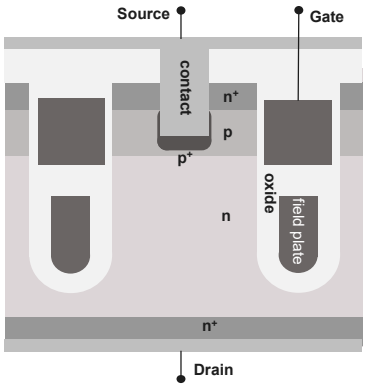

Fig. 2 Schematic cross section of the field plate trench MOSFET structure

This results in strong performance improvements for discrete 2x2 and 3.3x3.3 OptiMOS™7 products versus the previous OptiMOS™5/6 25V giving a 31% Rdson4.5 reduction, a 48% FOM_{oss} and 30% FOM_{Qg45} reduction (FOM_{Qg45} = Qg4.5 x Rds_{on}4.5) (Fig. 3)

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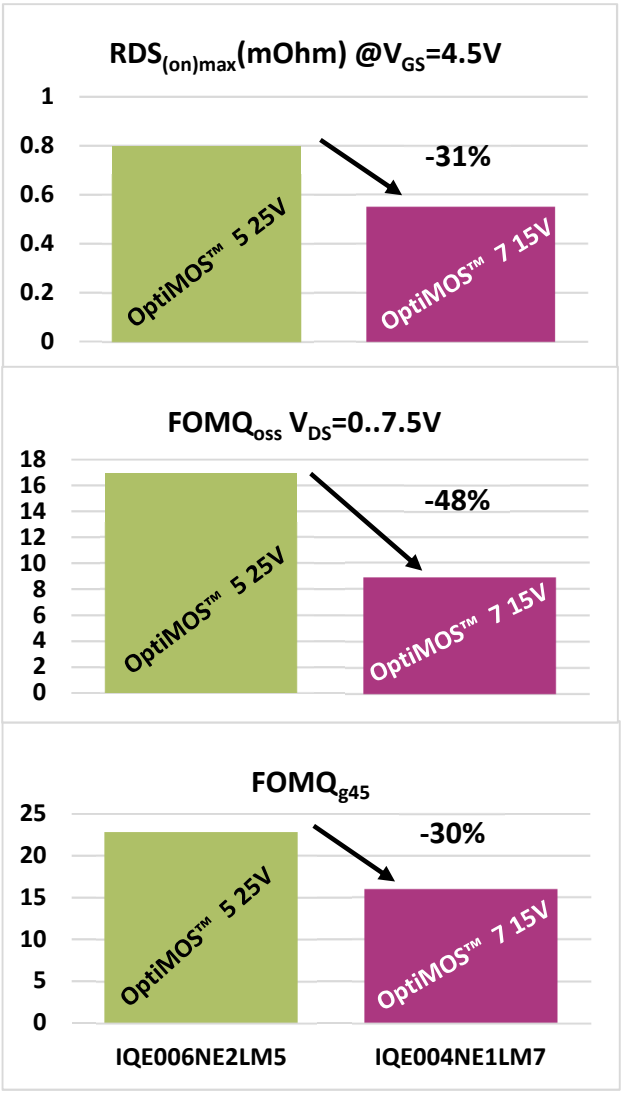

Fig. 3 Performance parameters comparison of the OptiMOS™7 15V and OptiMOS™5 25V

3 Application Results

3.1 Discrete Package Application Results

Infineon's newly introduced 15V discrete trench power MOSFET in 2x2 and 3.3x3.3 PQFN source down packages provides a leap forward in terms of performance in systems where a 25 V rated MOSFET is not required (Fig 3). The OptiMOS™7 15 V technology shows excellent ruggedness in a hard-switching environment making it the perfect choice for a fully integrated power stage.

Figure 4 shows the benchmark results in a generic synchronous buck converter test board comparing the new OptiMOS™7 15V with the OptiMOS™5/6 at a frequency of 750kHz with V_{in}=6 V and V_{out}=1.2 V. A clear improvement of the peak and full load efficiency of 0.2 % and 0.9 % respectively can be seen. Using a 2x2 PQFN package on the high side and a 3.3x3.3 PQFN source down package on the low side helps to keep the power loop short to enable fast switching and low overshoot.

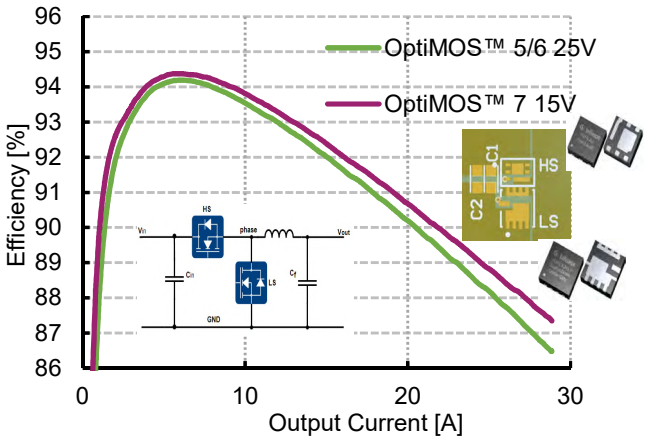

Fig. 4 Benchmarking the OptiMOS™ 7-15V OptiMOS™ 6(HS)/5(LS)-25V, synchronous buck: f=750kHz, V_{in}=6V, V_{out}=1.2V

The better high load efficiency also provides a thermal advantage leading to a lower application temperature or allowing a higher power for the same maximum rated temperature T_{max}. In addition the robustness against induced turn-on was tested for the lowest V_{th} possible from the production distribution.

3.2 Integrated Powerstage Application Results

To assess the benefit of the 15 V technology, an integrated powerstage comprising a low side, high side and driver IC in the same PQFN 5x6 package similar to OptiMOS™ powerstage TDA21570 was used. For comparison purposes just the low side was exchanged from a 25V to a 15V chip.

This low inductance package allows high switching frequencies as this is where the performance advantage of the 15 V technology is greatest. At 2.0 MHz and V_{in}=6.75 V and V_{out}=0.8 V the 15 V technology has an advantage in peak efficiency of 0.5 % whilst at high load an improvement of around 1 % was measured. (Fig. 5) The gain in peak efficiency at a high frequency of 2 Mhz is 0.1% higher than at a lower frequency of 1 Mhz (or 0.4% higher for 15V vs. 25V at 1MHz) thanks to the lower C_{oss} of the 15V technology.

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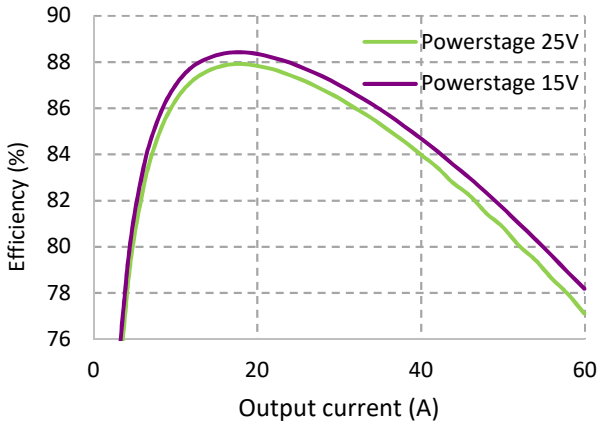

Fig. 5 Efficiency measurement on test board of integrated powerstage comparing 15V vs 25V low side from same generation, f=2.0MHz, V_{in}=6.75V, 100nH, V_{out}=0.8V

The robustness of the integrated powerstage of 15V for a higher V_{in} than 6.75V was also checked. For this the switch node voltage V_{sw} of the buck converter at low-side turnoff was measured which corresponds to the 15V low side MOSFET V_{ds} (Fig.6). The shape and value of the voltage peak was analyzed. When the V_{sw} is too high the MOSFET is clamped in avalanche and the V_{sw} peak shows a flattening rather than a clean sinusoidal shape. Up to V_{in} = 9.5V no clamping was observed. Starting with V_{in} = 10.5V the peak is flattened (marked by orange arrow) indicating that the MOSFET is in avalanche mode. This robust behavior up to 9.5V represents a good safety margin for the intended use of second stage buck converters with V_{in} = 6.75V.

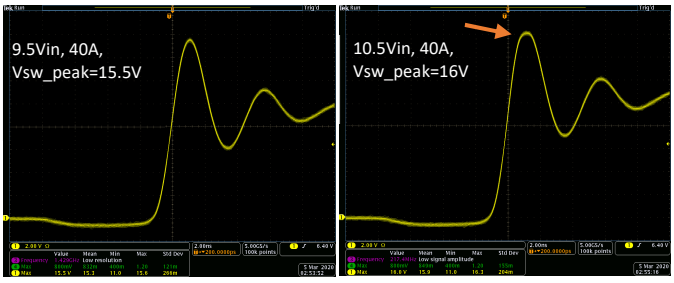

Fig. 6 Oscilloscope picture showing V_{sw} vs time for V_{in} = 9.5V and 10.5V. At V_{in} ≥ 10.5V the voltage peak shows flattening indicating a MOSFET in avalanche condition

4 Conclusion

A new Infineon 15V trench power MOSFET technology optimized for low V_{in} has been released. The efficiency increase for usage in buck converters over the whole load range for discrete 15V MOSFETs in comparison to the existing 25V technology MOSFETs has been shown. Also, the efficiency advantage of the 15V vs. the latest 25V technology in integrated buck converter powerstages has been demonstrated.

5 References

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