Accurate Characterization of the Gate Charge for SiC MOSFETs based on Double Pulse Test Scheme

Chenghui Qian[1] , Hongyao Liu[1] , Saijun Mao[1]

[1] UniSiC Technology (Shanghai) Co., Ltd., Shanghai, China

Corresponding author: Chenghui.Qian, chenghui.qian@unisic.tech
Speaker: Chenghui.Qian, chenghui.qian@unisic.tech

Abstract

The aim of this paper is to analyze the accurate gate charge characterization method of SiC MOSFETs based on the double pulse test scheme. This paper starts with four test methods for the gate charge of SiC MOFESTs including the operation principle and their influence on the obtained V_{gs}-Q_g curve. Experimental results are given to validate the theoretical analysis. By comparison, it is concluded that the double pulse test method is most suitable for the precise measurement of gate charge for SiC MOSFETs.

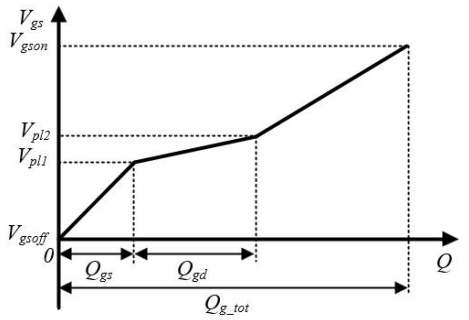
1 Introdution

The value of gate charge (Q_g) is a key parameter because it dictates the switching performance for wide band-gap power devices (such as SiC MOSFETs and GaN transistors) in high-frequency power electronics applications. It ' s important for the evaluation of the gate driver loss, switching performance etc [1].

Previous studies and standards have proposed the Q_g test methods and principles for Si devices. IEC60747-8 defines a test circuit with resistive load [2]. JESD24-2 gives the calculation for Q_{gs} and Q_{gd} [3]. In [4] and [5], three typical Q_g test circuits are provided. Also, a test method of combining two Q_g curves under lower power conditions is proposed. Besides, a simple gate charge measurement technique is given in [6] for on-wafer test. All of the test methods above are applicable to Si devices. However, the precise measurement of Q_g for SiC devices are still challenging. Compared with Si IGBT, the measurement of the gate charge for SiC MOSFET is more difficult because of its "Miller Ramp". Double pulse test method is introduced in [7]-[9] for the Q_g of SiC devices, as well as different ways of Q_{gs} and Q_{gd} extraction. Due to the lack of the detailed analysis of the different test circuits for SiC devices, no uniform test method has been developed. This paper compares four Q_g test methods for SiC MOSFETs and gives the conclusion of applicability.

2 Theory of the Measurement of the Gate Charge

Fig.1 shows four typical Q_{gs} and Q_{gd} extraction methods. The Q_{gs} extraction is similar, while the Q_{gd} extraction is quite different. Fig.1(a) shows that the charge during the "Miller Ramp" is Q_{gd}. Fig. 1(b) from JESD24-2 defines V_{pl} as the minimum slope of dV_{gs}/dt. The length between two kinking points *a* and *b* reflects the value of Q_{gd}. Fig. 1(c) from JEP192 intersects the third segment of V_{gs}-Q_g and the horizontal line that crosses V_p so that Q_{gd} is obtained. Fig. 1(d) overlays the V_{ds} waveform with the Q_g characteristic, and obtain the Q_{gd} by the limitation of V_{ds}. All the Q_{gd} extraction methods above can be applied if the V_{gs}-Q_g curve is measured correctly. Therefore, V_{gs}-Q_g curve is the key point of the measurement of Q_g.



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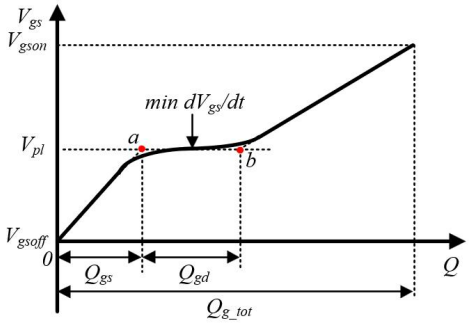

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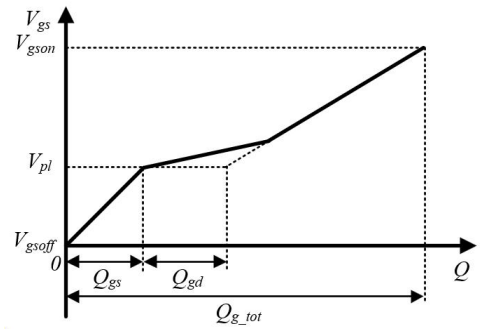

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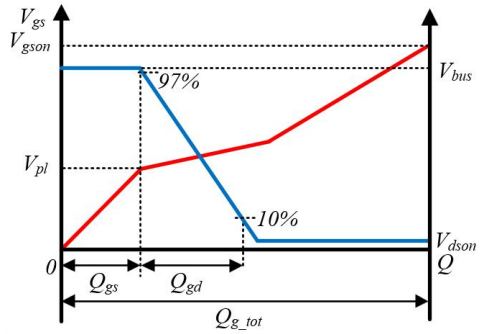


(d)

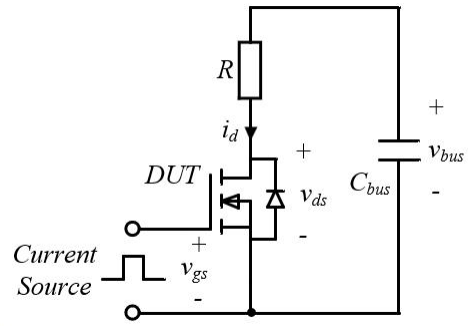
Fig. 1. Four typical V_{gs}-Q_g curve and Q_{gd} extraction methods.

The principles of the four test methods with test circuts and waveforms for SiC MOSFETs are described below. Fig. 2(a) and Fig. 2(b) show a single pulse test circuit with resistive load and waveforms. At t_1, the device under test(DUT) is drived by the current source. When vgs reaches vgsth at t_2, the drain current i_d starts increasing. Due to the resistive load, the drain-source voltage vds starts to decrease synchronously. Part of the gate current ig flows to gate-drain capacitor C_{gd}, which causes v_{gs} rising slowly. At the " Miller Ramp" during t_3-t_4, i_d remains rising until v_{ds} reaches V_{dson} at t_4. Then, the turn-on process ends at t_5 when v_{gs} reaches V_{gson} at t_5. Q_{g_tot} can be derived by

$$Q_{g\_tot} = \int_{t_1}^{t_5} i_g \, dt \qquad (1)$$

Fig. 3(a) and Fig. 3(b) provides a double pulse test circuit and waveforms of the second turn-on pulse. The entire current changing process is similar to the actual converter application. At the first pulse, the inductor is charged to the target current. At the second pulse, the inductance current i_L is commutated to the DUT at t_2-t_3. Unlike the circuit in Fig. 2, the v_{ds} voltage remains constant during the commutation process because of the freewheeling diode. All i_g current flows to the gate-source capacitor C_{gs} during t_2-t_3, which causes the v_{gs} to rise linearly. After t_3, i_d starts to rise linearly, and the rising slope depends on the value of the inductor.

Fig. 4(a) and Fig. 4(b) gives a single pulse test circuit with a high voltage and high current source meter



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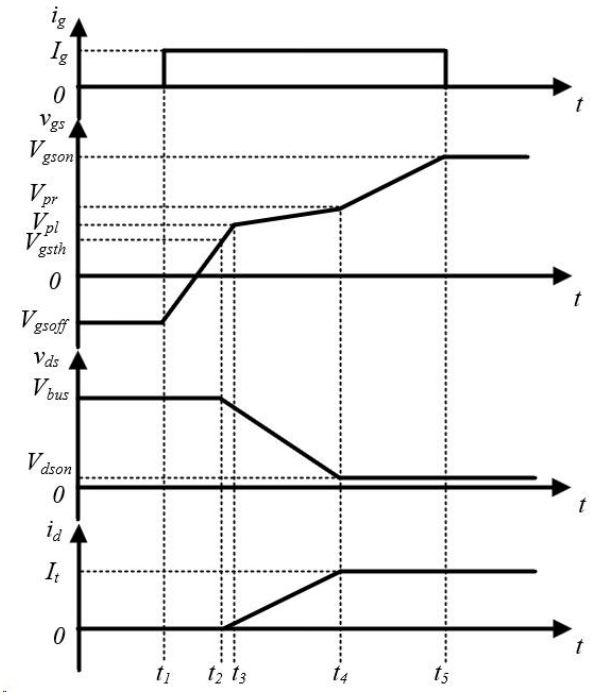

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Fig. 2. **(a)** Single pulse test circuit with resistive load. **(b)** Waveforms of i_g, v_{gs}, v_{ds} and i_d of DUT in Fig. 2(a).

unit(SMU). The gate-source capacitor starts to be charged at the rising edge of the Trigger signal. The Trigger signal is given by the SMU, which indicates the moment when the SMU begins to work in a closed loop. At t_2, i_d starts increasing and reaches the target current at t_3. The current i_d remains constant because the SMU works at constant current mode.

Fig. 5(a) and Fig. 5(b) show a test method by combining two V_{gs}-Q_g curves under different conditions. One curve is measured under high voltage and low current SMU, the other is measured under low voltage and high current SMU. Either of the test methods is similar to that in Fig. 4.

The following compares the advantages and disadvantages of the four test schemes. Single pulse test with resistive load can be easily implemented. However, the voltage drop at the resistor causes the

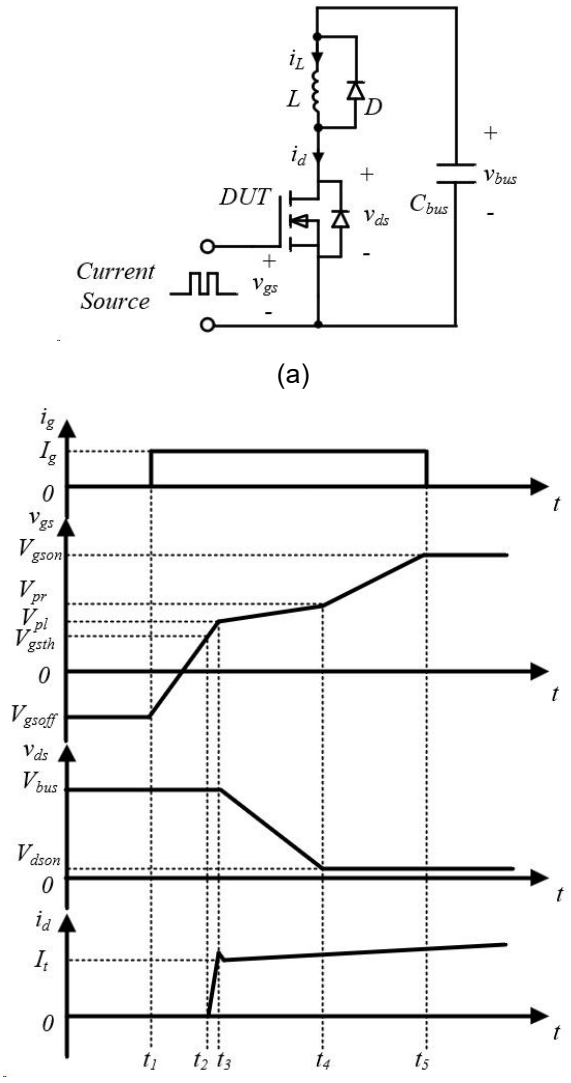


Fig. 3. **(a)** Double pulse test circuit. **(b)** Waveforms of i_g, v_{gs}, v_{ds} and i_d of DUT in Fig. 3(a).

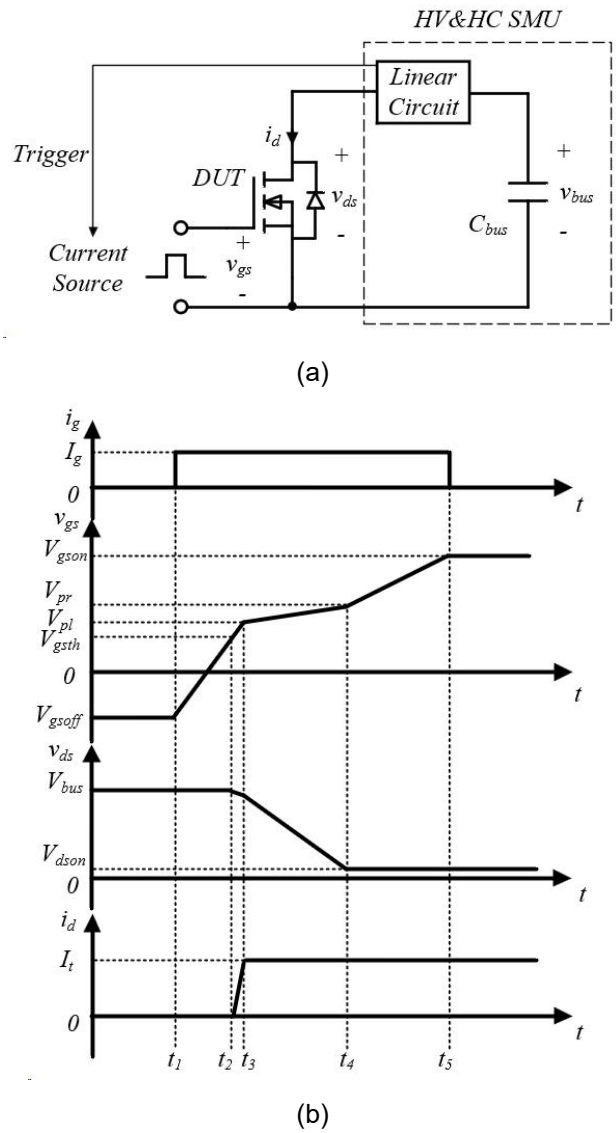
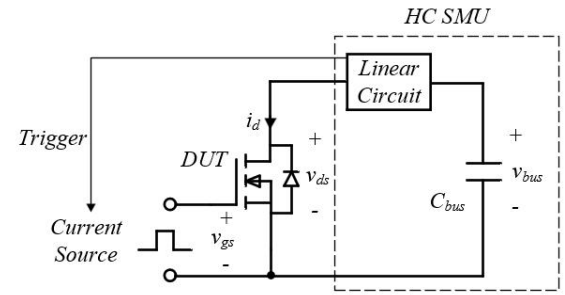


Fig. 4. **(a)** Single pulse test circuit with high voltage and high current SMU. **(b)** Waveforms of i_g, v_{gs}, v_{ds} and i_d of DUT in Fig. 4(a).

variation of v_{ds} of DUT. Also, the drain current id reaches the target value at the end of “Miller Ramp”, which results to the abnormally higher v_{gs}. This scheme requires changing resistors to achieve different target current. Stepwise regulation makes it unsuitable for a wide variety of DUTs, including discrete devices and modules, so this method is unfriendly to the test equipment design. Double pulse test is also simple to implement. It can realize accurate measurement with a high enough inductance value. Besides, the target current can be easily adjusted by changing the width of the first pulse. This method can be implemented in the existing dynamic test equipment. Single pulse test with a high voltage and high current SMU can also realize accurate measurement and adjustable target current, and its constant i_d implementation does not require large inductors. But it is difficult to develop such a high voltage and high current SMU, which is the main drawback of this scheme. Therefore, it is a potential way to be realized in static test equipment in the future. The test method with two SMUs can avoid the difficulty above, and its lower power offers better protection of the DUT. Although it is used in gate charge measurement for IGBTs, the more obvious of Drain Induced Barrier Lowering Effect (DIBL, or short-channel effect) of SiC MOSFETs causes Vgsth to increase with the decrease of vds voltage. As a result, the V_{pl} measured at low voltage and high current will be significantly higher than the V_{pl} measured at actual high voltage and high current, which makes it unsuitable for Q_g measurement of SiC MOSFETs. This problem is proved experimentally in the next section.



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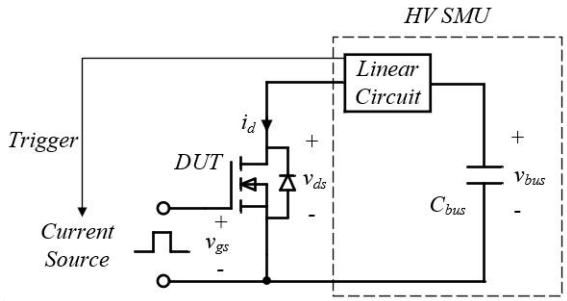

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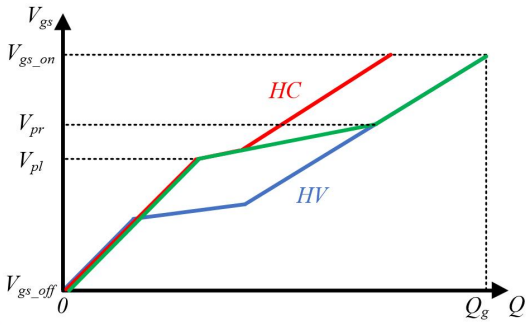


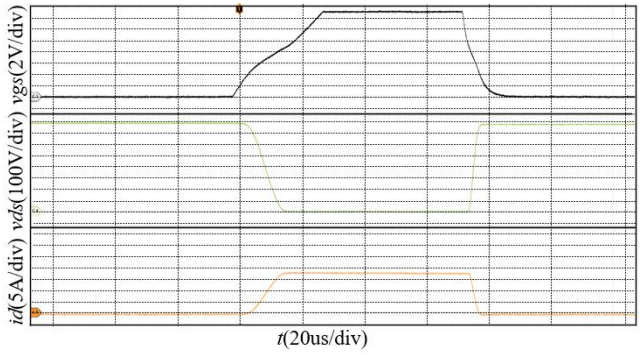
(c)

Fig. 5. **(a)** Single pulse test circuit with high current SMU. **(b)** Single pulse test circuit with high voltage SMU. **(c)** Combining high current and low voltage V_{gs}-Q_g curve and low current and high voltage V_{gs}-Q_g curve.

3 Experimental Results

To verify the effectiveness of the Q_g measurement of SiC devices, three prototypes are built. Due to the limitations of the test equipment, the test method in Fig. 4 does not perform experiment. The DUT is Infineon SiC MOSFET IMZ120R045M1 and is driven by a 1.8mA current source. The V_{gsoff} is 0V and the V_{gson} is 15V. The test condition is 800V/20A. Fig. 6(a), Fig. 6(b), Fig. 6(c) and Fig. 6(d) show the typical waveforms of the experiments, which are consistent with the above theoretical analysis.

By converting the v_{gs} waveform to the V_{gs}-Q_g curve, Fig. 7 is obtained. Obviously, it can be seen that the scheme of combining two V_{gs}-Q_g curves results in incorrect curve for SiC MOSFETs. Considering the device temperature rise, a large I_g is required. But fast



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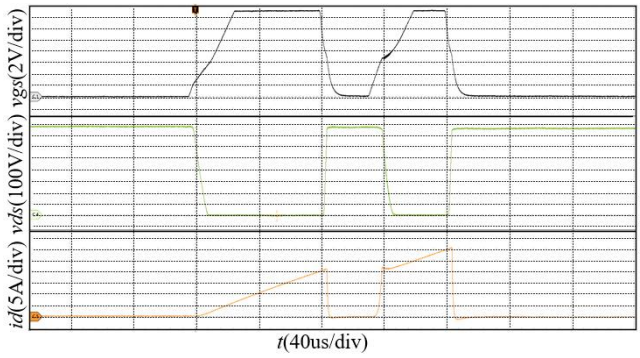

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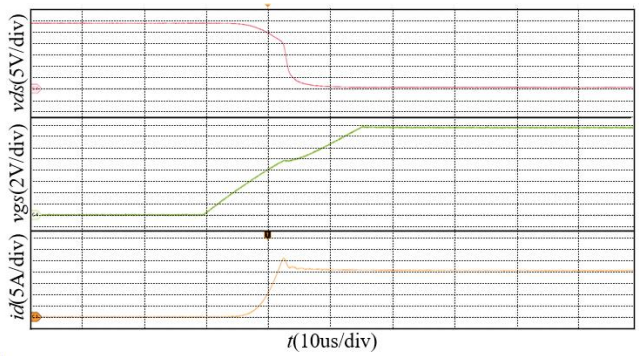

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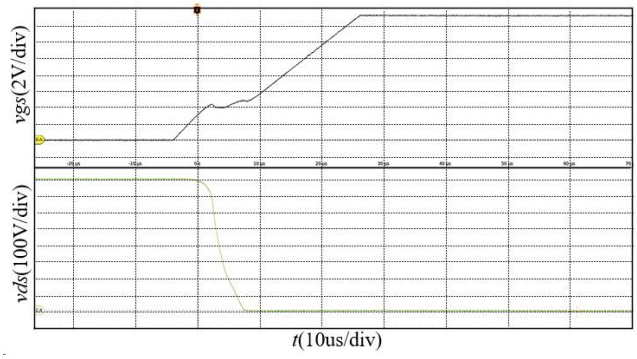

(d)

Fig. 6. **(a)** Waveforms of single pulse test with resistive load. **(b)** Waveforms of double pulse test. **(c)** Waveforms of single pulse test with high current and low voltage SMU. **(d)** Waveforms of single pulse test with high voltage and low current SMU.

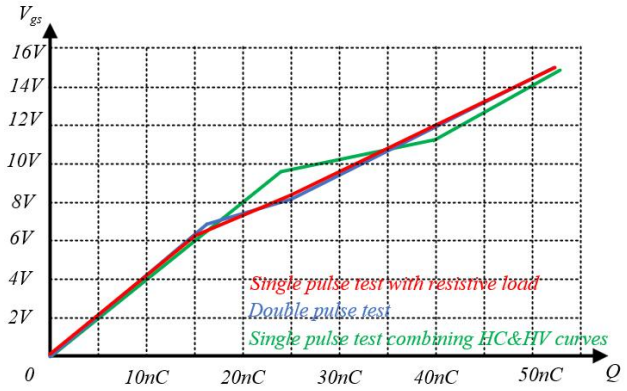

Fig. 7. V_{gs}-Q_g curves of three test methods.

switching, nonlinear v_{gs} variation and the i_d variation during “Miller Ramp” of SiC devices make it difficult to obtain V_{pl} for single pulse test with resistive load. Therefore, double pulse test is most suitable for the measurement of the gate charge for SiC MOSFETs.

4 Conclusion

In this paper, four Q_g characterization methods are compared theoretically and validated experimentally. The conclusion is that the measurement of gate charge by combining high voltage and high current V_{gs}-Q_g curves is not suitable for SiC MOSFETs. The double pulse test scheme is the most suitable for the measurement of Q_g for SiC MOSFETs.

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