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Analysis of the effect of system parasitic parameters on the switching of SIC devices

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Abstract

This paper mainly analyzes the impact of system parasitic parameters on the usage of SiC devices, and investigates the mechanism of over-current during SiC MOS switch turn-on. The reasons for turn-on current oscillation are also analyzed in this paper. In addition to the impact of parasitic inductance on the voltage stress of power devices, this paper also emphasizes the negative impact of parasitic capacitance on turn-on current stress, current oscillation, and turn-on losses in system design.

1. Introduction

Nowadays, with the maturity of SIC technology and the growth of the power electronics industry, SIC devices have become more and more familiar to engineers, from the original planar gates to the trench gates now being developed by the major semiconductor manufacturers [1,2]. This is largely due to the advantages of silicon as a wide bandwidth semiconductor, resulting in lower conduction losses. This has made it possible to productize high-voltage MOSFET and high-voltage SIC-Schottky diodes.

2. Switch on current overshoot

Conventional PN diodes have a reverse-recovery effect that is not present in the unipolar theory of Schottky structures [3], but in practice it is common to find that when current-switching occurs in SIC-MOS and SIC-Schottky diodes, the on-current overshoot of the MOSFET still resembles reverse-recovery [4,5].

2.1 Commutation Current Overshoot in SIC-Schottky Diodes

Since a Schottky diode has a Schottky barrier formed by the contact between the metal and the semiconductor, its inherent capacitance is called the Schottky junction capacitance. The capacitance of the Schottky barrier consists of two main components: the internal capacitance between the metal and the semiconductor and the capacitance of the remaining space charge in the semiconductor [6]. The Schottky barriers have certain capacitive properties, consisting mainly of the internal space capacitance between the metal and the semiconductor and the capacitance of the remaining space charge in the semiconductor. However, there are some differences between the Schottky barrier capacitance and the capacitance of an ordinary PN junction diode. The Schottky barrier capacitance is much smaller than the capacitance of an ordinary PN junction barrier. Its equivalent structure can be shown in Fig. 1.

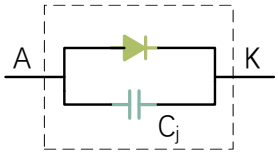

Fig. 1. Equivalent circuit diagram of Schottky diode

The theoretical Schottky diode does not have a PN junction, so there is no residual charge on the PN junction and no reverse recovery. Here, build the simulation circuit in Fig. 2 through the Spice model (IMZ120R030M1H, IDW30G120C5B) to simulate this phenomenon [7]. The simulation results are shown in Fig. 3. When the MOSFET starts to turn-on (diode turn-off), it seems that a current similar to reverse recovery can still be seen, which is mainly caused by the junction capacitance of the diode charging at the instant of current exchange, i.e., charging the junction capacitance of the diode in the lower bridge arm produces a junction current when the switch in the upper bridge arm is turned on.

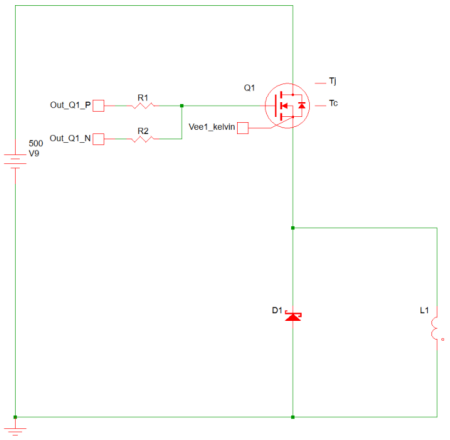

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Fig. 2. Circuit diagram of SIC-MOSFET converter simulation

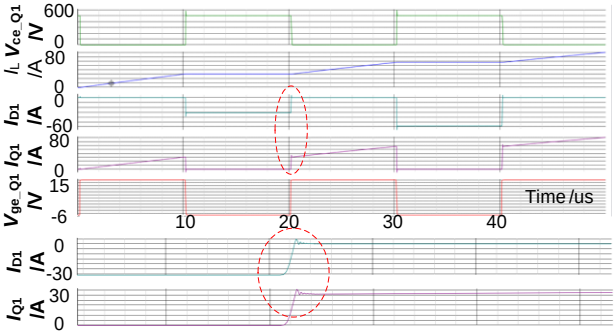

Fig. 3. SIC-MOSFET converter simulation results

The parasitic capacitance parameters of the SIC diode IDW30G120C5B are shown in Table 1 below, where it can be seen that it has a parasitic capacitance in the order of hundreds of pF (dynamic).

Table 1. Parasitic capacitance parameters of IDW30G120C5B

Parameter	Symbol	Conditions	Value	Unit
Total Capacitance	C	V_R=1V, f=1MHz	990/1980	pF
		V_R=400V, f=1MHz	70/140	
		V_R=800V, f=1MHz	55/111	

When a C_a=100pF capacitor is connected in parallel to both ends of the diode the simulation results can be seen as shown in Fig. 4 below.

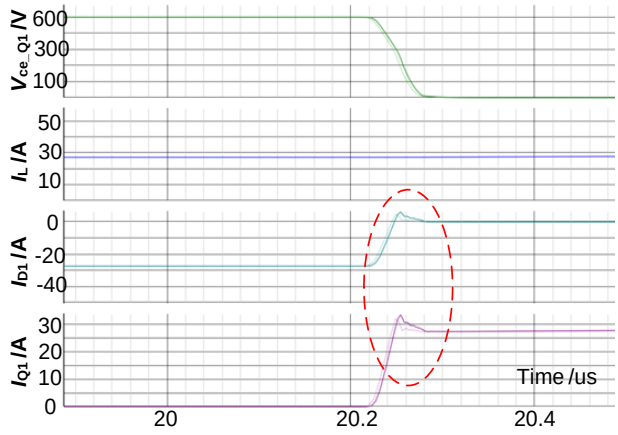

Fig. 4. The simulation results of current commutation after paralleling capacitor C_a of 100pF with the freewheeling diode

In parallel with different capacitances (none, 100pF, 200pF, 300pF) the simulation results are as shown in Fig. 5 as follows, overall it can be seen that as the diode parallel capacitance increases, the equivalent reverse recovery current increases.

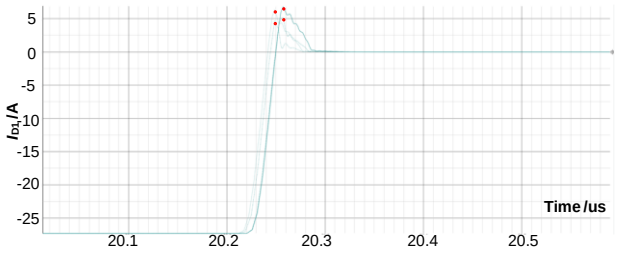

Fig. 5. Simulation results of current commutation after paralleling capacitor Ca with the freewheeling diode

The simulation data is summarized in Table 2, where it can be seen that the higher equivalent reverse recovery current leads to higher current, I_{Q1}, at the moment of turn-on of the commutation switch.

Table 2. Summary of data for the freewheeling diode with paralleling capacitance C_a

C_a(pF)	I_L(A)	I_{D1}(A)	I_{Q1}(A)	I_{Q1}- I_L(A)
/	27.3	4.68	31.98	4.68
100	27.3	5.18	32.47	5.17
200	27.3	6.27	33.61	6.31
300	27.3	6.65	33.99	6.69

When using the body diode of a SiC MOSFET in the freewheeling arm, unlike a Schottky diode, the body diode of a SiC MOSFET is a PN diode and therefore has the true reverse recovery effect of a diode, in addition to the "recovery current" characteristic caused by the charging of the parasitic capacitance. Therefore, parasitic capacitance is an important parameter when selecting SiC devices.

In summary, SiC Schottky diode theory is no reverse recovery current, but due to the existence of the capacitance (Of course, the parasitic capacitance referred to here may be the output capacitance of the diode, C_{oss}, or it may be a system parasitic capacitance, such as that of a PCB.), during the commutation of the upper and lower bridge arms, the parasitic capacitance charging current of the freewheeling bridge arm will superimpose onto the switching device, resulting in a phenomenon similar to 'reverse recovery current' effect. Therefore, it may cause two potential negative effects: ① Current stress during switch turn-on, ② switching loss increase.

2.2 SIC MOS switch turn-on current overcharge

The effect of the parasitic capacitance of the freewheeling bridge arms was discussed in the previous section. Similarly, the effect of switching bridge arm parasitic capacitance is discussed below.

The parasitic parameters of the SIC-MOS (IMZ120R030M1H), shown in Table 3 below, show

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that its output capacitance also reaches hundreds of pF (dynamic).

Table 3. Parasitic capacitance parameters of IMZ120R030M1H

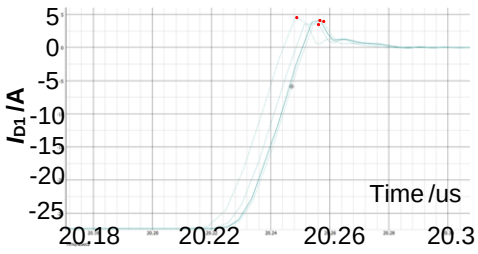
Parameter	Symbol	Conditions	Value	Unit
Input capacitance	C_{iss}	V_{DD}=800V,	2120	
Output capacitance	C_{oss}	f=1MHzV_{gs}=0V,	116	pF
Reverse capacitance	C_{rss}	V_{ac}=25mV	13	

The capacitance C_b (none, 100pF, 200pF, 300pF) is connected in parallel to the switch to equate to different parasitic capacitances. The simulation data is summarized in the following table.

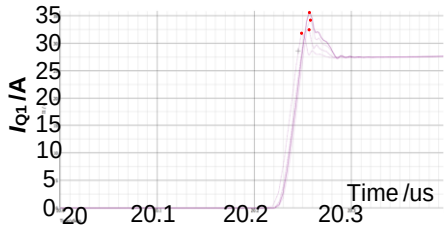
Table 4. Summary of data for the switch with paralleling capacitance C_b

C_b(pF)	I_L(A)	I_{D1}(A)	I_{Q1}(A)	I_{Q1}- I_L(A)
/	27.3	4.61	31.94	/
100	27.3	3.58	32.63	/
200	27.3	4.03	34.36	/
300	27.3	4.11	35.64	/

From Fig. 6, it can be seen that although the reverse recovery current does not have too obvious effect, the switching current I_{Q1} also tends to increase with the increase of C_b, which is mainly due to the parasitic capacitance of the MOS discharging to the channel at the on-time instant.



a. I_{D1}



b. I_{Q1}

Fig. 6. Simulation results of current commutation for the switch with paralleled capacitor C_b

As a result, the SIC MOS C_{oss} will also have two similar negative effects: ① Current stress during switch turn-on, ② switching loss increase.

3. Switching current oscillation

The previous section mainly analyzes the SIC in the use of the existence of the class "reverse recovery phenomenon" leading to the mechanism of the opening current overshoot. Fig. 7 below shows the measured waveform of a SIC MOS switch, the purple waveform is the current, and it can be seen that there is a large overcharge current at the moment of switching on, as well as a more pronounced current oscillation.

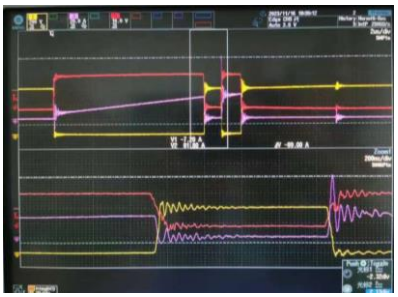


Fig. 7. Measured waveforms of SIC MOS and SIC Schottky commutator switches

The main reason here is that the stray inductance L_a of the power loop resonates with the parasitic capacitance of the loop [8], and again the reason is analyzed in the context of the simulation. The simulation circuit is shown in Fig. 8.

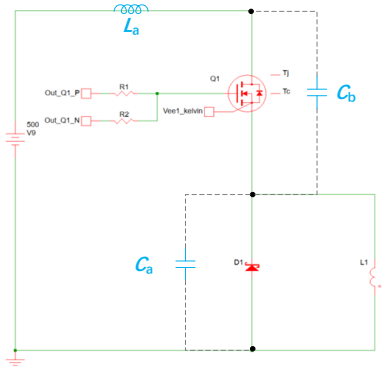


Fig. 8. Simulation of SIC MOS and SIC Schottky commutation considering system parasitic parameters

3.1 Impact of freewheeling switch (or AC/bus-) Parasitic Capacitance on Oscillation

Instead of the parasitic parameters of the main loop, the parasitic parameters of the power devices were taken into account. The typical parasitic inductance, L_q, of the TO-247 package is considered to be about 13 nH, the parasitic inductance, L_d, of the selected diode was about 6.5 nH. The C_{oss} of the MOS and the diode is shown below in Fig. 9, which varies with the voltage applied to the device.

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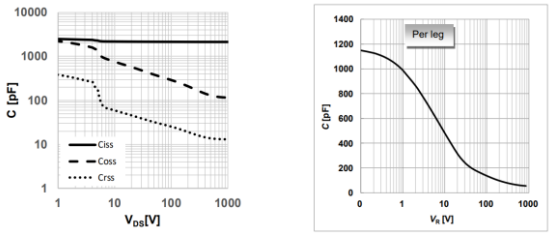
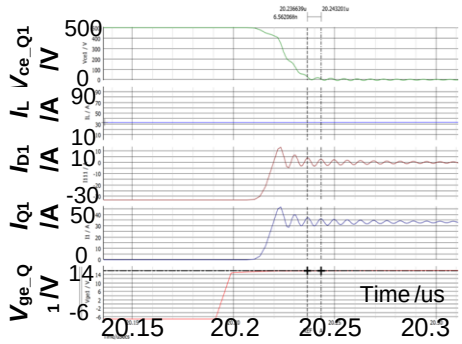


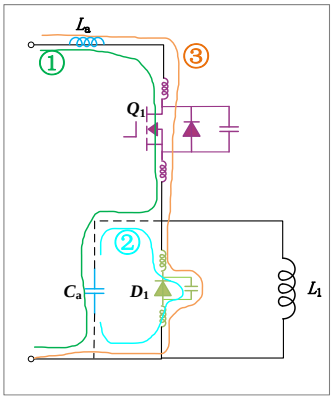
IMZ120R030M1H IDW30G120C5B

Fig. 9 Parasitic capacitance versus voltage curve

The simulation results with external C_a=none are shown in Fig. 10 below, and its current oscillation frequency at the turn-on moment is about 151 MHz.



a. Current oscillation frequency for Ca=none



b. Equivalent oscillatory loop

Fig. 10. Turn-on current oscillations when C_a is considered

The circuit oscillation loop at the turn-on moment is shown in Fig. 9b. At this instance, diode's capacitance is theoretically about 60 pF at 400~500 V. By stringing the additional stray inductance, L_a, into the main loop, and paralleling parasitic capacitance, C_a, in the freewheeling bridge arm, the simulated frequency of, I_{Q1}, was obtained with the collated computed frequency, as listed in Table 5.

Table 5. Oscillation frequency data for the freewheeling bridge arm with paralleling capacitor C_a

C_a (pF)	L_a (nH)	C_{equ} (pF)	L_{equ} (nH)	f_{sim} (kHz)	$f_{cal\text{-}loop1}$ (kHz)	$f_{cal\text{-}loop2}$ (kHz)	$f_{cal\text{-}loop3}$ (kHz)
/	/	60	13|6.5	**151**	/	/	**147**
100	/	60	13|6.5	**139**	**140**	322	147
200	/	60	13|6.5	**99**	**99**	291	147
300	/	60	13|6.5	**81**	**81**	279	147
/	15	60	15|13|6.5	**107**	/	/	**111**
100	15	60	15|13|6.5	**82**	**95**	322	111
200	15	60	15|13|6.5	**66**	**67**	291	111
300	15	60	15|13|6.5	**58**	**54**	279	111
/	30	60	30|13|6.5	**87**	/	/	**92**
100	30	60	30|13|6.5	**64**	**76**	322	92
200	30	60	30|13|6.5	**52**	**54**	291	92
300	30	60	30|13|6.5	**47**	**44**	279	92

From the results, it can be seen that when the parasitic capacitance of the system circuit is not considered and only the capacitance of the power device itself is considered, the oscillation is determined by loop3. When there is an additional parasitic capacitance C_a, then the oscillation is mainly determined by loop1.

3.2 Impact of switch (or AC/bus +) parasitic capacitance on oscillation

Similarly, analyze the effect of the parasitic capacitance of the switching bridge arm on the oscillation. The simulation circuit is as follows, with L_a in series in the main loop and the switch in parallel with the parasitic capacitance C_b, and the resonant equivalent loop is shown in Fig. 11.

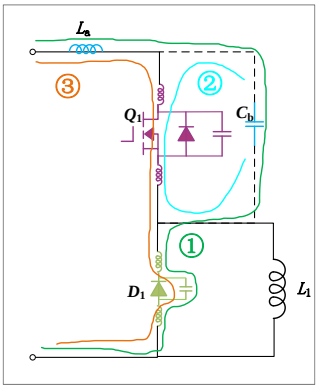


Fig. 11. Equivalent loop of turn-on current oscillation when considering C_b

According to the simulation and the equivalent oscillatory loop, the simulated frequency of I_{Q1} is obtained and the calculated frequency is organized as shown in Table 6.

Table 6. Oscillation frequency data with switching bridge arm paralleled capacitor C_b

C_b (pF)	L_a (nH)	C_{equ} (pF)	L_{equ} (nH)	f_{sim} (kHz)	$f_{cal\text{-}loop1}$ (kHz)	$f_{cal\text{-}loop2}$ (kHz)	$f_{cal\text{-}loop3}$ (kHz)
/	/	60	13|6.5	**152**	/	/	**147**
100	/	60	13|6.5	**144**	322	140	**147**
200	/	60	13|6.5	**134**	291	99	**147**
300	/	60	13|6.5	**129**	279	81	**147**
/	15	60	15|13|6.5	**108**	/	/	**111**
100	15	60	15|13|6.5	**112**	177	140	**111**
200	15	60	15|13|6.5	**116**	160	99	**111**
300	15	60	15|13|6.5	**125**	153	81	**111**
/	30	60	30|13|6.5	**87**	/	/	**92**
100	30	60	30|13|6.5	**91**	136	140	**92**
200	30	60	30|13|6.5	**91**	123	99	**92**
300	30	60	30|13|6.5	**81**	118	81	**92**

It can be seen that the resonant frequency is dominated by loop3 since the object under consideration is the current of the switch. Therefore, the SiC turn-on current oscillations are mainly the oscillations of the stray inductor and parasitic capacitance.

4. Effect of system's parasitic parameters on SiC MOS switching

The oscillations were previously analyzed to be mainly equivalent to resonance of the parasitic parameters of the power circuits, so the influence of the respective parasitic parameters on the switching performance is further analyzed here.

4.1 Effect of parasitic capacitance

Assuming that the stray inductance of the busbar is L_a=15nH, analyzing the parasitic capacitance of the continuator (or Ac and Bus-) with parasitic capacitance C_a=none, 100pF, 200pF, 300pF and R_{gon}=R_{goff}=5Ω, the simulation results are shown in Fig. 12, which shows that as the capacitance Ca increases, the frequency of oscillations decreases, and the peak value of the overcharge current increases.

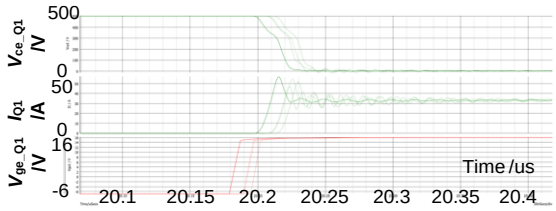


Fig. 12. Effect of parasitic capacitance, C_a, on the turn-on current oscillation**.**

The simulation results are summarized in Table 7, where the turn-on loss becomes larger and the turn-off loss decreases as the capacitance C_a increases.

Table 7. Impact of freewheeling bridge arm paralleled capacitor, C_a , on switching losses

C_a (pF)	I_L (A)	L_a (nH)	f_{sim} (kHZ)	I_{on_peak} (A)	E_{on} (uJ)	E_{off} (uJ)
/	33A	15	107	47.9A	154.2	74.3
100	33A	15	82	52.4A	167.8	57.7
200	33A	15	66	55.1A	181.6	47.1
300	33A	15	58	56.9A	190.7	43

Similarly, under L_a=15nH condition, the effect of parasitic capacitance C_b of switch (AC and Bus+) is analyzed, C_b=none, 100pF, 200pF, 300pF, R_{gon}=R_{goff}=5Ω, and the simulation results are shown in Table 8. As the capacitance C_b increases there are similar results, the turn-on loss becomes larger and the turn-off loss decreases.

Table 8. Impact of switching bridge arm paralleled capacitor, C_b, on switching losses

C_b (pF)	I_L (A)	L_a (nH)	f_{sim} (kHZ)	I_{on_peak} (A)	E_{on} (uJ)	E_{off} (uJ)
/	33A	15nH	108	47.9	154.2	74.3
100pF	33A	15nH	112	50.9	159.8	59.3
200pF	33A	15nH	116	53.3	172.1	47.7
300pF	33A	15nH	125	55.9	183.9	41.5

4.2 Effect of parasitic inductance

Under the influence of the parasitic capacitance C_a=100pF unchanged, analyzing the influence of bus stray inductance L_a=None/15nH/30nH/45nH, R_{gon}=R_{goff}=5Ω, the simulation results are shown in Fig. 13 below, it can be seen that with the increase of inductance L_a, the frequency of the oscillations decreases, the amplitude of oscillations is larger, and the speed of oscillations' attenuation [9].

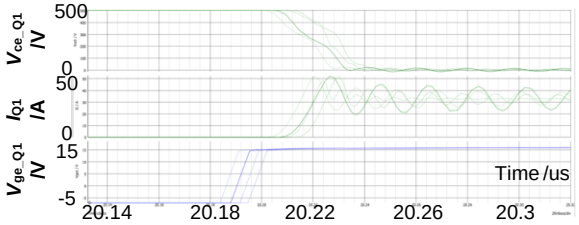


Fig. 13. Effect of parasitic inductance, L_a, on the turn-on current oscillation

Summarizing their data as shown in Table 9, the turn-on loss decreases and the turn-off loss increases as L_a increases [10].

Table 9. Effect of loop parasitic inductance, L_a, on switching losses

C_b (pF)	I_L (A)	L_a (nH)	f_{sim} (kHZ)	I_{on_peak} (A)	E_{on} (uJ)	E_{off} (uJ)
100pF	33A	/	139	49.8	193.7	50.7

100pF	33A	15nH	83	51.9	166.9	57.4
100pF	33A	30nH	64	53.5	145.3	63.3
100pF	33A	45nH	53	53.2	129.7	68.4

In summary, the extra stray inductance has a detrimental effect on the turn-off voltage spike, and the same extra parasitic capacitance increases the current spike at the turn-on moment.

From the oscillation EMI point of view, extra stray inductance is more likely to cause turn-on current oscillations, as well as turn-off voltage oscillations. The additional parasitic capacitance can significantly suppress the turn-on current oscillation.

In terms of loss, as shown in Fig. 14, extra stray inductance can reduce turn-on loss, but will increase turn-off loss; extra parasitic capacitance is favorable to reduce turn-off loss, but will increase turn-on loss.

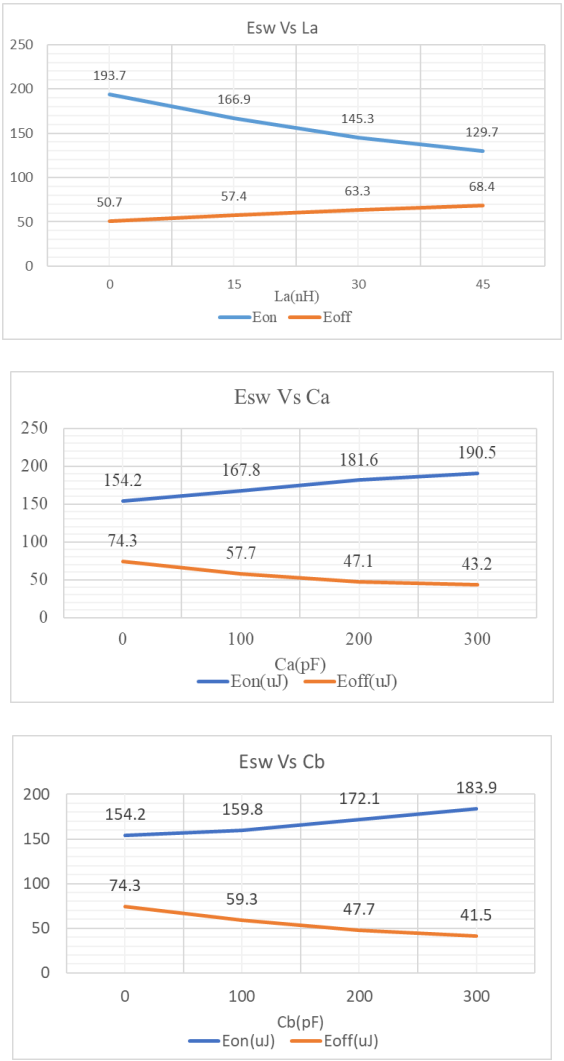


Fig. 14. Effect of parasitic inductance or capacitance on switching losses

As shown in Fig. 15, a loss curve taken from the manual for the IFX-SIC MOS IMZ120R030M1H, it can be seen that the E_{on} loss is much greater than the E_{off} loss. Therefore, it makes far more sense to reduce E_{on} than E_{off} when reducing losses. Therefore, the introduction of parasitic capacitance should be minimized in the design.

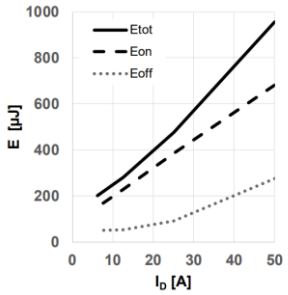


Fig. 15. IMZ120R030M1H Switching Loss Curve

5. Conclusion

This article combines simulation analysis to investigate the impact of system parasitic parameters on the switching performance of SiC devices. The study found that over-current during switch turn-on in SiC-MOS devices is caused by the discharge of switch bridge arm parasitic capacitance and charging of freewheeling diode bridge arm parasitic capacitance. High-speed switching causes turn-on current oscillation due to the resonance of parasitic inductance and capacitance in the system circuit. System parasitic inductance decreases turn-on losses but increases turn-off losses, while system parasitic capacitance has the opposite effect. To optimize efficiency, designers need to pay attention to the negative impact of parasitic capacitance on turn-on losses in SiC devices during the design phase.

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