

# Switching Behavior of a 5 kA Press-Pack IGBT for HVDC Applications

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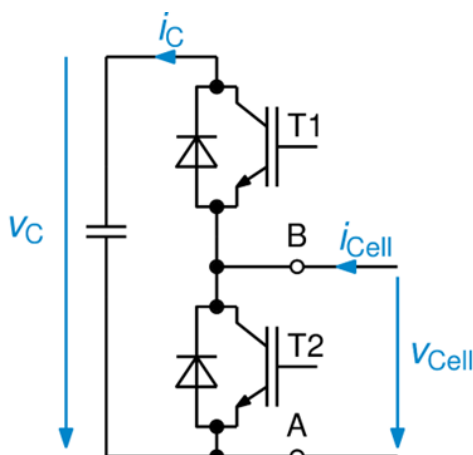
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## Abstract

Driven by renewable energy sources, the need to transmit a significant amount of energy over long distances leads to rising demand of high-voltage direct-current (HVDC) power grids. Based on this development the requirement for higher power density in insulated-gate bipolar transistors (IGBT) requires an increase in the current-carrying capability of a single package. Press-pack IGBTs (PPIs) are ideal for power-grid and premium medium-voltage-drive topologies in systems of up to  $\pm 800$  kV. Controlling and protecting these systems requires a highly reliable and robust gate-drive unit (GDU) with the ability to safely operate in the full reverse-bias safe operating area (RBSOA) including the ability to securely react to short circuit events and overvoltage situations. This work describes the efforts to achieve an optimized switching behavior using the SCALE™-2 1SP0351V GDU from Power Integrations in conjunction with the Infineon Bipolar 4.5 kV 5 kA P5000ZL45X202 PPI.

## 1 Introduction

A current topic in the field of power electronics is the need to move an immense amount of energy over long distances. This need is driven by the advance in renewable energy systems and their geographic location often far away from population centers. These challenges make HVDC transmission attractive. One of the main topologies used in HVDC power grids is the modular multilevel converter (MMC or M2C), a voltage source converter- high-voltage direct current (VSC-HVDC) topology consisting of multiple sub-modules in a series connection. An equivalent circuit of this sub-module (or cell) is the half-bridge shown in Figure 1.



**Fig. 1.** Electrical Equivalent Circuit of a Half-Bridge Cell used in the MMC Topology

The sealed press-pack housing, as well as the mechanical-short-on-fail characteristic of the PPI has led to this

package becoming increasingly popular in systems requiring rugged and robust elements. In stations of up to  $\pm 800$  kV/8 GW, a PPI with a nominal current of 3 kA is already used. In these applications a semiconductor blocking voltage of 4.5 kV is ubiquitous, but the need for higher output power has led to the development of a 5 kA PPI (i.e. shown in Figure 2), which can deliver the needed additional current density per package. [1]



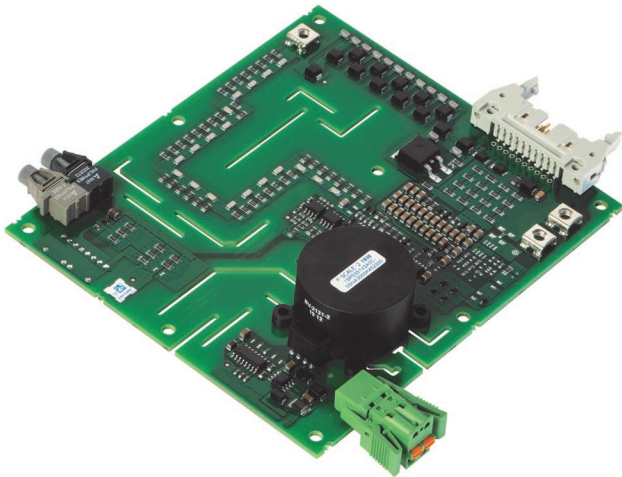
**Fig. 2.** 4.5 kV Press-Pack IGBT P5000ZL45X202

With higher power processing and localized energy in each system, the protection requirements are increasing along with additional demands on the driving and reactive capability of the GDU. Strong isolation, EMI robustness, ability to react fast to overvoltage and desaturation events, and a powerful output stage are needed to drive PPIs in this environment.

## 2 Electrical Considerations

The high gate charge of modern PPIs, coming from the paralleling of a large number of IGBTs in a single switch [2], calls for a strong output stage in the GDU. The ability to insert and extract charge quickly, to decrease

switching time (and therefore switching losses), is a valuable feature of 1SP0351V (i.e. shown in Figure 3) which uses SCALE-2 technology to achieve the necessary output power. [3] Due to the slow switching frequency in applications utilizing PPI, the continuous supply of energy to the secondary-side of the GDU is also needed to provide a stable gate voltage ( $V_{GE}$ ). To comply with isolation specifications, the 1SP0351V provides basic isolation between the primary and secondary side of the GDU. This is needed for safe operation of full RBSOA and with DC-Link voltages of up to 3600 V<sub>DC</sub>.



**Fig. 3.** High Voltage GDU 1SP0351V for Press-Pack IGBTs

The high current flow, resulting in high electromagnetic fields, calls for a GDU PCB design that is robust against EMI and which is tested and qualified according to industry standards to ensure no glitching or false triggering of signals during switching which could hinder the safe operation of the PPI. The measurement set-up needs to be configured to avoid measurement errors during the creation of the subject waveforms due to the strong fields involved.

Due to large Gate-Charges of the paralleled IGBTs the resulting Miller-Capacitance keeps the PPI conducting for a long period after the end of the input impulse. The challenge in having reliable discrimination between of real and false triggers of short circuit detection calls for a different approach compared to the usual desaturation detection technique.

### 3 Mechanical Setup

The mechanical characteristics of the complete setup must be considered. High current and the large amount of energy being converted during every switching event requires a robust DC-Link, busbar and mounting plates. The metal thickness (and needed space) must ensure low thermal stress on the used material during continuous operation and prevent catastrophic failure. The cooling of the PPI and diode during switching is also improved by the strong metal stack, with thick plates on top and bottom.

Stray inductance is minimized by using an optimized busbar and suitable connection. Due to the requirements of increasing DC-Link voltage resulting in a smaller margin for overvoltage during the turn-off switching event, the metal connection needs to utilize paralleling and overlapping wherever possible.

Currently used designs have a stray inductance of 100 to 150 nH. To ensure the best possible accuracy of the measurements for these applications, a setup with 125 nH for the complete assembly of DC-Link, busbar, diode and PPI was built to fit between those limits.

A high amount of energy is needed during the pulsing tests to ensure a stable voltage supply for the commutation cell. This requirement, together with the necessary stray inductance, called for a special setup of DC-Links. For testing purposes, a combination of two DC-Links was chosen. A smaller one with a low stray inductance and a combined capacity of 2.2 mF, in parallel with a larger one, setup as a backbone, with a combined capacity of 9.1 mF, resulting in a combined capacity of 11.3 mF.

For high peak currents and testing of up to twice nominal current a robust load was needed. During testing an air-coil with a inductance of 45  $\mu$ H was used. The special coil enabled convected air cooling and was not molded, to avoid catastrophic failures due to excessive heat when conducting more than 10 kA.

The setup used for the investigation of the PPI and adaptation of the GDU is shown in Figure 4.

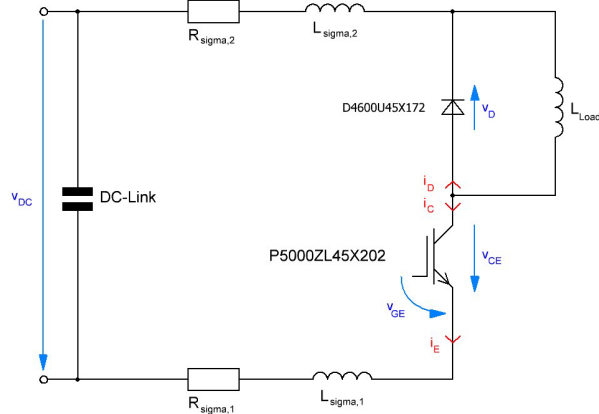


**Fig. 4.** Hardware laboratory setup for 4.5 kV Press-Pack IGBTs

### 4 Switching Characteristics

The single switch package of PPIs enables a setup for testing purposes with minimized part-count. Figure 5 shows the equivalent circuit, consisting of a 4.5 kV/5 kA PPI P5000ZL45X202 and the D4600U45X172 diode in conjunction with the GDU 1SP0351V from Power Integrations which uses SCALE-2 Technology.

On the low side, the PPI is utilized as a switch; while on the high side, the diode operating in parallel with the inductive load ensures a free-wheeling path between turn-on pulses. The stray-inductance and parasitic elements of  $R_{\text{sigma},i}$  and  $L_{\text{sigma},i}$  are shown in the connection between the DC-Link and the stack.



**Fig. 5.** Electrical Equivalent Circuit of the Investigated Setup

With the use of this setup the behavior of the PPI can be evaluated in all switching and failure situations necessary to ensure the safe and efficient operation in the end-application.

#### 4.1 Overvoltage Protection

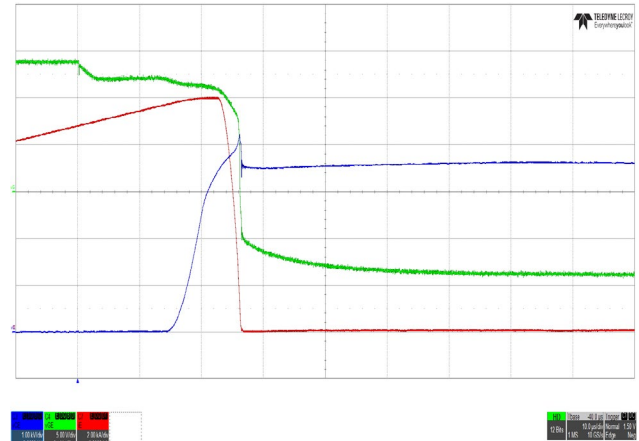
One of the basic functions of a Gate-Drive Unit is to ensure safe operation in all defined switching states. With SCALE-2 technology this includes an overvoltage protection scheme called Dynamic Advanced Active Clamping (DAAC). Active during the turn-off commutation, it prohibits the Collector-Emitter voltage from rising over a set threshold to protect both the PPI and the full system.

Turn-off commutation has been investigated for DC-Link voltages of up to  $V_{DC} = 3600$  V at a conducted current of up to twice nominal, to display the whole Reverse Bias Safe Operation Area (RBSOA) of the PPI. All waveforms were captured at room temperature.

Figure 6 shows the switching waveform with a time-base of  $10 \mu\text{s}/\text{div}$ . In the waveform, the gate-voltage provided by the GDU  $V_{GE}$  is shown in green; the IGBT voltage on the auxiliary connectors  $V_{CE}$  is shown in blue; and the Emitter current flowing into the DC-Link  $I_E$  is shown in red.

The large Miller plateau can be observed, which results in the comparatively long turn-off time of approximately  $26 \mu\text{s}$ . During commutation, a  $dv_{CE}/dt$  of  $550 \text{ V}/\mu\text{s}$  can be seen, which results in a soft switching behavior of the stack during this phase. After the voltage overshoot, a steeper negative  $dv_{CE}/dt$  of approximately  $1.7 \text{ kV}/\mu\text{s}$  occurs, which creates a large electromagnetic field. To

avoid electromagnetic coupling and to ensure safe operation in this condition, the EMI-resistant performance of the 1SP0351V is critical. The overvoltage stress dur-



**Fig. 6.** Waveform of the Turn-Off Behaviour for  $V_{DC} = 3600$  V at twice nominal current

ing turn-off reaches  $4222$  V for a short period which leaves a significant safety margin. Because of the short overvoltage peak the overvoltage protection circuit is not activated. The SCALE-2 technology of Advanced Active Clamping ensures safe operation inside the RBSOA, even in the presence of large stray inductances and high DC-Link voltages that could otherwise result in catastrophic failure.

#### 4.2 Large Gate Charge

A challenge when using PPIs designed to conduct currents of  $5 \text{ kA}$  and above is the large gate charge, coming from the high amount of IGBT chips paralleled inside the assembled Press-Pack. To switch efficiently

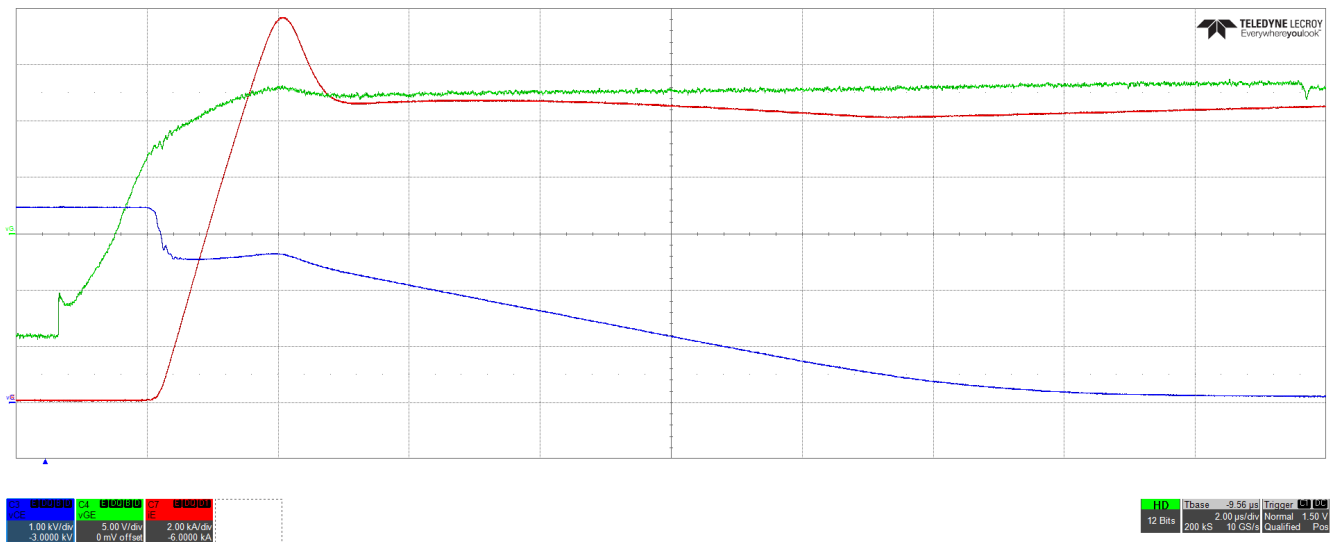


Fig. 7. Waveform of the Turn-On Behaviour for  $V_{DC} = 3600$  V into twice nominal current

and quickly and to avoid false triggering during the turn-on state transition a powerful GDU is needed. 1SP0351V provides up to 50 A of peak gate current, to ensure a fast change of switching states.

The turn-on transition for  $V_{DC} = 3600$  V and into twice nominal current can be observed in Figure 7 with a time-base of  $2 \mu\text{s}/\text{div}$ .  $V_{GE}$ ,  $V_{CE}$  and  $I_E$  are shown in the same colors as Figure 6.

During commutation the PPI saturates with a  $dv_{CE}/dt$  of  $-250 \text{ V}/\mu\text{s}$ , resulting in a turn-on time of approximately  $13 \mu\text{s}$ . The GDU is assembled with the minimum recommended turn-on gate-resistance [3] of  $1 \Omega$ . A faster transition is not achievable without abandoning the safe operation requirements.

To ensure operation without unintentional interruption due to false triggering of the short circuit detection, a new approach to detect the desaturation of the PPI is needed, which does not interfere with switching operation in standard use.

## 5 Two level Short Circuit detection

To insure safe and reliable switching of slower switching PPI's Power Integrations developed a two level detection scheme for the desaturation monitoring which is typically implemented with SCALE-2 technology. By using this technology, the short-circuit time limit [3] is respected, and uninterrupted switching can be achieved.

The critical characteristics during short circuit are the short circuit time, and the accumulated energy which result in heat inside the PPI. As long as the given thresholds are respected a catastrophic failure can be avoided.

The newly proposed scheme uses a shorter time, set to a higher detection threshold of the saturation voltage, which is adjusted to respect the given maximum short circuit energy  $E_{SC}$ . This also prevents false trigger

events during the turn-on transition, as the fall time of  $V_{CE}$  is relatively long, as shown in Figure 7.

With a second time-based detection scheme, set to a lower saturation voltage of the PPI, safe operation at lower DC-Link voltages is also ensured. For this detection scheme a longer time is allowed, as the accumulated energy inside the PPI for lower voltages does not rise above the given maximum short circuit energy  $E_{SC}$ .

By combining both schemes the defined short circuit time as well as safe operation for lower DC-Link voltages, can be achieved. A representation of the resulting waveforms is shown in Figure 8.

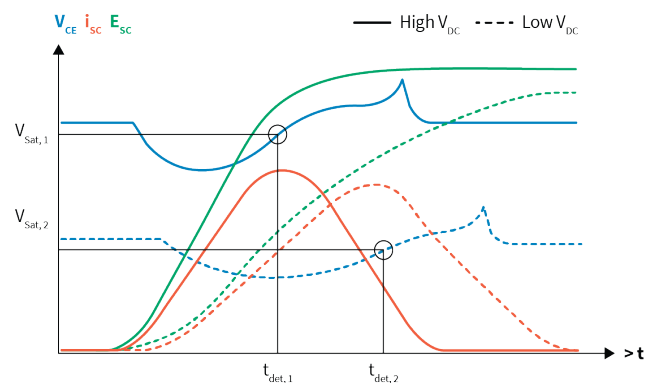


Fig. 8. Two level Short Circuit Detection

### 5.1 Short Circuit Protection

Among the tasks the GDU provides, special attention has been applied to the short circuit detection and safe turn-off of the resulting event. With the high amount of energy which can be released during the short circuit



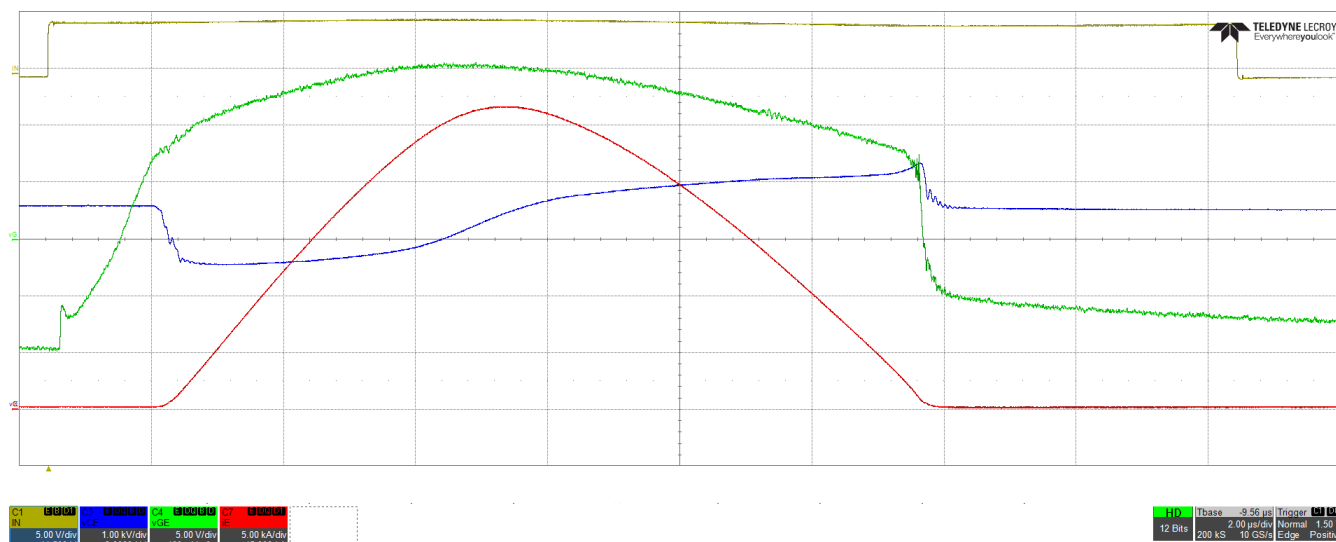


Fig. 9. Waveform of the Short Circuit Type 1 for  $V_{DC} = 3600$  V

event, the resulting catastrophic failure can potentially damage additional components inside the system, which is why robust detection and stable turn-off needs to be provided.

The behavior of the short circuit event can be observed in figure 9 for  $V_{DC} = 3600$  V with a time-base of  $2 \mu\text{s}/\text{div}$ .  $V_{GE}$ ,  $V_{CE}$  and  $i_E$  are shown in the colors used before. The input pulse of  $18 \mu\text{s}$  can be observed in yellow. The short circuit is detected with a desaturation voltage of  $V_{CE} = 2.6$  kV after approximately  $8 \mu\text{s}$ , resulting in a short-circuit time of approximately  $10.5 \mu\text{s}$  and a peak current of  $I_{SC} = 26.6$  kA. In total a short circuit energy of  $E_{SC} = 634$  J was built-up inside the PPI.

During short circuit tests, the PPI could be turned off multiple times safely without catastrophic failure or damage in any of the adjacent systems.

The resulting short circuit current shows a smooth behavior, which is another argument to enable a longer short-circuit time in favor of avoidance of false triggering during the turn-on onto twice nominal current, as the accumulated energy after the detection of the desaturation is growing slower as in other comparable IGBTs.

A stable  $V_{GE}$ , ensured by SCALE-2 gate clamping technology, avoids a steep rise of the  $di_{SC}/dt$  which can potentially lead to a positive feedback loop, resulting in catastrophic failure.

Finally Advanced Active Clamping activity can be observed during the turn-off of the short circuit, limiting the resulting overvoltage peak, and limiting the applied stress on the IGBT to ensure protection and a continued useful operation inside the system.

## 6 References

- [1] H. Wang, J. Przybilla, H. Zhang and J. Schiele, „A New Press Pack IGBT for High Reliable Applications With Short Circuit Failure Mode” in CPSS Transactions on Power Electronics and Applications, Vol. 6, No. 2, June 2021
- [2] Infineon Technologies Bipolar, “P5000ZL45X202: Press Pack IGBT” (2024), Revision 2.0
- [3] Power Integrations, “1SP0351V2xxC SCALE-2 Family: Gate Driver for 4500 V Press Pack IGBT Modules” (2023) in <https://www.power.com/design-support/data-sheets/1sp0351v2xxc-family-data-sheet> (2024-03-10)