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Experimental Analysis of 2000 V Discrete CoolSiC™ MOSFETs in TO-2474 High Creepage Packages

Sanbao Shi[1], Sekar Ajith Kumar[2]
[1] Infineon Semiconductors (Shenzhen) Company Limited, China
[2] Infineon Technologies Austria AG, Austria

Corresponding author: Sanbao Shi, simon.shi@infineon.com
Speaker: Sanbao Shi, simon.shi@infineon.com

Abstract

This paper presents the electrical performance of 2000 V discrete CoolSiC™ metal-oxide-semiconductor field-effect transistor (MOSFET) in a TO-247 4-pin, high-creepage package, installed on an evaluation board with half-bridge topology. The simulation is performed to show how the circuit's parasitic parameters and the snubber circuit influence the turn-on and turn-off behavior of the waveform. Based on the spice model of the device, this simulation was used to view and then verify the results that were obtained on the evaluation board. Finally, the optimal configuration that would reduce the turn-on and turn-off oscillation was determined.

1 Introduction

Silicon carbide devices are being used more and more frequently in power electronics systems. They not only improve the system's efficiency but also reduce the time and effort which is required for design from customers. However, as silicon carbide devices are high-speed switching devices with high $dv\,/\,dt$ and $di\,/\,dt$, they are very sensitive to the parasitic parameters of the circuit [1]. Therefore, they may encounter problems in the application, such as with waveform oscillation during the turn-on and turn-off process [2].

The authors of this article first used a simulation tool to study how parasitic parameters, such as parasitic inductance and capacitance in the main circuit, influence the dynamic switching process of the 2 kV silicon carbide device. According to the results of their study, they added different peripheral circuits such as a C snubber circuit and an RC snubber circuit on the evaluation board to test which method could be used to reduce the oscillation effectively.

2 Power Component Introduction

2.1 2000V SiC MOSFET

Infineon's CoolSiC™ trench technology [3] offers an optimized design trade-off, allowing the highest efficiency and reliability, compared to silicon carbide (SiC) planar MOSFETs.

Infineon's trench is well positioned to keep up with state-of-the-art SiC MOSFET robustness while boosting efficiency performance to new levels.

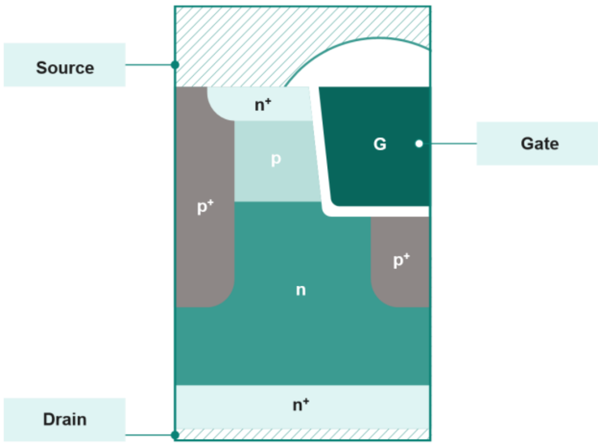

Fig. 1. Infineon's SiC folded double-trench structure

For a SiC MOSFET design, a trade-off must be found between performance on the one hand and robustness, reliability, and further application-relevant requirements on the other. Here, parameters such as static and dynamic behavior, gate oxide reliability, robustness against parasitic turn-on, and the gate-source voltage range must be considered.

The chip technology of 2 kV SiC MOSFETs investigated in this study is based on Infineon's CoolSiC™ technology. This SiC trench MOSFET concept (cell structure in Fig.1) is designed to balance low static and dynamic losses with a silicon insulate-gate bipolar transistor (Si-IGBT) such as gate oxide reliability. The higher channel conductivity of a trench MOSFET concept, as compared to a planar MOSFET design, is the main factor that enables such an optimized design with improved

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performance. This advantage of trench design results in lower electric fields in the gate oxide which limits the stress for the gate oxide.

The 2 kV technology is designed to obtain both low R_{DS}(on)*A and low failures in time (FIT) rate for cosmic ray-induced fails for systems using DC voltages up to 1.5 kV [4]. Furthermore, devices based on this technology can be operated with a virtual junction temperature up to 175°C and provide complete freedom of the gate voltage selection (e.g. maximum negative gate-source voltage down to -10 V).

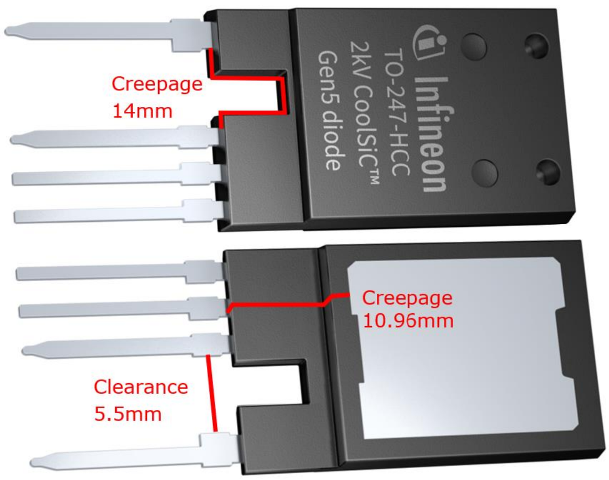

Fig. 2. 2000 V SiC MOSFET in TO-247PLUS package

2.2 Gate Driver IC

The switches are driven using EiceDriver™ X3-compact 1ED3124MC12H driver IC. The robust nature of the coreless transformer technology, combined with the 300-mil package makes, these drivers well-suited for applications that require high voltages, high frequencies, and fast switching speeds [5]. Both drivers are controlled with independent PWM signals on the connectors SIG-HS and SIG-LS, while also supporting an external XMC controller board to provide double-pulse or constant PWM signals. The driving voltage is provided by using the 12 V auxiliary supply and isolated DC/DC converters.

Fig. 3. 1ED31-X3 compact gate driver

3 Evaluation Board Design

As shown in the block diagram in Fig. 5, the evaluation board is essentially a half-bridge converter consisting of two MOSFETs, S1 and S2 [6]. Owing to the clip-based heat sink mounting and the plastic pillar on the printed circuit board (PCB), it was possible to assemble a TO-247-4 high-creepage package with sufficient creepage distance and a typical TO-247 2-pin package.

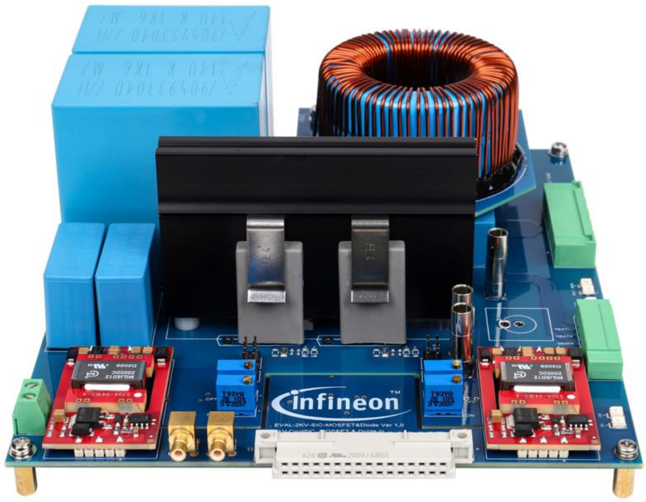

Fig. 4. Evaluation board photo

According to EN61800-5-1-2007 [7], the clearance and creepage distance are shown in Table 1.

Table. 1. Insulation distance requirement

	Distance	Condition
Clearance	5.5 mm	System voltage 1500V, Overvoltage category II
Creepage	10.43 mm	Pollution degree 2, insulation material group II, RMS voltage 1500V

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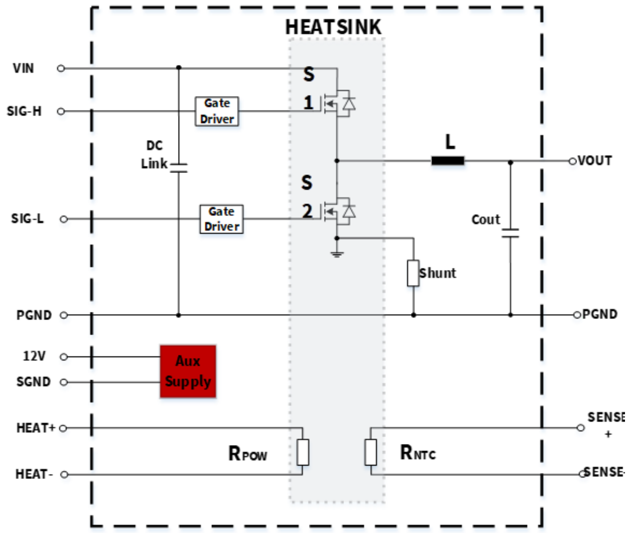

Fig. 5. Function block diagram

For versatility reasons, the evaluation board was equipped with input and output capacitors C_{in} and C_{out} as well as a load inductor L. Switching loss measurements are mainly considered while designing the input capacitor and the load inductor, and the output capacitor is required for continuous operation, for instance as a buck converter. The filter inductor provided might not meet the requirements for the latter case, but it can be easily replaced by a custom solution.

The heat sink follows the same feedback, whose dimensions and design suggest that it is unable to provide the cooling degree required for continuous operation. As opposed, it is intended to serve as a heating element related to switching loss at high temperatures. The power resistor RPOW and the thermistor RNTC can be used to adjust and monitor the heat sink temperature. Similarly, it is simple to replace the provided heat sink with a more effective one.

The gate voltage, the drain-source voltage, and the drain current must be measured using an oscilloscope to investigate the device's switching behavior. While measuring the voltage is simple, measuring the current is more challenging, especially when current slopes are high. A straightforward Surface Mounted Device shunt resistor solution is provided on this evaluation board. Although it provides an indication of the drain current waveform, there are better options to obtain accurate readings. Utilizing the Rogowski coil to measure the pin current directly is recommended from the standpoint of straightforward testing.

4 Simulation

In order evaluate the performance of the 2000 V SiC MOSFET, a double pulse simulation with SIMetrix software is done as the following figure 6, the simulation model of the SiC MOSFET could be download directly from the website [3].

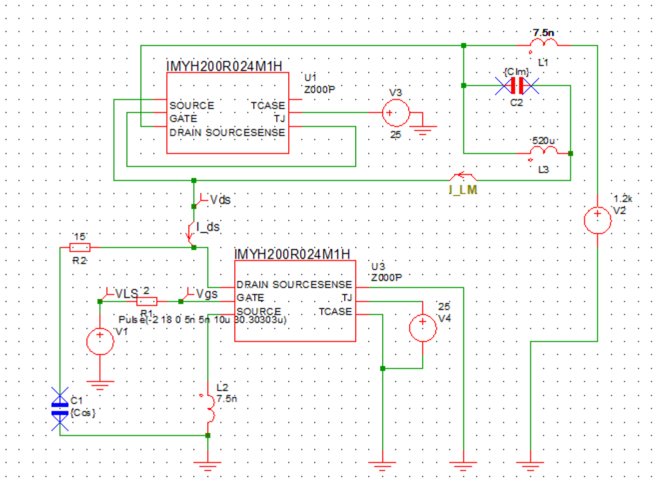

Fig. 6. Simulation schematic

To check the stray capacitance of the inductor, the different stray capacitance (1 pF, 10 pF and 20 pF) is simulated about the I_{DS} of the MOSFET U3 as the following figure 7. Which shows the stray capacitance would induce very big inrush current of the I_{DS}.

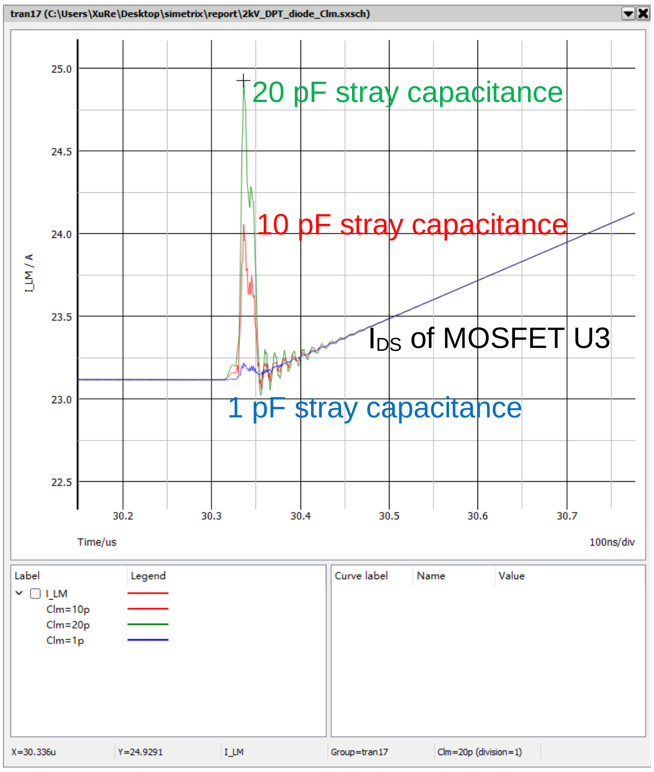

Fig. 7. Impact of stray capacitance of the inductor

On the other hand, the different snubber value is also simulated as the following figure 8. The RC snubber value is: resistor value = 15 Ohm, capacitor value from 0, 220 pF and 2.2 nF. The simulation result shows relatively increase the capacitance value could decrease the spike voltage of V_{DS} of the MOSFET.

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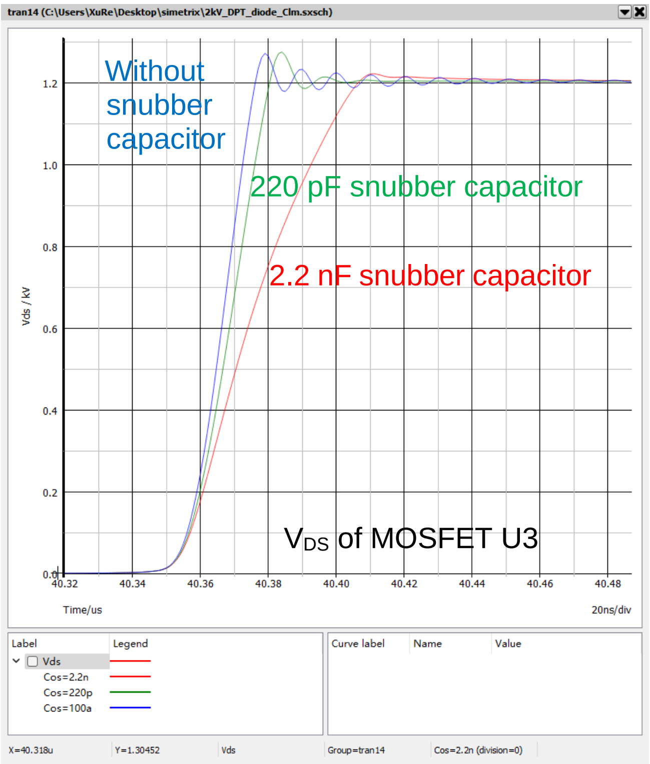

Fig. 8. Impact of different snubber value

5 Experiments

Based on the analyses above, some functional testing is done as shown below in Figure 9.

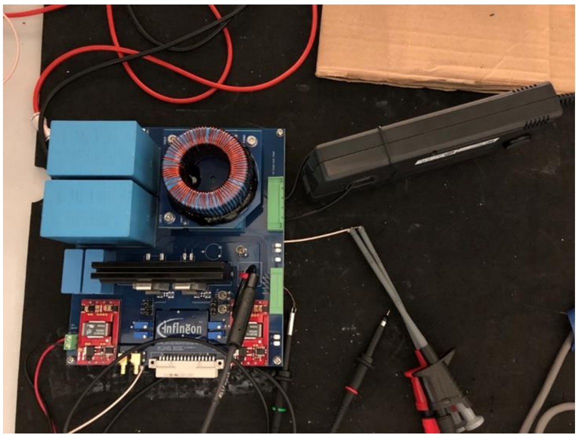

Fig. 9. Test set-up photo

With the friendly graphical user interface (GUI) as shown in the following Figure 10, the PWM duty cycle, pulse width, and dead time could be set easily.

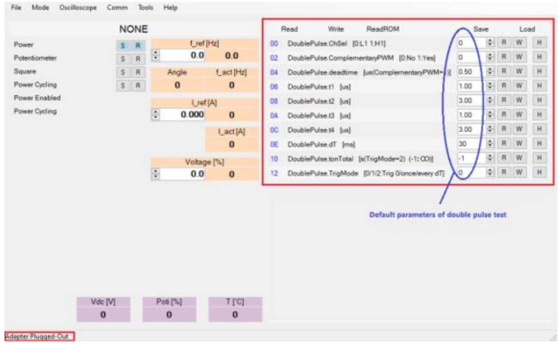

Fig. 10. Test Graphical User Interface (GUI)

Start the double pulse test through the set-up parameters in GUI, the test waveform is shown in Figure 11 as follows. There is a slight oscillation of the current waveform I_{DS}.

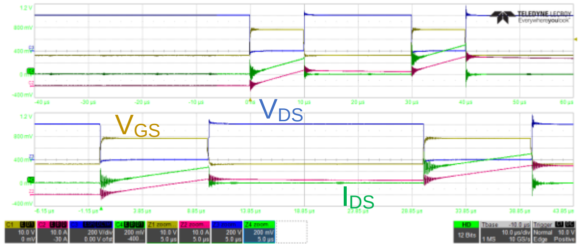

Fig. 11. Original test waveform

Change the output inductor to a coreless inductor, the stray capacitor is smaller and more suitable for high d_i / d_t application. The I_{DS} oscillation is improved as shown in Figure 12.

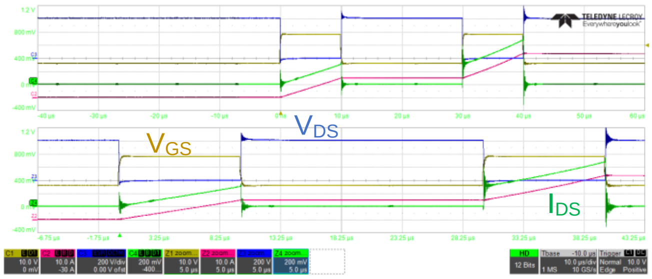

Fig. 12. Test waveform with external coreless inductor

Put the SMD 900V/250nF CeraLink™ capacitor close to SiC MOSFET, and test again, the switch on oscillation was improved due to the high frequency and high capacitance value characters of CeraLink™ capacitor [8], the waveform is shown in Figure 13.

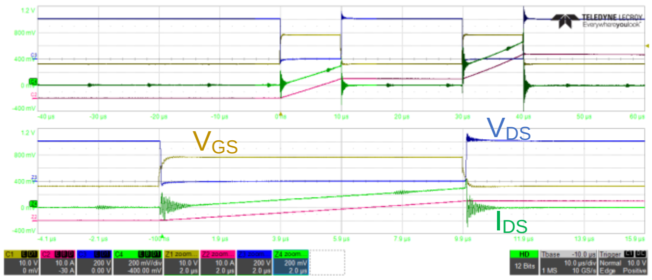

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Fig. 13. Test waveform with CeraLink™ capacitors

Change the CeraLink™ capacitor to common X7R 1000V/22nF, the test result is also very well as shown in Figure 14.

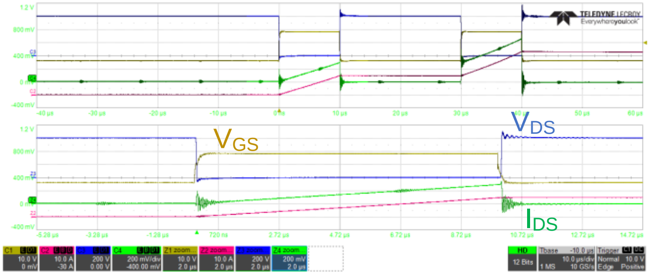

Fig. 14. Test waveform with X7R capacitors

Add RC snubber to the high side and low side SiC MOSFET, and test again, there is no special improvement as shown in Figure 15.

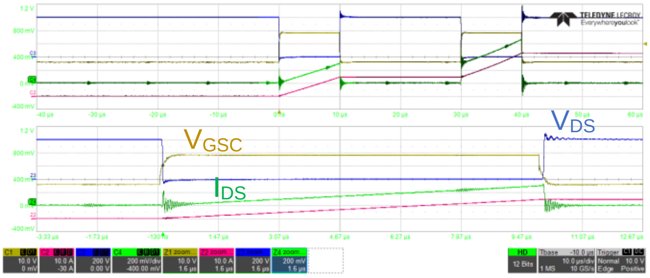

Fig. 15. Test waveform with RC snubber

6 Summary and Conclusion

This paper introduces the impact of parameters on the turn-on and turn-off waveform and discusses how to set up a suitable snubber circuit to suppress the oscillation during dynamic transients. The validity of the parameters selected is verified in the experiment.

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