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Next generation 4.5 kV IGBT StakPak module and FRD for 8GW HVDC application

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Abstract

This paper discusses Hitachi Energy's recent achievements related to next generation semiconductor devices for operation within 8 GW VSC-HVDC systems with MMC topology. For this purpose Hitachi Energy's most recent additions to its StakPak's insulated gate bipolar transistor (IGBT) press-pack platform, the 4.5 kV / 2.5 kA and 4.5 kV / 5 kA Gen-1 IGBT-only StakPak modules are presented. Furthermore, a brief description of the company's newly developed 4.5 kV fast recovery diode (FRD) platform will also be given. Finally, simulation results of the combined operation of the Gen-1 IGBT and a selected FRD will be showcased. The IGBT modules are based on Hitachi Energy's SPT++ planar IGBT technology. An improved variation of this technology (Gen-1) features 600 mV reduced V_{CEsat} compared to the reference (Gen-0) IGBT technology, boosting current capability while keeping turn-off losses unaffected. Additionally, an advanced backside technology design used in the Gen-1 IGBT reduces collector-emitter leakage current by more than 50%, enabling high temperature operation at $T_{vj(op)}$= 150°C. The technology possesses best in class reverse bias safe operating area switching capability with tests performed at T_{vj}=150°C, I_C > 2x I_{nom} (V_{CC} = 3.6 kV) on module level and excellent short circuit pulse withstand time t_p well above 10 µs (V_{CC} = 3.6 kV) as measured on submodule level. Hitachi Energy's Gen-1 IGBT combined with its FRD, which features a wide SOA and high surge current capability offers major potential for 8 GW VSC-HVDC systems, thus accelerating the transition to a green energy future.

1 Introduction

High voltage direct current transmission (HVDC) based on voltage sourced converter technology (VSC) is taking on an important role in ensuring that the energy of the future is reliable, renewable, and sustainable. VSC-HVDC allows the transfer of large amounts of electricity over long distances with high efficiency, enabling the effective integration of different energy sources into the power grid. Moreover, the technology is also used to efficiently interconnect power grids, adding stability and resilience to this infrastructure. Power semiconductors are critical components of VSC-HVDC technology. The trend towards 8 GW VSC-HVDC systems demands for more capable power semiconductors with higher current ratings, lower losses, higher operating temperature, better short circuit performance and improved reliability. Hitachi Energy is a world leader in the design and manufacture of such devices. Our continually evolving StakPak platform, based on insulated gate bipolar transistor (IGBT) and diode press-pack modules as well as our bimode IGBTs (BIGT) [1]-[5], is designed to address the unique challenges that HVDC systems face and will continue to push the limits of power ratings and performance. This cause is supported by our scalable discrete fast recovery diode (FRD) platform, which was developed with the goal to increase the ability of VSC-HVDC systems to handle high currents [3]. In this work we highlight improvements made to our IGBT technology, with respect to losses and temperature capability. Furthermore, we comment on the short circuit capability of our improved IGBT technology and briefly refer to our new FRD, showing results and simulations of combined operation of the two devices.

This paper is structured as follows. Section 2 introduces briefly the StakPak, the FRD and the VSC-HVDC system based on MMC topology. Section 3 will discuss the underlying improvements to the IGBT chip technology, setting the stage for section 4, where we will show comparative results between Gen-0 (reference) and Gen-1 (improved) technology and provide more insight into module operation of Gen-1 technology. In section 5 we will highlight some of the capabilities of the FRD and show combined Gen-1 and FRD measurements. Lastly, in section 6 we will show a VSC-HVDC system simulation with our Gen-1 5 kA IGBT-only module combined with our 5 kA FRD.

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2 Devices and application

2.1 4.5 kV IGBT-only StakPak

Fig. 1: 4.5 kV IGBT-only StakPak: submodule, 2.5 kA module, 5 kA module

The StakPak, a press-pack type power module developed specially for HVDC applications, has extensive field installation receiving excellent feedback. StakPak modules are optimized for assembly in a stack, allowing for more efficient system design, minimizing stray inductance, and enabling uniform current sharing among chips and submodules. In this work we focus on our newly developed StakPak modules featuring only IGBTs (IGBT-only) rated at 4.5 kV / 2.5 kA and 4.5 kV / 5 kA, consisting of three and six submodules respectively. The submodules are placed in a sturdy, high temperature capable frame. A submodule consists of IGBT chips soldered to a baseplate on which a housing is mounted. Completing the submodule is a spring package, which is laid into the housing for reliable contact as seen in Fig. 1. Once pressed within the stack, the spring package ensures that each chip is well contacted [2]. The modular nature of the StakPak allows scaling of the current by varying the number of submodules within a module frame. Hence, apart from modules with three and six submodules, devices with four and five submodules resulting in current ratings of 3300 A and 4000 A respectively could also be produced within the same footprint [1], [2].

2.2 4.5 kV fast recovery diode

Fig. 2: 4.5 kV FRD with 110, 119 and 143 mm pole piece diameter.

For use within VSC-HVDC systems the IGBT-only StakPak module can be complemented with one of Hitachi Energy's newly developed discrete FRD's. The devices contain diode wafers with active area ranging from 90 to 140 cm^2 in a hermetically sealed housing. Pole piece diameters of the housing can either be 110, 119 or 143 mm, and the corresponding devices are referred to as PP110, PP119 and PP143 respectively. The use of one of Hitachi Energy's new discrete FRD's in an HVDC system brings the advantage, that the StakPak can be fully populated with IGBT's, increasing current capability as high as 5 kA to date. Additionally, systems benefit from an increased robustness, a wide safe operating area (SOA) and strongly improved surge current I_{FSM} capability [1], [3].

2.3 VSC-HVDC modular multilevel converter

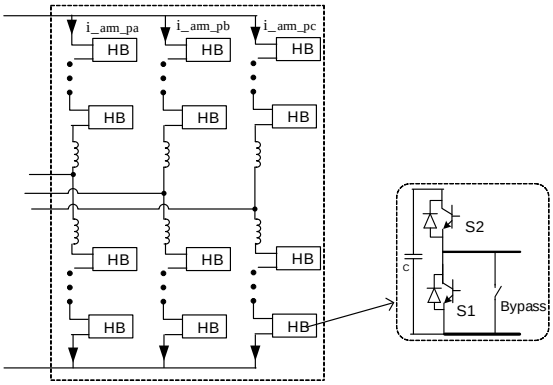

Fig 3: Schematic of modular multilevel converter used for VSC-HVDC applications.

VSC-HVDC applications predominantly utilize a half-bridge (HB) cell based modular multi-level converter (MMC) as shown in Fig. 3. Each cell may consist of two IGBT switches S1 and S2 with an anti-parallel diode each, connected in parallel with a capacitor. Parallel to S1, a mechanical bypass is installed to carry the phase current when S1 fails [2]. In a point-to-point HVDC system, typically one converter operates as rectifier and the other converter operates as inverter. In wind power integration, the offshore converter is a rectifier, and the onshore converter is an inverter. In HVDC interconnectors, the power direction may be changed at any time. Due to the high number of cells in an arm of the MMC, the switching frequency of the semiconductors is, typically between 1 to 3 times the fundamental frequency. This means that most of the losses occur during on-state. As we will show in the following sections, our Gen-1 based IGBT-only StakPak device features very low on-state V_{Cesat} holding significant potential to lower converter loss [2]. Furthermore, our IGBT-only and FRD designs aimed at high temperature operation can contribute to increasing the output power of HVDC systems, due to reduction in cooling power needed. Our device improvements in respect to SOA and the strong I_{FSM} performance of our discrete diodes [3] will also contribute to the overall safety of the systems.

3 Improved IGBT Chip technology

The reference chip technology used in this work is based on Hitachi Energy's enhanced planar cell concept described in [6]. This baseline chip design is then further optimized for lower on-state losses by enhancing the injection efficiency of the backside collector and

incorporating higher channel density as required for high current capability [2],[6]. Higher injection efficiency would have also resulted in an increase in the collector-emitter leakage current. However, our new chip also features advanced backside technology which not only lowers the sensitivity of collector leakage with respect to its injection efficiency but also helps in reducing the overall leakage current allowing higher temperature operations. The Gen-1 chip also features improved (shorter) termination design resulting in more available active area for a given chip size further strengthening its current capability. Furthermore, the improved termination design allowed us to reduce the thickness of the Si drift region which led to improvement in overall technology trade-off (E_{off} vs V_{CEsat} curve) as compared to the Gen-0 chip [2].

4 Results and discussion

4.1 Gen-1 vs. Gen-0 comparison

4.1.1 General remarks

Subsection 4.1 presents the improvements achieved by implementing the chip optimizations mentioned in the previous section. Data was mostly obtained through submodule level measurements, however, unless stated otherwise, we show results scaled to 5 kA module level. The Gen-0 and Gen-1 comparison was performed under the same conditions for all tested devices mostly at junction temperature T_{vj}=125°C. Information detailing the test setup, which is comparable for submodules and modules, will be given later in section 4.2.

4.1.2 On-state and technology curve

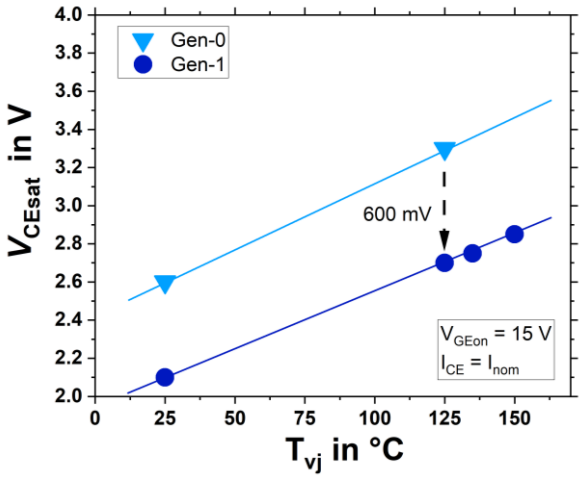

Fig. 4: Saturation voltage improvement of Gen-0 and Gen-1 compared at different temperatures at nominal current.

Measured results showed significant improvement during on-state of our optimized chip compared to reference. Figure 4 depicts the collector-emitter saturation voltage V_{CEsat} for Gen-0 and Gen-1 chip technology at nominal current I_C=5000 A, gate voltage V_{GE}=15 V and temperatures T_{vj}=25°C and 125°C. At T_{vj}=125°C the V_{CEsat} of the new generation device lies 600 mV below the reference technology. Gen-1 devices were further tested at T_{vj}=135°C and 150°C, also seen in Fig. 1. with V_{CEsat} below 3 V at all temperatures [2]. Lowering the V_{CEsat} of a bipolar device causes an increase in its turn-off switching losses. However, by incorporating a higher channel density and thinning the Si drift region of the Gen-1 chip technology, as mentioned in section 3, adverse effects on E_{off} were avoided. Consequently, the Gen-1 technology trade-off curve moves to a superior position as shown in Fig. 5 for conditions T_{vj}=125°C, V_{CC}=2800 V and nominal current I_C=2500 A [2].

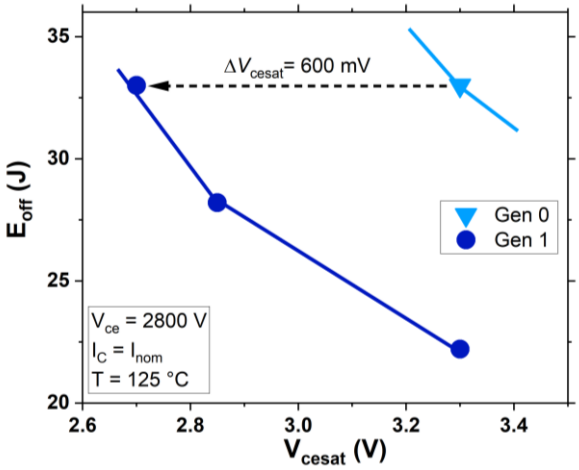

Fig. 5: Technology trade-off curve improvement from Gen-0 to Gen-1 technology at T_{vj}=125°C, nominal current I_C=5000 A, and V_{CC}=2800 V, scaled from submodule to module level.

4.1.3 Turn-on switching losses

The higher channel density design used for Gen-1 technology also affect the turn-on losses E_{on} of the new chip generation, reducing E_{on} close to 40% compared to Gen-0 at T_{vj}=125°C and V_{CC}=2800 V [1], [2].

4.1.4 Collector-emitter leakage current

Our new generation chip technology features strongly improved collector-emitter leakage current I_{CES} as seen in Fig. 6, significantly reducing the risk of thermal runaway. To measure I_{CES}, the gate and the emitter of the tested devices were shorted and V_{CE}=2800 V, 3400 V and 4500 V were applied for a pulse time t_p=100 ms each. I_{CES} reductions from Gen-0 to Gen-1 are well above 50% for T_{vj}=125°C for all measured voltages with Gen-1 collector-emitter leakage around 24 mA at rated blocking voltage V_{CE}=4500 V, allowing us to raise the operating junction temperature $T_{vj(op)}$ to 150 °C [2].

Figure 6 also shows measurements of Gen-1 single chip at T_{vj}=150°C with and without the advanced backside process and design mentioned previously, with I_{CES} reduced by over 60% at rated blocking voltage V_{CE}=4500 V [2].

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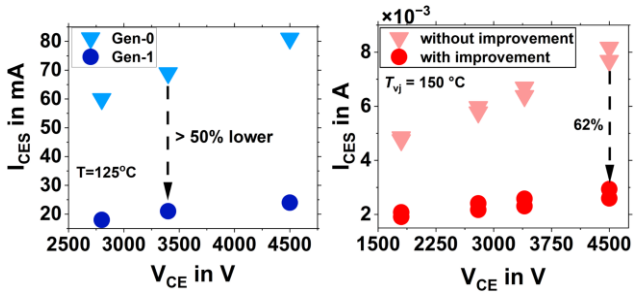

Fig. 6: Left: Collector-emitter leakage current for different V_{CE} and T_{vj}=125°C for Gen-0 and Gen-1 IGBT-only technology, scaled to module level. Right: Chip level collector-emitter leakage current versus different blocking voltages V_{CE} for Gen-1 chip with and without improved backside design at T_{vj}=150°C.

4.2 Gen-1 4.5 kV / 2.5 kV high temperature operation

4.2.1 Measured devices

Subsection 4.2 presents results from 4.5 kV / 2.5 kA Gen-1 IGBT-only StakPak module measurements.

4.2.2 On-state characteristics

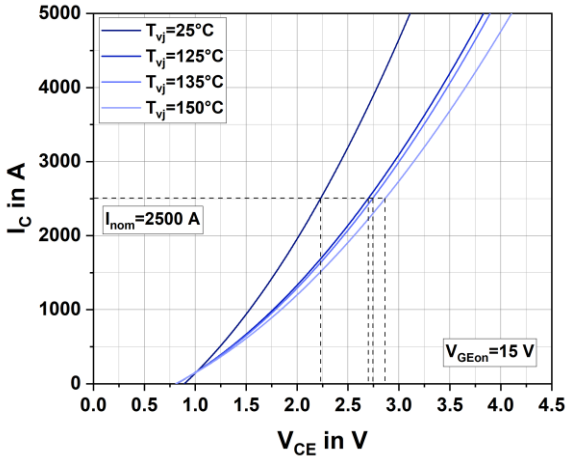

Fig. 7: On-state characteristics for Gen-1 based 4.5 kV / 2.5 kA IGBT-only module at different temperatures and V_{GEon}=15 V.

The on-state characteristics were obtained by pushing currents from I_C=100 A up to 2x I_{nom}=5 kA through the device at temperatures T_{vj}=25°C, 125°C, 135°C and 150°C with V_{GE}=15 V (see Fig. 7). The characteristics show positive temperature coefficient of resistivity and for nominal current I_C=2500 A, the saturation voltage V_{CEsat} is lower than 3 V [2].

4.2.3 Switching losses

To measure switching losses the standard double pulse test with an inductive load was used, with devices arranged in a phase-leg configuration and the Gen-1 IGBT-only module being used as the bottom switch. For the top switch we used an adapted version of Hitachi Energy's 5SNA 2000K450300 [11] featuring increased diode area. The measurement circuit comprised a DC-Link capacitor $C_{DC\text{-}Link}$=2.1 mF and a set of variable load inductances with a total stray inductance of L_σ=160 nH. A programmable gate drive unit was used to control the gate. Moreover, an external gate capacitor C_{GE}=330 nF was added close to the gate of the IGBT-only StakPak module.

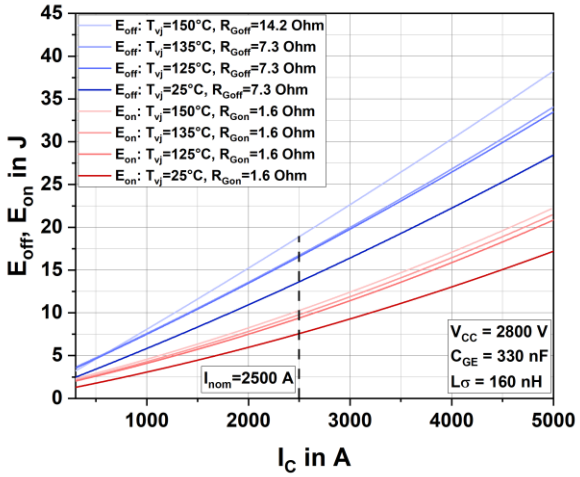

Fig. 8: IGBT turn-on and turn-off switching characteristics versus collector current I_C for Gen-1 based 4.5 kV / 2.5 kA IGBT-only module at different temperatures. V_{CC}=2800 V and L_σ=160 nH.

The current dependent dynamic switching losses at T_{vj}=25°C, 125°C, 135°C and 150°C are shown in Fig. 8, where I_C is swept from a few hundred ampere to 2x I_{nom}=5 kA, with V_{GEon}=15 V and V_{GEoff}=-15 V. At T_{vj}=150°C a gate resistor R_{Goff}=14.2 Ω was used. As for the remaining temperatures we chose R_{Goff}=7.3 Ω. This change in gate-driving is a consequence of a trade-off between losses and reverse bias safe operating area (RBSOA) capability as described in a later section of this paper. The turn-on gate resistor was chosen to be R_{Gon}=1.6 Ω.

Turn-off switching losses E_{off} of the new IGBT-only 2.5 kA StakPak module at nominal conditions V_{CC}=2800 V and I_C=2500 A fall below 20 J for all temperatures and IGBT turn-on losses E_{on} at the same conditions lie slightly above 10 J as seen in Fig. 8. Turn-on switching losses vary with the choice of freewheeling diode and will grow with increasing diode area. The switching losses characteristics with respect to gate resistor at otherwise same conditions as in Fig. 8 are shown in Fig.9 [2].

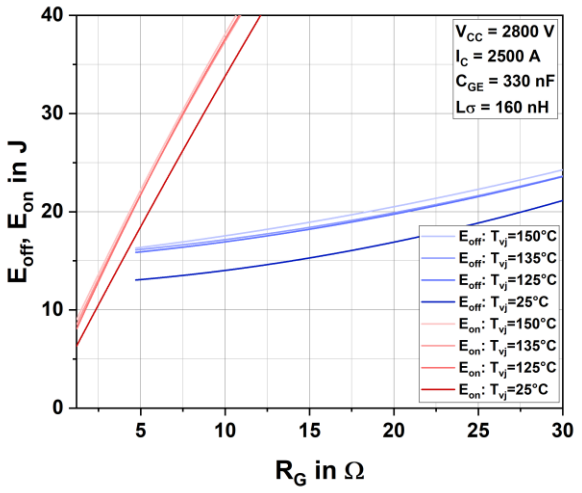

Fig. 9: Switching characteristics of the IGBT versus gate resistor R_G for Gen-1 based 4.5 kV / 2.5 kA IGBT-only module at different temperatures.

4.2.4 RBSOA

With the improved temperature capability, the 2.5 kA Gen-1 module manages to safely switch off currents beyond the reverse bias safe operating area at T_{vj}=150 °C, as reported in Fig. 10, which shows a switching event, where the DC-link voltage V_{CC}=3.6 kV, I_C=5.5 kA (2.2x I_{nom}) and R_{Goff}=14.2 Ω.

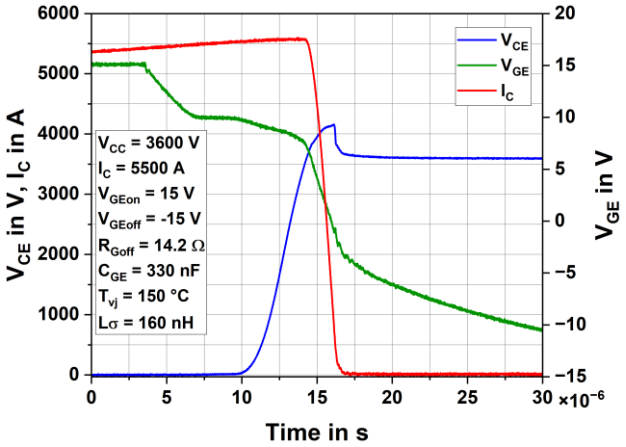

Fig. 10: RBSOA at 2.2x I_{nom} switching current for Gen-1 based 4.5 kV / 2.5 kA IGBT-only module at T_j=150°C and V_{CC}=3.6 kV.

The stray inductance of the test circuit $L_σ$=160 nH is notably higher than in a typical HVDC application, where $L_σ$ is likely below 100 nH. Despite such high parasitic inductance, the device could be safely operated under RBSOA conditions without the risk of reaching critical overvoltage and without any additional voltage clamping circuitry. Another threat to device safety in high-current-high-voltage situations is dynamic avalanche, which can lead to device failure, especially at high temperatures [8]-[10]. By choosing R_{Goff} high enough (14.2 Ω), we were able to avoid putting our device in a dynamic avalanche situation. As mentioned in section 4.2.3. there is a trade-off in respect to losses when choosing a higher R_{Goff} but as can be seen in Fig. 9, E_{off} is not strongly dependent on the gate resistor and hence losses don't increase dramatically even with large changes of the resistor value.

4.3 Gen-1 4.5 kV / 5 kA module operation

Nominal and RBSOA performance of the 6-pocket module at T_{vj}=150°C are expected to be in line with what was presented for the 3-pocket module in the previous section and efforts to qualify this product are under way. The main limiting factor to qualification is obviously the dynamic testing capability, which requires inductive switching of currents beyond 10 kA and handling yet higher short-circuit currents. This is why Hitachi Energy is extending its dynamic testing capability to ensure full and extended testing of the new 5 kA IGBT-only module and beyond. Meanwhile, extensive qualification testing on submodule level is ongoing to ensure sufficient SOA margin to offset any effects of de-rating due to paralleling. Early production runs of the 5 kA module at T_{vj}=125°C have shown that static parameters such as V_{CEsat} and I_{CES} are in accordance with what we have shown in section 4.1, as was expected and can be seen in Fig. 11.

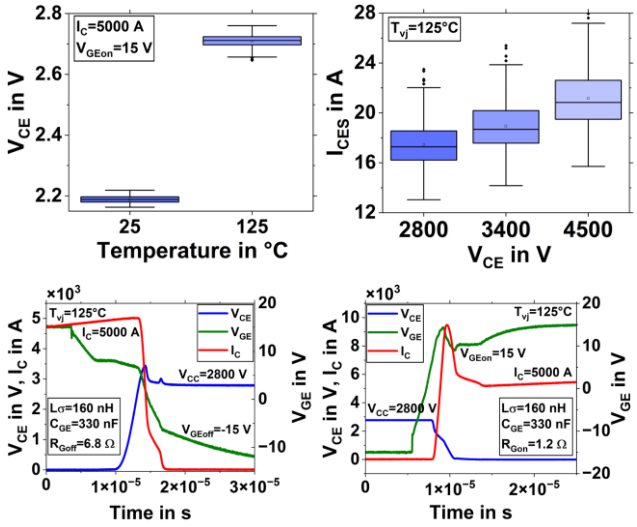

Fig. 11: Nominal on-state voltage and collector-emitter leakage current as measured in production, T_{vj}=125°C (top). Switching waveforms at nominal conditions V_{CC}=2800 V, I_C=5000 A, R_{Goff}=6.8 Ω, R_{Gon}=1.2 Ω and T_{vj}=125°C (bottom).

Additionally, IGBT turn-off and turn-on switching waveforms are shown in Fig. 11 as measured in production, with turn-off losses below 40 J at nominal conditions V_{CC}=2800 V and I_C=5000 A, matching well with the turn-off losses below 20 J observed at half the current for the 3-pocket module.

4.4 Short-circuit safe operating area

The Gen-1 technology also shows impressive short-circuit safe operating area (SCSOA) capability. Short-circuit currents presented in this section are scaled from submodule to 5 kA module level for more relatability to the application case, as current testing limitations don't permit full module SC testing. In Fig. 12 we show the SC waveform of a Gen-1 IGBT-only submodule at T_{vj}=150°C, with pulse length t_p greater than 18 µs, at V_{CC}=3.6 kV and V_{GE}=15 V. R_{GEon} on submodule level was 5.6 Ω corresponding to 0.93 Ω if scaled to module level. Hence, short circuit capability on module level above t_p=10µs, as usually specified in our data sheets, is highly expected.

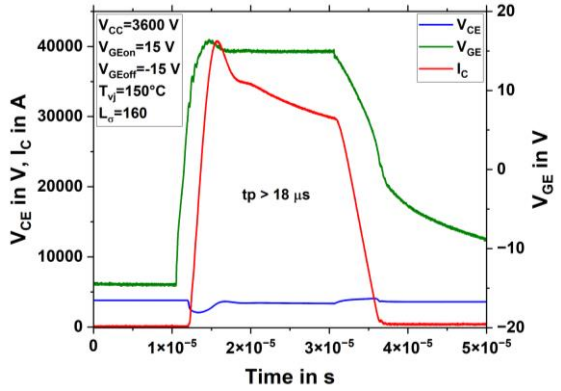

Fig. 12 SCSOA waveform at V_{CC}=3.6 kV and T_{vj}=150°C scaled from submodule to module level for Gen-1 IGBT technology.

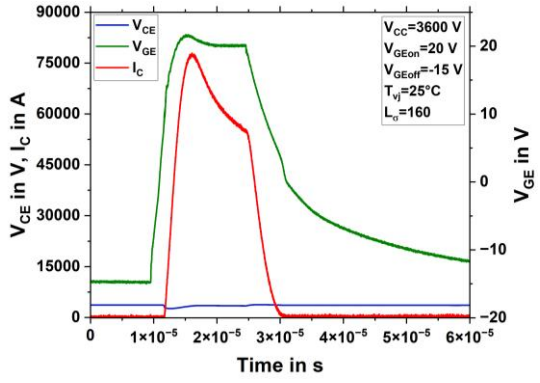

Fig. 13: SCSOA waveform at V_{CC}=3.6 kV, V_{GEon}=20 V and T_{vj}=25°C scaled from submodule to module level for Gen-1 IGBT technology.

Due to increased carrier mobility, at low temperatures the short-circuit current is higher than at high temperatures considering the same conditions, posing a risk to the device. Due to this we tested the Gen-1 IGBT-only with elevated V_{GEon}, as shown in Fig. 13, allowing us to check its capability under strongly increased currents. At T_{vj}=25°C, V_{CC}=3600 V, V_{GEon}>19 V, R_{GEon}=10 Ω and t_p=10 µs our Gen-1 submodule is capable of withstanding and safely turning off short-circuit pulses with scaled peak-currents as high as 75 kA. We expect that module performance with respect to the magnitude of the short-circuit current I_{SC} will show comparably impressive capability as for submodules. Despite the strong short circuit withstand capability of our Gen-1 based device, the magnitude of the short circuit current I_{SC}>30 kA can be undesirable. Development activities to lower the short circuit current of future chip technologies without compromising on-state characteristics using our novel MOS-cell design principle are ongoing, as reported previously in [7].

5 Fast recovery diode

5.1 Device characteristics

Hitachi Energy's newly developed FRDs consist of classical P-i-N diode wafers with typical on-state values V_F around 1.8 V and 2.7 V at I_F=2.5 and 5 kA respectively for all diode sizes mentioned in section 2.2. The anode buffer of the diode is designed for low leakage current and high robustness with respect to turn-off [3]. The cathode features segmented p-n structures for soft reverse recovery at low current densities as well as high DC-link voltages V_{CC}. The diode design has been optimized for operation up to T_{vj}=140°C with changes around the junction termination (negative bevel) and optimized dosing of proton and electron irradiation enabling soft reverse recovery and wide turn-off safe operation area up to V_{CC}=3.6 kV [3].

5.2 Dynamic performance

The results presented in this section were obtained using the same dynamic setup as previously described for the IGBT. The FRD and switch used were the PP119 and 5 kA / 4.5 kV IGBT-only module, respectively.

5.2.1 Dynamic high temperature performacne

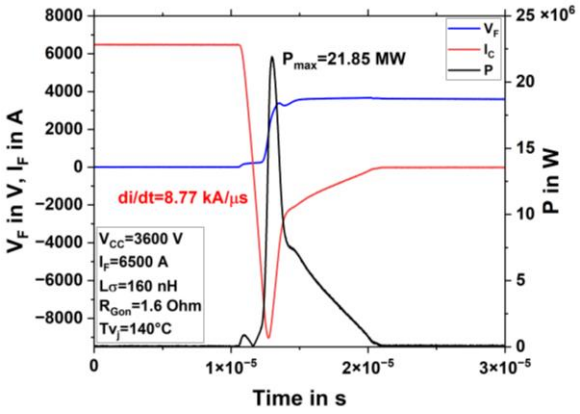

Fig. 14: Diode turn-off at SOA conditions V_{CC}=3.6 kV, I_F=6500 A at T_{vj}=140°C with R_{Gon}=1.6 Ω, L_σ=160 nH and 4.5 kV / 5 kA IGBT-only Gen-1 module used as switch.

Figure 14 shows an exemplary diode turn-off waveform at V_{CC}=3.6 kV and I_F=6.5 kA, with T_{vj}=140°C, R_{Gon}=1.6 Ω and L_σ=160 nH. Under these conditions,

the diode manages to safely turn off, with maximum peak-power P_{max} close to 22 MW and di/dt close to 9 kA/µs. Furthermore, as can be seen in the figure, the overshoot of the voltage is safely below the rated reverse voltage V_{RRM}=4.5 kV. Despite these capabilities, careful attention should be paid, when simultaneously operating at high currents and high di/dt, as the recovery current can thermally overload the IGBT during turn-on [3].

5.2.2 Dynamic room temperature performance

At low temperatures under high V_{CC} and *di/dt* conditions the diode can experience oscillations in voltage and current, during the reverse recovery. This condition, known as snappiness of the diode, occurs when current density in the on-state prior to turn-off approaches zero. The diode and the IGBT are then at risk of destruction due to overvoltage [3]. As reported in [3], during qualification measurements of the diode, with IGBT-only Gen-1 technology used as switch, high over voltage situations were provoked by narrowing the current pulse in the diode to t_p=30 µs, creating voltage spikes of nearly 7 kV without destruction of the diode or the IGBT (see Fig. 15). Of course, under normal operation, switching conditions should be chosen to not overcome reverse and blocking voltage of 4.5 kV, as elaborated in [3].

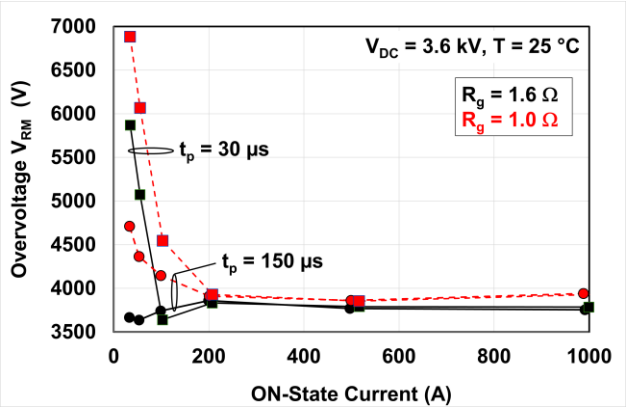

Fig. 15: Diode overvoltage vs. ON-state current at V_{CC}=3.6 kV, pulse width t_p = 30 and 150 µs, T_{vj}=25°C, R_{Gon}=1.0 and 1.6 Ω, L_σ=160 nH. The 4.5 kV / 5 kA IGBT-only Gen-1 module was used as switch.

5.3 Surge current capability

The surge current capability is key to clearing short-circuit cases in VSC-HVDC MMC topologies. Using a discrete diode over a combined IGBT-diode module comes with the advantage of increased surge current capability without destruction, allowing simplification in the protection of the MMC [3]. Figure 16 shows the last pass surge current test of our new scalable diode by area with t_p=10 ms and T_{vj}=140°C. As seen in the figure, the need for higher surge current capability can be accommodated by increasing the diode area [3]. The datasheet I_{FSM} values, which include safety margin, are 75 kA, 80 kA and 100 kA for PP110, PP119 and PP143 respectively [3].

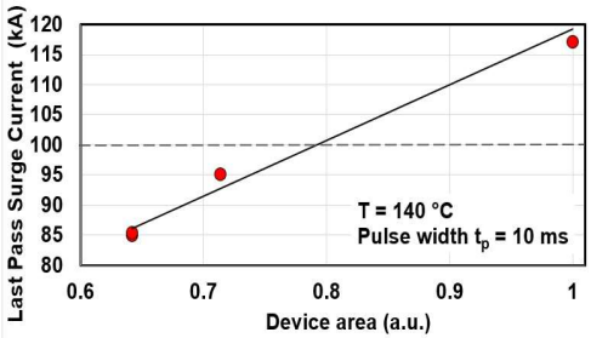

Fig. 16: Last pass surge current vs. diode area of PP110, PP119, and PP143 measured at T_{jmax}=140°C.

6 VSC-HVDC MMC simulation

Following we will show HVDC system simulation results based on typical values for a ±800 kV HVDC system operated in rectifier and converter mode. Simulation results were generated with Hitachi Energy's SEMIS circuit simulator. In the simulation we assume a cooling liquid temperature of T_w=60°C, a switching frequency of f_{sw}=96 Hz, and a cell voltage V_{CC}=2.8 kV with AC current I_{rms}=6670 A and arm current I_{arm}=4275 A (rms). Additionally, semiconductor input parameters are based on typical values for the 4.5 kV / 5 kA Gen-1 IGBT-only and complementary 4.5 kV / 5 kA FRD. The simulation allows us to estimate the link power reachable with the 5 kA Gen-1 IGBT-only StakPak and the complimentary FRD and is above 8 GW, which is achieved with an arm current of 3800 A (rms).

Operating mode	Arm Current (rms) [A]	T_{vj} IGBT [°C]	T_{vj} Diode [°C]	Losses [%]
Inverter	4275	143.3	93.3	0.95
Rectifier	4275	128.9	107.5	0.95

Table 1: Overview of device temperatures and overall losses with 4.5 kV Gen-1 IGBT StakPak and corresponding 4.5 kV FRD.

Table 1 shows, that with our technology improvements during steady state operation, device temperatures remain below maximum operating conditions and overall losses in inverter and rectifier mode are below 1%. An example of simulated waveforms is shown in Fig. 17, showing the system in inverter mode.

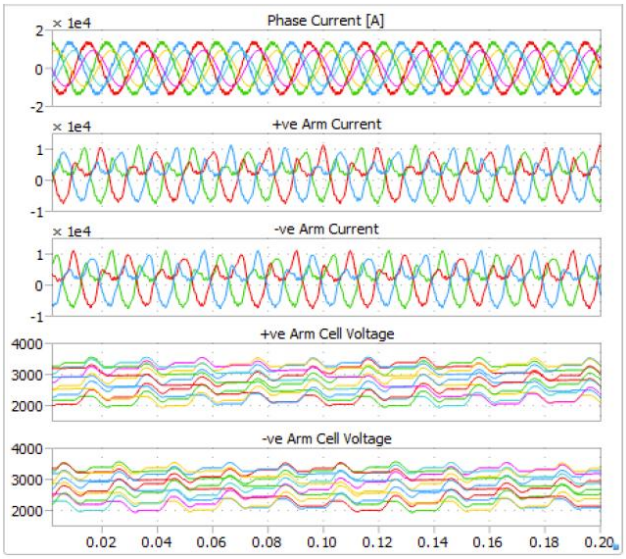

Fig. 17 Inverter operation with I_{rms} = 6670 A, V_{CC}=2800 V, T_W=60°C, f_{sw}=96 Hz.

7 Summary and conclusion

In this paper we have presented our advanced 4.5 kV Gen-1 IGBT chip technology scaled to 2.5 kA and 5 kA StakPak with overall improved losses and reduced leakage currents enabling high temperature operation. Our new scalable 4.5 kV fast recovery diode platform aimed at increasing the current capability of VSC-HVDC MMC topologies was also briefly presented. We have shown that our new technologies and devices are well suited for VSC-HVDC applications thanks to low on-state losses excellent SOA capabilities at high temperatures and strong surge current capability of the diode. A summary overview of important parameters is presented in Table 2.

Device	T_{vjmax}	V_{CEsat}/V_F	E_{off}	IGBT, Diode performance
IGBT 2.5 kA	150°C	< 3 V (T_{vj}=150°C)	< 20 J (T_{vj}=150°C)	**RBSOA:** > 2xI_{nom} (V_{CC}=3.6 kV, T_{vj}=150°C) To be verified for 5 kA module **SCSOA:** tp > 10 µs (V_{CC}=3.6 kV, T_{vj}=150°C) passed I_{SCmax} > 75 kA scaled from submodule (t_p=10 µs, V_{CC}=3.6 kV, V_{GEon}>19 V, T_{vj}=25°C)
IGBT 5 kA			< 40 J (T_{vj}=125°C) To be verified for T_{vj}=150°C	
PP110	140°C	1.8 V / 2.7 V (2.5 kA / 5 kA, 140°C)	-	I_{FSM}=75 kA (T_{vj}=140°C, t_p=10 ms)
PP119				I_{FSM} =80 kA (T_{vj}=140°C, t_p=10 ms) **SOA:** P_{max}: 22MW, di/dt: 9 kA/µs (V_{CC}=3.6 kV, I_F=6.5 kA T_{vj}=140°C)
PP143				I_{FSM}=100 kA (T_{vj}=140°C, t_p=10 ms)

Table 2: Summary overview of the parameters presented in this paper for IGBT-only Gen-1 and FRDs.

In conclusion, our new IGBT-only StakPak modules and discrete FRDs are an important and highly competitive addition to Hitachi Energy‘s ongoing efforts to contribute to 8 GW HVDC transmission, making such applications more efficient, reliable and safe.

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