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New 650V SiC MOSFET for System Efficiency, EMI and Reliability

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Abstract

The rapid growth of Artificial Intelligence (AI) is driving a significant demand for data centers, which has greatly increased energy demands and led to innovations in high-performance data center design. Today's Server PSUs in development aim to meet the 80 Plus Titanium standard, requiring over 96% peak efficiency at half loads. While Si Super-junction (SJ) MOSFETs struggle to meet the Titanium specifications, 650V SiC MOSFETs enable innovative, high-performance PSU designs that further shrink footprints while challenging both thermal and electromagnetic interference characteristics of power devices. 650V SiC MOSFETs, which have low $R_{DS(ON)}$, capacitances, and body diode recovery charge (Q_{RR}), are replacing SJ MOSFETs in advanced topologies such as Totem-pole PFC, and CLLC resonant topologies. This paper highlights key parameters of Power Master Semiconductor's 650V *e*SiC M1 MOSFET and its benefits over planar and trench competitors' 650V SiC MOSFETs.

1 Introduction

The digital transformation that many companies underwent as the pandemic continued to impact the world has driven the rapid growth of artificial intelligence (AI), which is expected to drive continued strong demand of data centers. This will spur innovations in data center design and technology to deliver the capacity that meets the increased power density requirements of high-performance computing. Future requirements for power supplies will necessitate a simultaneous increase in power density along with enhance operating efficiency. For example, 80 Plus Titanium will be a mandatory requirement for single output power supply units (PSU) by 2023 and all PSUs by 2026. (System efficiency > 90% at 10% load, System efficiency must achieve > 96% at 50% load) as shown in Fig 1. Si Super-junction MOSFETs have been widely used for 400~900V range in power conversion applications such as the power factor correction and primary switch for DC-DC converters. Si Super-junction MOSFETs already have trouble meeting the Platinum specifications. In response to these requirements, engineers are exploring alternative devices to design innovative and high-performance PSU's that further shrink footprints while addressing both thermal and electrical characteristics of power devices. Hence, the 650V SiC MOSFETs are quickly penetrating the server, telecom, and datacenter AC/DC power supply units (PSU's) due to their combined low $R_{DS(ON)}$, low capacitances, and very low diode recovery charge, Q_{RR}, versus silicon devices. These are the main features that are required for enabling increased power density and system efficiency demands of the next generation PSU's.

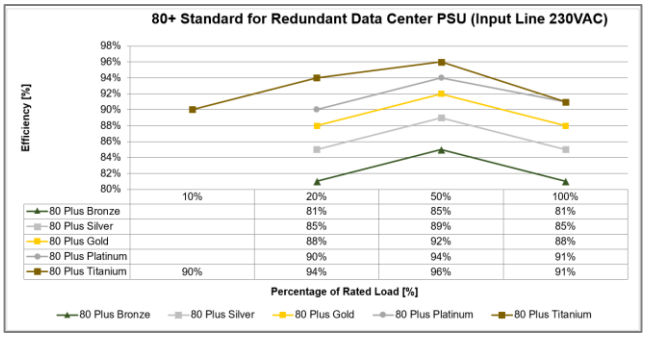

Fig. 1. 80 Plus standard for redundant / data center PSU (Input line $230V_{AC}$)

Requirements of increased power density and efficiency drive the need for more advanced circuit topologies that generally require the power switch to operate at higher switching frequencies (F_{SW}). This places a strong demand on the need for very low switching losses, which are related to some of the device figures-of merit (FOMs : $R_{DS(ON)}$ x Q_G, $R_{DS(ON)}$ x Q_{OSS}, $R_{DS(ON)}$ x Q_{RR}). Many PSU's still design-in and use Si Super-junction MOSFETs, with SiC being adopted very quickly and replacing Super-junction MOSFETs in some key sockets for the advanced topologies such as Totem Pole PFC, and high frequency LLC resonant converters. 650V to750V SiC MOSFET is also widely used for on board chargers (OBCs). The purpose of this paper is to highlight the key characteristics of Power Master Semiconductor's new 650V *e*SiC MOSFET M1 compared to competitor's 650V trench and planar SiC MOSFETs at both device and system levels.

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2 650V *e*SiC M1 MOSFET Technology

Two typical structures (planar and trench) of SiC MOSFET are available today, SiC MOSFET structures depend on the performance of the device, strategy, and the target applications [1]~[3]. The planar structure is easier to fabricate but has the disadvantage of having a higher R_{SP} (Resistance per unit area) compared to the same rating trench structure. This is due to the channel current flowing perpendicularly to the vertical direction and the existence of the inner JFET region. Trench structure is good to reduce both $R_{DS(ON)}$ and switching performance because the electron mobility of the channel formed in the trench sidewall is greater than that of the surface part. However, the disadvantage of trench struture is that it requires a complex SiC trench etching process and has lower ruggedness compared to the planar structure. 650V *e*SiC M1 technology is Power Master Semiconductor's first generation of SiC MOSFET.

2.1 Performance benchmark of *e*650V SiC MOSFET M1

Table 1 shows the key parameter comparison of 650V SiC MOSFETs. The advantages of 650V *e* SiC MOSFET M1 (PCZ65N45M1) are the reduced switching losses, lower dynamic C_{OSS} losses (E_{Dyn}) and robust avalanche capability, which contribute to both high system efficiency and reliability.

Specification	PCZ65N45M1	Comp. A (Planar)	Comp. B (Planar)	Comp. C (Trench)
BV_{DSS} [V]	650	650	650	650
I_D [A]	44	49	47	39
V_{GS_op} [V]	-5 / +18	-4 / +15	-5 / +18	0 / +18
V_{GS_max} [V]	-10 / +22	-8 / +19	-10 / +22	-5 / +23(pulse)
$R_{DS(on)}$ [mΩ] (typ)	45	45	44	45
V_{TH} [V]	1.8 / 2.8 / 4.5	1.8 / 2.6 / 3.6	1.8 / 2.8 / 4.3	3.5 / 4.5 / 5.7
E_{DYN} [uJ]	1.2	1.4	2.0	1.5
Q_G [nC]	55	63	74	33
E_{ON} [μJ] @ I_D=20A, R_G=2.7Ω	33	48	78	43
E_{OFF} [μJ] @ I_D=20A, R_G=2.7Ω	14	17	25	18
I_{AS} @ L=1mH, R_G=25Ω	34	30	15	21

Table 1. Key Parameter Comparison of Power Master Semiconductor's 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) and Competitors

2.1.1 Dynamic C_{OSS}, E_{Dyn}

Recently, power loss due to hysteresis C_{OSS} is analyzed in many papers [4]~[6]. Unexpected power losses, especially in SJ MOSFETs in ZVS topologies, are generated due to the hysteretic phenomenon of the output capacitance, C_{OSS}. These power losses related to C_{OSS} hysteresis are more critical in soft switching topologies such as LLC when operating under high frequency conditions, especially in medium and light loads. Consequently, a certain amount of energies is generated. Dynamic C_{OSS} loss (E_{Dyn}) can be defined as the difference between charging energy and discharge energy excluding some lost energy during discharging process. This energy losses can be observed by hysteresis loop area large signal C_{OSS} during charge-discharge cycle as shown in Fig. 2.

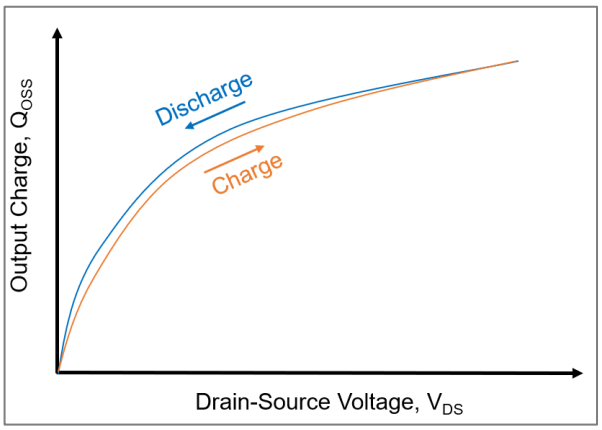


Fig. 2. Hysteresis Charging and Discharging of C_{OSS}

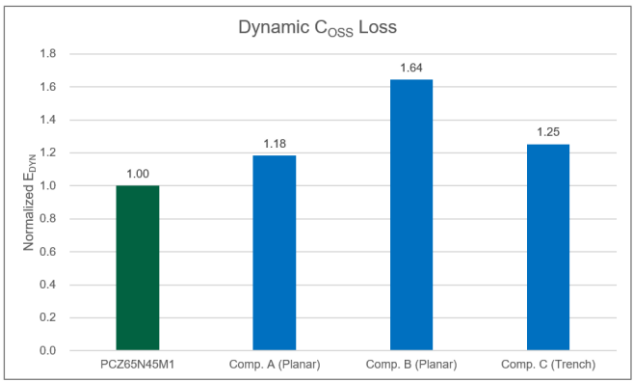


Fig. 3. Normalized Dynamic C_{OSS} loss of 650V *e*SiC MOSFET M1 (PCZ65N45M1) vs. Competitors

The dynamic C_{OSS} losses (E_{Dyn}) are affected by device structure especially the termination area, die size, and switching dV_{DS}/dt in SiC MOSFETs [5]. Fig. 3 shows a normalized dynamic C_{OSS} loss of the 650V *e*SiC MOSFET M1 (PCN65N45M1), and competitor under same condition, V_{DS}=0~400 V. The dynamic C_{OSS} loss of 650V *e*SiC MOSFET M1 (PCN65N45M1) is 15~39% less than both planar and trench SiC competitors.

2.1.2 Switching Characteristics

Fig. 4 shows the measured switching losses (E_{on} and E_{off}) comparisons of 650V/45mΩ *e* SiC MOSFET M1 (PCN65N45M1) and its competitors (trench and planar). The measurements were performed using the body diode of same DUT as a freewheeling diode in the high side device, with V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, under various I_D conditions. Turn-on loss (E_{on}) is 17% and 58% lower and turn-off loss (E_{off}) is 29% and 45% lower for 650V/45mΩ *e* SiC MOSFET M1 (PCN65N45M1) compared to that of competitor C (trench) and competitor B (planar) under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, I_D=30A, FWD=Same DUT.

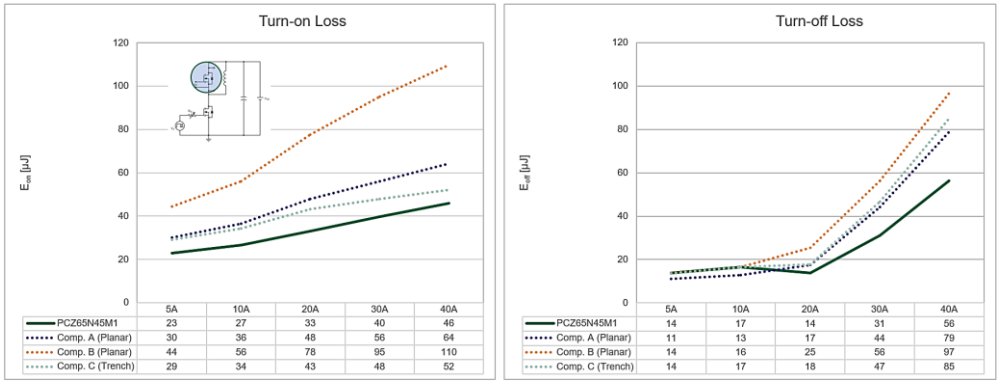
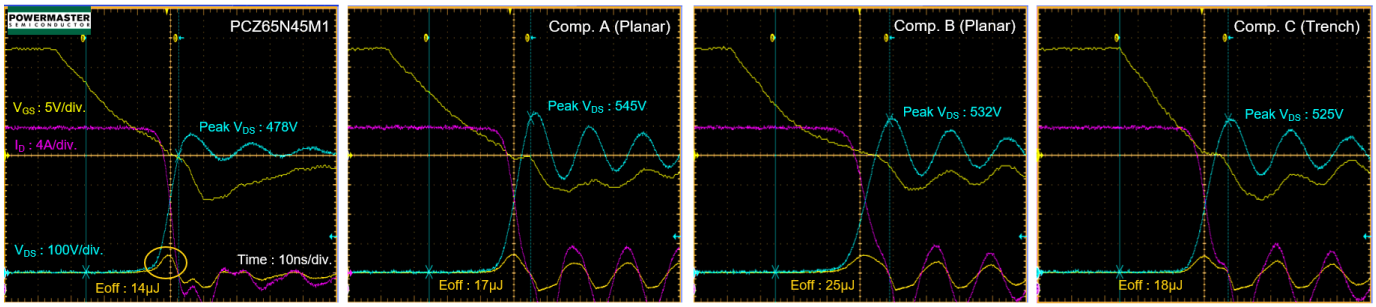


Fig. 4. Comparison of Switching Losses - 650V/45mΩ *e*SiC MOSFET M1(PCZ65N45M1) vs. competitors under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, Free-wheeling Diode: Same DUT



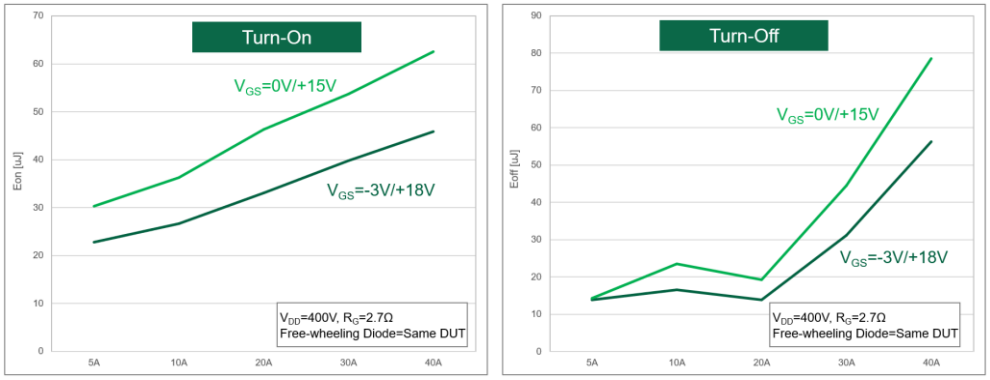
(a) PCZ65N45M1 (b) Comp. A (Planar) (c) Comp. B (Planar) (d) Comp. C (Trench)

Fig. 5. Comparison of Switching Waveforms at Turn-Off Transient - 650V/45mΩ *e* SiC MOSFET M1 (PCN65N45M1) vs. Planar and Trench Competitors under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, I_D=20A, Free-wheeling Diode: Same DUT

Fig. 5. shows the turn-off waveforms of SiC MOSFETs under V_{DD}=400V, V_{GS}=-3V/+18V, R_G=2.7Ω, I_D=20A, FWD=Same DUT. As shown in Fig. 5, 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) significantly reduces both turn-off loss and drain-source voltage spikes, which are typically in trade-off by its optimized design. The turn-off loss (E_{off}) is 22% less and peak drain-source voltage is reduced by 47V for 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) even compared to those of competitor C(trench). Additioanlly, both voltage and current ringing of 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) are substantially reduced compared to its competitors.

2.1.3 Switching Behavior vs. Gate Driving Voltage (V_{GS})

Unlike Super-junction MOSFETs, which typically operate with gate driving voltage (V_{GS}) ranging from 0 to 10V, SiC MOSFETs require higher gate driving voltage (V_{GS}) swing typically, -3 or 0 to +18V due to challenges such as lower channel mobility. Fig. 6. shows the variation in switching loss with different gate driving voltages for 650V/45mΩ *e*SiC MOSFET M1. As positive gate voltage increases, turn-on switching loss decreases, while turn-off loss remains similar as shown in Fig. 6 (a). However, higher gate voltage imposes more stress on gate oxide, potentially resulting in $V_{GS(TH)}$ drift. As negative gate voltage increases, turn-off switching loss decreases, while turn-on loss remains similar as shown in Fig. 6 (b). As a results, at I_D=30A,.E_{on} at $V_{GS(on)}$=18V is reduced by 26% compared to it at $V_{GS(on)}$=15V and E_{off} at $V_{GS(off)}$=-3V is reduced by 30% compared with it at $V_{GS(off)}$ =0V. Fig. 7 shows the measured switching losses (E_{on} and E_{off}) comparisons with different V_{GS} of 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) and its competitors (trench and planar). As shown in Fig. 7, 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) shows similar or lower E_{on} and E_{off} with V_{GS}=0/+15V compared to that of competitors with V_{GS}=-3V/+18V under same conditions except for gate driving voltage, V_{GS}. As shown in Fig. 8 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) shows similar switching waveforms with V_{GS}=0/+15V compared to its competitors with V_{GS}=-3V/+18V under V_{DD}=400V, I_D=30A, R_G=2.7Ω, free-wheeling diode=same DUT.



(a) Turn-on Loss (E_{on}) vs V_{GS} (b) Turn-off Loss (E_{off}) vs V_{GS}

Fig. 6. Switching Losses vs. V_{GS} of 650V/45mΩ *e*SiC MOSFET M1(PCZ65N45M1) under V_{DD}=400V, V_{GS}=-3V/+18V and 0V/15V, R_G=2.7Ω, Free-wheeling Diode=Same DUT

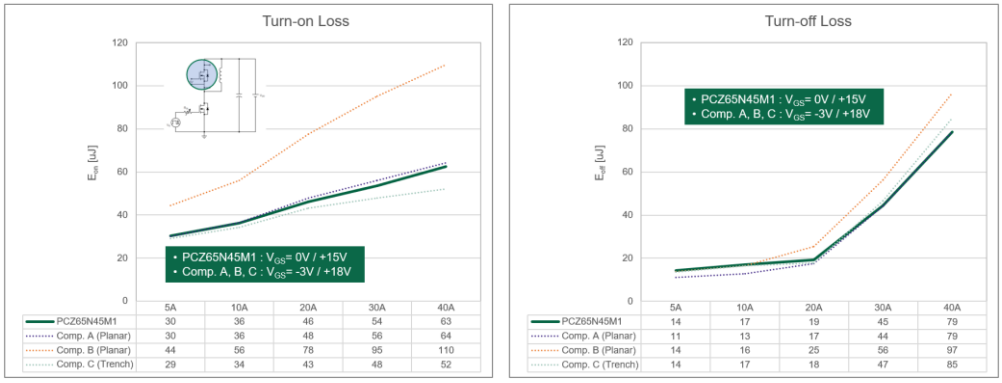


Fig. 7. Comparison of Switching Losses vs V_{GS} - 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) (V_{GS}=0V/+15V) vs. competitors (V_{GS}=-3V/+18V) under V_{DD}=400V, R_G=2.7Ω, Free-wheeling Diode : Same DUT

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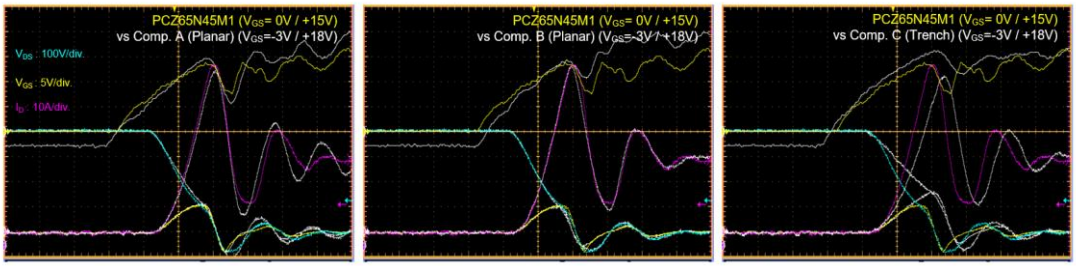
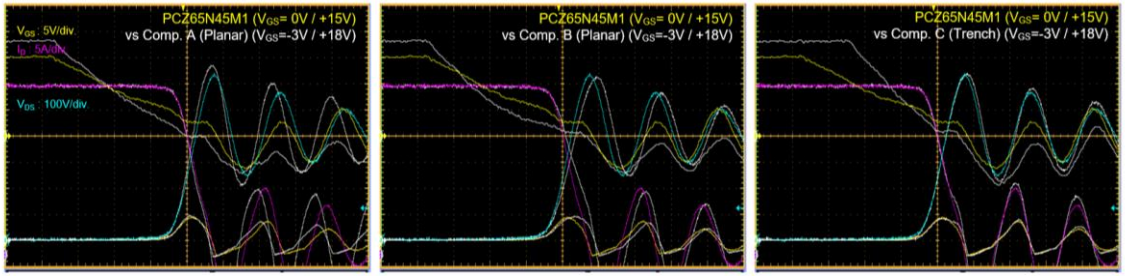


(a) Turn-on Transient



(b) Turn-off Transient

Fig. 8. Comparison of Switching Losses vs V_{GS} - 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) (V_{GS}=0V/+15V) vs. Competitors (V_{GS}=-3V/+18V) under V_{DD}=400V, R_G=2.7Ω, Free-wheeling Diode : Same DUT

650V *e*SiC MOSFET M1 can also be driven at lower gate driving voltages (15V) while maintaining similar turn-off loss compared to those of competitor's operation at $V_{GS(on)}$=18V. However operating at $V_{GS(on)}$=15V will negatively affect the $R_{DS(on)}$. Power Master recommends a $V_{GS(on)}$ of +18V as it can minimize both $R_{DS(on)}$ and turn-on switching loss. As shown in Fig. 8, 650V/45mΩ *e*SiC MOSFET M1 (PCN65N45M1) exhibits similar switching turn-on and turn-off waveforms with V_{GS}=0/+15V compared to competitors operating with V_{GS}=-3V/+18V under V_{DD}=400V, I_D=30A, R_G=2.7Ω and free-wheeling diode=same DUT.

2.1.4 Avalanche Capability (E_{AS}: Single Pulsed Avalanche Energy)

Typically, MOSFETs are employed in high-speed switching applications, therefore, electromagnetic force can be generated during switching transient due to abrupt changes of drain current from inductive loads. These forces may push the MOSFET into avalanche breakdown, potentially cause damage. Fig. 9 shows the avalanche current (I_{AS}) and energy (E_{AS}) measurement of the 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1), and its competitor under same conditions. The avalanche current (I_{AS}) and the avalanche energy (E_{AS}) of 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) are respectively 1.15 to 2.14 times higher and 1.32 to 4.58 times higher than those of both planar and trench SiC competitors. Fig. 10 shows drain current (I_D) and drain-source voltage (V_{DS}) waveforms during single pulse UIS test after failure under V_{DD}=70V, V_{GS}=-3/+18V, R_G=25Ω, L=1mH. The peak avalanche current (I_{AS}) gradually increases as the pulse width is increased until the device reaches its failure point. Upon failure, the voltage drops sharply, and the current begin to increase again linearly, as dictated solely by the inductor. After avalanche failure, the peak drain current of 650V/45mΩ *e*SiC MOSFET M1 (PCZ65N45M1) and its competitors is as follows:

- PCZ65N45M1 : 37.9A
- Competitor A : 30.2A
- Competitor B : 17.4A
- Competitor C : 22.1A

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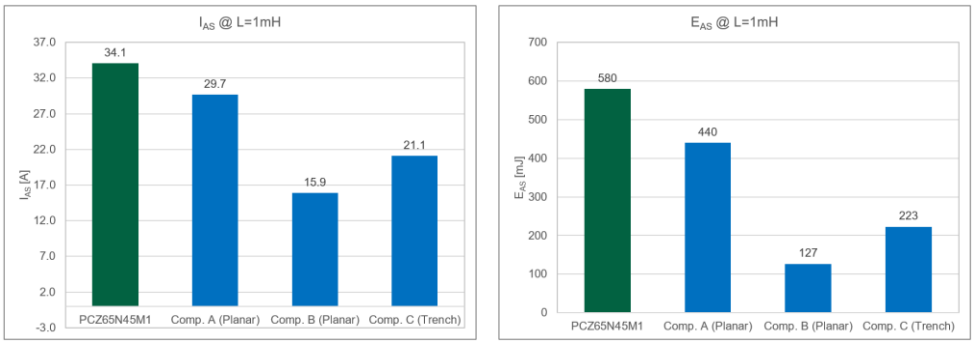
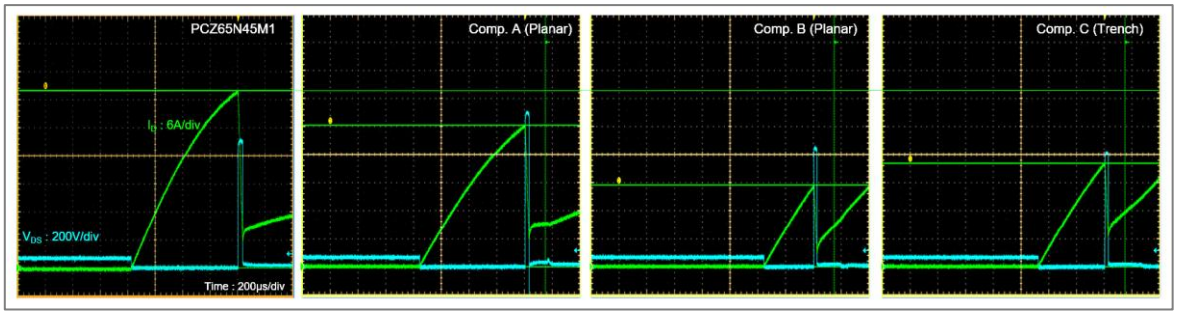


(a) Single Pulsed Avalanche Current (I_{AS}) (b) Single Pulsed Avalanche Energy

Fig. 9. Avalanche Capability under V_{DD}=70V, V_{GS}=-3/+18V, R_G=25Ω, L=1mH



(a) PCZ65N45M1 (b) Comp. A (Planar) (c) Comp. B (Planar) (d) Comp. C (Trench)

Fig. 10. Waveforms during Single Pulse Avalanche (E_{AS}) Test after Failure under V_{DD}=70V, R_G=25Ω, L=1mH

2.2 System efficiency comparison in 3kW CCM totem-pole PFC

The system efficinecy and switching noise of the 650V 𝒆SiC MOSFET M1 (PCZ65N45M1) are compared with competitor's 650V trench and planar SiC MOSFETs (DUTs), which is described in table 1, in a 3kW Continuous Conduction Mode (CCM) totem-pole PFC. Fig. 11 illustrates the block diagram of the 3kW CCM totem-pole PFC using SiC MOSFETs. Two SiC MOSFETs (Q_1 and Q_2) in fast leg operate at a switching frequency of 65kHz and another two MOSFETs (Q_{13} and Q_4), which are 650V/28mΩ SJ MOSFET (PMW60N028E7) in slow leg operate at line frequency (50/60Hz).

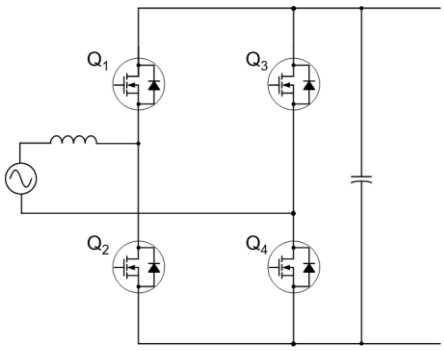


Fig. 11. 3kW CCM Totem-Pole PFC

The measured efficiency is shown in Fig 12. The 650V 𝒆 SiC MOSFET M1 (PCZ65N45M1) exhibits similar efficiency to the trench SiC competitor at half load and the highest efficiency, compared to competitor's planar and trench SiC MOSFETs at full load condition. The primary reason for higher efficiency is the reduced switch-off losses and output capacitive loss due to lower gate charger (Q_G) and dynamic C_{OSS} loss (E_{DYN}) of the 650V 𝒆 SiC MOSFET M1. This MOSFET combines faster and more rugged avalanche performance, aimed at achieving improved reliability and efficiency in various applications.

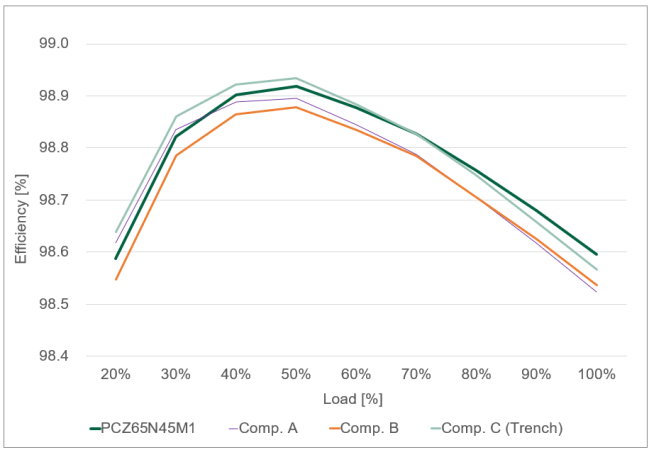
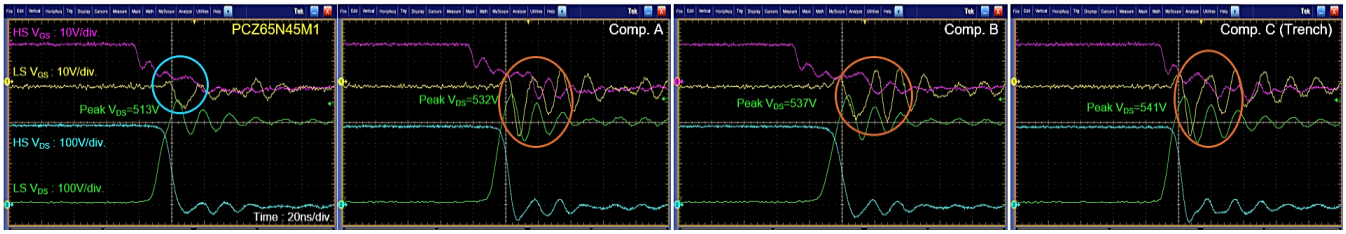


Fig. 12. Measureud Efficiency at 3kW CCM Totem-Pole



(a) PCZ65N45M1 (b) Comp. A (Planar) (c) Comp. B (Planar) (d) Comp. C (Trench)

Fig. 13. Measured Switching Waveforms during Low Side MOSFET Turn-Off Transient at 3kW CCM Totem-Pole PFC PFC under V_{IN}=220V_{ac}, V_{GS}=-2.5/+18V, R_{ON}=22Ω / R_{ON}=4.7Ω.

Fig. 13 shows the operating switching waveforms of V_{DS} and V_{GS} of both high side and low side MOSFETs during the low side MOSFET turn-off transient in a 3kW CCM Totem-Pole PFC under full load condition. As shown in Fig.13, the peak drain-source voltage (V_{DS}) and gate oscillation of 650V *e*SiC MOSFET M1 (PCZ65N45M1) are lower than those of competitor's planar and trench SiC MOSFETs. A unique advantage of the 650V *e*SiC MOSET is the lower voltage overshoot despite lower turn-off switching loss due to higher dv/dt compared to competitor's planar and trench SiC MOSFET. This unique switching characteristics of 650V *e*SiC MOSET can effectively reduce unwanted false turn-on and gate oxide damge failure during abnormal conditions.

3 Conclusion

The latest 650V *e*SiC M1 MOSFET technology shows significantly low switching losses, minimized voltage spikes, low dynamic C_{OSS} loss and high UIS capability, even when compared with trench SiC MOSFETs. The 650V *e*SiC M1 technology is designed to achieve high efficiency and reliability by minimizing switching losses, dynamic C_{OSS}, as well as improving avalanche ruggedness in both hard and soft switching topologies.

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