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# Switching Loss Reduction for 3.3kV-750A Full-SiC MOSFET Module by Active Gate Driver

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## Abstract

3.3kV high-current SiC MOSFET module is promising for enhancing efficiency in railway traction and renewable power generation sectors. Although it features low switching loss, high-frequency operation can still accumulate significant loss, potentially damaging long-term reliability and lifetime of the module. The conventional method for switching loss suppression is through the decrement of gate resistance, resulting in serious overshoot. To address these issues, an active gate driver (AGD) is designed in this paper to reduce the switching loss without intensifying the overshoot. A mathematical model is established to elucidate the design methodology of AGD, and experiments validate the proposed method's effectiveness.

## 1 Introduction

In recent years, semiconductor manufacturers such as Infineon, Mitsubishi, and Fuji have started releasing and promoting their 3.3kV high-current SiC MOSFET modules[1]. Fig. 1 illustrates the Fuji 3.3kV-750A SiC MOSFET module packaged with advanced HPnC, which is a proto-type module used in this work[2]. Currently, the 3.3kV-750A SiC MOSFET module as shown in Fig. 2 has been newly developed, and it has been added to the line-up of HPnC[3]. In comparison with HPM, the parasitic inductance of HPnC achieves 10nH, decreased by 76% owing to its laminated structure, as depicted in Fig. 3.

**Fig. 1:** A proto-typed Fuji 3.3kV-SiC MOSFET module

**Fig. 2:** Fuji 3.3kV-SiC MOSFET module under development

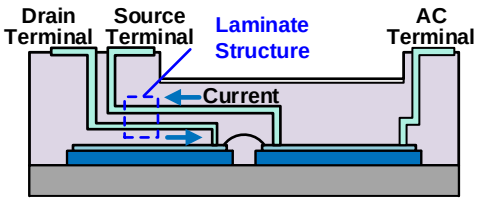


**Fig. 3:** Laminated structure of HPnC

Utilizing the Fuji 3.3kV SiC MOSFET module enables significant reductions in the volume of inverters. However, some studies have shown that the switching performances of SiC MOSFET still exhibit certain limitations[4]. Although SiC MOSFET features low switching loss, high-frequency operation can still accumulate significant loss, posing challenge to lifetime and long-term reliability of the power module. Nonetheless, this approach usually results in serious overshoots and oscillations, leading to an observed increment in electrical stress[5]. Therefore, a tradeoff between switching loss and electrical stress must be struck by CGD, limiting its effectiveness in switching loss reduction. Obviously, developing a driving technology that can achieve switching loss reduction without intensifying the electrical stress is crucial for fully leveraging the superior switching characteristics of SiC MOSFET module.

Recently, active gate drivers (AGD) have garnered widespread attention for its potential in switching loss reduction, and its effectiveness have been confirmed by many literatures. In [6], an AGD with multistage gate resistance control is proposed for Wolfspeed's C3M0021120K, achieving a reduction in switching loss by 5%-30%. In [7], an AGD designed for ROHM's SCH2080KE is developed, which reduced switching loss by 30.4% through dynamic adjustment of the driving resistance. Similar work can also be found in [8]-[10], and the effectiveness of AGD is fully demonstrated.

In summary, the working principle of AGD involves adjusting the driving resistance at different stages of the

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SiC MOSFET switching transient, thereby the values of driving resistance will have a critical impact on optimization effect on AGD. However, existing studies have only conducted qualitative analysis, lacking theoretical guidance, resulting in AGD's performance not reach optimality. To address this issue, a mathematical model is established in this paper to guide the selection of driving resistance of AGD. Based on this, an AGD tailored for Fuji 3.3kV SiC MOSFET is designed. The experimental results show taht AGD can reduce switching loss by 17.9%

This paper is organized as follows. Section II presents the mathematical model and the working principles of AGD. Then, Section III validates the mathematical model through rigorous analysis. Section IV details the designed AGD based on proposed method, and its effect on switching loss reduction is verified by experimental results. Finally, Section V concludes this paper.

## 2 Mathematical Model and Working Principle of Active Gate Driver

Fig. 4 illustrates four distinct stages of the switching transient: the current rise stage (Stage-I), current overshoot stage (Stage-II), voltage rise stage (Stage-III), and voltage overshoot stage (Stage-IV). The device behavior of SiC MOSFET and working principle of AGD during each stage is outlined as follows:

(1) Stage-I ($t_0$~$t_1$):

In this stage, gate-source capacitor $C_{GS}$ is charged by $U_{CC}$ through $R_{GON}$, as shown in Fig.5 (a). When the $U_{GS}$ exceeds the threshold voltage $U_{th}$, the channel current $I_{CH}$ of the SiC MOSFET begins to rise. In previous studies, a linearized formula is commonly used to represent the relationship between $I_{CH}$ and $U_{GS}$:

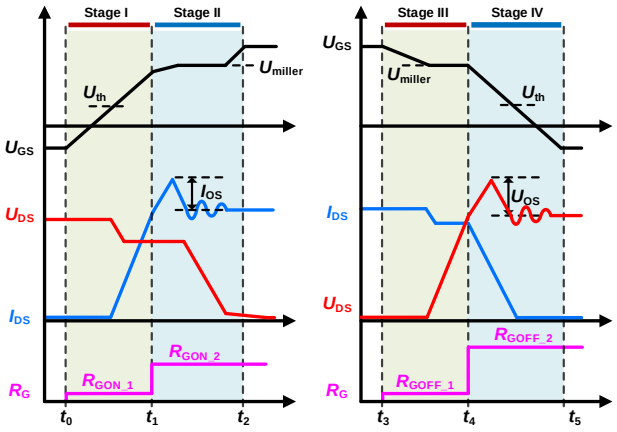
$$I_{CH} = g_m\left(U_{GS} - U_{th}\right) \tag{1}$$

where $g_m$ is the transconductance of the SiC MOSFET.

However, medium-voltage SiC MOSFET module's transfer characteristics exhibit a high degree of nonlinearity, leading to (1) being unable to accurately describe the device behavior. Therefore, in this paper, a quadratic formula is used[11]:

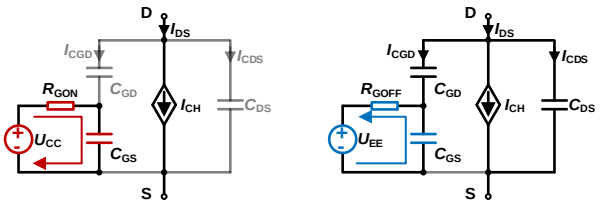
$$I_{CH} = k_{fs}\left(U_{GS} - U_{th}\right)^2 \tag{2}$$

where $k_{fs}$ is a coefficient determined by the transfer characteristics of SiC MOSFET module. In order to provide guidance for the design of AGD, $dI_{DS}/dt$ is required. As depicted in Fig. 5, $I_{DS}$ is composed by $I_{CH}$, $I_{CGD}$ and $I_{CDS}$. In Stage-I, due to $U_{DS}$ remains unchanged, the current of $C_{GD}$ and $C_{DS}$ can be neglected. Thereby, we can approximate that:




(a)Turn-on transient (b)Turn-off transient

**Fig. 4:** Switching transient characteristics of SiC MOSFET




(a)Stage-I (b)Stage-III

**Fig. 5:** Switching transient characteristics of SiC MOSFET

$$I_{DS} \approx I_{CH} = k_{fs}\left(U_{GS} - U_{th}\right)^2 \tag{3}$$

Then, take the derivative of (3):

$$\frac{dI_{DS}}{dt} = 2k_{fs}\left(U_{GS} - U_{th}\right)\frac{dU_{GS}}{dt} = 2k_{fs}\sqrt{\frac{I_{DS}}{k_{fs}}}\frac{dU_{GS}}{dt} \tag{4}$$

where $dU_{GS}/dt$ can be represented as:

$$\frac{dU_{GS}}{dt} = \frac{U_{CC} - U_{th} - \sqrt{\frac{I_{DS}}{k_{fs}}}}{R_{GON}C_{GS}} \tag{5}$$

Subsequently, by substituting (5) into (4), the $dI_{DS}/dt$ can be expressed as a function of $I_{DS}$ and $R_{GON}$:

$$\frac{dI_{DS}}{dt} = 2k_{fs}\sqrt{\frac{I_{DS}}{k_{fs}}}\frac{U_{CC} - U_{th} - \sqrt{\frac{I_{DS}}{k_{fs}}}}{R_{GON}C_{GS}} \tag{6}$$

This expression indicates that the control over $dI_{DS}/dt$ can be achieved by adjusting $R_{GON}$.

In Stage-I, the rise of $I_{DS}$ leads the overlap between $U_{DS}$ and $I_{DS}$, resulting in primary turn-on loss $E_{on}$. It is obvious that $E_{on}$ is inversely proportional to $dI_{DS}/dt$. Therefore, a smaller enough driving resistance $R_{GON\_1}$ should be selected by AGD, thus the turn-on loss reduction can be realized. The selection of $R_{GON\_1}$ is constrained by maximum output current of the gate driver:

$$R_{GON\_1} = \frac{U_{CC} - U_{EE}}{I_{omax}} - R_{Gint} \quad (7)$$

where $I_{omax}$ is the maximum output current of the gate driver, $R_{Gint}$ is the internal gate resistance of the SiC MOSFET.

(2) Stage-II ($t_1$~$t_2$):

In this stage, $I_{DS}$ reachs load current $I_{Load}$, the diode begins to recover, causing a current overshoot $I_{OS}$ in SiC MOSFET. The value of $I_{OS}$ can be expressed as:

$$I_{OS} = \sqrt{Q_{rr} \left.\frac{dI_{DS}}{dt}\right|_{I_{DS}=I_{Load}}} \quad (8)$$

where $Q_{rr}$ is the reverse recovery charge of the diode. According to (7), the value of $I_{OS}$ is directly proportional to $dI_{DS}/dt$ at the moment when $I_{DS}$ reachs to $I_{Load}$. Therefore, AGD should change gate resistance from $R_{GON\_1}$ to a larger resistance $R_{GON\_2}$ to suppress the $I_{OS}$. To ensure that $I_{OS}$ does not exceed the acceptable range, $R_{GON\_2}$ should satisfy the following formula:

$$R_{GON\_2} \geq 2\sqrt{k_{fs} I_{DS}} \frac{Q_{rr}}{I_{OS\_max}^2} \left.\frac{U_{CC} - U_{th} - \sqrt{\frac{I_{DS}}{k_{fs}}}}{C_{GS}}\right|_{I_{DS}=I_{Load}} \quad (9)$$

where $I_{OS\_max}$ is the maximum acceptable current overshoot.

(3) Stage-III ($t_3$~$t_4$):

In this stage, $C_{GS}$ is discharged by $U_{EE}$ through $R_{GOFF}$, as shown in Fig.5 (b). When the $U_{GS}$ drops to the miller plateau voltage $U_{miller}$, $U_{DS}$ begins to rise, and the $dU_{DS}/dt$ can be expressed as:

$$\frac{dU_{DS}}{dt} = \frac{U_{miller} - U_{EE}}{R_{GOFF} C_{GD}} \quad (10)$$

This formula indicates that the control over $dU_{DS}/dt$ can be achieved by adjusting $R_{GOFF}$.

In this stage, the rise of $U_{DS}$ leads the overlap between $U_{DS}$ and $I_{DS}$, resulting in primary turn-off loss $E_{off}$. Similar to Stage-I, a small resistance should be selected by AGD to increase $dU_{DS}/dt$, thereby reducing the switching loss. The selection of $R_{GON\_1}$ is constrained by maximum sink current of the gate driver:

$$R_{GOFF\_1} = \frac{U_{CC} - U_{EE}}{I_{smax}} - R_{Gint} \quad (11)$$

where $I_{omax}$ is the maximum sink current of the gate driver.

(4) Stage-IV ($t_4$~$t_5$):

In this stage, $U_{DS}$ reachs bus voltage $U_{DC}$, and the diode conducts, while simultaneously the channel current $I_{CH}$ of SiC MSOFET drops rapidly. Similar to the turn-on transient, the $dI_{CH}/dt$ can be expressed as:

$$\frac{dI_{CH}}{dt} = 2k_{fs}\sqrt{\frac{I_{DS}}{k_{fs}}} \frac{U_{EE} - U_{th} - \sqrt{\frac{I_{CH}}{k_{fs}}}}{R_{GOFF} C_{GS}} \quad (12)$$

In the turn-on transient, $I_{DS}$ is considered to be approximately equal to $I_{CH}$. However, in the turn-off transient, due to the rapid change in $U_{DS}$, the current of $C_{DS}$ and $C_{GD}$ can not be neglected. Therefore, the $dI_{DS}/dt$ should be expressed as:

$$\frac{dI_{DS}}{dt} = \frac{dI_{CH}}{dt} + \frac{dI_{CGD}}{dt} + \frac{dI_{CDS}}{dt} \quad (13)$$

The rapid decrease of $I_{DS}$ will induce a voltage in the power loop parasitic inductance $L_{Loop}$, causing voltage overshoot $U_{OS}$ in the SiC MOSFER:

$$U_{OS} = L_{Loop} \frac{dI_{DS}}{dt} \quad (14)$$

In order to suppress the voltage overshoot, AGD should change gate resistance from $R_{GOFF\_1}$ to a larger $R_{GOFF\_2}$ to reduce the $dI_{DS}dt$. The $R_{GOFF\_2}$ should satisfy that the $U_{OS}$ does not exceed acceptable range:

$$R_{GOFF\_2} \geq \frac{2L_{loop}\sqrt{k_{fs} I_{DS}}}{C_{GS}} \frac{\left|U_{EE} - U_{th} - \sqrt{\frac{I_{DS}}{k_{fs}}}\right|}{U_{OS\_max} - L_{loop}\left(\frac{dI_{CGD}}{dt} + \frac{dI_{CGD}}{dt}\right)} \quad (15)$$

where $U_{OS\_max}$ is the maximum acceptable voltage overshoot.

In the aforementioned analysis, a mathematical model has been established to determine the driving resistance within the AGD. The mathematical formulas will be validated in the next section.

# 3 Verification of Mathematical Model

In Section II, a series of mathematical formulas is utilized to describe the switching transient of the SiC MOSFET, among which four formulas are crucial for the design of AGD, namely (6), (8), (13), and (14). In this section, this paper experimentally verifies these four formulas based on Fuji 3.3kV-750A SiC MOSFET module, and the relevant parameters are summarized in Tab. I. In Tab. I, the parameters related to SiC MOSFET are derived from the manufacturer's datasheet and actual experimental results.

**Tab. I:** Relevant parameters in the experiment

| | | | |
|---|---|---|---|
| $C_{GS}$ | 100 nF | $k_{fs}$ | 36 S |
| $C_{GD}$ | 0.04 nF | $U_{th}$ | 4.7 V |
| $C_{DS}$ | 3.5 nF | $L_{Loop}$ | 150 nH |
| $Q_{rr}$ | 9.2 nC | $R_{Gint}$ | 7.5 Ω |

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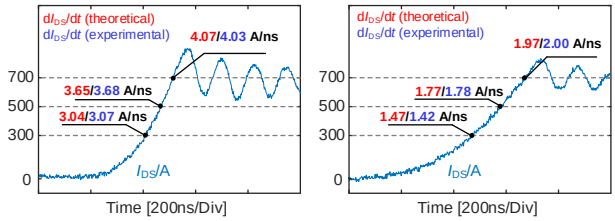
## 3.1 Verification of Mathematical Model in stage I and II

Formula (6) and (8) describe the current behavior of the SiC MOSFET during the turn-on transient. This paper conducts experiments under different external gate resistance of 1Ω and 10Ω, respectively. After measuring the turn-on current waveforms, the actual $dI_{DS}/dt$ is obtained. Subsequently, these values are compared with the one calculated using (6). The experimental waveforms are shown in Fig. 6. The experimental results demonstrate a high degree of consistency with the calculated values, confirming the correctness of (6).

A similar process is used to validate (8). The turn-on waveforms of the SiC MOSFET with varying driving resistances are measured and depicted in Fig. 7. The experimental values of current overshoot are measured and compared with the calculated values obtained from (8). A high degree of consistency can be observed, thus the effectiveness of (8) is validated.




(a) $R_G$=1Ω (b) $R_G$=10Ω

**Fig. 6:** Turn-on current waveforms under different driving resistances ($U_{DC}$=1500V, $I_{Load}$=700A)

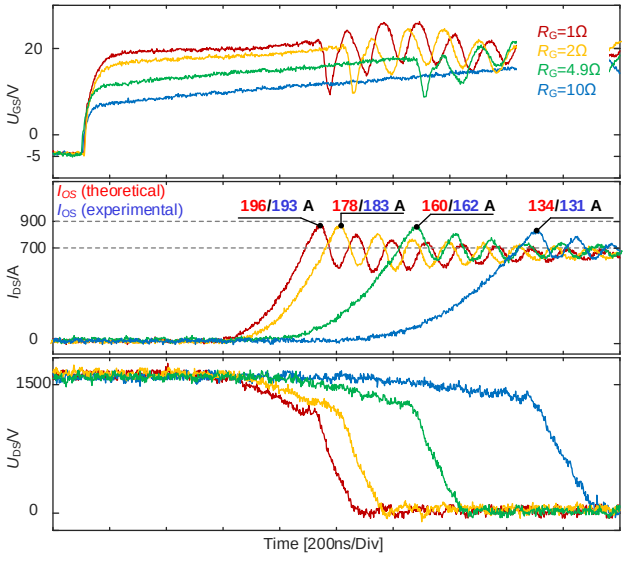



**Fig. 7:** Turn-on waveforms under different driving resistances ($U_{DC}$=1500V, $I_{Load}$=700A)

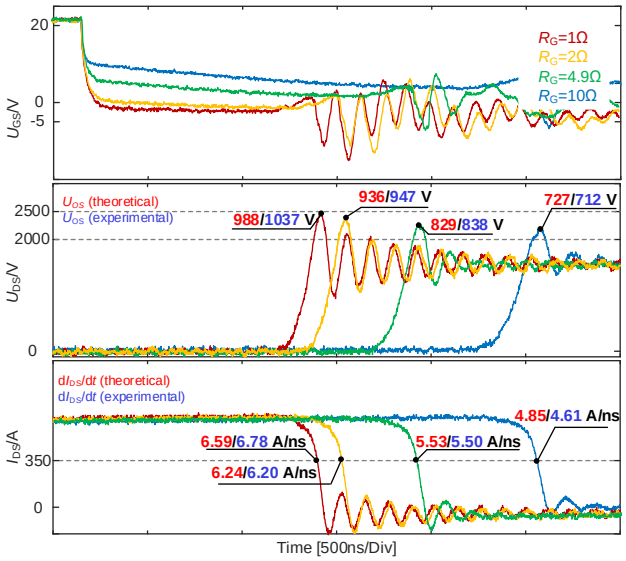



**Fig. 7:** Turn-on waveforms under different driving resistances ($U_{DC}$=1500V, $I_{Load}$=700A)

## 3.2 Verification of Mathematical Model in stage III and IV

## 3.3

Formula (13) describe the current behaviour of the SiC MOSFET during the turn-off transient. It should be noted that due to high $dU_{DS}/dt$ in Stage-I, causing $I_{DS}$ and $I_{CH}$ to have already decreased at the beginning of Stage-II. Therefore, in (13), the value of $I_{CH}$ is not 700A. Through a serious a double-pulse tests, it is found that $I_{DS}$ begins to drop rapidly when it approximately 450A. Since $I_{CH}$ is slightly less than $I_{DS}$, the value of $I_{CH}$ is approximately equal to 400A.

Additionally, to obtain $dI_{DS}/dt$, $dI_{CGD}/dt$ and $dI_{CDS}/dt$ must be taken into account. $dI_{CGD}/dt$ and $dI_{CDS}/dt$ are primarily determined by the resonance between the $L_{Loop}$ and the SiC MOSFET's output capacitance $C_{OSS}$ ($C_{OSS}=C_{GD}+C_{DS}$), and are less affected by the driving resistance. In the calculations of (13), the sum of $dI_{CGD}/dt$ and $dI_{CDS}/dt$ is approximated to be 3.2A/ns.

Finally, by substituting the aforementioned data into (13), the $dI_{DS}/dt$ under various driving resistances can be determined, and the voltage overshoot $U_{OS}$ can be calculated by (14) simultaneously. After comparison, it can be observed in Fig. 8 that the theoretical values are very close to the actual values, confirming the validity of (13) and (14).

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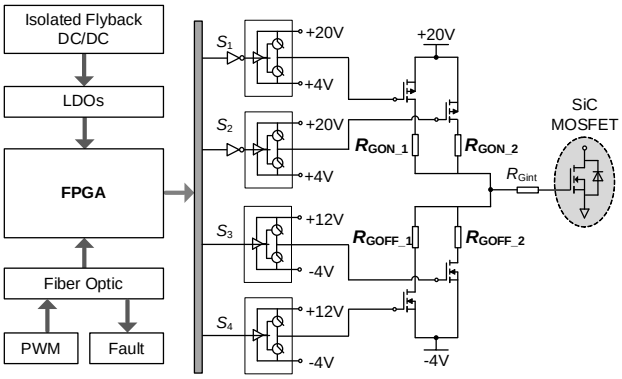


**Fig. 8:** Architecture diagram of designed active gate driver

# 4 Designed AGD and Experimental Verification

## 4.1 Parameters of Designed Active Gate Driver

In this section, a design demo of AGD tailored for Fuji 3.3kV SiC MOSFET module is presented. As shown in Fig. 8. The values of $R_{GON\_1}$ & $R_{GON\_2}$ and $R_{GOFF\_1}$ & $R_{GOFF\_2}$ can be calculated by (7), (9), (11), (15).

In order to reduce switching loss, $R_{GON\_1}$ and $R_{GOFF\_1}$ should be as small as possible. However, its values are limited by $I_{omax}$ and $I_{smax}$ of gate driver. In this paper, both $I_{omax}$ and $I_{smax}$ are set about 2.8A. Therefore, according to (7) and (11), the values of $R_{GON\_1}$ & $R_{GOFF\_1}$ can be calculated respectively:

$$R_{GON\_1} = \frac{U_{CC} - U_{EE}}{I_{omax}} - R_{Gint} = 1.07\Omega$$
$$R_{GOFF\_1} = \frac{U_{CC} - U_{EE}}{I_{smax}} - R_{Gint} = 1.07\Omega \quad (16)$$

Therefore, $R_{GON\_1}$ and $R_{GON\_2}$ are set to be 1Ω.

In this paper, the experimental conditions are set at 1500V/700A. To ensure the safety of the MOSFET, the AGD should limit the $I_{OS}$ and $U_{OS}$ to within 22% of rated values, meaning that $I_{OS}$ should not exceed 165A, and $U_{OS}$ should not exceed 726V. Thereby, according to (9) and (15), $R_{GON\_2}$ & $R_{GOFF\_2}$ can be determined:

$$R_{GON\_2} \geq 4.18\Omega$$
$$R_{GOFF\_2} \geq 10.11\Omega \quad (17)$$

(17) determines the lower limiation of $R_{GON\_2}$ and $R_{GOFF\_2}$. To ensure that the $dI_{DS}/dt$ in Stage-II and Stage-IV is adequately suppressed, this paper selects 10Ω and 15Ω as the values of $R_{GON\_2}$ and $R_{GOFF\_2}$.

## 4.2 Experimental Verification

To verified desigend AGD and proposed methods, a doubule pulses test plaftorm is established, as shown in Fig. 9. All expereiments are conducted under conditions of 1500V/700A.

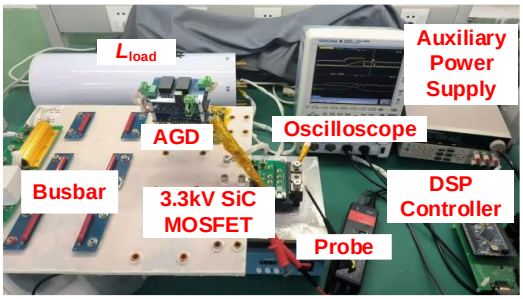


**Fig. 9:** Physical diagram of high-voltage double pulse test platform

The comparative experiment between AGD and CGD was conducted to verify the effectiveness of AGD. The waveforms of turn-on transient are shown in Fig. 10, and the turn-on performances are summaried in Tab. II. As shown in Fig. 10, during current rise stage (Stage-I), AGD has a high $dI_{DS}/dt$ nearly identical to that of the CGD when $R_G$ is 1Ω. Thus, the switching loss reduction is realized. During current overshoot stage (Stage-II), AGD changes driving resistance from $R_{GON\_1}$ to $R_{GON\_2}$ to suppress $dI_{DS}/dt$. At the point of $I_{DS}$ is 700A, the $dI_{DS}/dt$ of AGD is about 2.78A/ns, which is significantly less than the 4.00A/ns of the CGD when $R_G$ is 1Ω. Thus, the $I_{OS}$ of AGD is limited within 165A, verifying the effectiveness of the $R_{GON\_2}$ calculated by (9) in current overshoot suppression.

To demonstrate the role of AGD in loss reduction, CGD with $R_G$ of 4.9Ω is used for comparison with AGD. According to Tab. II, the both AGD and CGD exhibit $I_{OS}$ approximately 160A, thus a fair comparison is ensured. Compared with CGD when $R_G$ is 4.9Ω, AGD can reduce turn-on loss by 14.8%.

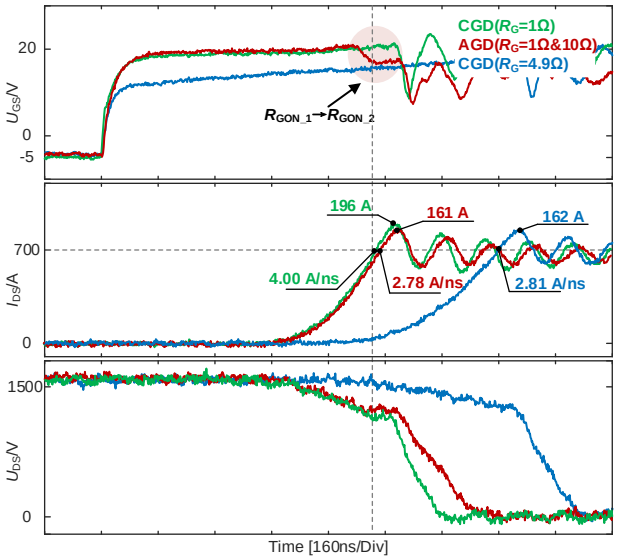


**Fig. 10:** Turn-on waveforms of AGD and CGD under 1.5kV/700A

 

**Tab. II:** Comparisons of turn-on performances between CGD and AGD under 1.5kV/700A

| Performances | Turn-on loss | $I_{OS}$ |
|---|---|---|
| CGD (1Ω) | 187 mJ | 196 A |
| CGD (4.9Ω) | 276 mJ | 162A |
| AGD (1&10Ω) | 235 mJ | 161 A |

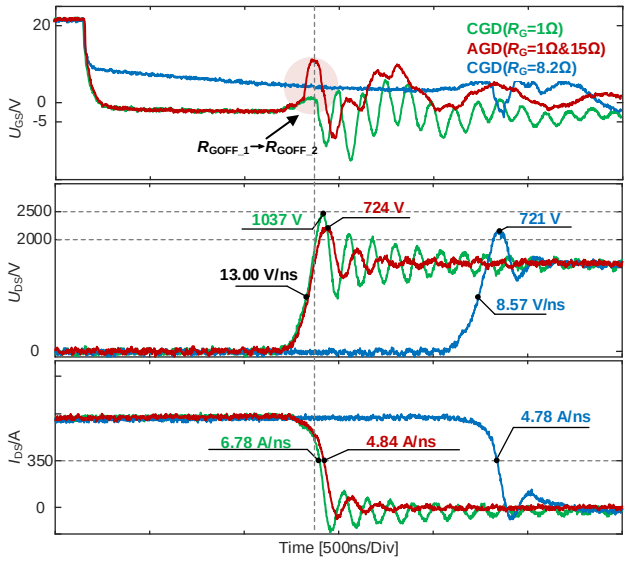


**Fig. 11:** Turn-on waveforms of AGD and CGD under 1.5kV/700A

**Tab. III:** Comparisons of turn-off performances between CGD and AGD under 1.5kV/700A

| Performances | Turn-on loss | $U_{OS}$ |
|---|---|---|
| CGD (1Ω) | 104 mJ | 1037 V |
| CGD (8.2Ω) | 148 mJ | 721 V |
| AGD (1&15Ω) | 113 mJ | 724 A |

Fig. 11 depicts the turn-off waveforms of AGD and CGD. It is obvious that during the voltage rise stage (Stage-III), AGD possesses the same high d$U_{DS}$/dt as the CGD with $R_G$ is 1Ω, reducing turn-off switching loss significantly. During the voltage overshoot stage (Stage-IV), $R_{GON\_2}$ is selected by AGD instead of $R_{GOFF\_1}$, thereby lower d$I_{DS}$/d$t$ is achieved to suppress voltage overshoot. As shown in Fig. 11, $U_{OS}$ of AGD is successfully limited to within 726V, verifying the effectiveness of RGON_2 calculated by (15) in voltage overshoot suppression.

In order to verify that AGD can reduce turn-off loss, a CGD with $R_G$ of 8.2Ω is used for a fair comparison. According to Tab. III, both AGD and CGD exhibit $U_{OS}$ around 725V. However, the turn-off loss caused by CGD is 148mJ, while the loss caused by AGD is only 113mJ, meaning that AGD can reduce turn-off loss of SiC MOSFET by 23.6%.

Finally, Tab. II and Tab. III demonstrate that AGD can achieve a 17.9% reduction in switching loss while keeping the same electrical stress with CGD.

# 5 Conclusion

In this paper, an AGD particularly tailored for the Fuji 3.3kV-750A SiC MOSFET module is designed, aiming for a reduction in switching loss without compromising the electrical stress. Firstly, the mechanisms behind overshoot and switching loss of SiC MOSFET are analyzed, indicating that SiC MOSFET switching characteristics can be optimized by regulating driving resistances at different stages of the switching transient. Subsequently, a mathematical model is fromulated to calculate the values of driving resistances in AGD. Finally, a double-pulse test platform is established to test the designed AGD. Experimental results show that a 17.9% reduction in switching loss is achieved by AGD under 1500V/700A, demonstrating the effectiveness of the mathematical model proposed in this paper.

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