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New 400 V SiC MOSFET technology delivering highest efficiency in three-level industrial drive applications

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Abstract

With the introduction of the first commercially available 400 V SiC MOSFET technology, a longstanding gap between 200 V medium-voltage MOSFETs and 600 V super-junction MOSFETs has been closed. Offering low switching losses and low on-state resistance, the technology is a perfect fit for 3-level (3L) topologies.

This work briefly introduces the device concept, and studies the performance in a 3-level 3-phase AC driven general purpose industrial drive in ANPC configuration, working with up to 800 VDC blocking voltage.

1 Introduction

Currently, there is no competitively available solution that addresses the market around 400 V. Scaling-up existing medium-voltage 200 V MOSFETs that employ lateral charge-compensation by means of an isolated deep field-plate is not ideal. Similarly, scaling-down existing 600 V SJ MOSFET technologies is problematic. In both cases, the application performance suffers from the compromises originating from the specific device set-ups, namely large input-, output- and reverse-recovery charges, and a pronounced drop in the output- and Miller-capacitance over drain voltage. These device properties prevent the devices finding common usage in hard-switching half- or full-bridge topologies.

2 Device Concept

2.1 Device structure considerations

Wide band-gap semiconductors based on silicon-carbide are very attractive for power devices due to their low losses, improved temperature capability and high thermal conductivity, and have recently developed into a mature technology. While the use of a wide-bandgap material such as silicon carbide offers many advantages over silicon, there are some noteworthy differences. This leads to a number of challenges when employing the 4H-SiC polytype which is the most prominent silicon-carbide polymorph used for power semiconductor devices:

- SiC has a higher surface density of atoms per unit area compared to Si, resulting in a higher density of dangling Si- and C- bonds and carbon clusters at the interface. Defects located in the gate oxide layer near to the interface may appear in the energy gap and act as traps for electrons [1].
- SiC devices allow much higher drain-induced electric fields in the blocking mode compared to their Si counterparts and thus require a limitation of the electric field in the gate oxide to maintain reliability [2].
- SiC devices show a higher Fowler-Nordheim current injection compared to Si devices due to a smaller barrier height, consequently the electric field on the SiC side of the interface must be limited [3],[4].

Consequently, one challenge of SiC MOSFETs is the low electron mobility at the SiO_2/SiC interface due to carbon related interface defects. Due to electron scattering and trapping at such point defects at the interface, the channel mobility is typically only a fraction of the bulk mobility of ca. 400 cm²/Vs (the value at a bulk doping level equal to the channel doping) [5]. Another challenge is the 4° off-axis tilt of commercially available SiC substrates. This is a consequence of the need for epitaxial layer growth. Due to this tilt, the wafer surface

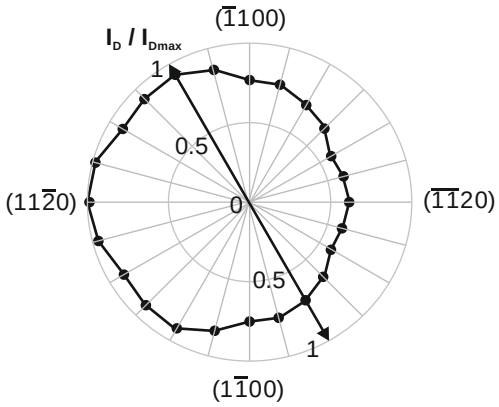

Fig. 1 Relative channel mobility for various trench planes of 4H-SiC on-axis substrate [6]

does not perfectly coincide with the (0001) crystal c-plane, causing increased surface roughness and steps when fabricating a MOS structure at the wafer surface.

This off-axis cut obviously imposes a challenge on devices using a lateral channel and will have a strong impact on the channel properties in addition to the usual limitations imposed by the cell pitch shrink. Nevertheless, the off-axis cut also affects trench MOSFET technologies, as a vertically etched trench will result in side walls with different roughness, performance and reliability.

Studies showed that the vertical channel mobility strongly depends on the crystal plane with a factor of almost two between worst and best channel mobility as indicated in Fig. 1 [6]. A suitable post-oxidation annealing step like a nitric oxide annealing can reduce the interface state density significantly [7]. The conditions of the post oxidation anneal (POA) also affect the stability of the threshold voltage. An optimized POA provides high channel mobility and high threshold voltage stability at the same time.

The limitation of the electric field strength in the blocking state is addressed by appropriate device design measures like a buried shielding region.

2.2 400 V Trench MOSFET structure

The general device structure follows the design approach introduced previously [8],[9]. Fig. 2 gives a schematic cross section of the general cell concept. The active channel aligns along the a-plane which gives the best channel mobility and the lowest interface trap density. The gate oxide is protected by deep p-wells that are connected to the source electrode at the semiconductor surface. As the other trench sidewall does not coincide with this crystal plane, it is not used as an active channel. Instead, the buried p-region is connected to the source electrode along the inactive sidewall. This leads to a very compact cell design and, in combination with the high channel mobility of the a-plane, to a low area-specific on-resistance.

While the new 400 V MOSFET is similar to the previously introduced designs of the first device generation [9],[10], it benefits from the continuous improvements of the technology that for example enable a clearly reduced cell pitch and further improved channel properties or improved control over the drift region properties. Additionally, the chip design is carefully optimized to avoid any unnecessary active area loss, for example by the optimization of the junction termination design.

2.3 Device properties

As a typical example, Fig. 3 indicates the most important device property improvements of the new CoolSiC™ 400 V device over a 650 V reference device of the same technology generation, with an identical chip size in a common TO-263-7 (D2PAK 7pin) package. All values are averaged over a batch of devices to account for typical production variations.

The comparison clearly reveals lower values and overall excellent technology figure-of-merit (FOM) improvements for the 400 V technology, indicating the potential of this new voltage class. The substantially lowered on-resistance values again underline the advantages of a trench technology, which benefits from a much better channel mobility compared to typical DMOS devices with a lateral channel. The indicated FOM describes the product of the on-resistance with the respective charge, e.g. $FOM_g = R_{DS(on)} \times Q_g$ etc. The FOMg is related to the total gate charge required to turn-on the transistor and affects the driving losses. The FOMgd is associated with the gate-drain-charge that governs the drain voltage transient and correlates with the switching losses. FOMoss is linked to the output charge of the MOSFET, while FOMEoss goes with the energy stored in the output charge.

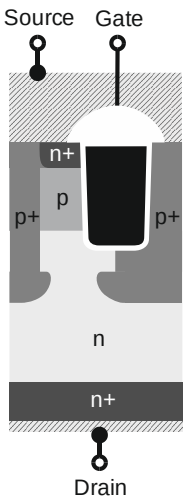

Fig. 2 SiC Trench MOSFET concept with an asymmetric channel

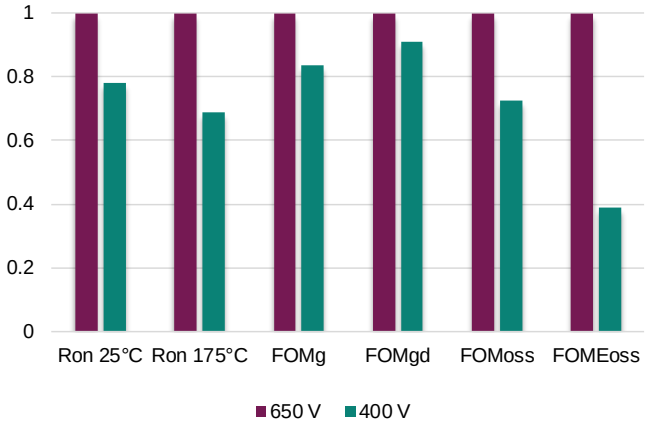

Fig. 3 Comparison of performance parameters of the 400 V and 650 V MOSFET

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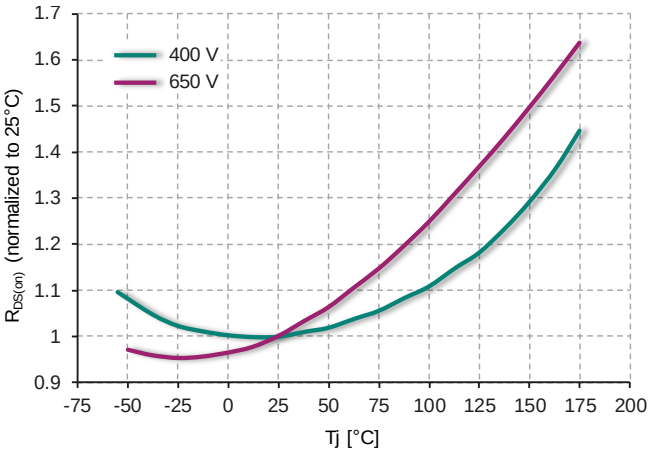

Fig. 4 Temperature dependence comparison of normalized on-resistance

These excellent parameters are complemented by a rather flat temperature dependence of the on-resistance $R_{DS(on)}$ as shown in Fig. 4. The value only increases by 11% from 25°C to 100°C in the case of the new 400 V device. This property allows a MOSFET with higher $R_{DS(on)}$ to be chosen, with the benefit of lower costs and better switching performance.

3 Test results in 3L ANPC inverter

3.1 Advantages of the 3-Level topology

The new devices are ideal for converting grid-connected applications with 3-phase / 400 VAC into a DC link voltage of 560 V after rectification. Currently these applications typically use 1200 V semiconductors in a 2-level topology as there is no other choice.

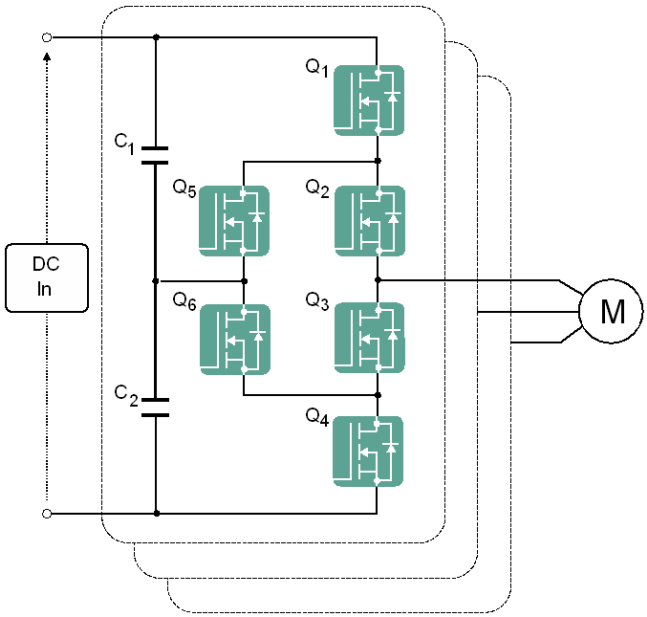

Fig. 5 Simplified basic schematic of the 3-phase 3L ANPC Inverter

The three-level active neutral point clamp (3L ANPC) topology [11] as depicted in Fig. 5 enables the use of 400 V devices. The DC capacitor bank divides the DC link voltage, therefore each half-bridge sees half of the DC link voltage. This topology, when employing 400 V devices, allows a maximum blocking capability of 800 V, and in addition offers a bidirectional energy transfer. The higher DC link bus voltage contributes to efficiency improvements and increased power density, reduces PCB copper content and eliminates the need for paralleling of devices.

However, there are further benefits of the 3L ANPC topology. As lower voltages over the devices are applied, a better switching performance is achieved, which enables a higher overall efficiency and output power. Due to the slower dv/dt and the use of three different voltage levels, EMI behavior improves.

3.2 Introduction of the test board

The device performance is studied in a medium-power 3-phase 3L ANPC inverter as depicted in Fig. 6. The inverter is equipped with 18x 11 mΩ 400 V SiC MOSFET in TOLL packages and can handle peak power levels up to 20 kW. The board offers a high reliability due to the absence of a need for paralleling.

The gate driver, which provides 18 isolated gate drive voltages, uses a reliable and cost-efficient solution based on a planar transformer. The forward converter requires just one input to drive all 18 isolated outputs.

To drive the 3L ANPC topology, one can select between three different modulation (control) schemes as depicted in Fig. 7.

In case of 4H2L modulation, Q2 is entirely turned-on during the positive half-cycle. Q1 and Q5 switch alternately, with Q1 controlling the duty cycle and phase voltage while Q5 acts as a synchronous rectifier. In the negative half-cycle, Q3 is turned-on completely. Now Q4 and Q6 switch alternately, with Q4 controlling the duty cycle and phase voltage and Q6 acting as a synchronous rectifier. The load will see the difference between the AC input voltage and the neutral point. This modulation scheme allows for an easy board layout and enables a uniform heat distribution between the devices.

The 6H0L modulation scheme works similarly, but with the advantage of sharing the freewheeling current during the freewheeling time between two devices. During the positive half-cycle, Q2 and Q6 are turned-on completely, and Q1 is switching during the power transfer. Q3 and Q5 are operated as synchronous rectifiers. At the negative half-cycle, Q2 and Q6 are turned-on and Q4 switches during the power transfer. Q3 and Q5 again operate as synchronous rectifiers. Also for this modulation type, the load will see the difference between the AC input voltage and the neutral point. The

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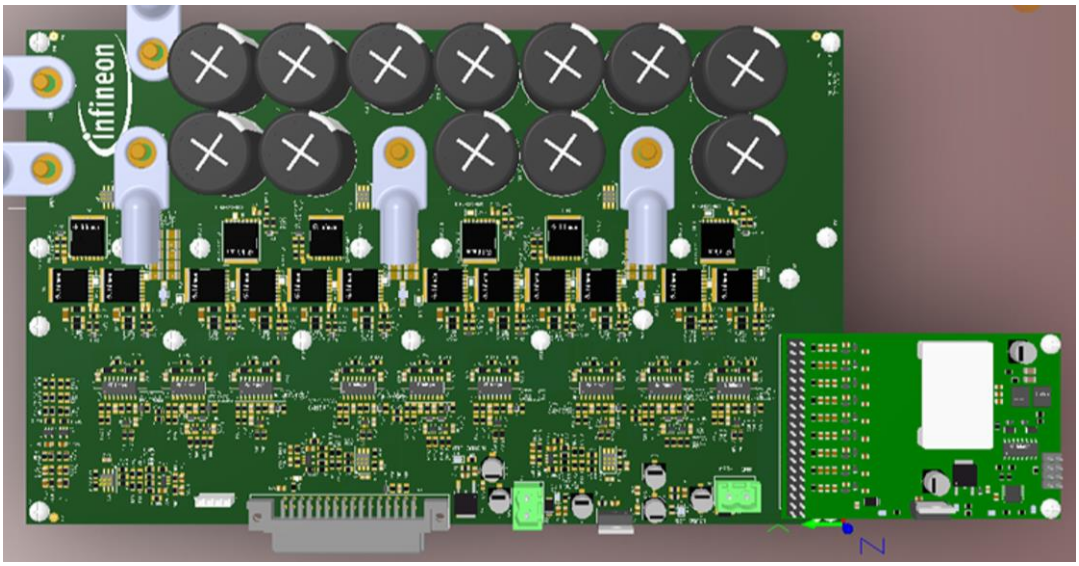

Fig. 6 The 3-phase 3L ANPC test board with attached gate driver

disadvantages of this scheme are that it requires a complex board layout and leads to a non-uniform heat distribution between the MOSFETs (Q1 and Q4 will became hotter than the other devices). Compared to the 4H2L modulation, power losses are slightly lower.

In case of the 2H4L modulation scheme, Q2 and Q3 need to switch fast. Q1 and Q6 are turned-on over the entire positive half-cycle, and Q2 switches during the power transfer. Q3 works as a synchronous rectifier. During the negative half-cycle, Q4 and Q5 are turned-on. Q3 switches during the power transfer and Q2 is operated as a synchronous rectifier. The load again sees the difference between the AC input voltage and the neutral point. From all three options, this modulation scheme results in the worst heat distribution, as Q2 and Q3 will heat-up significantly more than the other devices.

On the other hand, as only two devices operate with a high switching frequency, IGBTs could be used for the other switches. This offers an option for a cost-efficient solution, but the overall efficiency will decrease for such a configuration.

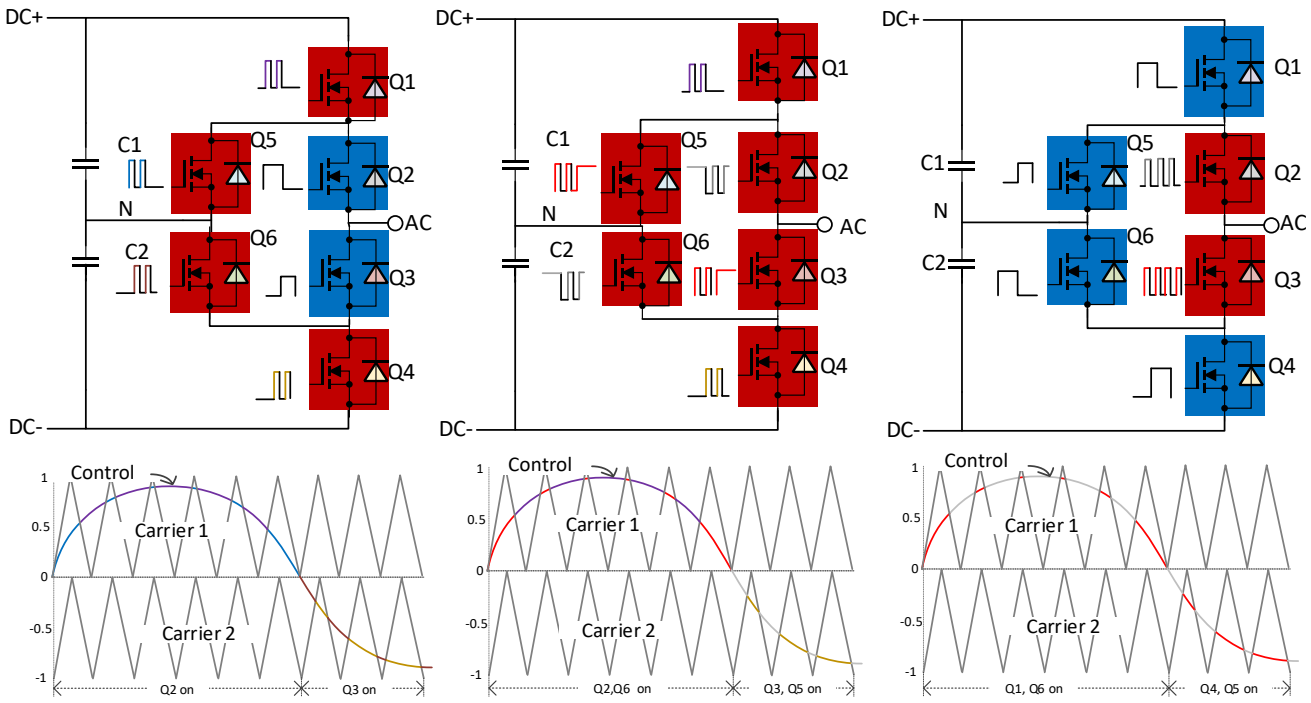

Fig. 7 Comparison of the possible modulation schemes: 4H2L modulation (left), 6H0L modulation (center) and 2H4L modulation (right)

For the test board, 4H2L modulation is selected due to the uniform temperature distribution between the MOSFETs and the lowest layout complexity.

3.3 Application test results

For the application tests, the inverter runs at a switching frequency of 10 kHz and limits the dv/dt per switch to 5 V/ns. Measurements were done at an inductive-resistive load (1 mH + variable resistance). During the tests, the heatsink was not connected, and a thermal camera measured the temperature of the whole board area. To analyze the performance, a Yokogawa WT5000 Precision Power Analyzer is employed. The efficiency analysis excludes the gate drivers and controller stage. The tests use sinusoidal pulse width modulation (SinPWM).

Fig. 8 shows the measured voltage and current waveforms during turn-on and turn-off of the high-side switch, using a double-pulse configuration of the 3L ANPC test board. The measurements indicate a very smooth switching behavior.

Fig. 9 depicts the measured efficiency and the maximum case temperature depending on the output power. At V_{DC} = 600 V and a phase current of 15 A, the inverter

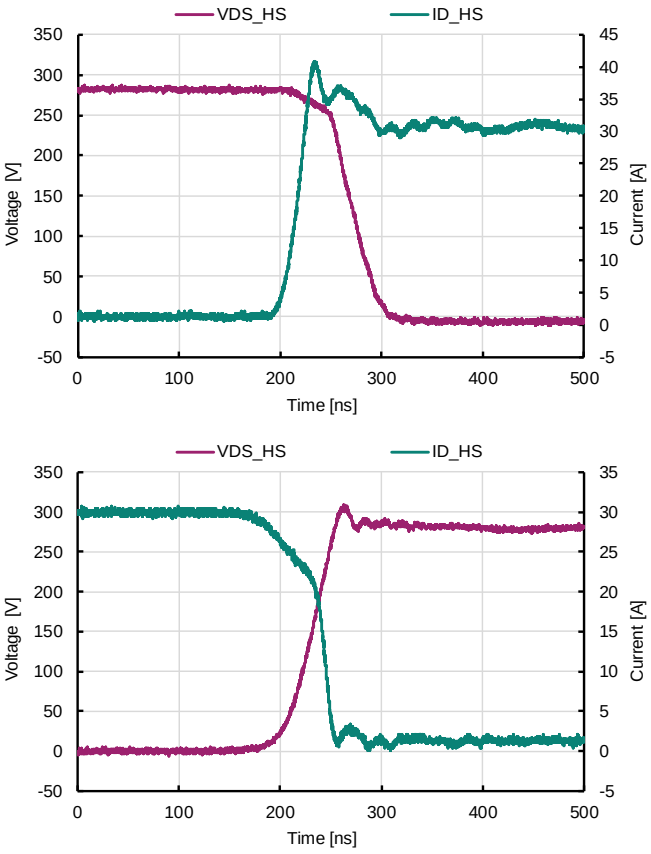

Fig. 8 Turn-on and turn-off waveforms of the high-side switch using a double-pulse configuration of the test board [V_{DS} = 300 V, I_{LOAD} = 30 A, di/dt ~ 750 A/µs, $R_{G(on)}$ = $R_{G(off)}$ = 30 Ω]

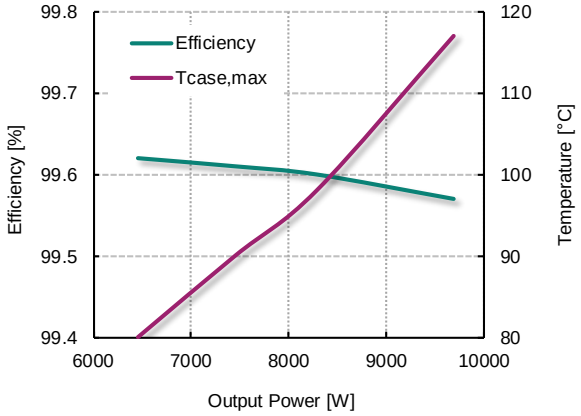

Fig. 9 Measurement of efficiency and maximum case temperature at inverter operation without heatsink [V_{DC} = 600 V, f_{sw} = 10 kHz, $R_{G(on)}$ = $R_{G(off)}$ = 30 Ω, t_{dead} = 500 ns]

delivers an efficiency of η = 99.57 % for 9.74 kVA load. Without an attached heatsink, the case temperature reached a value of 117°C, which reduced to 69°C when a heatsink is used.

4 Conclusion

This work introduces the new 400 V CoolSiC™ trench MOSFET technology, closing a longstanding gap between 200 V medium-voltage MOSFETs and 600 V super-junction and SiC MOSFETs. The new devices offer a unique combination of performance, reliability and ease of use and enable the adoption of innovative, highly efficient topologies as 3L ANPC for motor drive applications or 3L PFC for power supplies with blocking capabilities of up to 800 VDC.

The 400 V devices offer lower on-resistance and improved Figures-of-Merit compared to existing solutions and benefit from a rather flat temperature dependence of the on-resistance. Low gate-, gate-drain, output- and reverse-recovery charges provide a fast-switching capability.

The advantages of the new devices were investigated in a medium-power 3-phase 3L ANPC inverter equipped with a total of 18 MOSFETs, capable of delivering up to 20 kW output power with an attached heatsink. The results confirm the expected potential of this 400 V technology and reveal a superior inverter efficiency beyond 99.5%, despite the dv/dt limit of < 5 V/ns. As the generated heat is spread over 18 MOSFETs, the thermal management also improves.

Other potential application fields of this voltage class include battery-connected drives, which could benefit from the ability to use a higher battery input voltage of 288 V (achieved by a serial instead of parallel connection), using a simple two-level B6 topology. The reduction in currents with a higher bus-voltage will result in a lower number of paralleled MOSFETs (potentially even

eliminating the need for parallel devices), improved efficiency and significant copper reduction leading to improved power density and system-level cost improvement.

Another very attractive application is represented by the 3L Totem Pole Power Factor Correction (PFC) topology, which enables a jump in the efficiency and power density linked to a shrink in the inductor sizes as investigated in [12]. Such units pave the way for next generation AI Server and industrial SMPS with scalable solutions capable of delivering 5.5 kW to 8 kW and beyond.

5 Acknowledgements

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