ZG2100M Data Sheet

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Revision 04

Confidential

ZG2100M/ZG2101M

2.4GHz 802.11b Low Power Transceiver Module

Features

- 802.11b Solution including MAC, baseband, RF and power amplifier
- Low power operation
- 1 & 2Mbps
- API for embedded markets, no OS required
- PCB or external antenna options
- Pre-programmed MAC address
- Hardware support for AES, and TKIP (WEP, WPA, WPA2 security)
- SPI slave interface with interrupt
- Single 3.3v supply
- 21mm x 31mm 36-pin Dual Flatpack
- Wi-Fi & Regulatory (eg, FCC) certification

Applications

Consumer electronics
- Set top box
- Audio stream
- Remote controls
- Toys

PC & Portable Device Accessories
- Headsets
- Video cameras
- Keyboards and mice

Sensors/Controls
- Industrial & factory sensors
- HVAC
- Lighting
- Security and access
- Location and telemetry

Description

ZG2100M modules provide an easy to use, low power implementation of 802.11b. All RF components, the baseband, and the entire 802.11 MAC reside on-chip, enabling simple and cost-effective Wi-Fi connectivity for embedded devices. An on-chip processor hosts an API, simplifying design-in and allowing the ZG2100M or ZG2101M to be hosted by 8- and 16-bit host microcontrollers. Hardware accelerators support Wi-Fi security standards.

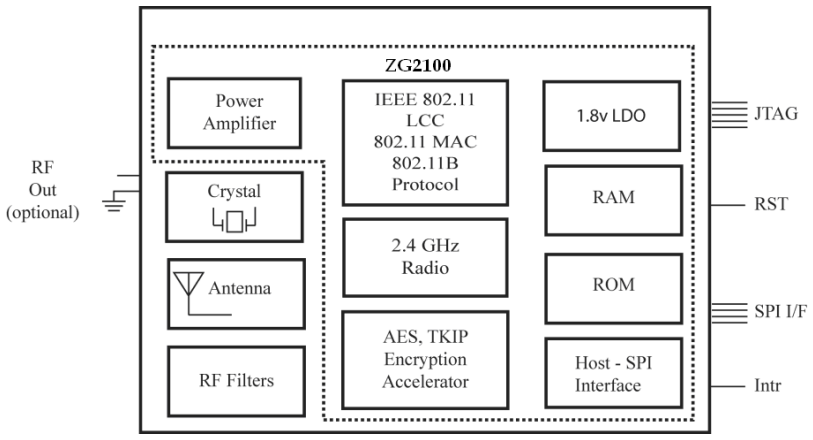

Figure 1. ZG2100M/ZG2101M Module Functional Block Diagram

Contents

1. Key Features

Ease of Software Development

- Simple API suited for embedded market
- Targeted for low resource host processors
- Entire MAC integrated on-chip with no resources required by host
- Wireless driver library provides all required control of device
- Simple usage model, no requirement for OS

Low Power Operation

- Low power, 3uA hibernate, 250uA sleep modes with fast wake up
- Sleep power state managed by ZG2100, enabling low average power while maintaining AP association without host control
- SPI slave interface with interrupt is active independent of power state

Low External Component Count

- Fully integrated RF frequency synthesizer
- Includes crystal and antenna
- On-chip LDO enables single 3.3V supply

Wi-Fi

- WiFi Certified/approved by WiFi alliance
- Supports 1Mbps & 2Mbps 802.11b
- Hardware support for WEP, WPA (PSK), and WPA2 (PSK)

RF

- Power output +10dBm typical at antenna
- Power output programmable from +0dBm to meet varying application needs
- Integrated PCB antenna (ZG2100M)
- Support for external antenna available (ZG2101M)

2. Detailed Description

2.1. Overview

The ZG2100M module incorporates the ZeroG ZG2100 single chip 802.11b transceiver with all associated RF components, crystal oscillator, and bypass and bias passives along with a printed antenna to provide a fully integrated Wi-Fi I/O solution controllable from an 8 or 16-bit processor.

The module is manufactured on an FR4 PCB substrate, with components on the top surface only. Connection is made as a surface mount component via flat pack (no pin) connections on two sides.

Electrical connections to the module consist of a single 3.3v supply and built in PCB antenna for ease of system integration and significant BOM reduction. There is also an option to supply both 1.8V and 3.3V for additional power saving and an antenna connector to use an external antenna instead of the PCB antenna. The digital interface uses a standard slave SPI connection.

2.2. ZG2100 Power States

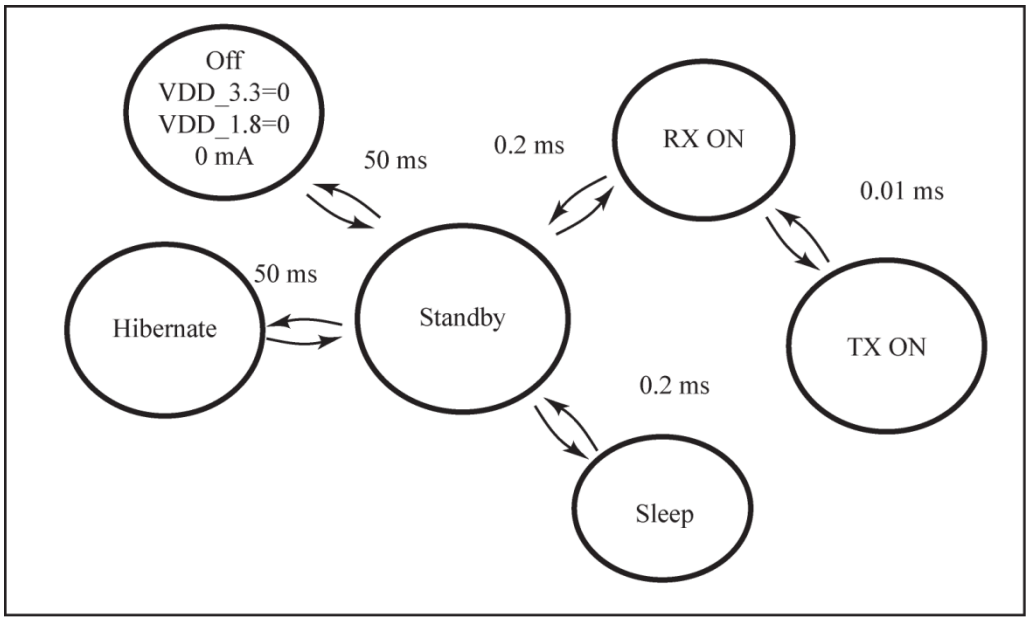

Figure 2. ZG2100M/ZG2101M Power State Diagram

The power state definitions are as follows:

Off:

- Power disconnected to ZG2100
- VDD_3.3 = 0V
- VDD_1.8 = 0V
- CE_N = 0V

Standby:

- PLL, LDO and OSC On
- VDD_3.3 = 3.3V

Hibernate:

- Core is off
- VDD_3.3 = 3.3V

Sleep:

- LDO and OSC On
- VDD_3.3 = 3.3V

Rx On:

- Receiver circuits on

Tx On:

- Transmit circuits on

Note: If VDD_1.8 is supplied externally, then CE_N must be held high (3.3V) except in the off state. If only VDD_3.3 is supplied, then CE_N must be held low (0V) except for the Hibernate state.

2.3. SPI Interface

There are two SPI interfaces on the ZG2100M/ZG2101M. One is for host control of the device and is a slave port. General references to the SPI port refer to this. The second port is a master SPI port used for FLASH for ROM image patches. The initial version of ZG2100M/ZG2101M enables loading the microcode from the on-board FLASH for startup.

The master SPI port shares pins used for test modes. Thus evaluation boards made to control a ZG2100 daughter card must allow special connection as detailed for factory debug.

2.3.1. Host Control SPI Interface

The SPI interface implements the [CPOL=0; CPHA=0] and [CPOL=0; CPHA=1] modes (0 and 3) of operation. That is, data is clocked in on the first rising edge of the clock after Chip Select goes valid.

There are two decode regions. One for register access and one for a FIFO interface. Timing for both regions is shown below. The INT_NX signal allows interrupts to be signaled to the host device.

2.3.2. SPI Register Access

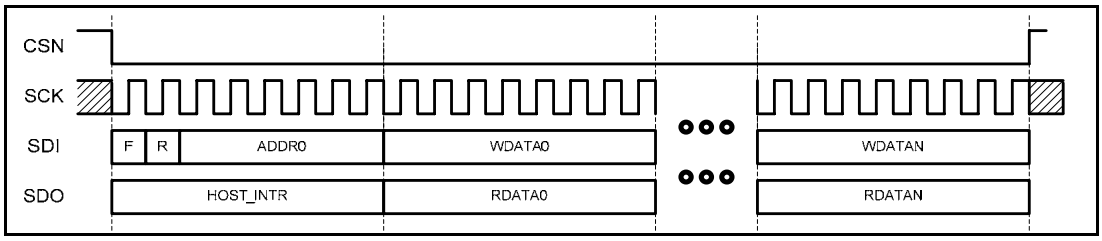

Figure 3. SPI Register Timing

F is a select between FIFO space and register space. If this bit is a 1, the data FIFO space is selected. If this bit is a 0, the register address space is selected.

R is the Read/Write bit. If this bit is a 1, the operation is a read. If this bit is a 0, the operation is a write

ADDR0 is the starting address for the transaction. This value is only used for register accesses and is ignored during FIFO accesses

WDATAn is the write data byte. This is only used from write operations and is ignored during read operations.

RDATAn is the read data byte. This is always valid for both read and write operations. If contains the current value of any register location.

HOST_INTR is the 8 bit interrupt register.

2.3.3. FIFO Interface

HOST FIFO Basic Commands

FCMD[2:0]

0x0 – RFIFO_CMD

0x1 – WCONT (Continue Previous Packet)

0x2 – WSTART0 (Start Packet, head/continue)

0x3 – WSTART1 (Start Packet, head0/continue)

0x4 – WEND CMD

0x5 – REND CMD

RSV: these fields are reserved for software microcode and are TBD at this writing.

2.3.4. FIFO Read

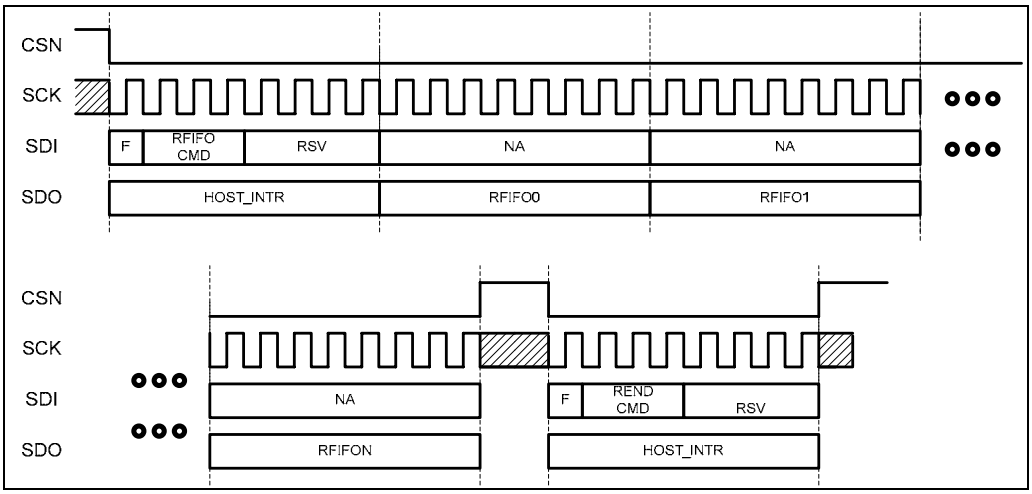

Figure 4. FIFO Read Timing

2.3.5. FIFO Write

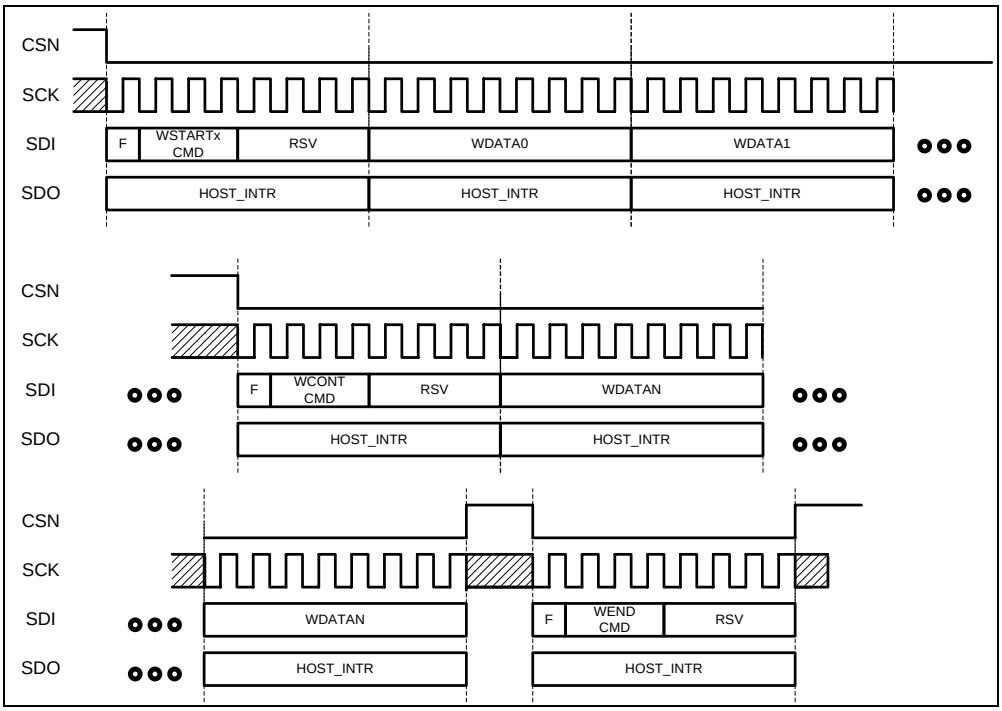

Figure 5. FIFO Write Timing

2.3.6. Host Control SPI Interface Example

As an example of any 32-bit register access, suppose a write to register 0xF0_0F18 is desired:

1. Write to host register 0x38 with addr[31:16] (0x00f0). 24 bit transaction.
2. Write to host register 0x39 with addr[15:0] (0x0F18). 24 bit transaction.
3. Write to host register 0x3a with data[31:16]. 24 bit transaction.
4. Write to host register 0x3b with data[15:0]. 24 bit transaction.
5. Write to host register 0x37 with a byte that has the following pattern: 8 bit transaction
   a. [7:4] byte enables (active high for the valid bytes that you want to write in steps 3 and 4).
   b. [3:0] - 4'b0001 -> activate write to register

For a read of 0xF0_0D00:

1. Write to host register 0x38 with addr[31:16] (0x00F0). 24 bit transaction.
2. Write to host register 0x39 with addr[15:0] (0x0F18). 24 bit transaction.
3. Write to host register 0x37 with a byte that has the following pattern: 8 bit transaction
   a. [7:4] byte enables (active high for the valid bytes that you want to read in steps 1 and 2).
   b. [3:0] - 4'b0011 -> active read of register
4. Read host register 0x3a to get data [31:24] 24 bit transaction
5. Read host register 0x3b to get data [15:0] 24 bit transaction

Each of the steps above is a single SPI transaction; the chip select is active low during each step.

2.3.7. Boot Up Sequence

The internal regulators for the digital and analog core power supplies are enabled by keeping the chip enable pin (CE_N) low. The waveforms for the core supplies are illustrated below for powering up the ZG2100M with a nominal 3.3V supply on pin VDD_3.3. There is an internal power-on-reset detect which starts the boot sequence from the internal ROM when the core supply (VDD_1.8) is up. After approximately 50 ms from when VDD_3.3 is within 10% of the 3.3V target, the ZG2100 is ready.

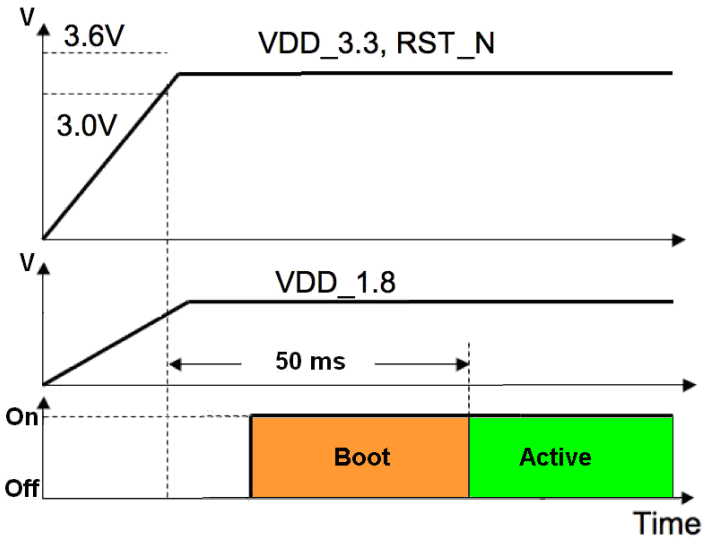

Figure 6. Boot Sequence Timing

3. Pin Out and Function

Pins	Name	Internal Bias	Required Bias resistor	Description
1	GND			Ground
2	VDD_1.8			See below
3	JTAG_TDO			JTAG data out
4	JTAG_TCK		Pull-up	JTAG Clock in
5	JTAG_TMS	H		JTAG Mode in
6	JTAG_TDI	H		JTAG data in
7	RST_N		Pull-up	Chip reset
8	DNC			Do Not Connect
9	JTAG_RST_N		Pull-down	JTAG Reset
10	GND			Ground
11	VDD_1.8			See below
12	DNC			Do Not Connect
13	DNC			Do Not Connect
14	DNC			Do Not Connect
15	DNC			Do Not Connect
16	RES			Ground
17	VDD_3.3			3.3V Power
18	GND			Ground
19	GND			Ground
20	CE_N			Chip enable
21	DNC			Do Not Connect
22	DNC			Do Not Connect
23	SCS_N			Serial chip select from host
24	VDD_1.8			See below
25	GND			Ground
26	UART_RX	H		Debug Serial in
27	UART_TX			Debug Serial out
28	GND			Ground
29	VDD_3.3			3.3V Power
30	GND			Ground
31	VDD_1.8			See below
32	SDO			Serial data out to host
33	INT_NX		Pull-up	Interrupt to host
34	SCK			Serial clock in from host
35	SDI	H		Serial data in from host
36	GND			Ground

Note: VDD_1.8 is an optional 1.8v core supply input rail. Use of this rail may provide better system power consumption versus using the modules internal LDO to create the supply. These pins can be left unconnected. **DO NOT USE** these pins to drive other components. For more information on supplying your own 1.8v rail, please contact the factory.

* SDI pullup used to prevent leakage during tri-state conditions. If Host biases this signal during non-use, ensure bias is high.

RES is used as write-protect for the internal module SPI Flash. For production use, this pin should be grounded. For prototype development, this pin may be pulled high to allow for reprogramming.

4. Package Information

4.1. Module Drawing

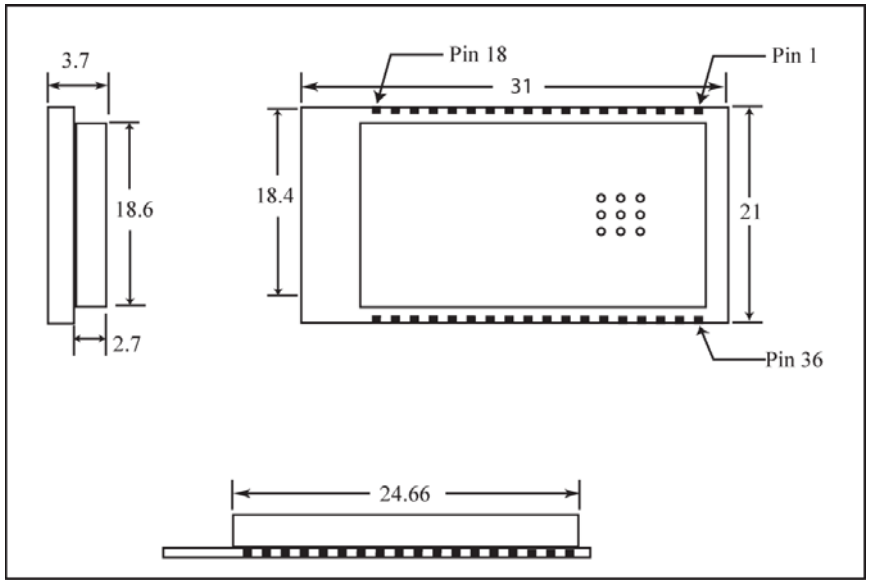

Figure 7. ZG2100 Module Physical Dimensions

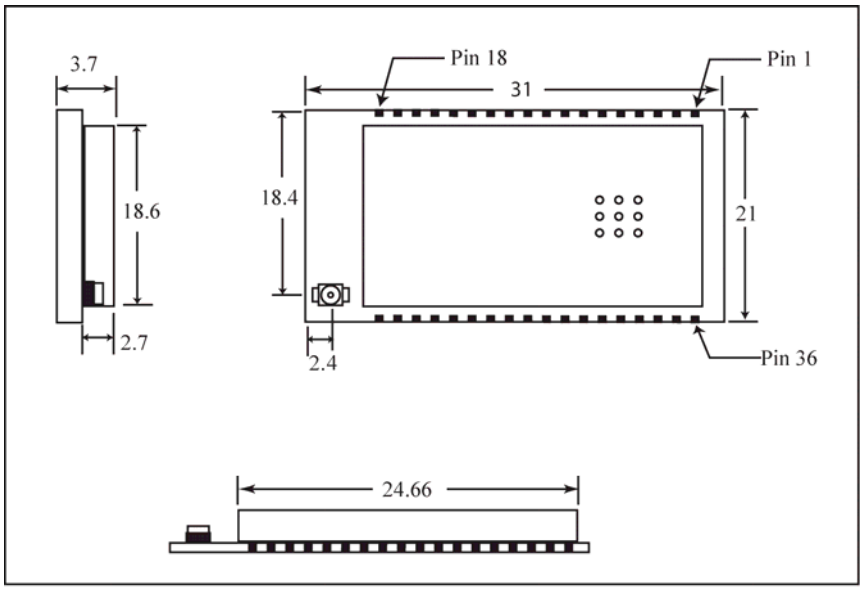

Figure 8. ZG2101 Module Physical Dimensions

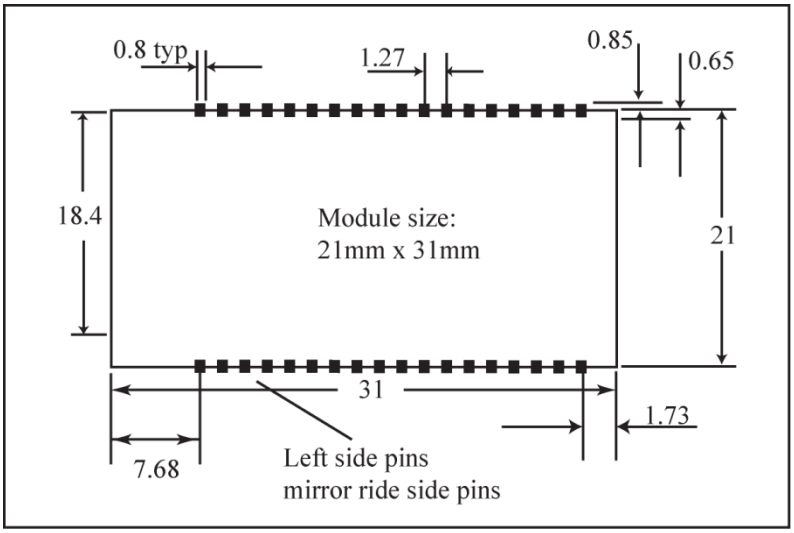

Figure 9. Module Layout Pad Dimensions

4.2. Module Layout Guidelines

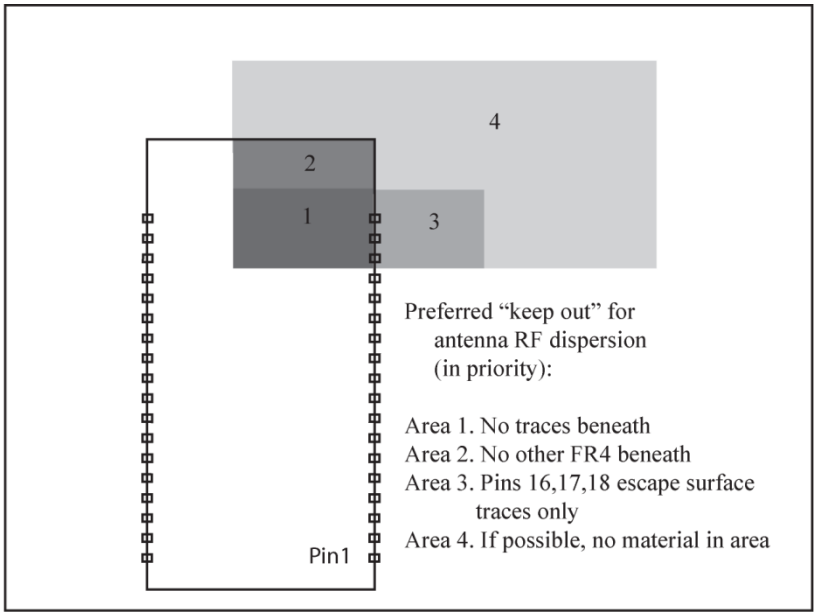

Figure 10. Module "Keep Out" Areas

In addition to the guidelines in Figure 10, note the following suggestions:

- Bypass capacitors for 3.3V should be close to pin 17.
- Routing under the module except for limits shown in Figure 10 is acceptable if they are solder masked.
- Do not route any nets to VDD_1.8 unless sourcing this supply externally (i.e. not using our internal LDO)
- Do not use VDD_1.8 to source any external nets.
- There are 4 test points under the pre-production module -- these do not need routing, but should be protected from any nets (i.e. use solder mask for nets under module)

4.3. Module Use Schematic

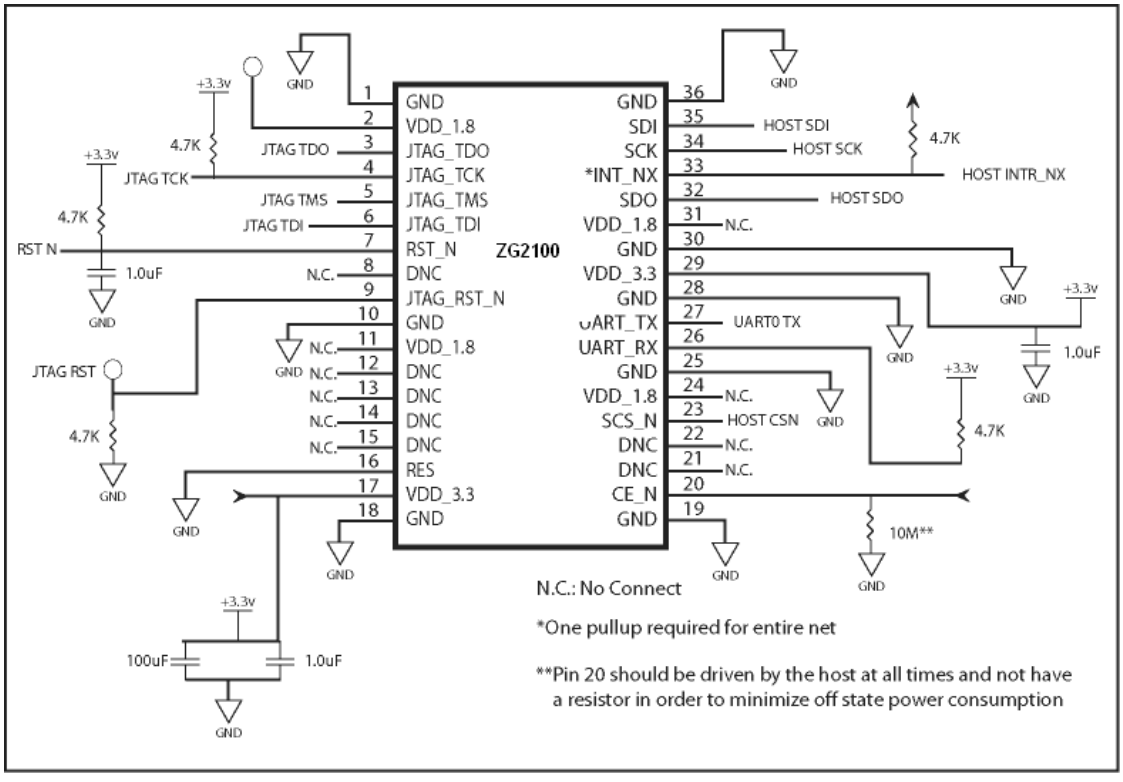

Figure 11. ZG2100M/ZG2101M Module Use Schematic

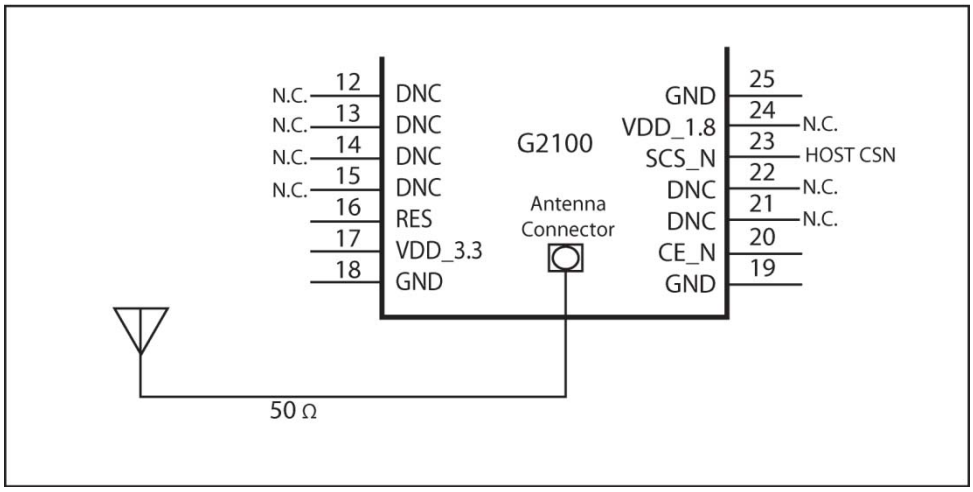

Figure 12. ZG2101M Antenna Placement

5. Electrical Characteristics

Note: Please contact your sales associate for the latest data on specific silicon revisions.

Absolute Maximum Ratings:

Rating	Min	Max
Storage Temperature	-40C	+125C
Supply Voltage (VDD 3.3v)	0V	3.63V

Recommended Operating Conditions:

Operating Condition	Min	Typ	Max
Ambient Operating Temperature Range, commercial parts	0C		+55C
Supply Voltage: (VDD 3.3v)	2.97V	3.30V	3.63V

5.1. Power Consumption

Nominal conditions: 25C, VDD_3.3 = 3.3V

Power Conservation Modes	Min	Typ	Max	Unit
Off	0	0	0	uA
Hibernate, CE_N=3.3v, 3.3v supply only		3		uA
Sleep		250		uA
Standby		10		mA

Core Supply	Min	Typ	Max	Unit
Rx On, Receive Irx, -83dBm		90		mA
Tx On, Transmit Itx, +0dBm		125		mA
Tx On, Transmit Itx, +10dBm		185		mA

Notes:

1. Power defined at antenna port.
2. ZG2100 RX chain is fully ON.
3. Pout= 0dBm (measured at module antenna connector); 2Mb/Sec.modulated signal
4. Pout= +10dBm (measured at module antenna connector); 2Mb/Sec.modulated signal
5. 3.3V Current Consumption values represent Typical Peak currents. Wi-Fi protocol is such that current draw occurs at less than 100% duty cycle. Tx is dependant on such criteria as transmit power setting, and transmit data rate and bandwidth being used. Rx is affected by connectivity distance.

5.2. Timing Characteristics

Characteristic	Min	Typ	Max	Unit
SPI, Data setup to falling clock	1			ns
SPI, Data hold from falling clock	1			ns

6. Radio Characteristics

Nominal conditions: 25C.

Frequency range	Min	Typ	Max	Unit
Flo	2412		2484	MHz

6.1. Transmitter 2.4GHz band

Nominal conditions: 25C, Flo=2437MHz; 2Mb/Sec. modulated signal duty cycled at 95% measured at RF antenna port on board the module.

TX	Min	Typ	Max	Unit
Pout (Transmit spectrum mask Compliant)		+10		dBm
Pout gain step resolution from +5 to +10 dBm		+0.5		dBm
Pout gain step resolution from -10 to +5 dBm		+1.0		dBm

Nominal conditions: 25C, Flo=2437MHz; Pout= +10dBm (measured at module antenna connector); 2Mb/Sec. modulated signal

6.2. Receiver 2.4GHz band

Nominal conditions: 25C, Flo=2437MHz; measured at RF antenna port on board the module.

RX	Min	Typ	Max	Unit
RX Min Input Level Sensitivity, 1Mbps, 8% PER		-84		dBm
RX Min Input Level Sensitivity, 2Mbps, 8% PER		-83		dBm
RX Max Input Level (Power), 1Mbps, 8% PER			-4	dBm
RX Max Input Level (Power), 2Mbps,8% PER			-4	dBm
RX Adjacent channel rejection, 1Mbps, 8% PER	35			dBc
RX Adjacent channel rejection, 2Mbps, 8% PER	35			dBc

7. Ordering Information

DEVICE DESCRIPTION	COMMENT	ORDERING NUMBER
Module	Version using PCB antenna	ZG2100MCC
Module	Version using external antenna	ZG2101MCC

8. Limitations

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, "HIGH RISK APPLICATIONS"). YOU AGREE AND ACKNOWLEDGE THAT YOU HAVE NO LICENSE TO, AND SHALL NOT (AND SHALL NOT ALLOW A THIRD PARTY TO) USE THE TECHNOLOGY IN ANY HIGH RISK APPLICATIONS, AND LICENSOR SPECIFICALLY DISCLAIMS ANY WARRANTY REGARDING, AND ANY LIABILITY ARISING OUT OF, HIGH RISK APPLICATIONS.

9. Revision History

Document ID	DN-1001.04	
Title	ZG2100M	
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