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# A configurable ultra-low noise current source for transition-edge sensor characterization

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**ABSTRACT.** Transition-edge sensors (TESs) are sensitive devices for detecting photons from millimeter radiation to  $\gamma$  rays. Their photon counting efficiency and collecting area benefit from large-array multiplexing scheme, and therefore the development of multiplexing readout system has been an important topic in this field. Among the many multiplex techniques, time-division multiplexing (TDM) superconducting quantum interference device (SQUID) has been used most widely for TES readout. In this work, we design a Configurable Ultra-Low Noise Current Source (CLCS) for TES characterization and as a part of a whole TDM-TES bias control system. The CLCS is based on the feedback structure of ultra-low noise instrumentation amplifiers and low-noise, high-resolution (20 bits) digital-to-analog converter (DAC). CLCS has an ultra-high resolution of 10 nA in the 0 to 5 mA current output range, and can perform current-voltage (IV) sweep and bias-step tests to measure key TES parameters on board. The feedback structure of the CLCS also avoids the issue of impedance mismatch.

**KEYWORDS:** Instrument optimisation; Instruments for CMB observations; Photon detectors for UV, visible and IR photons (vacuum); X-ray detectors

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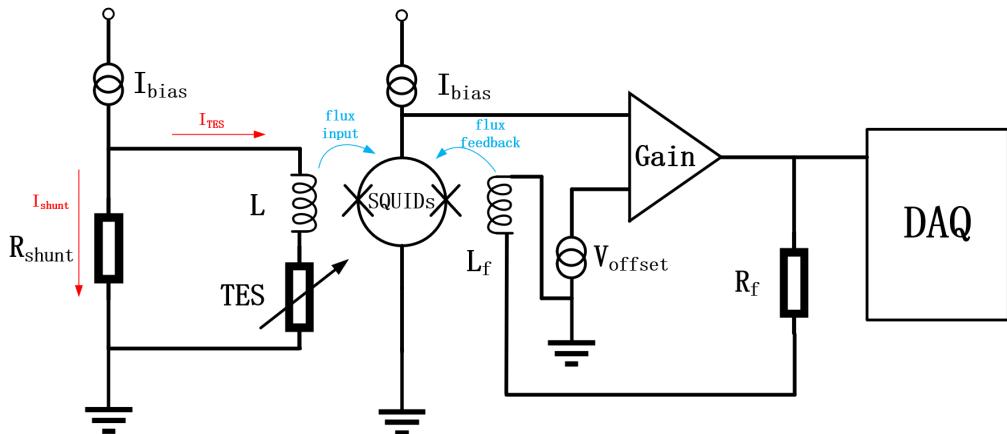
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## 1 Introduction

TESs as a type of superconducting detector have displayed high energy resolution, and have proven their advantages in photon measurement applications ranging from millimeter radiation to  $\gamma$  rays. During operation, a TES is placed on a low-temperature stage to dissipate input signal power, and is biased in an electrical circuit to turn photon signal input into electrical signal output. Figure 1 illustrates its electrical bias scheme. The TES is connected in parallel with a shunt resistor  $R_{\text{shunt}}$  which makes the circuit a stable negative feedback loop, and in series with a inductive coil  $L$  which



**Figure 1.** Schematic diagram of TES chip and simplified readout structure, which includes TES, shunt resistor  $R_{\text{shunt}}$ , inductive coil  $L$ . This is a electric thermal feedback structure with external current bias source  $I_{\text{bias}}$ . The current changes  $I_{\text{TES}}$  through TES can be detected by DC-SQUIDs. The DC SQUID can amplify signals using its flux-lock-loop (FLL) circuit.  $R_f$  is the feedback resistor and  $L_f$  is the feedback coil.

couples TES current signal to the SQUID readout system. TES requires an external bias current  $I_{\text{bias}}$  to operate [1–5]. The TES array developed to be used with this bias and readout system is for high-energy resolution hard X-ray spectroscopy.

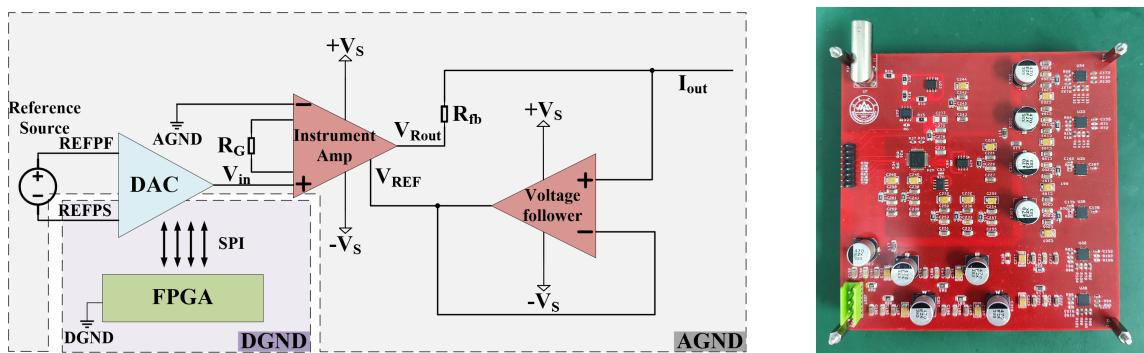
We thus design a Configurable Ultra-Low Noise Current Source (CLCS) as a bias source device for our future hard X-ray TES array spectrometer with a TDM readout system. In addition to supplying low-noise DC bias current, the CLCS also integrated bias current sweeping and square-wave step-bias test functions. So that measuring TES IV curves and decay times for thermoelectric parameters can be achieved without using additional instruments such as an external function generator. This integration is potentially useful for space-limited applications, for instance, in a narrow beam-line hub or space missions.

The paper is organized as follows: section 2 presents the CLCS design principles and testing system configuration; section 3 presents the thermal and electrical parameters of TES through IV curve measurement; section 4 presents the noise performance of the CLCS; section 5 presents the square wave function, and section 6 concludes the paper.

## 2 System design

### 2.1 Bias source electronics

A common way of supplying bias current  $I_{\text{bias}}$  to the TES circuit is by using a low noise source in series with a large resistor, which is usually on the order of  $\sim 1 \text{ k}\Omega$ . For example, the bias source electronics (DAC MAX5443, 16 bits) designed by NIST [6] and the Multi-Channel Electronics (MCE) designed by UBC [7]. However, the impedance of the cable connecting the room temperature bias source to the cold TES stage can be several tens of ohms. Given the  $\sim 1 \text{ k}\Omega$  series bias resistor value, the parasitic cable impedance can bring a non-negligible error in accurately calculating the  $I_{\text{bias}}$  delivered to the TES circuit. We avoid the impedance mismatch issue by using a feedback structure [8–10]. Thus CLCS has more wide dynamic output range. The bias module also contains precision instrument amplifiers with differential symmetric structure and low-noise, high-precision digital-to-analog converter (DAC). The operational amplifiers have high-input and low-output impedance. The design principle of the entire CLCS module is shown on the left side of figure 2.



**Figure 2.** The left figure shows the schematic diagram of CLCS. An instrumentation amplifier and a low noise voltage follower form a feedback loop structure. DAC is used as a configurable voltage source, which is controlled by FPGA. The right figure is printed circuit board (PCB) design of CLCS.

To ensure high-precision regulation of current output and to enhance the driving capability of the DAC, the input  $V_{in}$  of the instrumentation amplifier is connected to the output of the DAC module. The DAC module is DAC11001B of TI, which has 20-bit high-resolution single-channel configurable output based on the Serial Peripheral Interface (SPI) protocol. This high resolution enables very fine control of the TES bias point in the transition slope, and is an improvement over the widely used 16-bit devices. It also has low output noise, approximately  $7 \text{ nV}/\sqrt{\text{Hz}}$  as stated in the data sheet. The REFPF/S pin of DAC11001B determines the output voltage range, which is set to 0 to 5 V according to TES experiment requirements. We use INA849 of TI as the instrumentation amplifier part of CLCS. Its front-end high-impedance input operational amplifier serves as a voltage follower for the DAC. The internal topology ensures system stability and that the load and power supply share a common ground.

The CLCS output current can be represented as:

$$\begin{aligned} I_{out} &= \frac{V_{Rout} - V_{REF}}{R_{fb}} \\ &= \frac{V_{in}Gain}{R_{fb}} \end{aligned} \quad (2.1)$$

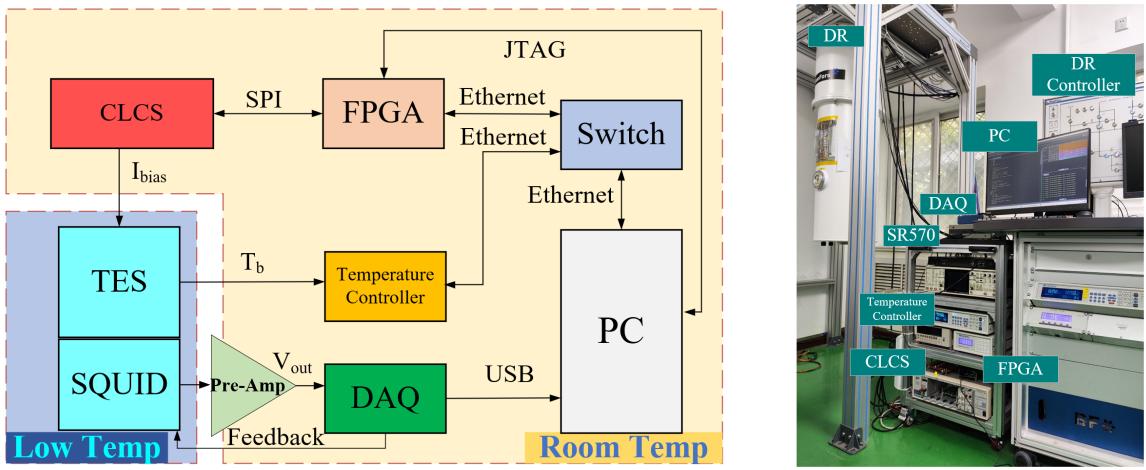
The output voltage  $V_{Rout}$  of the instrumentation amplifier depends on the voltage supply limits of the device  $\pm V_s$ , which is set to be  $\pm 12 \text{ V}$  in this case.  $V_{REF}$  is the reference input voltage of the instrument amplifier. Parasitic resistors on the REF pin that is in series with the internal resistor of the instrument amplifier can disrupt the symmetry of the differential amplifier, thereby reducing the common-mode rejection ratio (CMRR). Therefore, a low-noise, low-output impedance operational amplifier is used as the input for the REF pin. Here we use the TI's low-noise operational amplifier, OPA211. We connect the output port of OPA211 to its negative input port and the REF port, and connect positive input to the feedback resistor  $R_{fb}$ , forming a voltage follower and feedback structure, as shown in figure 2. This feedback structure enables a fixed voltage difference across  $R_{fb}$  based on Equation (2.1), thus providing a constant current. The value of  $R_{fb}$  will affect the current source resolution and output range. The larger the resistance value, the higher the resolution of the current source and the smaller the output current range. According to the testing need of the TES, the output current range of CLCS is configured to be 0 to 5 mA. By choosing a  $1 \text{ k}\Omega R_{fb}$  we get a resolution of 10 nA for the bias current.  $V_{in}$  is the input voltage of INA849, and in this single-ended design, its value is equal to the output voltage of the DAC. *Gain* is the gain factor of the INA849, set to 1 in this case.

## 2.2 Digital control electronics

To make the configuration of CLCS flexible and convenient for functional design, a Field Programmable Gate Array (FPGA) is used for digital control of CLCS. The model number used is Xilinx ARTIX-7 series XC7A35T and we utilize its abundant general purpose input and output (GPIO) resources. The CLCS configure and monitor interactive logic is based on the SPI serial protocol. Joint test action group (JTAG) interface and small form-factor pluggable (SFP) gigabit optical module are used to enable information exchange between the FPGA and the host computer.

## 2.3 Testing system

The testing system is shown in figure 3. It utilizes a dilution refrigerator (DR) to operate the TES in the sub-Kelvin temperature stage. The TES current is coupled to a two-stage direct current (DC) SQUIDs amplifier for low-noise readout. The SQUIDs amplifier is pcSQUID from STAR



**Figure 3.** Testing system: schematic diagram of the testing system, with the TES located in the 30 to 60 mK temperature region, amplified by SQUID and read out by room temperature electronics (left). The control logic of the system is implemented based on Python and FPGA. Physical diagram of the system setup (right).

Cryoelectronics, which consists of two stages of SQUIDs connected in series. They are operated in the flux-locked-loop (FLL) mode. At room temperature, the SQUIDs output signal is connected to a preamplifier for multistage amplification, and the amplified signal is then stored using a data acquisition system (DAQ). The DAQ system is the NI USB-6366, which is equipped with a 2 MSPS sampling rate, 16-bit resolution, and 8 channels analog-to-digital converter (ADC). The Lakeshore 372 temperature controller is used to monitor the real-time temperature changes of the TES cooling stage. The FPGA controls and monitors the CLCS output with different bias currents based on the SPI 4-wire protocol. The communication software framework between these devices and the host computer is implemented using the Python libraries socket, pyvisa, and nidaqmx. It is based on the TCP/IP protocol or USB serial communication.

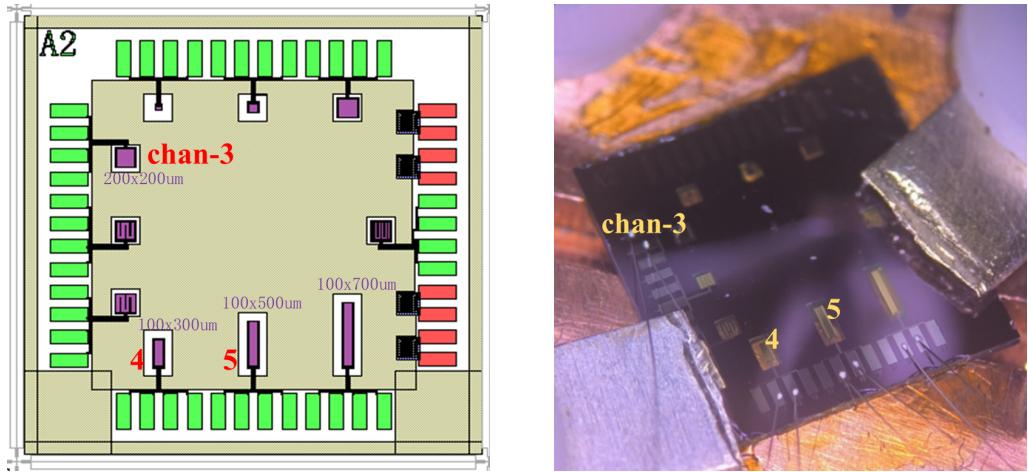
### 3 IV analysis on TES samples

The IV curve measurement under different bath temperatures  $T_{bath}$  reveals several important thermal and electrical parameters about the TES. During the measurement, the voltage  $V$  across the TES is swept by varying the external bias source  $I_{bias}$ , and the TES current  $I$  is sensed at the same time directly through the 2-stage SQUID system. Given the equilibrium condition

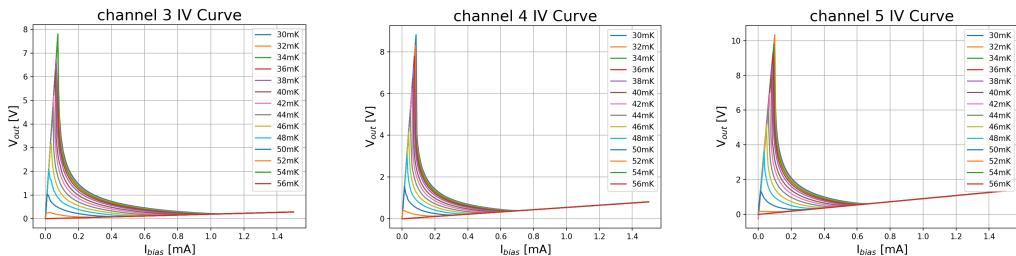
$$I \cdot V = \frac{G}{nT_c^{n-1}} (T_c^n - T_{bath}^n), \quad (3.1)$$

one can fit for the TES critical temperature  $T_c$ , the thermal conductance  $G$  between the TES and the thermal bath, and the thermal conducting index  $n$ . The TES normal resistance  $R_n$  can also be calculated from the slope of the IV curve. Furthermore, a reasonable combination of bath temperature and DC bias current values that yield a specific bias resistance (i.e. %  $R_n$ ) can be found directly from the IV data.

The TESs tested in this experiment are made of aluminum-manganese (AlMn) alloy and the film is deposited on  $\text{Si}_3\text{N}_4$ . This type of TESs has been widely used in long-wavelength applications in the past but rarely utilized as X-ray devices. Our goal is to make AlMn TES arrays for hard X-ray



**Figure 4.** The structure and distribution of TESs: three TESs of different sizes labeled 3,4,5 are selected for the experiment (left). The sizes of channel 3, 4, 5 are  $200 \mu\text{m} \times 200 \mu\text{m}$ ,  $100 \mu\text{m} \times 300 \mu\text{m}$  and  $100 \mu\text{m} \times 500 \mu\text{m}$ , respectively. The expected ratio of resistance is 15:5:3. Physical image shows the actual sample mounting status (right).



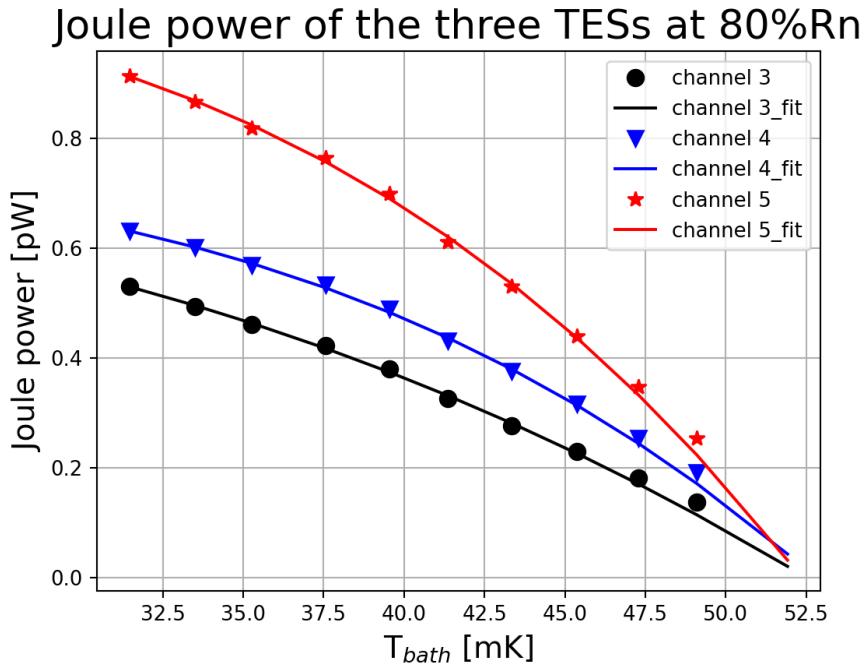
**Figure 5.** The IV test results of the three TES samples based on CLCS. The testing temperature ranges from 30 mK to 56 mK at every 2 mK. The bias current at each temperature is swept from 1.5 mA to 0 mA with an interval of 5  $\mu\text{A}$ .

spectroscopy. As an initial step, we fabricate dark TESs of various sizes to explore the influence of the geometric factors on device thermal and electrical parameters. This is done through IV measurement with the CLCS. The design layout and picture of the TES devices measured are shown in figure 4.

During test, the CLCS outputs a specific bias current at the command from PC through Ethernet port. Meanwhile, the DAQ card and the temperature controller are synchronized to collect the SQUID output signal and temperature data. After each data acquisition, the system controls the bias current supply to output the next value, and repeat the above operation until the entire IV sweep is completed.

The TESs tested here are designed to have a critical temperature of  $\sim 55$  mK. We conduct IV tests on three different-sized TES in a temperature range of 30 mK to 56 mK at an interval of 2 mK. To ensure that the TES goes sufficiently to the normal state, the bias current sweep starts from 1.5 mA. The bias step is 5  $\mu\text{A}$ , which expresses the high resolution performance of CLCS. The IV test data is shown in figure 5. The SQUID feedback resistor is  $100 \text{ k}\Omega$ , giving a gain of 100000 V/A. The TES current  $I$  is calculated by dividing SQUID output voltage by the gain value, and the TES voltage  $V = (I_{\text{bias}} - I) \cdot R_{\text{shunt}}$ . Here  $R_{\text{shunt}}$  is  $0.25 \text{ m}\Omega$ . With  $I$  and  $V$  values at a specific bias point, in this case 80%  $R_n$ , at different bath temperatures,  $G$ ,  $n$  and  $T_c$  can be calculated from Equation (3.1). The results are summarized in table 1.

The ratio of  $R_n$  for the three TESs is approximately 15:5:3, which agrees well with the length-to-width ratios of the samples as shown in figure 4. The G ratio, however, is 0.7:1:1.5, differing obviously from the 1:1:1.5 perimeter ratio. The deviation in  $n$  of channel-3 indicates a difference in the thermal conducting mechanism. While more experiments need to be conducted to pin out the reason, one possible explanation is that the distance between the TES and the silicon substrate in channel-3 is half the distance of the other two samples. The  $T_c$  values of these samples are about the same, and meet expectation.



**Figure 6.** The test and fit results of CLCS, for the Joule power of the three TESs.

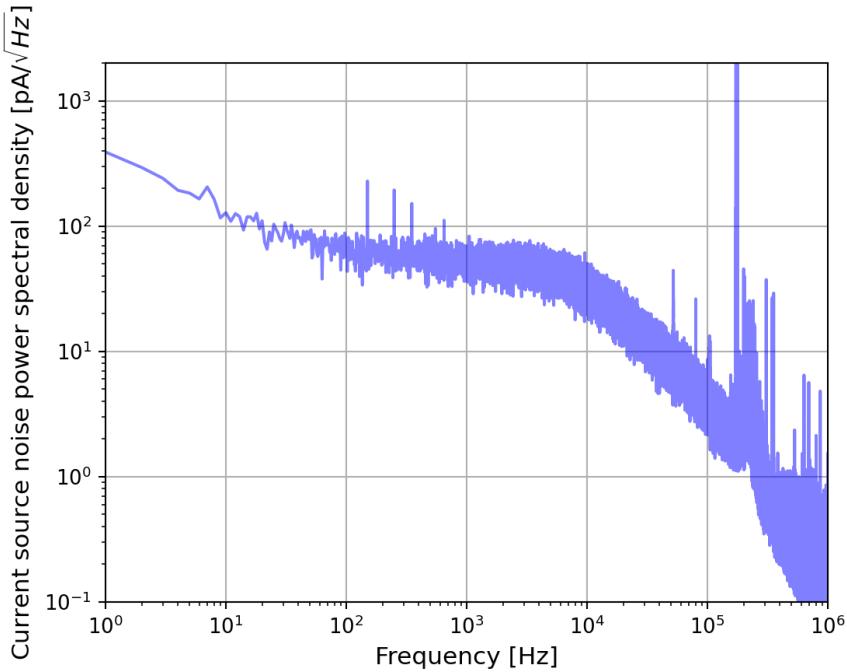
**Table 1.**  $R_n$ ,  $G$ ,  $n$ , and  $T_c$  of the three TESs calculated from CLCS IV tests.

	Channel 3	Channel 4	Channel 5
$R_n$ [mΩ]	136.9	48.1	28.6
$G$ [pW/K]	35.3	51.0	74.5
$n$	2.6	3.6	3.6
$T_c$ [mK]	52.5	52.8	52.4

#### 4 Noise analysis

Noise is an important factor because it determines TES energy resolution. The CLCS noise level should be sufficiently lower than TES intrinsic noise and SQUID noise. The noise contribution of SQUID is typically about some  $\text{pA}/\sqrt{\text{Hz}}$ , which is less than TES intrinsic noise. Our goal is to achieve  $\text{sub-pA}/\sqrt{\text{Hz}}$  noise contribution from the CLCS.

By converting output current into voltage via a low-noise current amplifier (SRS-SR570), the intrinsic noise of CLCS is measured and analyzed in frequency domain by fast Fourier transform function (FFT), as shown in figure 7. The main noise components of CLCS includes  $1/f$  noise and white noise, which is below 5 kHz. We calculate the average noise value is about  $52 \text{ pA}/\sqrt{\text{Hz}}$ , which can be used to calculate the noise contribution of CLCS to system.



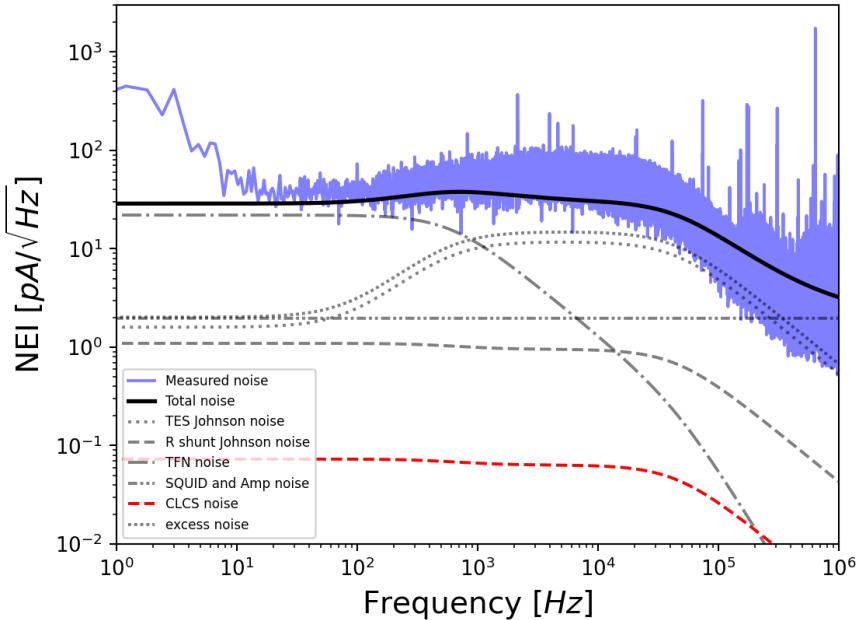
**Figure 7.** The intrinsic noise spectrum of CLCS. The gain of SR570 is  $10 \mu\text{A/V}$ , and the sampling rate of DAQ is 2 MSPS. Below 5 kHz ( $1/f$  noise and white noise), the average noise of CLCS is about  $52 \text{ pA}/\sqrt{\text{Hz}}$ , which is the mainly noise contribution of CLCS to TES system.

Figure 8 shows the noise of channel-4 TES biased at 40%  $R_n$  with CLCS. Using a one-body thermoelectric model [11], the TES noise can be properly fitted. The low frequency regime ( $< 1 \text{ kHz}$ ) is dominated by the thermal fluctuation noise (TFN), which is caused by phonon transfer between TES and thermal bath. The middle frequency regime ( $1 \text{ kHz} \sim 100 \text{ kHz}$ ) is dominated by TES Johnson noise, which is caused by thermal agitation of electrons in the TES. There is often discrepancy between the measured and theoretical TES Johnson noise, which is called “excess noise”. Excess noise can be expressed by  $M$  times Johnson noise of TES, where  $M = 0.2\sqrt{\alpha_I} = 1.4$  [12] and  $\alpha_I = \frac{\partial \log R}{\partial \log T} \Big|_{I_0}$  is the unitless logarithmic temperature sensitivity of TES [1] at 40%  $R_n$  bias point for our TES model.

In the high frequency regime ( $> 100 \text{ kHz}$ ), the TES noise rolls off below SQUID and readout electronics noise. The noise contribution of CLCS is compared with all other components by multiplying it with TES circuit transfer function:

$$\text{NEI}_{\text{CLCS}} = \sqrt{S_{I_{\text{CLCS}}}} R_{\text{shunt}} |Y_{\text{ext}}|, \quad (4.1)$$

where  $\text{NEI}_{\text{CLCS}}$  is the noise equivalent current density (NEI) contribution of CLCS to TES system.  $S_{I_{\text{CLCS}}}$  is the intrinsic current noise density of CLCS, which is measured and shown in figure 7.  $Y_{\text{ext}}$  is the external admittance of the TES electrothermal feedback circuit [1]. The noise contribution is less



**Figure 8.** System noise components analysis. The solid blue line is the measured system noise of the channel-4 TES biased at 40%  $R_n$  with CLCS. The solid black line is the calculated total noise. The dotted gray line is the TES Johnson noise. The dashed gray line is the Johnson noise of shunt resistor. The dash-dotted gray line is the thermal fluctuation noise (TFN) noise. The dash-dot-dotted gray line is the SQUID and readout electronics noise. The solid red line is the noise contribution of CLCS. The excess noise (densely dotted line) is  $M$  times Johnson noise of TES, where  $M = 1.4$ .

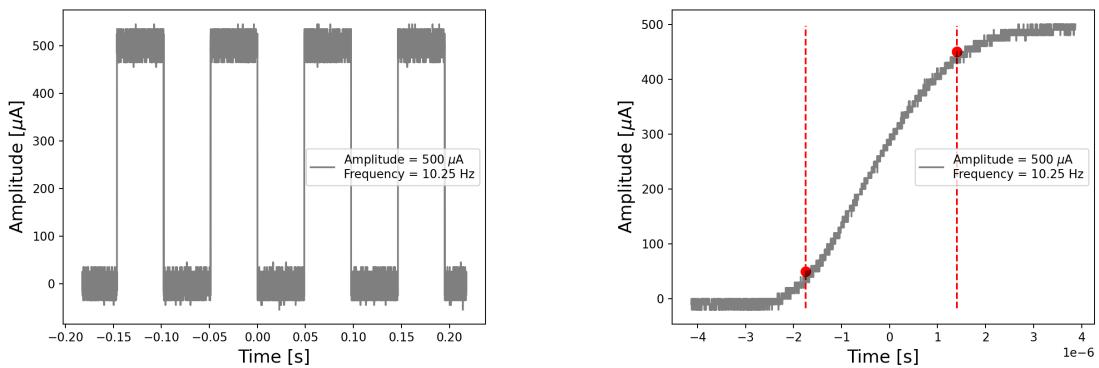
than 0.08 pA/ $\sqrt{\text{Hz}}$ , which meets our design goal. Based on this analysis, the CLCS noise contribution to the whole TES system meets the requirement.

## 5 AC function

Count rate, which is another important factor of X-ray TESs, is directly related to the signal decay time. Furthermore, by measuring decay time at different bias currents and temperatures, the temperature sensitivity, current sensitivity and heat capacity of a TES can be fitted. The decay response can be measured by DC biasing the TES at a desired transition point while superimposing a square wave signal [13]. The amplitude of the square wave should be very small compared to the DC bias that it causes negligible changes in TES bias fraction.

This type of experiment usually is conducted with an external function generator. By implementing the alternating current (AC) function into the CLCS system, we are now able to complete the test in a more compact setup. And due to the higher current resolution of the CLCS than existing commercial function generators, we are able conduct this characterization with minimal square wave amplitude.

For X-ray applications, the time constant of TESs is typically on the order of  $\sim 1$  ms. In figure 9, we show a 10.25 Hz square wave, with 3.204  $\mu\text{s}$  rise time (10% to 90% amplitude), generated by the CLCS, demonstrating its capability of characterizing X-ray TES decay time.



**Figure 9.** CLCS square wave test: the left figure shows a 10.25 Hz square wave with an amplitude of 500  $\mu\text{A}$  generated by CLCS. The right figure is the rise time. The red points and dashed lines indicate the positions of the 10% and 90% amplitudes.

In addition to square wave, CLCS can be configured to generate sine wave up to 100 kHz, which potentially can be used for complex impedance measurements.

## 6 Conclusion

We have designed a current source CLCS for TES bias and characterization. The CLCS has low noise, high resolution output and flexible configuration. It effectively avoids the impedance mismatch issue of voltage bias sources by applying a feedback structure. We performed successful IV characterization on different TES samples, demonstrated low noise contribution (sub-pA/ $\sqrt{\text{Hz}}$  level), and showed AC singal generation functions with this CLCS.

In the future work, we will upgrade the CLCS with DC-SQUID bias function and integrate it with a TDM feedback module to a whole TDM-TES control system. The final version of the control system is expected to perform TDM-TES bias, characterization, and data-acquisition tasks.

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