Altera FPGA 综合设计实验

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实验内容

调用一个宏功能模块 ROM，并在 ROM 中存放正弦波一个完整周期的数据。再编写顶层实体，将 ROM 模块当作元件调用，实现一个正弦波产生器。最终的结果采用 SignalTap II 来观察

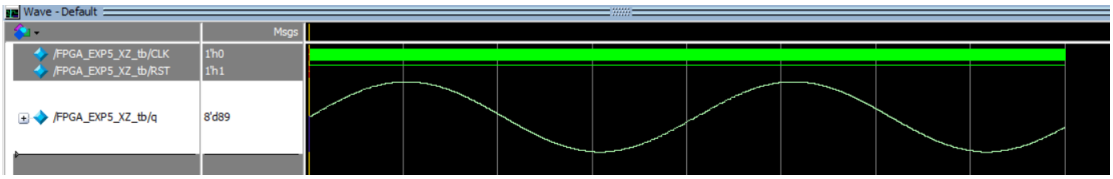
设计分析

设计顶层模块调用 mystorage 模块，顶层模块的输入包括时钟和复位，输出是 8 位正弦数据。在顶层模块中调用 mystorage 模块，编写一个 1024 位计数器作为其地址输入

源码

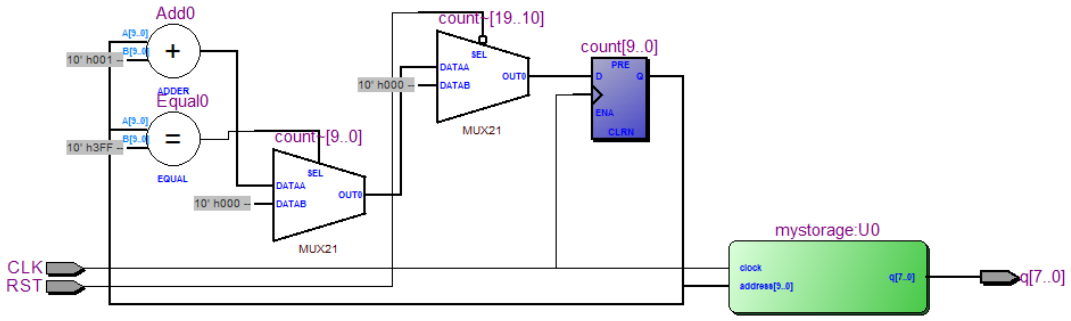
```
module FPGA_EXP5_XZ(RST,CLK,q);
   input RST,CLK;
   output [7:0]q;
   reg [9:0]count;

   mystorage U0(count,CLK,q);

   always@(posedge CLK)begin
      if(!RST)count<=10'b0000000000;
      else if(count==10'b1111111111)count<=10'b0000000000;
      else count<=count+10'b0000000001;
   end
endmodule
```

仿真



```
1   `timescale 10ns/1ns
2   module FPGA_EXP5_XZ_tb();
3      reg CLK,RST;
4      wire [7:0]q;
5
6      initial CLK<=0;
7      always #1 CLK=~CLK;
8
9      initial begin
10     RST<=0;
11     #2 RST<=1;
12     end
13
14     FPGA_EXP5_XZ U0(RST,CLK,q);
15  endmodule
```

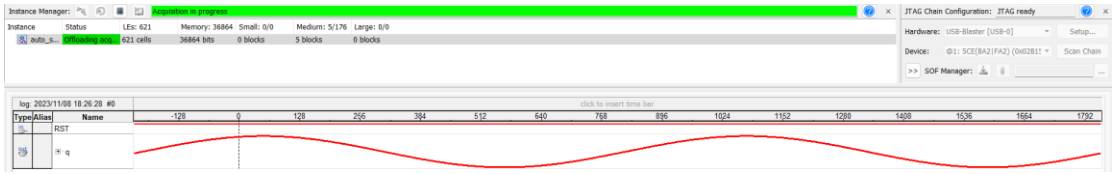
中间结果



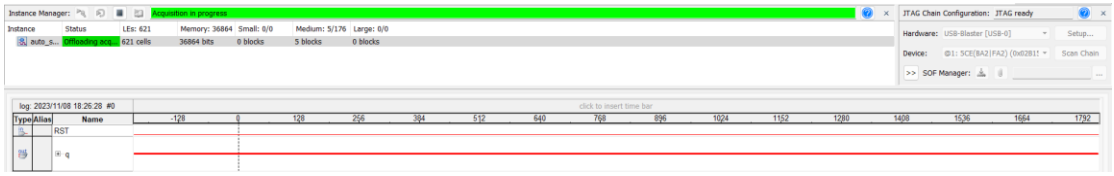
Flow Summary	
Flow Status	Successful - Wed Nov 08 18:22:27 2023
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	FPGA_EXP5_XZ
Top-level Entity Name	FPGA_EXP5_XZ
Family	Cyclone V
Device	5CEFA2F23C8
Timing Models	Final
Logic utilization (in ALMs)	275 / 9,430 (3 %)
Total registers	519
Total pins	10 / 224 (4 %)
Total virtual pins	0
Total block memory bits	45,056 / 1,802,240 (3 %)
Total DSP Blocks	0 / 25 (0 %)
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI PMA RX ATT Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total HSSI PMA TX ATT Serializers	0
Total PLLs	0 / 4 (0 %)
Total DLLs	0 / 4 (0 %)

FPGA 验证

1. RST 为高电平时



2. RST 为高电平时



Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
CLK	Input	PIN_W16	4A	B4A_N0	PIN_W16	2.5 V (default)		12mA (default)	
RST	Input	PIN_Y11	3B	B3B_N0	PIN_Y11	2.5 V (default)		12mA (default)	
altera_reserved_tck	Input				PIN_V5	2.5 V (default)		12mA (default)	
altera_reserved_tdi	Input				PIN_W5	2.5 V (default)		12mA (default)	
altera_reserved_tdo	Output				PIN_M5	2.5 V (default)		12mA (default)	1 (default)
altera_reserved_tms	Input				PIN_P5	2.5 V (default)		12mA (default)	
q[7]	Output	PIN_V20	4A	B4A_N0	PIN_V20	2.5 V (default)		12mA (default)	1 (default)
q[6]	Output	PIN_U20	4A	B4A_N0	PIN_U20	2.5 V (default)		12mA (default)	1 (default)
q[5]	Output	PIN_AA22	4A	B4A_N0	PIN_AA22	2.5 V (default)		12mA (default)	1 (default)
q[4]	Output	PIN_T22	5A	B5A_N0	PIN_T22	2.5 V (default)		12mA (default)	1 (default)
q[3]	Output	PIN_AB21	4A	B4A_N0	PIN_AB21	2.5 V (default)		12mA (default)	1 (default)
q[2]	Output	PIN_T17	5A	B5A_N0	PIN_T17	2.5 V (default)		12mA (default)	1 (default)
q[1]	Output	PIN_AB18	4A	B4A_N0	PIN_AB18	2.5 V (default)		12mA (default)	1 (default)
q[0]	Output	PIN_P18	5A	B5A_N0	PIN_P18	2.5 V (default)		12mA (default)	1 (default)
<<new node>>									

实验总结

注意在初期给 RST 一个低电平以设定电路的初值

当 RST 为低电平，地址默认为 0 时，输出为 80h 即 2^7