Zhen Xu

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Education

University of Science and Technology of China **Sep. 2020 – Present**

Bachelor of Engineering in Electrical Engineering *Hefei, Anhui*

GPA: 3.42/4.3(85/100) **Ranking**: 25/76

Honors: Scholarship for Elite Class, Awarded to students admitted to the Elite Class

Relevant Coursework

- Design of Analog Integrated Circuits
- Digital Integrated Circuits Design
- The Practice of Chip Design
- Electromagnetic Field and Wave
- Linear Electronic Circuits
- Nonlinear Electronic Circuits
- Digital Logic Circuits
- Materials and physics of semiconductors

Research Experience

Integrated Nanoelectronics and X-Computing Lab, USTC **March 2023 – August 2023**

Research Intern *Hefei, Anhui*

- Conducted extensive research on two-dimensional semiconductor devices, focusing particularly on the manufacture and properties of MoS_2, and enhancing its interface properties using *hexagonal BN*.
- Participated in hands-on production activities for transistor devices, including scribing, lithography, lift-off, ALD, CVD, and more, to assess the properties of 2D semiconductor devices.

Power and Mixed-signal IC Lab, USTC **September 2024 – Present**

Research Intern *Hefei, Anhui*

- Using the TSMC 180nm process, a current-mode Bandgap Reference was designed, incorporating Chopping and Dynamic Element Matching (DEM) techniques to mitigate mismatch in Amplifiers and PMOS current mirrors. Trimming technology was utilized to reduce PTAT errors, and an LDO was integrated to enhance the Power Supply Rejection Ratio (PSRR) of the Bandgap circuit.
- The Bandgap Reference achieved an output voltage of $2.5V$, with a supply voltage range of $3.3V$ to $5V$, operating over a temperature range of $-40°$C to $125°$C. It demonstrated a Power Supply Rejection Ratio (PSRR) of $-118dB$, a Line Regulation (LR) of $42ppm/V$, a Temperature Coefficient (TC) of $2.44ppm/°$C, and a startup time of $7ms$. The process variation (σ/μ) was 0.52%, with a Current Consumption of $120\mu A$.

Academic Activities

Design and Implementation of Integer Square Root Circuit | *Verilog HDL, Cadence* **May 2024**

- Designed an Integer Square Root circuit and its testbench using Verilog HDL.
- Conducted code simulation and netlist simulation using Cadence Incisive.
- Conducted logic synthesis and equivalence checking using Cadence Genus.
- Completed physical design of the chip using Cadence Innovus.

Design and Application of Operational Amplifier Circuits | *Cadence* **June 2024**

- Used Cadence to design an Open Loop Operational Amplifier that meets the following specifications: a Gain of $90dB$, a Unit Gain Bandwidth of approximately $80MHz$, a Phase Margin greater than $50°$, a Slew Rate greater than $25V/\mu s$, an Output Swing greater than $0.6V$, an output DC level of approximately $1V$, and a power consumption of less than $1mW$.
- Used this Operational Amplifier to design a Voltage Follower, which has a Bandwidth of $90MHz$ and good tracking characteristics within the range of $450mV$ to $1.8V$ (with a supply voltage of $1.8V$ and an allowable error of $10\mu V$).
- Used this Operational Amplifier to design an Inverting Amplifier with a Gain of -10, featuring excellent low-frequency gain and Bandwidth.

Skills

Languages: Chinese(native), English(TOEFL 106, GRE 323+3.5)
Programming Languages: Verilog HDL, C, LaTeX, MATLAB
Developer Tools: Cadence, Quartus, VS Code, MATLAB

Interests

Long-distance Running: Running long distances 4 to 5 times a week has become a habit that helps me stay focus at work.
Frontend Development: I created my personal homepage and developed a guide website for studying abroad.