Organization of Digital Computers

EECS 112/CSE 132

Solutions Week 6

Problem 1

and rd, rs1, rs2

a)

RegWrite	ALUSrc	ALUoperation	MemWrite	MemRead	MemToReg
1	0	AND	0	0	0

b) PC flip-flop , Instruction memory, Register file, ALUsrc mux, ALU, the MemToReg mux, PC+4 adder, and PCSrc Mux.

Problem 2

R-type	I-type(non-ld)	Load	Store	Branch	Jump
24%	28%	25%	10%	11%	2%

a)

Load and Store instructions use data memory
25% + 10% = 35%

b) What fraction of all instructions use instruction memory?
100% Every instruction must be fetched from instruction memory before it can be executed

c) What fraction of all instructions use the sign extend (Immediate generator)?
I-type (non-load), Load, Store, Branch, and jump instructions have immediate part and use the immediate generator module
28% + 25% + 10% + 11% + 2% = 76%

Problem 3

a) MemToReg wire is stuck at 0
Only loads are broken. MemToReg is either 1 or "don't care" for all other instructions.

b) Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0?

I-type, loads, stores are all broken

Problem 4

0x00c6ba23

0000 000 01100 01101 011 10100 0100011

Opcode is 0100011

From table in page 119 it is a S-type instruction

Funct3 is 011 so it is Sd (Store double word) instruction

Source 1 is 01101 13

And source 2 is 01100 12

The immediate value is 000000010100 => 20

Sd x12, 20 (x13)

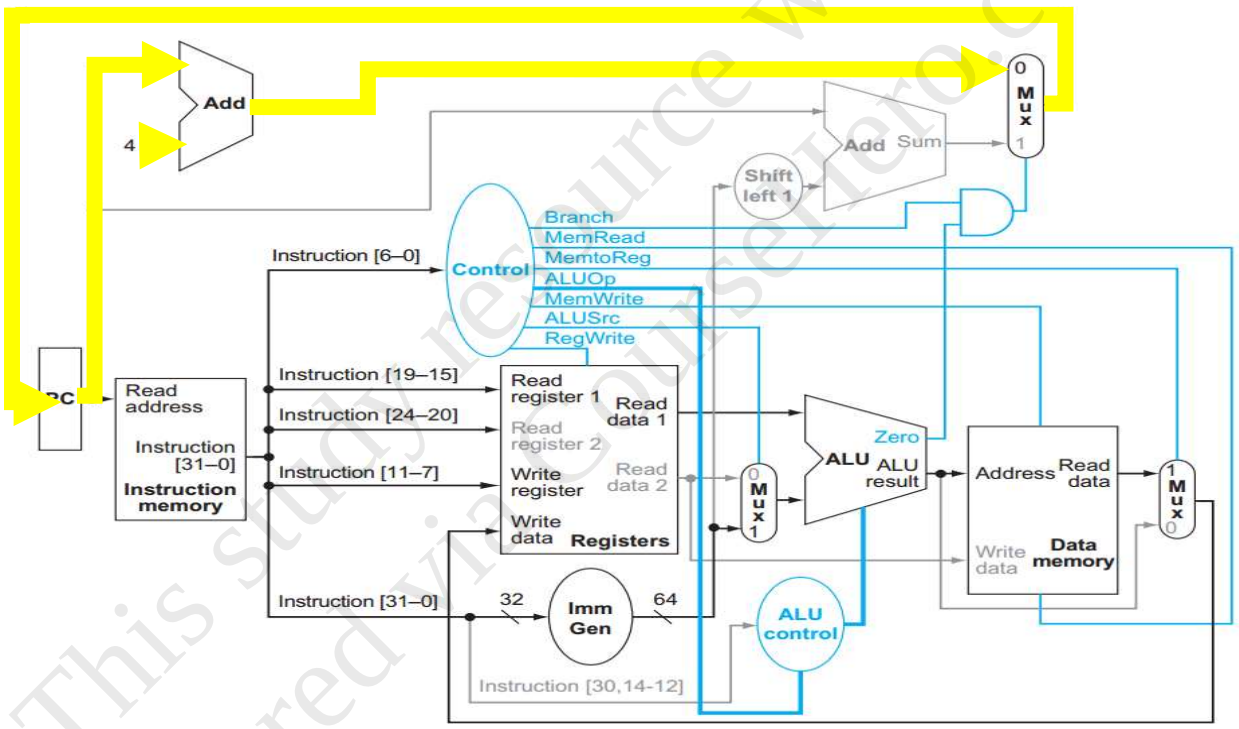
a) What are the values of the ALU control unit's inputs for this instruction?
ALU Control takes ALUop and Instruction [30, 14-12]

Based on the table on page 252 ALUop for sd instructions is 00
Instruction [30] = 0
Instruction [14:12] = 011

What is the ALU control output?
For Store instruction we want the ALU to add and based on the table on page 252 the ALU Control output would be 0010

b) What is the new PC address after this instruction is executed? Highlight the path through which this value is determined.

PC + 4



c) For each mux, show the values of its inputs and outputs during the execution of this instruction.
ALUSrc mux
Input 0 x12

Input 1 20
Output 20 (select 1)

MemToReg mux
Input 0 x13 + 20 (ALU result)
Input 1 Undefined (cause we are not reading anything from memory)
Output Undefined (select don't care)

PCSrc mux
Input 0 PC + 4
Input 1 PC + 40 (shifted immediate)
Output PC + 4 (select 0)

d) What are the input values for the ALU and the two add units?

ALU
Inputs x13 , 20
Output x13 + 20

PC + 4 adder
Inputs PC , 4
Output PC + 4

Branch adder
Inputs PC , 40
Output PC + 4

e) What are the values of all inputs for the registers file?

Inputs :
Read Register 1 13
Read Register 2 12
Write Register 20 (10100_2) we are not going to write anything to register file for this instruction but the rd field of the instruction has this value which we will use it as immediate in this instruction

Write data — undefined (the output from MemToReg mux)

RegWrite — 0

Output:

Read data 1 — x13

Read data 2 — x12

Problem 5

I-Mem / D-Mem	Register file	Mux	ALU	Adder	Single gate	Register read	Register setup	Sign extend	Control
250ps	150ps	25ps	200ps	150ps	5ps	30ps	20ps	50ps	50ps

"Register read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

a) What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)?

Register read + I-Mem + Register file + ALUSrc mux + ALU + MemToReg mux + register setup = 30 + 250 + 150 + 25 + 200 + 25 + 20 = 700ps

b) What is the latency of ld? (Check your answer carefully. Many students place extra muxes on the critical path.)

Register read + I-Mem + Register file + ALU + D-Mem + MemToReg mux + register setup = 30 + 250 + 150 + 200 + 250 + 25 + 20 = 925ps

c) What is the latency of sd? (Check your answer carefully. Many students place extra muxes on the critical path.)

Register read + I-Mem + Register file + ALU + D-Mem = 30 + 250 + 150 + + 200 + 250 = 880ps

d) What is the latency of beq?

Register read + I-Mem + Register file + ALUSrc mux + ALU + AND gate + PCSrc mux + Register Setup = 30 + 250 + 150 + 25 + 200 + 5 + 25 + 20 = 705ps

e) What is the minimum clock period for this CPU?

The minimum clock period is 925 ps