Exercici 2.4

Si assumim cache "look-aside" (mentre fa l'accés alhora va a la memòria principal):

a) $t_{miss\ L1} = t_{MP},\ t_{CPU\ mem} = 5\ ns,\ hit_{L1} = 99\% \Rightarrow miss_{L1} = 1\%,\ t_{L1} = \frac{1}{400} t_{MP} \Rightarrow t_{MP} = 400\ t_{L1}$

$$\boxed{t_{CPU\ mem} = hit_{L1} t_{L1} + miss_{L1} t_{MP}}$$

$$t_{CPU\ mem} = 0.99\ t_{L1} + 0.01 \cdot 400\ t_{L1} = 5\ ns$$

$$t_{L1} = \frac{5\ ns}{0.99+0.01 \cdot 400} = \frac{5\ ns}{4.99} = 1.002...\ ns$$

b) $t_{CPU\ mem} = 2\ ns,\ hit_{L2} = 99\% \Rightarrow miss_{L2} = 1\%,\ t_{miss\ L2} = t_{MP}$

$$\boxed{t_{CPU\ mem} = hit_{L1} t_{L1} + miss_{L1} hit_{L2} t_{L2} + miss_{L1} miss_{L2} t_{MP}}$$

$$t_{CPU\ mem} = 0.99 t_{L1} + 0.01 \cdot 0.99 \cdot t_{L2} + 0.01^2 t_{MP} = 2\ ns$$

$$t_{L2} = \frac{2\ ns - 0.99 t_{L1} - 0.01^2 \cdot 400}{0.01 \cdot 0.99} = \frac{0.9579...\ ns}{0.0099} = 96.767...\ ns$$

Si assumim cache "look-through" (fa l'accés i si falla va a la memòria principal):

a) $t_{miss\ L1} = t_{MP},\ t_{CPU\ mem} = 5\ ns,\ hit_{L1} = 99\% \Rightarrow miss_{L1} = 1\%,\ t_{L1} = \frac{1}{400} t_{MP} \Rightarrow t_{MP} = 400\ t_{L1}$

$$\boxed{t_{CPU\ mem} = t_{L1} + miss_{L1} t_{MP}}$$

$$t_{CPU\ mem} = t_{L1} + 0.01 \cdot 400\ t_{L1} = 5\ ns$$

$$t_{L1} = \frac{5\ ns}{1+0.01 \cdot 400} = 1\ ns$$

b) $t_{CPU\ mem} = 2\ ns,\ hit_{L2} = 99\% \Rightarrow miss_{L2} = 1\%,\ t_{miss\ L2} = t_{MP}$

$$\boxed{t_{CPU\ mem} = t_{L1} + miss_{L1} (t_{L2} + miss_{L2} t_{MP})}$$

$$t_{CPU\ mem} = t_{L1} + 0.01\ (t_{L2} + 0.01 t_{MP}) = 2\ ns$$

$$t_{L2} = \frac{2\ ns - t_{L1} - 0.01^2 \cdot 400}{0.01} = \frac{0.96\ ns}{0.01} = 96\ ns$$