Exercici 2.5

a)

$$miss_{L1\ i\ L2} = 0.04 \cdot 0.2 = 0.008 = 0.8\%$$

Si assumim cache "look-aside" (mentre fa l'accés alhora va a la memòria principal):

b)

$$\boxed{t_{CPU\ mem} = hit_{L1} t_{L1} + miss_{L1} hit_{L2} t_{L2} + miss_{L1} miss_{L2} t_{MP}}$$

$$t_{CPU\ mem} = 0.96\tau + 0.04 \cdot 0.8 \cdot 15\tau + 0.04 \cdot 0.2 \cdot 100\tau = 2.24\tau$$

c)

$$t_{CPU\ mem\ L2\ ideal} = 0.96\tau + 0.04 \cdot 1 \cdot 15\tau = 1.56\tau$$

$$Factor_{reducció} = \frac{t_{CPU\ mem}}{t_{CPU\ mem\ L2\ ideal}} = \frac{2.24\tau}{1.56\tau} = 1.43$$

d)

$$t_{CPU\ mem\ sense\ L2} = 0.98\tau + 0.02 \cdot 100\tau = 2.98\tau$$

Si assumim cache "look-through" (fa l'accés i si falla va a la memòria principal):

b)

$$\boxed{t_{CPU\ mem} = t_{L1} + miss_{L1} (t_{L2} + miss_{L2} t_{MP})}$$

$$t_{CPU\ mem} = \tau + 0.04 (15\tau + 0.2 \cdot 100\tau) = 2.4\tau$$

c)

$$t_{CPU\ mem\ L2\ ideal} = \tau + 0.04 (15\tau) = 1.6\tau$$

$$Factor_{reducció} = \frac{t_{CPU\ mem}}{t_{CPU\ mem\ L2\ ideal}} = \frac{2.4\tau}{1.6\tau} = 1.5$$

d)

$$t_{CPU\ mem\ sense\ L2} = \tau + 0.02 \cdot 100\tau = 3\tau$$