# CSC258 Lab 5

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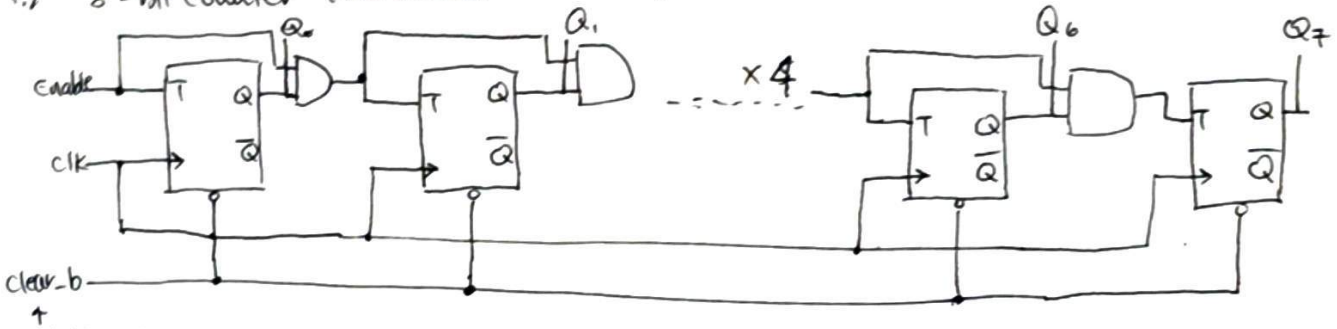
## Part I

1.) 8-bit counter (bits labelled $Q_0 \dots Q_7$)




* Asynchronous ⇒ clear b. edge & clock edge both paid attn to

6.a) Logic utilization < 1% (13/32070)

Registers: 8 total (picture in the submission)

b) 625.0 MHz (the smaller frequency is max freq that design could run on DE1-SoC board)

↑ picture attached

5CSEMA5F31C6

(hex) rev. ← 00 ... 15 (counter) 0001 →

7.) picture attached.

Diff in comparison w/ Figure 1?

Same components, just different configuration

## Part II

Ex. q is 4-bit counter. Max value not needed b/c: when you increment, will just "wrap" (b/c overflow)

- if went 4-bit → 0-9 count ⇒ Add a check for 9 (replace q == 4'b1111 w/ q == 4'b1001)
- full speed (50 MHz), expect to see flickering (count from 0 → F in 1/50 millionth of a second)
- How large a counter for 50 million clock cycles? $\lceil \log_2 \lceil 50 \text{ million} \rceil \rceil = 26$ bits needed

1.)


enable is clock_50 but delayed by Rate Divider. Count counts # times enable pulses up.

## Part III

Need 16 bits (Y longest)

0.5 secs/bit
Pause each time (a 0)
111 is dash, 1 is dot

count to 50 million → 1 pulse/50 million = 1Hz (1 sec)

1 pulse/25 million = 2Hz b/c 2x/second

| | | | |
|---|---|---|---|
| 1. | S | ... | 1 0 1 0 1 0 0000000000 |
| | T | — | 111 0000000000000 |
| | U | ..— | 1 0 1 0 111 0 0 0000000 |
| | V | ...— | 1 0 1 0 1 0 111 0 0000000 |
| | W | .— — | 1 0 111 0 111 0 0000000 |
| | X | —..— | 111 0 1 0 1 0 111 0 0000 |
| | Y | —.— — | 111 0 1 0 111 0 111 0 0 |
| | Z | — —... | 111 0 111 0 1 0 1 0 0000 |

2.