CSC258 Lab 4

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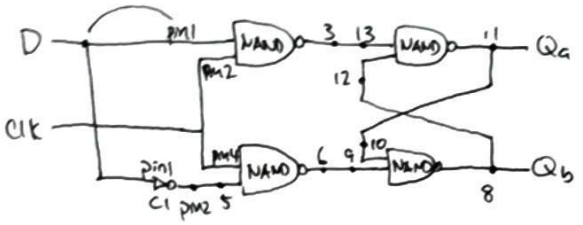
Part I

1. Gated D latch, numbers are the pins



000
101
100
010 → A+B

0010
0100
0110

011
100
110
111

4. Input combinations of clk and D that shouldn't be tested first:
   - When clock is set to 0 initially, the outputs will be 1 out of NAND gate and so whatever the previous values were for Qa and Qb will be outputted (which will be random, b/c it's whatever was there prior).
   - Idea of clock is to store values consistently
   - 00 → 11
     11 → 00
     ⇒ want to override assignments

Part II

1. When load_n=1 and ShiftRight = 0, behaviour of 8-bit shifter: loads the value of load_val into the register

2. 8 bit Shift register