2017 Computer Architecture Midterm Exam (Total Scores=100) 2017/11/23

1. Translate the following C codes into the MIPS assembly code. (10, 15 pts)

(a)
```
Int Test(int n)
{   if (n>0 && n<5) return (0);
    else return (1);
}
```

(b)
```
Int fab(int n)
{
    if (n<3) return (1);
    else return ( fab(n-1) + fab(n-2) );
}
```

addi $sp, $sp, -12
sw 8 ($sp)
sw 4 : (n)
sw 0 :

2. We have two processors CPU1 and CPU2, which have different parameters as shown in the following table.

Processor	Clock rate	Integer CPI	Floating Point CPI
CPU1	2.4GHz	0.8	4
CPU2	2GHz	0.6	2

(a) Now we have a program A which contains 40% integer instructions and 60% floating-point instructions. Is it true that CPU1 has a higher clock rate, so it is faster than CPU2 for program A? Explain your answer. (算式) (10 pts)

(b) Now we have a new hardware to execute floating-point operations, which has 2 times speedup, compared with the old floating-point version. We implement this new hardware only on CPU1, and let "New CPU1" execute program A again. Which CPU is faster for program A, "New CPU1" or "CPU2"? By how much speedup? (算式) (10 pts)

3. A MIPS processor has three different control instructions: (assume "Label" is the position of an instruction)

```
beq    $t1, $t2, offset;
J      Label;
Jal    Label;
```

Explain how to calculate their "target addresses" (i.e., the address of branch or jump) for each of them? (Hint. Reference the value of "PC")

(15 pts)

4. Fig. 1 shows a design for the multiplication operations. (10 pts, 10 pts)

(a) Draw the flowchart to illustrate how the multiplication can be performed on Fig. 1

(b) Use the design of Fig. 1 to compute 5*4. (Trace 4個 Cycles)

(Assume that we use four bits to represent the multiplicand and the multiplier.)

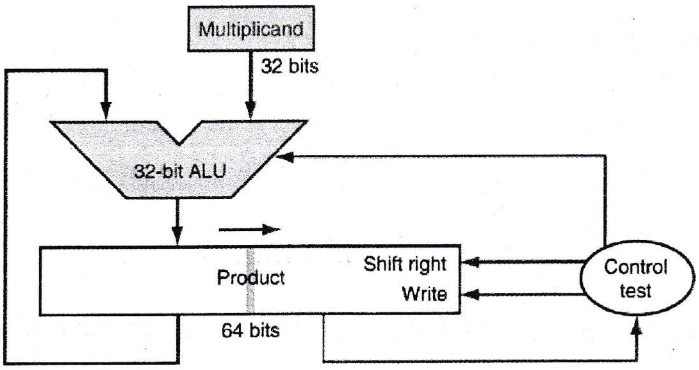

Fig. 1

5. Explain the following questions based on your understanding. (10 pts, 10 pts)

(a) List at least two different features between the MIPS ISA and the Intel ISA.

(b) A typical compiler will have two compiling phases, front-end and back-end. Explain the major differences between these two phases.

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Phase I parsing

optimization

II code generation

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長庚大學期中、期末考試答案用紙

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科目 計算機架構 (11/23)

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1. 設定 n 儲存在 $s0 , return 值儲存在 $s1

(a)

```
Test:  slt  $t0, $zero, $s0      // 判斷 n 是否大於 0
       beq  $t0, $zero, Else     // 若否,則跳至 Else
       slt  $t1, $s0, 5          // 判斷 n 是否小於 5
       beq  $t1, $zero, Else     // 若否,則跳至 Else
       sw   $s1, $zero           // return 0
       jr
Else:  sw   $s1, 1               // return 1
       jr
```

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(b)

```
fab:   slt  $t0, $s0, 3          // 判斷 n 是否小於 3
       beq  $t0, $zero, Else     // 若否,則跳至 Else
       sw   $s1, 1               // return 1
Else:  addi $s0, $s0, -1         // n=n-1
       jr   fab
       sw   $t1, $s1             // 儲存 fab(n-1)
  →    sw   $t2, $s1             // 儲存 fab(n-2)
       add  $t3, $t1, $t2        // $t3 = fab(n-1) + fab(n-2)
       sw   $s1, $t3             // return fab(n-1) + fab(n-2)
```

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addi $s0 , $s0 , -1 // n = n-2

jr fab

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2. CPU Time = IC × CPI × $\frac{1}{\text{Clock Rate}}$

(a) CPU Time 1 = Instruction Count 1 × (0.8×0.4+4×0.6) × $\frac{1}{2.4\times10^9}$ = ~~8.5~~ 1.13×10^-9 × 10^{-10} × (Instruction Count 1)

0.32+2.4 = 2.72

$\frac{2.72}{2.4} = \frac{\cancel{272}\ 68}{\cancel{240}\ 60} = \frac{34}{30}$ 1.13

CPU Time 2 = Instruction Count 2 × (0.6×0.4+2×0.6) × $\frac{1}{2\times10^9}$ = 7.2 × $10^{\cancel{-10}\,-9}$ × (Instruction Count 2)

No, 計算後發現 CPU Time 1 > CPU Time 2 , ∴ CPU 2 is faster !

6 8

(b) CPU Time 1N = Instruction Count 1 × (0.8×0.4 + $\frac{4}{2}$×0.6) × $\frac{1}{2.4\times10^9}$ ≒ 6.3×10^{-10} × Instruction Count 1

∴ CPU Time 1N < CPU Time 2 , $\frac{7.2\times10^{-10}}{6.3\times10^{-10}} = \frac{8}{7}$ ≒ 1.14

⇨ New CPU1 is faster , 比 CPU2 快約 1.14 倍

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3. ① beq ⇨ target address = PC + offset × 4 (PC+4+offset×4)

② J ⇨ target address = PC (PC前 4bits + Label shift 2 bits)

③ Jal ⇨ target address = PC + $ra

(請翻面繼續作答)

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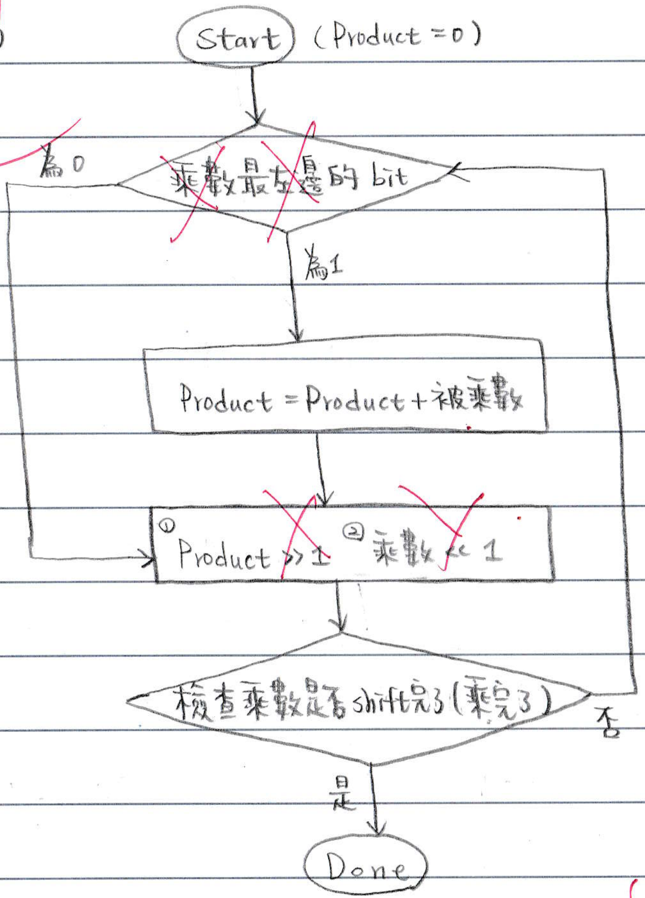
4. (a)



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(b) Multiplicand = 0101 , Multiplier = 0100

Cycle 1: 乘數最左邊的bit為0

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Product = 0 , Multiplier = 100X

↓

尚未shift完

↓

Cycle 2: 乘數最左邊的bit為1

↓

Product = 0000 + 0101 = 0101

↓

Product = 0101 , Multiplier = 00XX

↓

尚未shift完

↓

Cycle 3: 乘數最左邊的bit為0

↓

Product = 00101 , Multiplier = 0XXX

↓

尚未shift完

↓

Cycle 4: 乘數最左邊的bit為0

Product = 000101 , Multiplier = XXXX

↓

shift完畢

↓

5

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Done : Product = $(00010100)_2 = (20)_{10}$

5. (a) ① MIPS 分成 3 種 type 的 Instructions , Intel 則是將 32 bit 指令切成一半(各16bit)

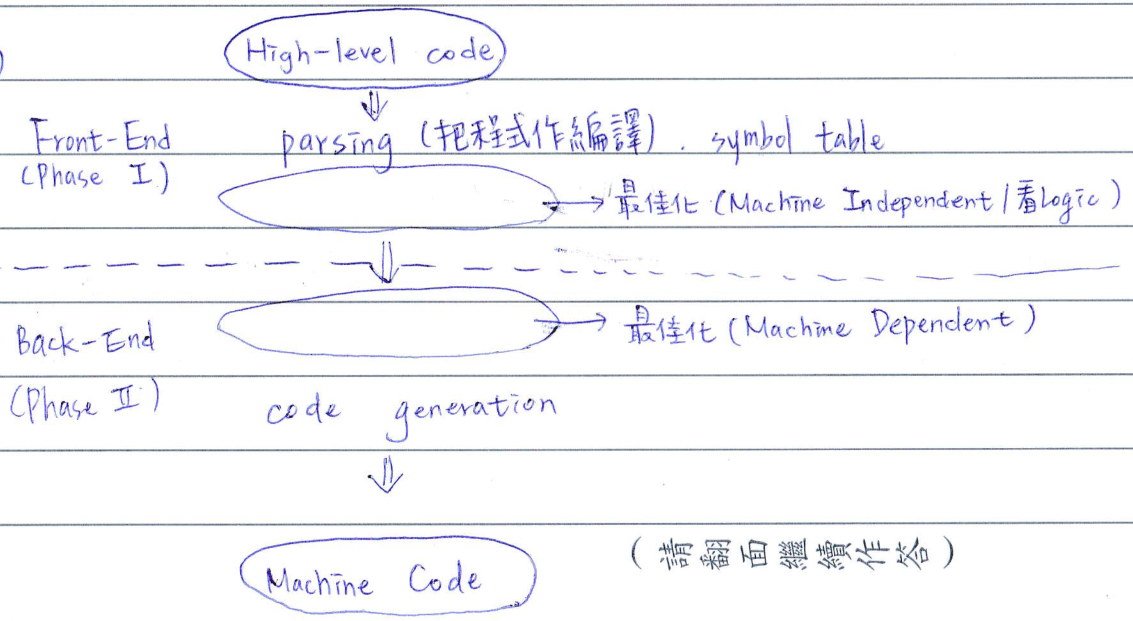
② Intel 為 4 bits 一單位, MIPS 則不一定 (5 or 6 bits)

(b) Phase I　parsing

Phase II　optimization + code generation

(a) ① 長度不同 ② 格式不同 ③ 複雜度不同

(b)


High-level code
Front-End (Phase I)
parsing (把程式作編譯) . symbol table
最佳化 (Machine Independent / 看Logic)
Back-End (Phase II)
最佳化 (Machine Dependent)
code generation
Machine Code

(請翻面繼續作答)