2017 Computer Architecture Midterm Exam (Total Scores=100) 2017/11/23

1. Translate the following C codes into the MIPS assembly code. (10, 15 pts)

(a)
```
Int Test(int n)
{    if (n>0 && n<5) return (0);
     else return (1);
}
```

(b)
```
Int fab(int n)
{
     if (n<3) return (1);
     else return ( fab(n-1) + fab(n-2) );
}
```

2. We have two processors CPU1 and CPU2, which have different parameters as shown in the following table.

$= \frac{\text{Instruction Count} \times CPI}{\text{clock Rate(GHz)}}$ 10^9

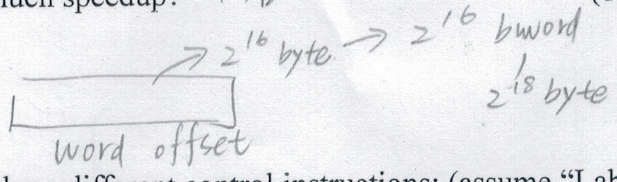
Processor	Clock rate	Integer CPI	Floating Point CPI
CPU1	2.4GHz	0.8	4 ×2
CPU2	2GHz	0.6 ($\frac{\text{Clock}}{指令}$)	2

Instruction × CPI = clock cycles

CPU Time = Instruction Count × CPI × Clock Cycle Time

(a) Now we have a program A which contains 40% integer instructions and 60% floating-point instructions. Is it true that CPU1 has a higher clock rate, so it is faster than CPU2 for program A? Explain your answer. (10 pts) pro A.

(b) Now we have a new hardware to execute floating-point operations, which has 2 times speedup, compared with the old floating-point version. We implement this new hardware only on CPU1, and let "New CPU1" execute program A again. Which CPU is faster for program A, "New CPU1" or "CPU2"? By how much speedup? 了倍. (10 pts)



3. A MIPS processor has three different control instructions: (assume "Label" is the position of an instruction)

```
beq     $t1, $t2, offset;
J       Label;
Jal     Label;
```

8 byte/4 = 2 wooor

address ⇒ ○/4

Explain how to calculate their target addresses (i.e., the address of branch or jump) for each of them? (Hint. Reference the value of "PC") (15 pts)

取指令 Jump 的 4 bits pc RIL counter.

4. Fig. 1 shows a design for the multiplication operations. (10 pts, 10 pts)

(a) Draw the flowchart to illustrate how the multiplication can be performed on Fig. 1

(b) Use the design of Fig. 1 to compute 5*4. =20

(Assume that we use four bits to represent the multiplicand and the multiplier.)

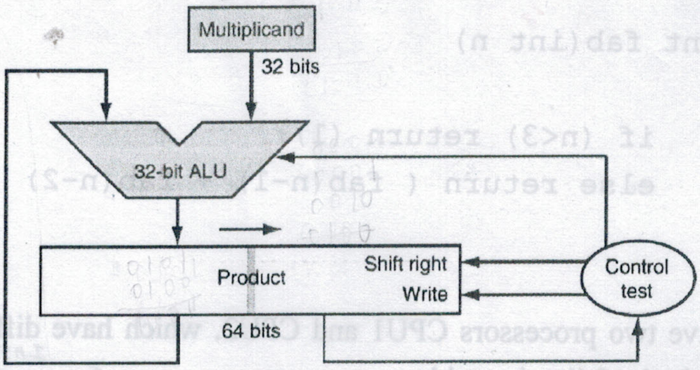


Fig. 1

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5. Explain the following questions based on your understanding. (10 pts, 10 pts)

None

(a) List at least two different features between the MIPS ISA and the Intel ISA.

(b) A typical compiler will have two compiling phases, front-end and back-end. Explain the major differences between these two phases.