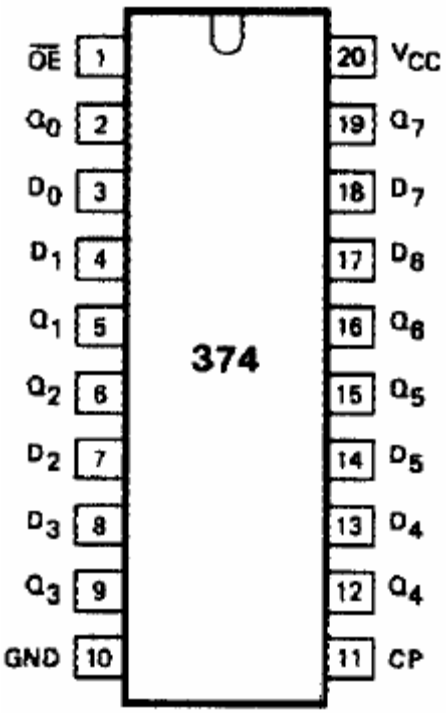
TRANSFER BETWEEN REGISTERS and THREE STATE LOGIC

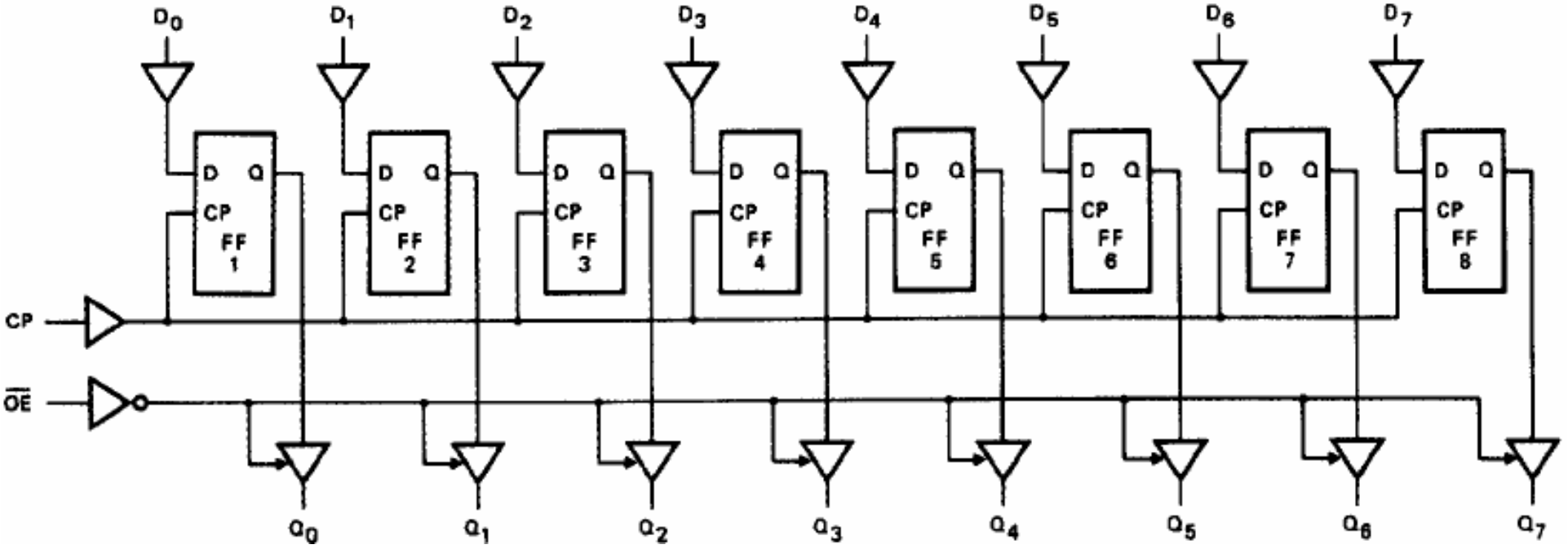
Introduction

- Bus design is made using **Three State Logic**, implemented at circuit outputs
- For information transfer, usually are used three state registers, three state bus amplifiers (uni or bi directional), together with decoders
- Important examples will follow

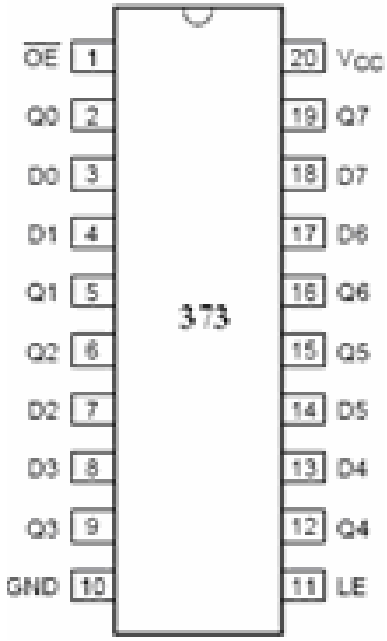
74374 REGISTER



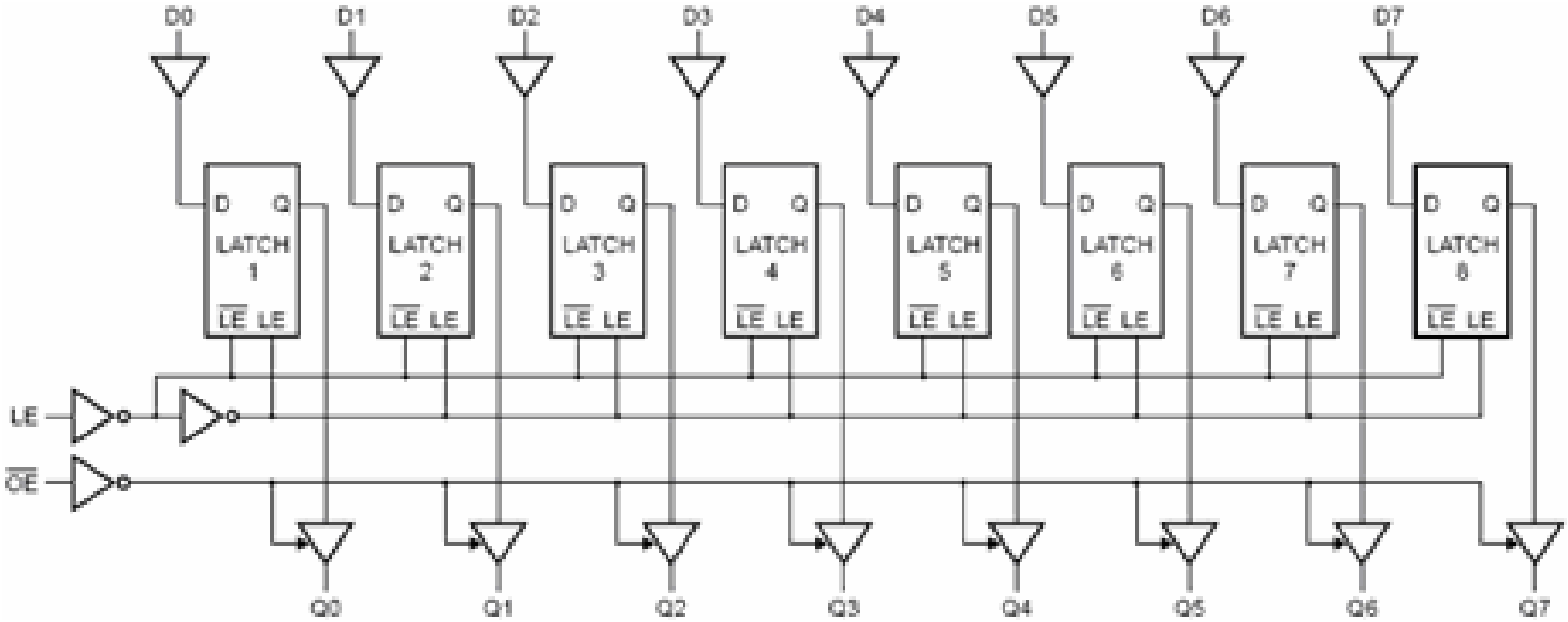
- 8 D type flip flops, outputs are buffered with three state circuits, activated using Output Enable command signal OE\ (signal is effective on '0' logic); so, output data will be available if signal OE\ is Low
- Writing data into register is made on the positive front of clock signal CP



74373 Register

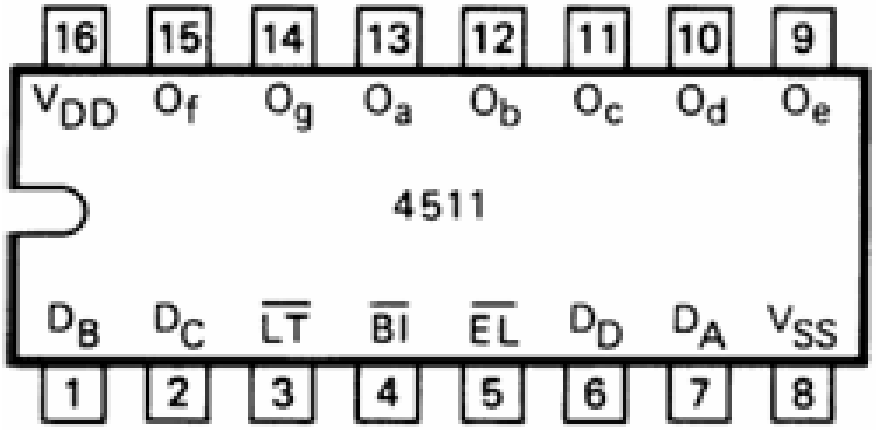


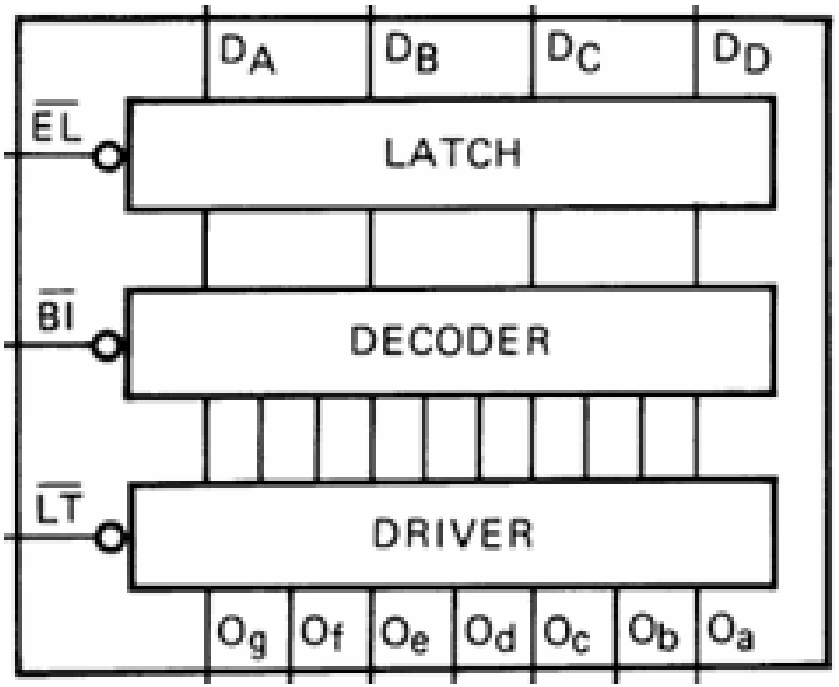
- 8 D type flip-flops, with outputs buffered with three-state circuits, enabled with OE\ input, zero-active
- Data are sent at outputs while LE input is ‘1’.
- When LE goes ‘0’ data are stored in latches.



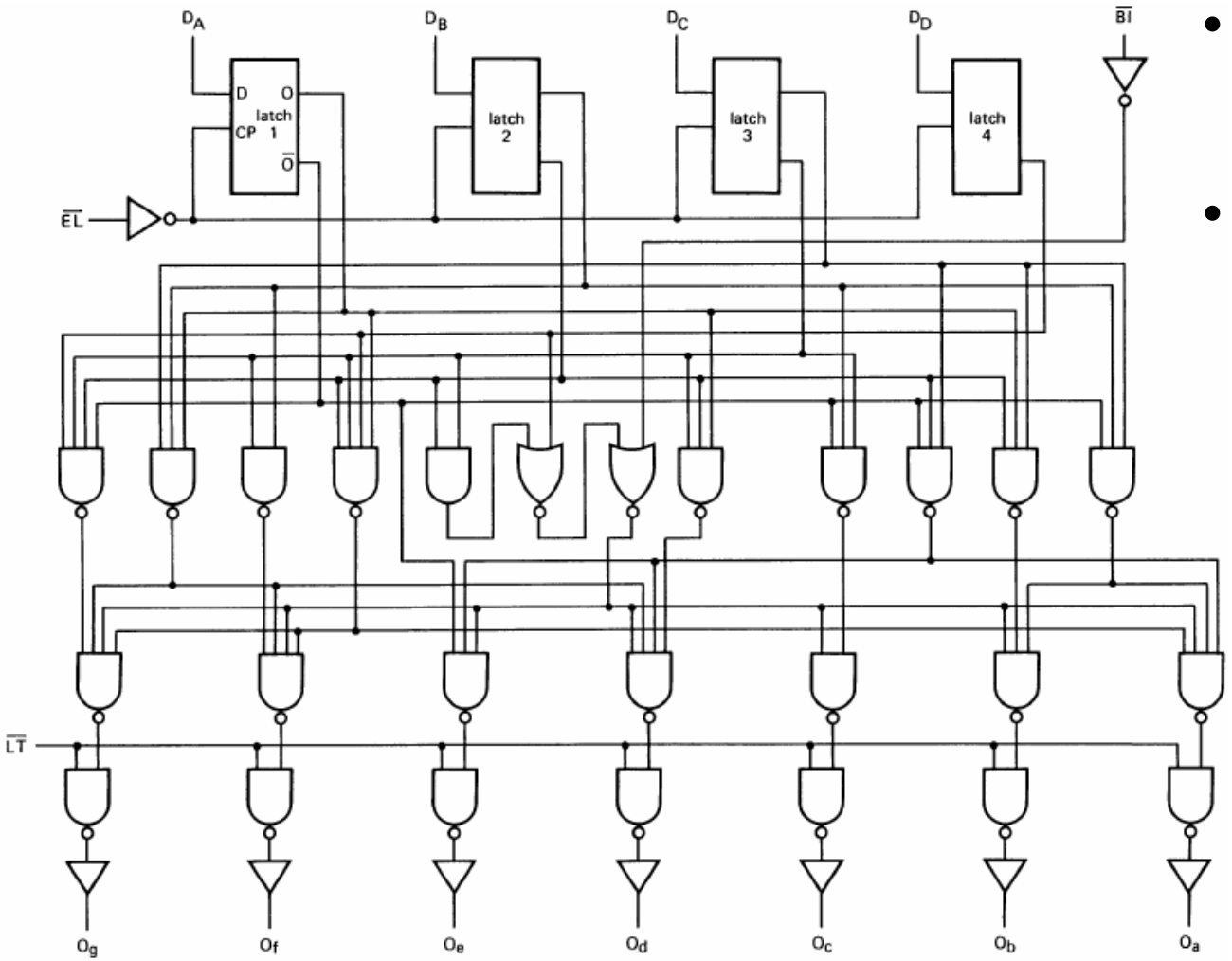
4511 - latch, decoder, driver

- Control of 7-segments LED display
- Functions: latch, decoder BCD to7 segments and driver
- 4 data inputs (D_A-D_D)
- 1 latch enable input, ‘0’ active (EL\)
- 1 blanking input (all segments off) , ‘0’ active (BI\)
- 1 test lamp input (all segments on), ‘0’ active (LT\)
- 7 outputs for segments, ‘1’ active(O_a-O_g)





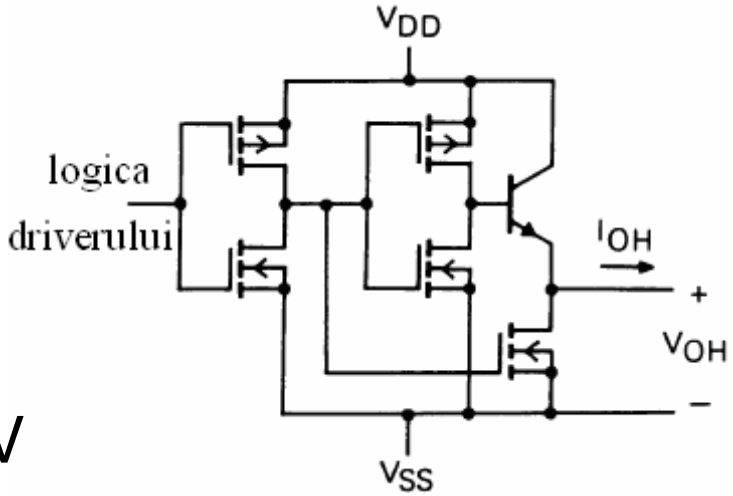
- When EL\ is ‘0’, O_a-O_g are imposed by D_A–D_D
- When EL\ is ‘1’, last values for D_A-D_D are latched and O_a-O_g present steady values
- If LT\ is ‘0’, O_a-O_g are ‘1’ no matter input values

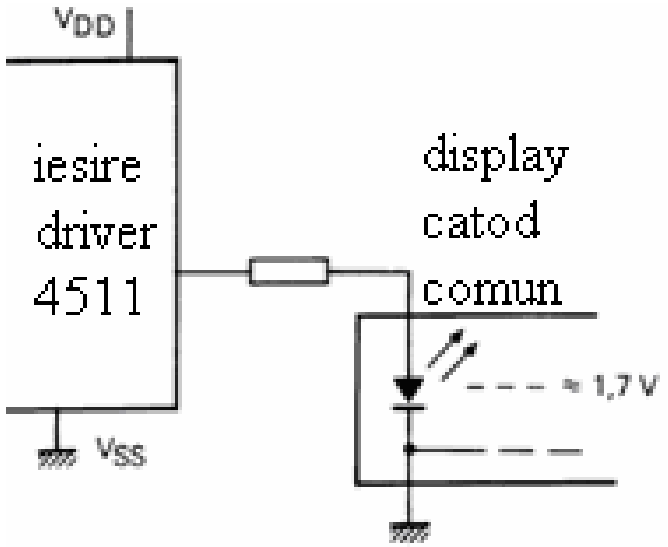


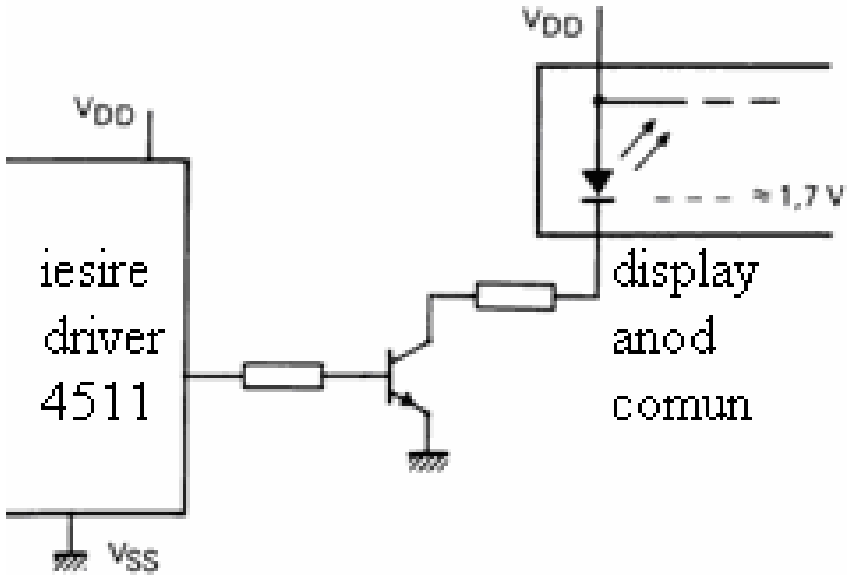
- If LT\ is ‘1’, ‘0’ value for BI\ drives O_a-O_g into ‘0’
- If LT\ and BI\ are ‘1’, outputs O_a-O_g present values depending on decoder

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{BI}$	$\overline{LT}$	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X				*				*

- For having a high value for the output current, the output circuit is a bipolar transistor
- Output voltage depends on the generated current
- For V_{DD}=5V:
- I_{OH}=0mA->V_{OHmin}=4,10V,V_{OHtyp}=4,40V
- I_{OH}=10mA->V_{OHmin}=3,60V,V_{OHtyp}=4,25V
- I_{OH}=20mA->V_{OHmin}=2,80V,V_{OHtyp}=4,20V

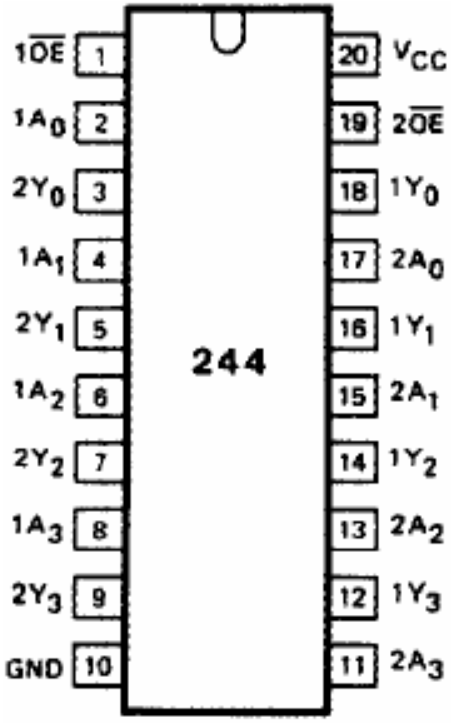


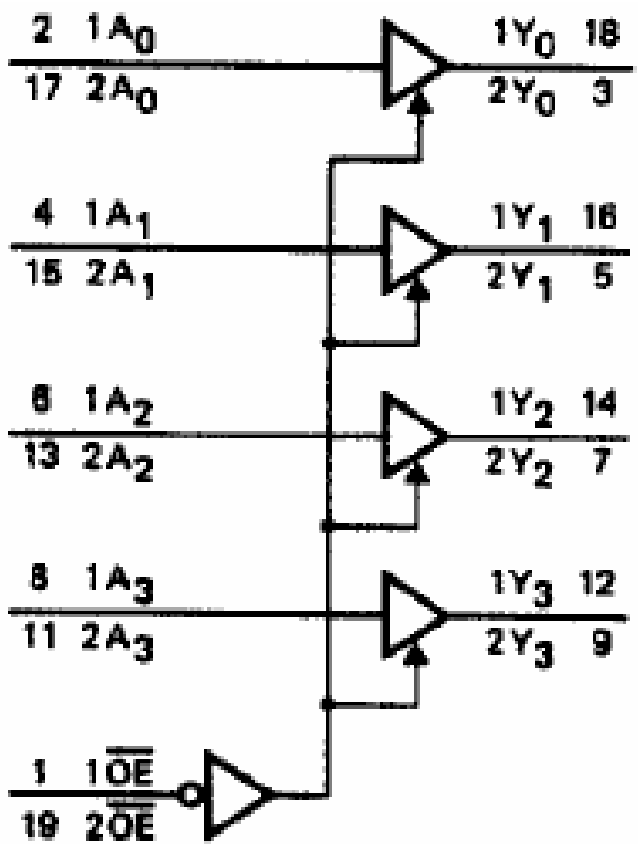




Unidirectional Amplifier 74244

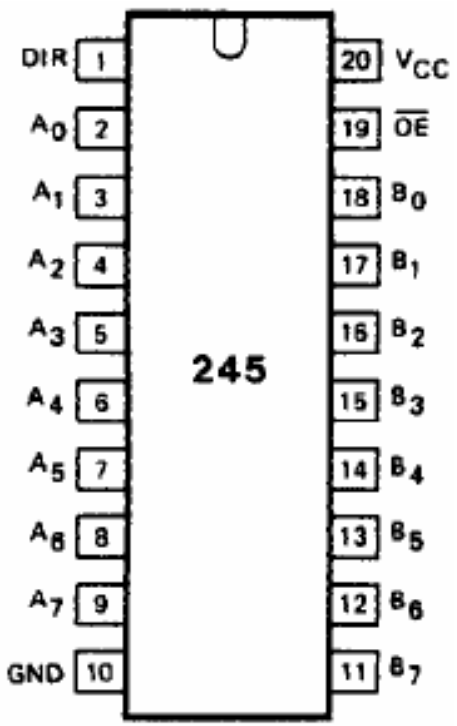
- 8 three state amplifiers, outputs are effective if enable signals 1OE\ and 2OE\ are Low
- The two enable input signals allow to activate independentely each set of 4 outputs: outputs $1Y_0 – 1Y_3$ will be enabled by low active signal 1OE\ and outputs $2Y_0 – 2Y_3$ will be enabled by signal 2OE\

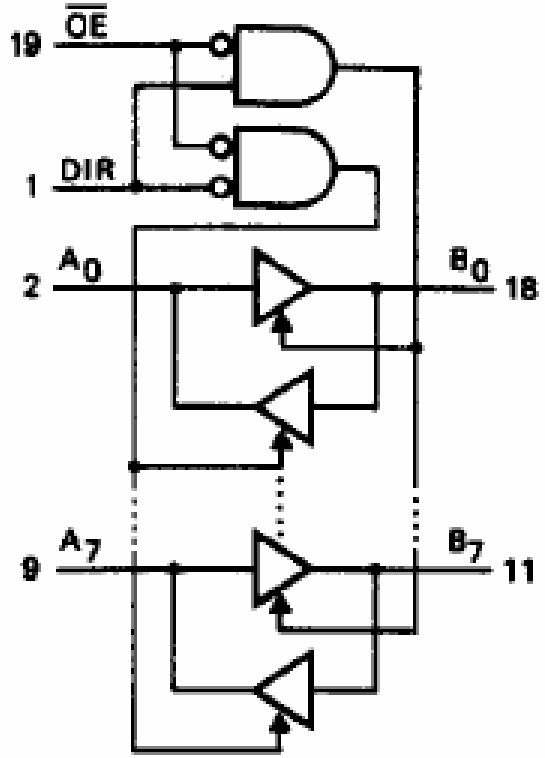




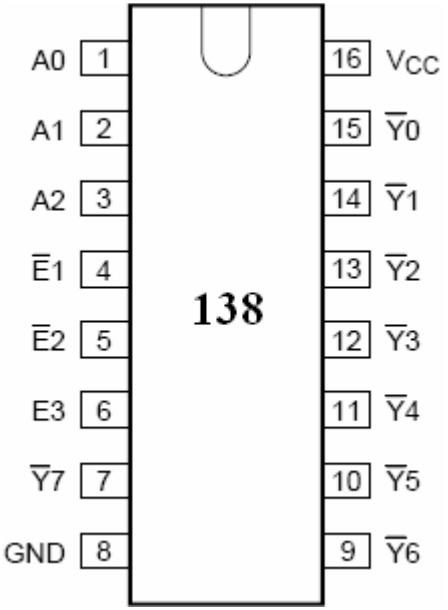
Bidirectional Amplifier 74245

- 16 three state amplifiers, eight for each direction
- Logoc state for DIRECTION input signal DIR allows selecting group of eight amplifiers whos outputs may be activated (enabled) : DIR=‘1’ data sent from inputs A_i to outputs B_i, DIR=‘0’ data sent from inputs B_i to outputs A_i
- OE\=‘1’ disables all outputs, OE\=‘0’ enables outputs selected by signal DIR





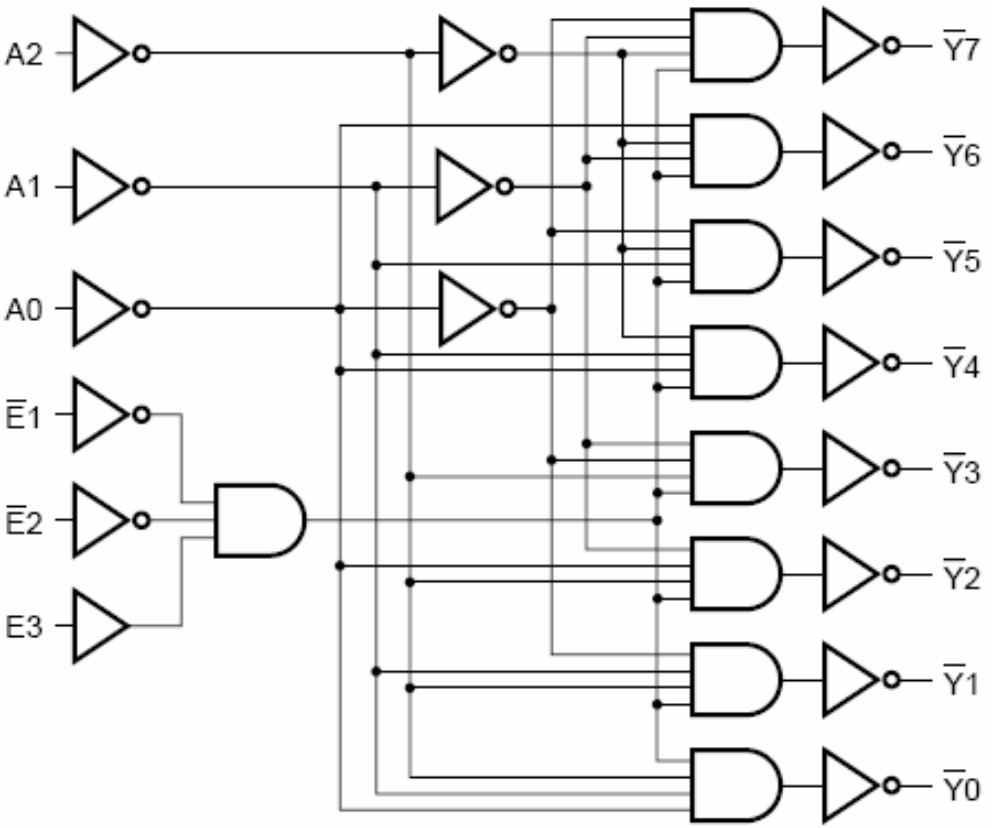
Decoder 74138



3 address inputs, 8 Low active outputs and

3 enable signals

If E1\=‘0’, E2\=‘0’ si E3=‘1’ output Y_i\ selected by binary combination of address signals A0, A1& A2, will be ‘0’, the rest of outputs being ‘1’



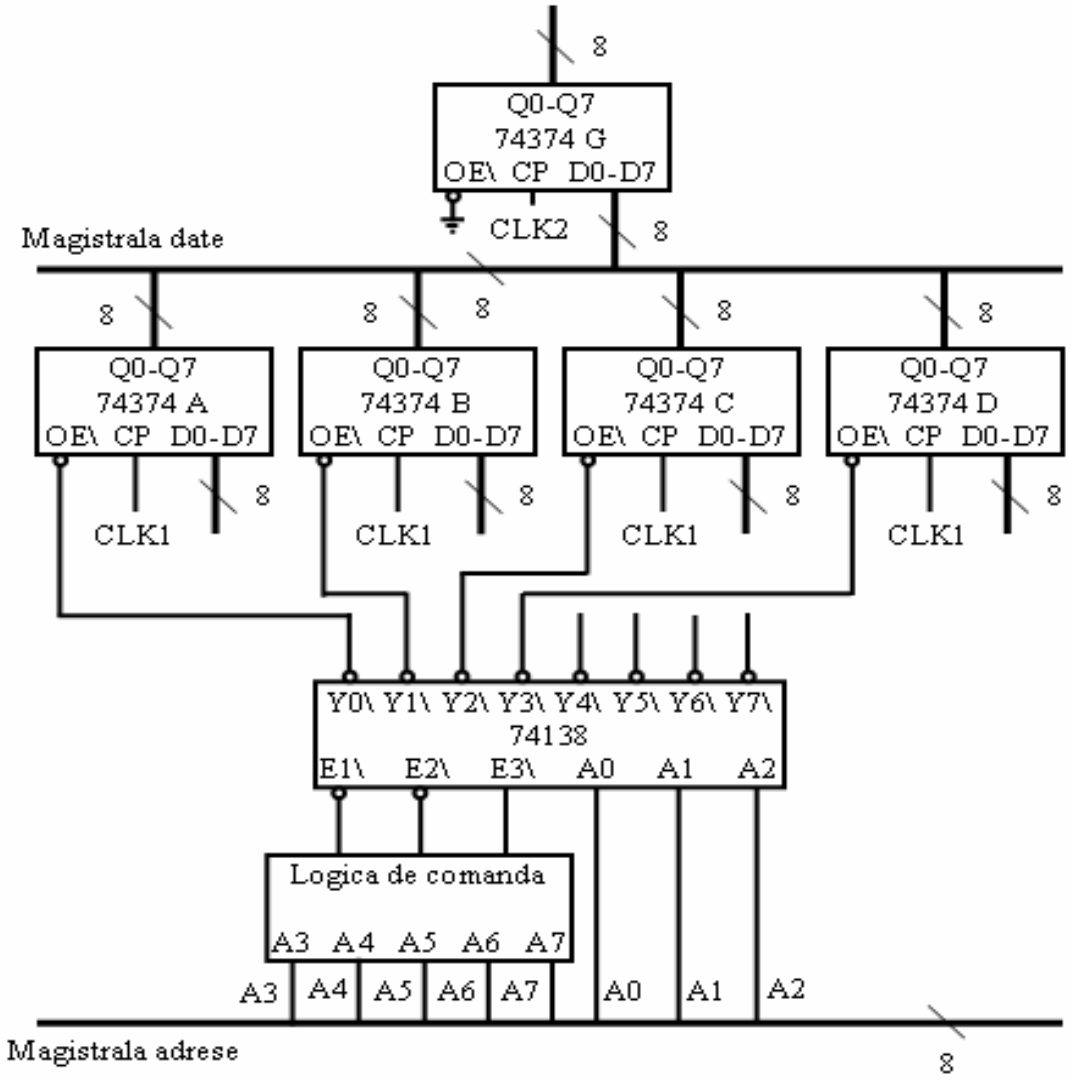
For any other combination of values for enable inputs E1, E2 & E3, all outputs will be ‘1’

For disabled circuit, all outputs will NOT be in HZ state, but in logic ‘1’; this way, the low active outputs will NOT select other circuits

TRANSFER BETWEEN REGISTERS (1)

Data from one (out of four registers: A, B, C or D), is transfered in a fifth one, G

Common data bus (8 lines), either output data from registers A, B, C or D, either input data for register G



Activating one register: a result of decoding some address lines from the address bus; corresponding active Output Enable line (OE\) will select register

For selecting a register all address lines are considered (total selection)

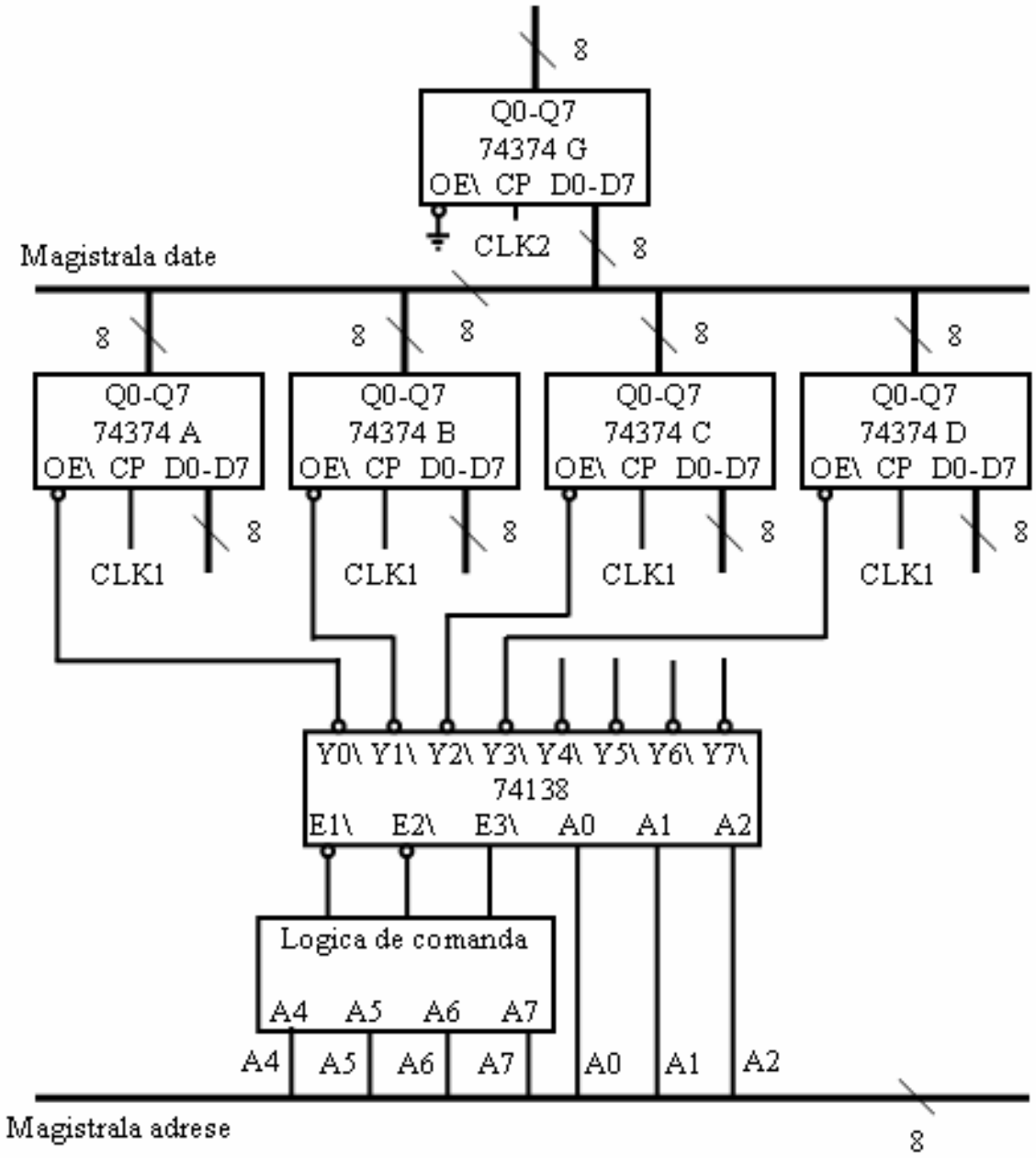
Advantage – all address space may be used

Drawback – selection circuit complex

Data writing made on raising edges of the clock signals CLK1 & CLK2

Register G is selected all time

REGISTER TRANSFER (2)



For partial selection method, only a part of address space is used

Advantage – lower complexity

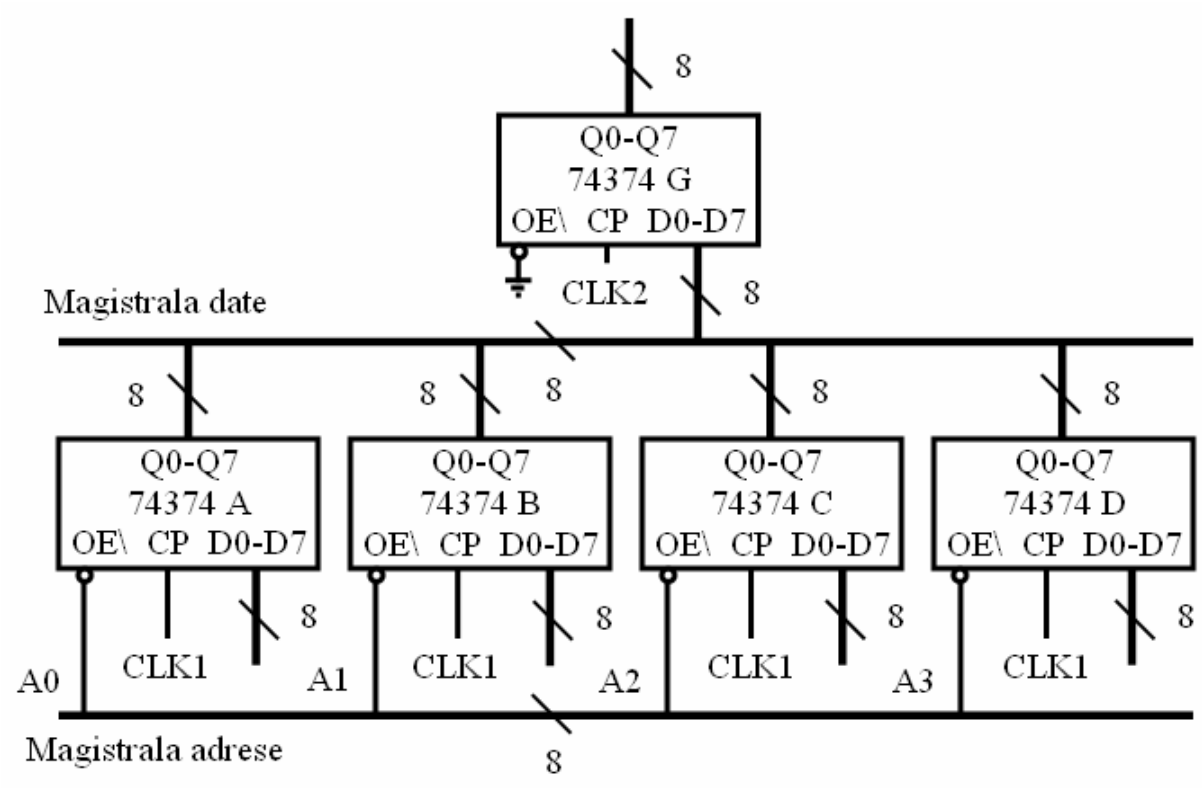
Drawback – fewer selection possibilities

REGISTER TRANSFER (3)

Linear selection method: only one address line used for selection

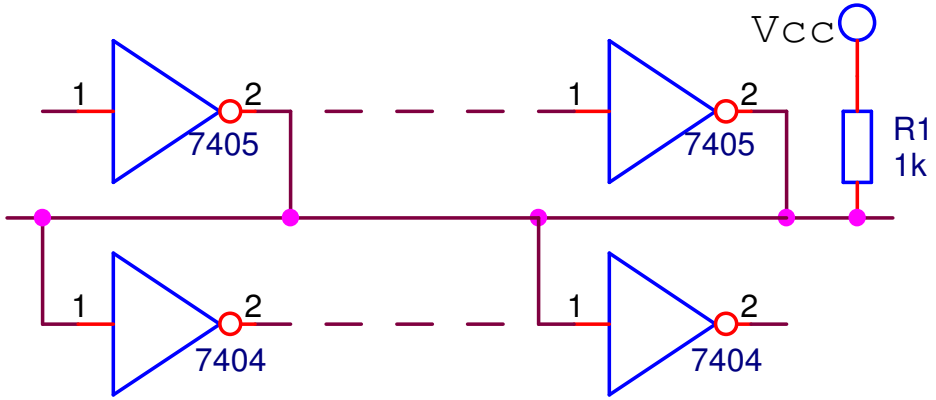
Advantage – minimum complexity

Drawback – very few possibilities for selecting within a more complex circuit



Proposed Problems

- Design an un-adapted transmission line with 5 OpenCollector transmitters and 5 TTL standard receivers.



$$R_{1\max} = \frac{V_{CC\min} - V_{OH\min}}{5I_{OH} + 5I_{IH}} \approx 1{,}6k\Omega$$

$$R_{1\min} = \frac{V_{CC\max} - V_{OL\max}}{I_{OL} + 4I_{OH} - 5I_{IL}} \approx 0{,}5k\Omega$$

$$R_1 = 1k\Omega$$

- Design an adapted line with 10 OC transmitters and 2 TTL standard receivers. Bus line has a characteristic impedance of Z_0 =250Ω.

$$R_{1\max} = \frac{V_{CC\min} - V_{OH\min}}{10\,I_{OH} + 2\,I_{IH}} \approx 910\Omega$$

$$R_{1\min} = \frac{V_{CC\max} - V_{OL\max}}{I_{OL} + 9\,I_{OH} - 2\,I_{IL}} \approx 322\Omega$$

$$R_1 = 330\Omega$$

$$Z_0 = \frac{R_1 R_2}{R_1 + R_2};\; R_2 = \frac{Z_0 R_1}{R_1 - Z_0} \approx 1k\Omega$$

$$V_{OH} = \frac{V_{CC\min} R_2}{R_1 + R_2} \approx 3{,}5V$$