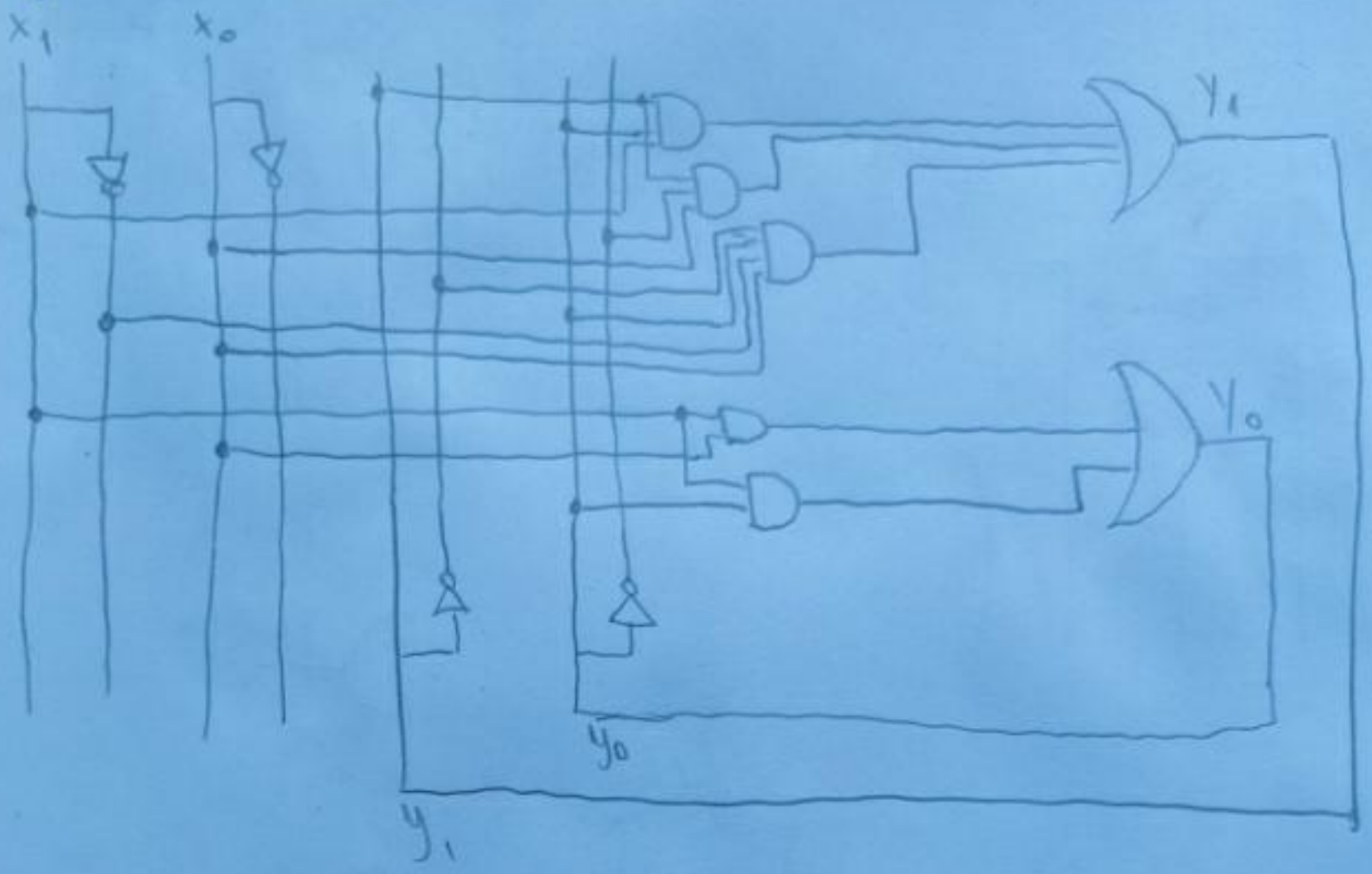
1.a)



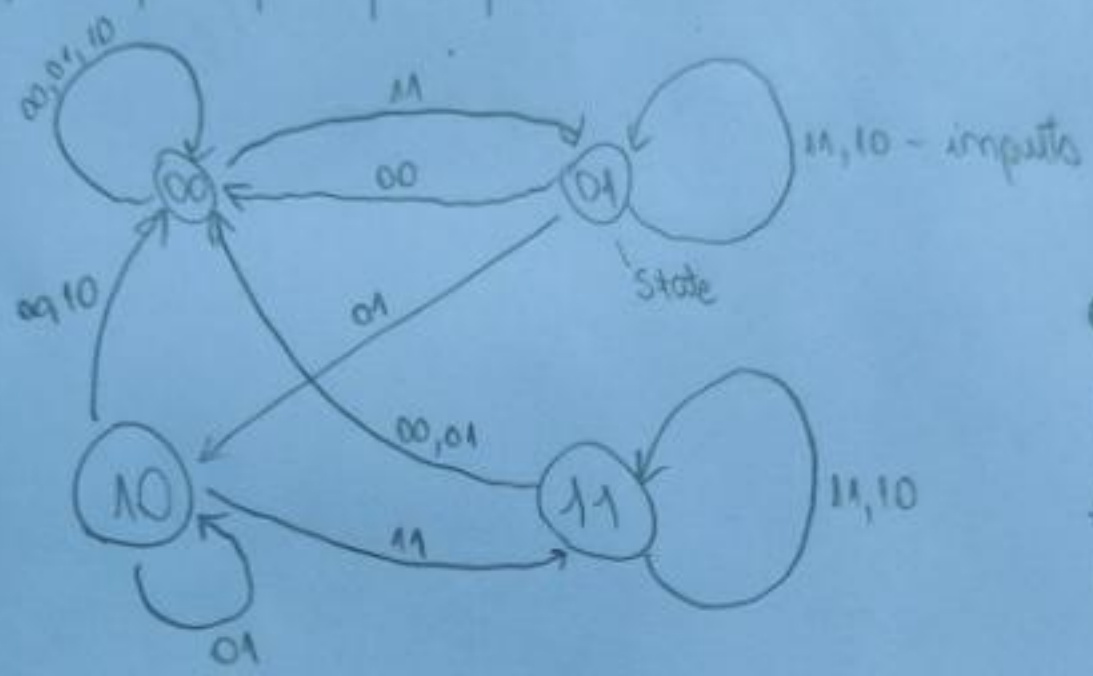
b)
```
library IEEE;
use IEEE.std_logic_1164.all;

entity E is
    port(x1, x0 : in std_logic);
end E;
architecture A of E is
    signal y1, y0, Y1, Y0 : std_logic;
begin
    Y1 <= (y1 and y0 and x1) or (y1 and not(y0) and x0) or
          (not(y1) and y0 and not(x1) and x0);
    Y0 <= (x1 and x0) or (x1 and y0);
    process(Y1, Y0)
        begin
        y1 <= Y1;
        y0 <= Y0;
    end process; end A;
```

c)

y_1y_0 \ x_1x_0	00	01	11	10
00	(00)	(00)	01	(00)
01	00	10	(01)	(01)
11	00	00	(11)	(11)
10	00	(10)	11	00

$\rightarrow Y_1Y_0$

d)



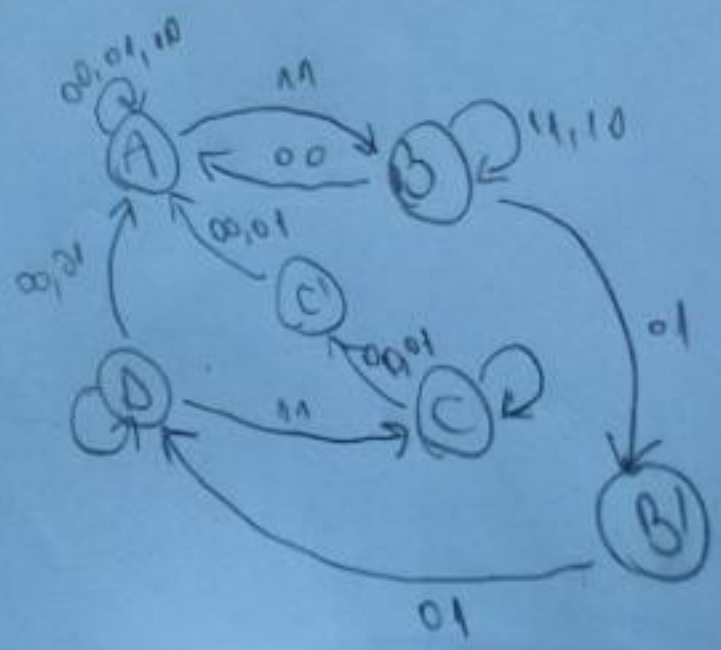
00: A
01: B
11: C
10: D

e) Potential problems in its functioning include critical races when we want to go from state 01 to state 10 and from state 11 to state 00.

f) No matter how the states are encoded, we will have a critical race so we have to add some extra states and increase the encoding to 3 bits.

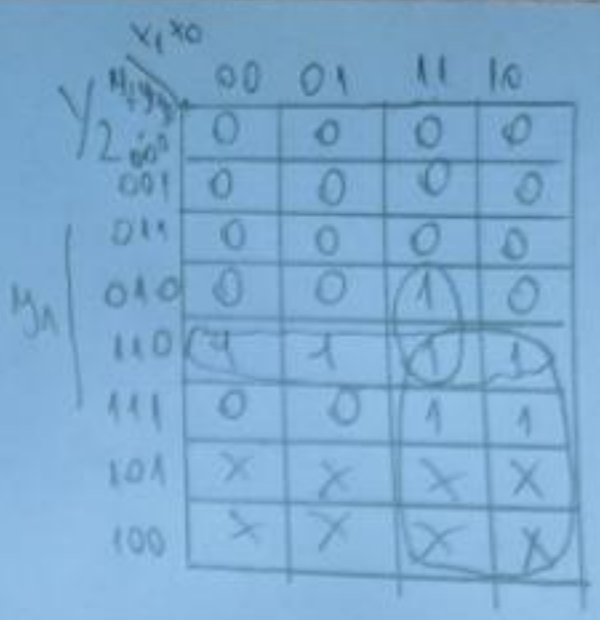
	00	01	11	10
0	B'	B	A	D
1	X	X	C'	C

C' is a clone of C
B' is a clone of B



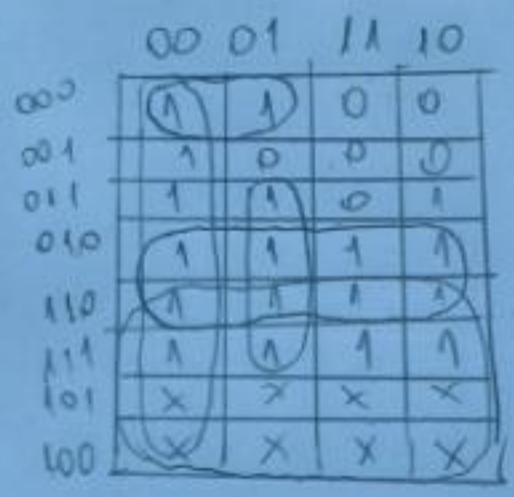
$y_2y_1y_0$ \ x_1x_0	00	01	11	10
B 000	011	010	000	000
B 001	011	000	001	001
A 011	011	011	001	011
D 010	011	010	110	011
C 110	111	111	110	110
C' 111	011	011	111	111
X 101	xx	xx	xx	xx
X 100	xx	xx	xx	xx

States transition table



$$Y_2 = y_2x_1 + y_2y_1\bar{y}_0 + y_1\bar{y}_0x_1x_0$$

Y_1:



$$Y_1 = y_2 + y_1\bar{y}_0 + \bar{x}_0\bar{x}_1 + y_1\bar{x}_1x_0 + \bar{y}_2y_1\bar{y}_0x_1$$

The groups that are in the top and bottom half of the KMAP have to be symmetrical to the half

Same for Y_0 (Kmap procedure)