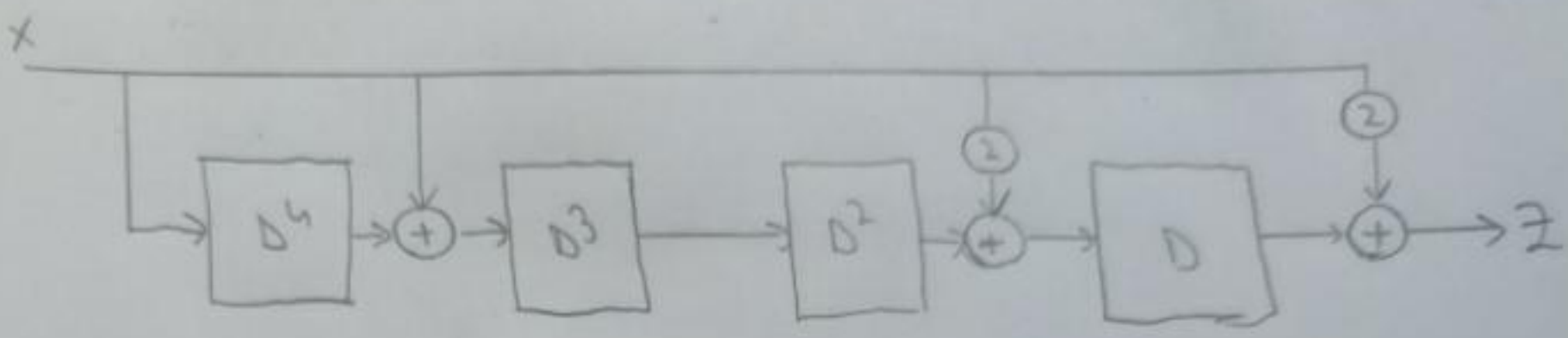
4. GF5

a) $T_1 = 1+D^3$, $T_2 = 1+2D+D^4$

They are connected in parallel, so $T_3 = T_1 + T_2$

$\Rightarrow T_3 = 2+2D+D^3+D^4$



b) c) According to the block schematic and the transfer function, the impulse response is $h = 22011$

d) The input sequence is 2123, so the response will be $2h + 0h + 2D^2h + 3D^3h$

h	2	2	0	1	1	0	0	0	0	...
$2h$	4	4	0	2	2	0	0	0	0	
Dh	0	2	2	0	1	1	0	0	0	
$2D^2h$	0	0	4	4	0	2	2	0	0	
$3D^3h$	0	0	0	1	1	0	3	3	0	
Response	4	1	1	2	4	3	0	3	0	0...

Response is obtained by adding the 4 lines, bit by bit, without carry, using operations in GF5

Response is 4112430300...0

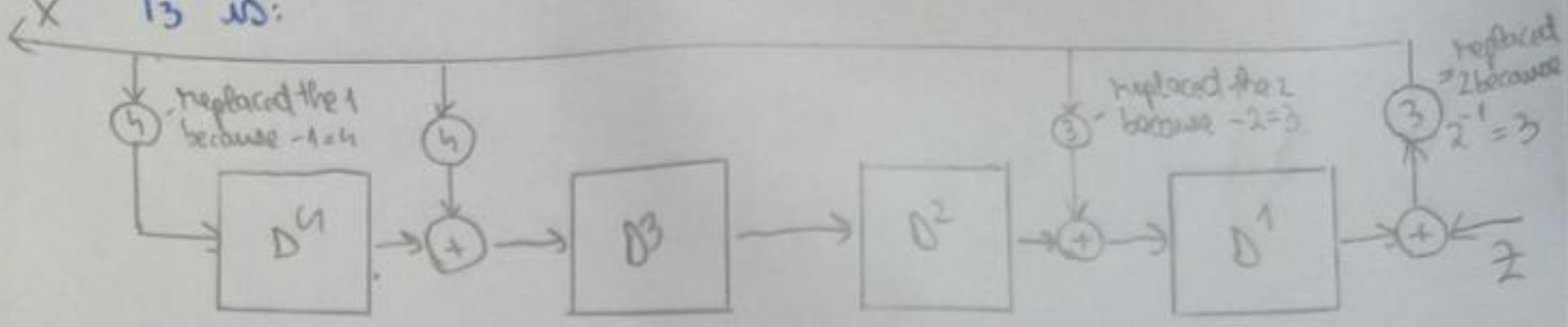
e) To get T_3^{-1}, we must first find:

$2^{-1} = 3$ in GF5 because $2 \cdot 3 = 1$

$-2 = 3$ in GF5

$-1 = 4$ in GF5

X T_3^{-1} is:



b) D flip flop in GF(5) on 4bits:

```
library IEEE;
use IEEE.std_logic_1164.all;

entity DFF is
    port(D: in std_logic_vector(3 downto 0);
         CLK: in std_logic;
         Q: out std_logic_vector(3 downto 0));
end DFF;
architecture A of DFF is
begin
 process(CLK)
    if CLK'EVENT and CLK='1' then
        Q<=D;
    end if;
 end process;
end A;
```

Top-level:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity T is
    port( CLK: in std_logic;
          X: in std_logic_vector(3 downto 0);
          Z: out std_logic_vector(3 downto 0));
end T;
```

```
architecture A of T is
begin
  process(CLK)
    variable v1, v2, v3, v4, v5, v6, v7, v8: std_logic_vector(3 downto 0);
    v1 := X(2 downto 0)&'0';
    v2 := v1;
    DFF: port map( D(3)=>v2(3  D => v2, Q => v3);
    v4 := X;
    DFF: port map (D => v4, Q => v5);
    DFF: port map(D => v5, Q => v6);
    v7 := X;
    DFF: port map (D => v7, Q => v8);
    v4 := X + v8;
    DFF: port map (D => v4, Q => v5);
    DFF: port map (D => v5, Q => v6);
    v3 := v4 + v1;
  end process;
  Z <= v1;
  end process;
end A;
```