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Problem 1

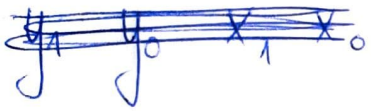
$Y_1 = y_1 y_0 x_1 + y_1 \bar{y_0} x_0 + \bar{y_1} y_0 \bar{x_1} x_0$;

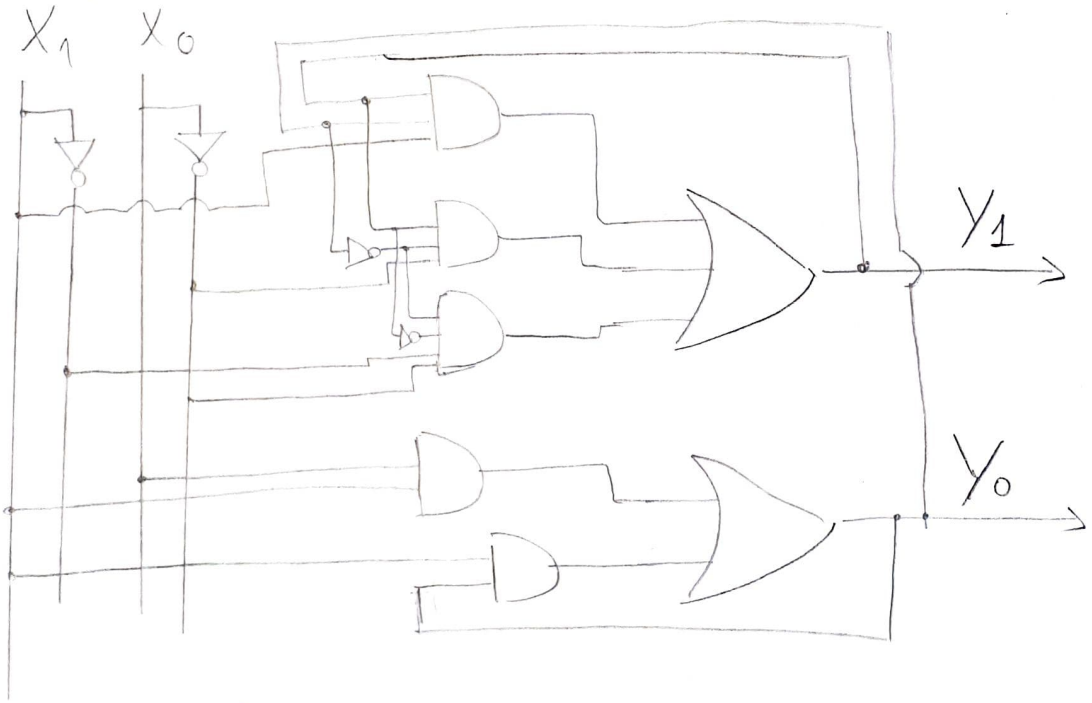
$Y_0 = x_1 x_0 + x_1 y_0$

– asyn automaton

a) Draw the schematic

x_1, x_0 – inputs





b) Implement in VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
```

```
entity prob1 is
    port( x1, x0 : in std_logic;
          Y1, Y0 : out std_logic);
end prob1;
architecture arh of prob1 is
signal y1, y0 : std_logic;
begin y1 <= 0; y2 := 0; -- initialization
    process (x1, x0)
    begin
        y1 <= (y1 and y0 and x1) or (y1 and (not y1) and x0)
              or ((not y1) or and y0 and (not x1) and x0);
        y0 <= (x1 and x0) or (x1 and y0);
    end process;
    Y1 <= y1;
    Y0 <= y0;
end arh;
```

c) Determine state transition:

State $y_1 y_0$ \ Inputs $x_1 x_0$	00	01	11	10
0 0	00/00	00/00	01/01	00/00
0 1	00/00	~~00/00~~	01/01	01/01
1 0	00/00	10/10	11/11	00/00
1 1	00/00	00/00	11/11	00/00

(I considered $Y_1 Y_0$ outputs here as well as functions) but it was not a good idea

outputs same as next state here

AND	
00	0
01	0
10	0
11	1

OR	
00	0
01	1
10	1
11	1

for 0000 ($y_1y_0x_1x_0$) $\Rightarrow y_1 = 0+0+0=0$
$y_0 = 0+0 = 0$

for 0001 $\Rightarrow y_1 = 0$
$y_0 = 0$

for 0010 $\Rightarrow y_1 = 0;\ y_0 = 0$

for 0011 $\Rightarrow y_1 = 0$
$y_0 = 1$

for 0100 $\Rightarrow y_1 = 0;\ y_0 = 0$

0101 $\Rightarrow y_1 = 0+0+1 = 1;\ y_0 = 0+0 = 0$

0111 $\Rightarrow y_1 = 0+0+1 = 0;\ y_0 = 1+1 = 1$

0110 $\Rightarrow y_1 = 0+0+0 = 0;\ y_0 = 0+1 = 1$

for 1000 $\Rightarrow y_1 = 0+0+0 = 0;\ y_0 = 0$

1001 $\Rightarrow y_1 = 0+1+0 = 1;\ y_0 = 0+0 = 0$

1011 $\Rightarrow y_1 = 0+1+0 = 1;\ y_0 = 1+0 = 1$

1010 $\Rightarrow y_1 = 0+0+0 = 0;\ y_0 = 0$

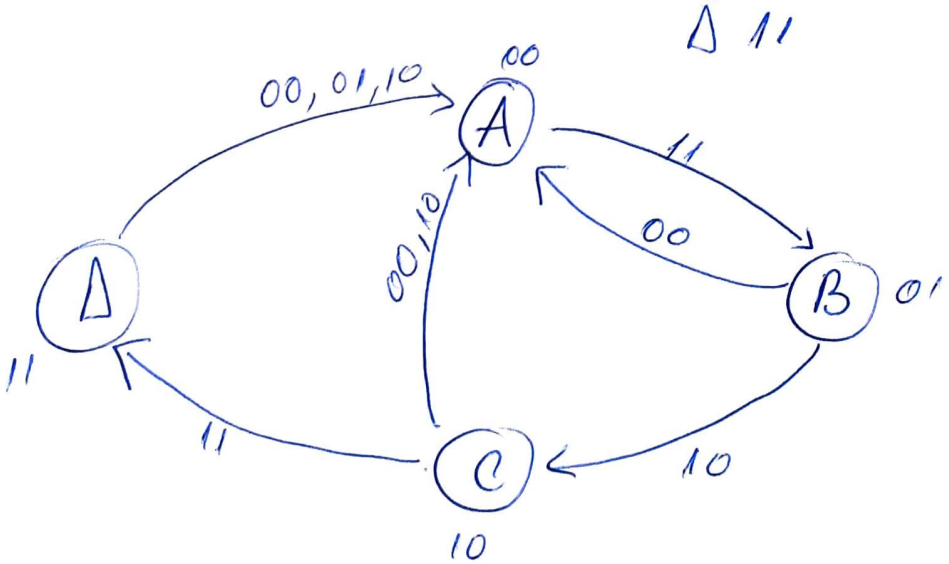
for 1100 $\Rightarrow y_1 = 0+0+0 = 0;\ y_0 = 0$

1101 $\Rightarrow y_1 = 0+0+0 = 0;\ y_0 = 0+0 = 0$

1111 $\Rightarrow y_1 = 1;\ y_0 = 1$

1010 $\Rightarrow y_1 = 0+0+0 = 0;\ y_0 = 0+0 = 0$

d) Transition graph
Encode states like this:
A 00
B 01
C 10
Δ 11

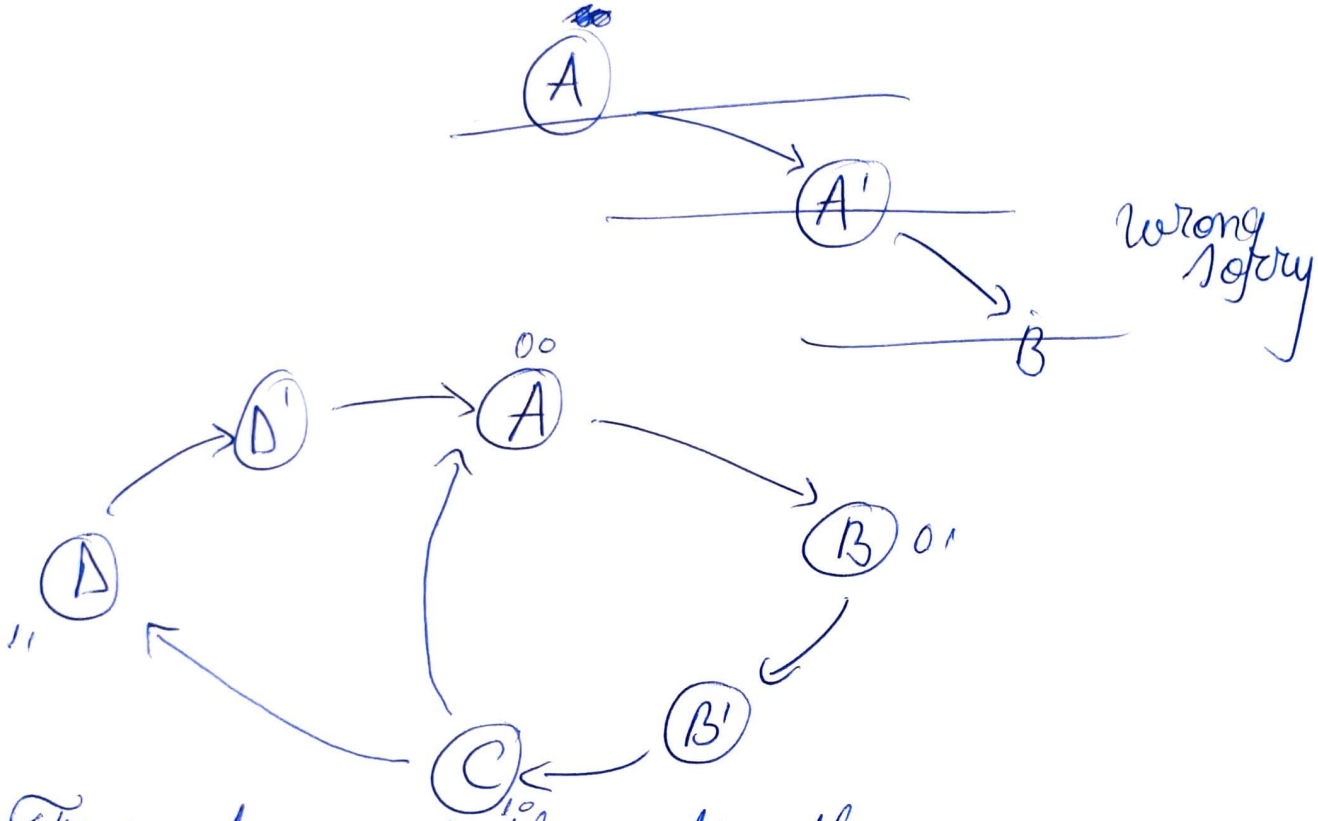


e) Potential problems are critical races: we have this kind of problem at the transition from:

$\Delta \rightarrow A \quad (11 \rightarrow 00)$

$B \rightarrow C \quad (01 \rightarrow 10)$

f) We can solve this by adding another state variable and two new states like so:



Trying to encode them adjacently:

	00	01	11	10
0	A_A	B_0	B'_0	C_C
1	Δ'_A	B_1	Δ_1	Δ_C

So we have: states:

000	A
001	B
010	C
011	B'
100	Δ'
101	—
110	Δ
111	—

g) New transition table:

States	X_1X_0 = 00	01	11	10
A 000	(000)	000	001	(000)
B 001	000	(001) (010)	(001)	(011)
C 010				
B' 011				
Δ' 100	000	000	(100)	000
— 101	—	—	—	—
Δ 110	100	100	(111)	100
— 111	—	—	—	—