Homework # 3

Due date: Nov. 3 (Thursday)

[Textbook]

Problem 6.3

PROBLEM 6.3 Consider a family of logic gates that operate under the static discipline with the following voltage thresholds: $V_{OL} = 1$ V, $V_{IL} = 1.3$ V, $V_{OH} = 4$ V, and $V_{IH} = 3$ V. Consider the N-input NAND gate design shown in Figure 6.63. In the design $R = 100k$ and R_{ON} for the MOSFETs is given to be $1k$. V_T for the MOSFETs is 1.5 V. What is the maximum value of N for which the NAND gate will satisfy the static discipline? What is the maximum power dissipated by the NAND gate for this value of N?

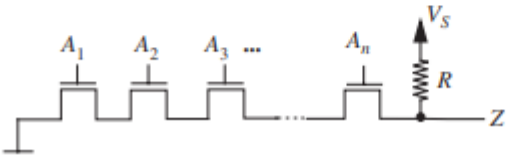


FIGURE 6.63

Problem 6.6 (b)

PROBLEM 6.6 Consider a family of logic gates that operate under the static discipline with the following voltage thresholds: $V_{OL} = 0.5$ V, $V_{IL} = 1$ V, $V_{OH} = 4.5$ V, and $V_{IH} = 4.0$ V.

b) Using the switch-resistor MOSFET model, design an inverter satisfying the static discipline for the four voltage thresholds using an n-channel MOSFET and a resistor. The MOSFET has $R_n = 1\,\text{k}\Omega$ and $V_T = 1.8$ V. Recall, $R_{ON} = R_n(L/W)$. Assume $V_S = 5$ V and $R_\square$ for a resistor is 500 Ω. Further assume that the area of the inverter is given by the sum of the areas of the MOSFET and the resistor. Assume that the area of a device is $L \times W$. The inverter should take as little area as possible with minimum size for L or W being 0.5 μm. Graph the input-output transfer function of the inverter. What is the total area of the inverter? What is its maximum static power dissipation?

Exercise 7.10 (a) (b)

EXERCISE 7.10 In this exercise you will perform a large signal analysis of the BJT amplifier shown in Figure 7.72. Assume that the BJT is characterized by the large signal model from Exercise 7.8. Assume further that $V_S = 5$ V, $R_L = 10$ kΩ, $R_I = 500$ kΩ, and $\beta = 100$.

a) Write an expression relating v_O to v_I.

b) What is the lowest value of the input voltage v_I for which the BJT operates in its active region? What are the corresponding values of i_B, i_C, and v_O?

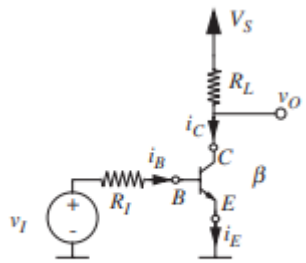


FIGURE 7.72

<The large signal model from Exercise 7.8>

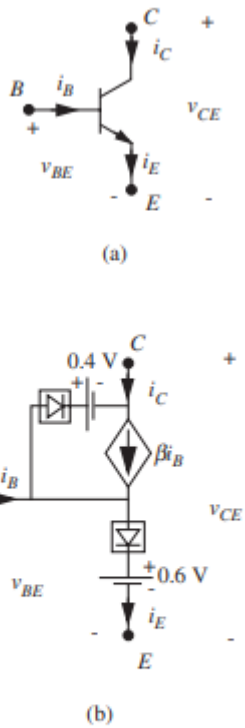


FIGURE 7.71 (a) A bipolar junction transistor. B stands for base, E for emitter, and C for collector; (b) a piecewise-linear model for the BJT.

EXERCISE 7.8 The three terminal device shown in Figure 7.71a is called a bipolar junction transistor (BJT). Figure 7.71b shows a piecewise-linear model for the device, in which the parameter β is a constant. When

$$i_B > 0$$

and

$$v_{CE} > v_{BE} - 0.4\ \text{V},$$

the emitter diode behaves like a short circuit, the collector diode like an open circuit, and the collector current is given by:

$$i_C = \beta i_B.$$

Under the given constraints, the BJT is said to operate in its active region. For the rest of this exercise, assume that $\beta = 100$:

Problem 7.2 (a) (c)

PROBLEM 7.2 An inverting MOSFET amplifier is shown in Figure 7.74, together with an i_{DS}–v_{DS} characteristic for the MOSFET. This characteristic is simpler than the SCS model presented in this chapter. The characteristic is simply the standard MOSFET characteristic with the triode region compressed onto the y-axis.

Alternatively, this characteristic can be viewed as describing ideal switch behavior that is extended to exhibit a saturating drain-source current. In other words, for $v_{GS} < V_T$, the MOSFET behaves like an open switch with $i_{DS} = 0$. For $v_{GS} \geq V_T$, the MOSFET behaves like a closed switch with $v_{DS} = 0$ provided that $i_{DS} < K/2(v_{GS} - V_T)^2$. However, once i_{DS} reaches $K/2(v_{GS} - V_T)^2$, which is the maximum current the MOSFET can carry for a given v_{GS}, MOSFET operation enters a saturation region in which the MOSFET behaves as a current source of value $K/2(v_{GS} - V_T)^2$. Saturated operation is as described by the saturation model given in Figure 7.74.

a) Determine v_{OUT} as a function of v_{IN} for $0 \leq v_{IN}$.

c) Assume that $V_S = 15$ V, $R = 15$ kΩ, $V_T = 1$ V, and $K = 2$ mA/V^2. Graph v_{OUT} versus v_{IN} for $0\ \text{V} \leq v_{IN} \leq 3\ \text{V}$.

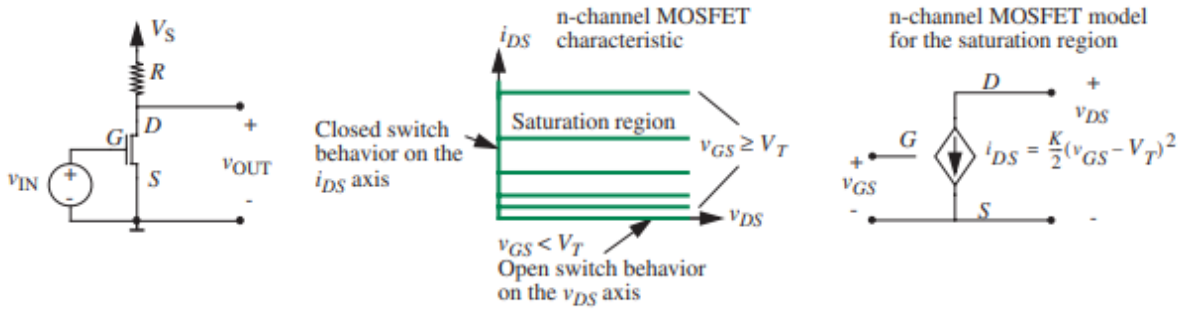


FIGURE 7.74

Problem 7.14

PROBLEM 7.14 Figure 7.85 shows a MOSFET amplifier driving a load resistor R_E. The MOSFET operates in saturation and is characterized by parameters K and V_T. Determine v_{OUT} versus v_{IN} for the circuit shown.

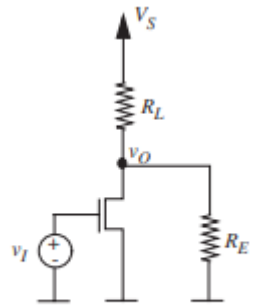


FIGURE 7.85

Problem 7.17

PROBLEM 7.17 Determine v_O versus v_I for the circuit shown in Figure 7.88. Assume that the MOSFET operates in saturation and is characterized by the parameters K and V_T.

Problem 9.1

PROBLEM 9.1 A voltage source is connected in series with two capacitors as shown in Figure 9.62. The source voltage is $V(t) = 5$ V $u(t)$, as shown. If the current i and voltage v are given by $i(t) = 4$ μC $\delta(t)$ and $v(t) = 1$ V $u(t)$, again as shown, what are C_1 and C_2?

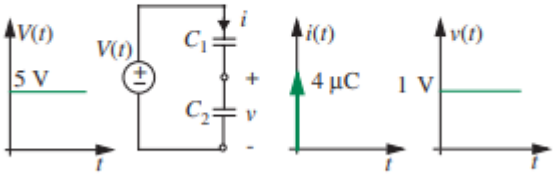


FIGURE 9.62

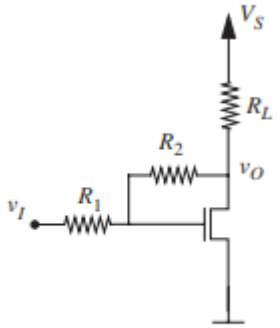


FIGURE 7.88

Problem 9.4

PROBLEM 9.4 A voltage source drives a parallel-connected capacitor and inductor as shown in Figure 9.65. Let $V(t) = V_o \sin(\omega t)u(t)$, and assume that the inductor and capacitor both stored no energy prior to $t = 0$.

Determine the current i for $t \geq 0$.

Is there any relation between V_o, ω, C, and L for which i is constant for $t \geq 0$? If so, state the relation and determine i.

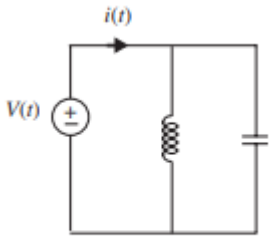
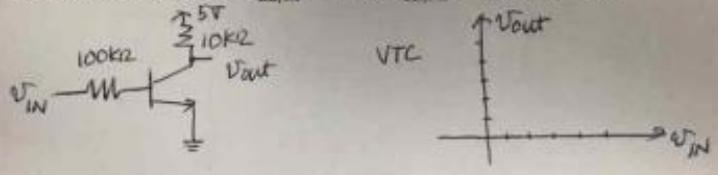


FIGURE 9.65

[Previous exams]

2019. 2nd exam

1. [15 points] 다음 BJT 인버터 회로에 대해서 물음에 답하시오.
Bipolar transistor characteristics: $V_{BE,on} = 0.7\,V$, $V_{CE,sat} = 0.2\,V$, $\beta = 100$



(a) [10 points] Bipolar 회로의 VTC (Voltage transfer characteristics)를 도시하여라. Bipolar junction transistor 의 동작 영역이 바뀌는 부분을 정확히 명시하여라.
Draw the VTC (Voltage transfer characteristics) of the BJT(bipolar junction transistor) inverter. Specify the voltage levels when the BJT changes its operation region.

(b) [5 points] BJT inverter를 증폭기로 사용하는 경우의 전압이득을 구하고 NMOS inverter 보다 증폭기로써 BJT 인버터가 더 좋은 이유를 설명하여라. Find the voltage gain when the BJT inverter is used as an amplifier and explain why it is better than the NMOS inverter as an amplifier.