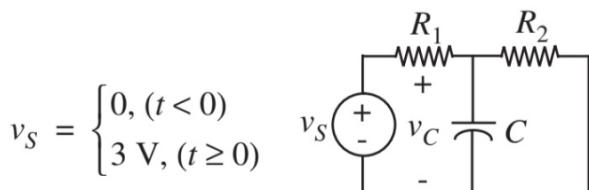
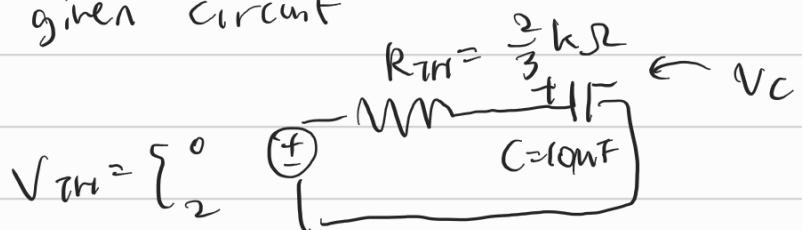


EXERCISE 10.11 In Figure 10.72, $R_1 = 1 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, and $C = 10 \mu\text{F}$. The driving voltage $v_S = 0$ for $t < 0$. Assume v_S is a 3-volt step at $t = 0$. Make a sketch of $v_C(t)$ for $t > 0$. Be sure to label the dimensions of the voltage and time axes and identify characteristic waveform shapes with suitable expressions.



First, we can find the Thevenin equivalent circuit of the given circuit



$$R_{TH} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2} = \frac{1 \cdot 2}{1+2} = \frac{2}{3} \text{ (k}\Omega\text{)}$$

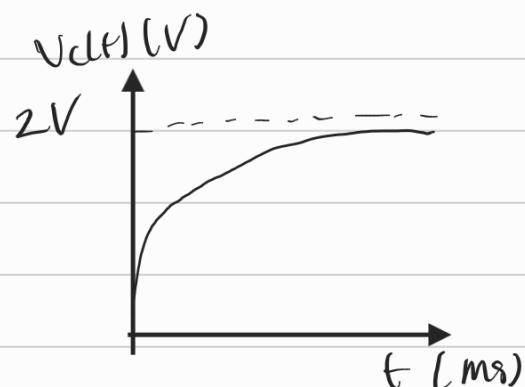
$$V_{TH} = V_S \cdot \frac{R_2}{R_1 + R_2} = V_S \cdot \frac{2}{1+2} = \begin{cases} 0 \text{ V } (t < 0) \\ 2 \text{ V } (t > 0) \end{cases}$$

In this RC circuit, $V_C(t)$ is of the form

$$V_C(t) = (V_C(0) - V_C(\infty)) e^{-t/\tau} + V_C(\infty)$$

Substituting $V_C(0) = 0$, $V_C(\infty) = 2$, $\tau = R_{TH}C = \frac{20}{3}$, we get the solution

$$V_C(t) = 2 \left(1 - e^{-\frac{3}{20}t} \right)$$



PROBLEM 10.1 Figure 10.92a illustrates an inverter *INV1* driving another inverter *INV2*. The corresponding equivalent circuit for the inverter pair is illustrated in Figure 10.92b. *A*, *B*, and *C* represent logical values, and v_A , v_B , and v_C represent voltage levels. The equivalent circuit model for an inverter based on the SRC model of the MOSFET is depicted in Figure 10.93.

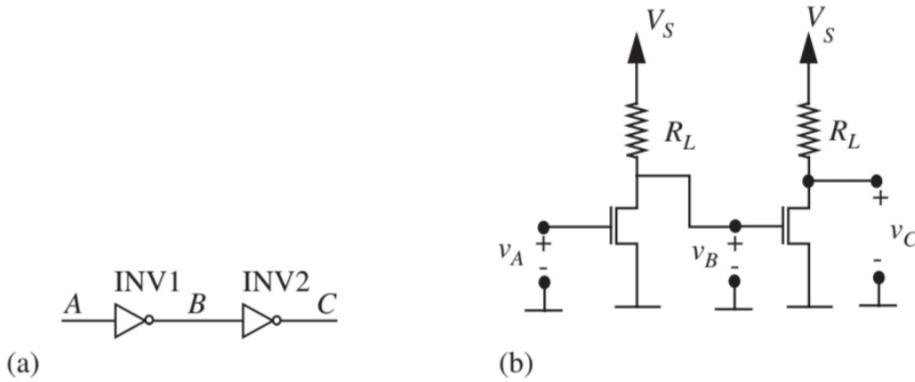


FIGURE 10.92

- a) Write expressions for the rise and fall times of *INV1* for the circuit configuration shown in Figure 10.92. Assume that the inverters satisfy the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$.

(Hint: The rise time of *INV1* is the time v_B requires to transition from the lowest voltage reached by v_B (given by the voltage divider action of R_L and R_{ON}) to V_H for a V_S to 0-V step transition at the input v_A . Similarly, the fall time of *INV1* is the time v_B requires to transition from the highest voltage reached by v_B (that is, V_S) to V_L for a 0-V to V_S step transition at the input v_A .)

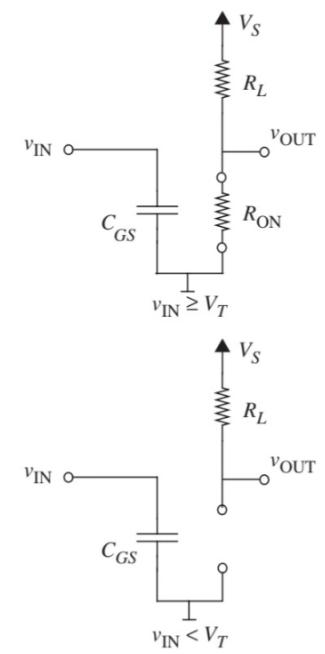
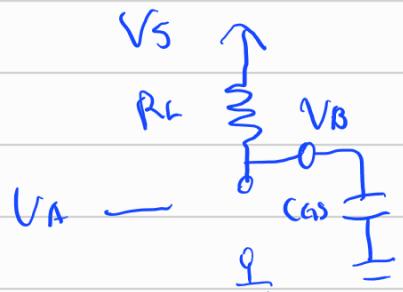


FIGURE 10.93

① Rise time

$$\text{Assume } v_B(t=0^-) = V_S \cdot \frac{R_{ON}}{R_L + R_{ON}}$$



Since the inverter in OFF state forms an RC circuit,

$v_B(t)$ is of the form

$$v_B(t) = (v_B(0) - v_B(\infty)) e^{-t/\tau} + v_B(\infty)$$

Substituting $v_B(0) = V_S \cdot \frac{R_{ON}}{R_L + R_{ON}}$, $v_B(\infty) = V_S$, $\tau = R_L C_{GS}$, we get :

$$v_B(t) = V_S \left(1 - \frac{R_L}{R_L + R_{ON}} e^{-t/R_L C_{GS}} \right)$$

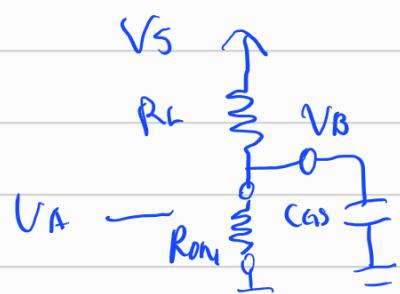
We can get the rise time t_{rise} by solving the equation $V_B(t_{rise}) = V_H$

$$e^{-t_{rise}/R_L C_{GS}} = \frac{(V_S - V_H)(R_L + R_{ON})}{V_S R_L}$$

$$t_{rise} = -R_L C_{GS} \ln \frac{(V_S - V_H)(R_L + R_{ON})}{V_S R_L}$$

② Fall time

We can find the Thevenin equivalent circuit for the inverter in ON state



$$R_{TH} = R_L // R_{ON} = \frac{R_L R_{ON}}{R_L + R_{ON}}$$

$$V_{TH} = V_S \frac{R_{ON}}{R_L + R_{ON}}$$



Note that $V_B(t=0^-) = V_S$

Then, V_B is of the form

$$V_B(t) = (V_B(0) - V_B(\infty)) e^{-t/\tau} + V_B(\infty)$$

$$V_B(0) = V_S, V_B(\infty) = V_S \frac{R_{ON}}{R_L + R_{ON}}, \quad \tau = R_{TH} C_{GS} = \frac{R_L R_{ON} C_{GS}}{R_L + R_{ON}}$$

$$\therefore V_B(t) = \frac{V_S}{R_L + R_{ON}} (R_{ON} + R_L e^{-\frac{t}{R_L R_{ON} C_{GS}}})$$

From $V_B(t_{fall}) = V_H$, we get

$$t_{fall} = -\frac{R_L R_{ON} C_{GS}}{R_L + R_{ON}} \ln \frac{V_L (R_L + R_{ON}) - V_S R_{ON}}{V_S R_L}$$

- b) What is the propagation delay t_{pd} of INV1 in the circuit configuration shown in Figure 10.92, for $R_{ON} = 1 \text{ k}\Omega$, $R_L = 10R_{ON}$, $C_{GS} = 1 \text{ nF}$, $V_S = 5 \text{ V}$, $V_L = 1 \text{ V}$, and $V_H = 3 \text{ V}$?

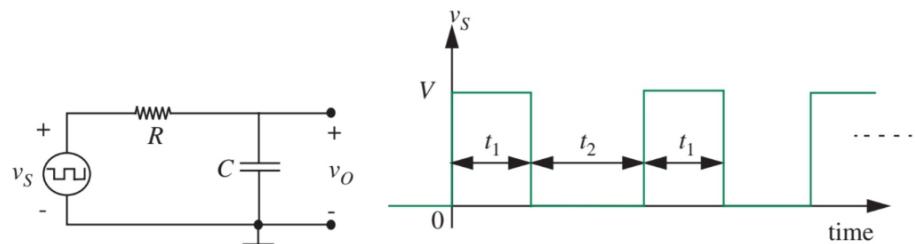
$$\text{rise time } t_{\text{rise}} \stackrel{(\mu\text{s})}{=} -10 \cdot 1 \cdot \ln \frac{(5-3)(1+10)}{5 \cdot 10} = \\ = -10 \ln \frac{1}{25} \doteq 8.2 \text{ } (\mu\text{s})$$

$$\text{fall time } t_{\text{fall}} \stackrel{(\mu\text{s})}{=} -\frac{1.6 \cdot 1}{10+1} \ln \frac{1 \cdot (1+10) - 5 \cdot 1}{5 \cdot 10} \\ = -\frac{16}{61} \ln \frac{3}{25} \doteq 1.9 \text{ } (\mu\text{s})$$

$$\text{propagation delay} = \max(t_{\text{rise}}, t_{\text{fall}}) \doteq 8.2 \text{ } \mu\text{s}$$

PROBLEM 10.12 You can see from Problem 10.10 that for circuit time constant $\tau \gg t_1$ and t_2 the capacitor voltage starts from some value V_{\min} and increases when v_S is positive; then when v_S is zero, v_O starts at some value V_{\max} and decreases. By definition, the “steady state” of the circuit is when v_O charges from V_{\min} to V_{\max} , then discharges from V_{\max} to the same V_{\min} . Assuming $t_1 = t_2$, sketch the v_O waveform in the steady state.

Find the average value of the voltage v_O . Problem 10.11 may give you a hint. Explain your answer. It may help to consider the waveform v_S to be made up of a DC voltage $V/2$ and a symmetrical square wave whose values alternate between $+V/2$ and $-V/2$.



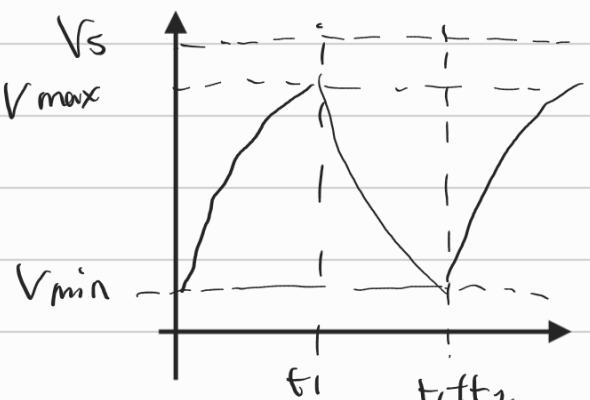
$$0 < t < t_1$$

$$v_o(0) = V_{\min}, \quad v_o(\infty) = v_s, \quad \tau = RC$$

$$\Rightarrow v_o = (V_{\min} - v_s) e^{-t/RC} + v_s$$

$$t_1 < t < t_1 + t_2 \quad (= 2t_1)$$

$$v_o(t_1) = V_{\max}, \quad v_o(\infty) = 0, \quad \tau = RC$$



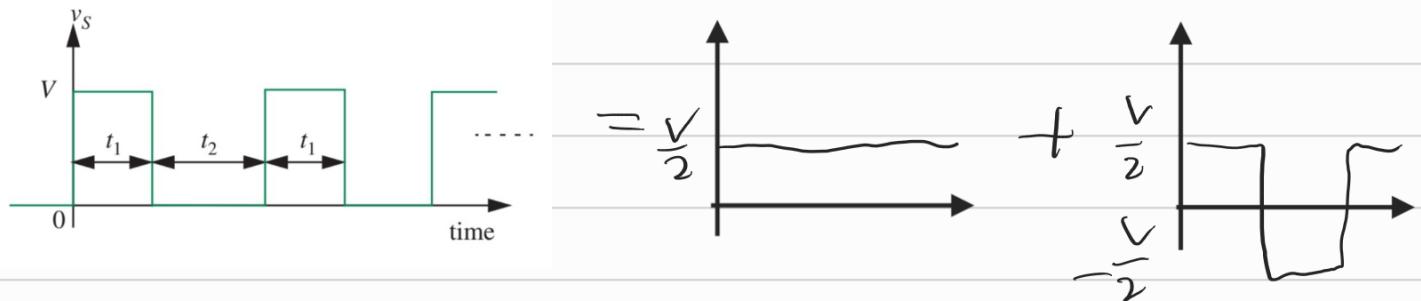
$$\Rightarrow v_o = V_{\max} e^{-(t-t_1)/RC}$$

$$V_s + (V_{\min} - v_s) e^{-t_1/RC} = V_{\max}$$

$$V_{\max} e^{-(t_1 + t_2 - t_1)/RC} = V_{\max} e^{-t_2/RC} = V_{\min}$$

Average voltage

Using the hint, we can think of V_s as the sum of a DC term and a symmetric square wave.



We can calculate each contribution of the DC term and the square wave by the superposition principle

Clearly, for the DC term, V_o is constant with the value of $V_o = V/2$.

For the symmetric square wave, the capacitor would be charged and discharged periodically and symmetrically.

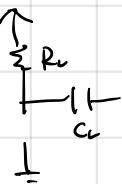
Therefore, one can figure out that the average contribution to V_o of the square wave would be 0.

∴ The average value of $V_o = \frac{V}{2}$

EXERCISE II.1 An inverter built using an NMOS transistor and a resistor R_L drives a capacitance C_L . The power supply voltage is V_S and the on resistance of the MOSFET is R_{ON} . The threshold voltage for the MOSFET is V_T . Assume that logical 0's are represented using 0 V and logical 1's using V_S volts.

- a) Determine the steady-state power consumed by the inverter when a 0 is applied to its input.

a) when the input is 0,

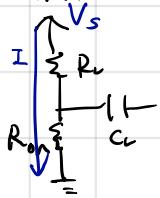


No current flows in the steady state.

$$\therefore P_{\text{steady-state}} = 0$$

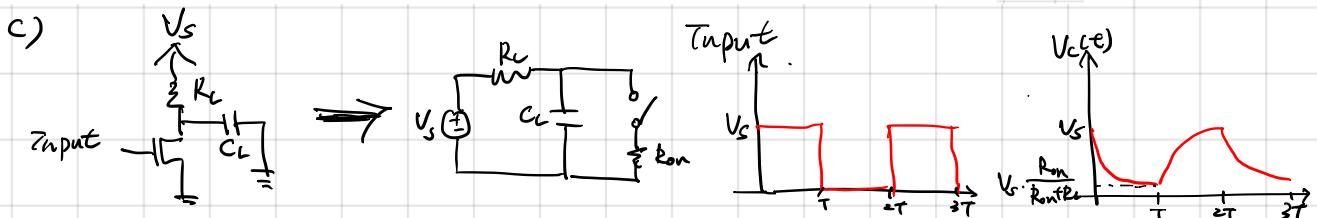
- b) Determine the steady-state power consumed by the inverter when a 1 is applied to its input.

b) when the input is 1,



$$\therefore P_{\text{steady-state}} = V_S \cdot I = \frac{V_S^2}{R_{ON} + R_L}$$

- c) Determine the static power and the dynamic power consumed by the inverter when a sequence of the form 01010101 ... is applied to its input. Assume that signal transitions (0 to 1, or 1 to 0) happen every T seconds. Assume further than T is much greater than the circuit time constant.



Solution 1

During the input is low

$$V_c(\infty) = V_s, \quad V_c(0) = V_s \frac{R_{on}}{R_L + R_{on}}, \quad \tau = R_L C_L$$

$$V_c(t) = V_c(\infty) + (V_c(0) - V_c(\infty)) e^{-\frac{t}{\tau}}$$

$$= V_s + \left(V_s \frac{R_{on}}{R_L + R_{on}} - V_s \right) e^{-\frac{t}{R_L C_L}}$$

$$I_s = I_c(t) = C_L \frac{dV_c}{dt} = \frac{V_s}{R_L} \left(1 - \frac{R_{on}}{R_L + R_{on}} \right) e^{-\frac{t}{R_L C_L}}$$

$$E_{low} = \int_0^T V_s I_s dt = \int_0^T V_s \cdot I_c(t) dt = \int_0^T \frac{V_s^2}{R_L} \left(1 - \frac{R_{on}}{R_L + R_{on}} \right) e^{-\frac{t}{R_L C_L}} dt$$

$$= V_s^2 \left(\frac{R_{on}}{R_L + R_{on}} - 1 \right) C \cdot e^{-\frac{T}{R_L C_L}} \int_0^T = C V_s^2 \left(\frac{R_{on}}{R_L + R_{on}} - 1 \right) \left(e^{-\frac{T}{R_L C_L}} - 1 \right)$$

Because $T \gg \tau$ $E_{low} = C V_s^2 \left(\frac{R_{on}}{R_L + R_{on}} \right) = \frac{V_s^2}{R_L + R_{on}} \cdot C \cdot R_L$

During the input is high

$$V_c(\infty) = V_s \cdot \frac{R_{on}}{R_L + R_{on}}, \quad V_c(0) = V_s, \quad \tau = (R_L || R_{on}) \cdot C_L$$

$$V_c(t) = V_s \left(\frac{R_{on}}{R_L + R_{on}} \right) + \left(V_s - V_s \frac{R_{on}}{R_L + R_{on}} \right) e^{-\frac{t}{\tau}}$$

$$I_s = \frac{V_s - V_c}{R_L} = \frac{V_s}{R_L} \left(1 - \left(\frac{R_{on}}{R_L + R_{on}} \right) \right) \cdot \left(1 - e^{-\frac{t}{\tau}} \right)$$

$$E_{high} = \int_0^T V_s I_s dt = \int_0^T \frac{V_s^2}{R_L} \left(1 - \frac{R_{on}}{R_L + R_{on}} \right) \left(1 - e^{-\frac{t}{\tau}} \right) dt$$

$$= \frac{V_s^2}{R_L} \left(1 - \frac{R_{on}}{R_L + R_{on}} \right) \left(t + \tau e^{-\frac{t}{\tau}} \right) \Big|_0^T = \frac{V_s^2}{R_L} \left(1 - \frac{R_{on}}{R_L + R_{on}} \right) \left(T + \tau e^{-\frac{T}{\tau}} - \tau \right)$$

Because $T \gg \tau$ $E_{high} = \frac{V_s^2}{R_L} \left(1 - \frac{R_{on}}{R_L + R_{on}} \right) \left(T - \frac{R_{on}}{R_L + R_{on}} \cdot \tau \right) = \frac{V_s^2}{R_L + R_{on}} \left(T - \frac{R_{on}}{R_L + R_{on}} \cdot \tau \right)$

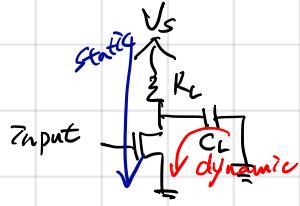
$$E_{total} = E_{high} + E_{low} = \frac{V_s^2}{R_L + R_{on}} \left(T - \frac{R_{on}}{R_L + R_{on}} \cdot C_L + C_L \cdot R_L \right) = \frac{V_s^2}{R_L + R_{on}} T + \left(\frac{R_L \cdot V_s}{R_L + R_{on}} \right)^2 \cdot C_L$$

$$\bar{P} = \frac{E_{total}}{2T} = \frac{V_s^2}{2(R_L + R_{on})} + \left(\frac{R_L \cdot V_s}{R_L + R_{on}} \right)^2 C_L \cdot \frac{1}{2T}$$

static dynamic

$$\therefore P_{static} = \frac{V_s^2}{2(R_L + R_{on})}, \quad P_{dynamic} = \frac{C_L}{2T} \left(\frac{R_L \cdot V_s}{R_L + R_{on}} \right)^2$$

C) Solution 2



$$E_{\text{static}} = \frac{V_s^2}{R_{\text{L}} t_{\text{RON}}} \cdot T$$

$$P_{\text{static}} = \frac{E_{\text{static}}}{2T} = \frac{V_s^2}{2(R_{\text{L}} t_{\text{RON}})}$$

$$P_{\text{dynamic}} = C_L f V_s^2 \left(\frac{R_L}{R_{\text{L}} + R_{\text{ON}}} \right)^2, \quad f = \frac{1}{2T}$$

$$\therefore P_{\text{static}} = \frac{V_s^2}{2(R_{\text{L}} t_{\text{RON}})}, \quad P_{\text{dynamic}} = \frac{C_L}{2T} \left(\frac{R_L V_s}{R_{\text{L}} + R_{\text{ON}}} \right)^2$$

- d) Assuming the input in part(c), by what factor does the dynamic power decrease if
 (i) T is increased by a factor of 2, (ii) V_s is decreased by a factor 2, and (iii) C_L is decreased by a factor 2?

$$P_{\text{dynamic}} \propto \left(\frac{1}{T} \cdot V_s^2 \cdot C_L \right)$$

\therefore

- i) $T \rightarrow 2T$. $P_{\text{dynamic}} = \frac{1}{2} P_{\text{dynamic}}$
- ii) $V_s \rightarrow \frac{1}{2} V_s$ $P_{\text{dynamic}} = \frac{1}{4} P_{\text{dynamic}}$
- iii) $C_L \rightarrow \frac{1}{2} C_L$ $P_{\text{dynamic}} = \frac{1}{2} P_{\text{dynamic}}$

- e) Suppose that the inverter must satisfy a static discipline with high and low voltage thresholds $V_{IH} = V_{OH} = V_H = V_{OL} = V_L$, respectively. You are given a MOSFET with on resistance R_{ON} and threshold V_T . Assume that $V_L < V_T < V_H < V_s$ choose a value for R_L in terms of the other circuit parameters such that the power consumed by the inverter is minimized.

Correct a typo $V_{IH} = V_{OH} = V_H$ and $V_{IL} = V_{IH} = V_L$

$$V_{OH}^* \geq V_{OH} \iff V_s \geq V_H \quad (\text{ok})$$

$$V_{IL}^* \geq V_{IL} \iff V_T \geq V_L \quad (\text{ok})$$

$$V_{IH}^* \leq V_{IH} \iff V_T \leq V_H \quad (\text{ok})$$

$$V_{OL}^* \leq V_{OL} \Rightarrow V_s \cdot \frac{R_{\text{on}}}{R_{\text{L}} + R_{\text{on}}} \leq V_L \Rightarrow R_{\text{on}} \left(\frac{V_s}{V_L} - 1 \right) \leq R_L$$

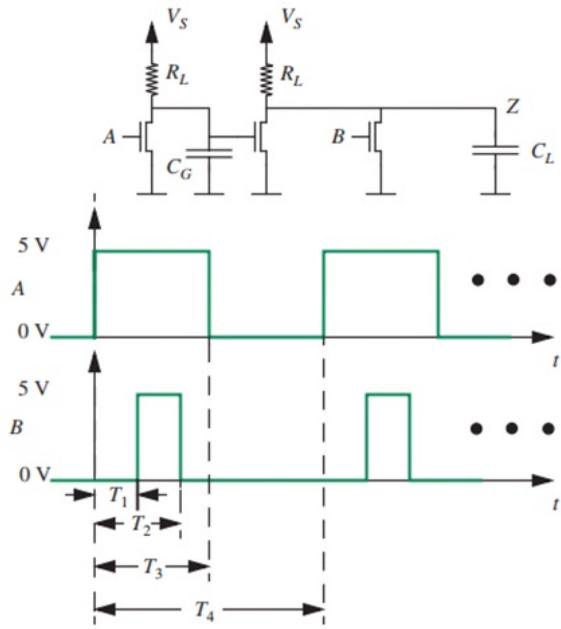
$$\text{Because } \bar{P} = \frac{V_s^2}{2(R_L + R_{\text{on}})} + \frac{C_L}{2T} \left(\frac{R_L V_s}{R_L + R_{\text{on}}} \right)^2$$

\bar{P} decreases when R_L increases.

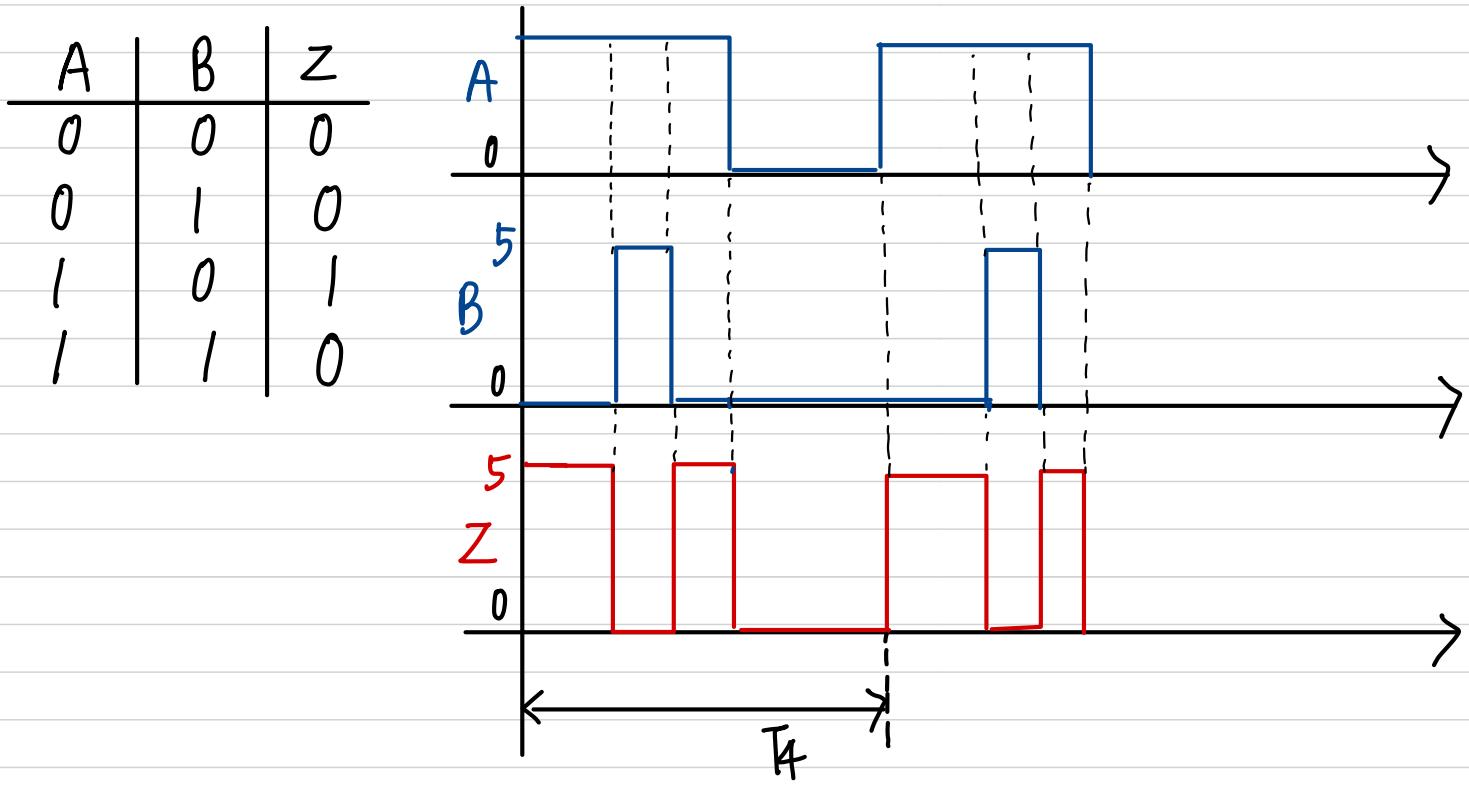
We can increase R_L without violating the static discipline.

Thus, if there is no limit to the inverter delay time, the power is minimized when $R_L = \infty$.

PROBLEM II.1 This problem examines the power dissipated by a small digital logic circuit. The circuit comprises a series-connected inverter and NOR gate as shown in Figure 11.29. The circuit has two inputs, A and B, and one output, Z. The inputs are assumed to be periodic with period T_4 as shown in Figure 11.29. Assume that R_{ON} for each MOSFET is zero.



- a) Sketch and clearly label the waveform for the output Z for $0 \leq t \leq T_4$. In doing so, assume that C_G and C_L are both zero.



- b) Derive the time-average static power consumed by the circuit in terms of V_S , R_L , T_1 , T_2 , T_3 and T_4 . Here, time-average power is defined as the total energy dissipated by the gate during the period $0 \leq t \leq T_4$ divided by T_4 .

$$i) 0 \leq t \leq T_1 : P_{\text{static}} = \frac{V_S^2}{R_L}$$

$$ii) T_1 \leq t \leq T_2 : P_{\text{static}} = 2 \cdot \frac{V_S^2}{R_L}$$

$$iii) T_2 \leq t \leq T_3 : P_{\text{static}} = \frac{V_S^2}{R_L}$$

$$iv) T_3 \leq t \leq T_4 : P_{\text{static}} = \frac{V_S^2}{R_L} \quad (\text{second MOSFET})$$

$$\therefore P_{\text{static,avg}} = \frac{T_1}{T_4} \left(\frac{V_S^2}{R_L} \right) + \frac{T_2-T_1}{T_4} \left(\frac{2V_S^2}{R_L} \right) + \frac{T_3-T_2}{T_4} \left(\frac{V_S^2}{R_L} \right) + \frac{T_4-T_3}{T_4} \left(\frac{V_S^2}{R_L} \right)$$

- c) Now assume that C_G and C_L are nonzero. Derive the time-average dynamic power consumed by the circuit in terms of V_S , R_L , C_G , C_L , T_1 , T_2 , T_3 and T_4 . In doing so, assume that the circuit time constants are all much smaller than T_1 , $T_2 - T_1$, $T_3 - T_2$ and $T_4 - T_3$.

$$T_4 \text{ ATRST } C_G \in 1\text{st charge-discharge} \rightarrow \frac{C_G V_S^2}{T_4}$$

$$(1 \in 2\text{nd charge-discharge} \rightarrow 2 \cdot \frac{C_L V_S^2}{T_4})$$

$$\therefore P_{\text{dynamic,avg}} = \frac{1}{T_4} (C_G V_S^2 + 2 C_L V_S^2)$$

- d) Evaluate the time-average static and dynamic powers for $V_S = 5 \text{ V}$, $R_L = 10 \text{ k}\Omega$, $C_G = 100 \text{ fF}$, $C_L = 1 \text{ pF}$, $T_1 = 100 \text{ ns}$, $T_2 = 200 \text{ ns}$, $T_3 = 300 \text{ ns}$ and $T_4 = 600 \text{ ns}$.

$$P_{\text{static. avg}} = \frac{V_S^2}{R_L + R_N} \left(\frac{-T_1 + T_2 + T_4}{T_4} \right)$$

$$= \frac{25}{10^4} \left(\frac{-100 + 200 + 600}{600} \right)$$

$$= \frac{175}{10^4 \times 6} = 2.9 \text{ mW}$$

$$P_{\text{dynamic. avg}} = \frac{1}{T_4} (C_G V_S^2 + 2 C_L V_S^2)$$

$$= \frac{1}{600 \times 10^{-9}} \left(100 \cdot 10^{-15} \cdot 25 + 2 \cdot 1 \cdot 10^{-12} \cdot 25 \right)$$

$$= \frac{1}{6 \cdot 10^{-7}} \left(25 \cdot 10^{-13} + 500 \cdot 10^{-13} \right)$$

$$= \frac{525}{6} \cdot 10^{-6}$$

$$= 87.5 \mu\text{W}$$

[Previous Exam]

Answer the following questions for the CMOS inverter with the following characteristics.

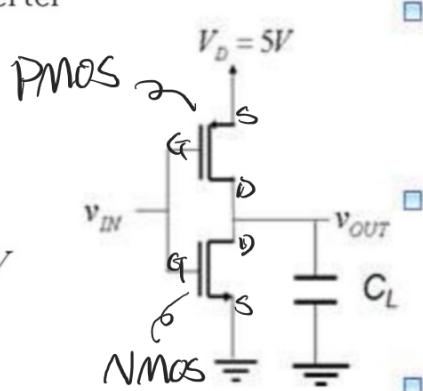
NMOS saturation current:

$$i_{Dn} = K_n (V_{GS} - V_{th})^2, K_n = 0.1 \text{mA/V}^2, V_{th} = 1.0 \text{V}$$

PMOS saturation current:

$$i_{Dp} = K_p (V_{S.G.} - |V_{th}|)^2, K_p = 0.1 \text{mA/V}^2, V_{th} = -1.0 \text{V}$$

$$C_L = 100 \text{pF}$$



- (a) Find the dynamic power consumption of this inverter when the input is changing with 1 GHz frequency.

$$(a) P_{\text{dynamic}} = \frac{1}{2} \cdot C \cdot V^2 \cdot f = \frac{1}{2} \cdot 100 \cdot 10^{-12} \cdot 5^2 \cdot 10^9 = 1.25 \text{W}$$

- (b) Find the input voltage to make both NMOS and PMOS transistors "saturated."

When both transistors are saturated, what would be the range of the output voltage of the inverter? (Hint: find the minimum output voltage to make NMOS saturated. Then find the maximum output voltage to make PMOS saturated (dual of NMOS case)).

(b) If both NMOS and PMOS are saturated,

$$i_{Dn} = i_{Dp} \rightarrow 0.1 (V_{IN} - 1)^2 = 0.1 (5 - V_{IN} - 1)^2$$

$$\therefore V_{IN} = 2.5 \text{V} \dots \textcircled{1}$$

NMOS saturation condition

$$V_{GS} \geq V_T, V_{GD} < V_T$$

$$V_{GS} = V_{IN}, V_{GD} = V_{IN} - V_{out}$$

$$\therefore V_{IN} \geq 1, V_{IN} - V_{out} < 1 \dots \textcircled{2}$$

PMOS saturation condition

$$V_{GS} \leq V_T, V_{GD} > V_T$$

$$V_{GS} = V_{IN} - 5, V_{GD} = V_{IN} - V_{out}$$

$$\therefore V_{IN} - 5 \leq -1, V_{IN} - V_{out} > -1 \dots \textcircled{3}$$

By \textcircled{1}, \textcircled{2}, \textcircled{3}, 1.5 < V_{out} < 3.5 (1.5 \leq V_{out} \leq 3.5 \text{ allowed})

(c) Using this information, sketch a voltage transfer characteristics of the CMOS inverter.



- ① NMOS cutoff, PMOS triode
- ② NMOS saturated, PMOS triode
- ③ Both NMOS and PMOS saturated
- ④ NMOS triode, PMOS saturated
- ⑤ NMOS triode, PMOS cutoff