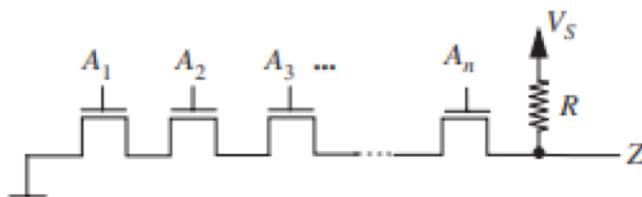


**PROBLEM 6.3** Consider a family of logic gates that operate under the static discipline with the following voltage thresholds:  $V_{OL} = 1 \text{ V}$ ,  $V_{IL} = 1.3 \text{ V}$ ,  $V_{OH} = 4 \text{ V}$ , and  $V_{IH} = 3 \text{ V}$ . Consider the N-input NAND gate design shown in Figure 6.63. In the design  $R = 100k$  and  $R_{ON}$  for the MOSFETs is given to be  $1k$ .  $V_T$  for the MOSFETs is  $1.5 \text{ V}$ . What is the maximum value of  $N$  for which the NAND gate will satisfy the static discipline? What is the maximum power dissipated by the NAND gate for this value of  $N$ ?



**Solution**

$$Z = \overline{A_1 \cdot A_2 \cdot \dots \cdot A_N}$$

# max  $V_z$ .

① if  $Z = 0$ , then  $V_z \leq V_{OL}$ .

$$\Rightarrow V_z = \frac{N \cdot R_m}{R + N \cdot R_{on}} \cdot V_s \leq V_{OL}$$

$$\Rightarrow \frac{N}{100 + N} \cdot V_s \leq 1$$

$$\Rightarrow N \leq \frac{100}{V_s - 1}$$

② if  $Z = 1$ , then  $V_s = V_z \geq V_{OH}$

$$\Rightarrow V_s \geq 4$$

from ① and ②  $N \leq \frac{100}{4-1}$ ,  $\therefore$  maximum  $N = 33$

# max power (with  $N=33$ )

$$4 \leq V_s, \quad 33 = N \leq \frac{100}{V_s - 1}$$

$$\Rightarrow 4 \leq V_s \leq \frac{133}{33}$$

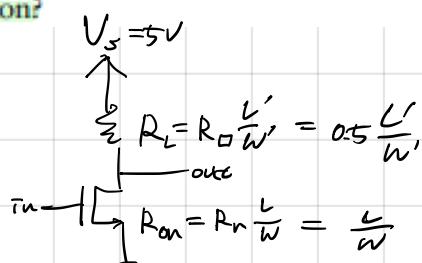
$$P = \frac{V_s^2}{R + N \cdot R_{on}} = \frac{V_s^2}{133}$$

$$\therefore \max P = \frac{\left(\frac{133}{33}\right)^2}{133} = \frac{133}{33^2} = \frac{133}{1089} \doteq 0.12 \text{ mW}$$

**PROBLEM 6.6** Consider a family of logic gates that operate under the static discipline with the following voltage thresholds:  $V_{OL} = 0.5$  V,  $V_{IL} = 1$  V,  $V_{OH} = 4.5$  V, and  $V_{IH} = 4.0$  V.

- b) Using the switch-resistor MOSFET model, design an inverter satisfying the static discipline for the four voltage thresholds using an n-channel MOSFET and a resistor. The MOSFET has  $R_n = 1\text{ k}\Omega$  and  $V_T = 1.8$  V. Recall,  $R_{ON} = R_n(L/W)$ . Assume  $V_S = 5$  V and  $R_\square$  for a resistor is  $500\ \Omega$ . Further assume that the area of the inverter is given by the sum of the areas of the MOSFET and the resistor. Assume that the area of a device is  $L \times W$ . The inverter should take as little area as possible with minimum size for  $L$  or  $W$  being  $0.5\ \mu\text{m}$ . Graph the input-output transfer function of the inverter. What is the total area of the inverter? What is its maximum static power dissipation?

**Solution**



$$\frac{R_{on}}{R_L + R_{on}} \cdot V_S \leq V_{OL}$$

$$\Rightarrow \frac{R_{on}}{R_L + R_{on}} \cdot 5 \leq 0.5$$

$$\Rightarrow 9 R_{on} \leq R_L$$

$$\Rightarrow 18 \frac{L}{w} \leq \frac{L'}{w'}$$

To minimize area,  $L = w' = 0.5\ \mu\text{m}$ .

$$18 \frac{L}{w} \leq \frac{L'}{w'}$$

$$\Rightarrow 18 \cdot (0.5)^2 \leq L'w \Rightarrow \frac{9}{2} \leq L'w$$

when  $L'w = \frac{9}{2}$ ,  $L' = w$ , the area of inverter is minimized.

$$\text{Thus, } L' = w = \frac{3}{\sqrt{2}}\ \mu\text{m}$$

$$\therefore \text{total area} = Lw + L'w' = 2 \cdot 0.5 \cdot \left(\frac{3}{\sqrt{2}}\right) = \frac{3}{\sqrt{2}} \doteq 2.12\ \mu\text{m}^2$$

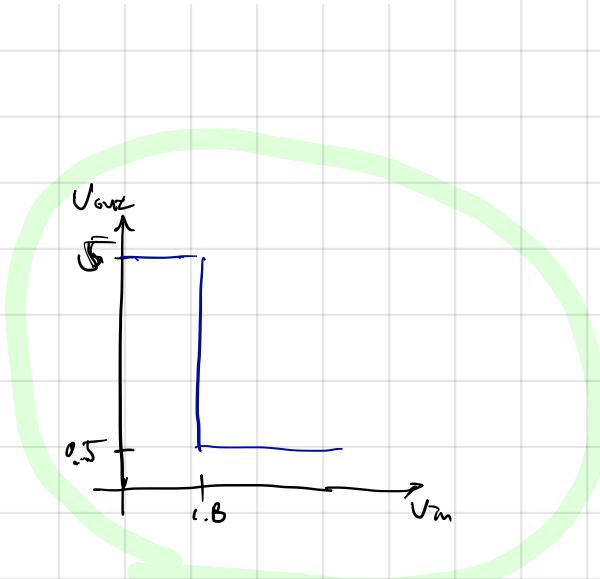
$$\text{Static power dissipation} = P_{\text{static}} = \frac{V_S^2}{R_L + R_{on}}$$

$$R_L = 0.5 \left( \frac{\frac{3}{\sqrt{2}}}{0.5} \right) = \frac{3}{\sqrt{2}}$$

$$R_{on} = \left( \frac{0.5}{\frac{3}{\sqrt{2}}} \right) = \frac{1}{2\sqrt{2}}$$

$$P_{\text{static}} = \frac{5^2}{\frac{3}{\sqrt{2}} + \frac{1}{2\sqrt{2}}}$$

$$\therefore P_{\text{static}} = \frac{25}{\sqrt{2}} \doteq 10.61\ \text{mW}$$



### Exercise 7.10 (a) (b)

**EXERCISE 7.10** In this exercise you will perform a large signal analysis of the BJT amplifier shown in Figure 7.72. Assume that the BJT is characterized by the large signal model from Exercise 7.8. Assume further that  $V_S = 5 \text{ V}$ ,  $R_L = 10 \text{ k}\Omega$ ,  $R_I = 500 \text{ k}\Omega$ , and  $\beta = 100$ .

- Write an expression relating  $v_O$  to  $v_I$ .
- What is the lowest value of the input voltage  $v_I$  for which the BJT operates in its active region? What are the corresponding values of  $i_B$ ,  $i_C$ , and  $v_O$ ?

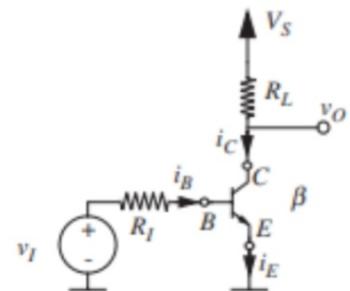


FIGURE 7.72

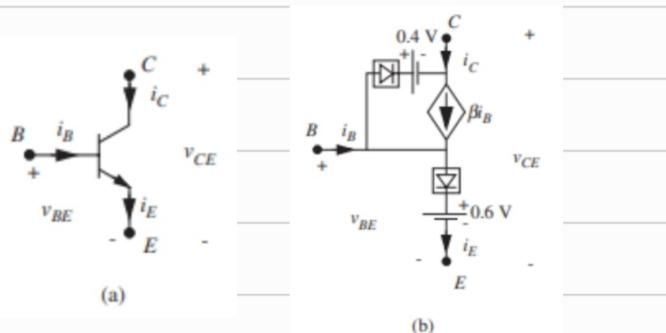


FIGURE 7.71 (a) A bipolar junction transistor. B stands for base, E for emitter, and C for collector; (b) a piecewise-linear model for the BJT.

(From Problem 7.8)

$i_B > 0$ ,  $V_{CE} > V_{BE} \sim 0.4 \text{ V}$  (active region)  
 $\Rightarrow$  The emitter diode behaves like a short circuit,  
 the collector diode like an open circuit, and  $i_C = 100i_B$

- Write an expression relating  $v_O$  to  $v_I$ .

Case 1.  $v_I \leq 0.6 \text{ V}$  (cutoff region)

In this case, clearly,  $i_B \leq 0$ .

Therefore, the BJT operates in cutoff region

$$\therefore v_O = V_S$$

Case 2.  $0.6 \text{ V} < v_I < 3 \text{ V}$  (active region)

Assume the BJT operates in active region.  
 Then, since the emitter diode is turned ON,

$$i_B = \frac{v_I - 0.6}{R_I} = \frac{v_I - 0.6}{500}$$

$$V_o = V_s - R_L \beta i_B$$

$$= 5 - 10 \cdot 100 \cdot \frac{V_I - 0.6}{500}$$

$$= 6.2 - 2V_I$$

Since  $V_o = V_{CE}$ ,  $V_o \geq 0.2V$ ,  $V_I < 3V$

Case 3.  $V_I \geq 3V$  (saturation region)

In this case, since the collector diode is turned ON,

$$V_o = V_{CE} = 0.2$$

In summary,

$$V_o = \begin{cases} V_s & \text{if } V_I \leq 0.6V \\ 6.2 - 2V_I & \text{if } 0.6V < V_I < 3V \\ 0.2 & \text{if } V_I \geq 3V \end{cases}$$

(b) What is the lowest value of the input voltage  $V_I$  for which the BJT operates in its active region? What are the corresponding values of  $i_B$ ,  $i_C$ , and  $V_o$ ?

The lowest value of  $V_I = 0.6V$

$$i_B = 0, i_C = 100 \cdot i_B = 0, V_o = 6.2 - 2 \times 0.6 = 5$$

**Problem 7.2** An inverting MOSFET amplifier is shown in Figure 7.12, together with an  $i_{DS}$ - $v_{DS}$  characteristic for the MOSFET. This characteristic is simpler than the SCS model presented in this chapter. The characteristic is simply the standard MOSFET characteristic with the triode region compressed onto the Y axis.

Alternatively, this characteristic can be viewed as describing ideal switch behavior that is extended to exhibit a saturating drain-source current. In other words, for  $v_{GS} < V_T$ , the MOSFET behaves like an open switch with  $i_{DS} = 0$ . For  $v_{GS} \geq V_T$ , the MOSFET behaves like a closed switch with  $v_{DS} = 0$  provided that  $i_{DS} < \frac{K}{2}(v_{GS} - V_T)^2$ . However, once  $i_{DS}$  reaches  $\frac{K}{2}(v_{GS} - V_T)^2$ , which is the maximum current the MOSFET can carry for a given  $v_{GS}$ , MOSFET operation enters a saturation region in which the MOSFET behaves as a current source of value  $\frac{K}{2}(v_{GS} - V_T)^2$ . Saturated operation is as described by the saturation model given in Figure 7.12.

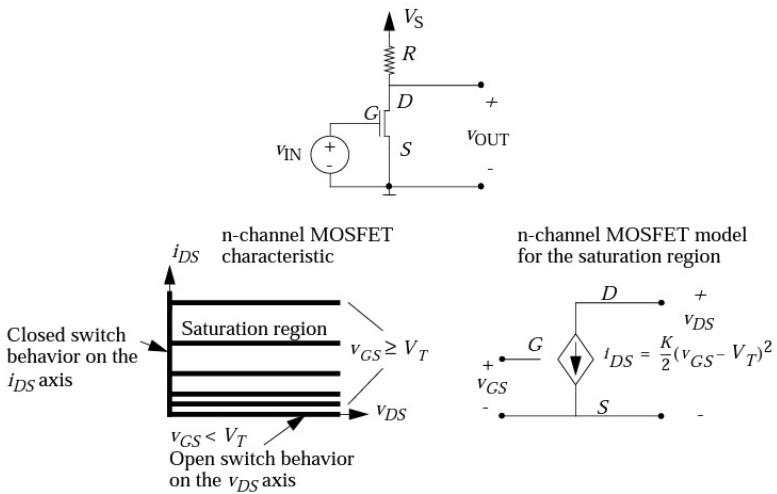


Figure 7.12:

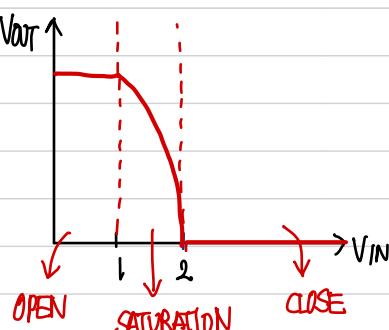
a) Determine  $v_{OUT}$  as a function of  $v_{IN}$  for  $0 \leq v_{IN}$ .

- i)  $v_{GS} < V_T \rightarrow i_{DS} = 0 \therefore V_{out} = V_S \quad \text{open}$
- ii)  $v_{GS} \geq V_T, i_{DS} = \frac{K}{2} \cdot (v_{GS} - V_T)^2 \therefore V_{out} = V_S - V_{DS} = V_S - R \cdot \frac{K}{2} \cdot (V_{IN} - V_T)^2 \quad \text{saturated}$
- iii)  $i_{DS}$  reaches  $V_S/R$  at specific voltage  $V^*$   $\therefore V_{out} = 0 \quad \text{closed}$

$$V_{out} = \begin{cases} V_S & (V_{IN} < V_T) \\ V_S - R \cdot \frac{K}{2} \cdot (V_{IN} - V_T)^2 & (V_T \leq V_{IN} < V^*) \\ 0 & (V^* \leq V_{IN}) \end{cases}$$

c) Assume that  $V_S = 15 \text{ V}$ ,  $R = 15 \text{ k}\Omega$ ,  $V_T = 1 \text{ V}$  and  $K = 2 \text{ mA/V}^2$ . Graph  $v_{OUT}$  versus  $v_{IN}$  for  $0 \text{ V} \leq v_{IN} \leq 3 \text{ V}$ .

$$V_{out} = \begin{cases} 15 & 0 \leq V_{IN} < 1 \\ 15 - 15(V_{IN} - 1)^2 & 1 \leq V_{IN} < 2 \\ 0 & 2 \leq V_{IN} \leq 3 \end{cases}$$



**Problem 7.14** Figure 7.28 shows a MOSFET amplifier driving a load resistor  $R_L$ . The MOSFET operates in saturation and is characterized by parameters  $K$  and  $V_T$ . Determine  $v_{\text{OUT}}$  versus  $v_{\text{IN}}$  for the circuit shown.

assume saturation. ( $V_{GS} \geq V_T$ ,  $V_{GD} \leq V_T$ ,  $V_{GS} - V_{DS} \leq V_T$ )

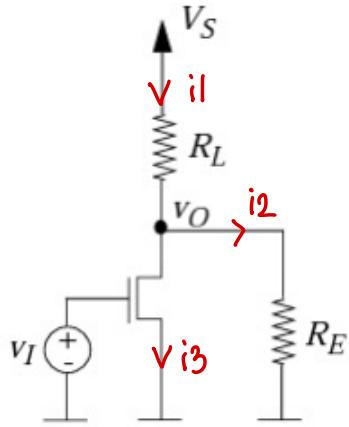


Figure 7.28:

$$i_1 = i_2 + i_3$$

$$V_o = V_s - R_L \cdot i_1 = i_2 \cdot R_E \rightarrow i_2 = \frac{V_o}{R_E}$$

$$i_3 = \frac{k}{2} (V_{IN} - V_T)^2 \quad // K(V_{IN} - V_T)^2 \text{로 풀어도 좋음.}$$

$$V_o = V_s - R_L \cdot i_1 = V_s - R_L (i_2 + i_3)$$

$$= V_s - R_L \left( \frac{V_o}{R_E} + \frac{k}{2} (V_{IN} - V_T)^2 \right)$$

$$\therefore V_o = \frac{V_s - \frac{k \cdot R_L}{2} (V_{IN} - V_T)^2}{1 + \frac{R_L}{R_E}} = \frac{2V_s \cdot R_E - k \cdot R_E \cdot R_L (V_{IN} - V_T)^2}{2(R_L + R_E)}$$

$$V_{IN} - V_o \leq V_T$$

$$V_{IN} - \frac{V_s R_E}{R_L + R_E} + \frac{k \cdot R_E \cdot R_L}{2(R_E + R_L)} (V_{IN} - V_T)^2 \leq V_T$$

$$(V_{IN} - V_T)^2 + \frac{2(R_E + R_L)}{k \cdot R_E \cdot R_L} (V_{IN} - V_T) - \frac{2V}{KR_L} \leq 0$$

근의 공식 적용.

$$\therefore V_T \leq V_{IN} \leq V_T - \frac{R_L + R_E}{KR_L R_E} + \sqrt{\frac{1}{K^2} \left( \frac{1}{R_L} + \frac{1}{R_E} \right)^2 + \frac{2V}{KR_L}}$$

### Problem 7.17

**PROBLEM 7.17** Determine  $v_o$  versus  $v_i$  for the circuit shown in Figure 7.88. Assume that the MOSFET operates in saturation and is characterized by the parameters  $K$  and  $V_T$ .

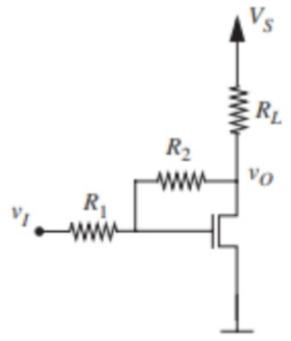


FIGURE 7.88

Since the MOSFET operates in saturation,

$$i_{DS} = \frac{K}{2} (V_{GS} - V_T)^2$$

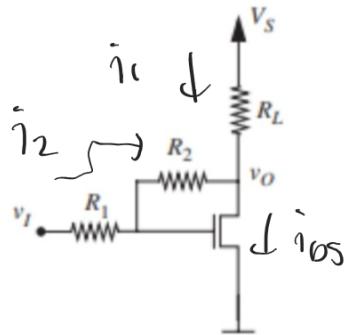
(Note: You may use  $K$  instead of  $K/2$ )

Let the current flowing through  $R_L$  be  $i_1$ , and the one flowing through  $R_1$  and  $R_2$  be  $i_2$  as follows:

Then, we get

$$i_1 = \frac{V_s - v_o}{R_L}, \quad i_2 = \frac{V_s - v_o}{R_1 + R_2}$$

$$V_{GS} = \frac{R_1 V_o + R_2 V_s}{R_1 + R_2}$$



By KCL, we get the equation  
for the relationship between  $v_i$  and  $v_o$ ,

$$i_1 + i_2 = i_{DS}$$

$$\frac{V_s - v_o}{R_L} + \frac{V_s - v_o}{R_1 + R_2} = \frac{k}{2} \left( \frac{R_1 V_o + R_2 V_s}{R_1 + R_2} - V_T \right)^2$$

$$(v_o \geq 0)$$

Bonus: We can get boundaries for  $V_o$  from the conditions for its saturation region.

$$V_{GS} \geq V_T \Rightarrow \frac{R_1 V_o + R_2 V_I}{R_1 + R_2} \geq V_T$$

$$\Rightarrow V_o \geq \frac{(R_1 + R_2) V_T - R_2 V_I}{R_1}$$

$$V_{DS} \geq V_{GS} - V_T \Rightarrow V_o \geq \frac{R_1 V_o + R_2 V_I}{R_1 + R_2} - V_T$$

$$\Rightarrow V_o \geq V_I - \frac{R_1 + R_2}{R_2} V_T$$

**PROBLEM 9.1** A voltage source is connected in series with two capacitors as shown in Figure 9.62. The source voltage is  $V(t) = 5 \text{ V } u(t)$ , as shown. If the current  $i$  and voltage  $v$  are given by  $i(t) = 4 \mu\text{C } \delta(t)$  and  $v(t) = 1 \text{ V } u(t)$ , again as shown, what are  $C_1$  and  $C_2$ ?

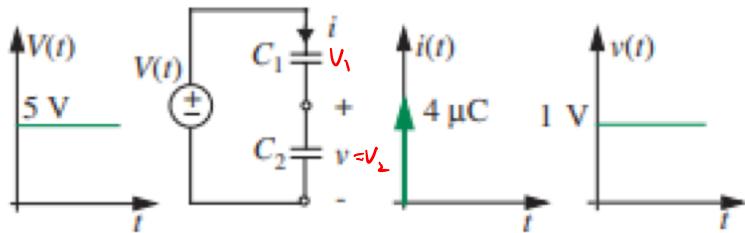


FIGURE 9.62

$$V_2 = V(t) = U(t)$$

$$\frac{dV_2}{dt} = S(t)$$

$$V_1 = V(-t) - V(t)$$

$$\frac{dV_1}{dt} = 4 \delta(t)$$

$$T(t) = T_1(t) = T_2(t) = 4 \mu\text{C} \delta(t)$$

$$T_2(t) = C_2 \cdot \frac{dV_2}{dt}$$

$$4 \mu\text{C} \delta(t) = C_2 \cdot S(t)$$

$$C_2 = 4 \mu\text{C}$$

$$T_1(t) = C_1 \frac{dV_1}{dt}$$

$$4 \mu\text{C} \delta(t) = C_1 U(t)$$

$$C_1 = 1 \mu\text{C}$$

$$\therefore C_1 = 1 \mu\text{C}, \quad C_2 = 4 \mu\text{C}$$

### Problem 9.4

**PROBLEM 9.4** A voltage source drives a parallel-connected capacitor and inductor as shown in Figure 9.65. Let  $V(t) = V_0 \sin(\omega t)u(t)$ , and assume that the inductor and capacitor both stored no energy prior to  $t = 0$ .

Determine the current  $i$  for  $t \geq 0$ .

Is there any relation between  $V_0$ ,  $\omega$ ,  $C$ , and  $L$  for which  $i$  is constant for  $t \geq 0$ ? If so, state the relation and determine  $i$ .

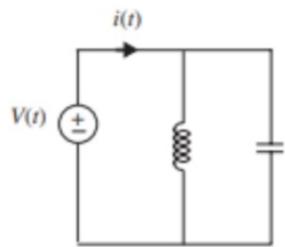
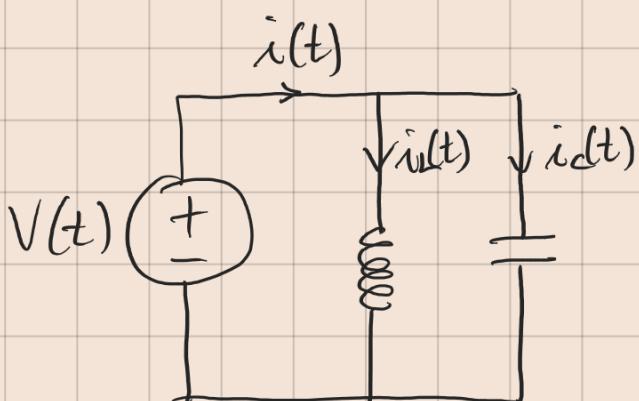


FIGURE 9.65



$$t \geq 0, V(t) = V_0 \sin(\omega t)$$

$$t < 0, V(t) = 0$$

$$i_C(t) = C \frac{dV(t)}{dt}$$

$$V(t) = L \frac{di_L(t)}{dt}$$

$$i_L(t) = \frac{1}{L} \int_{-\infty}^t V(u) du$$

$$\text{By KCL, } i(t) = i_C(t) + i_L(t)$$

$$\text{For } t \geq 0, i_C(t) = C \frac{dV_0 \sin(\omega t)}{dt} = \omega C V_0 \cos(\omega t)$$

$$i_L(t) = \frac{1}{L} \left[ \int_0^t 0 du + \int_0^t V_0 \sin(\omega u) du \right]$$

$$= -\frac{V_0}{\omega L} (\cos(\omega t) - 1)$$

$$\therefore i(t) = \omega C V_0 \cos(\omega t) - \frac{V_0}{\omega L} (\cos(\omega t) - 1)$$

$$= V_0 \left( \omega C - \frac{1}{\omega L} \right) \cos(\omega t) + \frac{V_0}{\omega L}$$

For  $i(t)$  to be constant for  $t \geq 0$ ,

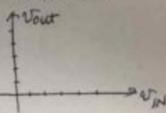
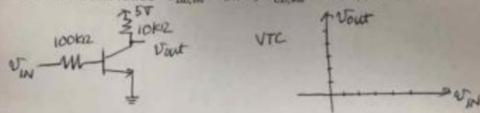
$$V_0 \left( \omega C - \frac{1}{\omega L} \right) = 0.$$

$$\therefore \text{If } \omega C - \frac{1}{\omega L} = 0 \Rightarrow \omega = \pm \sqrt{\frac{1}{LC}},$$

$i(t)$  becomes constant ( $i(t) = \pm V_0 \sqrt{\frac{C}{L}}$ )

1. [15 points] 다음 BJT 인버터 회로에 대해서 물음에 답하시오.

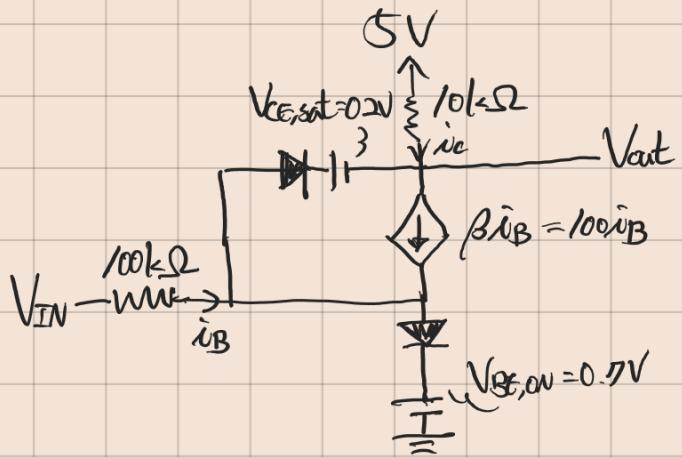
Bipolar transistor characteristics:  $V_{BE,ON} = 0.7 V$ ,  $V_{CE,sat} = 0.2 V$ ,  $\beta = 100$



(a) [10 points] Bipolar 회로의 VTC (Voltage transfer characteristics)를 도시하여라. Bipolar junction transistor 의 동작 영역이 바뀌는 부분을 정확히 명시하여라.

Draw the VTC (Voltage transfer characteristics) of the BJT(bipolar junction transistor) inverter. Specify the voltage levels when the BJT changes its operation region.

(b) [5 points] BJT inverter를 증폭기로 사용하는 경우의 전압비를 구하고 NMOS inverter 보다 증폭기로써 BJT 인버터가 더 좋은 이유를 설명하여라. Find the voltage gain when the BJT inverter is used as an amplifier and explain why it is better than the NMOS inverter as an amplifier.



$$(a) \textcircled{1} V_{IN} < V_{BE,ON} = 0.7 \text{ : cutoff}$$

$$\textcircled{2} V_{IN} \geq V_{BE,ON} = 0.7$$

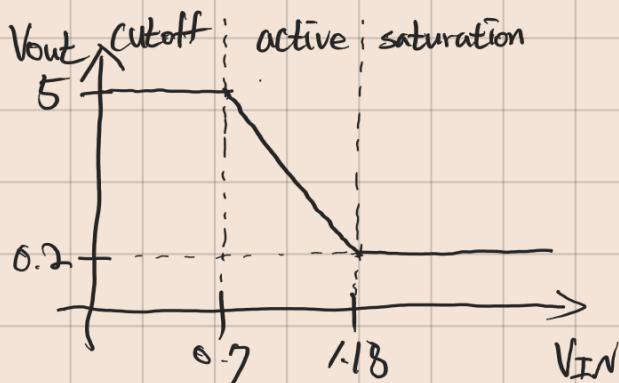
$$\bar{i}_B = \frac{V_{IN} - 0.7}{100}$$

$$i_C = \beta \bar{i}_B = 100 \bar{i}_B = V_{IN} - 0.7$$

$$= \frac{5 - V_{out}}{10} \text{ (in resistor } 10k\Omega \text{)}$$

$$\therefore V_{out} = 1/2 - 10V_{IN}$$

If  $V_{out} = V_{CE,sat} = 0.2 \Rightarrow V_{IN} = 1.18$ ,  
the BJT operates in saturation region.



$$(b) \text{ Voltage gain} : \frac{0.2 - 5}{1.18 - 0.7} = \frac{-4.8}{0.48} = -10. \quad (10 \text{ also allowed})$$

BJT inverter has greater voltage gain for amplification than NMOS inverter. And BJT has a linear VTC so it can amplify a wide range of input signal.