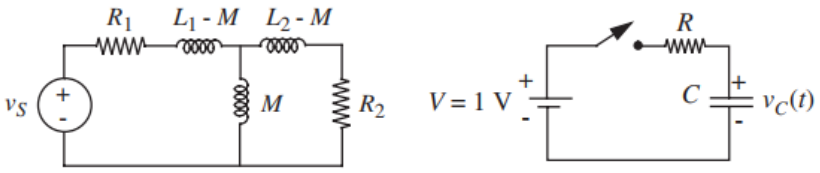
EXERCISE 10.11 In Figure 10.72, $R_1 = 1\ \text{k}\Omega$, $R_2 = 2\ \text{k}\Omega$, and $C = 10\ \mu F$. The driving voltage $v_S = 0$ for $t < 0$. Assume v_S is a 3-volt step at $t = 0$. Make a sketch of $v_C(t)$ for $t > 0$. Be sure to label the dimensions of the voltage and time axes and identify characteristic waveform shapes with suitable expressions.

FIGURE 10.72



PROBLEM 10.1 Figure 10.92a illustrates an inverter *INV*1 driving another inverter *INV*2. The corresponding equivalent circuit for the inverter pair is illustrated in Figure 10.92b. *A*, *B*, and *C* represent logical values, and v_A, v_B, and v_C represent voltage levels. The equivalent circuit model for an inverter based on the SRC model of the MOSFET is depicted in Figure 10.93.

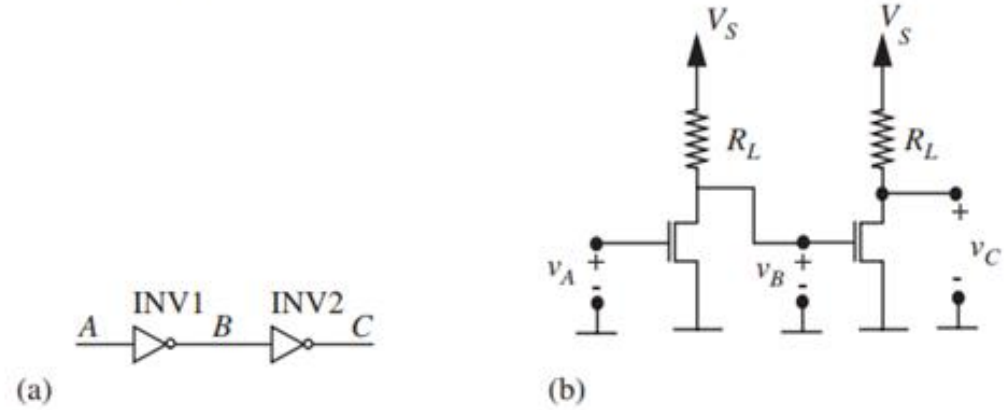


FIGURE 10.92

a) Write expressions for the rise and fall times of *INV*1 for the circuit configuration shown in Figure 10.92. Assume that the inverters satisfy the static discipline with voltage thresholds $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$.
(Hint: The rise time of *INV*1 is the time v_B requires to transition from the lowest voltage reached by v_B (given by the voltage divider action of R_L and R_{ON}) to V_H for a V_S to 0-V step transition at the input v_A. Similarly, the fall time of *INV*1 is the time v_B requires to transition from the highest voltage reached by v_B (that is, V_S) to V_L for a 0-V to V_S step transition at the input v_A.)

b) What is the propagation delay t_{pd} of *INV*1 in the circuit configuration shown in Figure 10.92, for $R_{ON} = 1\ \text{k}\Omega$, $R_L = 10R_{ON}$, $C_{GS} = 1\ \text{nF}$, $V_S = 5\ \text{V}$, $V_L = 1\ \text{V}$, and $V_H = 3\ \text{V}$?

PROBLEM 10.12 You can see from Problem 10.10 that for circuit time constant $\tau \gg t_1$ and t_2 the capacitor voltage starts from some value V_{min} and increases when v_S is positive; then when v_S is zero, v_O starts at some value V_{max} and decreases. By definition, the "steady state" of the circuit is when v_O charges from V_{min} to V_{max}, then discharges from V_{max} to the same V_{min}. Assuming $t_1 = t_2$, sketch the v_O waveform in the steady state.

Find the average value of the voltage v_O. Problem 10.11 may give you a hint. Explain your answer. It may help to consider the waveform v_S to be made up of a DC voltage $V/2$ and a symmetrical square wave whose values alternate between $+V/2$ and $-V/2$.

EXERCISE 11.1 An inverter built using an NMOS transistor and a resistor R_L drives a capacitance C_L. The power supply voltage is V_S and the on resistance of the MOSFET is R_{ON}. The threshold voltage for the MOSFET is V_T. Assume that logical 0's are represented using 0 V and logical 1's using V_S volts.

a) Determine the steady-state power consumed by the inverter when a 0 is applied to its input.

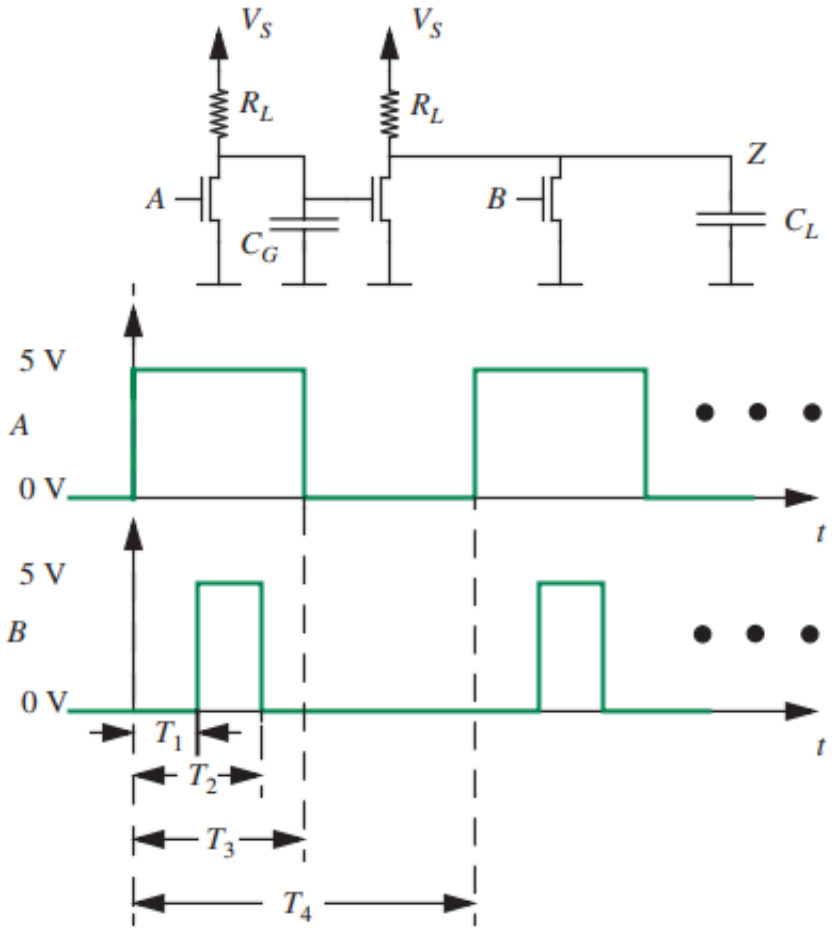
b) Determine the steady-state power consumed by the inverter when a 1 is applied to its input.

c) Determine the static power and the dynamic power consumed by the inverter when a sequence of the form 01010101 ... is applied to its input. Assume that signal transitions (0 to 1, or 1 to 0) happen every T seconds. Assume further than T is much greater than the circuit time constant.

d) Assuming the input in part(c), by what factor does the dynamic power decrease if (i) T is increased by a factor of 2, (ii) V_S is decreased by a factor 2, and (iii) C_L is decreased by a factor 2?

e) Suppose that the inverter must satisfy a static discipline with high and low voltage thresholds $V_{IH} = V_{OH} = V_H = V_{OL} = V_L$, respectively. You are given a MOSFET with on resistance R_{ON} and threshold V_T. Assume that $V_L < V_T < V_H < V_S$ choose a value for R_L in terms of the other circuit parameters such that the power consumed by the inverter is minimized.

PROBLEM 11.1 This problem examines the power dissipated by a small digital logic circuit. The circuit comprises a series-connected inverter and NOR gate as shown in Figure 11.29. The circuit has two inputs, A and B, and one output, Z. The inputs are assumed to be periodic with period T_4 as shown in Figure 11.29. Assume that R_{ON} for each MOSFET is zero.



a) Sketch and clearly label the waveform for the output Z for $0 \leq t \leq T_4$. In doing so, assume that C_G and C_L are both zero.

b) Derive the time-average static power consumed by the circuit in terms of V_S, R_L, T_1, T_2, T_3, and T_4. Here, time-average power is defined as the total energy dissipated by the gate during the period $0 \leq t \leq T_4$ divided by T_4.

c) Now assume that C_G and C_L are nonzero. Derive the time-average dynamic power consumed by the circuit in terms of V_S, R_L, C_G, C_L, T_1, T_2, T_3, and T_4. In doing so, assume that the circuit-time constants are all much smaller than T_1, $T_2 - T_1$, $T_3 - T_2$, and $T_4 - T_3$.

d) Evaluate the time-average static and dynamic powers for $V_S = 5$ V, $R_L = 10$ kΩ, $C_G = 100$ fF, $C_L = 1$ pF, $T_1 = 100$ ns, $T_2 = 200$ ns, $T_3 = 300$ ns, and $T_4 = 600$ ns.

[Previous Exam]

Answer the following questions for the CMOS inverter with the following characteristics.

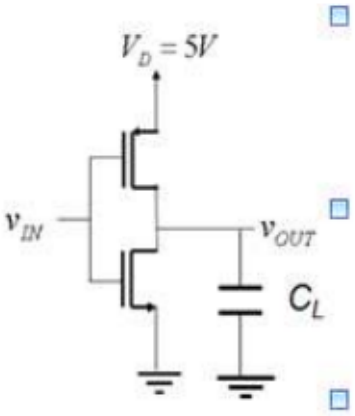
NMOS saturation current:

$i_{Dn} = K_n(V_{GS} - V_{th})^2,\ K_n = 0.1mA/V^2,\ V_{th} = 1.0\,V$

PMOS saturation current:

$i_{Dp} = K_{p.}(V_{S.G.} - |V_{th}|)^2,\ K_p = 0.1mA/V^2,\ V_{th} = -1.0\,V$

$C_L = 100pF$



(a) Find the dynamic power consumption of this inverter when the input is changing with 1 GHz frequency.

(b) Find the input voltage to make both NMOS and PMOS transistors "saturated." When both transistors are saturated, what would be the range of the output voltage of the inverter? (Hint: find the minimum output voltage to make NMOS saturated. Then find the maximum output voltage to make PMOS saturated (dual of NMOS case).

(c) Using this information, sketch a voltage transfer characteristics of the CMOS inverter.